Jameco Part Number 843868

National Semiconductor

June 2006

# LP2996
# DDR Termination Regulator

## General Description

The LP2996 linear regulator is designed to meet the JEDEC SSTL-2 specifications for termination of DDR-SDRAM. The device contains a high-speed operational amplifier to provide excellent response to load transients. The output stage prevents shoot through while delivering 1.5A continuous current and transient peaks up to 3A in the application as required for DDR-SDRAM termination. The LP2996 also incorporates a $V_{SENSE}$ pin to provide superior load regulation and a $V_{REF}$ output as a reference for the chipset and DIMMs.

An additional feature found on the LP2996 is an active low shutdown ($\overline{SD}$) pin that provides Suspend To RAM (STR) functionality. When $\overline{SD}$ is pulled low the $V_{TT}$ output will tri-state providing a high impedance output, but, $V_{REF}$ will remain active. A power savings advantage can be obtained in this mode through lower quiescent current.

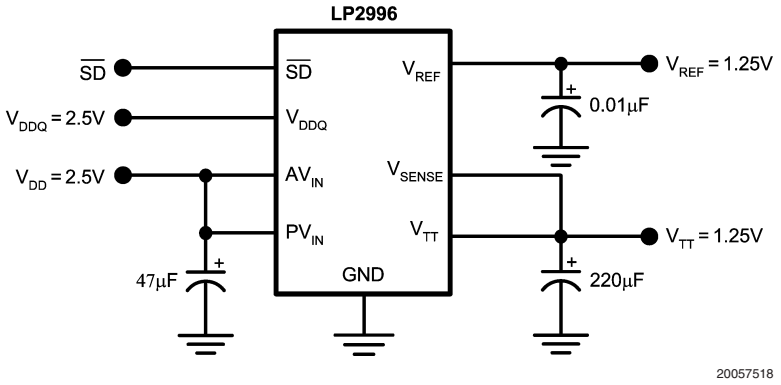
## Features

- Source and sink current
- Low output voltage offset
- No external resistors required
- Linear topology
- Suspend to Ram (STR) functionality
- Low external component count
- Thermal Shutdown
- Available in SO-8, PSOP-8 or LLP-16 packages

## Applications

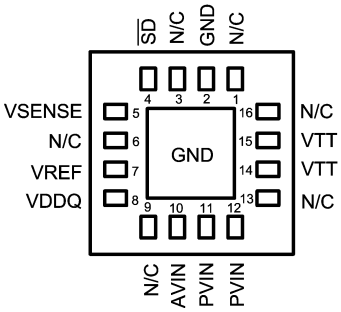
- DDR-I and DDR-II Termination Voltage
- SSTL-2 and SSTL-3 Termination
- HSTL Termination

## Typical Application Circuit



## Connection Diagrams

Top View

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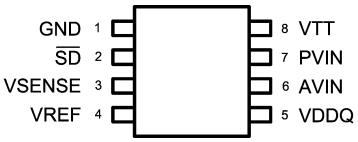
LLP-16 Layout

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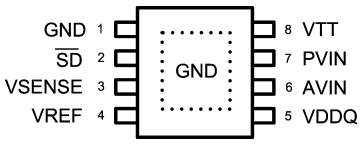
SO-8 Layout

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PSOP-8 Layout

## Pin Descriptions

| SO-8 Pin or PSOP-8 Pin | LLP Pin | Name | Function |
|---|---|---|---|
| 1 | 2 | GND | Ground |
| 2 | 4 | $\overline{SD}$ | Shutdown |
| 3 | 5 | VSENSE | Feedback pin for regulating $V_{TT}$. |
| 4 | 7 | VREF | Buffered internal reference voltage of $V_{DDQ}/2$ |
| 5 | 8 | VDDQ | Input for internal reference equal to $V_{DDQ}/2$ |
| 6 | 10 | AVIN | Analog input pin |
| 7 | 11, 12 | PVIN | Power input pin |
| 8 | 14, 15 | VTT | Output voltage for connection to termination resistors |
| - | 1, 3, 6, 9, 13, 16 | NC | No internal connection |
| | EP | EP | Exposed pad thermal connection. Connect to soft Ground. |

## Ordering Information

| Order Number | Package Type | NSC Package Drawing | Supplied As |
|---|---|---|---|
| LP2996M | SO-8 | M08A | 95 Units per Rail |
| LP2996MX | SO-8 | M08A | 2500 Units Tape and Reel |
| LP2996MR | PSOP-8 | MRA08A | 95 Units Tape and Reel |
| LP2996MRX | PSOP-8 | MRA08A | 2500 Units Tape and Reel |
| LP2996LQ | LLP-16 | LQA16A | 1000 Units Tape and Reel |
| LP2996LQX | LLP-16 | LQA16A | 4500 Units Tape and Reel |

## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | | | |
|---|---|---|---|
| PVIN, AVIN, VDDQ to GND | −0.3V to +6V | PSOP-8 Thermal Resistance ($\theta_{JA}$) | 43˚C/W |
| Storage Temp. Range | −65˚C to +150˚C | LLP-16 Thermal Resistance ($\theta_{JA}$) | 51˚C/W |
| Junction Temperature | 150˚C | Lead Temperature (Soldering, 10 sec) | 260˚C |
| SO-8 Thermal Resistance ($\theta_{JA}$) | 151˚C/W | ESD Rating (Note 2) | 1kV |

## Operating Range

| | | | |
|---|---|---|---|
| Junction Temp. Range (Note 3) | 0˚C to +125˚C | PVIN Supply Voltage | 0 to AVIN |
| AVIN to GND | 2.2V to 5.5V | SD Input Voltage | 0 to AVIN |

## Electrical Characteristics

Specifications with standard typeface are for $T_J$ = 25˚C and limits in **boldface type** apply over the full **Operating Temperature Range** ($T_J$ = 0˚C to +125˚C) (Note 4). Unless otherwise specified, AVIN = PVIN = 2.5V, VDDQ = 2.5V (Note 5).

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{REF}$ | $V_{REF}$ Voltage | VIN = VDDQ = 2.3V | **1.135** | 1.158 | **1.185** | |
| | | VIN = VDDQ = 2.5V | **1.235** | 1.258 | **1.285** | V |
| | | VIN = VDDQ = 2.7V | **1.335** | 1.358 | **1.385** | |
| $Z_{VREF}$ | $V_{REF}$ Output Impedance | $I_{REF}$ = -30 to +30 µA | | 2.5 | | kΩ |
| $V_{TT}$ | $V_{TT}$ Output Voltage | $I_{OUT}$ = 0A | | | | V |
| | | VIN = VDDQ = 2.3V | **1.125** | 1.159 | **1.190** | |
| | | VIN = VDDQ = 2.5V | **1.225** | 1.259 | **1.290** | |
| | | VIN = VDDQ = 2.7V | **1.325** | 1.359 | **1.390** | |
| | | $I_{OUT}$ = ±1.5A (Note 8) | | | | |
| | | VIN = VDDQ = 2.3V | **1.125** | 1.159 | **1.190** | |
| | | VIN = VDDQ = 2.5V | **1.225** | 1.259 | **1.290** | |
| | | VIN = VDDQ = 2.7V | **1.325** | 1.359 | **1.390** | |
| $Vos_{TT}/V_{TT}$ | $V_{TT}$ Output Voltage Offset ($V_{REF}$-$V_{TT}$) | $I_{OUT}$ = 0A | **-20** | 0 | **20** | mV |
| | | $I_{OUT}$ = -1.5A (Note 8) | **-25** | 0 | **25** | |
| | | $I_{OUT}$ = +1.5A (Note 8) | **-25** | 0 | **25** | |
| $I_Q$ | Quiscent Current (Note 6) | $I_{OUT}$ = 0A (Note 4) | | 320 | **500** | µA |
| $Z_{VDDQ}$ | VDDQ Input Impedance | | | 100 | | kΩ |
| $I_{SD}$ | Quiescent Current in Shutdown (Note 6) | SD = 0V | | 115 | **150** | µA |
| $I_{Q\_SD}$ | Shutdown Leakage Current | SD = 0V | | 2 | **5** | µA |
| $V_{IH}$ | Minimum Shutdown High Level | | **1.9** | | | V |
| $V_{IL}$ | Maximum Shutdown Low Level | | | | **0.8** | V |
| $I_V$ | $V_{TT}$ Leakage Current in Shutdown | SD = 0V<br>$V_{TT}$ = 1.25V | | 1 | **10** | µA |
| $I_{SENSE}$ | $V_{SENSE}$ Input Current | | | 13 | | nA |
| $T_{SD}$ | Thermal Shutdown | (Note 7) | | 165 | | Celcius |
| $T_{SD\_HYS}$ | Thermal Shutdown Hysteresis | | | 10 | | Celcius |

**Electrical Characteristics** Specifications with standard typeface are for $T_J$ = 25˚C and limits in **boldface type** apply over the full **Operating Temperature Range** ($T_J$ = 0˚C to +125˚C) (Note 4). Unless otherwise specified, AVIN = PVIN = 2.5V, VDDQ = 2.5V (Note 5). (Continued)

**Note 1:** Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating range indicates conditions for which the device is intended to be functional, but does not guarantee specific performance limits. For guaranteed specifications and test conditions see Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

**Note 2:** The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.

**Note 3:** At elevated temperatures, devices must be derated based on thermal resistance. The device in the SO-8 package must be derated at $\theta_{JA}$ = 151.2˚ C/W junction to ambient with no heat sink.

**Note 4:** Limits are 100% production tested at 25˚C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate National's Average Outgoing Quality Level (AOQL).

**Note 5:** VIN is defined as VIN = AVIN = PVIN.

**Note 6:** Quiescent current defined as the current flow into AVIN.

**Note 7:** The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J(MAX)}$, the junction to ambient thermal resistance, $\theta_{JA}$, and the ambient temperature, $T_A$. Exceeding the maximum allowable power dissipation will cause excessive die temperature and the regulator will go into thermal shutdown.

**Note 8:** $V_{TT}$ load regulation is tested by using a 10 ms current pulse and measuring $V_{TT}$.

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