LP2996-N, LP2996A DDR Termination Regulator

1 Features

- Minimum V_{DDQ}:
  - 1.8 V (LP2996-N)
  - 1.35 V (LP2996A)
- Source and Sink Current
- Low Output Voltage Offset
- No External Resistors Required for Setting Output Voltage
- Linear Topology
- Suspend to Ram (STR) Functionality
- Stable With Ceramic Capacitors With Appropriate ESR
- Low External Component Count
- Thermal Shutdown

2 Applications

- LP2996-N: DDR1 and DDR2 Termination Voltage
- LP2996A: DDR1, DDR2, DDR3, and DDR3L Termination Voltage
- FPGA
- Industrial and Medical PC
- SSTL-2 and SSTL-3 Termination
- HSTL Termination

3 Description

The LP2996-N and LP2996A linear regulators are designed to meet the JEDEC SSTL-2 specifications for termination of DDR-SDRAM. The device also supports DDR2, while LP2996A supports DDR3 and DDR3L VTT bus termination with V_{DDQ} minimum of 1.35 V. The device contains a high-speed operational amplifier to provide excellent response to load transients. The output stage prevents shoot through while delivering 1.5-A continuous current and transient peaks up to 3 A in the application as required for DDR-SDRAM termination. The LP2996-N and LP2996A also incorporate a VSENSE pin to provide superior load regulation and a VREF output as a reference for the chipset and DIMMs.

An additional feature found on the LP2996-N and LP2996A is an active-low shutdown ($\overline{SD}$) pin that provides Suspend To RAM (STR) functionality. When $\overline{SD}$ is pulled low the VTT output will tri-state providing a high impedance output, but VREF remains active. A power savings advantage can be obtained in this mode through lower quiescent current.

TI recommends the LP2998 and LP2998-Q1 devices for automotive applications and DDR applications that require operating at temperatures below zero.

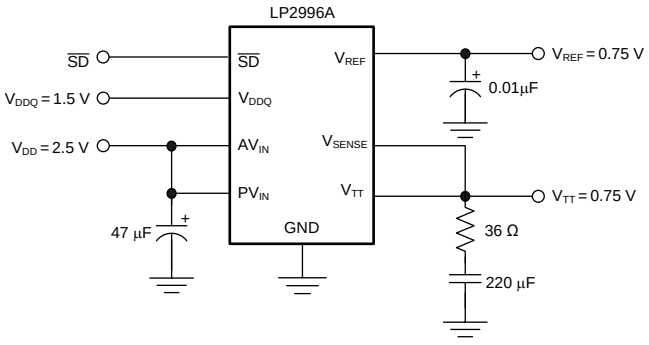
WEBENCH® design tools can be used by application designers to generate, optimize, and simlulate applications using the LP2998 and LP2998-Q1.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LP2996-N	SOIC (8)	4.90 mm x 3.90 mm
LP2996-N, LP2996A	WSON (8)	4.90 mm x 3.90 mm
LP2996-N	WQFN (16)	4.00 mm x 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision J (March 2013) to Revision K — **Page**

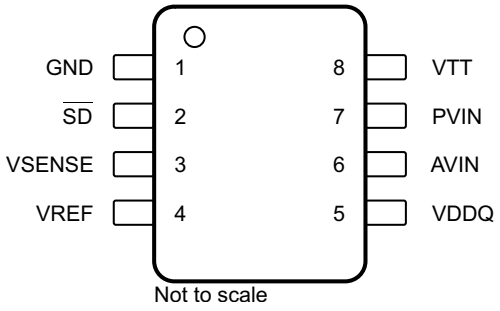
- Added *Device Information* table, *Specifications* section, *ESD Ratings* table, *Thermal Information* table, *Feature Description* section, *Device Functional Modes* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Added LP2996A throughout data sheet ... 1
- Added DDR3 support throughout data sheet ... 1
- Deleted Lead temperature (260°C maximum) from *Absolute Maximum Ratings* ... 5
- Changed Thermal Resistance, $R_{\theta JA}$, values in *Thermal Information* From: 151°C/W To: 119.5°C/W (SOIC), From: 151°C/W To: 56.5°C/W (SO), and From: 151°C/W To: 52.7°C/W (WQFN) ... 5

Changes from Revision I (March 2013) to Revision J — **Page**

- Changed layout of National Semiconductor Data Sheet to TI format ... 1
- Added V_{DDQ} Range ... 1

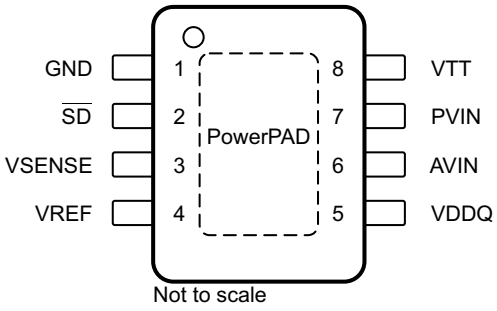
5 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



Not to scale

DDA Package
8-Pin SO With PowerPAD
Top View



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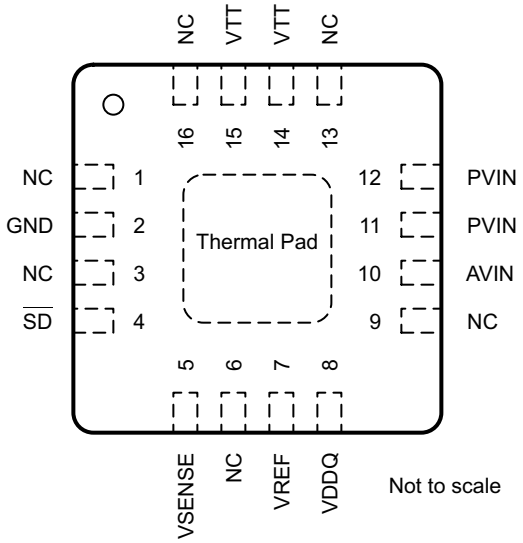
NHP Package
16-Pin WQFN
Top View



Not to scale

Pin Functions

PIN				I/O	DESCRIPTION
NAME	SO PowerPAD	SOIC	WQFN		
AVIN	6	6	10	I	Analog input pin. AVIN is used to supply all the internal control circuitry. This pin has the capability to work from a supply separate from PVIN depending on the application. For SSTL-2 applications, a good compromise would be to connect the AVIN and PVIN directly together at 2.5 V. This eliminates the requirement for bypassing the two supply pins separately. The only limitation on input voltage selection is that PV_{IN} must be equal to or lower than AV_{IN}.
GND	1	1	2	—	Ground
PVIN	7	7	11, 12	I	Power input pin. PVIN is used exclusively to provide the rail voltage for the output stage used to create VTT. This pin has the capability to work from a supply separate from PVIN depending on the application. Higher voltages on PVIN increases the maximum continuous output current because of output $R_{DS(ON)}$ limitations at voltages close to V_{TT}. The disadvantage of high values of PV_{IN} is that the internal power loss also increases, thermally limiting the design. For SSTL-2 applications, a good compromise would be to connect the AVIN and PVIN directly together at 2.5 V. This eliminates the requirement for bypassing the two supply pins separately. The only limitation on input voltage selection is that PV_{IN} must be equal to or lower than AV_{IN}. TI recommends connecting PVIN to voltage rails equal to or less than 3.3 V to prevent the thermal limit from tripping because of excessive internal power dissipation. If the junction temperature exceeds the thermal shutdown then the part enters a shutdown state identical to the manual shutdown where VTT is tri-stated and VREF remains active.

Pin Functions (continued)

PIN				I/O	DESCRIPTION
NAME	SO PowerPAD	SOIC	WQFN		
$\overline{SD}$	2	2	4	I	Shutdown. The LP2996-N and LP2996A contain an active low shutdown pin that can be used to tri-state VTT. During shutdown VTT must not be exposed to voltages that exceed AV_{IN}. With the shutdown pin asserted low the quiescent current of the LP2996-N and LP2996A drops, however, VDDQ always maintains its constant impedance of 100 kΩ for generating the internal reference. Therefore, to calculate the total power loss in shutdown, both currents must be considered. See *Thermal Considerations* for more information. The shutdown pin also has an internal pullup current, therefore to turn the part on, the shutdown pin can either be connected to AVIN or left open.
VDDQ	5	5	8	I	Input for internal reference equal to V_{DDQ} / 2. VDDQ is the input used to create the internal reference voltage for regulating V_{TT}. The reference voltage is generated from a resistor divider of two internal 50-kΩ resistors. This ensures that V_{TT} tracks V_{DDQ} / 2 precisely. The optimal implementation of VDDQ is as a remote sense. This can be achieved by connecting VDDQ directly to the 2.5-V rail at the DIMM instead of AVIN and PVIN. This ensures that the reference voltage tracks the DDR memory rails precisely without a large voltage drop from the power lines. For SSTL-2 applications V_{DDQ} is a 2.5-V signal, which creates a 1.25-V termination voltage at VTT. See *Electrical Characteristics* for exact values of V_{TT} over temperature.
VREF	4	4	7	O	Buffered internal reference voltage of V_{DDQ} / 2. VREF provides the buffered output of the internal reference voltage V_{DDQ} / 2. This output must be used to provide the reference voltage for the Northbridge chipset and memory. Because these inputs are typically an extremely high impedance, there must be little current drawn from VREF. For improved performance, an output bypass capacitor can be placed close to the pin to help reduce noise. TI recommends a ceramic capacitor from 0.1 µF to 0.01 µF. This output remains active during the shutdown state and thermal shutdown events for the suspend to RAM functionality.
VSENSE	3	3	5	I	Feedback pin for regulating V_{TT}. The purpose of the sense pin is to provide improved remote load regulation. In most motherboard applications the termination resistors connect to VTT in a long plane. If the output voltage was regulated only at the output of the device then the long trace causes a significant IR drop resulting in a termination voltage lower at one end of the bus than the other. The VSENSE pin can be used to improve this performance by connecting it to the middle of the bus. This provides a better distribution across the entire termination bus. If remote load regulation is not used then the VSENSE pin must still be connected to VTT. Take care when a long VSENSE trace is implemented in close proximity to the memory. Noise pickup in the VSENSE trace can cause problems with precise regulation of V_{TT}. A small 0.1-µF ceramic capacitor placed next to the VSENSE pin can help filter any high frequency signals and preventing errors.
VTT	8	8	14, 15	O	Output voltage for connection to termination resistors. VTT is the regulated output that is used to terminate the bus resistors. It is capable of sinking and sourcing current while regulating the output precisely to V_{DDQ} / 2. The LP2996-N and LP2996A are designed to handle peak transient currents of up to ±3 A with a fast transient response. The maximum continuous current is a function of V_{DD} and can be seen in *Typical Characteristics*. If a transient above the maximum continuous current rating is expected to last for a significant amount of time then the output capacitor must be large enough to prevent an excessive voltage drop. Despite the fact that the device is designed to handle large transient output currents it is not capable of handling these for long durations under all conditions. The reason for this is the standard packages are not able to thermally dissipate the heat as a result of the internal power loss. If large currents are required for longer durations, then ensure that the maximum junction temperature is not exceeded. Proper thermal derating must always be used (see *Thermal Considerations*). If the junction temperature exceeds the thermal shutdown point then VTT tri-states until the part returns below the hysteretic trip-point.
NC	—	—	1, 3, 6, 9, 13, 16	—	No internal connection
Thermal Pad	PowerPAD	—	Thermal Pad	—	Exposed pad thermal connection. Connect to Ground.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
AVIN to GND	−0.3	6	V
PVIN to GND	–0.3	AV_{IN}	V
Input voltage (VDDQ)(3)	−0.3	6	V
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) VDDQ voltage must be less than 2 × (AVIN – 1) or 6 V, whichever is smaller.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V

(1) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
	AVIN to GND	2.2	5.5	V
	PVIN supply voltage	0	AV_{IN}	V
	$\overline{SD}$ input voltage	0	AV_{IN}	V
T_J	Junction temperature(1)	0	125	°C

(1) At elevated temperatures, devices must be derated based on thermal resistance.

6.4 Thermal Information

THERMAL METRIC		LP2996-N, LP2996A			UNIT
		D (SOIC)	DDA (SO)	NHP (WQFN)	
		8 PINS	8 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	119.5	56.5	52.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	65.3	65.1	50.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	59.8	36.5	30.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	16.7	15.9	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	59.3	36.5	30.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	8.4	9.8	°C/W

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