Technical Note

Power Solutions for DDR2 Notebook PCs

In cooperation with TEXAS INSTRUMENTS

Overview

This technical note provides general guidelines for designing power circuitry for DDR2 memory. It includes the DDR2 voltage requirements and encompasses a sample reference design focused on the Texas Instruments Incorporated (TI) TPS51116, a complete DDR2 memory power solution that includes a synchronous buck controller, 3A linear dropout regulator (LDO), and buffered references.

DDR2 Advantages for Notebooks

DDR2 memory is an excellent solution for notebook computers. Aside from faster speeds, its greatest advantage over older memory technologies is its reduced power consumption, which results in cooler operating temperatures and extended battery life (see Figure 1 on page 2).

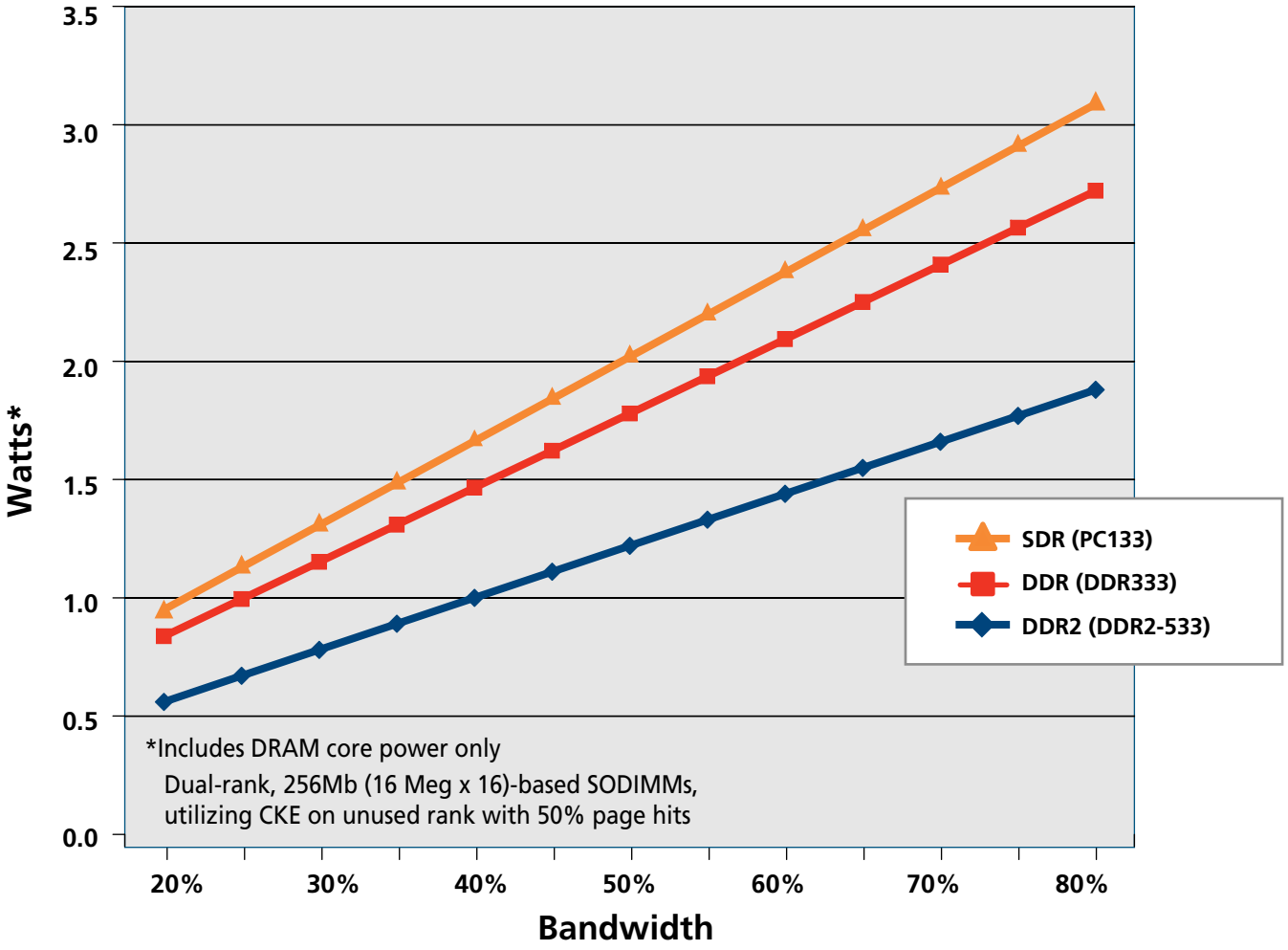
The reduced power consumption is realized through a number of design features, including lower operating voltages, reduced page sizes, and 4*n*-prefetch support. DDR2 memory uses a low operating voltage of only $V_{DD} = V_{DDQ} = 1.8V$ and supports an SSTL_18 I/O interface. The reduced page sizes minimize the activation current, and the 4*n*-prefetch architecture allows the device core to run at a slower frequency while driving an ultra-fast data rate (currently up to 1066 MT/s/b).

Another advantage of DDR2 memory in notebooks is higher density in the same space; aside from the voltage-key placement and pinout change, the DDR2 SODIMM uses the same 200-pin socket as DDR.

At the device level, DDR2 components are manufactured at individual memory densities up to 2Gb (at the component level, this reflects a 128Mb x 16 or 256Mb x 8 device), which means DDR2 supports a 4GB channel with just 2 slots.

Also new with DDR2 memory is on-die termination (ODT), which has a significant impact on signal quality and power dissipation. ODT gives the controller more effective management of termination to the high-speed signals where and when it is needed.

Figure 1: Power Performance Curves on SDR, DDR, and DDR2



DDR2 Notebook Assumptions

JEDEC has defined 4 standardized small outline, dual in-line memory modules (SODIMMs) that include single- and dual-rank DIMMs utilizing either x16 or x8 devices. All 4 configurations are 64-bit-wide unbuffered SODIMMs with predefined electrical and mechanical specifications.

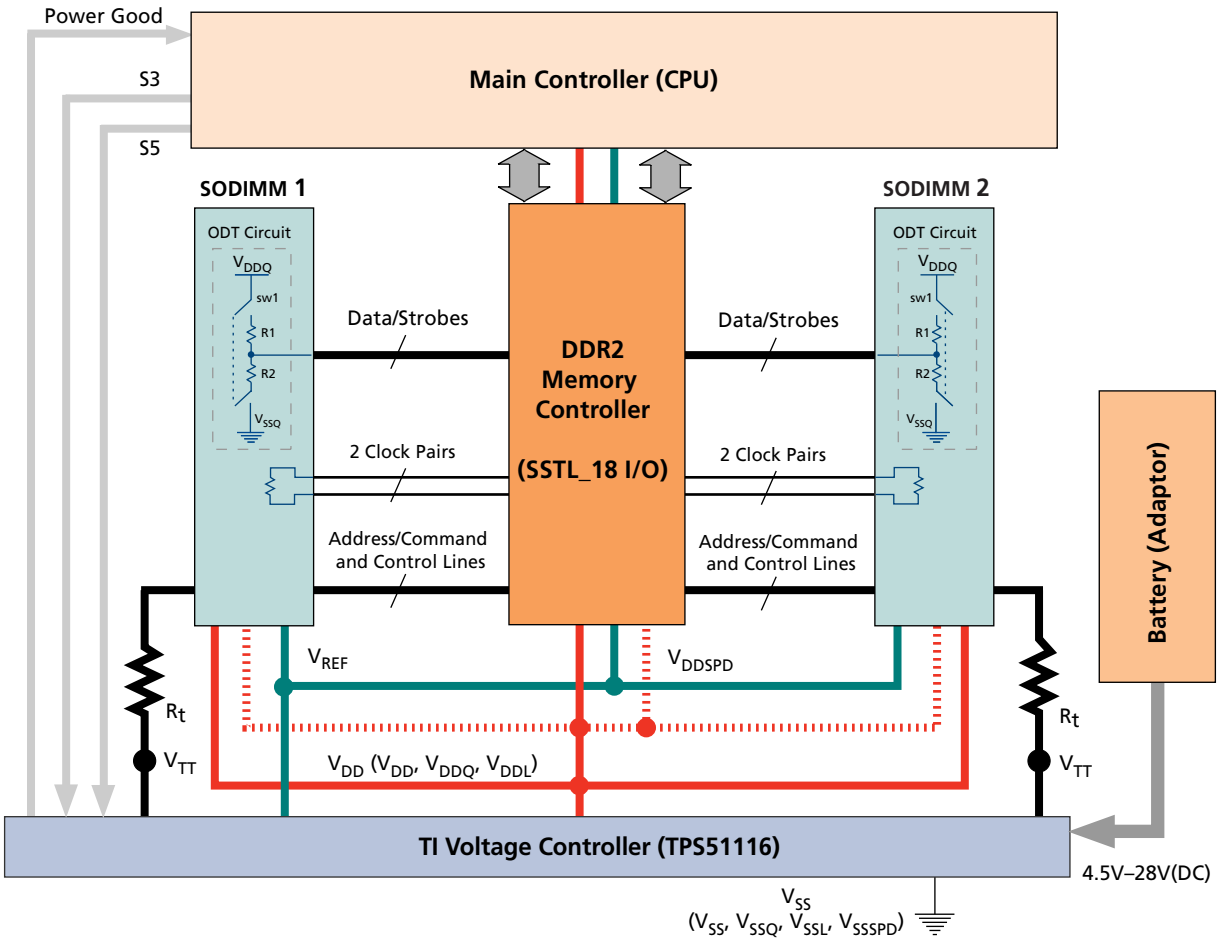
This technical note assumes that the notebook system designer will utilize a dual memory channel with 2 slots, 1 per channel (see Figure 2 on page 3). For a dual-channel, 2-slot system, both the address and command lines terminate at V_{TT} through a resistor. All the high-speed data strobes and data signals utilize localized ODT. On the module, the differential clock pairs (CK/CK#) are differentially terminated.

This combination makes for a low-cost, low-power application that maximizes battery life while maintaining a small size and high performance.

DDR2 Voltage Requirements

One challenge in designing a DDR2 system is meeting the strict power requirements and predefined power-up and initialization sequences as defined by JEDEC (JESD79-2 DDR2 SDRAM Specification). Therefore, it is critical that the initial power ramps be controlled to meet specifications. In addition, both the termination voltage (V_{TT}) and reference voltage (V_{REF}) must maintain their respected relationships to V_{DD} at all times. The following sections provide detailed voltage requirements for DDR2 notebook systems.

Figure 2: Functional Block Diagram of a Dual-Channel, 2-Slot DDR2 Notebook



Supply

V_{DD} (V_{DD}, V_{DDL}, V_{DDQ})

The DDR2 device requires a single power source for primary supply voltages in order to ensure that all voltage levels track each other, especially during the power ramp. At the module level, V_{DD} (device core), V_{DDL} (device DLL), and V_{DDQ} (device I/O) share a single power plane with the interconnecting pins labeled as V_{DD}. Likewise, V_{SS}, V_{SSL}, and V_{SSQ} share a common ground plane labeled as V_{SS}.

The memory supply voltage is specified as $V_{DD} = V_{DDQ} = 1.8V$ with a DC tolerance of ±100mV. DC is defined as any signal ≤20 MHz. At the initial power-up, all supply power should be stable and meet specification within ≤10ms.

The amount of current each module consumes depends on the density and speed of the module, number of ranks, and, most importantly, the usage conditions. For example, to build a high-density, dual-rank module using (x8) DRAMs, 16 individual devices are required. A system utilizing 2 of these modules and running a heavy-use condition may consume up to 7W–8W. However, the same system, using 1 lower-density, dual-rank module using (x16) DRAMs, will have only 8 discrete components each, and, under moderate use conditions, might consume a total of only 1.5W–2W.

Micron's Web site has a dedicated technical note, "TN-47-04: Calculating Memory System Power for DDR2," and a custom DDR2 power calculator that provide additional information about how to estimate actual module power usage at www.micron.com/systemcalc.

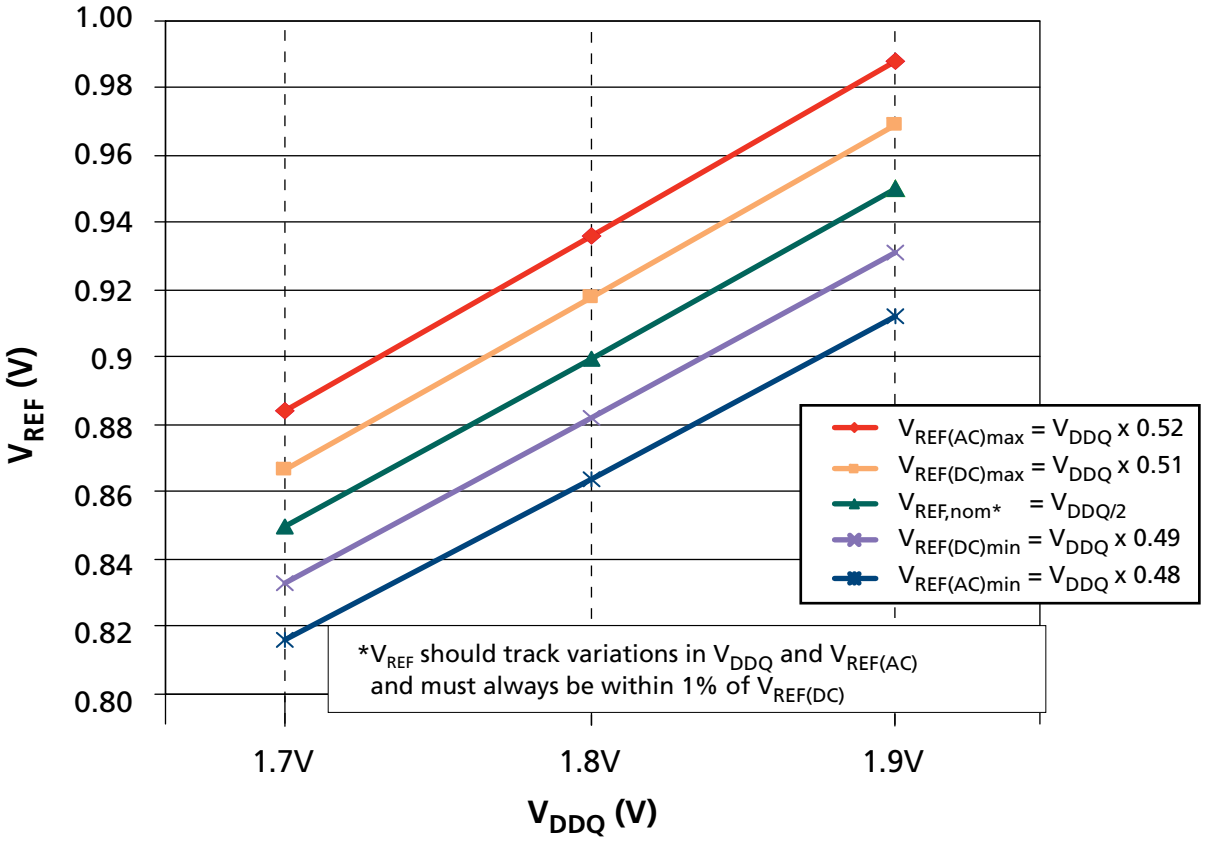
V_{REF}

Another key supply voltage is the input reference voltage (V_{REF}). All DDR2 input receivers are calibrated to operate within the specified V_{REF} input levels. For proper device operation, it is critical that the V_{REF} input is free from excess noise or voltage variations. Any degrading of the V_{REF} input voltage directly affects the setup and hold times of the DDR2 device.

V_{REF} is expected to equal $V_{DDQ/2}$ of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise (non-common mode) on V_{REF} may not exceed ±1% of the DC value. Peak-to-peak AC noise on V_{REF} must not exceed ±2% of $V_{REF(DC)}$. AC noise is defined as any noise over 20 MHz in frequency. There is virtually no current draw on the DDR2 V_{REF} pin; only leakage current is present (less than 5µA per DRAM component).

Figure 3 on page 5 shows the industry-standard voltage specifications and tracking requirements for V_{REF}

Figure 3: Required V_{REF} Voltage Relationships



V_{TT}

DDR2 memory is optimized for stub-series terminated logic at 1.8V (SSTL_18) operation. The address, command, and control lines require system-level termination to a midpoint voltage. This midpoint voltage is called V_{TT} (or the I/O termination voltage). Having the termination sit at midpoint ensures symmetry for switching times. It is important that V_{TT} tracks any variation in the DC levels of V_{REF}. By specification, at all times V_{TT} must equal V_{REF} ±40mV. The termination voltage (V_{TT}) is supplied directly to the motherboard but not to the module. See Figure 4 on page 6 for logic levels of a properly terminated SSTL_18 signal.

ODT (On-Die Termination)

As previously mentioned, DDR2's high-speed, bidirectional signals (data and strobes) are uniquely terminated with on-die termination (ODT). This new feature allows for optimal signal quality (see Figure 5 on page 6) by dynamically controlling the exact termination value where and when it is needed. For example, the ideal placement for termination is at the end of the active signal trace. So, when WRITING to SODIMM1, the memory controller dynamically disables the ODT function on SODIMM2 and the memory controller (both buses) and activates the ODT circuitry on SODIMM1 (at the end of the active transmission line). Likewise, during a READ from either SODIMM, the

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