Single-Inductor Multiple-Output Switching Converters With Time-Multiplexing Control in Discontinuous Conduction Mode

Dongsheng Ma, *Student Member, IEEE*, Wing-Hung Ki, *Member, IEEE*, Chi-Ying Tsui, *Member, IEEE*, and Philip K. T. Mok, *Senior Member, IEEE*

Abstract—An integrated single-inductor dual-output boost converter is presented. This converter adopts time-multiplexing control in providing two independent supply voltages (3.0 and 3.6 V) using only one 1-μH off-chip inductor and a single control loop. This converter is analyzed and compared with existing counterparts in the aspects of integration, architecture, control scheme, and system stability. Implementation of the power stage, the controller, and the peripheral functional blocks is discussed. The design was fabricated with a standard 0.5-μm CMOS n-well process. At an oscillator frequency of 1 MHz, the power conversion efficiency reaches 88.4% at a total output power of 350 mW. This topology can be extended to have multiple outputs and can be applied to buck, flyback, and other kinds of converters.

Index Terms—Cross regulation, discontinuous conduction mode (DCM), pulsewidth modulation (PWM), single-inductor dual-output (SIDO) converter, single-inductor multiple-output (SIMO) converter, time-multiplexing (TM) control.

I. INTRODUCTION

WITH THE proliferation of battery-operated portable applications such as personal digital assistants and mobile phones, minimizing power consumption becomes one of the most important design criteria. It has been shown that voltage scaling and effective power management are the most effective ways in reducing the power consumption for digital systems [1]. Recent works showed that having multiple supply voltages can further reduce the power consumption at different design abstraction levels [2]–[7]. In [3], an energy-efficient high-level scheduling and allocation algorithm exploiting multiple supply voltages was proposed. In [4], system-level memory power optimization technique using multiple supply voltages was discussed. Gate- and system-level power reduction techniques utilizing multiple supply voltages were presented in [5], [6], and [7]. In these works, it is assumed that multiple supply voltages are available on-chip. Yet, details of the supply voltage generation were not discussed. Traditional on-chip dc–dc converters only provide one supply voltage for the core of the chip [8]. These designs cannot be directly adapted to systems that require
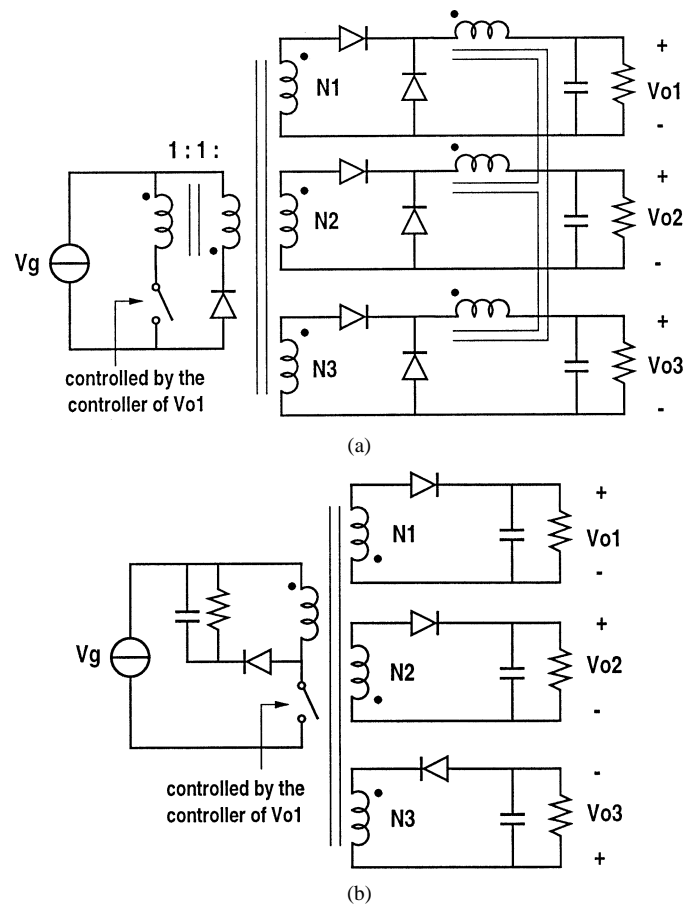

Fig. 1. Isolated multiple-output converters. (a) Forward converter. (b) Flyback converter.

multiple supply voltages. To reduce the number of power and ground pins and to have a clean power supply, an on-chip dc–dc converter that can provide multiple output voltages is desirable for these applications. In this paper, we address the issues of designing an on-chip single-inductor multiple-output (SIMO) dc–dc converter.

Conventional implementation of a dc–dc converter that has N output voltages may consist of N independent converters, or employ a transformer that has N secondary windings to distribute energy into the various outputs (isolated multiple-output converter) [Fig. 1(a) and 1(b)] [9], [10]. The first method requires too many components, including controllers and power devices, and this will increase the system cost. The second method does not allow individual outputs to be

The authors are with the Department of Electrical and Electronic Engineering, The Hong Kong University of Science and Technology, Hong Kong, China (e-mail: eemds@ee.ust.hk).
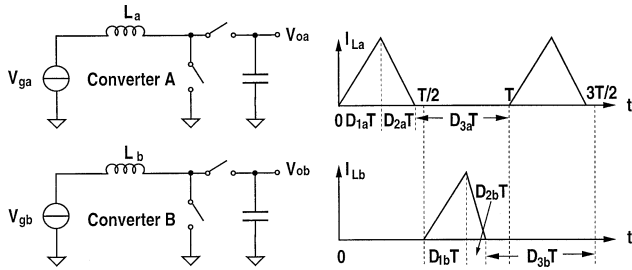
Fig. 2.   Two boost converters with interleaving inductor currents in DCM.

precisely controlled and has a big limitation for the applications of multiple voltage supply scaling. In addition, leakage inductance and cross coupling among windings cause a serious cross-regulation problem. Moreover, both methods require at least N inductors or windings, which may be too bulky and costly. In [11], a multiple-output architecture was proposed which combines the control loops of N converters into a single one. Multiple inductors are still needed and the reduction in external components is very small.

In this paper, we introduce a new single-inductor dual-output (SIDO) dc–dc converter [12]. Only a single inductor is required for providing two different output voltages. Using a novel time-multiplexing (TM) control scheme, the converter only needs one controller to regulate all the outputs. Compared with other designs, both on-chip and off-chip components are reduced significantly. Implementation issues such as synchronous rectification, controller design, current detection, dead-time buffer, and ringing suppression techniques are also addressed. The design of a SIDO boost converter has been fabricated using a standard 0.5-μm CMOS n-well process. Experimental results verify the validity of the design. The topology can easily be extended to give multiple outputs and to implement buck and flyback converter architectures. The remainder of the paper is organized as follows. Section II describes the basic architecture and control strategy of the proposed converter. Section III discusses the implementation details of the design. Section IV presents experimental results and Section V concludes our research efforts.

II. SIMO Boost Converter

A. Architecture and Control Strategy

Consider two conventional boost converters A and B working at the same switching frequency. If both converters are working in the discontinuous conduction mode (DCM), a possible scheme of their inductor currents could be as shown in Fig. 2. For Converter A, during $D_{1a}T$, the inductor current I_L ramps up and the inductor is charged with a voltage of $V_L = V_{ga}$, where D_{1a} is the duty ratio, T is the switching period and V_{ga} is the voltage of the source. During $D_{2a}T$, I_L ramps down with $V_L = -(V_{oa} - V_{ga})$, and during $D_{3a}T$, I_L stays zero. A similar scheme also applies to Converter B. Obviously, if $D_{1a} + D_{2a} \leq 0.5$ and $D_{1b} + D_{2b} \leq 0.5$, the two inductor currents can be alternately assigned to occupy different parts of the switching cycle without affecting each other. Hence, a SIDO converter can be obtained as shown in Fig. 3.
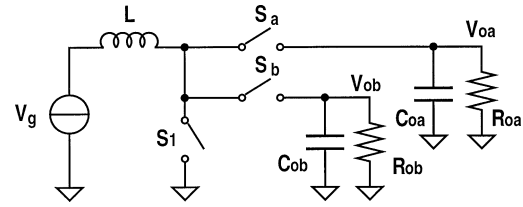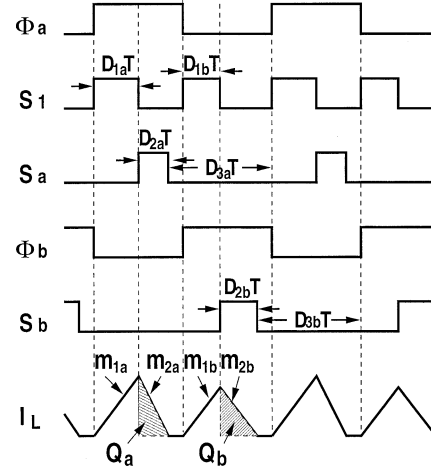

Fig. 3.   Proposed SIDO converter.

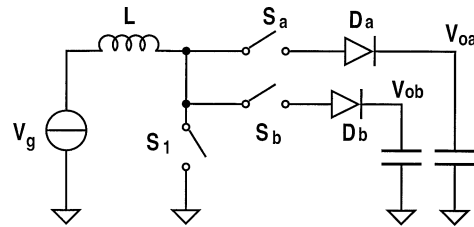Fig. 4.   Timing diagram of the SIDO converter.

Fig. 5.   Converter presented in [13].

scribed with reference to the timing diagram shown in Fig. 4. Let ϕ_a and ϕ_b be the complementary phases of the same duration. During $\phi_a = 1$, S_b is opened and no current flows into the output V_{ob}. Then, S_1 is closed first. The inductor current I_L increases until $D_{1a}T$ expires, which is determined by the output of an error amplifier. During $D_{2a}T$, S_1 is opened and S_a is closed to divert the inductor current into the output V_{oa}. A zero current detector senses the inductor current, and when it goes to zero, the converter enters $D_{3a}T$, and S_a is opened again. The inductor current stays zero until $\phi_b = 1$. Here, D_{1a}, D_{2a} and D_{3a} satisfy the requirements that

$$D_{1a} + D_{2a} \leq \frac{1}{2} \tag{1}$$
$$D_{1a} + D_{2a} + D_{3a} = 1. \tag{2}$$

During $\phi_b = 1$, the inductor current is multiplexed into the output V_{ob}. Similar switching action repeats for subconverter B and the two outputs are regulated alternately.

Similar switching converter topologies have also been reported [13]–[16]. However, in [13] and [14], power diodes are added in series with S_a and S_b to prevent the inductor current

efficiency significantly, which is unacceptable for low-voltage applications. The converter in [13] works at the boundary of continuous conduction mode (CCM) and DCM and the converter in [15] works in CCM. Both of the converters suffer serious cross regulation (Section II-C). [14] shows three control schemes, all of which employ hysteretic control. For the first scheme, if both outputs drop at the same time, only one output could be charged up immediately, while the other has to wait until the first output surpasses its upper bound voltage. If a large load change occurs at the second output during this "dead-time" period, its voltage drop could be tremendous and lead to a very large ripple voltage. In the worst case, the converter may fail to be regulated. For the second and third schemes, if the converter operates in CCM, cross-regulation problem occurs as in [13] and [15]. The design in [16] is, in fact, a special case of [14]. Therefore, it suffers similar problems on large load changes and cross regulation. In addition, since the error signals are extracted based on the differential and common mode voltages of the two outputs, the converter requires two control loops.

B. Design Considerations

Next, our proposed converter is considered. Let the conversion ratio of subconverter A be $M_a = V_{oa}/V_g$. Volt-second balance of subconverter A gives

$$V_g D_{1a} = (V_{oa} - V_g) D_{2a}. \qquad (3)$$

The conversion ratio is thus given by

$$M_a = \frac{V_{oa}}{V_g} = 1 + \frac{D_{1a}}{D_{2a}}. \qquad (4)$$

For a boost converter, the load current is equal to the averaged diode current. Hence, from Fig. 4, a routine analysis gives

$$I_{oa} = \frac{V_g}{2L} \frac{D_{1a}^2}{(M_a - 1) f_s} \qquad (5)$$

where f_s is the switching frequency. The average power of subconverter A is given by

$$P_{oa} = V_{oa} I_{oa} = \frac{V_g^2}{2L} \frac{D_{1a}^2 M_a}{(M_a - 1) f_s}. \qquad (6)$$

Maximum power occurs when $D_{1a} + D_{2a} = 1/2$, and subconverter A works at the boundary of DCM and CCM. The maximum duty ratio, maximum load current, and maximum power are then given by

$$D_{1a(\max)} = \frac{M_a - 1}{2M_a} \qquad (7)$$

$$I_{oa(\max)} = \frac{V_g}{2L} \frac{(M_a - 1)}{4M_a^2 f_s} \qquad (8)$$

$$P_{oa(\max)} = V_{oa} I_{oa(\max)} = \frac{1}{8M_a (M_a - 1) f_s} \frac{V_g^2}{L}. \qquad (9)$$

Similar results apply to subconverter B. The total output power $P_o (= P_{oa} + P_{ob})$ is less than $P_{o(\max)}$, where
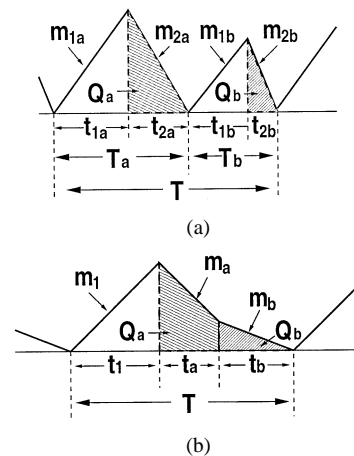
$$P_{o(\max)} = P_{oa(\max)} + P_{ob(\max)}$$

Fig. 6.   (a) Inductor current in the first scheme of [13]. (b) Inductor current in the second scheme of [13].

C. Cross Regulation

For a multiple-output converter with stable outputs, each output should be independently regulated. If the output voltage of a subconverter is affected by the change of load of another subconverter, cross regulation occurs. In the worst case, the overall converter could become unstable. The following discussion compares the performance of the control schemes in [13] with our suggested scheme.

The two control schemes in [13] require the converter to operate at the boundary of CCM and DCM (Fig. 6). For the first scheme, the inductor current assumes the form as shown in Fig. 6(a), with $D_{3a}T = t_{1b} + t_{2b}$. Depending on the load, in general, T_a is not equal to T_b, and the converter does not operate with a fixed switching frequency. Moreover, analysis shows that

$$t_{1b} = \sqrt{\frac{M_b (M_b - 1) R_{oa}}{M_a (M_a - 1) R_{ob}}} \cdot t_{1a} \qquad (11)$$

while R_{oa} and R_{ob} are the equivalent load resistances at the two outputs, respectively. This means that t_{1a} and t_{1b}, as well as T_a and T_b, are interdependent. The consequence is that a load change at the output V_{oa} will affect not only T_a, but also T_b at the same time, and, thus, cross regulation occurs.

For the second scheme, the inductor current is charged to a peak value. It is then discharged into V_{oa} for a duration of t_a, before the inductor current reaches zero. The remaining charge is then transferred to V_{ob} during t_b until the inductor current is zero. The relationship between t_a and t_b is given by

$$t_b = \frac{R_{oa}}{R_{ob}} \left[\frac{M_b (M_a - 1)}{M_a (M_b - 1)} t_a^2 + \frac{2}{M_a} t_a \right]. \qquad (12)$$

Again, the subconverters run at a variable switching frequency according to the loads, and the interdependence of t_a and t_b causes severe cross regulation between the two outputs. Analysis on the design in [14] gives similar results.

Different from the above, the proposed SIDO converter employs TM control and works in the DCM. The converter switches at a fixed frequency and the inductor current goes to
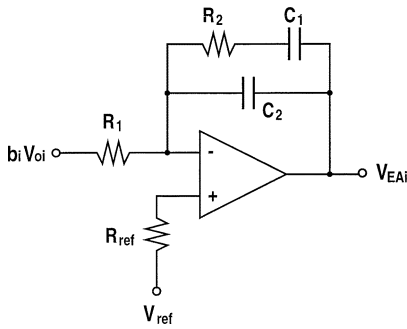
Fig. 7.   Error amplifier with pole-zero compensation.

Fig. 8.   Frequency responses of the converter with pole-zero compensation.

the energy transfer for V_{ob} will remain unaffected. In fact, D_{1a} is given by

$$D_{1a} = \sqrt{\frac{2M_a\left(M_a - 1\right)L}{R_{oa}T}} \qquad (13)$$

which depends only on R_{oa} and not on R_{ob}. Hence, the converter does not exhibit cross regulation.

D. Loop Gain Analysis and Compensation

Since subconverters A and B are decoupled from each other, they can be considered as two independent converters. Without going into the arguments of modeling, we make use of the result derived in [17]–[19], which is accurate enough for our purpose. The loop gain of subconverter i, with $i = a, b$, is given by

$$\begin{aligned}
T_i(s) &= A_i(s) \cdot h_i(s) \\
&= A_i(s)b_i \frac{2V_{oi}}{V_m\left(2M_i - 1\right)}\sqrt{\frac{M_i - 1}{K_i M_i}} \\
&\quad \cdot \frac{1 + sR_{ESRi}C_{oi}}{1 + s\dfrac{M_i - 1}{2M_i - 1} \cdot R_{oi}C_{oi}}
\end{aligned} \qquad (14)$$

where $A_i(s)$ is the gain of the error amplifier, which consists of the op-amp and the compensation network, $h_i(s)$ is the control-to-output transfer function, b_i is the scaling factor, $K_i = 2L/(R_{oi}T)$, V_m is the peak-to-peak voltage of the oscillator ramp, C_{oi} is the filtering capacitance, R_{ESRi} is the equivalent series resistance (ESR) of C_{oi}, and R_{oi} is the equivalent load resistance.

The low-frequency pole at $-(2M_i - 1)/((M_i - 1)R_{oi}C_{oi})$ moves as R_{oi} changes. The strategy of compensation is to ensure that the converter would be stable for all possible load changes. By using the pole-zero compensation network shown in Fig. 7, the corresponding transfer function, assuming an infinity gain of the op-amp, is

$$\begin{aligned}
A_i(s) &= \frac{1 + sC_2R_2}{s\left(C_1 + C_2\right)R_1\left[1 + s\left(C_1\|C_2\right)R_2\right]} \\
&= \frac{1 + \dfrac{s}{2\pi f_{z-ea}}}{s\left(C_1 + C_2\right)R_1\left(1 + \dfrac{s}{2\pi f_{p-ea}}\right)}
\end{aligned} \qquad (15)$$

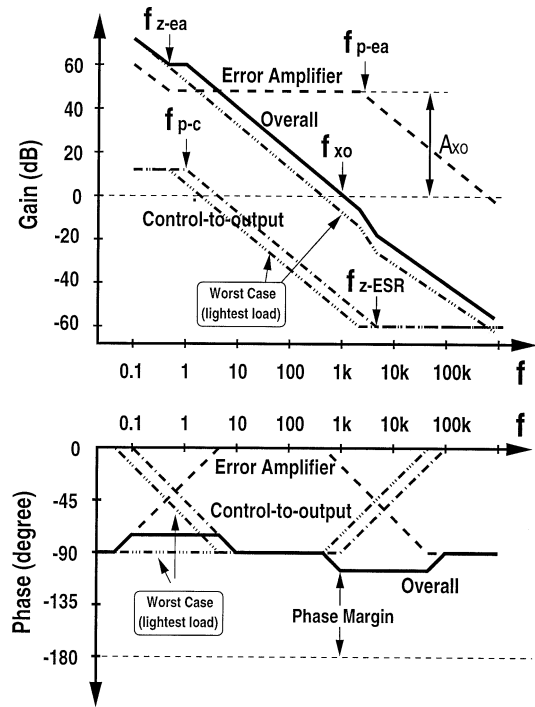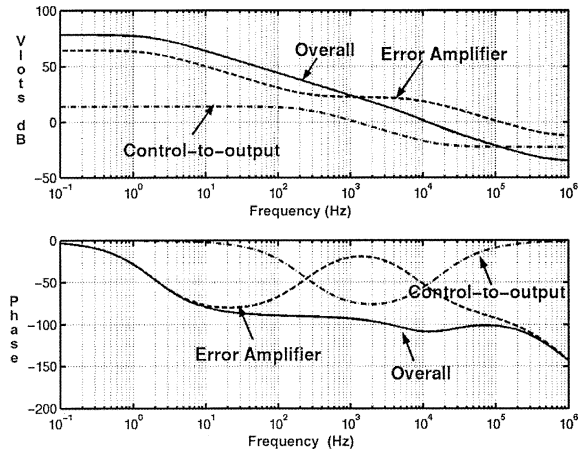which has a first pole at 0, a zero at $-1/(C_2R_2)$, and a second

Fig. 9.   Simulated frequency responses of the proposed converter.

shown in Fig. 8. The control-to-output transfer function $h_i(s)$ changes as R_{oi} changes (Fig. 8), and combines with $A_i(s)$ to give the overall loop gain $T_i(s) = A_i(s)h_i(s)$ (Fig. 8). To ensure stability in the worst case, the zero f_{z-ea} introduced by C_1 and R_2 is placed at the lowest possible pole frequency of f_{p-c} ($= ((2M_i - 1)/(2\pi(M_i - 1)R_{oi}C_{oi}))$) in (14), which corresponds to the lightest load, i.e., when the load resistance is the largest. The high-frequency pole f_{p-ea} of the compensation network caused by C_2 and R_2 is placed at the frequency of the zero f_{z-ESR} ($= (1/(2\pi R_{ESRi}C_{oi}))$ in the control-to-output response curve caused by the ESR of the filtering capacitor. Hence, the values of the components are given by

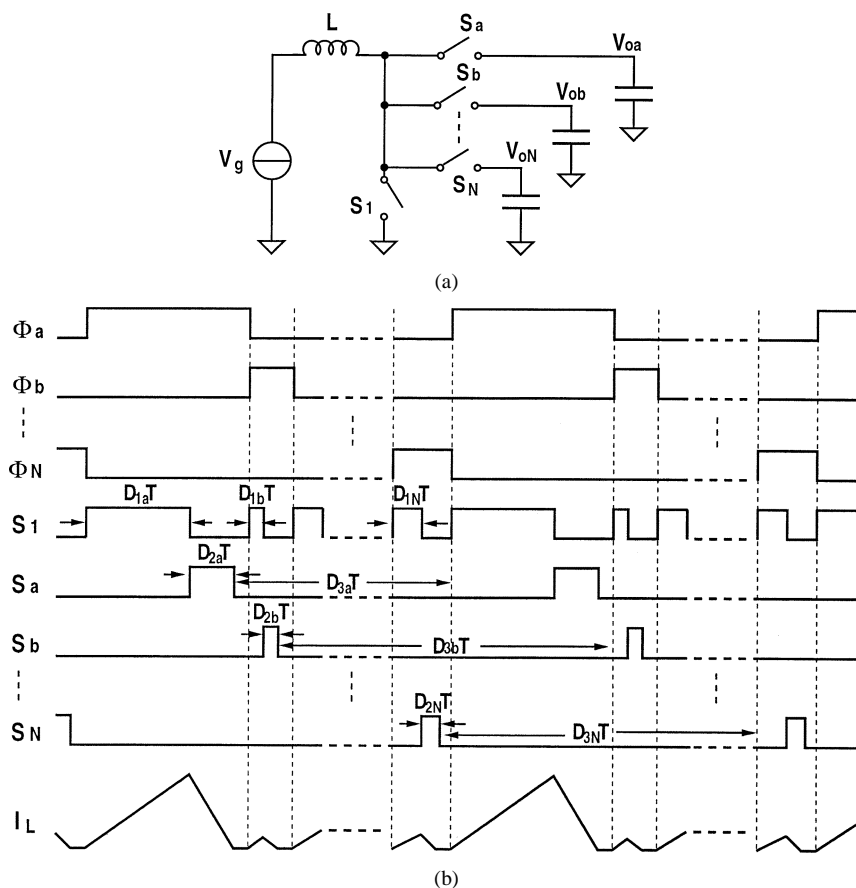$$C_1 = \frac{1}{2\pi f_{z-ea}R_2} \qquad (16)$$

(a)

(b)

Fig. 10.   (a) SIMO converter with N outputs. (b) Timing diagram of the converter with N outputs having unbalanced loads.

TABLE I
COMPARISON OF MULTIPLE-OUTPUT CONVERTER ARCHITECTURES

	Inductors	Power devices	Control loops	Others
Isolated converter [10]	$\geq N$	$\geq N+1$	≥ 1	Post regulation circuits
Independent converters	$\geq N$	$\geq 2N$	$\geq N$	
Dancy's [11]	N	$2N$	1	
Li's [13]	1	$2N+1$	N/A†	
Goder's [14]	1	$\geq N+1$	1	2N voltage references
May's [16]	1	$N+1$	$\geq \frac{N(N-1)}{2}+1$	ADC
This design	1	$N+1$	1	

† No control loop(s) is available in [13].

$$R_2 = A_{xo}R_1 \qquad (18)$$

where A_{xo} is the gain of the compensation network at the crossover frequency of the loop gain, and f_{xo} is the crossover frequency which is related to the bandwidth of the converter. Fig. 9 shows the simulated loop gain with compensation of this design.
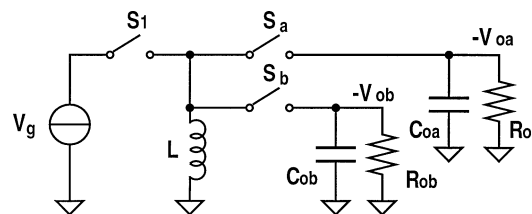
E. Topological Extensions

Fig. 11.   SIDO flyback converter.

DOCKET ALARM

Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

Real-Time Litigation Alerts

Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

Advanced Docket Research

With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

Analytics At Your Fingertips

Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

LAW FIRMS
Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

FINANCIAL INSTITUTIONS
Litigation and bankruptcy checks for companies and debtors.

E-DISCOVERY AND LEGAL VENDORS
Sync your system to PACER to automate legal marketing.

fastcase®
Smarter legal research.