24.6 A 4-Output Single-Inductor DC-DC Buck Converter with Self-Boosted Switch Drivers and 1.2A Total Output Current

M. Belloni[1], E. Bonizzoni[1], E. Kiseliovas[2], P. Malcovati[1], F. Maloberti[1], T. Peltola[2], T. Teppo[2]

[1]University of Pavia, Pavia, Italy
[2]National Semiconductor, Oulu, Finland

Minimizing power consumption in multi-processor systems requires the use of multiple supplies with a wide range of regulated voltages and currents. Since one inductor per DC-DC converter is expensive, there is an increasing interest in single-inductor-multiple-output (SIMO) DC-DC converters. Recent research results report a SIMO boost converter [1] and various boost or buck converters with two outputs [2, 3]. This 0.5μm CMOS system is a four-output, single-inductor buck converter with independent regulation of each output in the range 0 to (V_{DD} – 0.500)V. The minimum and maximum total currents are 0.15 and 1.2A, respectively. The switching frequency is 3MHz and the external inductance is 1μH.

Figure 24.6.1 shows the overall architecture of the four-output DC-DC converter. It uses *n*- and *p*-channel switches (M_P and M_N) to obtain a conventional buck structure and four *n*-channel switches (M_{swi}, i=1, … , 4) for time-sharing the inductor current among the loads. The buck converter operates in continuous mode, but the current delivered to the 10-μF capacitors is discontinuous because it goes to zero when the corresponding switch opens.

The analog processor produces four control signals. One is used to control the buck converter switching, and the others to divide the clock period into four slots. The processor uses four control loops and the errors resulting from the four outputs: $\varepsilon_i = V_{set}(i) - V_{out}(i)$ (i=1, …, 4). However, using several nested plain-PWM circuits, which is acceptable for two outputs [3], is problematic with four loops because instability occurs in many regions of operation. The solution used in this circuit combines simplicity with good performance and employs four PWM generators driven by suitable linear combinations of errors. The equations used are:

$$\begin{aligned} \varepsilon_D &= \varepsilon_1+\varepsilon_2+\varepsilon_3+\varepsilon_4; \\ \varepsilon_{D1} &= \varepsilon_1-\varepsilon_2-\varepsilon_3-\varepsilon_4; \\ \varepsilon_{D12} &= \varepsilon_1+\varepsilon_2-\varepsilon_3-\varepsilon_4; \\ \varepsilon_{D123} &= \varepsilon_1+\varepsilon_2+\varepsilon_3-\varepsilon_4; \end{aligned} \qquad (1)$$

As shown in Fig. 24.6.2, in the analog processor channel controlling the buck converter, a zero-pole filter, $H(s)$, is used in front of the PWM generator, while the other channels use just an amplifier. The pulses generated by the PWM driven by ε_{D1}, ε_{D12} and ε_{D123} determine the four time-sharing slots. The first slot is defined by the first pulse, the second by the logic "ex-or" of the first and second pulses, the third by the "ex-or" of the second and third pulses, and the fourth slot is the remaining part of the period. The signals sent to the switches do not overlap in order to avoid short-circuits among the loads.

The analog processor is realized with switched-capacitor circuits that achieve the error combinations given by Equations (1) as well as other functions. Figure 24.6.3 shows the details of the first processing channel, which consists of three sections. The first section combines the errors and provides a gain equal to 5, while the second section is the zero-pole switched-capacitor filter. The branch including C_5 and V_{bias} achieves a DC level shift. Finally, the flip-around double sample-and-hold decouples the filter from the PWM, thus limiting the kickback from the switching part and eliminating the glitches produced by switching from phase 1 to phase 2. The other channels only have two sections: one is an amplifier that processes the errors by providing a gain of 10 and shifting the DC level, and the other is the sample-and-hold. The unity capacitance used in the SC processors is 100fF. The OTAs are based on a two-stage architecture with pole splitting compensation and 0.8mA current consumption; the supply voltage can vary from 2.3 to 5V.

The driving of the switches of the buck converter is straightforward, since they are connected to V_{DD} or ground. By contrast, the control of the load switches is problematic because they connect to the regulated voltages. Self-boosted drivers are used to solve this problem as shown in Fig. 24.6.4. Since all the paths to ground are open when the switeches are all off (the non-overlap period), the inductor current flows trough diode D and charges the internal capacitor C_S = 170pF, which is in parallel with an external capacitor C_{S1} = 430pF, to boost the voltage. At the end of the non-overlap period the i^{th} control signal coming from the analog processor goes low, which turns M_{Ni} off and switches M_{Pi} on. Capacitors C_S and C_{S1} share their charge with the gate of the power switch M_{swi}, which turns on when its gate-source voltage reaches the threshold voltage. At that time, the voltage at the right terminal of the inductor drops down and diode D turns off. To ensure proper control of M_{Ni} through M_{Pi}, the logic signal provided by the analog processor is almost doubled by means of a charge pump (CP), [4].

The circuit has been fabricated using a 0.5μm 2P5M CMOS process. Experimental results show that, with a 2.3V minimum supply, it is possible to independently regulate the four outputs in the range 0 - 1.8V with output currents of 0.2A in each channel. With a higher supply voltage, the 1.2A overall driving capability provides 0.5A in one channel and about 240mA in the others. Lower currents are obviously possible, but the minimum average inductor current needed by the self-boosting switch driver is 0.15A. The voltage ripple is lower than 150mV for all operating conditions. The circuit operates with supplies up to 5V. However, since the ESD protection on the self-boosted driver output limits the boosted voltage to 5V, the regulated outputs can only go up to 3.6V with low currents. Figure 24.6.5 is a cross regulation plot, which shows that, with V_{DD} = 2.8V, when the voltage in one channel (V_{out3}) changes from 1.1 to 2V it minimally affects the three other channels, V_{out1}, V_{out2} and V_{out4}, which are set at fixed voltages equal to 0.9V, 0.7V and 1.6V, respectively. The worst cross regulation (120mV) is for the channel number 4. Figure 24.6.6 shows the operation of the self-boosted driver. Trace 1 is the logic control for the switch. Trace 3 shows the boosted voltage that reaches the maximum allowed value (5V). Trace 2 is the regulated voltage. Trace 4 is the inverted main clock.

The power used by the analog processor does not limit the efficiency of the circuit. Indeed, with an output current of 0.4A for example, the current used by the analog processor (8mA) is only 2% of that value and the drop in efficiency is negligible. Experimental results reveal that η= 82% with 0.8, 1, 1.2 and 1.8V regulated voltages and currents of 230, 120, 100 and 50mA, respectively. The minimum efficiency is η=72% with the maximum output current and large output voltages. The reduction of the efficiency in these conditions is due to the limitation of the boosted control voltages to 5V, which reduces the overdrives of the switches and hence increases their on-resistances.

Figure 24.6.7 shows the chip micrograph. The total area is 3.5mm×3.8mm with 1.2mm² used for analog processing.

References:

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[2] D. Ma, W-H. Ki and C-Y. Tsui, "A Pseudo-CCM/DCM SIMO Switching Converter with Freewheel Switching," *ISSCC Dig. Tech. Papers*, pp. 390–391, 2002.
[3] E. Bonizzoni, F. Borghetti, P. Malcovati et al., "A 200mA 93% Peak Efficiency Single-Inductor Dual-Output DC-DC Buck Converter," *ISSCC Dig. Tech. Papers*, pp. 526–527, 2007.
[4] P. Favrat, P. Deval and M. J. Declercq, "A New High Efficiency CMOS Voltage Doubler," *Proc. CICC*, pp. 259–262, 1997.

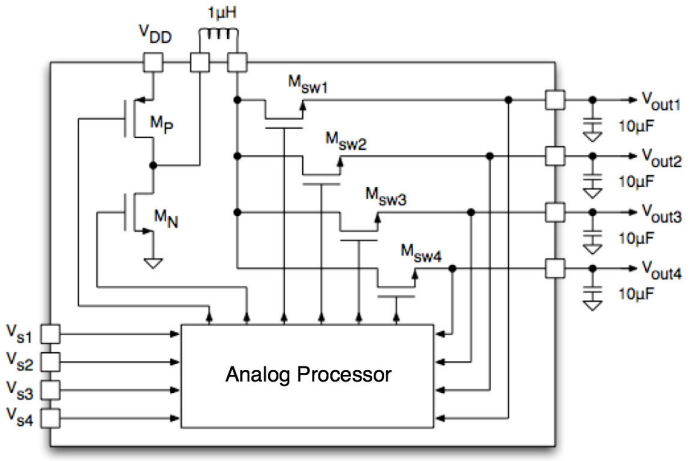

Figure 24.6.1: Architecture of the single-inductor four-output DC-DC buck converter.

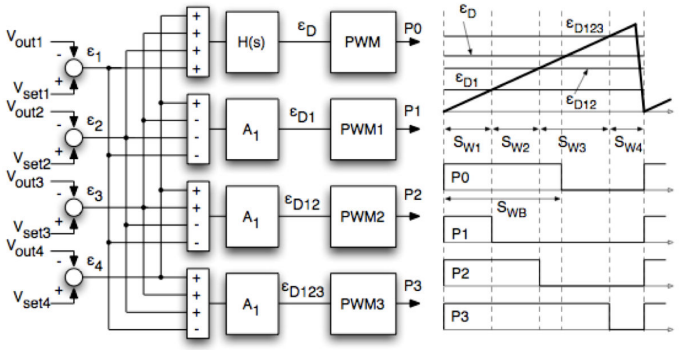

Figure 24.6.2: Analog processor block diagram.

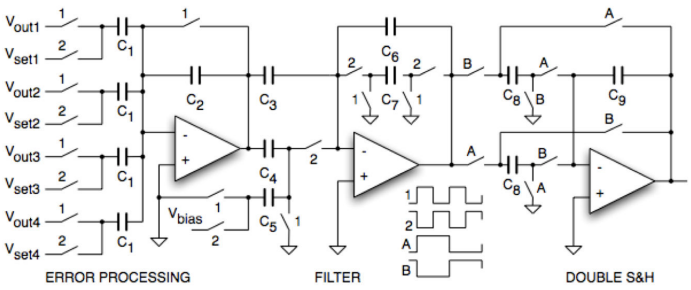

Figure 24.6.3: Analog processor first channel schematic diagram.

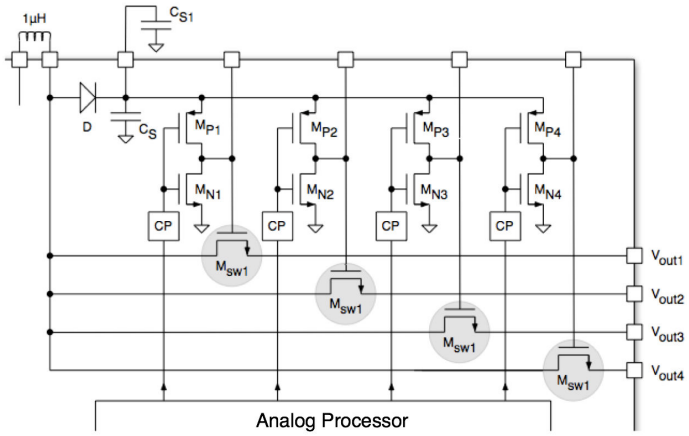

Figure 24.6.4: Self-boosted switch drivers schematic diagram.

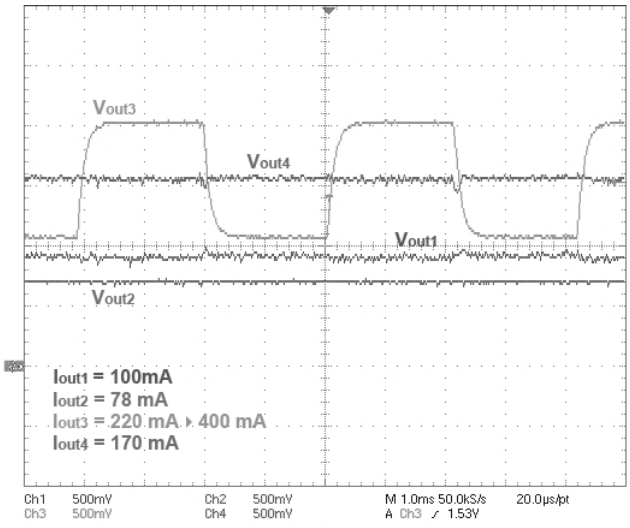

Figure 24.6.5: Measured regulated output voltages (V_{out1} = 0.9V ch. 1, V_{out2} = 0.7V ch. 2, V_{out3} = 1.1 to 2V ch. 3, V_{out4} = 1.6V ch. 4)

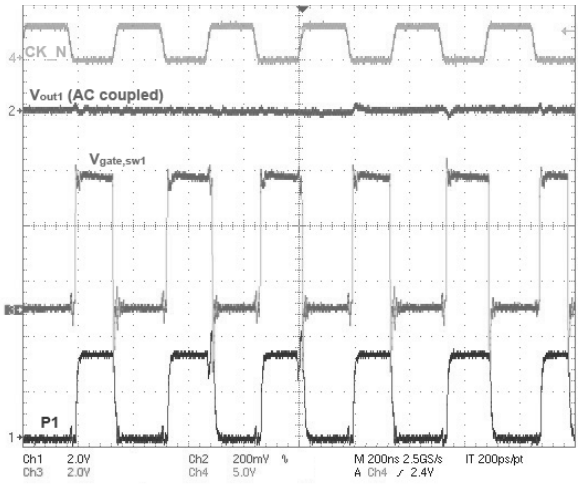

Figure 24.6.6: Measured waveforms: digital control signal (P1, ch. 1), output voltage (V_{out1} AC coupled, ch. 2), self boosted switch gate ($V_{gate,\ sw1}$, ch. 3), inverted main clock (CK_N, ch. 4).

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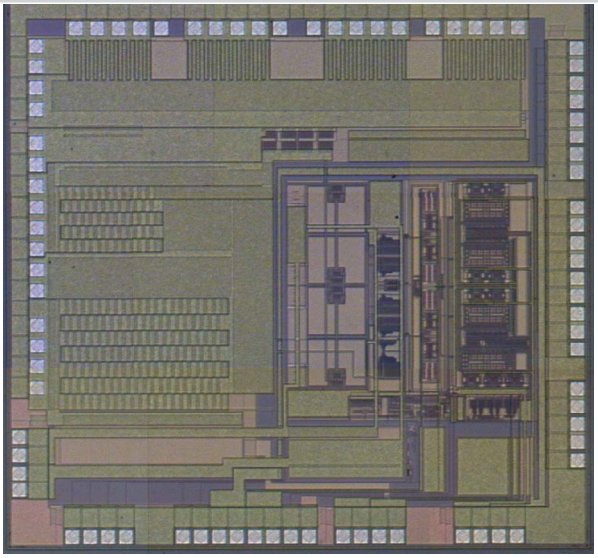

Figure 24.6.7: Chip micrograph.