UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

Case No. IPR2022-00996
Patent No. 11,016,918

DECLARATION OF DR. SUNIL P. KHATRI

DECLARATION OF SUNIL P. KHATRI, PH. D

I, Sunil P. Khatri, do hereby declare as follows:

I. INTRODUCTION

1. I have been retained on behalf of Netlist, Inc. ("Patent Owner") as an expert to evaluate certain technical aspects of U.S. Patent No. 11,016,918 ("the '918 patent"), and to provide certain options relating thereto. I am personally knowledgeable about the matters stated herein and am competent to make this declaration.

2. I understand that Patent Owner will submit this declaration ("Declaration") in connection with IPR2022-00996 ("Proceeding"), which I have been informed is an *inter partes* review (IPR) proceeding before the Patent Trial and Appeal Board challenging the patentability of claims 1-30 of the '918 patent.

3. I receive compensation at my normal consulting rate for my time working on this matter, plus expenses. I have no financial interest in Patent Owner or in the patents involved in this litigation, and my compensation is not dependent on the outcome of this litigation. The opinions I present are due to my own judgment.

4. All "EX10XX" cites herein are to exhibits I understand are being submitted by the Patent Owner in this Proceeding. All "Appendix _" cites followed by a letter are to appendices to this Declaration. All citations to "Section XX" are

internal citations to the sections of this Declaration. All citations to "Paragraph XX" are internal citations to the paragraphs of this Declaration.

II. BACKGROUND AND QUALIFICATIONS

5. I have over thirty-five years of experience with electronics, electrical engineering, and computer engineering. A copy of my latest curriculum vitae (CV), which I understand is being submitted with this Declaration as Appendix A, provides further details regarding my background and qualifications. During my career, I have acquired extensive knowledge and experience with VLSI circuits, computer architecture, testing, computer-aided design (CAD) algorithms and algorithm acceleration, logic synthesis, semiconductor memory, redundancy, synchronous and asynchronous circuits, and related software and hardware topics. Most relevant to the '054 patent, my technical expertise includes extensive work with semiconductor memory devices such as dynamic random access memory (DRAM), static random access memory (SRAM), and flash memory. My work with semiconductor memory devices has included work on 3D integration and novel ring-based DRAM memory DIMM architectures, power and speed tradeoffs using selective body bias, architectures and circuit approaches for processing-in-memory within DIMM-based DRAM architectures, stability modeling of RAM memory, power reduction in memory designs, and clocking and source-synchronous design. My graduate as well as undergraduate coursework covers memory circuit design extensively, including

DRAM memory circuits as well as DIMMs and their system-level design and latency properties. Additionally, I have served as an expert witness in several cases involving semiconductor memory, including DRAM and flash memory. My MS thesis involved designing a memory interface for a multi-threaded Reduced Instruction Set Computing (RISC) microprocessor.

6. The following describes some of my relevant experience. I earned my Bachelor of Science in Electrical Engineering in 1987 from the Indian Institute of Technology, Kanpur, India. After graduating with my B.S. degree, I was a candidate for a Master of Science degree in Electrical and Computer Engineering at the University of Texas from 1987–89. At the University of Texas, I held the Microelectronics and Computer Development (MCD) Fellowship from 1987–89. I also conducted my M.S. research and wrote my thesis on the design of the METRIC memory interface and memory system. METRIC was one of the first super-scalar processors that was developed in the world. I earned an M.S. degree in 1989 from the University of Texas, Austin.

7. After leaving the University of Texas, I worked at Motorola Inc. from 1989–93 as a design engineer for the MC88110 RISC microprocessor team, followed by the PowerPC 603 RISC microprocessor design team. My duties included the design of digital and analog circuitry, test logic circuits, layout, JTAG boundary scan design, input/output driver design, and clock phase-locked loop

(PLL) logic and clock distribution. During my time at Motorola, I was independently responsible for the design of the factory test controller of the MC88110 microprocessor. I performed all attendant tasks in a "vertical" VLSI design methodology, which included high-level modeling, circuit and layout design and verification, as well as global and detailed routing. I also helped in the design of the Translation Lookaside Buffer (TLB) unit, which included a static random-access memory (SRAM) block.

8. In 1999, I earned a Doctor of Philosophy degree in Electrical Engineering and Computer Sciences from the University of California, Berkeley. While at Berkeley, I held the California Microelectronics (MICRO) Fellowship in 1993.

9. I joined the faculty at the University of Colorado, Boulder, in 2000 as an Assistant Professor of Electrical and Computer Engineering. At the University of Colorado my research focused on VLSI logic design automation, VLSI layout design automation, and VLSI design methodologies to address Deep Submicron (DSM) issues such as crosstalk and power.

10. I joined the faculty at Texas A&M University in 2004 as an Assistant Professor in Electrical and Computer Engineering. In 2010, I was promoted to Associate Professor in Electrical and Computer Engineering. In 2015, I was promoted to full Professor in Electrical and Computer Engineering. My research

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