UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD., MICRON TECHNOLOGY, INC., MICRON SEMICONDUCTOR PRODUCTS, INC., and MICRON TECHNOLOGY TEXAS LLC,[†]

Petitioner,

v.

NETLIST, INC.,

Patent Owner

IPR2022-00996
Patent 11,016,918 B2

EXHIBIT 1079:

Petitioner's Demonstratives for Oral Argument on September 11, 2023

[†] Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC filed a motion for joinder and a petition in IPR2023-00406 and have been joined as petitioners in this proceeding.

Petitioner Samsung Electronics Co., Ltd.'s Oral Argument for PTAB Hearing

Samsung Electronics Co., Ltd. v. Netlist, Inc.,

IPR2022-00996 and IPR2022-00999 (U.S. Patent Nos. 11,016,918 and 11,232,054)

September 11, 2023

BAKER BOTTS

Table of Contents

OVERVIEW 01

OVERVIEW OF ’918 AND ’054 PATENTS, AND INSTITUTED GROUNDS

‘918 AND ‘054 PATENTS

’918 Patent

(12) **United States Patent**
Chen et al.

(10) **Patent No.: US 11,016,918 B2**
(45) **Date of Patent: May 25, 2021**

(54) **FLASH-DRAM HYBRID MEMORY MODULE**

(71) Applicant: **Netlist, Inc.**, Irvine, CA (US)

(72) Inventors: **Chi-She Chen**, Walnut, CA (US); **Jeffrey C. Solomon**, Irvine, CA (US); **Scott H. Milton**, Irvine, CA (US); **Jayesh Bhakta**, Cerritos, CA (US)

(73) Assignee: **Netlist, Inc.**, Irvine, CA (US)

Related U.S. Application Data

No. 14/840,865, filed on Aug. 31, 2015, now Pat. No. 9,928,186, which is a continuation of application No. 14/489,269, filed on Sep. 17, 2014, now Pat. No. 9,158,684, which is a continuation of application No. 13/559,476, filed on Jul. 26, 2012, now Pat. No. 8,874,831, which is a continuation-in-part of application No. 12/240,916, filed on Sep. 29, 2008, now Pat. No. 8,301,833, which is a continuation of application No. 12/131,873, filed on Jun. 2, 2008, now abandoned.

(60) Provisional application No. 60/941,586, filed on Jun. 1, 2007, provisional application No. 61/512,871, filed on Jul. 28, 2011.

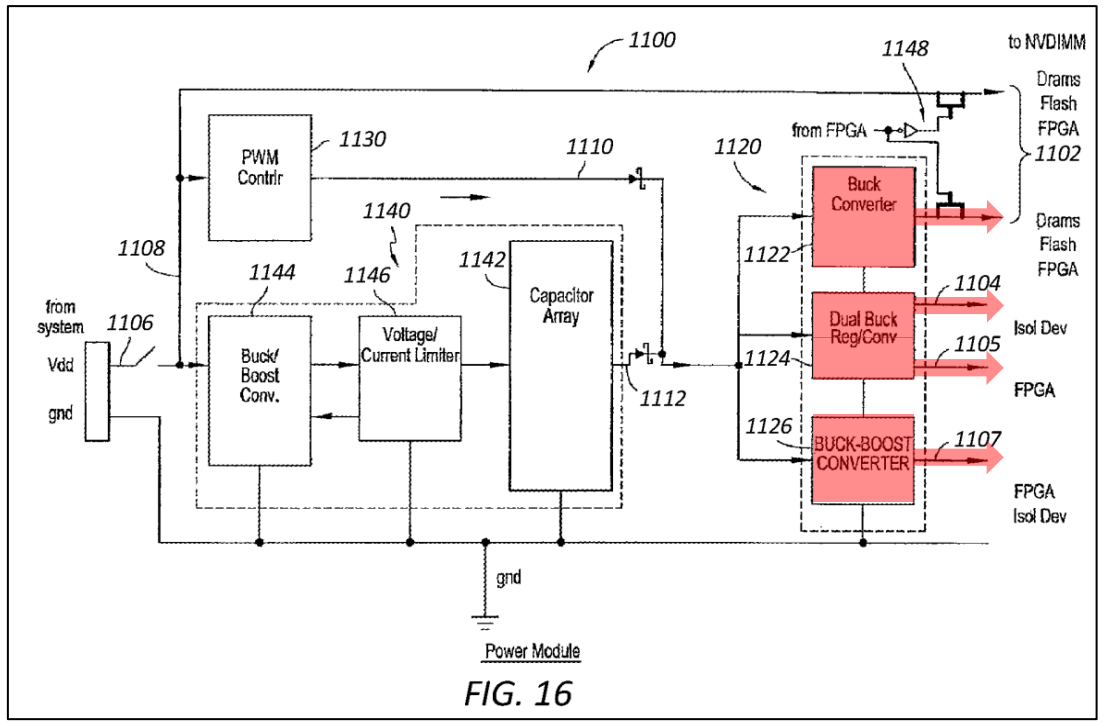


FIG. 16

1. A memory module comprising:

a printed circuit board (BCB) having an interface configured to fit not a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;

a first buck converter configured to provide a first regulated voltage having a first voltage amplitude;

a second buck converter configured to provide a second regulated voltage having a second voltage amplitude;

a third buck converter configured to provide a third regulated voltage having a third voltage amplitude;

a converter circuit configured to provide a fourth regulated voltage having a fourth voltage amplitude; and

a plurality of components coupled to the PCB, each component of the plurality of components coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages, the plurality of components comprising:

a plurality of synchronous dynamic random access memory (SDRAM) devices coupled to the first regulated voltage, and

[1] at least one circuit coupled between a first portion of the plurality of edge connections and the plurality of SDRAM devices,

[2] the at least one circuit operable to (i) receive a first plurality of address and control signals via the first portion of the plurality of edge connections, and (ii) output a second plurality of address and control signals to the plurality of SDRAM devices,

[3] the at least one circuit coupled to both the second regulated voltage and the fourth regulated voltage,

[4] wherein a first one of the second and fourth voltage amplitudes is less than a second one of the second and fourth voltage amplitudes.

’054 Patent

(12) **United States Patent**
Chen et al.

(10) **Patent No.: US 11,232,054 B2**
(45) **Date of Patent: *Jan. 25, 2022**

(54) **FLASH-DRAM HYBRID MEMORY MODULE**

(71) Applicant: **Netlist, Inc.**, Irvine, CA (US)

(72) Inventors: **Chi-She Chen**, Walnut, CA (US); **Jeffrey C. Solomon**, Irvine, CA (US); **Scott H. Milton**, Irvine, CA (US); **Jayesh Bhakta**, Cerritos, CA (US)

(73) Assignee: **NETLIST, INC.**, Irvine, CA (US)

Related U.S. Application Data

(63) Continuation of application No. 17/138,766, filed on Dec. 30, 2020, now Pat. No. 11,016,918, which is a continuation of application No. 15/934,416, filed on Mar. 23, 2018, now abandoned, which is a continuation of application No. 14/840,865, filed on Aug. 31, 2015, now Pat. No. 9,928,186, which is a continuation of application No. 14/489,269, filed on Sep. 17, 2014, now Pat. No. 9,158,684, which is a continuation of application No. 13/559,476, filed on Jul. 26, 2012, now Pat. No. 8,874,831, which is a continuation-in-part of application No. 12/240,916, filed on Sep. 29, 2008, now Pat. No. 8,301,833, which is a continuation of application No. 12/131,873, filed on Jun. 2, 2008, now abandoned.

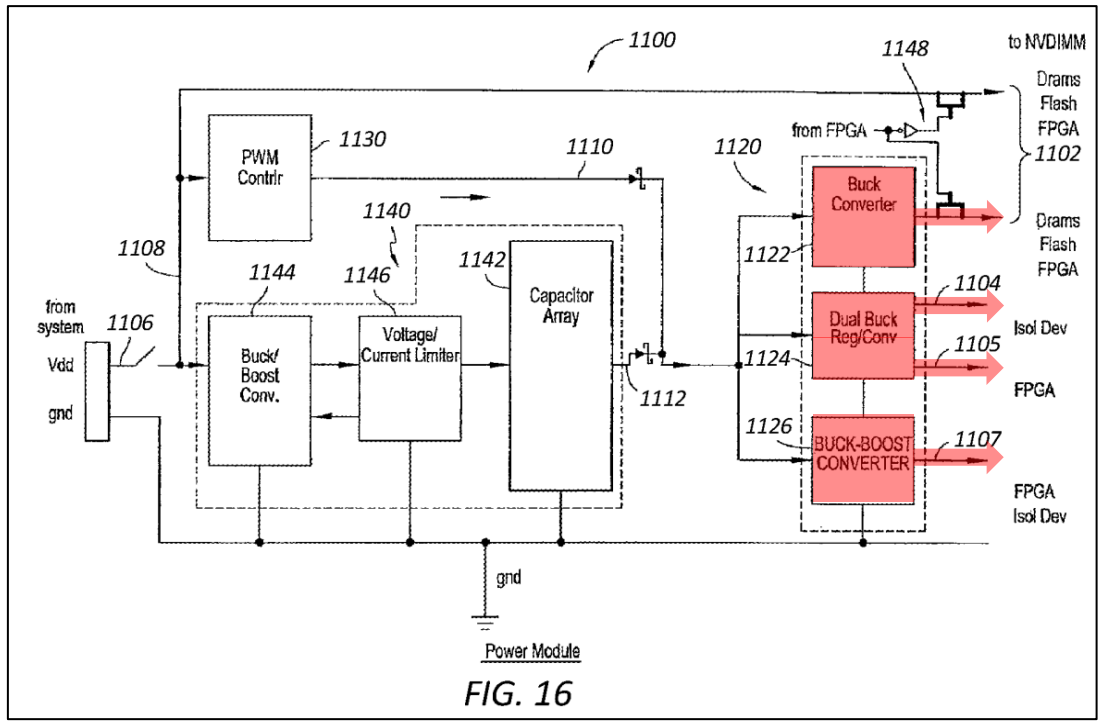


FIG. 16

1. A memory module comprising:

a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;

a voltage conversion circuit coupled to the PCB and configured to provide **at least three regulated voltages**, wherein the voltage conversion circuit includes **at least three buck converters** each of which is configured to produce a regulated voltage of the at least three regulated voltages;

[1] a plurality of components coupled to the PCB, each component of the plurality of components coupled to at least one regulated voltage of the at least three regulated voltages,

[2] the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices and

[3] a first circuit that is coupled to the plurality of SDRAM devices and to a first set of edge connections of the plurality of edge connections,

[4] wherein the first circuit is coupled to first and second regulated voltages of the at least three regulated voltages, and

[5] wherein the plurality of SDRAM devices are coupled to the first regulated voltage of the at least three regulated voltages.

054: EX1001 (’054 Patent) at Claim 1

‘918 and ‘054 Patent Overview

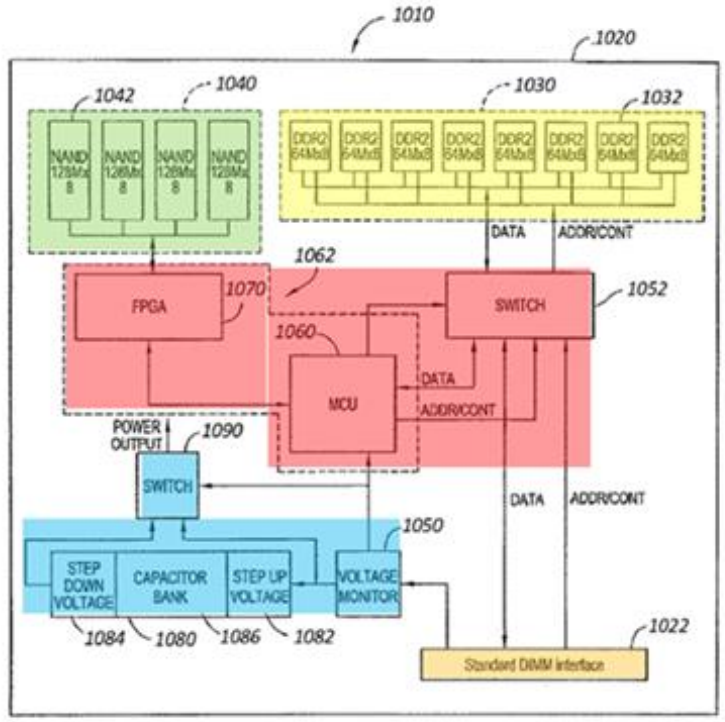


FIG. 12

FIG. **12** is a block diagram of an example memory system **1010** compatible with certain embodiments described herein. The memory system **1010** can be coupled to a host computer system and can include a volatile memory subsystem **1030**, a non-volatile memory subsystem **1040**, and a controller **1062** operatively coupled to the non-volatile memory subsystem **1040**. In certain embodiments, the memory system **1010** includes at least one circuit **1052** configured to selectively operatively decouple the controller **1062** from the volatile memory subsystem **1030**.

Power may be supplied to the volatile memory subsystem **1030** from a first power supply (e.g., a system power supply) when the memory system **1010** is in the first state and from a second power supply **1080** when the memory system **1010** is in the second state.

For example, the interface **1022** can comprise a plurality of edge connections which fit into a corresponding slot connector of the host system. The interface **1022** of certain embodiments provides a conduit for power voltage as well as data, address, and control signals between the memory system **1010** and the host system.

‘918: EX1001 (918 Patent) at Fig. 12, 21:14-23, 25:54-58, 22:1-6; Paper 1 (Pet.) at 5-7; EX1003 at ¶¶68-81
‘054: EX1001 (054 Patent) at Fig. 12, 21:14-23, 25:54-58, 22:1-6; Paper 1 (Pet.) at 4-6; EX1003 at ¶¶62-75

‘918 and ‘054 Patent Overview

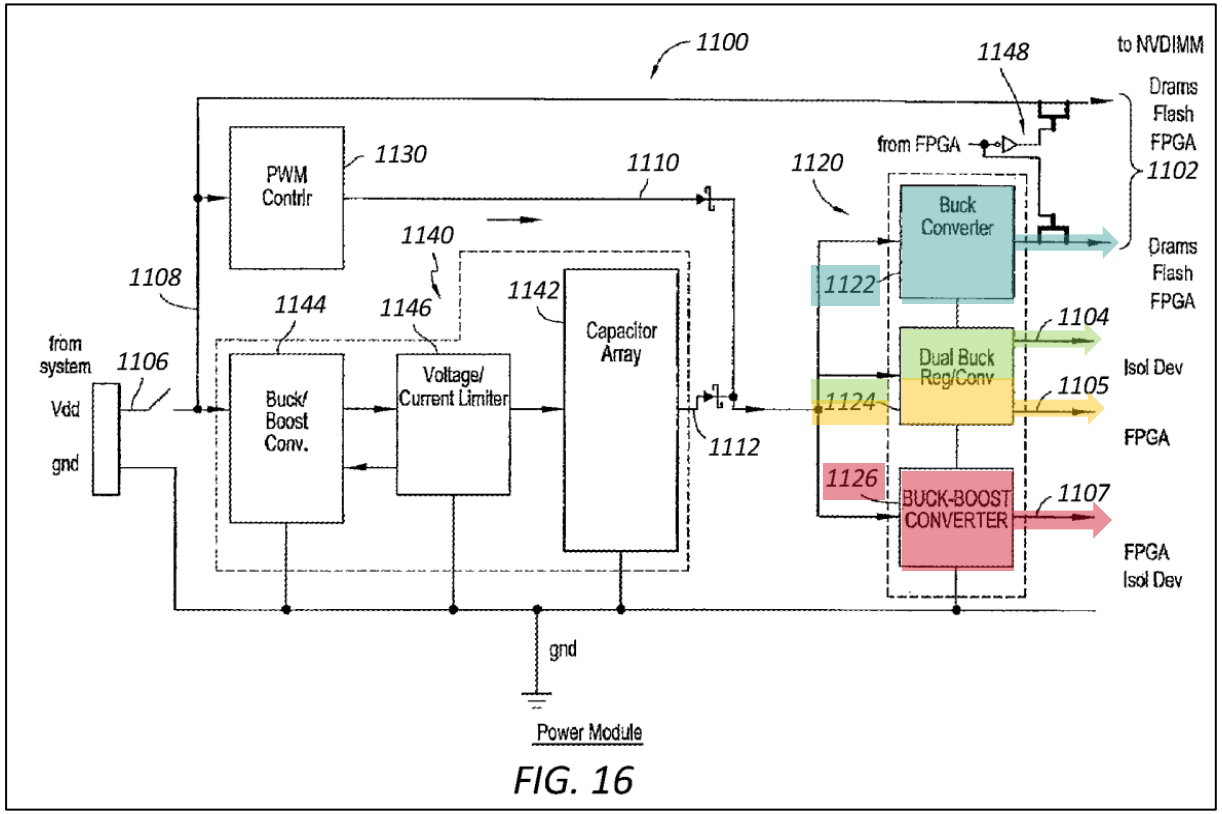


FIG. 16

The conversion element **1120** can comprise one or more buck converters and/or one or more buck-boost converters. The conversion element **1120** may comprise a plurality of sub-blocks **1122**, **1124**, **1126** as schematically illustrated by FIG. **16**, which can provide more voltages in addition to the second voltage **1104** to the memory system **1010**. The sub-blocks may comprise various converter circuits such as buck-converters, boost converters, and buck-boost converter circuits for providing various voltage values to the memory system **1010**. For example, in one embodiment, sub-block **1122** comprises a buck converter, sub-block **1124** comprises a dual buck converter, and sub-block **1126** comprises a buck-boost converter as schematically illustrated by FIG. **16**.

For example, the buck-converter of sub-block **1122** can provide 1.8V at 2A for about 60 seconds to the volatile memory elements **1032** (e.g., DRAM), the non-volatile memory elements **1042** (e.g., flash), and the controller **1062** (e.g., an FPGA) in one embodiment. The sub-block **1124** can provide the second voltage **1104** as well as another reduced voltage **1105** to the memory system **1010**. In one example embodiment, the second voltage **1104** is 2.5V and is used to power the at least one circuit **1052** (e.g., isolation device) and the other reduced voltage **1105** is 1.2V and is used to power the controller **1062** (e.g., FPGA). The subblock **1126** can provide yet another voltage **1107** to the memory system **1010**. For example, the voltage **1107** may be 3.3V and may be used to power both the controller **1062** and the at least one circuit **1052**.

‘918: EX1001 at Fig. 16, 29:18-31, 29: 39-54; Paper 1 (Pet.) at 5-7; EX1003 at ¶¶68-81
‘054: EX1001 at Fig. 16, 29:18-31, 29:39-54; Paper 1 (Pet.) at 4-6; EX1003 at ¶¶62-75

INSTITUTED GROUNDS & PRIOR ART

Instituted Grounds

Grounds	'918 Claims	'054 Claims	Prior art
1	Claims 1-3, 8, 14-15, 23	Claims 1-3, 15	***Harris*** + FBDIMM Standards
2	Claims 1-30	Claims 1-30	Ground 1 + Amidi
3	Claims 1-30	Claims 1-30	Ground 2 + Hajeck
4	Claims 1-30	Claims 1-30	***Spiers*** + Amidi
5	Claims 1-30	Claims 1-30	Ground 4 + Hajeck

'918: Paper 1 (Pet.) at 3-4; Paper 10 (ID) at 8, 55
'054: Paper 1 (Pet.) at 3; Paper 11 (ID) at 8, 54

Prior Art: Harris (U.S. Patent Pub. No. 2006/0174140) [EX1023]

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2006/0174140 A1**

Harris et al. (43) **Pub. Date: Aug. 3, 2006**

(22) Filed: **Jan. 31, 2005**

[0002] To cope with power requirements, industry standard memory modules, e.g., Dual In-line Memory Modules (DIMMS) populated with dynamic random access memory (DRAM) devices, are provided with power supply rails (on a relatively large number of pins) that are powered from system board or main board voltage sources, and are specific to the memory technology.

[0010] In accordance with the teachings of the present patent disclosure, at least one on-board voltage regulator module (VRM) is provided as part of the memory board assembly module **100**A for converting an externally supplied voltage level available on external source path **104** into appropriate local voltage levels that power the first and second voltage paths, i.e., the V_{dd} and V_{cc} paths **108**, **106**,

[0012] By way of example, a standard FBD module requires 28 V_{dd} pins (for DRAM devices) and 8 V_{cc} pins (for buffer and logic) and associated Ground returns, resulting in a total of 72 pins that provide a power supply interface for up to two x4 DRAM ranks (36 devices) and buffer logic. A voltage-independent FBD design incorporating the embodiment of **FIG. 1A** is capable of replacing these power supply interface pins with as few as six +12V pins (from an external voltage source), with local conversion to V_{dd} (to DRAM) and V_{cc} (to buffer/logic) being added. Alternatively, using

[0014] It should be readily recognized that the external voltage sources may comprise any combination of known or heretofore unknown voltage supplies, either regulated or unregulated, and even including variable voltages.

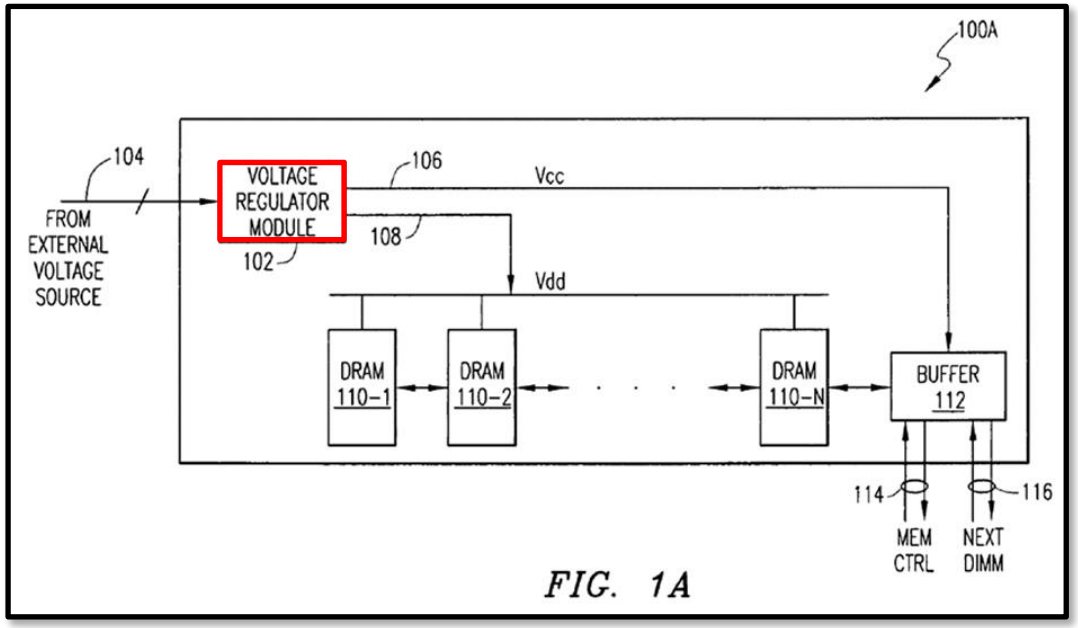


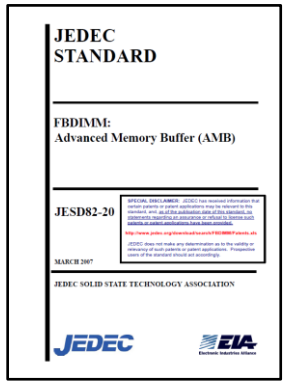
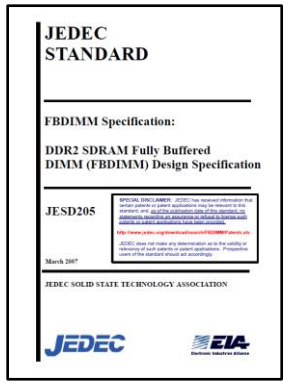
FIG. 1A

[0009] a V_{dd} path, that may be energized to appropriate voltage levels depending on the type, functionality, and design of the memory devices, e.g., from about 0.5V to 3.5V or more.

the V_{cc} path may be energized to appropriate voltage levels depending on the buffer and DIMM technology, e.g., from about 0.5V to 3.5V or more.

EX1023 (Harris)
'918: Paper 1 (Pet.) at 10; Paper 25 (Reply) at 2-7
'054: Paper 1 (Pet.) at 9-10; Paper 26 (Reply) at 2-8

Prior Art: FBDIMM Standards [EX1027, EX1028]

Exhibit	Description	Exemplary Teachings
EX1027 	"JESD82-20" – FBDIMM: Advanced Memory Buffer (AMB) standard, published in March of 2007 by JEDEC	Voltages for the "AMB buffer" on the FBDIMM memory module:
EX1028 	"JESD205" – DDR2 SDRAM Fully Buffered DIMM (FBDIMM) Design Specification, published in March of 2007 by JEDEC	Voltages for other components on the FBDIMM memory module:

Power Supplies

VCC (24 pins)	A	1.5V nominal supply for core IO
VCCFBD (8 pins)	A	1.5V nominal supply for FBD high speed IO
VDD (24 pins)	A	1.8V nominal supply for DDR IO
VSS (156 pins)	A	Ground
VDDSPD	A	3.3V nominal supply for SMB receivers and ESD diodes

EX1027 at p. 83

	min	typ	max	
Supply voltages (nominal)	1.7	1.8	1.9	(DRAM V_{DD}/V_{DDQ}, AMB V_{DDQ})
	1.455[1]	1.5	1.575[1]	(AMB V_{CC}/V_{CCFBD})
	0.453*V_{DD}	0.5*V_{DD}	0.547*V_{DD}	(DRAM Interface V_{TT}) This supply should track as 0.5 * 1.8 volt supply
	3.0	3.3	3.6	(V_{DDSPD})

EX1028 at p. 9

EX1027-EX1028 (FBDIMM Standards)
'918: Paper 1 (Pet.) at 11; Paper 25 (Reply) at 9, 15-16, 19
'054: Paper 1 (Pet.) at 10-11; Paper 26 (Reply) at 10, 16-17, 20

Prior Art: Amidi (U.S. Patent No. 7,724,604) [EX1024]

(12) **United States Patent**
Amidi et al.

(10) **Patent No.: US 7,724,604 B2**
(45) **Date of Patent: May 25, 2010**

(22) Filed: **Oct. 25, 2006**

(54) **CLOCK AND POWER FAULT DETECTION FOR MEMORY MODULES**

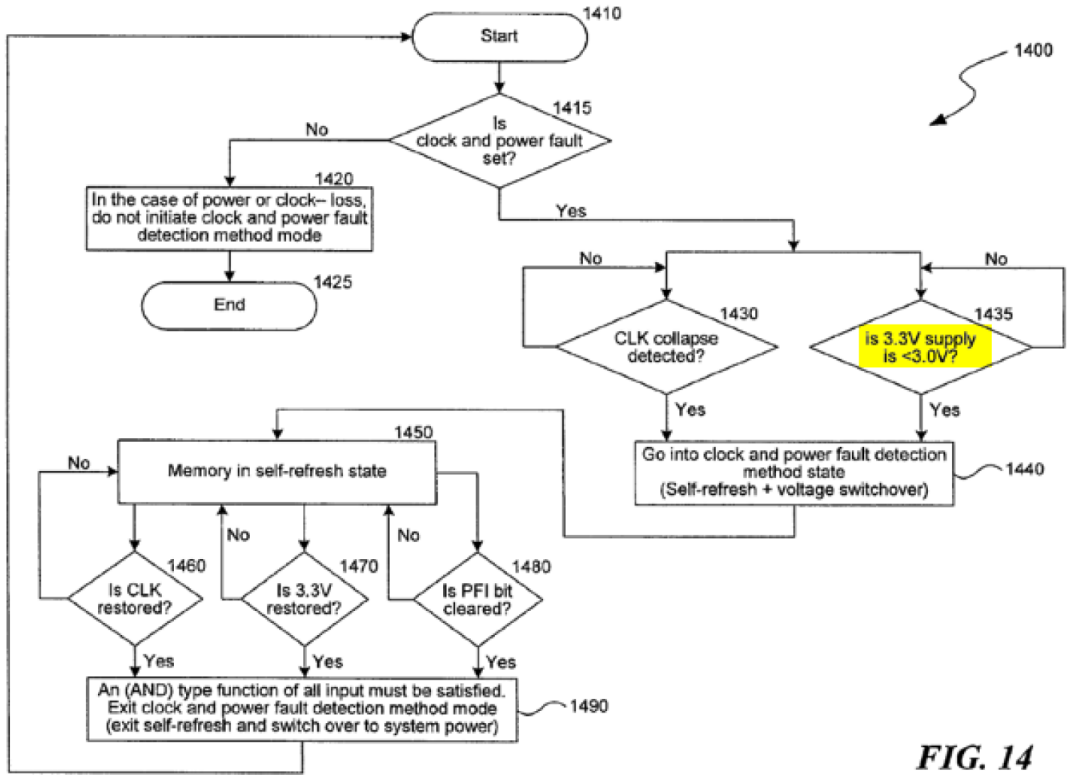


FIG. 14

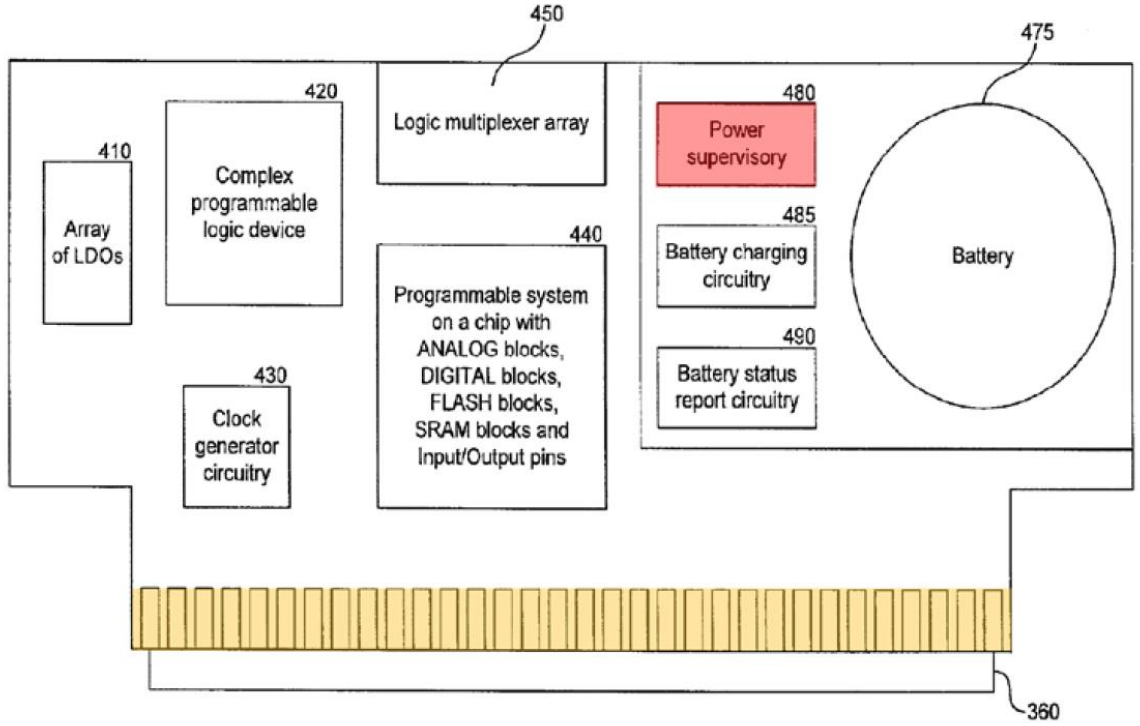


FIG. 4

EX1024 (Amidi)
'918: Paper 1 (Pet.) at 12, 62; Paper 25 (Reply) at 18-20
'054: Paper 1 (Pet.) at 11-12, 56, 60; Paper 26 (Reply) at 19-21

Prior Art: Hajeck (U.S. Patent No. 6,856,556) [EX1038]

(12) **United States Patent**
Hajeck

(10) **Patent No.: US 6,856,556 B1**
(45) **Date of Patent: Feb. 15, 2005**

The voltage detection circuit **48** is responsible for detecting anomalies in the power signal V_{IN} supplied by the host on line **36**, and for driving the ready/busy signal to the "busy" state when such anomalies are detected. A conventional voltage detection circuit may be used. The voltage detection circuit **48** may be designed to generate a "busy" signal whenever V_{IN} falls below a certain level, such as 2.6 or 2.7 volts. The voltage detection circuit may also be designed to generate a busy signal when the voltage exceeds a certain level, and/or when other types of anomalies are detected. To inhibit rapid transitions between the "ready" and "busy" states, the voltage detection circuit may be designed to provide a degree of hysteresis, and/or to hold its output for a particular time period after a state transition.

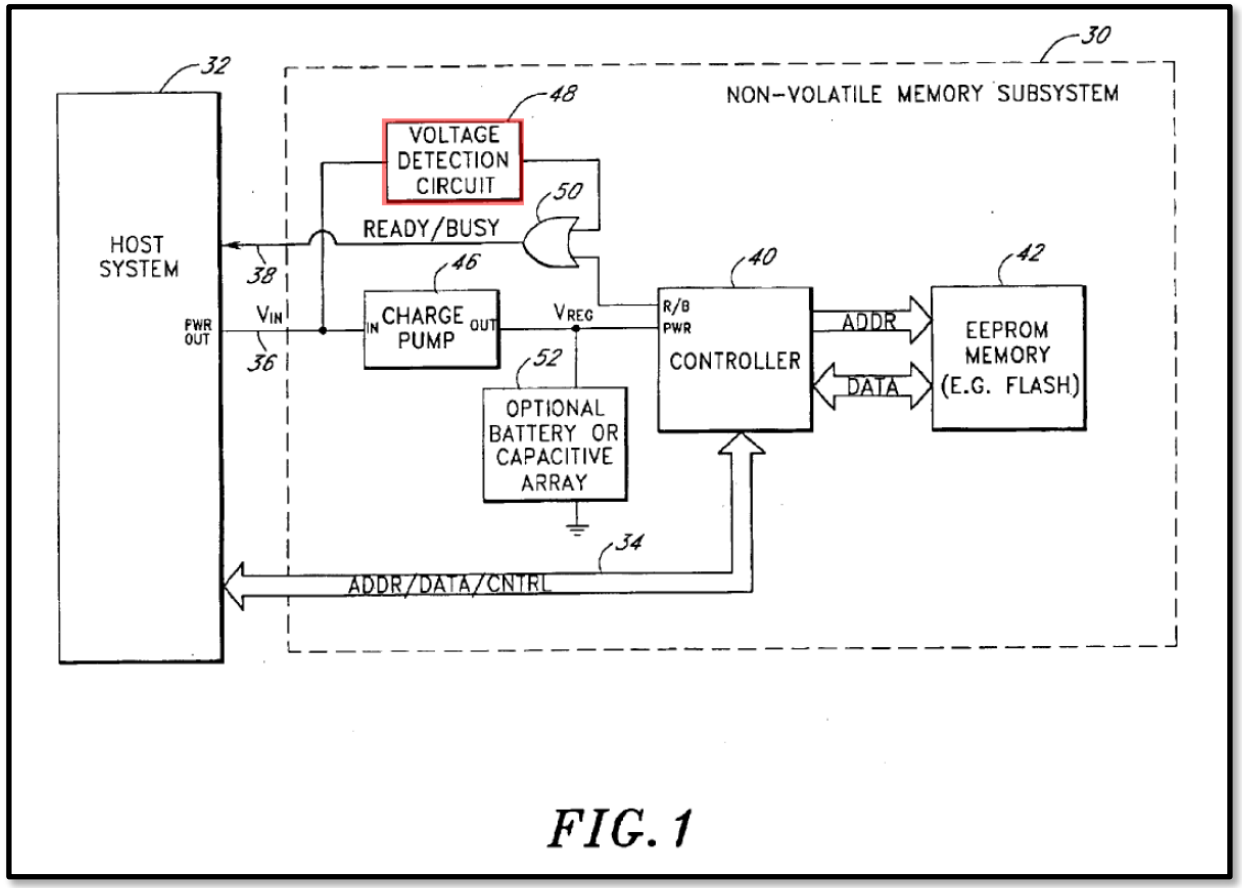


FIG. 1

EX1038 (Hajeck), 3:30-:43 & Fig. 1
'918: Paper 1 (Pet.) at 12-13; Paper 25 (Reply) at 22, 35-37
'054: Paper (Pet.) at 12-13; Paper 26 (Reply) at 21-22, 35

Prior Art: Spiers (U.S. Patent Pub. No. 2006/0080515) [EX1025]

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2006/0080515 A1**

Spiers et al. (43) **Pub. Date: Apr. 13, 2006**

(54) **NON-VOLATILE MEMORY BACKUP FOR NETWORK STORAGE SYSTEM**

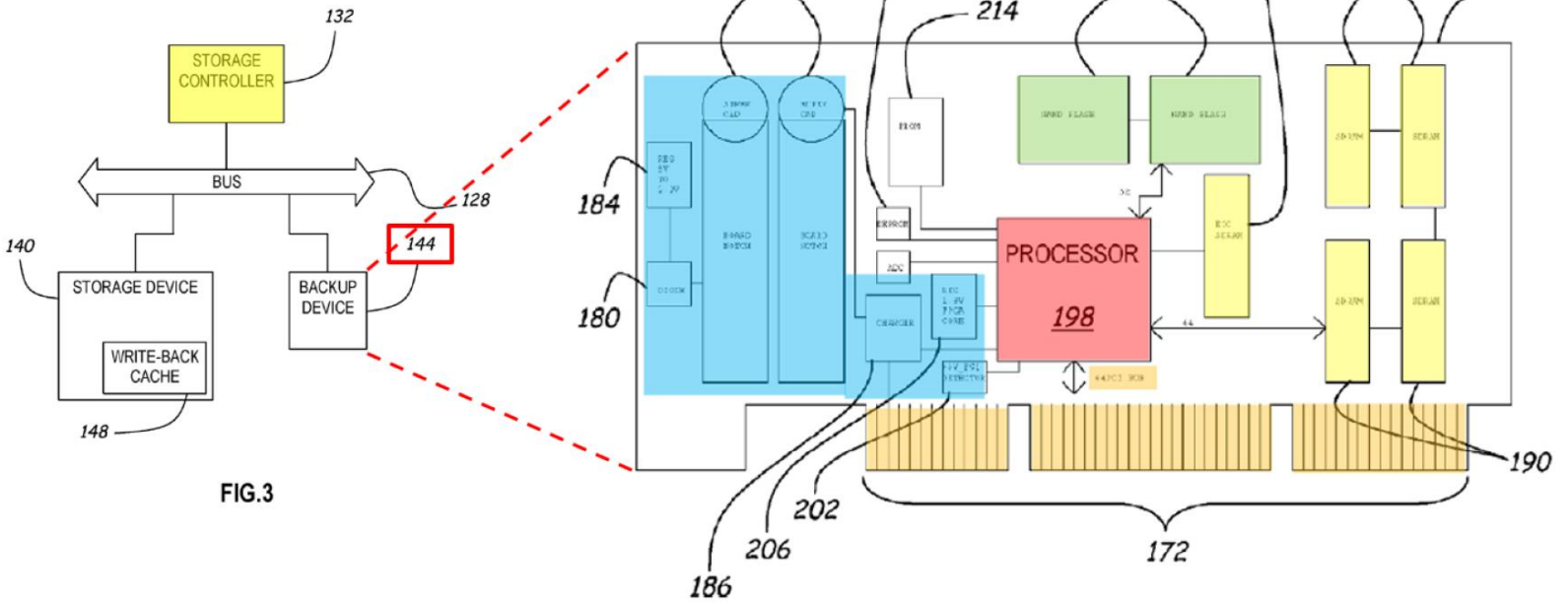
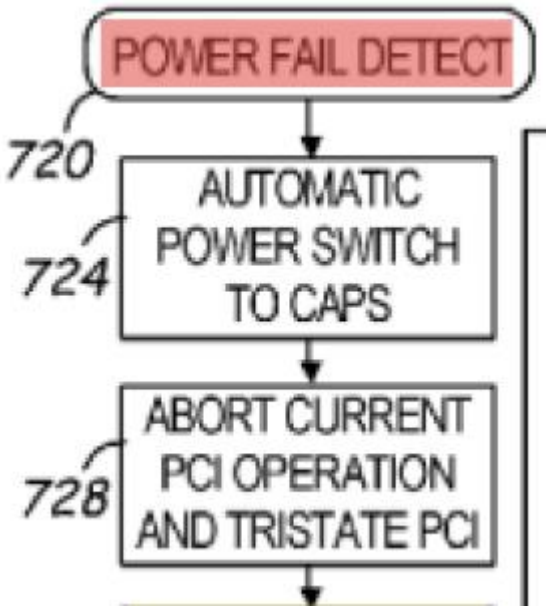


FIG.3

FIG.5



EX1025 (Spiers), Figs. 3, 5, 14
'918: Paper 1 (Pet.) at 13-14, 114; Paper 25 (Reply) at 23-27
'054: Paper 1 (Pet.) at 13-14, 102; Paper 26 (Reply) at 24-27

GROUNDS 1-3 (HARRIS) 02

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SUMMARY OF COMBINATIONS

Ground 1: Harris + JEDEC's FBDIMM Standards

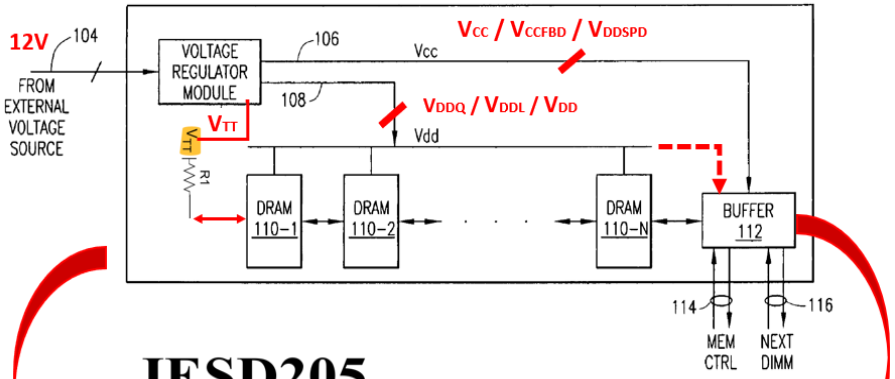
Harris

- One or more Voltage Regulator Modules on the memory module with buck converters to convert from 12V to lower voltages for various components
- Memory module can be "Fully buffered DIMM" (i.e., FBDIMM)

FBDIMM Standards

- Specify particular voltages for various components on an FBDIMM

Ground 1: Harris with JEDEC's FBDIMM Standards



JESD205

FBDIMM Specification:

DDR2 SDRAM Fully Buffered DIMM (FBDIMM) Design Specification

March 2007

JESD82-20

FBDIMM: Advanced Memory Buffer (AMB)

MARCH 2007

054 Mappings

Voltage Mapping (A)
1st : VDD / VDDQ = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VDDL = 1.8V

Voltage Mapping (B)
1st : VDD / VDDQ = 1.8V
2nd : VCC = 1.5V
3rd : VCCFBD = 1.5V

Voltage Mapping (C)
1st : VDD / VDDQ = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VTT = 0.9V

918 Mappings

Voltage Mapping (A)
1st : VDD / VDDQ = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VDDL = 1.8V
4th : VDDSPD = 3.3V

Voltage Mapping (B)
1st : VDD / VDDQ / VDDL = 1.8V
2nd : VCC = 1.5V
3rd : VCCFBD = 1.5V
4th : VDDSPD = 3.3V

Voltage Mapping (C)
1st : VDD / VDDQ / VDDL = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VTT = 0.9V
4th : VDDSPD = 3.3V

'918: Paper 1 (Pet.) at 14-19
'054: Paper 1 (Pet.) at 14-19

Ground 1: Harris + JEDEC's FBDIMM Standards

"Where a prior art patent discloses a ***range of values***, showing a claimed value falls within that range meets a party's burden of establishing the narrower claim would have been obvious where there is no reason to think the result would be unpredictable."

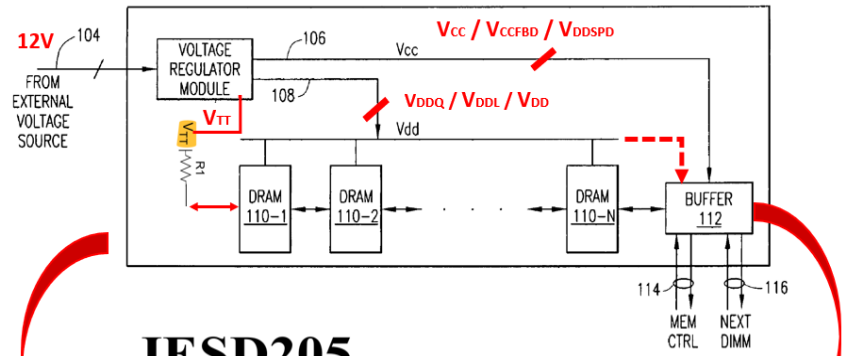
Gen. Hosp. Corp. v. Sienna Biopharms., Inc., 888 F.3d 1368, 1373 (Fed. Cir. 2018); *see also, e.g., Iron Grip Barbell Co. v. USA Sports, Inc.*, 392 F.3d 1317, 1320-23 (Fed. Cir. 2004) (claim to three grips obvious in light of prior art teaching one, two, and four grips)

[0009] a V_{dd} path, that may be energized to appropriate voltage levels depending on the type, functionality, and design of the memory devices, e.g., from about 0.5V to 3.5V or more.

the V_{cc} path may be energized to appropriate voltage levels depending on the buffer and DIMM technology, e.g., from about 0.5V to 3.5V or more.

[0010] In accordance with the teachings of the present patent disclosure, at least one on-board voltage regulator module (VRM) is provided as part of the memory board assembly module **100**A for converting an externally supplied voltage level available on external source path **104** into appropriate local voltage levels that power the first and second voltage paths, i.e., the V_{dd} and V_{cc} paths **108**, **106**,

Ground 1: Harris with JEDEC's FBDIMM Standards



JESD205

FBDIMM Specification:

DDR2 SDRAM Fully Buffered DIMM (FBDIMM) Design Specification

March 2007

JESD82-20

FBDIMM: Advanced Memory Buffer (AMB)

MARCH 2007

054 Mappings

Voltage Mapping (A)
1st : V_{DD} / V_{DDQ} = 1.8V
2nd : V_{CC} / V_{CCFBD} = 1.5V
3rd : V_{DDL} = 1.8V

Voltage Mapping (B)
1st : V_{DD} / V_{DDQ} = 1.8V
2nd : V_{CC} = 1.5V
3rd : V_{CCFBD} = 1.5V

Voltage Mapping (C)
1st : V_{DD} / V_{DDQ} = 1.8V
2nd : V_{CC} / V_{CCFBD} = 1.5V
3rd : V_{TT} = 0.9V

918 Mappings

Voltage Mapping (A)
1st : V_{DD} / V_{DDQ} = 1.8V
2nd : V_{CC} / V_{CCFBD} = 1.5V
3rd : V_{DDL} = 1.8V
4th : V_{DDSPD} = 3.3V

Voltage Mapping (B)
1st : V_{DD} / V_{DDQ} / V_{DDL} = 1.8V
2nd : V_{CC} = 1.5V
3rd : V_{CCFBD} = 1.5V
4th : V_{DDSPD} = 3.3V

Voltage Mapping (C)
1st : V_{DD} / V_{DDQ} / V_{DDL} = 1.8V
2nd : V_{CC} / V_{CCFBD} = 1.5V
3rd : V_{TT} = 0.9V
4th : V_{DDSPD} = 3.3V

'918: Paper 1 (Pet.) at 27-28
'054: Paper 1 (Pet.) at 27

Ground 2: adds Amidi

Amidi

- Adds battery backup and "logic" for detecting power faults
- Also uses buck converters

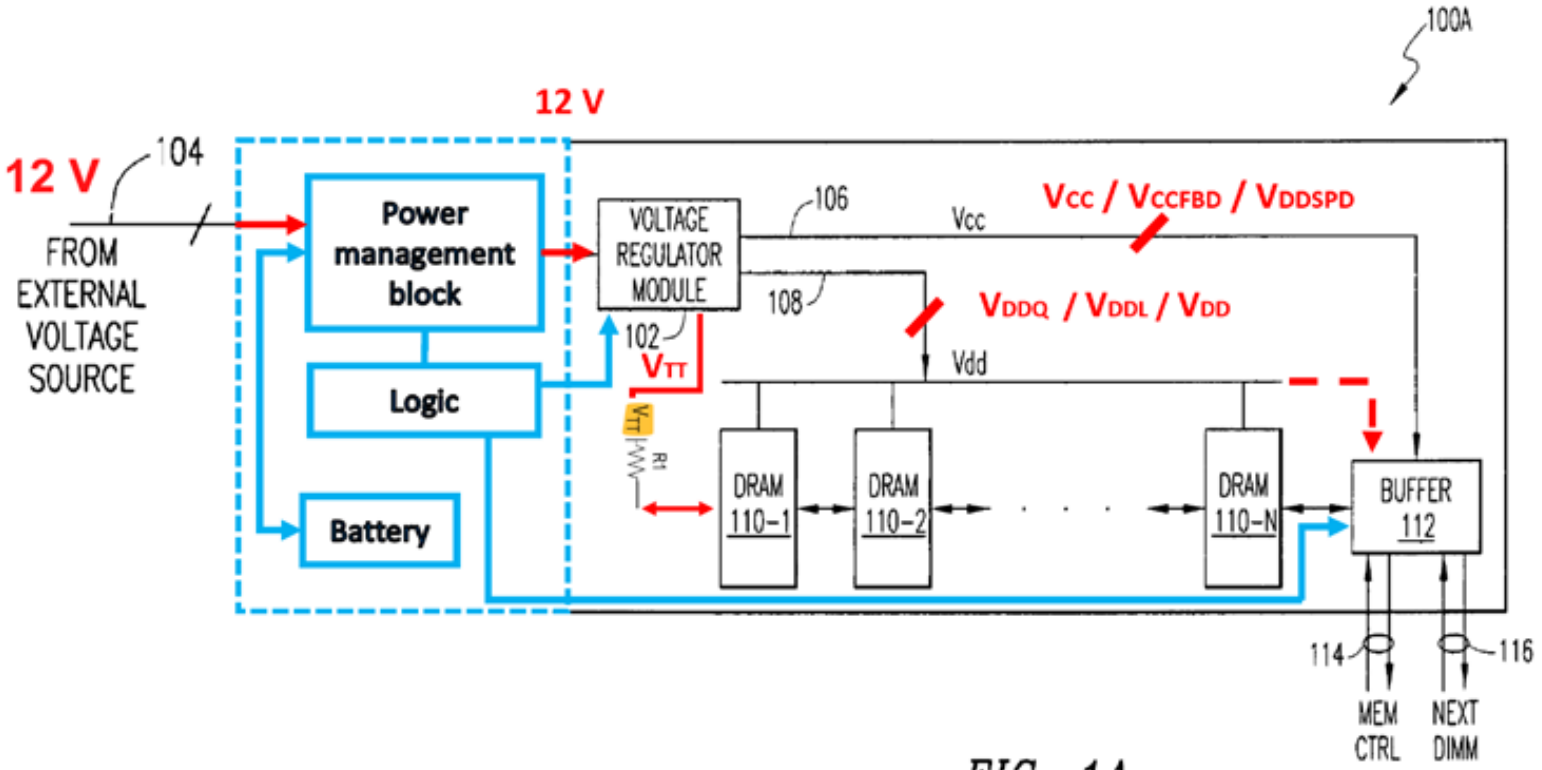


FIG. 1A

054 Mappings

Voltage Mapping (A)
1st : VDD / VDDQ = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VDDL = 1.8V
4th : VDDSPD = 3.3V

Voltage Mapping (B)
1st : VDD / VDDQ / VDDL = 1.8V
2nd : VCC = 1.5V
3rd : VCCFBD = 1.5V
4th : VDDSPD = 3.3V

Voltage Mapping (C)
1st : VDD / VDDQ / VDDL = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VTT = 0.9V
4th : VDDSPD = 3.3V

918 Mappings

Voltage Mapping (A)
1st : VDD / VDDQ = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VDDL = 1.8V
4th : VDDSPD = 3.3V

Voltage Mapping (B)
1st : VDD / VDDQ / VDDL = 1.8V
2nd : VCC = 1.5V
3rd : VCCFBD = 1.5V
4th : VDDSPD = 3.3V

Voltage Mapping (C)
1st : VDD / VDDQ / VDDL = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VTT = 0.9V
4th : VDDSPD = 3.3V

'918: Paper 1 (Pet.) at 52-56; Paper 25 (Reply) at 18-20
'054: Paper 1 (Pet.) at 41-45; Paper 26 (Reply) at 19-21

Ground 3: adds Hajeck

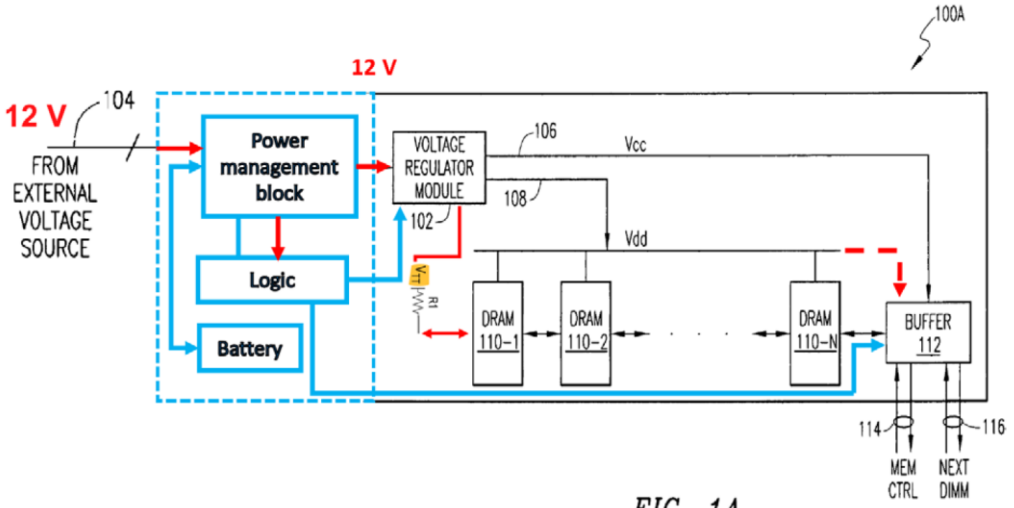


FIG. 1A

The voltage detection circuit **48** is responsible for detecting anomalies in the power signal V_{IN} supplied by the host on line **36**, and for driving the ready/busy signal to the "busy" state when such anomalies are detected. A conventional voltage detection circuit may be used. The voltage detection circuit **48** may be designed to generate a "busy" signal whenever V_{IN} falls below a certain level, such as 2.6 or 2.7 volts. The voltage detection circuit may also be designed to generate a busy signal when the voltage exceeds a certain level, and/or when other types of anomalies are detected. To inhibit rapid transitions between the "ready" and "busy" states, the voltage detection circuit may be designed to provide a degree of hysteresis, and/or to hold its output for a particular time period after a state transition.

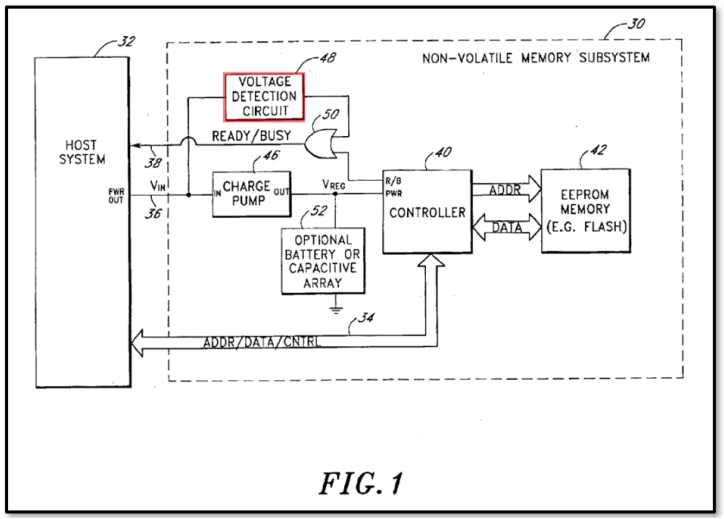


FIG. 1

Hajeck

- Teaches **voltage detection circuit**
- Specifically includes monitoring both **over**voltage and **under**voltage conditions

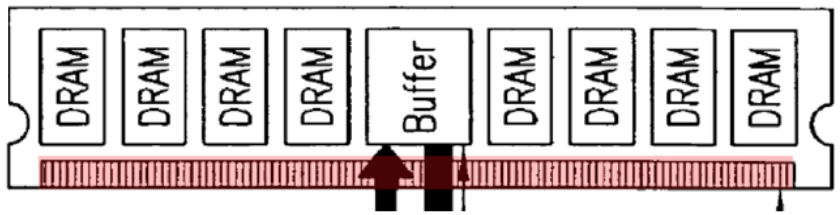
'918: Paper 1 (Pet.) at 12-13, 52-56, 75-76
'054: Paper 1 (Pet.) at 12-13, 41-45, 70-71

EDGE CONNECTIONS RECEIVE POWER FROM HOST

GROUND 1

(HARRIS + FBDIMM STANDARDS)

The Institution Decision correctly found that Ground 1 teaches "edge connections configured to couple power…signals"



EX1023, Fig. 3

Patent Owner argues that Petitioner has not made a *prima facie* case that Harris discloses a memory module having a PCB interface that receives power from the host system. Prelim. Resp. 14-20. Harris states, however, that DRAM devices may be "powered from system board or main board voltage sources." Ex. 1023 ¶ 2. Harris also discloses that "external voltage sources may comprise any combination of *known* or heretofore unknown voltage supplies, either regulated or unregulated, and even including variable voltages." Ex. 1023 ¶ 14 (emphasis added). Patent Owner does not argue that voltage supplied by a host system is not a "known" voltage supply as referenced by Harris. Furthermore, Petitioner indicates that the FBDIMM Standards show that the buffer AMB may be connected to a host, suggesting that the FBDIMM may derive its power from the host. Pet. 24 (showing figure at Ex. 1027, 4). These facts point to the conclusion that Harris's external voltage source may be the host system notwithstanding Patent Owner's arguments to the contrary.

'918: ID at 19-20
See also '054: ID at 19-20 (similar)

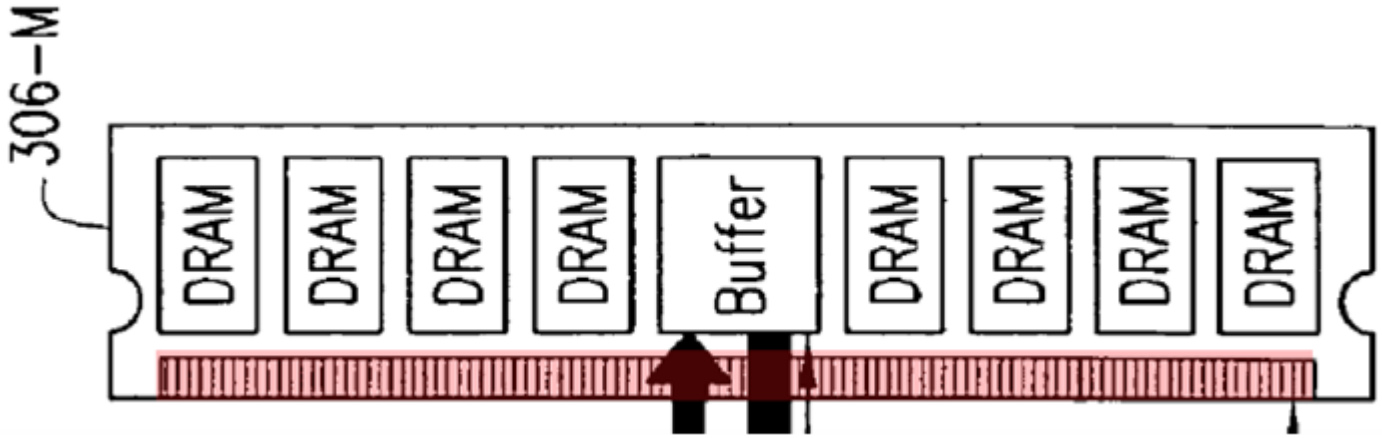
Harris teaches replacing standard "power supply interface pins" with fewer 12V pins

[0002] To cope with power requirements, industry standard memory modules, e.g., Dual In-line Memory Modules (DIMMS) populated with dynamic random access memory (DRAM) devices, are provided with power supply rails (on a relatively large number of pins) that are powered from system board or main board voltage sources, and are specific to the memory technology.

[0010] In accordance with the teachings of the present patent disclosure, at least one on-board voltage regulator module (VRM) is provided as part of the memory board assembly module **100**A for converting an externally supplied voltage level available on external source path **104** into appropriate local voltage levels that power the first and second voltage paths, i.e., the V_{dd} and V_{cc} paths **108**, **106**,

[0012] By way of example, a standard FBD module requires 28 V_{dd} pins (for DRAM devices) and 8 V_{cc} pins (for buffer and logic) and associated Ground returns, resulting in a total of 72 pins that provide a power supply interface for up to two x4 DRAM ranks (36 devices) and buffer logic. A voltage-independent FBD design incorporating the embodiment of **FIG. 1A** is capable of replacing these power supply interface pins with as few as six +12V pins (from an external voltage source), with local conversion to V_{dd} (to DRAM) and V_{cc} (to buffer/logic) being added. Alternatively, using

[0014] It should be readily recognized that the external voltage sources may comprise any combination of known or heretofore unknown voltage supplies, either regulated or unregulated, and even including variable voltages.

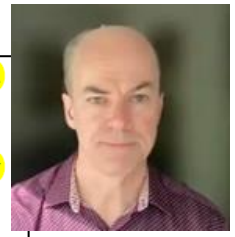


EX1023 (Harris), [0002], [0010], [0012], [0014], Fig. 3
'918: Paper 1 (Pet.) at 10; Paper 25 (Reply) at 2-7
'054: Paper 1 (Pet.) at 9-10; Paper 26 (Reply) at 2-8

Supplying power via edge connections was "standard"

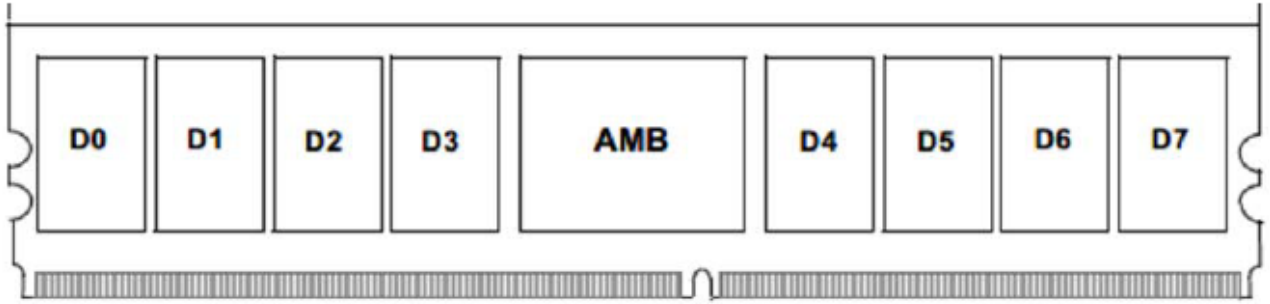
Q. You would agree that it's very common for a memory module to receive power from the edge connections along the bottom of the memory module that plugs into the host system; right?

A. Yes, that is standard approach. But Harris directly, in my opinion, teaches against that.



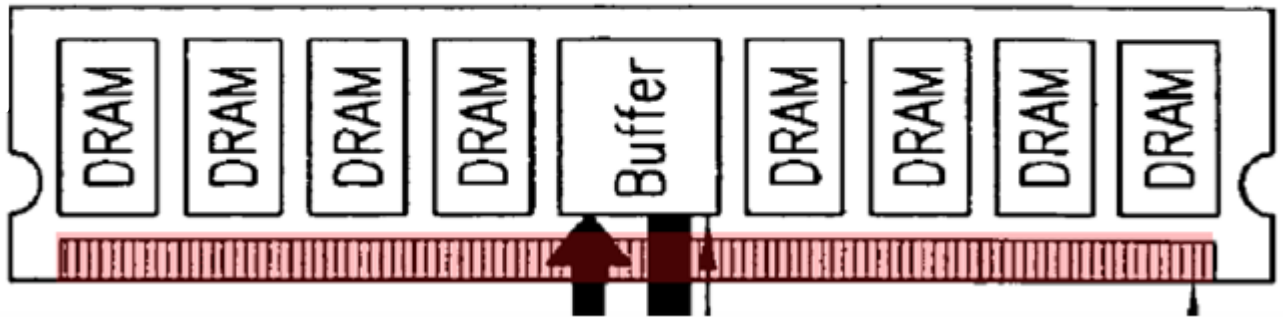
EX1075 (Mangione-Smith) at 163:16-22

FBDIMM:



EX1028 (JEDEC's FBDIMM Standards), p.38

Harris (FBDIMM):



EX1023 (Harris) at Fig. 3

'918: Paper 1 (Pet.) at 16-21; Paper 25 (Reply) at 2-7
'054: Paper 1 (Pet.) at 16-21; Paper 26 (Reply) at 2-8

Harris teaches supplying power from the host via edge connections

Q. And Figure 3 of Harris shows a memory controller 302 that's part of the host system; correct?

A. Yes, that's correct.

EX1075 (Mangione-Smith) at 167:23-168:1

[0017] **FIG. 3** is a block diagram of an exemplary memory assembly **300** according to one embodiment. A memory controller **302** is operable to drive a bidirectional memory link **304** to which a plurality of memory boards **306-1** through **306**-M are coupled in a daisy-chain fashion at their respective buffers. As exemplified by the memory board **306-3**, each memory board includes eight DRAM devices **312-1** through **312-8**, with a buffer component **314**. A clock source **308** is operable to drive a plurality of clock signals to the memory boards via a clock bus **314**. Additionally, the clock source **308** is also operable to drive a clock signal **316** to the memory controller **302** for providing a time base with respect to its operations. A system management bus (SM bus) **310** coupled to the memory boards **306-1** through **306**-M is driven by the memory controller **302**. Although not explicitly shown in this FIGURE, each memory board also receives a supply voltage that is locally converted by an on-board VRM for powering the DRAM and buffer components therein. In one arrangement, the supply voltage may be sourced from the memory controller **302** or from a separate voltage source.

EX1023 [0017], Fig. 3 (annotated)

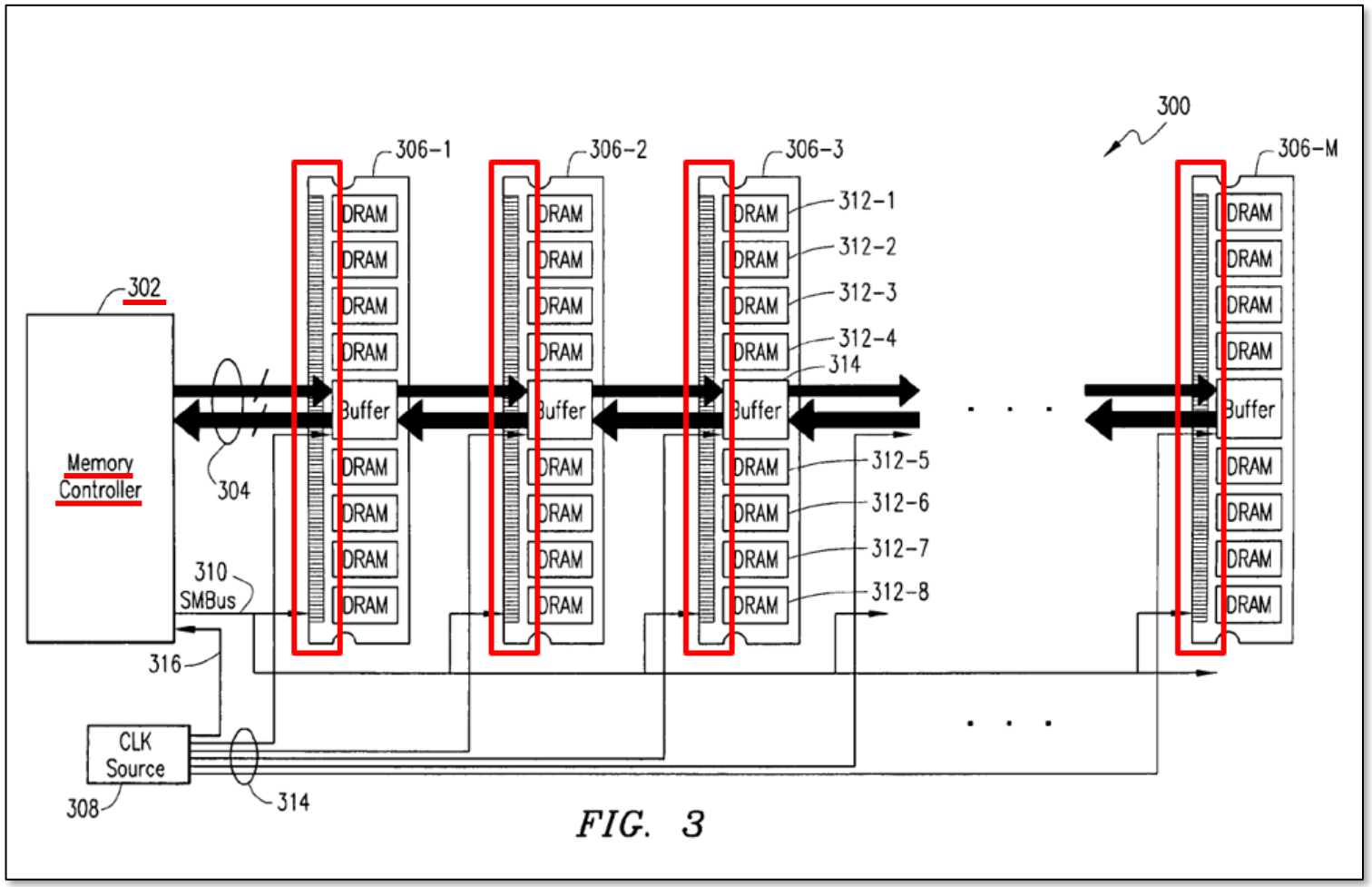
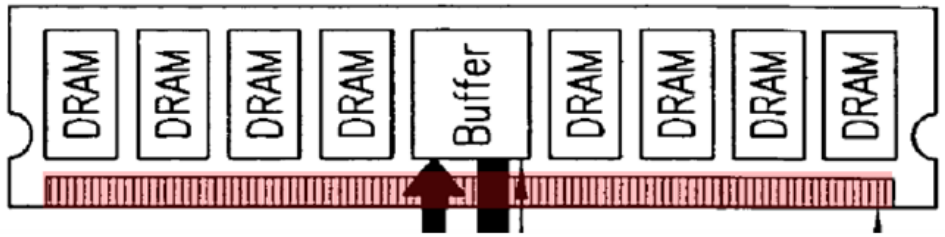


FIG. 3

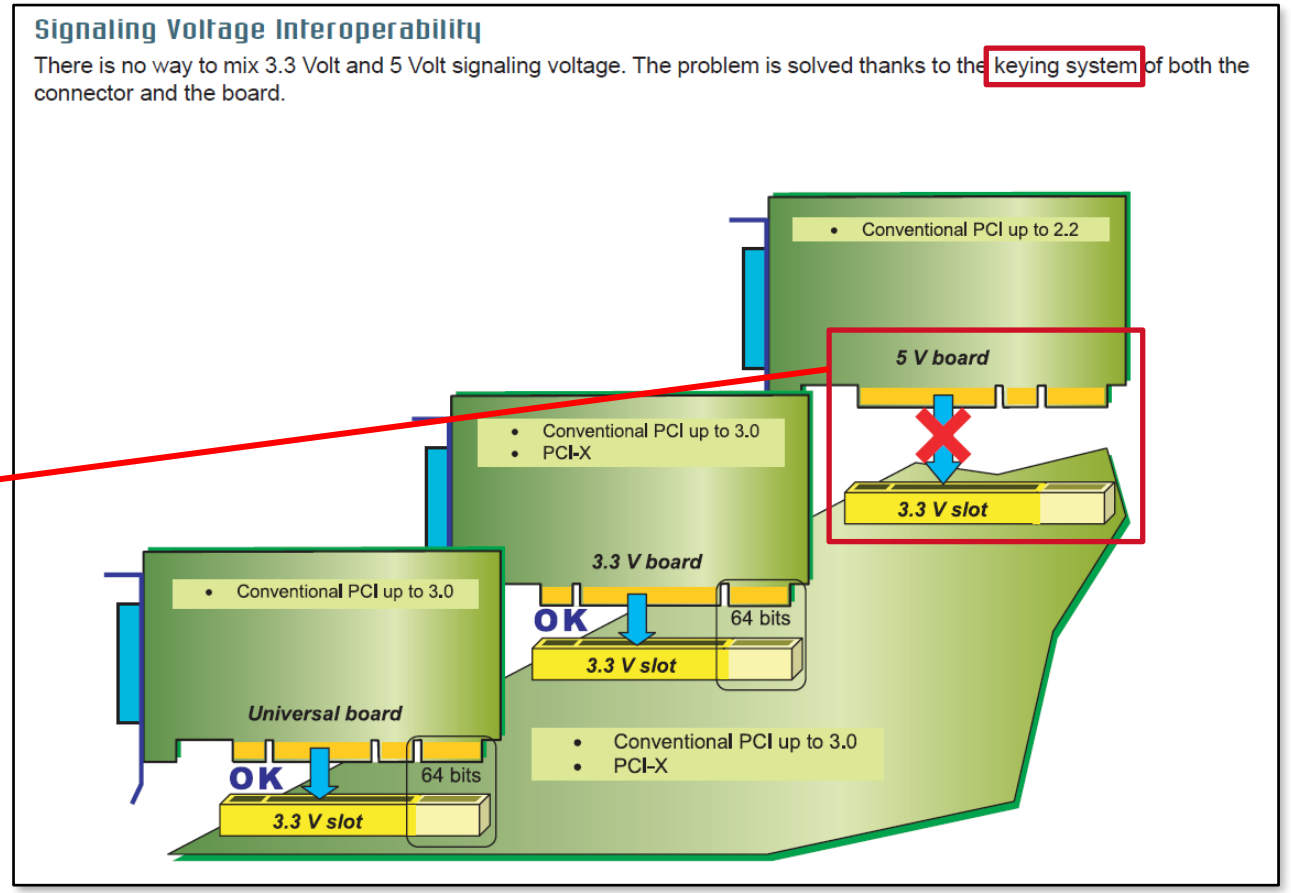
'918: Paper 25 (Reply) at 3-4
'054: Paper 26 (Reply) at 3-5

Harris's reference to removing the "keyway" confirms industry standard practice of supplying power using edge connections

[0013] It is contemplated that local supply voltage conversion for double-rank DIMMs can be accommodated with a form factor design of approximately about one square inch (both sides of the printed circuit board), and at a component height compatible with applicable Joint Electron Device Engineering Council (JEDEC) standards. Further, since the +12V power supply is not used directly by DRAM devices or buffer/logic components of the memory assembly, a wide tolerance (e.g., around +/−15%) can be accommodated, allowing low cost power distribution for system boards (such as, e.g., motherboards, cell boards, et cetera) wherein design requirements for bypass/hold-up capacitors may be relaxed or minimized. By way of an additional variation in implementation, the form factor associated with the memory assembly module **100**A may be suitably modified (e.g., removing the board's connector keyway) so as to ensure that a memory assembly module embodying the teachings of the present disclosure is not interchangeable with the standard DIMM, thereby preventing any accidental damage.



EX1023 at [0013], Fig. 3



EX2016 at 6-7; *see also* EX2030/2060, 117:7-:21; EX2101, 21-22; EX1075, 171:21-175:20

'918: Paper 25 (Reply) at 5-6
'054: Paper 26 (Reply) at 6-7

Harris's "external" voltage just needs to be external to the module

Q. Harris mentions external power source in, for example, Figure 1A; correct?

A. External voltage source.

Q. What is "external voltage source"?

A. It's one that comes from off the DIMM.

Q. So in your mind, a voltage source that comes from the host is also an external voltage source?

A. With respect to Harris' figures, I would think that's correct.

Q. And so when Harris mentions external source path 104, to you that just means a path to a voltage source that's off the DIMM; is that correct?

A. Yes.

EX2030/EX2060 (Wolfe) at 66:7-19

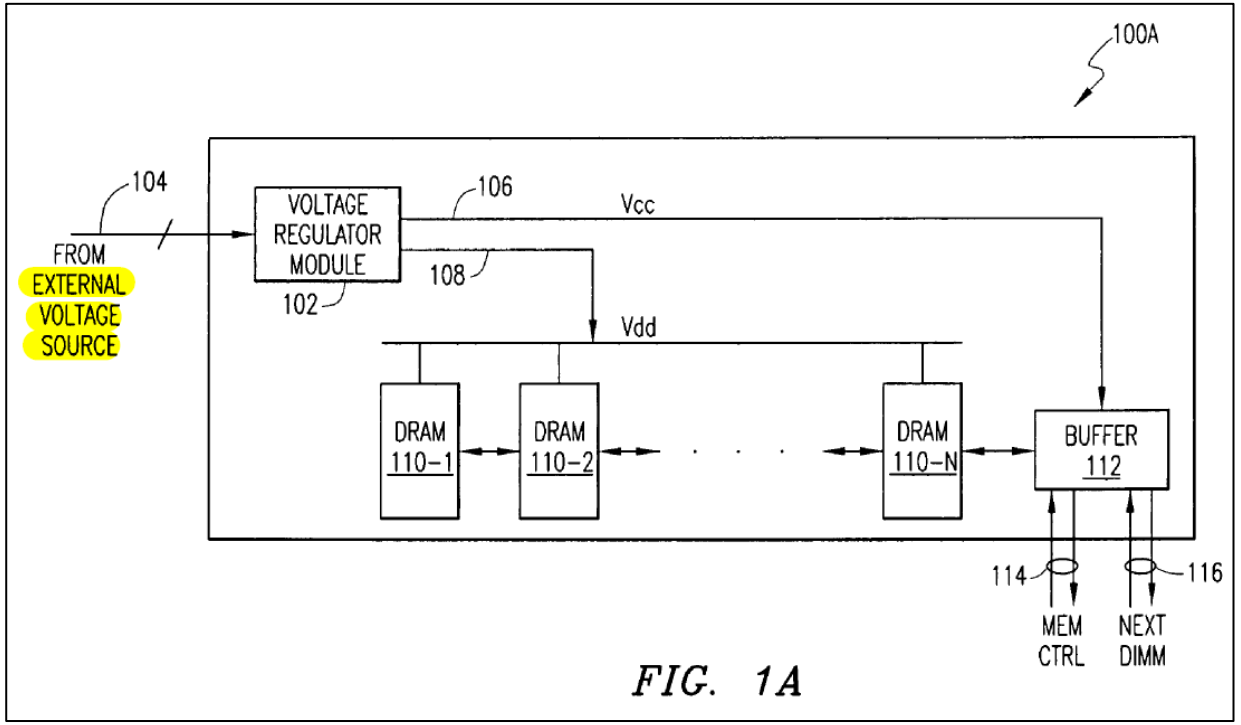


FIG. 1A

EX1023 (Harris) at Fig. 1A

'918: Paper 21 (POR) at 5; Paper 25 (Reply) at 2-7
'054: Paper 22 (POR) at 7; Paper 26 (Reply) at 2-8

Harris's "external" voltage can come from the host computer

Are you aware of any computer systems at the time of the invention that are suitable for use with FB-DIMM that provides unregulated supply voltages for the memory systems?

A. The one described in Harris.

Q. So you're assuming that the power supply for Harris FB-DIMM comes from the host system; correct?

MR. CHANDLER: Objection. Form.

THE WITNESS: I think a person of ordinary skill would generally assume that the external voltage source 104 comes from the host computer.

EX2030/EX2060 (Wolfe) at 91:22-92:7; *see also id.* 129:24-130:17

Q. Where in Harris does it disclose that the external voltage source comes from host system?

A. Well, I think there's a couple things that push us in that direction.

Q. Okay.

A. One is that Harris tells us that these are supplied on the DIMM pins. And normally, all the pins to a DIMM connect to the host. So that would lead one to expect that voltage to come from the host.

Secondly, there are claims on a computer system that describe that voltage that would be indicative. In general, the discussion of the external voltage source is in the context of a memory board assembly. So, again, that would lead one to think that it's external from the memory board assembly and not necessarily external from anything else.

And then on top of all that, I think there is just some commonsense that anyone who's designed or built a computer understands that there is typically a single-power supply, the host power supply, and that for both safety and convenience reasons, memories are powered from the host power supply, that it would be very difficult to make a safe and reliable system where memories were not powered by the computer system.

'054: Paper 26 (Reply) at 3
'918: Paper 25 (Reply) at 2

EX2030/EX2060 (Wolfe) at 67:20-68:21

Harris [0019] proposes eliminating board-specific power supply in favor of a "technology-independent" 12V supply, not eliminating all power from the host

[0019] Based on the foregoing Detailed Description, it should be appreciated that an implementation of the embodiments described herein thus provides a technology-independent voltage distribution scheme for memory devices wherein system board power supply and associated voltage plane(s) are eliminated. Accordingly, power supply design's complexity as well as the cost of memory-specific power distribution are reduced. Cost savings may include, for example, elimination of system-board-specific power supply or regulator output, associated bypass capacitor arrangements, heavy etch or power planes. Also, under the technology-independent voltage distribution scheme disclosed herein, cost of memory power regulation scales with populated memory devices, rather than being pre-provisioned for maximum memory capacity as is typically the case in existing systems. Additionally, one or more of the following advantages may be realized in an exemplary voltage distribution embodiment: provision of tighter, lower inductance regulation which decreases voltage variability and increases timing margins; reduction in the pin count on DIMM connector to system board or memory riser card (whereby a smaller connector or wider pin spacing may be accommodated); improved signal integrity due to reduced crosstalk on the same size connector; and reservation of extra pins for implementing additional standard or proprietary functions.

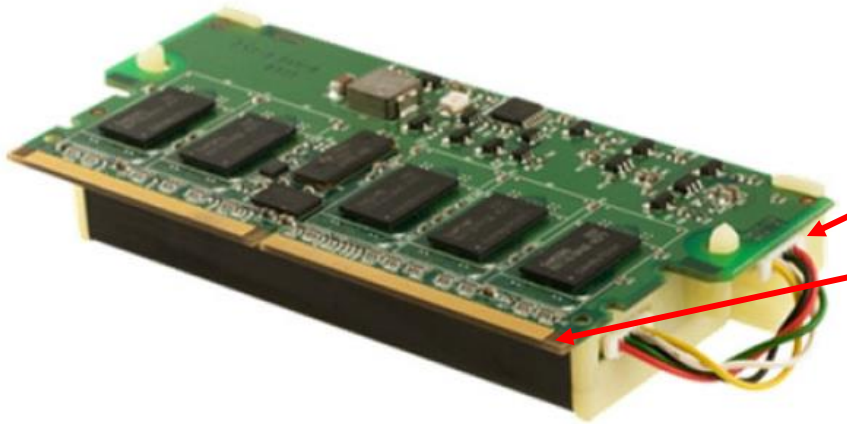
[0020] Because voltage-independent embodiments disclosed herein can provide upgradeability and extensibility without changing system board power distribution, transitioning to newer DRAM technologies (e.g., at lower operating voltages) is more cost-effective as well as simpler to implement. Further, the embodiments are amenable to dual +12V power supply rail implementations so that industry-standard form factors can be advantageously accommodated.

EX1023 at [0019-0020]
'918: Pet. 19; EX1003, ¶221
'054: Pet. 19; EX1003, ¶222

Netlist misinterprets paragraph [0019] of Harris to conclude that "system board power supply…[is] eliminated" ***entirely***. POR 4-5, 8, 10-11. To the contrary, Harris proposes avoiding the need for ***different*** system board voltages — such as "3.3V, 2.5V, 1.8V, 1.5V and beyond," EX1023, [0002] — by simply supplying a ***single*** voltage (i.e., "12V")[2] to the memory module, *id.* [0012-13], so that an "on-board voltage regulator module [e.g., 102 above] [can] generate appropriate local voltage levels" on the memory module, *id.* [0003]. As Dr. Wolfe explained, Harris's "technology-independent voltage distribution scheme" eliminates the need for a "system-***board-specific*** power supply," *id.* [0019], not all power, EX2030, 116:10-117:6.

'918: Paper 25 (Reply) at 4-5
'054: Paper 26 (Reply) at 5-6

Netlist's expert admits that it was known to use a side connector to a battery, and an edge connector to the host, making both obvious



EX2035, 39

Q. Last page of Exhibit 2035 it shows BBvault, which you reference in paragraph 59 of your declarations; correct?
A. Yes, that's correct.
Q. BBvault is a memory module that was released back in 2005; correct?
A. Yes, that's correct.
Q. And the side connection on the BBvault memory module connects to a battery backup; correct?
A. Yes.
Q. And in addition to that side connection on BBvault, there is also edge connections along the bottom of the memory module that permit BBvault to plug in to a host system and receive power along the edge connections on the bottom of the memory module; correct?
A. Yes, that's correct.
Q. So the side connection on the BBvault memory is for battery backup, while the edge connections along the bottom of the memory module are for power from the host system; correct?
A. Yes. The side connections are -- go to the battery backup and are used when the power coming in from the host system along the edge connectors is not used.
Q. And this was known by 2005; correct?
A. Yes.

EX1075 (Mangione-Smith) at 165:10-166:12

"[J]ust because 'better alternatives' may exist in the prior art 'does not mean that an inferior combination is inapt for obviousness purposes.'"

Dome Pat. L.P. v. Lee, 799 F.3d 1372, 1381 (Fed. Cir. 2015)

'918: Paper 25 (Reply) at 2-7
'054: Paper 26 (Reply) at 2-8

DATA, ADDRESS, AND CONTROL SIGNALS FROM THE HOST

GROUND 1

(HARRIS + FBDIMM STANDARDS)

The Institution Decision correctly found that Ground 1 teaches "data, address and control signals between the memory module and the host system"

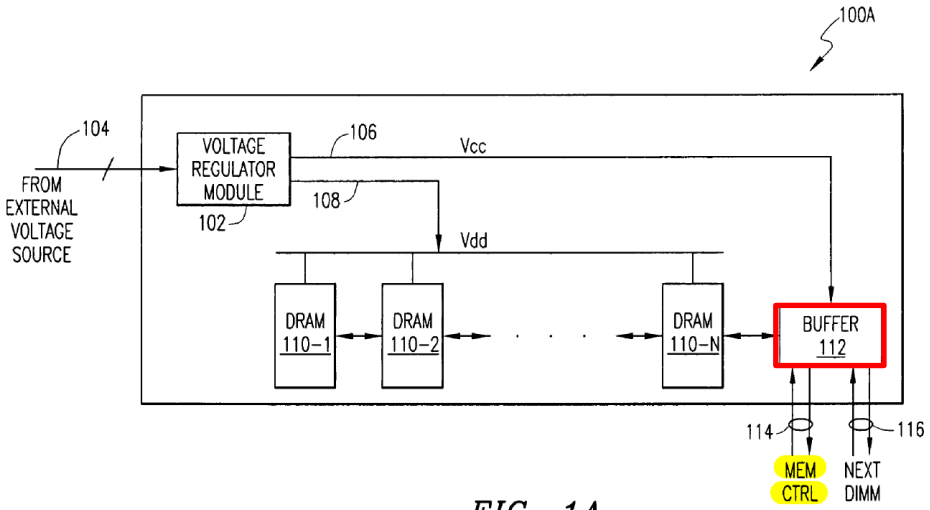


FIG. 1A

EX1023, Fig. 1A

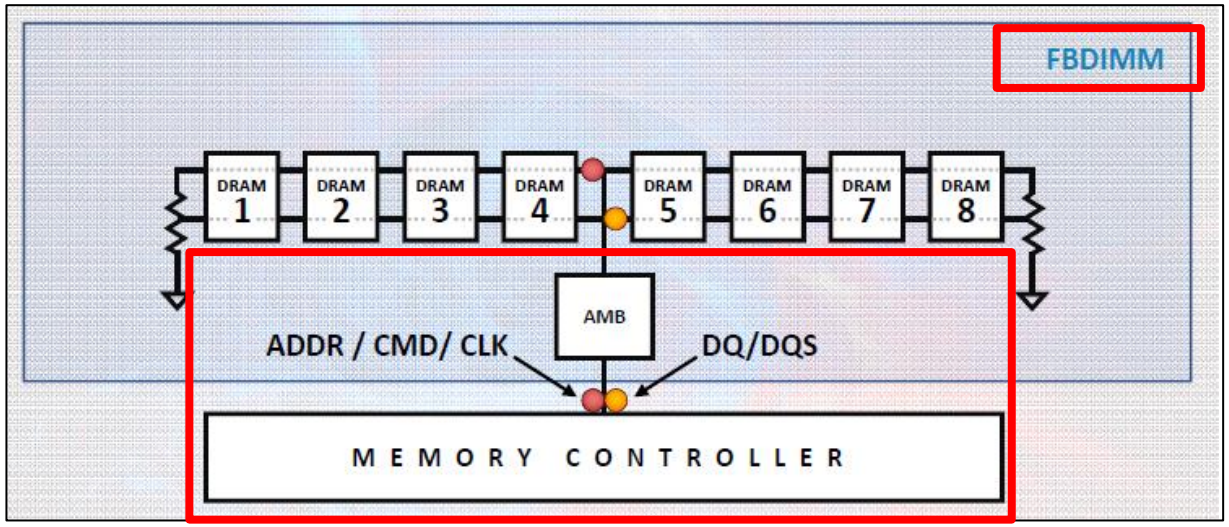
Petitioner further contends that Harris, consistent with the FBDIMM Standards, discloses that the edge connections are "configured to couple power, data, address and control ***signals*** between the memory module and the host system." Pet. 21–25. Petitioner contends that the power signal corresponds to Harris's voltage 104 in Figure 1A. Id. at 21 (citing Ex. 1023 ¶¶ 10, 12, 19). Petitioner contends that Harris's buffer 112 in Figure 1A is called "AMB" (Advanced Memory Buffer) in the FBDIMM Standards. Pet. 23–24. Petitioner indicates that Harris's buffer 112 receives data, address, and control ***signals*** via memory controller interface 114 and transmits these signals to DRAMs 110-1 to 110-N in Figure 1A. Pet. 22–25 (citing Ex. 1023 ¶ 9 ("buffer/logic component 112 is provided for buffering command/address (C/A) space as well as data space at least for a portion of memory devices 110-1 through 110-N"). In addition, Petitioner argues that the FBDIMM Standards indicate that buffer AMB receives data ***signals*** DQ0–DQ63; address ***signals*** A0–A15; and control ***signals*** RAS, CAS, WE, CS, etc. Pet. 22–23 (citing Ex. 1028, 13).

. . . .

Based on our review and consideration of the current record, we determine that Petitioner has adequately shown that the combination of Harris and the FBDIMM Standards teaches this limitation for purposes of institution.

'918: ID at 18-20 (emphasis added)
See also '054: ID at 18-20 (similar)

The AMB Buffer in an FBDIMM (like Harris) receives data, address, and control signals from the host



EX1077 at 9

Q. So when the host computer wants to send a read or write command to an FBDIMM, that read or write command and the associated address information is sent as packetized serial signals; correct?

A. Yes, that's correct.

Q. And similarly, when the host computer wants to send data to an FBDIMM that data is sent as packetized serial signals; correct?

A. Yes, that's correct.

Q. And then in the fourth line of paragraph 31 of your declarations, you explain that the AMB on the FBDIMM receives the data address and control information that was sent by the host computer using packetized serial signals; and the AMB decodes that information and generates the data address and control signals needed by the DDR2 SDRAM memory devices; correct?

A. Yes, that's correct. That's what it says.

EX1075 (Mangione-Smith) at 156:4-:23; *see also id.* at 219:2-:11 ("signals")

'054: Paper 26 (Reply) at 8-9
'918: Paper 25 (Reply) at 7-8

The AMB Buffer in an FBDIMM (like Harris) receives data, address, and control signals from the host

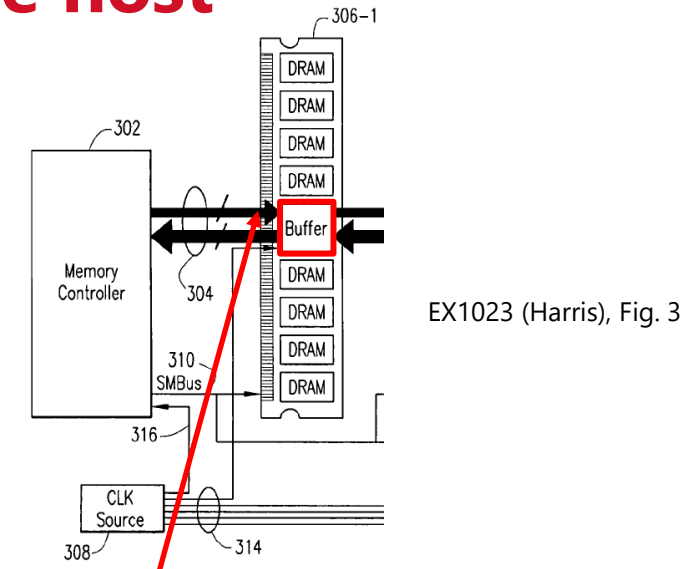
1.1 Advanced Memory Buffer Overview

The Advanced Memory Buffer (AMB) reference design complies with the *FB-DIMM Architecture and Protocol Specification* . It supports DDR2 SDRAM main memory. The Advanced Memory Buffer allows buffering of memory traffic to support large memory capacities. All memory control for the DRAM resides in the host, including memory request initiation, timing, refresh, scrubbing, sparing, configuration access, and power management. The Advanced Memory Buffer interface is responsible for handling FBD channel and memory requests to and from the local DIMM and for forwarding requests to other DIMMs on the FBD channel.

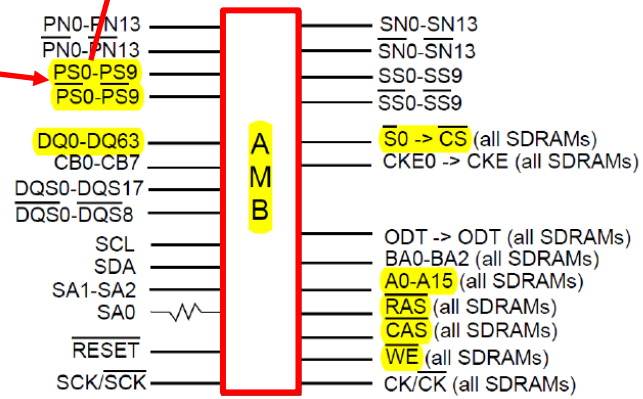
- Acts as DRAM memory buffer for all read, write, and configuration accesses addressed to the DIMM.

Signal	Type	Description
Channel Interface		
PN[13:0]	O	**Northbound Output Data:** High speed serial signal. Read path from AMB toward host on primary side of the DIMM connector.
$\overline{PN}$[13:0]	O	Northbound Output Data Complement
SN[13:0]	I	**Northbound Input Data:** High speed serial signal. Read path from the previous AMB toward this AMB on secondary side of the DIMM connector.
$\overline{SN}$[13:0]	I	Northbound Input Data Complement
PS[9:0]	I	**Southbound Input Data:** High speed serial signal. Write path from host toward AMB on primary side of the DIMM connector.
DQ[63:0]	I/O	Data
DQS[17:0]	I/O	**Data Strobe:** DDR2 data and check-bit strobe.
$\overline{DQS}$[17:0]	I/O	**Data Strobe Complement:** DDR2 data and check-bit strobe complements.
A0A-A15A, A0B-A15B	O	**Address:** Used for providing multiplexed row and column address to SDRAM.
BA0A-BA2A, BA0B-BA2B	O	**Bank Active:** Used to select the bank within a rank.
$\overline{RASA}$, $\overline{RASB}$	O	**Row Address Strobe:** Used with $\overline{CS}$, $\overline{CAS}$, and $\overline{WE}$ to specify the SDRAM command.
$\overline{CASA}$, $\overline{CASB}$	O	**Column Address Strobe:** Used with $\overline{CS}$, $\overline{RAS}$, and $\overline{WE}$ to specify the SDRAM command.
$\overline{WEA}$, $\overline{WEB}$	O	**Write Enable:** Used with $\overline{CS}$, $\overline{CAS}$, and $\overline{RAS}$ to specify the SDRAM command.
$\overline{CS0A}$-$\overline{CS1A}$, $\overline{CS0B}$-$\overline{CS1B}$	O	**Chip Select:** Used with $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ to specify the SDRAM command. These signals are used for selecting one of two SDRAM ranks. $\overline{CS0}$ is used to select the first rank and $\overline{CS1}$ is used to select the second rank.

EX1027 at pp. 1, 81-82



EX1023 (Harris), Fig. 3



EX1028 at p. 13

'918: Pet. at 22-25; Paper 25 (Reply) at 7-8
'054: Pet. at 22-25; Paper 26 (Reply) at 8-9

The claims require "signals," not "dedicated pins"

The claims require "signals"	. . . . not "dedicated pins"
['918 claim 1] A memory module comprising: a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple ***power, data, address and control signals*** between the memory module and the host system; **['054 claim 1]** 1. A memory module comprising: a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple ***power, data, address and control signals*** between the memory module and the host system;	BY [NETLIST] ATTORNEY LINDSAY: Q. Are there any ***pins that are dedicated to data*** signals shown in the table in -- that you just described? THE WITNESS: No, I don't believe so. Q. Are there any ***dedicated address pins*** in the table that you just described? THE WITNESS: No. There are ***no dedicated address signal pins*** shown in this table. Q. And are there any ***dedicated control signal pins*** shown in the table? THE WITNESS: No, there are ***no dedicated control signal pins*** shown in this table. EX1075 (Mangione-Smith) at 214:24-215:20 (objections omitted)

'054: Paper 26 (Reply) at 8-9
'918: Paper 25 (Reply) at 7-8

Netlist's theory would exclude FBDIMMs, contrary to the preferred embodiment of the '918 and '054 Patents

'918 and '054 Patents

> Other form factors including, but not limited to, small-outline (SO-DIMM), unbuffered (UDIMM), registered (RDIMM), fully-buffered (FB-DIMM), miniDIMM, mini-RDIMM, VLP mini-DIMM, micro-DIMM, and SRAM DIMM are also compatible with certain embodiments described herein.

918: EX1001 at 21:46-51
054: EX1001 at 21:46-51

"A claim construction that excludes a preferred embodiment is ***rarely, if ever correct*** and would require highly persuasive evidentiary support."

Kaufman v. Microsoft Corp., 34 F.4th 1360, 1372 (Fed. Cir. 2022) (emphasis added)

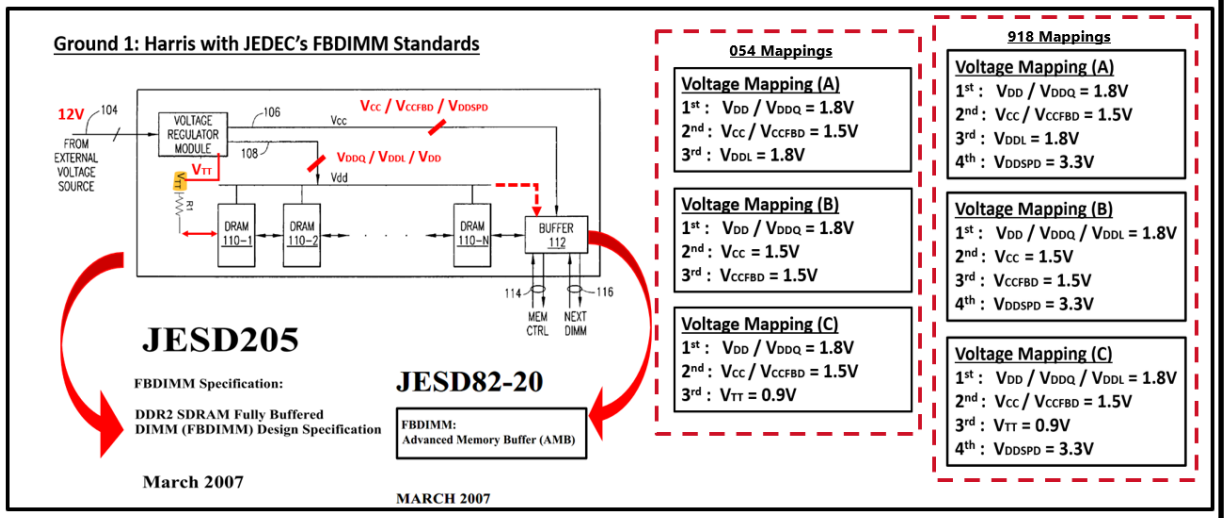
'054: Paper 26 (Reply) at 9-10
'918: Paper 25 (Reply) at 8-9

OBVIOUS TO USE THREE (‘054) OR FOUR (‘918) BUCK CONVERTERS

GROUND 1

(HARRIS + FBDIMM STANDARDS)

The Institution Decision correctly found that Ground 1 renders obvious the use of four buck converters



Patent Owner argues that Harris requires at most two or three buck converters to provide the voltages needed and thus, does not disclose the four claimed converters. Prelim. Resp. 20-25. Specifically, Patent Owner contends that Harris discloses a single converter generating two regulated voltages, so Harris does not disclose four converters as claimed. Prelim. Resp. 21-22. Petitioner showed sufficiently that the FBDIMM Standards mentioned in Harris call for at least four voltages, and that given Harris's teaching of a converter, it would have been obvious to one of ordinary skill in the art to use multiple converters, including well-known buck converters, to generate the four voltages needed. Pet. 26-31. . . .

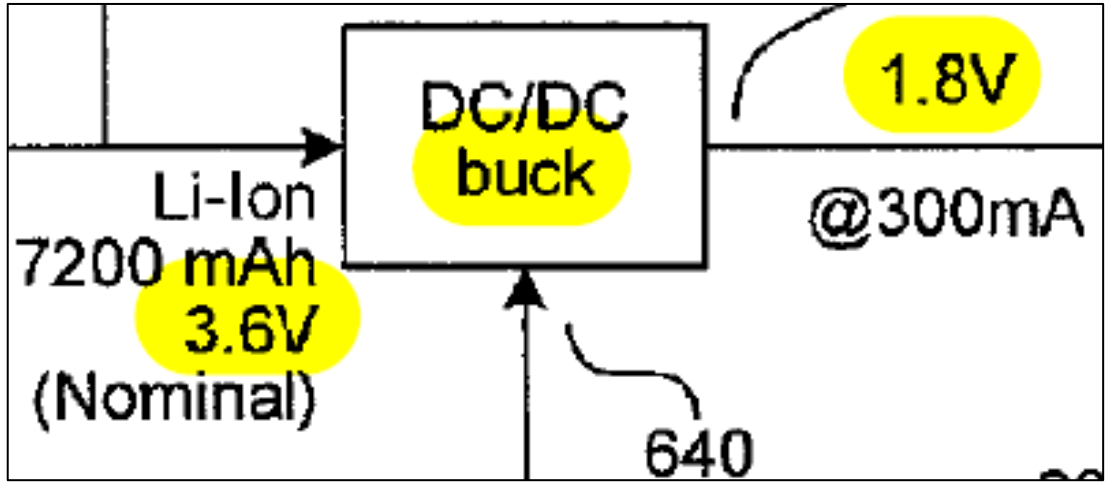
Patent Owner contends that Petitioner did not make the case that a person of ordinary skill in the art would have used a third buck converter, as opposed to a linear regulator, to provide termination voltage VTT. Prelim. Resp. 29–33. Petitioner explained sufficiently that "buck converters" were well-known as a highly-efficient way to step down voltages without generating excess heat or requiring large cooling devices, providing further motivation to use buck converters. Pet. 29–30.

'918: ID at 22-24
See also '054: ID at 20-23 (similar, 3 converters)

Obvious to use buck converters to provide lower, regulated voltages

[0010] Preferably, a high-frequency switching voltage converter capable of generating tightly-controlled voltage levels may be implemented as the on-board VRM **102** for purposes of the present patent disclosure. For instance, multi-phase synchronous Pulse-Width Modulated (PWM) controllers, Low Drop-Out (LDO) controllers, et cetera, that are capable of accepting unregulated supply voltages in a broad range may be configured to operate as a local voltage supply for the memory module **100**A.

EX1023 (Harris) at [0010]



EX1024 (Amidi) at Fig. 6

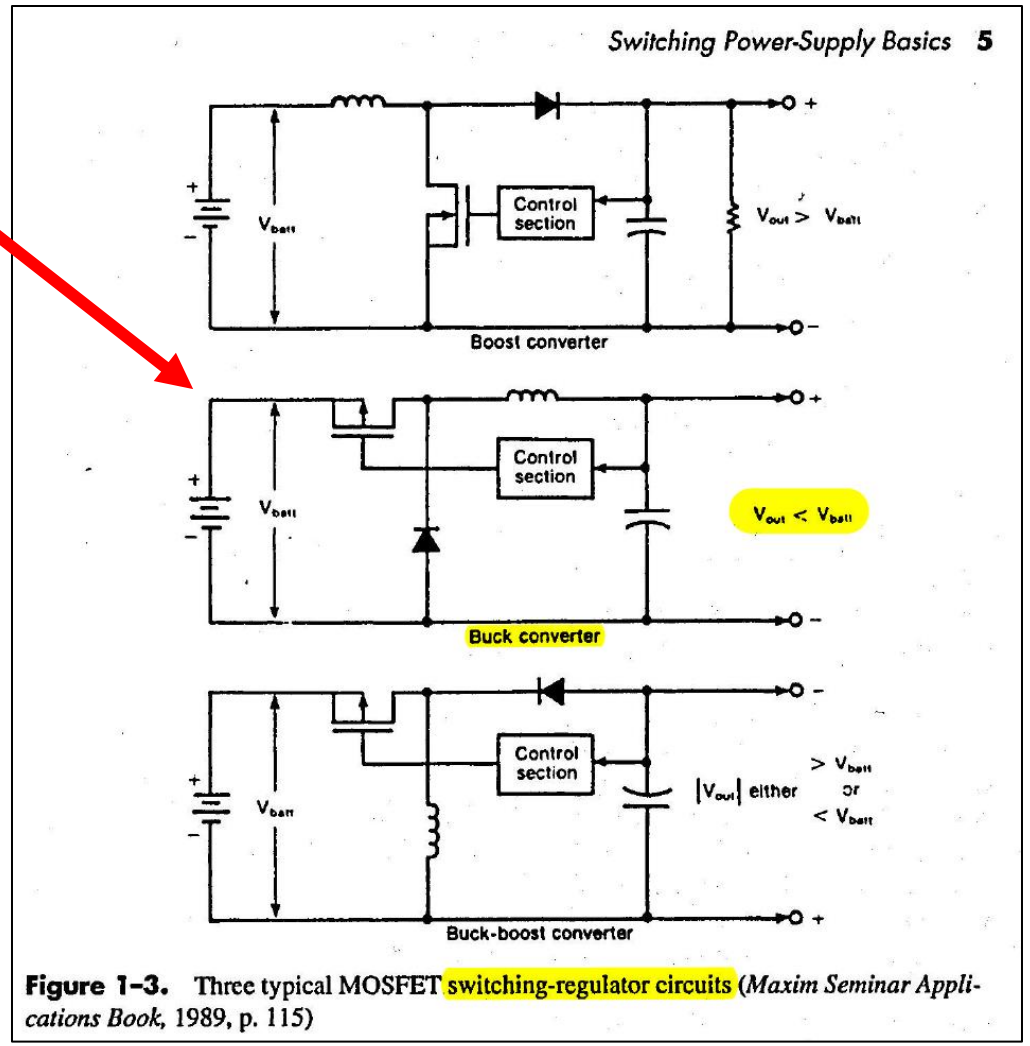


Figure 1-3. Three typical MOSFET switching-regulator circuits (*Maxim Seminar Applications Book*, 1989, p. 115)

EX1058 at p. 5; *see also* EX1075 (Mangione-Smith) at 103:21-111:17

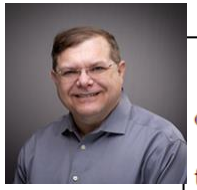
'918: Paper 1 (Pet.) at 29-30 and 90-91; Paper 25 (Reply) at 10, 18 and 29-30
'054: Paper 1 (Pet.) at 29-30 and 85-86; Paper 26 (Reply) at 11, 19 and 30-31

Obvious to use buck converters to provide lower, regulated voltages

Q. All right. Would you agree that buck converters were known in the art by the time of the '918 and '054 patents?

A. Yes. For example, I was familiar with them at least as -- back in the 1996 time frame.

EX1075 (Mangione-Smith) at 104:23-105:2



Q. And you did not provide any analysis on the cost of buck converters versus LDOs that can be used to generate the needed voltage rail; correct?

MR. CHANDLER: Object to form.

THE WITNESS: Not a specific comparison, other than to say that both are available at very low cost today and both would be feasible to provide SPD power, and that the trend over the years has been to move all computer power supplies to buck converters.

EX2030/EX2060 (Wolfe) at 140:15-24

Further, "buck converters" were well-known as a ***highly-efficient*** way to step down voltages without generating excess heat or requiring large cooling devices, providing a further motivation (beyond Harris's express disclosure above) to implement Harris's voltage regulator using "*[buck] converter[s].*" EX1003, ¶237; EX1059, 5:23-30 ("***Switch mode buck converters*** have become popular due to two attractive features: first, they are ***more efficient*** than traditional low drop out regulators (LDO) (e.g., up to 95%) and second, ***they can provide relatively high currents with lower power dissipation on chip than an LDO can.***"); EX1058, p.5 (explaining the "***high efficiency*** of switching regulators"); *see also, e.g.*, EX1040, pp.1 ("high efficiency"), 23-24 (Figs.22-25); EX1041, pp. 1, 13 ("high efficiency"); EX1048, p.3; EX1062, p.11; EX1064, ¶[0101].

918: Pet. at 29-30

054: Pet. at 29 (similar)

'918: Paper 1 (Pet.) at 29-30 and 90-91; Paper 25 (Reply) at 10, 18 and 29-30

'054: Paper 1 (Pet.) at 29-30 and 85-86; Paper 26 (Reply) at 11, 19 and 30-31

Obvious to use buck converters to provide lower, regulated voltages

"[J]ust because 'better alternatives' may exist in the prior art 'does not mean that an inferior combination is inapt for obviousness purposes.'"

Dome Pat. L.P. v. Lee,
799 F.3d 1372, 1381 (Fed. Cir. 2015)

"[I]t's not necessary to show that a combination is the *best* option, only that it be a ***suitable*** option."

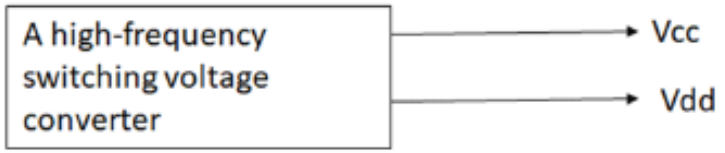
Intel Corp. v. PACT XPP Schweiz AG,
61 F.4th 1373, 1380-81 (Fed. Cir. 2023)
(reversing Board)

'918: Paper 25 (Reply) at 18 and 29-30
'054: Paper 1 (Pet.) at 29-30 and 85-86; Paper 26 (Reply) at 19 and 30-32

1. Harris is not limited to one buck converter

Netlist argues Harris is limited to one buck converter…

Harris expressly discloses using a ***single*** converter to provide at least two of the voltages in each of Petitioner's voltage mappings. EX2031, ¶¶75-79. Specifically, Harris discloses "***a*** high-frequency switching voltage converter capable of generating tightly-controlled voltage level**s**." EX1023, FIG. 1A, [0010]



'918: Paper 21 (POR) at 18-19
'054: Paper 22 (POR) at 20-21

…but Harris teaches "*at least* one"…

[0010] In accordance with the teachings of the present patent disclosure, ***at least one*** on-board voltage regulator module (VRM) is provided as part of the memory board assembly module 100A…. Preferably, ***a*** high-frequency switching voltage converter capable of generating tightly-controlled voltage levels may be implemented as the on-board VRM 102 for purposes of the present patent disclosure. . . .

What is claimed is: 1. A memory board assembling, comprising: . . . ***at least one*** voltage regulator module.

… and "a" is interpreted as "one or more"

"[T]his court has repeatedly emphasized that an indefinite article ***'a' or 'an'*** in patent parlance ***carries the meaning of 'one or more'*** in open-ended claims containing the transitional phrase 'comprising.' " That "a" or "an" can mean "one or more" is best described as a rule, rather than merely as a presumption or even a convention.

Baldwin Graphic Sys., Inc. v. Siebert, Inc., 512 F.3d 1338, 1342-43 (Fed. Cir. 2008)

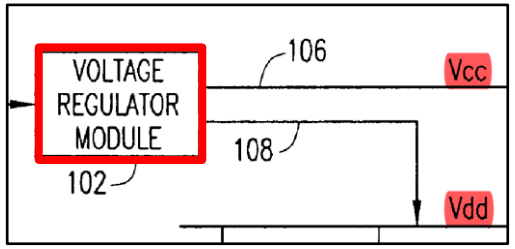
'918: Paper 25 (Reply) at 10-13
'054: Paper 26 (Reply) at 11-14

1. Harris is not limited to one buck converter — Figure 1A shows multiple buck converters

What Netlist calls one converter (with two outputs)…

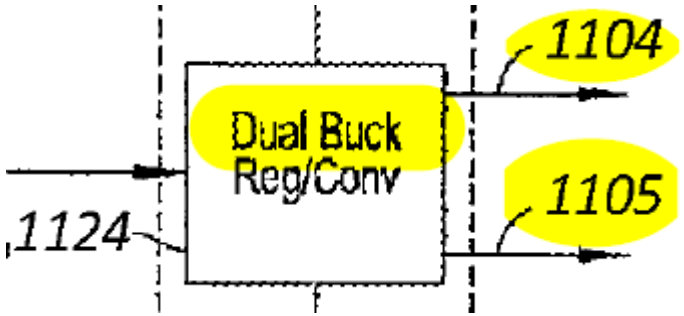
Harris expressly discloses using a ***single*** converter to provide at least two of the voltages in each of Petitioner's voltage mappings. EX2031, ¶¶75-79. Specifically, Harris discloses "***a*** high-frequency switching voltage converter capable of generating tightly-controlled voltage level***s***." EX1023, FIG. 1A, [0010]

'918: Paper 21 (POR) at 18-19
'054: Paper 22 (POR) at 20-21



EX1023 (Harris) at Fig. 1A

…is two converters according to the 918/054 Patent…



See also EX1075 (Mangione-Smith) at 117:25-118:16

2. The memory module of claim 1, wherein the ***first and third*** buck converters are further configured to operate as a ***dual buck converter***.

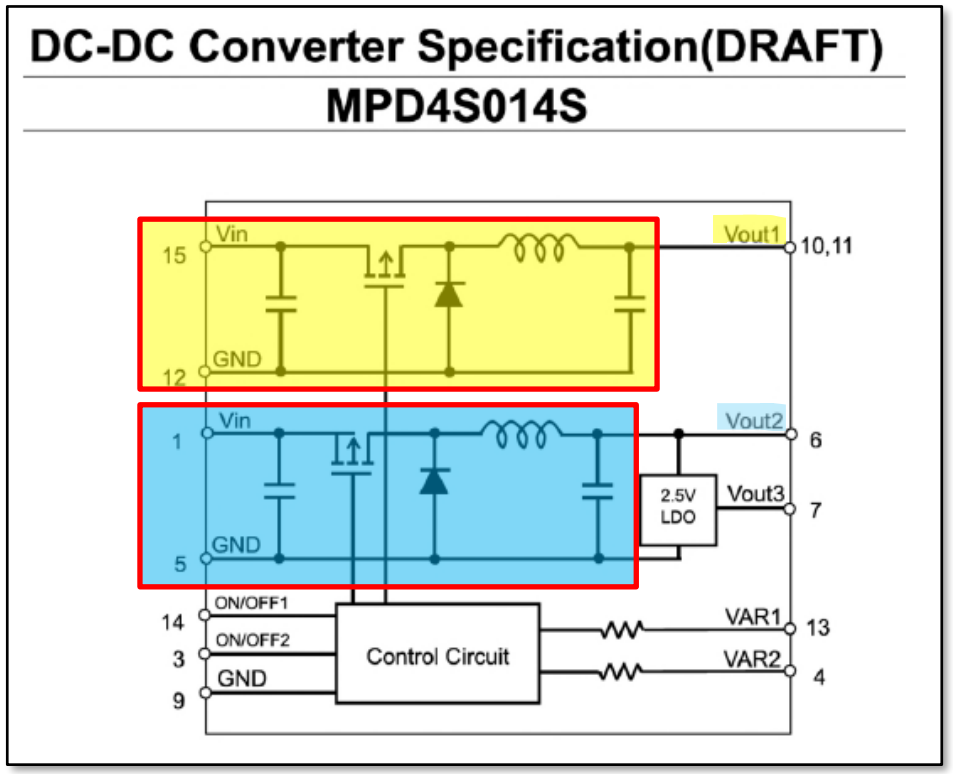
… and has been construed as two converters (given the two outputs)

Term	The Court's Construction
"dual buck converter" ('918 Patent, Claims 2, 17, 28) "dual-buck converter" ('054 Patent, Claim 15)	"a buck converter with two regulated voltage outputs"

EX2032, 34; *see also id.* 18-21;
EX1075, 124:22-125:8, 126:9-:18; EX2030, 97:13-98:3

'918: Paper 25 (Reply) at 10-13
'054: Paper 26 (Reply) at 11-14

1. Harris is not limited to one buck converter — it was common for a single chip to have multiple buck converters



EX1048 at 2

Q. Does page 2 of Exhibit 1048 show two buck converters operating as a dual buck converter?

A. It does not label that as a dual buck converter. In fact, it doesn't label it as a buck converter, but it is indeed two buck converters.

Q. With two regulated output voltages?

A. Pardon me?

Q. With two regulated output voltages; correct?

A. Yes, that's correct.

EX1075 (Mangione-Smith) at 129:13-:24

'918: Paper 25 (Reply) at 10-13
'054: Paper 26 (Reply) at 11-14

1. Harris is not limited to one buck converter — it was common for a single chip to have multiple buck converters

As another example, Fairchild offered a FAN5026 "***Dual-Output*** PWM Controller" with two different outputs (each anywhere from 0.9V to 5.5V), such as 2.5V and 1.8V similar to Ground 1A or 1B, or V_{DDQ} and V_{TT} like Ground 1C:

FAIRCHILD SEMICONDUCTOR®

October 2005

FAN5026
Dual DDR/Dual-Output PWM Controller

Circuit Description

Overview

The FAN5026 is a multi-mode, dual channel PWM controller intended for graphic chipset, SDRAM, DDR DRAM or other low output voltage power applications in PC's, VGA Cards and set top boxes. The IC integrates a control circuitry for two synchronous buck converters. The output voltage of each controller can be set in the range of 0.9V to 5.5V by an external resistor divider.

Applications

- DDR V_{DDQ} and V_{TT} voltage generation

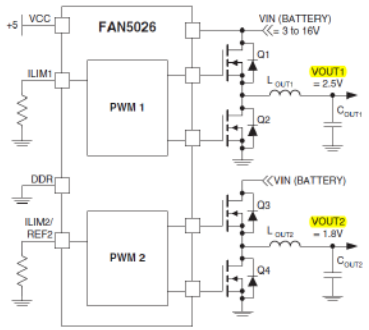


Figure 1. Dual Output Regulator

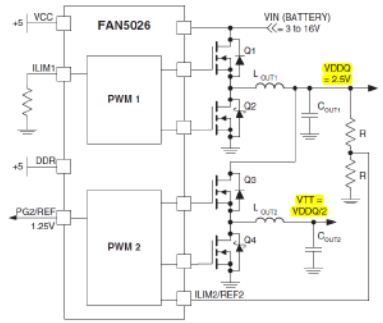


Figure 2. Typical Application

EX1041, pp.1-2, 9; *see also id.*, pp.7-8 (similar).

As another example, Texas Instruments offered a TPS51020 "***Dual***" buck converter, e.g., for V_{DDQ} and V_{TT} voltages for DDR or DDR2 memory devices (similar to Ground 1C where "*first*"=V_{DDQ} and "*third*"= V_{TT}):

TEXAS INSTRUMENTS

TPS51020

SLUS564B – JULY 2003 – REVISED DECEMBER 2003

DUAL, VOLTAGE MODE, DDR SELECTABLE, SYNCHRONOUS, STEP-DOWN CONTROLLER FOR NOTEBOOK SYSTEM POWER

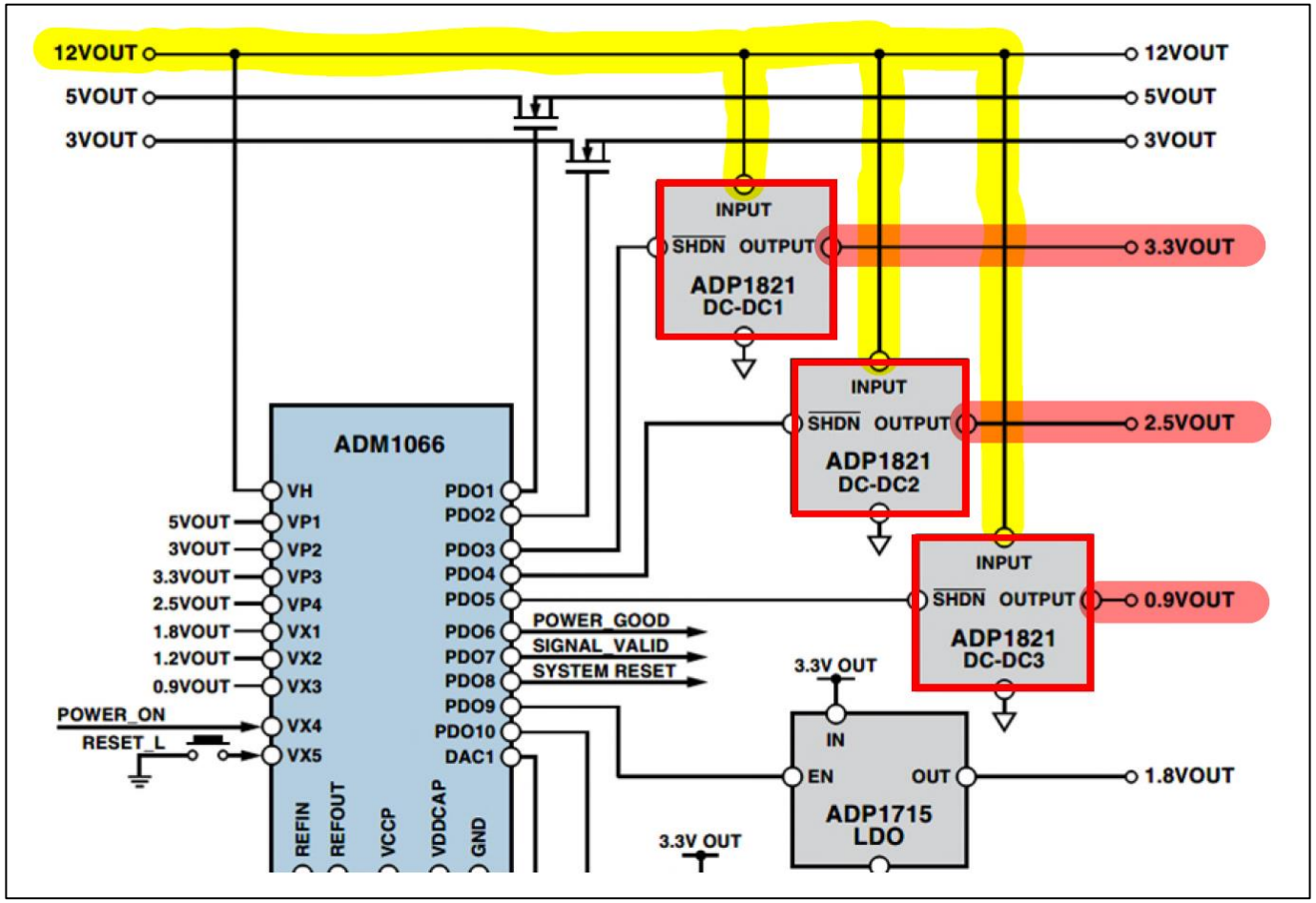
APPLICATIONS

- **Notebook Computers System Bus and I/O**
- **DDR I or DDR II Termination**

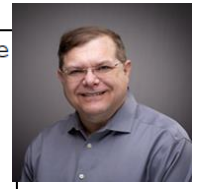
EX1040, pp.1, 11 ("TPS51020 gives a complete function set required for the DDR termination supply such as VDDQ/2 tracking V_{TT}").

'918: Pet. at 38-40
'054: Pet. at 38-40

1. Harris is not limited to one buck converter — it was common to use multiple buck converters for multiple outputs



EX1062, 15; see also EX1075, 134:22-141:23; EX1078, 1 (ADP1821 datasheet)



Q. Okay. And but it was well known at the time of the invention that you can have a single-voltage converter to generate two different voltage levels; correct?

MR. CHANDLER: Objection. Form.

THE WITNESS: It was possible under some circumstances, but certainly not the most common thing to do. Normally, if you need to generate multiple output voltages, you would use multiple regulators, especially in a high-current situation

EX2030/EX2060 (Wolfe) at 53:16-:25

'918: Paper 25 (Reply) at 10-13
'054: Paper 26 (Reply) at 11-14

1. Harris is not limited to one buck converter — and space is not disclosed as a problem in Harris or the 918/054 Patents

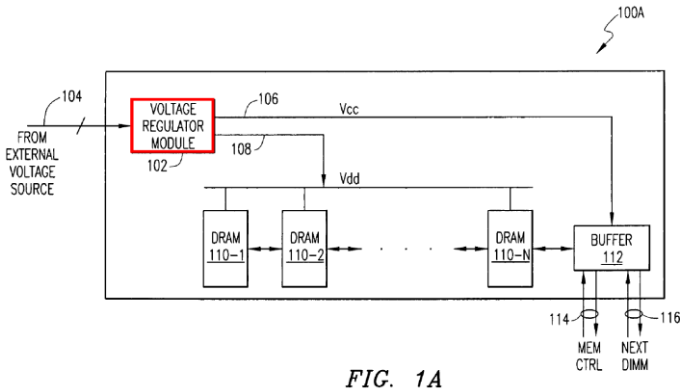
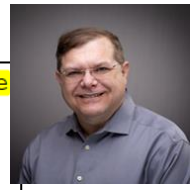


FIG. 1A

[0010] In accordance with the teachings of the present patent disclosure, at least one on-board voltage regulator module (VRM) is provided as part of the memory board assembly module **100**A for converting an externally supplied voltage level available on external source path **104** into appropriate local voltage levels that power the first and second voltage paths, i.e., the V_{dd} and V_{cc} paths **108**, **106**,

[0013] It is contemplated that local supply voltage conversion for double-rank DIMMs can be accommodated with a form factor design of approximately about one square inch (both sides of the printed circuit board), and at a component height compatible with applicable Joint Electron Device Engineering Council (JEDEC) standards.

EX1023 (Harris) at Fig. 1A, [0010], [0013]



Q. Okay. Certainly, the LDO design would take up less space; correct?

MR. CHANDLER: Objection --

THE WITNESS: Not necessarily.

(Clarification requested by Reporter.)

MR. CHANDLER: Object to form.

BY MS. ZHONG:

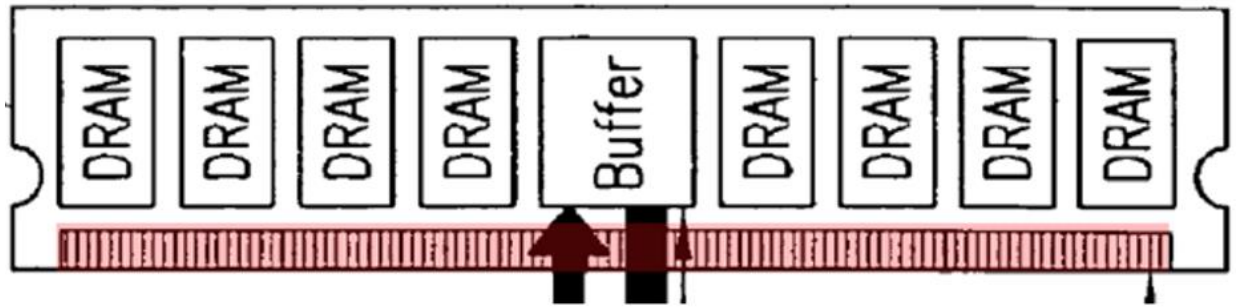
Q. Why not?

A. It depends on the external components, the packaging. You have to actually do the analysis. Both are viable solutions and, again, since buck converters, especially low current buck converters, are designed for some very small battery powered systems like cell phones, or even smaller things, they often can be extremely small.

EX2030/EX2060 (Wolfe) at 89-1:15

'918: Paper 25 (Reply) at 10-13
'054: Paper 26 (Reply) at 11-14

1. Harris is not limited to one buck converter — and chips can be stacked to save space



EX1023 (Harris) at Fig. 3

Q. And in what circumstances would you want to use a stacked/dual-die memory device?

A. Sorry. There's a fellow who was making the noise earlier outside my window.

When you wanted to increase the capacity of the memory system.

Q. And could you explain that a little more.

A. Sure. The physical space on a DIMM would require a certain amount of space, a rectangle or, typically, a square -- I guess it's rectangular -- for one of these integrated circuits. If they were stacked, you've now doubled the amount of memory stored in the same amount of physical space -- two-dimensional physical space. It certainly has a little additional height.

EX1075 (Mangione-Smith) at EX1075, 74:22-75:25, 77:10-:17

'918: Paper 25 (Reply) at 10-13, 19-20
'054: Paper 26 (Reply) at 11-14, 20-21

2. The Institution Decision correctly found it obvious to use different buck converters for different voltages (e.g., V_{DD} vs. V_{DDL})

	Voltage Mappings (Grounds 1-3)		
	A	B	C
"*first*":	V_{DD} or V_{DDQ} = 1.8V	V_{DD}, V_{DDQ}, or V_{DDL} = 1.8V	V_{DD}, V_{DDQ}, or V_{DDL} = 1.8V
"*second*":	V_{CC} or V_{CCFBD} = 1.5V	V_{CC}=1.5V	V_{CC} or V_{CCFBD} = 1.5V
"*third*":	V_{DDL}=1.8V	V_{CCFBD}=1.5V	V_{TT}=0.9V
"*fourth*":	V_{DDSPD}=3.3V	V_{DDSPD}=3.3V	V_{DDSPD}=3.3V

'918: Paper 1 (Pet.) at 27

	Voltage Mappings (Grounds 1-3)		
	A	B	C
"*first*":	V_{DD} or V_{DDQ} = 1.8V	V_{DD} or V_{DDQ} = 1.8V	V_{DD} or V_{DDQ} = 1.8V
"*second*":	V_{CC} or V_{CCFBD} = 1.5V	V_{CC}=1.5V	V_{CC} or V_{CCFBD} = 1.5V
"*third*":	V_{DDL}=1.8V	V_{CCFBD}=1.5V	V_{TT}=0.9V

'054: Paper (Pet.) at 27

Patent Owner further contends that Petitioner has not made out a case to use two or more buck converters to provide voltages having the same level. Prelim. Resp. 25-29. Petitioner explained sufficiently, however, that the FBDIMM Standards identify V_{DD}, V_{DDQ} and V_{DDL} as well as V_{CC} and V_{CCFBD} as separate voltages of the same level with separate pins that can be turned on and off independently of one another. Pet. 30-31. Petitioner contends this provides independence for the power supplies with improved stability and flexibility for power management. *Id.* at 31. Petitioner also relies on voltage mapping C (Pet. 27) which has different voltage levels for the four voltages used, so Patent Owner's argument, even if correct, would not negate Petitioner's showing with respect to this voltage mapping.

'918: ID at 23
See also '054: ID at 20-23

2. JEDEC teaches multiple converters for V_{DD}, V_{DDL}, and V_{DDQ}, even though they are all 1.8V, to permit independent control

2.3.1 Power-up and initialization sequence

The following sequence is required for POWER UP and Initialization.

a) Apply power and attempt to maintain CKE below 0.2*VDDQ and ODT*1 at a low state (all other inputs may be undefined.) The power voltage ramp time must be no greater than 20mS; and during the ramp, VDD>VDDL>VDDQ and VDD-VDDQ<0.3 volts.

- VDD, VDDL and VDDQ are driven from a single power converter output, AND
- VTT is limited to 0.95 V max, AND
- Vref tracks VDDQ/2.

or

- Apply VDD without any slope reversal before or at the same time as VDDL.
- Apply VDDL without any slope reversal before or at the same time as VDDQ.
- Apply VDDQ without any slope reversal before or at the same time as VTT & Vref.

at least one of these two sets of conditions must be met.

NOTE VDDL and VSSDL are power and ground for the DLL. It is recommended that they be isolated on the device from VDD, VDDQ, VSS, and VSSQ.

First option: "single power converter" for all three voltages

Second option: multiple converters to permit independent control

EX1026 at 9 (DDR2); *see also* EX1046 at 15 (same for DDR3)

EX1026 at 3

Q. When would you use multiple regulators to generate multiple 1.8 volts output?

A. It would be an ordinary design decision. One might do it when they want to ***sequence the power***, one might want to do it when they ***turn the power on and off independently***, or one may do it simply because it's ***more cost effective*** to use multiple small regulators than one large regulator. It's a design choice.

EX2030/EX2060 (Wolfe) at 39:2-:10

'918: Paper 1 (Pet.) at 30-31; Paper 25 (Reply) at 13-15
'054: Paper 1 (Pet.) at 29-30; Paper 26 (Reply) at 14-16

2. There are known advantages to using multiple buck converters, even if they all output 1.8V

Netlist argues that using a ***single*** converter (as shown in blue above) was more common, POR 21-27, but the Petition explained the motivation for ***multiple*** converters (e.g., red above), including because the JEDEC standards treat those voltages separately, thus permitting power-on sequencing; providing independent control; improving efficiency; and saving power. Pet. 30-31; EX2030, 39:2-:10, 44:25-46:10; EX1075, 134:22-136:2, 194:23-195:7; EX1062, 13-15 ("sequence"/"sequencing"); EX2012, 73 ("sequencing"). The example Netlist provides with a "***single*** power source" is ***not*** for an FBDIMM like Harris. POR 23 (citing EX2006, 4 ("SODIMM")); EX1075, 102:17-103:9 (SODIMM is unbuffered as shown in EX2045 and EX2046, 4.20.11-23).

918: Paper 25 (Reply) at 14
054: Paper 26 (Reply) at 15

Power Sequencing Violations

DDR memories must be powered up in a specific manner. Any violation of the power up sequencing will result in undefined operations. Also, power down sequencing serves as a power saving tool when the DDR device needs to be shut down without all other devices connected to the same power supply. Violating these sequences will present poor power saving results.

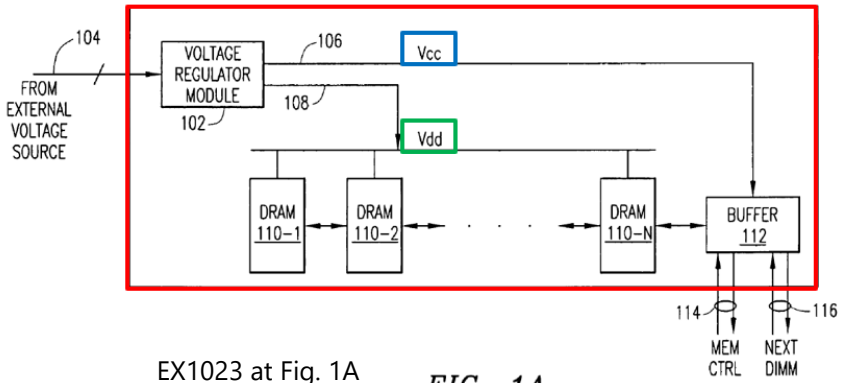
EX2012, 73

Many devices share standard voltage levels (such as 3.3 V), while others may require device-specific voltages. In addition, a particular standard voltage level may have to be independently furnished in numerous places. For example, separate analog- and digital supplies, such as 3.3 V_{ANALOG} and 3.3 $V_{DIGITAL}$, may be required. Generating the same voltage numerous times may be necessary to improve efficiency (e.g., memory rails running at hundreds of amperes) or to meet sequencing requirements (3.3 V_A and 3.3 V_B needed by separate devices at different times). All of these factors contribute to the proliferation of voltage sources.

EX1062, 13

'918: Paper 1 (Pet.) at 30-31; Paper 25 (Reply) at 13-15
'054: Paper 1 (Pet.) at 29-30; Paper 26 (Reply) at 14-16

3. The Institution Decision correctly found that Harris teaches generating all FBDIMM voltages on the module, including V_{TT}



EX1023 at Fig. 1A

FIG. 1A

Voltage Mappings (Grounds 1-3)			
	A	B	C
"*first*":	V_{DD} or V_{DDQ} = 1.8V	V_{DD}, V_{DDQ}, or V_{DDL} = 1.8V	V_{DD}, V_{DDQ}, or V_{DDL} = 1.8V
"*second*":	V_{CC} or V_{CCFBD} = 1.5V	V_{CC}=1.5V	V_{CC} or V_{CCFBD} = 1.5V
"*third*":	V_{DDL}=1.8V	V_{CCFBD}=1.5V	V_{TT}=0.9V
"*fourth*":	V_{DDSPD}=3.3V	V_{DDSPD}=3.3V	V_{DDSPD}=3.3V

Voltage Mappings (Grounds 1-3)			
	A	B	C
"*first*":	V_{DD} or V_{DDQ} = 1.8V	V_{DD} or V_{DDQ} = 1.8V	V_{DD} or V_{DDQ} = 1.8V
"*second*":	V_{CC} or V_{CCFBD} = 1.5V	V_{CC}=1.5V	V_{CC} or V_{CCFBD} = 1.5V
"*third*":	V_{DDL}=1.8V	V_{CCFBD}=1.5V	V_{TT}=0.9V

Harris's Figure 1A shows that the voltages **V_{cc}** and **V_{dd}** are generated on the **module**. On this record, we agree with Petitioner that it would logically follow to generate V_{TT} on the **module** using the same voltage regulator module 102 as used to generate voltages **V_{cc}** and **V_{dd}**. *See* Pet. 15-19. In addition, "when there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp." *KSR*, 550 U.S. at 421. Here, there are only two options – generate the voltage V_{TT} on the module, as Petitioner indicates, or obtain the voltage V_{TT} from interface pins. Petitioner's choice of the former of the two options does not negate its showing of obviousness.

'918: ID at 24
'054: ID at 23

3. Harris teaches generating all FBDIMM voltages on the module, which would include V_{TT}

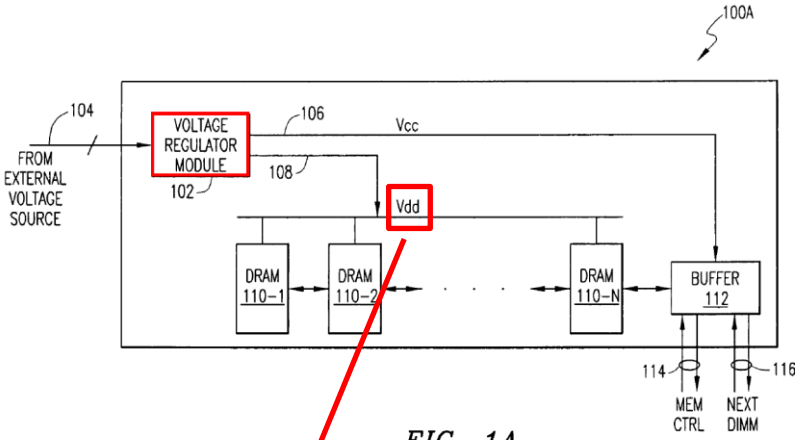
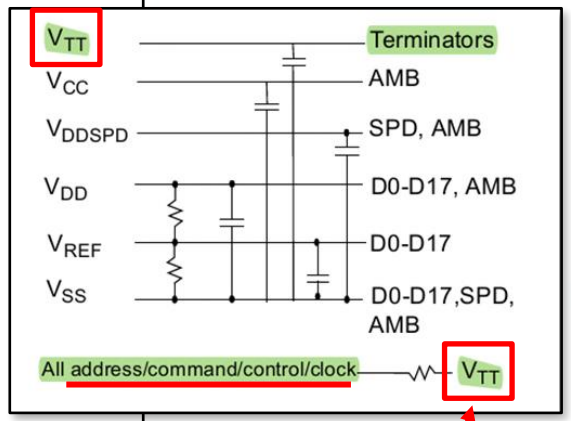


FIG. 1A

[0012] By way of example, a standard FBD module requires 28 V_{dd} pins (for DRAM devices) and 8 V_{cc} pins (for buffer and logic) and associated Ground returns, resulting in a total of 72 pins that provide a power supply interface for up to two x4 DRAM ranks (36 devices) and buffer logic. A voltage-independent FBD design incorporating the embodiment of **FIG. 1A** is capable of replacing these power supply interface pins with as few as six +12V pins (from an external voltage source), with local conversion to V_{dd} (to DRAM) and V_{cc} (to buffer/logic) being added.

EX1023 at [0012], Fig. 1A



EX1028 at 15, 68

Q. So you think that when Harris is referring to the VDD pins, it includes both what the FB-DIMM specification calls the VTT and VDD pins?
A. I think so because he says there's 28 of them . . . and the specification has 24 VDDs and 4 VTTs.

EX2030/EX2060 (Wolfe) at 103:24-104:6

DDR2 SDRAM Fully Buffered DIMM Design Specification — **Architecture**

Pin Name	Pin Description	Count
V_{DD}	DRAM Power and AMB DRAM I/O Power (1.8 Volt)	24
V_{TT}	DRAM Address/Command/Clock Termination Power ($V_{DD}/2$)	4

EX1028 at 11

'918: Paper 1 (Pet.) at 17-18; Paper 25 (Reply) at 15-17
'054: Paper 1 (Pet.) at 17-18; Paper 26 (Reply) at 16-19

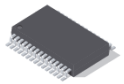
3. Dual buck converters for V_{TT} were common (to track V_{DDQ})

Q. Okay. Any reason for not generating VTT locally on the DIMM board?
A. I think if you read Harris and the FB-DIMM standard together, it's clear that it would be preferable to do it locally.
Q. Any reason for not doing it locally?
A. It would depend on particular circumstances. Because it has to track VDD in the standard, I think it would be preferable to do it locally.

EX2030/EX2060 (Wolfe) at 72:22-73:7 (objection omitted); *see also id.* 196:3-197:7

TEXAS INSTRUMENTS

TPS51020



SLUS564B – JULY 2003 – REVISED DECEMBER 2003

DUAL, VOLTAGE MODE, DDR SELECTABLE, SYNCHRONOUS, STEP-DOWN CONTROLLER FOR NOTEBOOK SYSTEM POWER

APPLICATIONS

- Notebook Computers System Bus and I/O
- DDR I or DDR II Termination

DUAL MODE AND DDR MODE

TPS51020 provides one-chip solution for system power supply, such as for 5 V, 3.3 V or 1.8 V, and a dual switcher DDR power supply. By simply selecting DDR signal and some external configuration change following the instructions below, TPS51020 gives a complete function set required for the DDR termination supply such as VDDQ/2 tracking V_{TT} source/sink capability and V_{TT} reference output.

EX1040 at 1, 11

FAIRCHILD SEMICONDUCTOR

October 2005

FAN5026
Dual DDR/Dual-Output PWM Controller

- Complete DDR Memory power solution
  - VTT Tracks VDDQ/2
  - VDDQ/2 Buffered Reference Output
- Supports DDR-II and HSTL

Applications

- DDR V_{DDQ} and V_{TT} voltage generation
- Desktop computer
- Graphics cards

The FAN5026 is a multi-mode, dual channel PWM controller intended for graphic chipset, SDRAM, DDR DRAM or other low output voltage power applications in PC's, VGA Cards and set top boxes. The IC integrates a control circuitry for two synchronous buck converters. The output voltage of each controller can be set in the range of 0.9V to 5.5V by an external resistor divider.

EX1041 at 1, 9

'918: Paper 1 (Pet.) at 17-18, 39; Paper 25 (Reply) at 15-17
'054: Paper 1 (Pet.) at 17-18, 39; Paper 26 (Reply) at 16-19

3. Dual buck converters for V_{TT} were common (to track V_{DDQ}) — and much more efficient than an LDO for converting 12V to 0.9V

Q. And what were some of the trade-offs that were known at the time between using a buck converter and an LDO linear regulator?

A. Well, in general, a buck converter might achieve what's referred to as higher efficiency, which is to say, all of these voltage regulators, voltage converters that we're talking about have some amount of electrical power that goes in, and a smaller amount of electrical power that's made available on the output. There's always entropy.· There's always loss.

So in general, the -- it's understood that something like a switch regulator will have better efficiency than LDOs generally. . . .

Q. Is there a way to calculate the rough efficiency of an LDO regulator if you know what the input voltage is and the output voltage is?

A. If you know what the input voltage and current is, and the output voltage and current, you can calculate the efficiency.

Q. So . . . if the input is 10 volts and one amp, and the output is 1 volt and one amp, what would be the rough efficiency?

A. Well, I'm generally reluctant to do even simple math on the spot, but I believe that would be a 10 percent efficiency.

EX1075 (Mangione-Smith) at 112:12-114:8

Q. And what was the efficiency of buck convertors at the time of the invention?

A. It varies from situation to situation. But typically, in the 80 to 98 percent range.

Q. And you did not provide any analysis on the cost of buck converters versus LDOs that can be used to generate the needed voltage rail; correct?

MR. CHANDLER: Object to form.

THE WITNESS: Not a specific comparison, other than to say that both are available at very low cost today and both would be feasible to provide SPD power, and that the trend over the years has been to move all computer power supplies to buck converters.

EX2030/EX2060 (Wolfe) at 57:17-20, 140:15-24

'918: Paper 1 (Pet.) at 17-18; Paper 25 (Reply) at 15-17
'054: Paper (Pet.) at 17-18; Paper 26 (Reply) at 16-19

3. Netlist's proposal to produce V_{TT} off the module would defeat Harris's claimed benefit (technology-independent voltage distribution)

[0012] By way of example, a standard FBD module requires 28 V_{dd} pins (for DRAM devices) and 8 V_{cc} pins (for buffer and logic) and associated Ground returns, resulting in a total of 72 pins that provide a power supply interface for up to two x4 DRAM ranks (36 devices) and buffer logic. A voltage-independent FBD design incorporating the embodiment of **FIG. 1A** is capable of replacing these power supply interface pins with as few as six +12V pins (from an external voltage source), with local conversion to V_{dd} (to DRAM) and V_{cc} (to buffer/logic) being added. Alternatively, using additional power supply pins would provide the capability to support even more devices. For instance, with 12 supply pins (at +12V), the embodiment of **FIG. 1A** can provide enough power to supply 4 ranks (i.e., 72 devices). Likewise, a memory assembly of 8 ranks (144 devices) may be powered with 24 pins at +12V.

EX1023 (Harris) at [0012], [0019]-[0020]

[0019] Based on the foregoing Detailed Description, it should be appreciated that an implementation of the embodiments described herein thus provides a technology-independent voltage distribution scheme for memory devices wherein system board power supply and associated voltage plane(s) are eliminated. Accordingly, power supply design's complexity as well as the cost of memory-specific power distribution are reduced. Cost savings may include, for example, elimination of system-board-specific power supply or regulator output, associated bypass capacitor arrangements, heavy etch or power planes. Also, under the technology-independent voltage distribution scheme disclosed herein, cost of memory power regulation scales with populated memory devices, rather than being pre-provisioned for maximum memory capacity as is typically the case in existing systems. Additionally, one or more of the following advantages may be realized in an exemplary voltage distribution embodiment: provision of tighter, lower inductance regulation which decreases voltage variability and increases timing margins; reduction in the pin count on DIMM connector to system board or memory riser card (whereby a smaller connector or wider pin spacing may be accommodated); improved signal integrity due to reduced crosstalk on the same size connector; and reservation of extra pins for implementing additional standard or proprietary functions.

[0020] Because voltage-independent embodiments disclosed herein can provide upgradeability and extensibility without changing system board power distribution, transitioning to newer DRAM technologies (e.g., at lower operating voltages) is more cost-effective as well as simpler to implement. Further, the embodiments are amenable to dual +12V power supply rail implementations so that industry-standard form factors can be advantageously accommodated.

DDR1: 2.5V
DDR2: 1.8V
DDR3: 1.5V

See EX1023 (Harris) at [0002], [0009]

'918: Paper 1 (Pet.) at 17-19; Paper 25 (Reply) at 5, 15-17
'054: Paper (Pet.) at 17-19; Paper 26 (Reply) at 6, 16-19

4. The Institution Decision correctly found that '918 Ground 1 renders obvious the use of a fourth converter for V_{DDSPD}

	Voltage Mappings (Grounds 1-3)		
	A	B	C
"*first*":	V_{DD} or V_{DDQ} = 1.8V	V_{DD}, V_{DDQ}, or V_{DDL} = 1.8V	V_{DD}, V_{DDQ}, or V_{DDL} = 1.8V
"*second*":	V_{CC} or V_{CCFBD} = 1.5V	V_{CC}=1.5V	V_{CC} or V_{CCFBD} = 1.5V
"*third*":	V_{DDL}=1.8V	V_{CCFBD}=1.5V	V_{TT}=0.9V
"*fourth*":	V_{DDSPD}=3.3V	V_{DDSPD}=3.3V	V_{DDSPD}=3.3V

'918: Pet. at 27

Patent Owner argues that Harris requires at most two or three buck converters to provide the voltages needed and thus, does not disclose the four claimed converters. Prelim. Resp. 20-25. Specifically, Patent Owner contends that Harris discloses a single converter generating two regulated voltages, so Harris does not disclose four converters as claimed. Prelim. Resp. 21-22. Petitioner showed sufficiently that the FBDIMM Standards mentioned in Harris call for at least four voltages, and that given Harris's teaching of a converter, it would have been obvious to one of ordinary skill in the art to use multiple converters, including well-known buck converters, to generate the four voltages needed. Pet. 26-31. . . .

Patent Owner contends that Petitioner did not make the case that a person of ordinary skill in the art would have used a third buck converter, as opposed to a linear regulator, to provide termination voltage VTT. Prelim. Resp. 29–33. Petitioner explained sufficiently that "buck converters" were well-known as a highly-efficient way to step down voltages without generating excess heat or requiring large cooling devices, providing further motivation to use buck converters. Pet. 29–30.

'918: ID at 22-24

4. Netlist does not argue that the claims require the fourth converter (e.g., for V_{DDSPD}) to be a buck converter

1. A memory module comprising:

a printed circuit board (BCB) having an interface configured to fit not a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;

a first buck converter configured to provide a first regulated voltage having a first voltage amplitude;

a second buck converter configured to provide a second regulated voltage having a second voltage amplitude;

a third buck converter configured to provide a third regulated voltage having a third voltage amplitude;

a converter circuit configured to provide a fourth regulated voltage having a fourth voltage amplitude; and

a plurality of components coupled to the PCB, each component of the plurality of components coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages, the plurality of components comprising:

a plurality of synchronous dynamic random access memory (SDRAM) devices coupled to the first regulated voltage, and

[1] at least one circuit coupled between a first portion of the plurality of edge connections and the plurality of SDRAM devices,

[2] the at least one circuit operable to (i) receive a first plurality of address and control signals via the first portion of the plurality of edge connections, and (ii) output a second plurality of address and control signals to the plurality of SDRAM devices,

[3] the at least one circuit coupled to both the second regulated voltage and the fourth regulated voltage,

[4] wherein a first one of the second and fourth voltage amplitudes is less than a second one of the second and fourth voltage amplitudes.

'918: Paper 1 (Pet.) at 16-18, 26-31 & n.2; Paper 21 (POR) 30 n.5; Paper 25 (Reply) at 18

4. Using a buck converter for V_{DDSPD} was obvious given the higher efficiency compared to an LDO for converting 12V to 3.3V

Further, "buck converters" were well-known as a ***highly-efficient*** way to step down voltages without generating excess heat or requiring large cooling devices, providing a further motivation (beyond Harris's express disclosure above) to implement Harris's voltage regulator using "*[buck] converter[s].*" EX1003, ¶237; EX1059, 5:23-30 ("***Switch mode buck converters*** have become popular due to two attractive features: first, they are ***more efficient*** than traditional low drop out regulators (LDO) (e.g., up to 95%) and second, ***they can provide relatively high currents with lower power dissipation on chip than an LDO can.***"); EX1058, p.5 (explaining the "***high efficiency*** of switching regulators"); *see also, e.g.*, EX1040, pp.1 ("high efficiency"), 23-24 (Figs.22-25); EX1041, pp. 1, 13 ("high efficiency"); EX1048, p.3; EX1062, p.11; EX1064, ¶[0101].

918: Pet. at 29-30

Q. Is there a way to calculate the rough efficiency of an LDO regulator if you know what the input voltage is and the output voltage is?

A. If you know what the input voltage and current is, and the output voltage and current, you can calculate the efficiency.

Q. So . . . if the input is 10 volts and one amp, and the output is 1 volt and one amp, what would be the rough efficiency?

A. Well, I'm generally reluctant to do even simple math on the spot, but I believe that would be a 10 percent efficiency.

EX1075 (Mangione-Smith) at 113:20-114:8

Q. And an LDO is selected over a buck converter, especially when the current is low; correct?

A. It can be either way, right. So, you know, a cell phone in sleep mode uses very, very low currents and yet would typically use a buck -- a buck converter because of the efficiency. It's a host of things that are taken into consideration, and there are many situations where either one is suitable, but there are different costs, there are different size constraints, there are different efficiency levels, and one makes -- uses one's engineering judgment to decide between two common alternatives.

EX2030/EX2060 (Wolfe) at 78:18-79:7 (objection omitted);
see also id. 76:4-:19, 79:24-80:11, 82:7-85:10, 88:4-:20, 89:1-:21, 138:14-:21, 140:15-:24

Paper 1 (Pet.) at 16-18, 29-30; Paper 25 (Reply) at 17-18

4. Netlist's proposal to produce V_{DDSPD} off the module would defeat Harris's claimed benefit (technology-independent voltage distribution)

[0012] By way of example, a standard FBD module requires 28 V_{dd} pins (for DRAM devices) and 8 V_{cc} pins (for buffer and logic) and associated Ground returns, resulting in a total of 72 pins that provide a power supply interface for up to two x4 DRAM ranks (36 devices) and buffer logic. A voltage-independent FBD design incorporating the embodiment of **FIG. 1A** is capable of replacing these power supply interface pins with as few as six +12V pins (from an external voltage source), with local conversion to V_{dd} (to DRAM) and V_{cc} (to buffer/logic) being added. Alternatively, using additional power supply pins would provide the capability to support even more devices. For instance, with 12 supply pins (at +12V), the embodiment of **FIG. 1A** can provide enough power to supply 4 ranks (i.e., 72 devices). Likewise, a memory assembly of 8 ranks (144 devices) may be powered with 24 pins at +12V.

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[0019] Based on the foregoing Detailed Description, it should be appreciated that an implementation of the embodiments described herein thus provides a technology-independent voltage distribution scheme for memory devices wherein system board power supply and associated voltage plane(s) are eliminated. Accordingly, power supply design's complexity as well as the cost of memory-specific power distribution are reduced. Cost savings may include, for example, elimination of system-board-specific power supply or regulator output, associated bypass capacitor arrangements, heavy etch or power planes. Also, under the technology-independent voltage distribution scheme disclosed herein, cost of memory power regulation scales with populated memory devices, rather than being pre-provisioned for maximum memory capacity as is typically the case in existing systems. Additionally, one or more of the following advantages may be realized in an exemplary voltage distribution embodiment: provision of tighter, lower inductance regulation which decreases voltage variability and increases timing margins; reduction in the pin count on DIMM connector to system board or memory riser card (whereby a smaller connector or wider pin spacing may be accommodated); improved signal integrity due to reduced crosstalk on the same size connector; and reservation of extra pins for implementing additional standard or proprietary functions.

[0020] Because voltage-independent embodiments disclosed herein can provide upgradeability and extensibility without changing system board power distribution, transitioning to newer DRAM technologies (e.g., at lower operating voltages) is more cost-effective as well as simpler to implement. Further, the embodiments are amenable to dual +12V power supply rail implementations so that industry-standard form factors can be advantageously accommodated.

'918: Paper 1 (Pet.) at 16-18; Paper 25 (Reply) at 5, 18

4. Netlist's proposal to produce V_{DDSPD} off the module would also defeat Ground 2's claimed benefit (battery backup)

Ground 2: Ground 1 and Battery Backup of Amidi

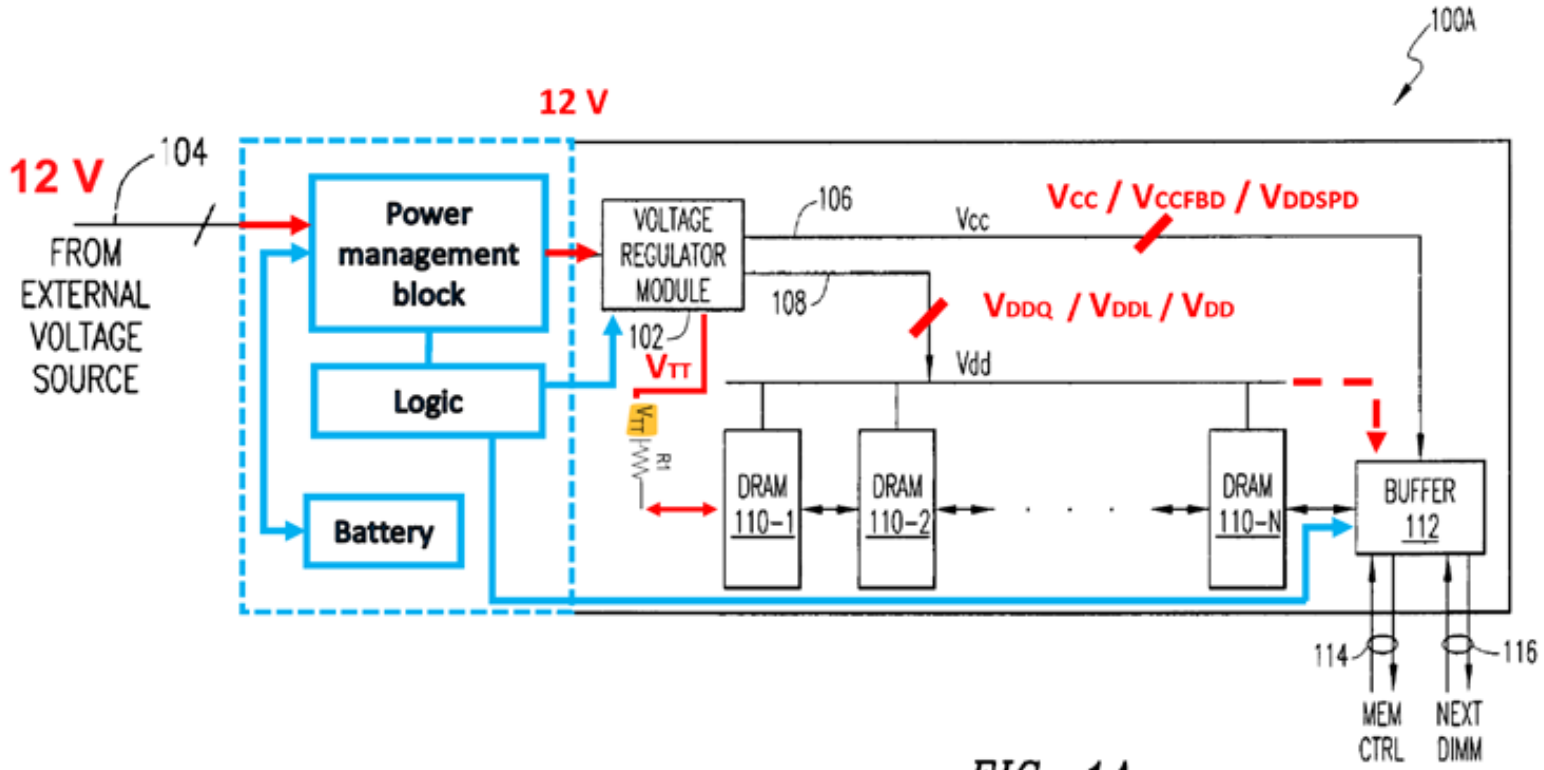
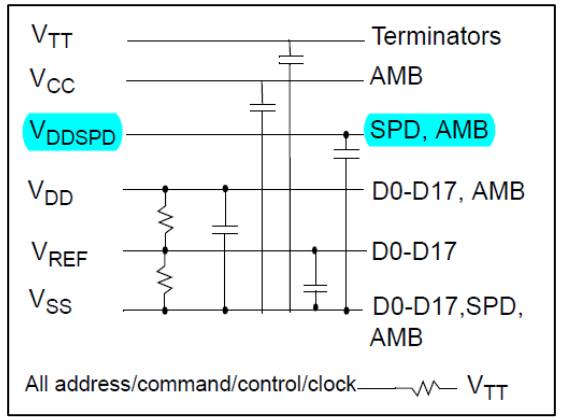


FIG. 1A



EX1028 at 15

'918: Paper 1 (Pet.) at 16-18 , 52-56; Paper 25 (Reply) at 18; EX1003, ¶¶284-86, 436-37, 442, 474

OBVIOUS TO COMBINE AMIDI'S BATTERY BACKUP WITH HARRIS

GROUND 2

(HARRIS + FBDIMM STANDARDS + AMIDI)

The Institution Decision correctly found a motivation to combine Amidi's battery backup with Harris for Ground 2

Ground 2: Ground 1 and Battery Backup of Amidi

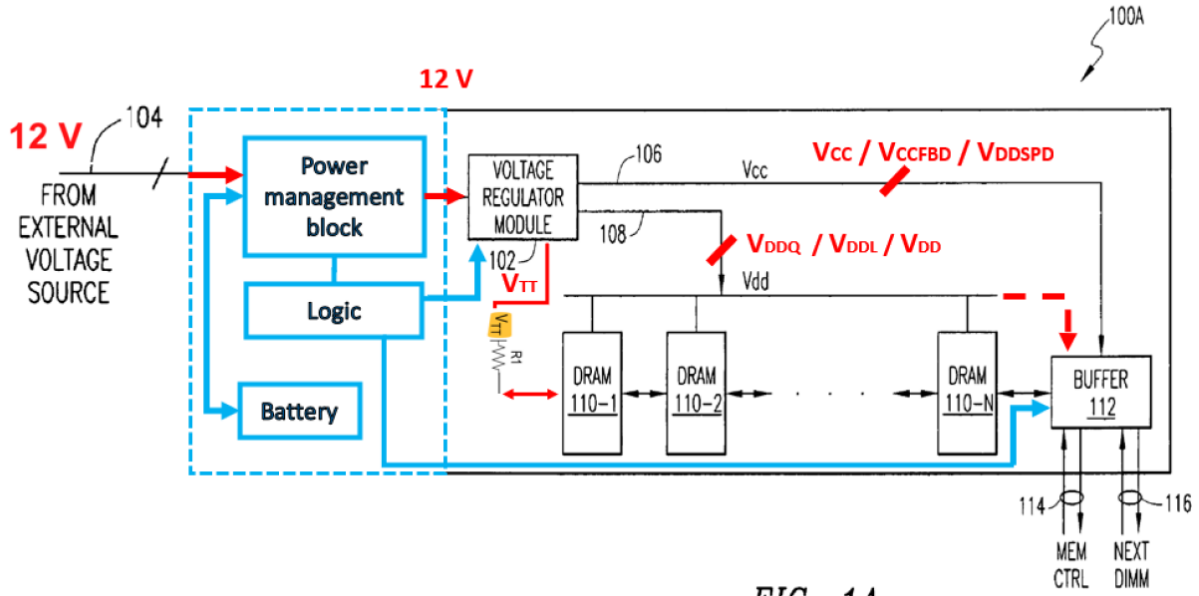
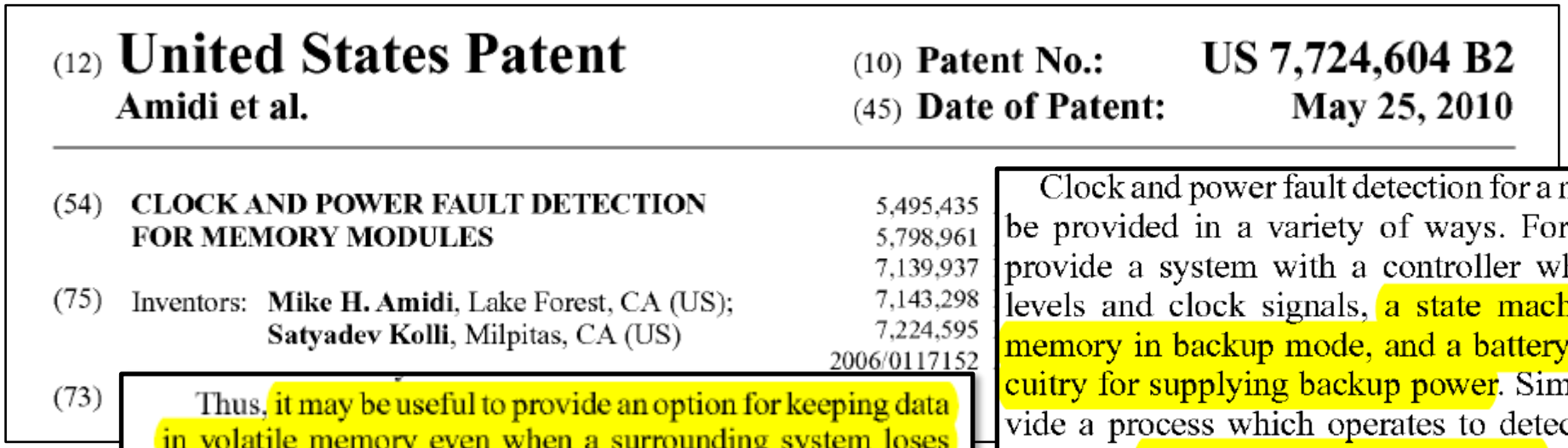


FIG. 1A

Patent Owner argues that Harris provides alternate voltage sources to power a memory module in the event of a power interruption, so Harris already provides a solution for the alleged problem that Amidi addresses. Prelim. Resp. 35-39. Harris does not appear to describe, however, switching to an alternate voltage source in response to power loss, nor does it explicitly mention a battery as an alternate voltage source, whereas Amidi does. Ex. 1024, code (57). Thus, Patent Owner's argument does not undermine Petitioner's motivation to combine the references.

'918: ID at 35-37
See also '054: ID at 30-33

Amidi provides battery backup power on the module, which is not disclosed by Harris



(12) **United States Patent**
Amidi et al.

(10) **Patent No.: US 7,724,604 B2**
(45) **Date of Patent: May 25, 2010**

(54) **CLOCK AND POWER FAULT DETECTION FOR MEMORY MODULES**

(75) Inventors: **Mike H. Amidi**, Lake Forest, CA (US); **Satyadev Kolli**, Milpitas, CA (US)

5,495,435
5,798,961
7,139,937
7,143,298
7,224,595
2006/0117152

(73)

Thus, it may be useful to provide an option for keeping data in volatile memory even when a surrounding system loses power. Moreover, it may also be useful to keep data in volatile memory when a surrounding system suffers some form of an error which causes a clock to malfunction even though power is still supplied. Likewise, it may be useful to provide volatile memory which has non-volatile characteristics in short- or medium-term time periods.

EX1024 at 1:28-35

Clock and power fault detection for a memory module may be provided in a variety of ways. For example, one may provide a system with a controller which detects voltage levels and clock signals, a state machine for operating a memory in backup mode, and a battery and supporting circuitry for supplying backup power. Similarly, one may provide a process which operates to detect voltage and clock signals, initiate backup operations, maintain memory (through refresh, for example), and detect a recovery status. Providing such a system or process within a memory module can be very helpful, as it avoids the need for system circuitry in a computer system or similar device which can maintain a memory module from outside the module. Moreover, such a system or process may be tuned to the specific memory module, instead of requiring overhead to deal with many different types of memory modules, for example.

EX1024 at 2:11-26

'918: Paper 1 (Pet.) at 52-56; Paper 25 (Reply) at 18-20
'054: Paper 1 (Pet.) at 41-45; Paper 26 (Reply) at 19-21

Netlist admits battery backup was a known option — thus obvious

May 2005 . . . . . 1st BBvault shipped (battery-backed cache module). In production w/ 3rd generation.

BBvault

EX2035 at 39

Q. So the side connection on the BBvault memory is for battery backup, while the edge connections along the bottom of the memory module are for power from the host system; correct?

A. Yes. The side connections are -- go to the battery backup and are used when the power coming in from the host system along the edge connectors is not used.

Q. And this was known by 2005; correct?

A. Yes.

EX1075 (Mangione-Smith) at 166:3-:12

"[J]ust because 'better alternatives' may exist in the prior art 'does not mean that an inferior combination is inapt for obviousness purposes.'"

Dome Pat. L.P. v. Lee, 799 F.3d 1372, 1381 (Fed. Cir. 2015)

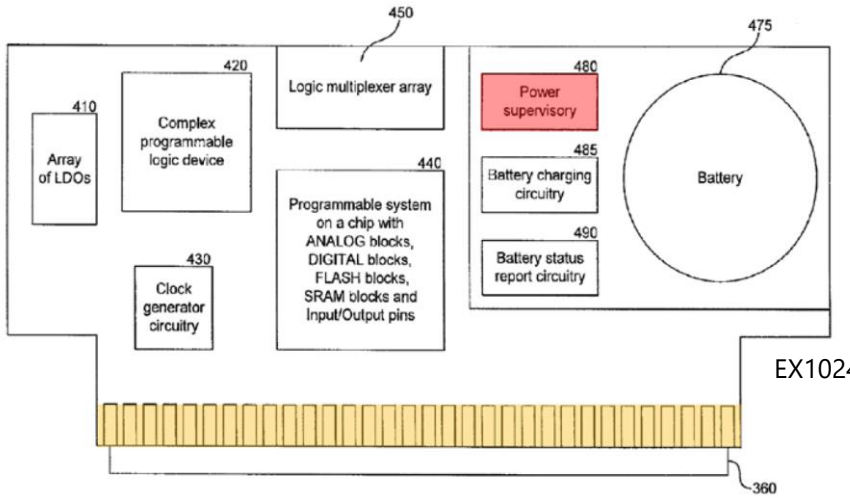
'918: Paper 1 (Pet.) at 52-56; Paper 25 (Reply) at 7, 18-20
'054: Paper 1 (Pet.) at 41-45; Paper 26 (Reply) at 7-8, 19-21

Space for battery backup on <u>one</u> side of the module does not prevent the combination of Ground 2

May 2005 . . . . . 1st BBvault shipped (battery-backed cache module). In production w/ 3rd generation.

BBvault

EX2035 at 39;
EX1075, 165:10-167:7



EX1024 (<u>Amidi</u>) at Fig. 4

22	Q. And as shown on the bottom of pages 4	
23	and 5 of Exhibit 1026, DDR2 SDRAM memory devices	
24	could also be stacked/dual-die x4 or x8 memory	
25	devices; is that correct?	11:05:34
1	A. At the bottom on page 4 it says	11:05:36
2	"Figure 4--stacked/dual-die DDR2 SDRAM x4," and	11:05:39
3	then on page 5 it says x8.	11:05:50
4	Q. Are you done or --	11:05:59
5	A. Yes, I am.	11:06:01
6	Q. What is stacked/dual-die?	11:06:03
7	A. Typically, that means that the dies are	11:06:08
8	stacked on top of each other physically.	11:06:12
9	Q. And in what circumstances would you	11:06:16
10	want to use a stacked/dual-die memory device?	11:06:18
11	A. Sorry. There's a fellow who was making	11:06:25
12	the noise earlier outside my window.	11:06:28
13	When you wanted to increase the	11:06:33
14	capacity of the memory system.	11:06:36
15	Q. And could you explain that a little	11:06:41
16	more.	11:06:42
17	A. Sure. The physical space on a DIMM	11:06:44
18	would require a certain amount of space, a	11:06:48
19	rectangle or, typically, a square -- I guess it's	11:06:53
20	rectangular -- for one of these integrated	11:06:58
21	circuits. If they were stacked, you've now	11:07:03
22	doubled the amount of memory stored in the same	11:07:09
23	amount of physical space -- two-dimensional	11:07:12
24	physical space. It certainly has a little	11:07:15
25	additional height.	11:07:17

EX1075 (Mangione-Smith) at 74:22-75:25

'918: Paper 1 (Pet.) at 52-56; Paper 25 (Reply) at 18-20
'054: Paper 1 (Pet.) at 41-45; Paper 26 (Reply) at 19-21

OVER-VOLTAGE PROTECTION
(‘918 CLAIMS 5-7, 9-13, 16-22, 24-27)
(‘054 CLAIMS 6-7, 9-12, 17)

GROUND 2 & 3

(HARRIS + FBDIMM STANDARDS + AMIDI + HAJECK)

The Institution Decision correctly found a "trigger" signal for over-voltage protection obvious in light of Grounds 2-3

National Semiconductor

LMC6953
PCI Local Bus Power Supervisor

DC Electrical Characteristics

Unless otherwise specified, all **boldface** limits guaranteed for T_J = 0°C to 70°C, V_{DD} = 5V, $R_{PULL-UP}$ = 4.7 kΩ and C_{EXT} = 0.01 µF. Typical numbers are room temperature (25°C) performance.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{H5}	V_{DD} Over-Voltage Threshold	(Note 4)	**5.45**	5.6	**5.75**	V
V_{L5}	V_{DD} Under-Voltage Threshold	(Note 4)	**4.25**	4.4	**4.55**	V
$V_{H3.3}$	3.3V Over-Voltage Threshold	(Note 5)	**3.8**	3.95	**4.1**	V
$V_{L3.3}$	3.3V Under-Voltage Threshold	(Note 5)	**2.5**	2.65	**2.8**	V

EX1063, pp.1-2; *see also* EX1061, p.15 (Analog Device circuit for "undervoltage" and "overvoltage" detection); EX1062, p.15 (same); EX1065, Abstract, ¶¶[0014, 18-19], Figs.1, 5 (similar).

'918: Pet. at 63
'054: Pet. at 54 (similar)

Claims 5-7, 9-13, 16-22 and 24-27 recite, or depend from a claim that recites, that the voltage monitor circuit generates the trigger signal in response to the input voltage being greater than a predetermined threshold voltage. Ex. 1001, 38:61-67, 40:7-13, 41:22-27, 42:21-26. Claims 5-7, 9-13, 16, 17, 20-22, and 24 require generation of a trigger signal, and we determine that Petitioner sufficiently shows for institution that these claims would have been obvious over the combination of Harris, the FBDIMM Standards, and Amidi.

'918: ID at 38
See also '054: ID at 35 (similar)

Over-voltage protection is needed to avoid damage and data loss

Other types of power signal anomalies, such as power surges and spikes, can additionally cause permanent damage to the circuitry of the storage subsystem.

EX1038 (Hajeck) at 1:28-:31

Absolute Maximum Ratings

Absolute maximum ratings are the values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Parameter	Min.	Typ.	Max.	Units
VCC Supply Voltage			6.5	V
VIN			18	V

Recommended Operating Conditions

Parameter	Conditions	Min.	Typ.	Max.	Units
Supply Voltage VCC		4.75	5	5.25	V
Supply Voltage VIN				16	V

EX1041 at 4

'918: Paper 1 (Pet.) at 12-13, 60-66, 75-77; Paper 25 (Reply) at 20-22
'054: Paper 1 (Pet.) at 12-13, 41-45, 53-54, 70-72; Paper 26 (Reply) at 21-23

Both over- and under-voltage protection was obvious, and common

National Semiconductor

LMC6953
PCI Local Bus Power Supervisor

DC Electrical Characteristics

Unless otherwise specified, all **boldface** limits guaranteed for T_J = 0°C to 70°C, V_{DD} = 5V, $R_{PULL-UP}$ = 4.7 kΩ and C_{EXT} = 0.01 µF. Typical numbers are room temperature (25°C) performance.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{H5}	V_{DD} Over-Voltage Threshold	(Note 4)	**5.45**	5.6	**5.75**	V
V_{L5}	V_{DD} Under-Voltage Threshold	(Note 4)	**4.25**	4.4	**4.55**	V
$V_{H3.3}$	3.3V Over-Voltage Threshold	(Note 5)	**3.8**	3.95	**4.1**	V
$V_{L3.3}$	3.3V Under-Voltage Threshold	(Note 5)	**2.5**	2.65	**2.8**	V

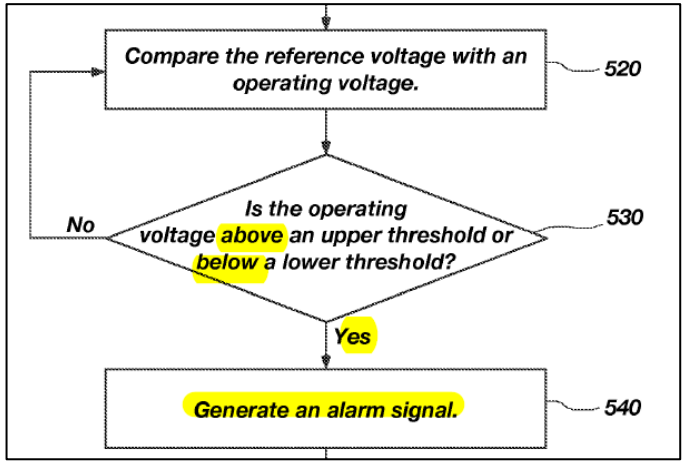
EX1063, pp.1-2; *see also* EX1061, p.15 (Analog Device circuit for "undervoltage" and "overvoltage" detection); EX1062, p.15 (same); EX1065, Abstract, ¶¶[0014, 18-19], Figs.1, 5 (similar).

'918: Pet. at 63
'054: Pet. at 54 (similar)

PROGRAMMING THE SUPPLY FAULT DETECTORS

The ADM1066 has up to 10 supply fault detectors (SFDs) on its 10 input channels. These highly programmable reset generators enable the supervision of up to 10 supply voltages. The supplies can be as low as 0.573 V and as high as 14.4 V. The inputs can be configured to detect an undervoltage fault (the input voltage drops below a preprogrammed value), an overvoltage fault (the input voltage rises above a preprogrammed value), or an out-of-window fault (undervoltage or overvoltage). The thresholds can be programmed to an 8-bit resolution in registers provided in the ADM1066. This translates to a voltage resolution that is dependent on the range selected.

EX1061 at 15



EX1065, Fig. 5

'918: Paper 1 (Pet.) at 12-13, 60-66. 75-77; Paper 25 (Reply) at 20-22
'054: Paper 1 (Pet.) at 12-13, 41-45, 53-54, 70-72; Paper 26 (Reply) at 21-23

Both over- and under-voltage protection was obvious, and common

Harris

[0013] It is contemplated that local supply voltage conversion for double-rank DIMMs can be accommodated with a form factor design of approximately about one square inch (both sides of the printed circuit board), and at a component height compatible with applicable Joint Electron Device Engineering Council (JEDEC) standards. Further, since the +12V power supply is not used directly by DRAM devices or buffer/logic components of the memory assembly, a wide tolerance (e.g., around +/−15%) can be accommodated, allowing low cost power distribution for system boards (such as, e.g., motherboards, cell boards, et cetera) wherein design requirements for bypass/hold-up capacitors may be relaxed or minimized. By way of an additional variation in implementation, the form factor associated with the memory assembly module **100**A may be suitably modified (e.g., removing the board's connector keyway) so as to ensure that a memory assembly module embodying the teachings of the present disclosure is not interchangeable with the standard DIMM, thereby preventing any accidental damage.

EX1023 (Harris) at [0013]

Amidi

A system, method and apparatus is provided for a clock and power fault detection for a memory module. The specific embodiments described in this document represent examples or embodiments of the present invention, and are illustrative in nature rather than restrictive.

Clock and power fault detection for a memory module may be provided in a variety of ways. For example, one may provide a system with a controller which detects voltage levels and clock signals, a state machine for operating a memory in backup mode, and a battery and supporting circuitry for supplying backup power. Similarly, one may provide a process which operates to detect voltage and clock signals, initiate backup operations, maintain memory (through refresh, for example), and detect a recovery status.

EX1024 (Amidi) at 2:6-19

Hajeck

The voltage detection circuit **48** is responsible for detecting anomalies in the power signal V_{IN} supplied by the host on line **36**, and for driving the ready/busy signal to the "busy" state when such anomalies are detected. A conventional voltage detection circuit may be used. The voltage detection circuit **48** may be designed to generate a "busy" signal whenever V_{IN} falls below a certain level, such as 2.6 or 2.7 volts. The voltage detection circuit may also be designed to generate a busy signal when the voltage exceeds a certain level, and/or when other types of anomalies are detected. To inhibit rapid transitions between the "ready" and "busy" states, the voltage detection circuit may be designed to provide a degree of hysteresis, and/or to hold its output for a particular time period after a state transition.

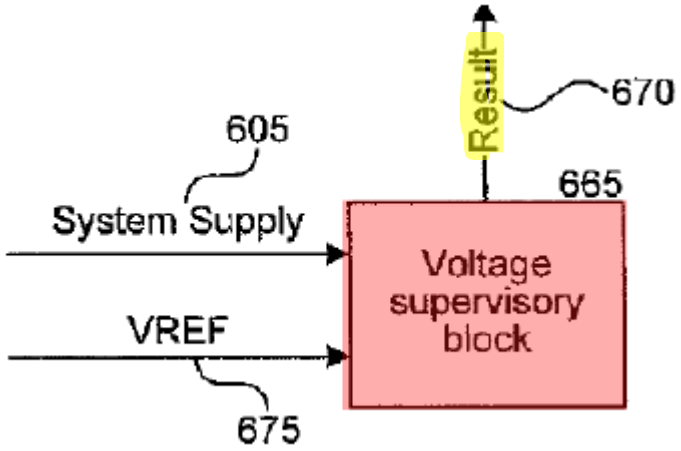
EX1038 (Hajeck) at 3:30-40

"Where a prior art patent discloses a ***range of values***, showing a claimed value falls within that range meets a party's burden of establishing the narrower claim would have been obvious where there is no reason to think the result would be unpredictable."

Gen. Hosp. Corp. v. Sienna Biopharms., Inc., 888 F.3d 1368, 1373 (Fed. Cir. 2018); *see also, e.g.*, *Iron Grip Barbell Co. v. USA Sports, Inc.*, 392 F.3d 1317, 1320-23 (Fed. Cir. 2004) (claim to three grips obvious in light of prior art teaching one, two, and four grips)

'918: Paper 1 (Pet.) at 12-13, 60-66. 75-77; Paper 25 (Reply) at 20-22
'054: Paper 1 (Pet.) at 12-13, 41-45, 53-54, 70-72; Paper 26 (Reply) at 21-23

Amidi in Ground 2 specifically discloses a trigger ("Result") signal for power disruptions



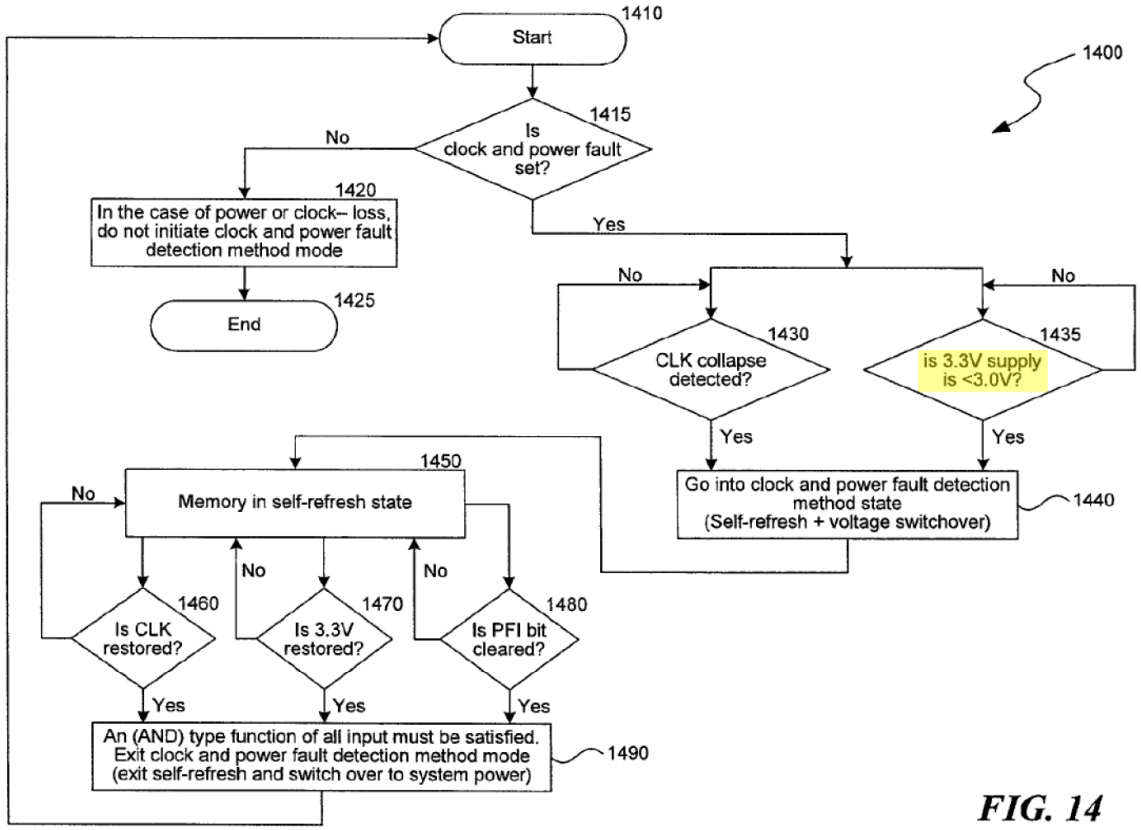


FIG. 14

EX1024 (Amidi) at Figs. 6, 14, 4:44-52, 5:25-43, 8:23-29, 9:8-12

'918: Paper 1 (Pet.) at 12-13, 60-66. 75-77; Paper 25 (Reply) at 20-22
'054: Paper 1 (Pet.) at 12-13, 41-45, 53-54, 70-72; Paper 26 (Reply) at 21-23

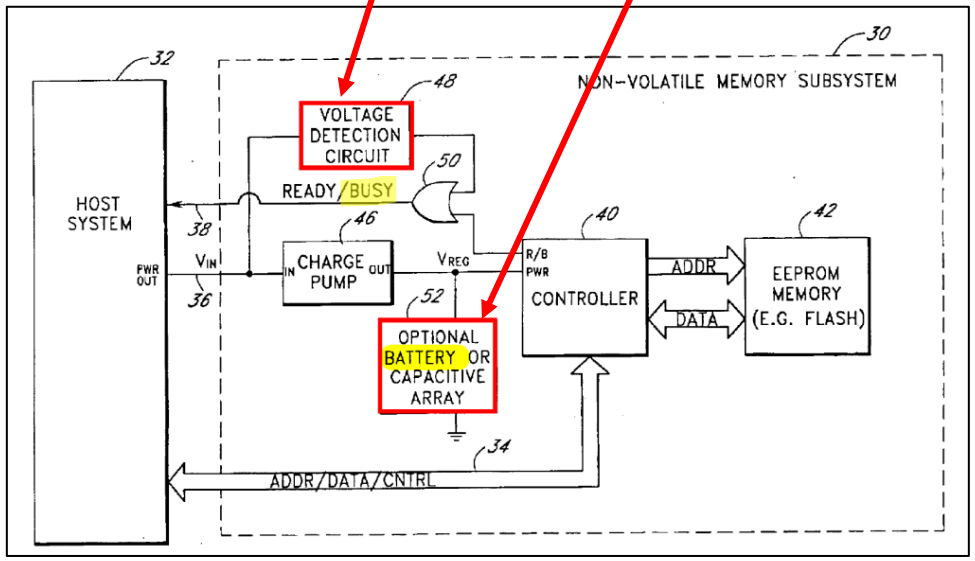
Hajeck in Ground 3 specifically discloses a trigger ("busy") signal for over-voltage protection

Other types of power signal anomalies, such as power surges and spikes, can additionally cause permanent damage to the circuitry of the storage subsystem.

The storage subsystem in the preferred embodiment also includes a voltage detection circuit that monitors the power signal from the host system to detect anomalies. The voltage detection circuit responds to detection of a power signal anomaly by asserting a busy signal to block the host system from performing write operations to the storage subsystem. By asserting the busy signal, the voltage detection circuit substantially ensures that backup power provided by the charge pump (and by the battery and/or capacitive array, if provided) will be sufficient for the controller to complete all outstanding operations. The likelihood that data will be lost as the result of the power signal anomaly is therefore significantly reduced.

The voltage detection circuit **48** is responsible for detecting anomalies in the power signal V_{IN} supplied by the host on line **36**, and for driving the ready/busy signal to the "busy" state when such anomalies are detected. A conventional voltage detection circuit may be used. The voltage detection circuit **48** may be designed to generate a "busy" signal whenever V_{IN} falls below a certain level, such as 2.6 or 2.7 volts. The voltage detection circuit may also be designed to generate a busy signal when the voltage exceeds a certain level, and/or when other types of anomalies are detected. To inhibit rapid transitions between the "ready" and "busy" states, the voltage detection circuit may be designed to provide a degree of hysteresis, and/or to hold its output for a particular time period after a state transition.

EX1038 (Hajeck) at 1:28-:31, 1:62-2:7, 3:30-40 & Fig. 1



EX1038 (Hajeck) at Fig. 1

Q. And the power anomalies that Hajeck's voltage detection circuit 48 can detect include both when the voltage V-in falls below a certain level, such as 2.6 or 2.7 volts, and also when the voltage exceeds a certain level; correct?

A. Yes, I see that.

Q. It says -- it would be fair to say that it was known at the time that detection circuits could detect both of those cases when the voltage drops too low or spikes too high?

A. Yes.

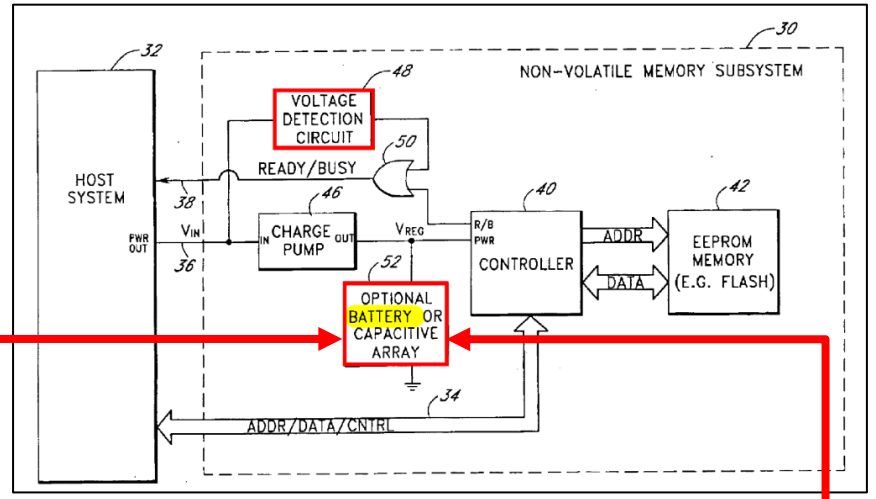
EX1075 (Mangione-Smith) at 196:16-197:1

'918: Paper 1 (Pet.) at 12-13, 60-66. 75-77; Paper 25 (Reply) at 20-22
'054: Paper 1 (Pet.) at 12-13, 41-45, 53-54, 70-72; Paper 26 (Reply) at 21-23

Hajeck in Ground 3 specifically discloses a trigger ("busy") signal for over-voltage protection

By asserting the busy signal, the voltage detection circuit substantially ensures that backup power provided by the charge pump (and by the battery and/or capacitive array, if provided) will be sufficient for the controller to complete all outstanding operations. The likelihood that data will be lost as the result of the power signal anomaly is therefore significantly reduced.

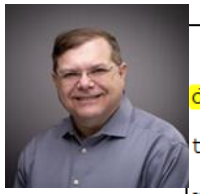
EX1038 (Hajeck) at 2:1-7 & Fig. 1



Q. So in the overvoltage situation, how does the charge pump operate differently?

A. The charge pump gets the power signal from the host, so if the power signal from the host is cut off because an anomaly was detected and reported to the host through ready-busy, then the charge pump begins to shut down.

EX2030/EX2060 (Wolfe) at 251:10-16



Q. So in Hajeck's case, before and after the detection of an input undervoltage or overvoltage, there is no switching of the power supplies; is that right?

A. Did you say before or after?

Q. Before and after, yes.

A. Well, after there is an indication that there's a shutdown, so that would certainly indicate to me that everything is being shut down, the entire computer.

Also, Hajeck contemplates that some of the anomalies may be a loss of power, in which case the power supplies are maintained for a minimum period, but then they're shut down.

Q. Okay. But during that period it's -- the power is supplied by the charge pump as before detection of the anomaly; is that right?

A. Well, there are two embodiments. There is one where it is supplied by the charge pump and there is another one in which a battery takes over to provide additional time for shutdown.

EX2030/EX2060 (Wolfe) at 230:17-232:6;
see also id. at 226:16-:2, 251:16-254:2

'918: Paper 1 (Pet.) at 12-13, 60-66. 75-77; Paper 25 (Reply) at 20-22
'054: Paper 1 (Pet.) at 12-13, 41-45, 53-54, 70-72; Paper 26 (Reply) at 21-23

WRITE OPERATIONS ('918 CLAIMS 11-12, 18-19, 25-26)

GROUNDS 2-3

(HARRIS + FBDIMM STANDARDS + AMIDI + HAJECK)

Grounds 2-3 use the battery-powered "logic" in Amidi to switch to S3 sleep mode in the event of a power disruption

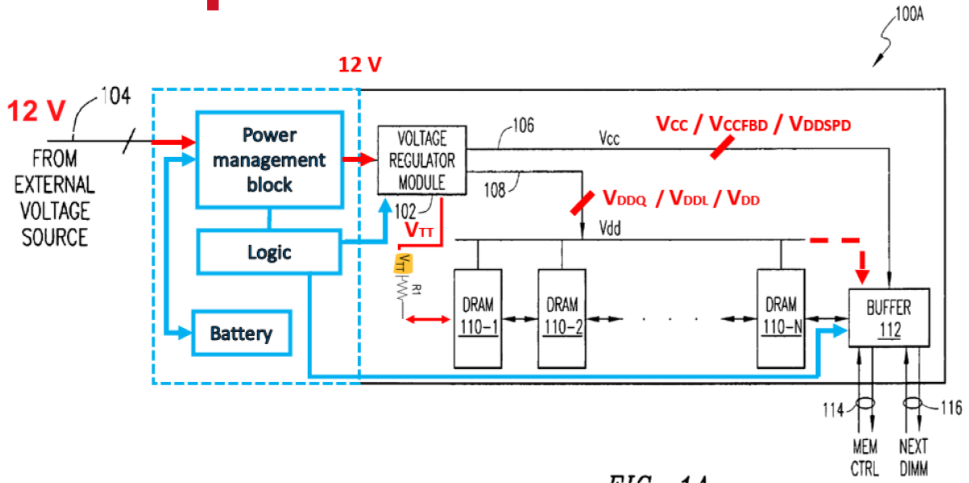


FIG. 1A

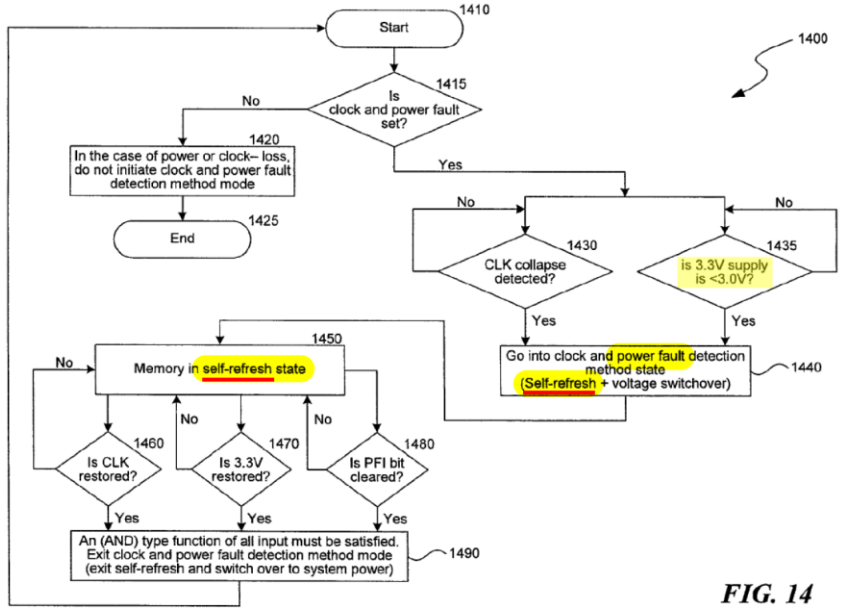


FIG. 14

Furthermore, Amidi's battery backup mode is similar to the S3 power-saving mode of Harris's FBDIMM memory module discussed above (pp.45-46), providing another motivation to combine Ground 1 with Amidi. Both modes put the SDRAMs in a self-refresh state to preserve data while conserving power. *Compare* pp.45-46, *with* EX1024, Fig.11, 2:16-19 ("Similarly, one may provide a process which operates to … maintain memory (through refresh, for example)"). Thus, a POSITA would have been motivated to use the teachings of S3 mode in Ground 1 when implementing Amidi's backup power supply and logic functionality. EX1003, ¶173. Indeed, the S3 mode was described in the FBDIMM Standards for the very purpose of saving power in all types of computers, including servers and workstations. EX1027, p.39 ("very lower power state"); EX1028, p.9 ("FB-DIMMs are intended for use as main memory when installed in systems such as servers and workstations.").

'918: Paper 1 (Pet.) at 54

'918: Paper 1 (Pet.) at 12-13, 52-56, 60-66, 75-77; Paper 25 (Reply) at 20-23

S3 sleep mode writes to non-volatile memory to avoid data loss

3.7.3 S3 Recovery Configuration Registers

The following CSRs should be stored in non-volatile memory before entering S3 mode and restored before normal DRAM transactions begin.

- DRC
- MTR
- DSREFTC
- DAREFTC
- S3RESTORE[15:0]
- SPDPAR[15:0] - SPD Personality Bytes

NOTE: Refer to "Advanced Configuration and Power Interface Specification Version 2.0c" as published by www.acpi.info for S3 mode definition.

EX1027 at 25

4.1.3 S3 current Specification

S3 is an ACPI mode in which the DIMMs are put into a very lower power state, with the DRAMs in self refresh mode. This AMB S3 current specification is required for the sizing of the power supply used for the S3 mode.

In this mode is defined as:
DRAMs in self refresh.
AMB maintaining the DRAMs in self refresh by driving the CKE signals low.
REFCLK not toggling.
VDD = VDDmax (1.9V).
VCC = 0V
VTT = 0V

			533 MHz		667 MHz		800 MHz		
Symbol	Conditions	Power Supply	Nominal	Max Current	Nominal	Max Current	Nominal	Max Current	Units
Idd_S3	**S3 current** VDD = 1.9V VCC = 0V VTT = 0V Across process variations Across the operating TCASE temperature range. DIMM types: Raw Card A, B, C, D, E, H, J, and future raw card type as adopted by FB-DIMM.	VDD (1.8V)		75		75		75	mA

Note that the total DIMM current will include the AMB IDD_S3 value as well as the self refresh current of all of the DRAMs on the DIMM.

EX1027 at 39; *see also id.* at 21

Paper 1 (Pet.) at 12-13, 60-66, 75-77; Paper 25 (Reply) at 20-23

Grounds 2-3 include over-voltage protection (with S3 sleep mode) to avoid damage and data loss (as discussed in prior section)

Other types of power signal anomalies, such as power surges and spikes, can additionally cause permanent damage to the circuitry of the storage subsystem.

EX1038 (Hajeck) at 1:28-:31

Absolute Maximum Ratings

Absolute maximum ratings are the values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Parameter	Min.	Typ.	Max.	Units
VCC Supply Voltage			6.5	V
VIN			18	V

Recommended Operating Conditions

Parameter	Conditions	Min.	Typ.	Max.	Units
Supply Voltage VCC		4.75	5	5.25	V
Supply Voltage VIN				16	V

EX1041 at 4

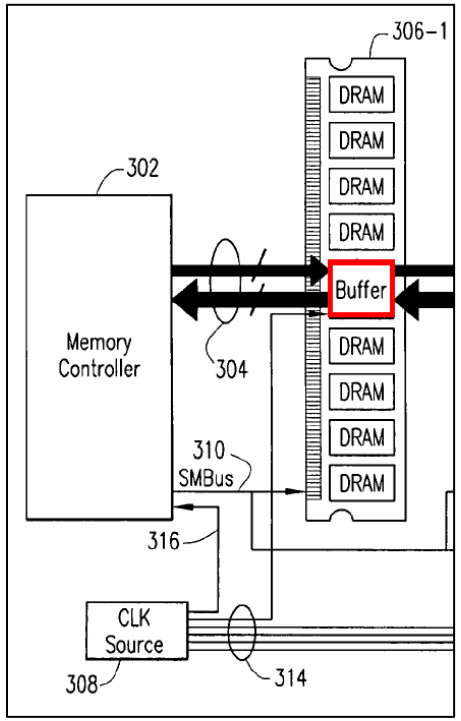
'918: Paper 1 (Pet.) at 12-13, 60-66, 68-69, 75-77; Paper 25 (Reply) at 20-23

NON-VOLATILE MEMORY ('918 CLAIMS 10-11, 15, 22)

GROUNDS 1-2

(HARRIS + FBDIMM STANDARDS + AMIDI)

The Institution Decision correctly found that Grounds 1-2 teach "non-volatile memory" in either the AMB Buffer or SPD



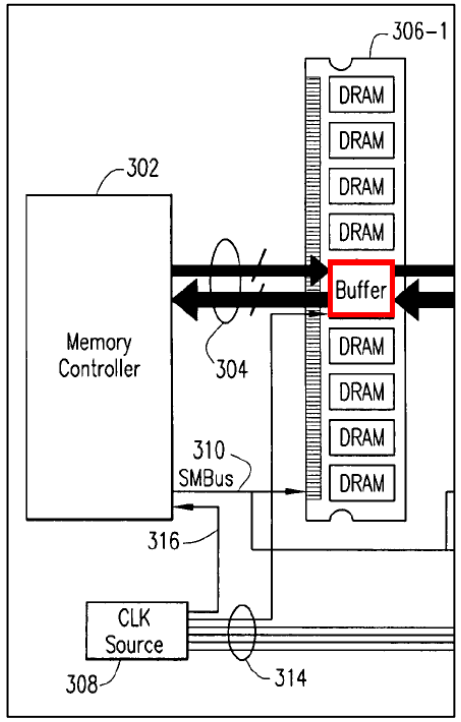
EX1023 (Harris) Fig. 3

Petitioner contends that the combination of Harris and the FBDIMM Standards discloses claim 15. Pet. 47–50. Specifically, Petitioner contends logic in Harris's buffer includes an integrated circuit, as does its serial presence detect (SPD), including non-volatile memory. Pet. 47 (citing Ex. 1027, 25; Ex. 1003 ¶¶ 435–437, 468–476). Petitioner further contends the logic element includes discrete elements such as resistors and capacitors to terminate voltages for Harris's buffer. Id. Petitioner asserts that the S3 sleep mode of the FBDIMM Standards requires S3 Recovery Configuration Registers. Id. According to Petitioner, an FBDIMM like Harris's memory module will store configuration information in non-volatile memory before entering into S3 sleep mode. Id. (citing Ex. 1027, 25, 95, 96, 141). Petitioner further contends that a person of ordinary skill in the art would have understood that the "non-volatile memory" can be implemented in the SPD device separate from the integrated circuit implements the AMB (Advanced Memory Buffer) where the SPD is used to store configuration information in the non-volatile memory. Id. at 48–49 (citing Ex. 1023 ¶ 19; Ex. 1027, 117; Ex. 1028, 13; Ex. 1066, 26:64–27:4; Ex. 1067, p.1-1; Ex. 1003 ¶ 436). Petitioner further contends a person of ordinary skill in the art would have understood that the logic element includes discrete electrical elements such as resistors and capacitors, as taught by the FBDIMM Standards. Id. at 49–50 (citing Ex. 1003 ¶ 475; Ex. 1023 ¶ 9, Fig. 1A; Ex. 1028, 13, 42–45). . . .

. . . . Based on our review and consideration of the current record, we determine that Petitioner has adequately shown that the combination of Harris with the FBDIMM Standards renders claim 15 obvious for purposes of institution.

'918: ID at 32-33

Grounds 1-2 teach "non-volatile memory" in either the AMB Buffer or SPD



EX1023 (Harris) Fig. 3

7. Non-volatile memory for claims 10-11, 15, 22 (POR 43)

The Petition explained that the "non-volatile memory" for the "logic" can either be in Harris's Buffer (e.g., an AMB) or in an SPD connected to that Buffer. Pet. 47-50, 67-68, 72; EX2030, 285:3-286:17. Netlist argues it cannot be in an SPD—contrary to the Board's finding, ID 31-33—because the SPD is a "different component[]" from the AMB, POR 43. But Netlist's argument is contrary to the specification, which provides that the "logic" can be "***one or more*** integrated circuits," EX1001, 23:1-18, meaning the "logic" could comprise an SPD (with non-volatile memory) connected to an AMB, Pet. 47-49. Netlist also argues that standard AMBs did not include non-volatile memory, ignoring the obviousness of such a design, particularly in combination with Amidi. EX1003, ¶¶434-36.

'918: Paper 25 (Reply) at 23

'918: Paper 1 (Pet.) at 47-50, 67-68, 72; Paper 25 (Reply) at 23

"PRE-REGULATED INPUT VOLTAGE" ('918 CLAIMS 16-22 & 30)

GROUND 2

(HARRIS + FBDIMM STANDARDS + AMIDI)

The Institution Decision construed the claim such that Harris's "regulated" 12V input is a "*pre-regulated input voltage*"

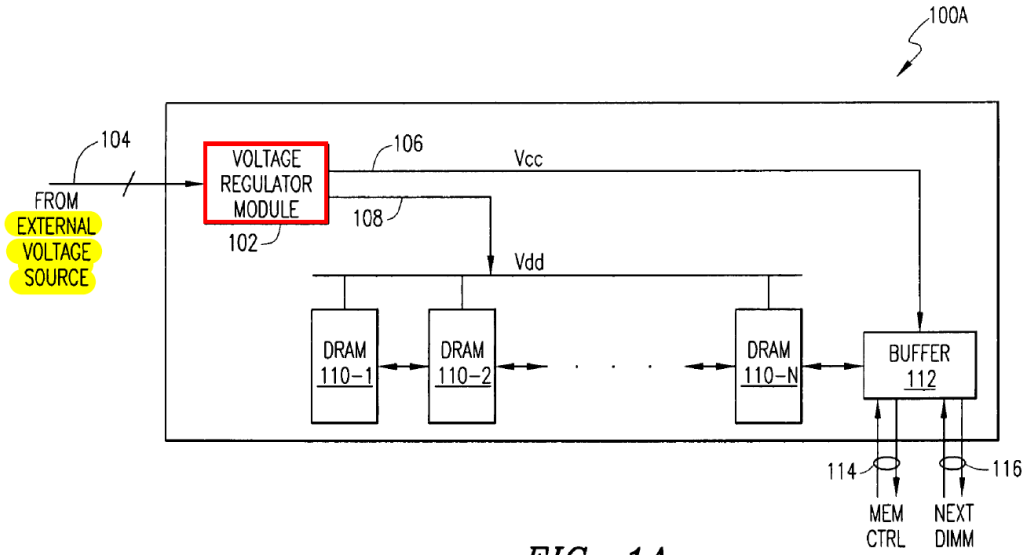


FIG. 1A

[0014] It should be readily recognized that the external voltage sources may comprise any combination of known or heretofore unknown voltage supplies, either regulated or unregulated, and even including variable voltages.

For purposes of this decision, we interpret "pre-regulated voltage" to mean that the voltage is ***regulated before conversion*** to a stepped up or down level. *See* Ex. 1001, code (57), 28:53-58, Fig. 16 (1110, 1112). Patent Owner further argues that Amidi does not disclose a "pre-regulated voltage" but offers no interpretation for the term. Prelim. Resp. 39-40. We invite development of the record at trial to explain the meaning of "pre-regulated voltage." In any case, we find Petitioner's showing of obviousness with respect to these claims sufficient for institution.

'918: ID at 38 (emphasis added)
See also '054: ID at 39 (similar)

'918: Paper 1 (Pet.) at 73-75; Paper 25 (Reply) at 20

The District Court adopted a broad construction of "*pre-regulated input voltage*" (consistent with the Institution Decision)

> Samsung contends the claims require the "pre-regulated voltage" to be regulated by the memory module rather than the host system to which it connects. . . .Notably, the disputed term is a small part of the "buck converter" limitations and gives context to what the buck converters do – that is, receive an input voltage and produce an output voltage. And although the claims characterize the input voltage into the buck converters as "pre-regulated" and the output voltages as "regulated," they impose no further limitations on the buck converters or, for that matter, the memory module. Although the written description discloses such structure (e.g., first and second power elements 1130, 1140), the claims do not require it. Instead, they only require what the buck converters receive, not what the other elements of the memory module provides. Accordingly, the Court rejects Samsung's proposed construction. The term will otherwise be given its plain and ordinary meaning.

EX2032 (Claim Construction Order) at 21-22

'918: Paper 1 (Pet.) at 73-75; Paper 25 (Reply) at 20

It is undisputed Ground 2 teaches a "*pre-regulated input voltage*"

[2] Netlist's expert admitted that it was common at the time for the host system to provide a ***regulated*** "12V power supply." EX2031, ¶65; EX1075, 180:14-183:3; EX2038, 8, 13. Netlist argues that Harris is limited to receiving an ***unregulated*** 12V supply, POR 6-7, when in fact Harris teaches that the input voltage can be "***regulated*** or unregulated," EX1023 [0014]. Indeed, both experts agree that Harris's disclosure of a 12V supply with "wide tolerance (e.g., around +/-15%)," *id*. [0013], means that the voltage is ***regulated*** to stay within those limits. EX1003, ¶487; EX1075, 179:21-180:6, 183:7-184:11; EX2030, 65:23-66:6, 273:7-:12, 274:17-275:3.

[3] The District Court construed "pre-regulated input voltage" to have its plain and ordinary meaning, EX2032, 21-22, 34, similar to the Board, ID 37-38, and rejected Samsung's argument that the voltage must be pre-regulated ***on*** the memory module, EX2030, 268:18-270:5. Netlist's expert does not dispute the District Court's construction. EX1075, 142:10-144:18. Both experts agree that the 12V input to Harris can be pre-regulated under that construction. *See supra* p.5, note 2.

'918: Paper 25 (Reply) at 5 n.2, 20 & n.3

CONTROLLER
(’054 CLAIMS 5, 7-8, 23-24)

GROUND 2

(HARRIS + FBDIMM STANDARDS + AMIDI)

Grounds 2-3 use the battery-powered "logic" in Amidi as the "controller" to switch to S3 sleep mode in the event of a power disruption

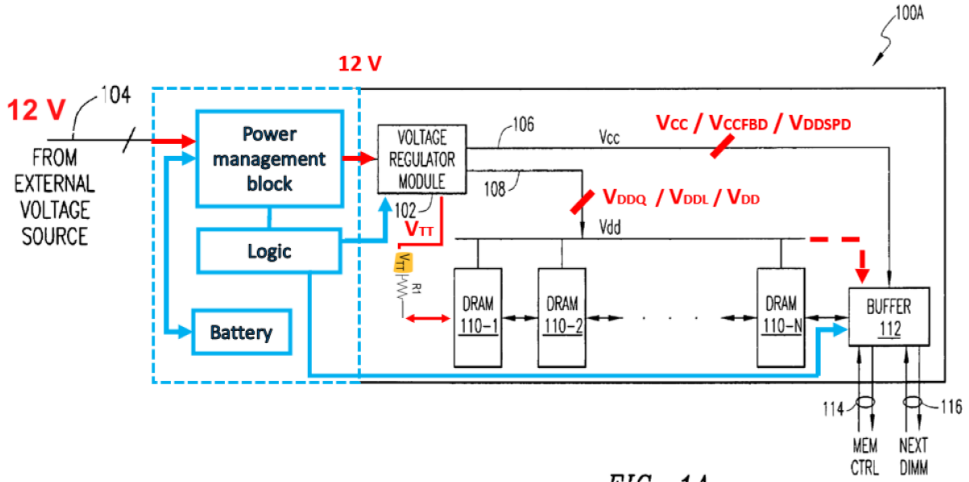


FIG. 1A

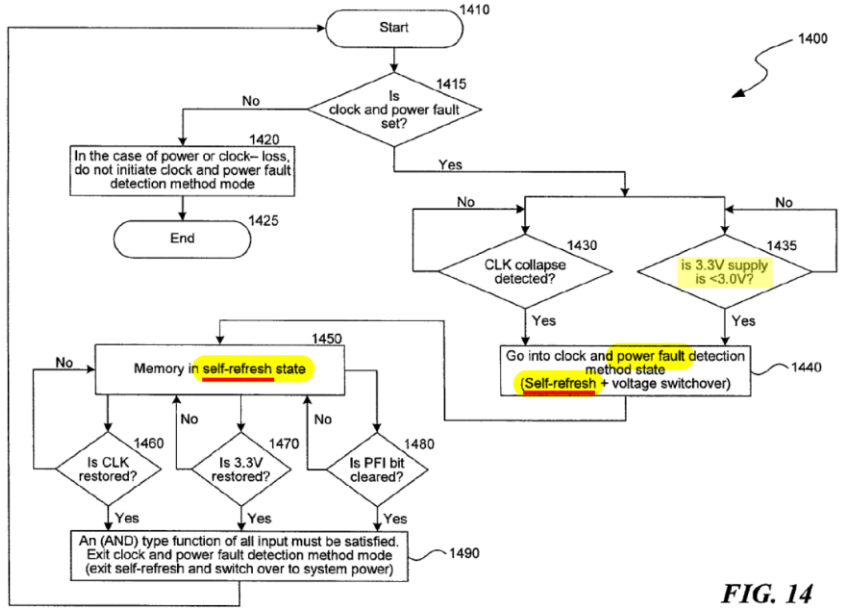


FIG. 14

Petitioner contends that the logic for controlling the S3 sleep mode (Pet. 43–44) corresponds to the claimed "controller" that is coupled to the voltage monitor circuit. Pet. 50–51. Petitioner contends that S3 configuration information is stored in non-volatile memory before entering the S3 sleep mode in response to the trigger signal, satisfying the "wherein" clause of claim 4. Id. at 51 (citing Ex. 1003 ¶¶ 322–340). . . . Petitioner shows sufficiently that claim 5 would have been obvious over the combination of Harris, the FBDIMM Standards, and Amidi.

'054: ID at 35

'054: Pet. 43-44, 50-52; Paper 26 (Reply) at 23-24

Grounds 2-3 use the battery-powered "logic" in Amidi as the "controller" to switch to S3 sleep mode in the event of a power disruption

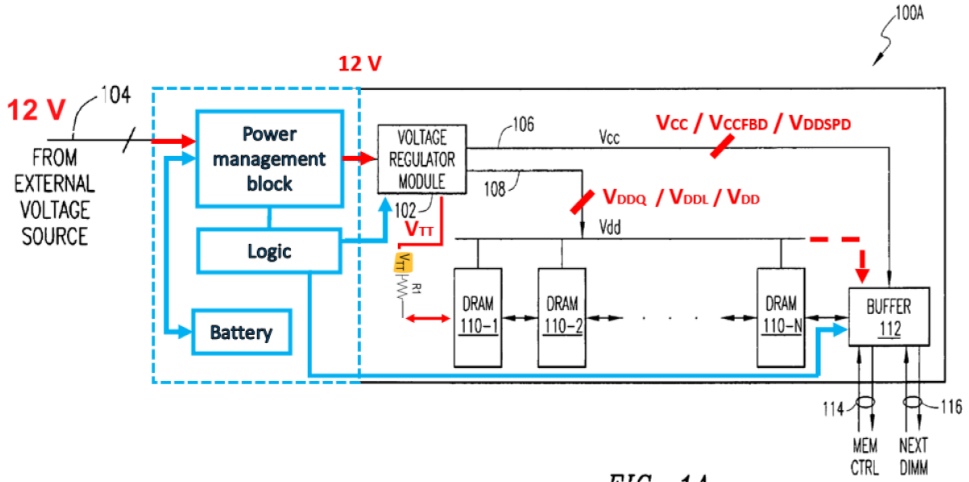


FIG. 1A

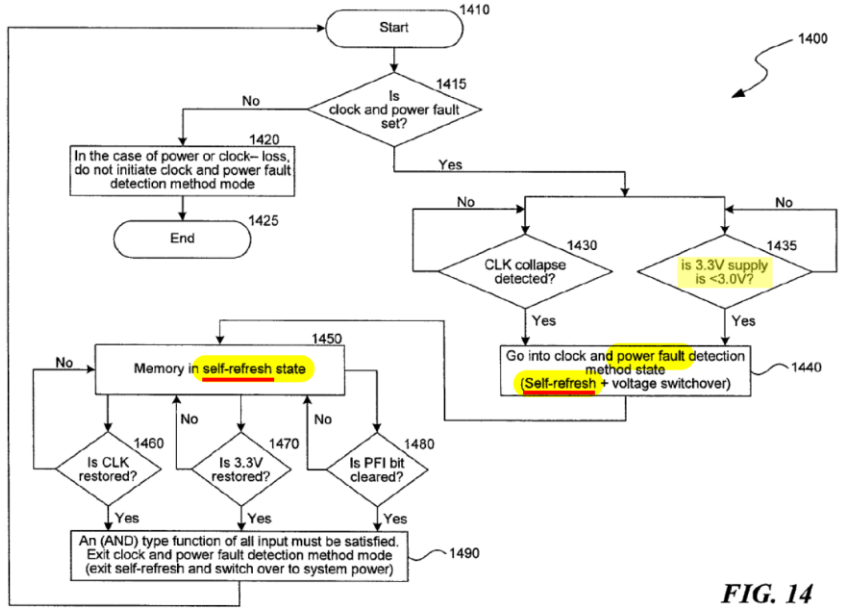


FIG. 14

6. Controller for claims 5, 7–8, 23–24 (POR 46-47)

Netlist misleadingly argues that Grounds 1-3 lack the "*controller*" to cause the S3 sleep mode, because conventionally this mode is initiated by the system controller, which is outside of the memory module. POR 46-47. But this argument ignores the combination of FBDIMM's S3 mode in Harris with Amidi's teaching of backup power management and logic functionality on the memory module to "maintain memory (through refresh, for example)." Pet. 43-44, 50-52; ID 35, 36; EX1024, 2:16-:19, Fig.11; EX1003, ¶¶175-77. In case of a power failure, Amidi's logic disconnects the system memory controller from the module, EX1003, ¶¶329-30, so a POSITA "would have been motivated to use the S3 mode of buffer 112 [on Harris's module] when implementing the backup power supply and logic functionality as disclosed in Amidi, because S3 mode performs the function of refreshing the memory (e.g., self refresh), just like in Amidi," *id.* ¶330.

'054: Paper 26 (Reply) at 23-24

'054: Pet. 43-44, 50-52; Paper 26 (Reply) at 23-24

GROUNDS 4-5 (SPIERS) 03

BAKER BOTTS

SUMMARY OF COMBINATIONS

Ground 4: Spiers + Amidi

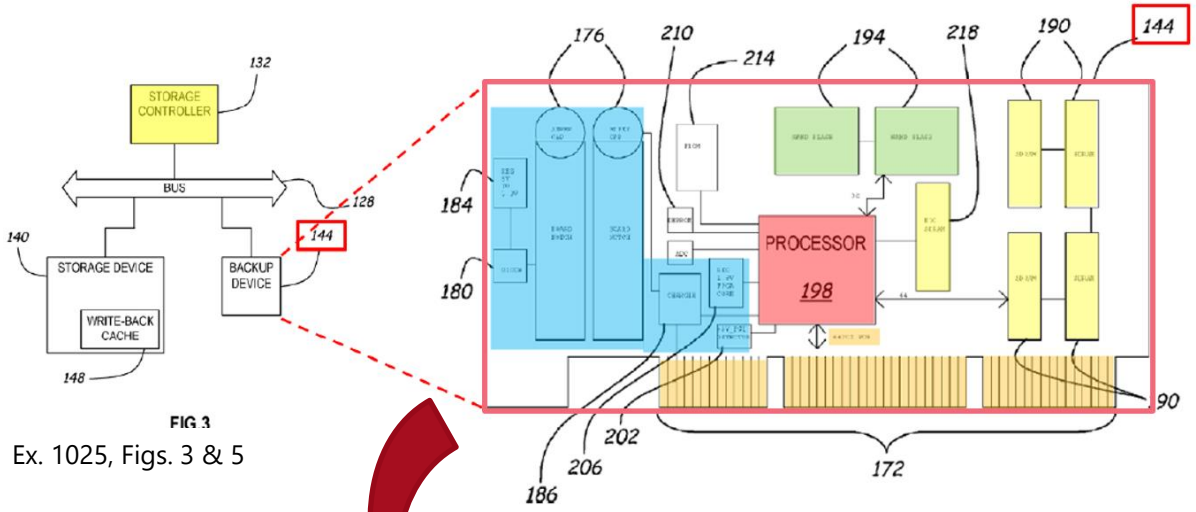


FIG 3

Ex. 1025, Figs. 3 & 5

Spiers

- Teaches **memory module** that transfers data from **volatile memory** to **non-volatile** in event of power disruption using **backup power from capacitors**
- Very similar to the disclosure of the '918 and '054 Patents

Amidi

- Directed at providing **battery backup** for a **memory module**
- Teaches DDR2 SDRAM devices, and DDR3 was also known by 2007

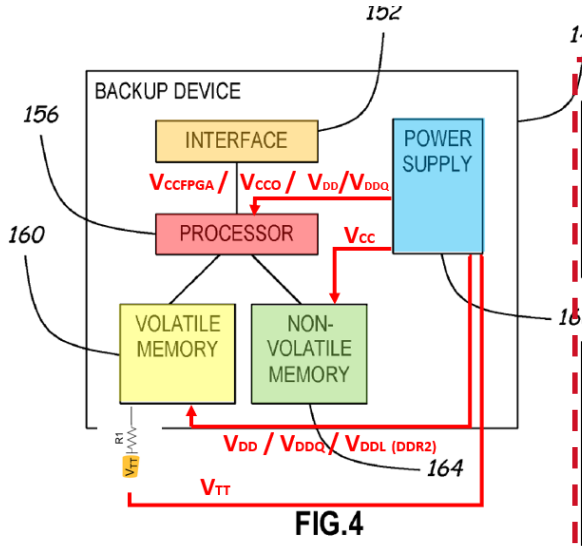


FIG.4

144

054 Mappings

Voltage Mapping (A) for DDR3
1st : VDD/VDDQ to DRAM/FPGA = 1.5V
2nd : VCCFPGA to FPGA Core = 1.8V
3rd : (i) VTT to DRAM Bus = 0.75V
(ii) VCC to NV Memory = 3.3V
(iii) VCCO to FPGA I/O = 3.3V

Voltage Mapping (B) for DDR2
1st : VDD/VDDQ to DRAM/FPGA = 1.8V
2nd : VCCFPGA to FPGA Core = 1.8V
3rd : (i) VTT to DRAM Bus = 0.9V
(ii) VCC to NV Memory = 3.3V
(iii) VCCO to FPGA I/O = 3.3V
(iv) VDDL to DRAM = 1.8V

188

918 Mappings

Voltage Mapping (A) for DDR3
1st : VDD/VDDQ to DRAM = 1.5V
2nd : VCCFPGA to FPGA Core = 1.8V
3rd : VTT to Terminate DRAM Bus = 0.75V
4th : VCC to NV Memory / VCCO to FPGA I/O = 3.3V

Voltage Mapping (B) for DDR2
1st : VDD/VDDQ to DRAM = 1.8V
2nd : VCCFPGA to FPGA Core = 1.8V
3rd : VTT to Terminate DRAM Bus = 0.9V
4th : VCC to NV Memory / VCCO to FPGA I/O = 3.3V

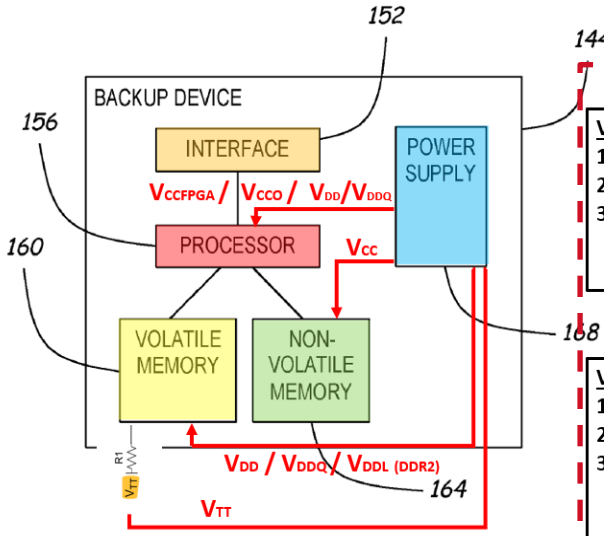
Voltage Mapping (C) for DDR2
1st : VDD/VDDQ to DRAM = 1.8V
2nd : VCCFPGA to FPGA Core = 1.8V
3rd : VCC to NV Memory = 3.3V
4th : VCCO to FPGA I/O = 3.3V

'918: Paper 1 (Pet.) at 79-82; Paper 25 (Reply) at 24
'054: Paper 1 (Pet.) at 72-77; Paper 26 (Reply) at 24

Ground 4: Spiers + Amidi

"Where a prior art patent discloses a ***range of values***, showing a claimed value falls within that range meets a party's burden of establishing the narrower claim would have been obvious where there is no reason to think the result would be unpredictable."

Gen. Hosp. Corp. v. Sienna Biopharms., Inc., 888 F.3d 1368, 1373 (Fed. Cir. 2018); *see also, e.g., Iron Grip Barbell Co. v. USA Sports, Inc.*, 392 F.3d 1317, 1320-23 (Fed. Cir. 2004) (claim to three grips obvious in light of prior art teaching one, two, and four grips)



Ex. 1025, Fig. 4

144

054 Mappings

Voltage Mapping (A) for DDR3
1st : VDD/VDDQ to DRAM/FPGA = 1.5V
2nd : VCCFPGA to FPGA Core = 1.8V
3rd : (i) VTT to DRAM Bus = 0.75V
(ii) VCC to NV Memory = 3.3V
(iii) VCCO to FPGA I/O = 3.3V

168

Voltage Mapping (B) for DDR2
1st : VDD/VDDQ to DRAM/FPGA = 1.8V
2nd : VCCFPGA to FPGA Core = 1.8V
3rd : (i) VTT to DRAM Bus = 0.9V
(ii) VCC to NV Memory = 3.3V
(iii) VCCO to FPGA I/O = 3.3V
(iv) VDDL to DRAM = 1.8V

918 Mappings

Voltage Mapping (A) for DDR3
1st : VDD/VDDQ to DRAM = 1.5V
2nd : VCCFPGA to FPGA Core = 1.8V
3rd : VTT to Terminate DRAM Bus = 0.75V
4th : VCC to NV Memory / VCCO to FPGA I/O = 3.3V

Voltage Mapping (B) for DDR2
1st : VDD/VDDQ to DRAM = 1.8V
2nd : VCCFPGA to FPGA Core = 1.8V
3rd : VTT to Terminate DRAM Bus = 0.9V
4th : VCC to NV Memory / VCCO to FPGA I/O = 3.3V

Voltage Mapping (C) for DDR2
1st : VDD/VDDQ to DRAM = 1.8V
2nd : VCCFPGA to FPGA Core = 1.8V
3rd : VCC to NV Memory = 3.3V
4th : VCCO to FPGA I/O = 3.3V

'918: Paper 1 (Pet.) at 87
'054: Paper 1 (Pet.) at 82-83

Ground 5: adds Hajeck

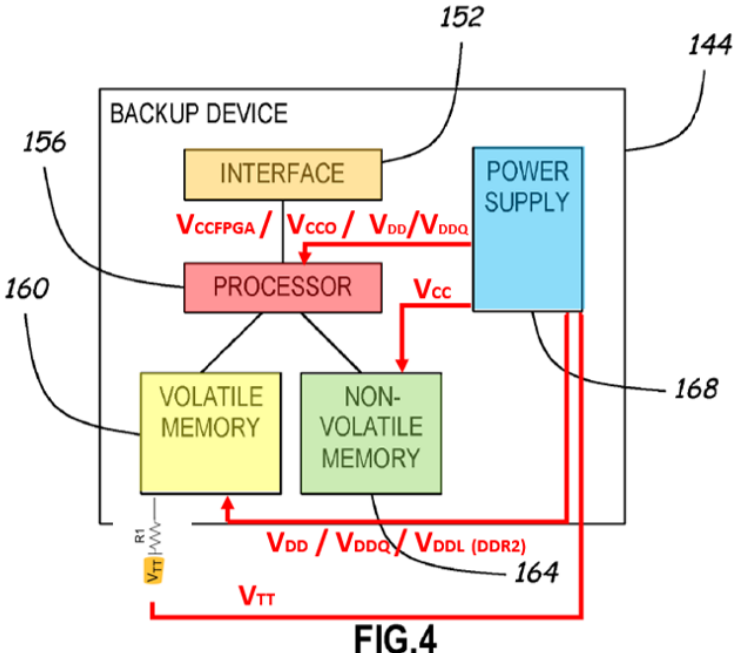
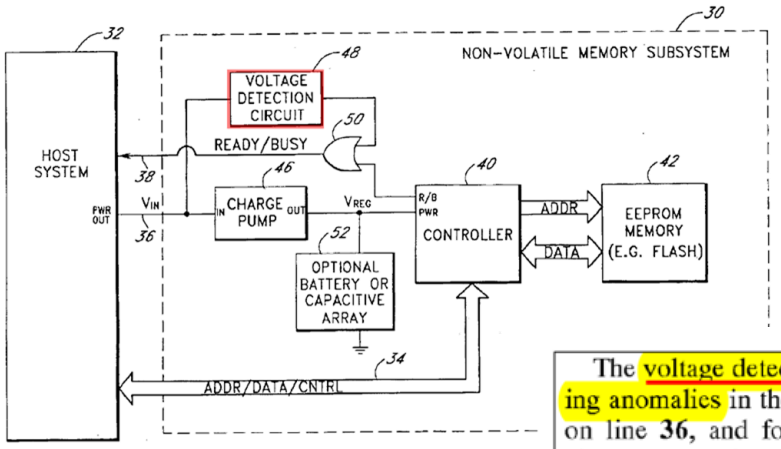


FIG.4

Ex. 1025, Fig. 4



Ex. 1038 (Hajeck), Fig. 1 & 3:30-43

The voltage detection circuit **48** is responsible for detecting anomalies in the power signal V_{IN} supplied by the host on line **36**, and for driving the ready/busy signal to the "busy" state when such anomalies are detected. A conventional voltage detection circuit may be used. The voltage detection circuit **48** may be designed to generate a "busy" signal whenever V_{IN} falls below a certain level, such as 2.6 or 2.7 volts. The voltage detection circuit may also be designed to generate a busy signal when the voltage exceeds a certain level, and/or when other types of anomalies are detected. To inhibit rapid transitions between the "ready" and "busy" states, the voltage detection circuit may be designed to provide a degree of hysteresis, and/or to hold its output for a particular time period after a state transition.

Hajeck

- Teaches **voltage detection circuit**
- Specifically includes monitoring both **over**voltage and **under**voltage conditions

'918: Paper 1 (Pet.) at 13-14 and 129
'054: Paper 1 (Pet.) at 12-13 and 125-26

SPIERS' PCI CARD WITH MEMORY IS A "MEMORY MODULE"

GROUND 4

(SPIERS + AMIDI)

The Institution Decision correctly found that Spiers discloses a "*memory module*" (144)

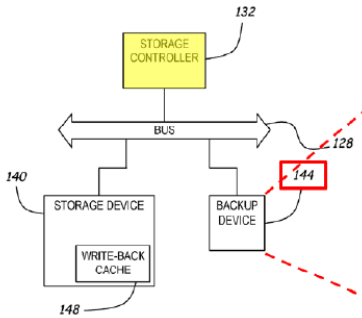


FIG.3

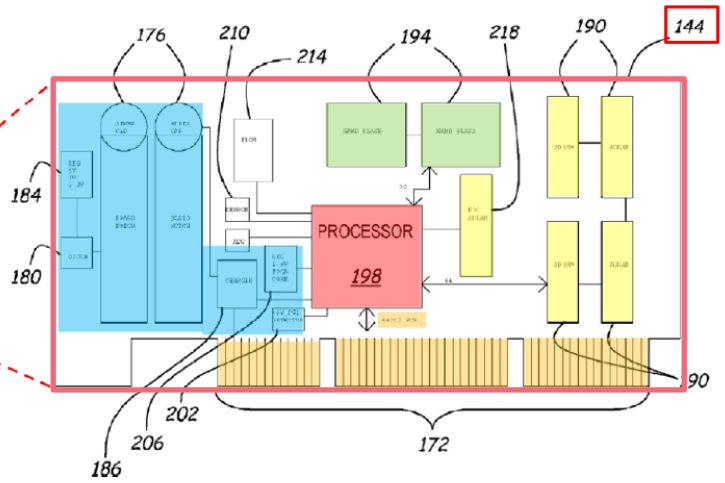


FIG.5

Ex. 1025, Figs. 3 & 5

Petitioner contends that Spiers discloses the preamble of claim 1. Pet. 82. Petitioner contends that Spiers's **backup device 144** corresponds to the claimed "memory module." *Id.* at 77. Spiers's **backup module 144** has both volatile memory (**SDRAMs 190**) and non-volatile memory (**NAND flash 194**). *Id.* (citing Ex. 1025 ¶¶ 34, 37, Figs. 3, 5; Ex. 1003 ¶¶ 643-646). . . .

Based on our review and consideration of the current record, we determine that Petitioner has adequately shown that Spiers teaches the preamble for purposes of institution.

'918: ID at 45
See also '054: ID at 47-48 (similar)

Neither the Board nor the District Court limited a "*memory module*" to a "***main*** memory module"

Neither party argues whether the preamble limits claim 1. Although we find that the evidence supports that the prior art teaches the preamble, we make no determination at this stage of the proceeding that the preamble of claim 1 is limiting.

'054: ID at 18 n.2; '918 ID at 18 n.1

"a memory module" ('918 Patent, all claims; '054 Patent, all claims)	Limiting.

The Court **ORDERS** each party not to refer, directly or indirectly, to its own or any other party's claim-construction positions in the presence of the jury. Likewise, the Court **ORDERS** the parties to refrain from mentioning any part of this opinion, other than the actual positions adopted by the Court, in the presence of the jury. Neither party may take a position before the jury that contradicts the Court's reasoning in this opinion. Any reference to claim construction proceedings is limited to informing the jury of the positions adopted by the Court.

EX2032 at 35

'918: Paper 25 (Reply) at 1 and 23-26
'054: Paper 26 (Reply) at 1-2 and 24-28

District Court did not limit a "*memory module*" to a "*main* memory module"

Having reviewed the entire patent "to gain an understanding of what the inventors actually invented and intended to encompass by the claim[s]," *Catalina Mktg. Int'l*, 289 F.3d at 808–09, the Court finds the preamble limiting. While the claims recite many of the structural requirements of a "memory module," the claims arguably read on other modular computer devices, such as a video card or network controller, despite no evidence the inventors intended to encompass such devices by the claims. To the contrary, as the Overview section explains, the invention "is couplable *to a memory controller* of a host system," '918 Patent at 3:66–67 (emphasis added), not just the host system as recited in the claims. *See also id.* at 1:66–67 ("[t]he present disclosure relates generally to computer memory devices"). Thus, a skilled artisan would understand a "memory module" is distinct from, and has essential structural requirements not necessarily found in, other modular computer accessories. That includes the structure necessary to connect to a memory controller. *See Memory Systems: Cache, DRAM, Disk*, Dkt. No. 76-17 at 319 (depicting, in FIG. 7.6, a memory controller connected to two memory modules). Accordingly, the preambles are limiting.

EX2032 at 28

'918: Paper 25 (Reply) at 1 and 23-26
'054: Paper 26 (Reply) at 1-2 and 24-28

"*memory module*" not limited to "*<u>main</u>* memory module"

[] Q. Okay. And you said that at the time of the invention, memory modules are generally understood to be ones designed to connect to the primary memory controller for the purpose of the holding general purpose code and data in a computer system.

A. If we were talking about them in a general purpose computer context, I think that that would be the most common understanding.

Q. Okay. What about in the context of '918? What is that understanding? [...]

[A]: I think the '918 is a little bit broader, that it talks about a memory module as kind of being a circuit board that connects to a host computer that includes memory.

[]Q. Where does it say that?

A. In the abstract. [...]

EX2030/EX2060 (Wolfe) at 125:5-126:4

(57) **ABSTRACT**

In certain embodiments, a memory module includes a printed circuit board (PCB) having an interface that couples it to a host system for provision of power, data, address and control signals. First, second, and third buck converters receive a pre-regulated input voltage and produce first, second and third regulated voltages. A converter circuit

EX1001 at Abstract

'918: Paper 25 (Reply) at 1
'054: Paper 26 (Reply) at 1-2

"memory module" not limited to *"main* memory module"

Q. Okay. So like by 2004-2005 time period, if a person of ordinary skill in the art at one time was talking about memory module, they are thinking about a printed circuit board that's going to be inserted into a memory slot rather than a general-purpose bus slot. Does that sound right? [...]

[A]: I think that would be the most common, but I think they would be familiar with both.

[]Q. I'm just asking you, when a person of ordinary skill in the art hear the word "memory module," what would they understand it to be?

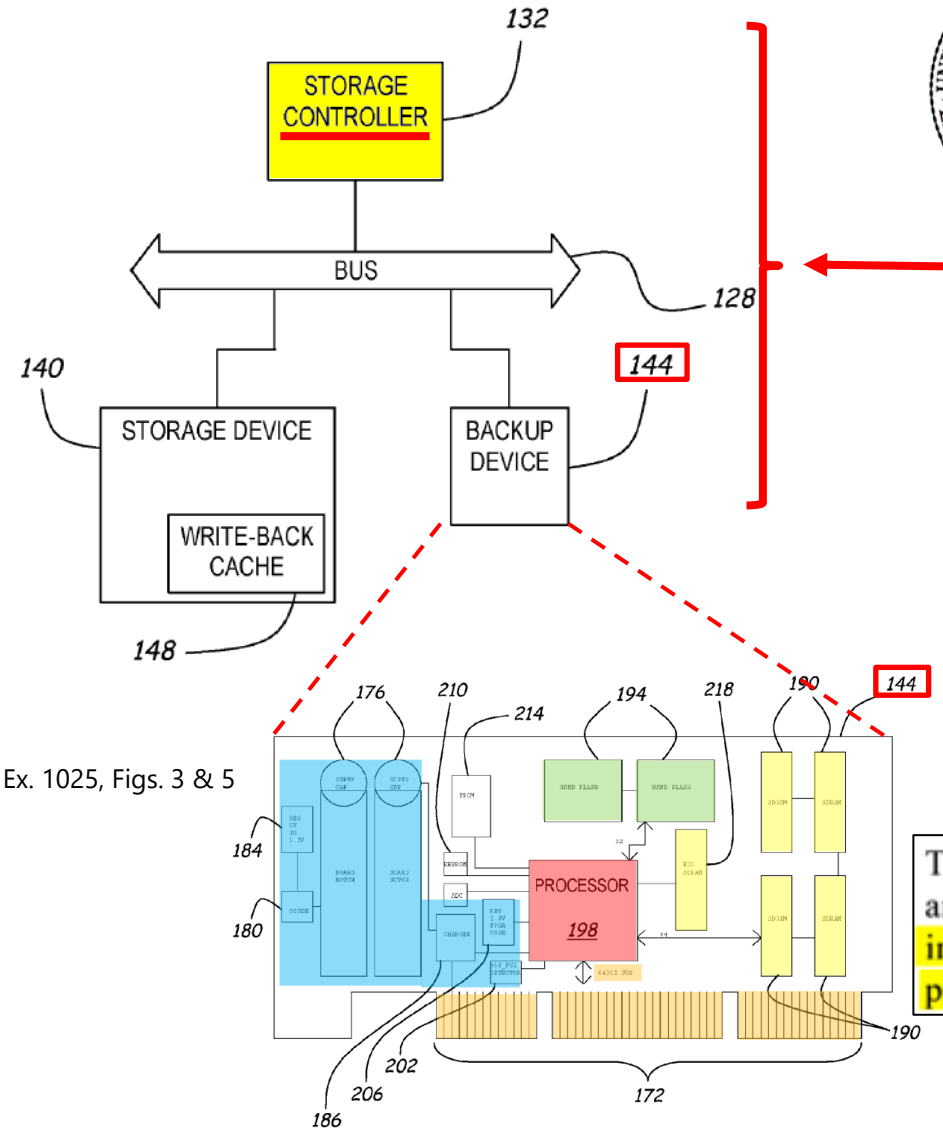
A. I think they'd look for context. And in the context of the '912 patent, I think that they are looking for something that would go into a dedicated memory slot. But in another context, they may be looking for something broader.

Unrelated patent and IPR

EX2056 at 101:9-102:3 (from unrelated IPR about unrelated patent)

'918: Paper 25 (Reply) at 1
'054: Paper 26 (Reply) at 1-2

The PCI card in Spiers satisfies the District Court's comments on *"memory module"*

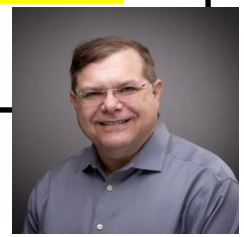


Ex. 1025, Figs. 3 & 5

"Thus, a skilled artisan would understand a 'memory module' is distinct from, and has essential structural requirements not necessarily found in, other modular computer accessories. That includes the structure necessary to connect to a memory controller."

EX2032 at 28

[A]: Why would this card be memory? Because its purpose is to hold memories. If you look at the intended use of the PCI bus in the spec, it says it's used for peripheral controllers, add-in boards and processor memory systems.



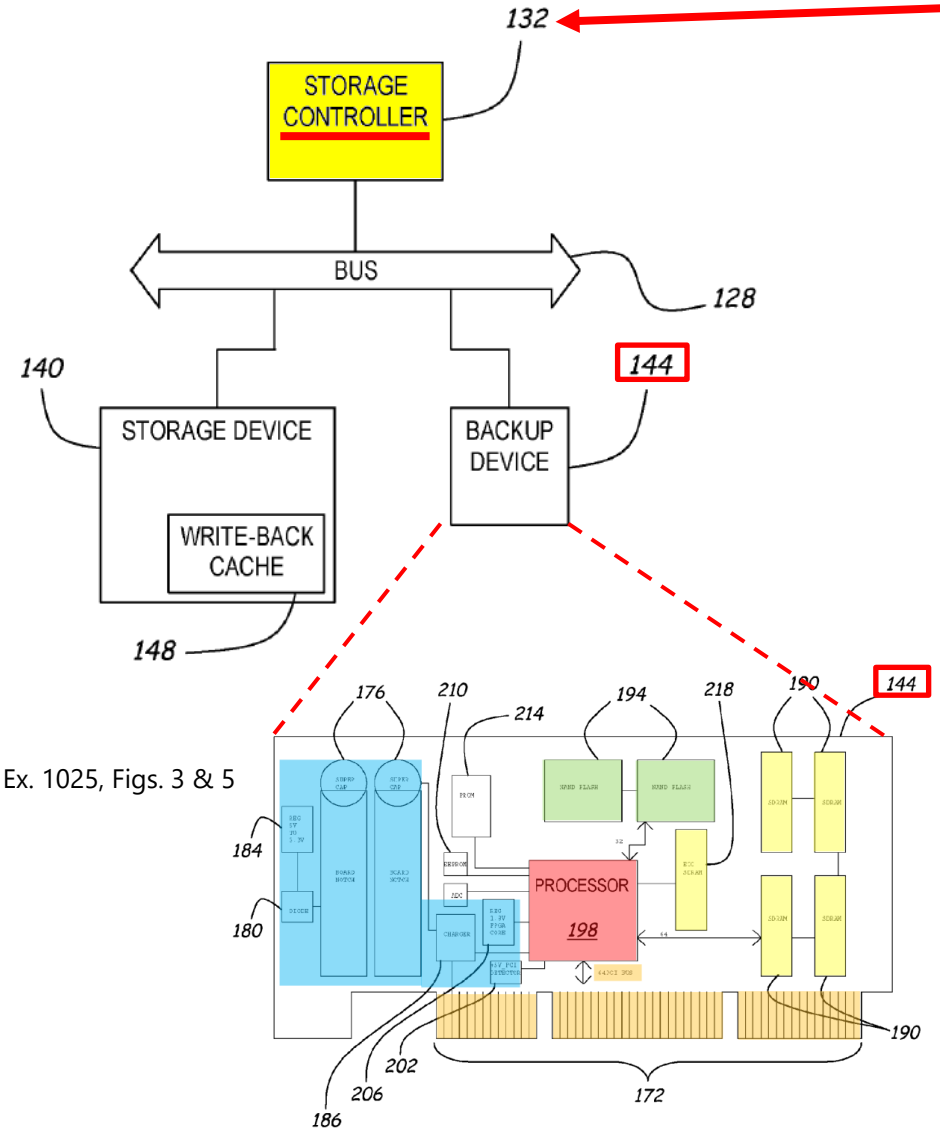
EX2030/EX2060 (Wolfe) at 177:25-179:9

The PCI Local Bus is a high performance 32-bit or 64-bit bus with multiplexed address and data lines. The bus is intended for use as an interconnect mechanism between highly integrated peripheral controller components, peripheral add-in boards, and processor/memory systems.

EX1031 (PCI Local Bus Specification) at 1

'918: Paper 25 (Reply) at 1 and 23-26
'054: Paper 26 (Reply) at 1-2 and 24-28

The PCI card in Spiers satisfies the District Court's comments on *"memory module"*



Ex. 1025, Figs. 3 & 5

Q. And what is the storage controller in Figure 3 of Spiers?

A. I think the most likely understanding of a person of ordinary skill is that it's an ordinary microprocessor.

Q. Is that a memory controller?

A. It would incorporate a memory controller to access memory.

EX2030/EX2060 at 213:1-8

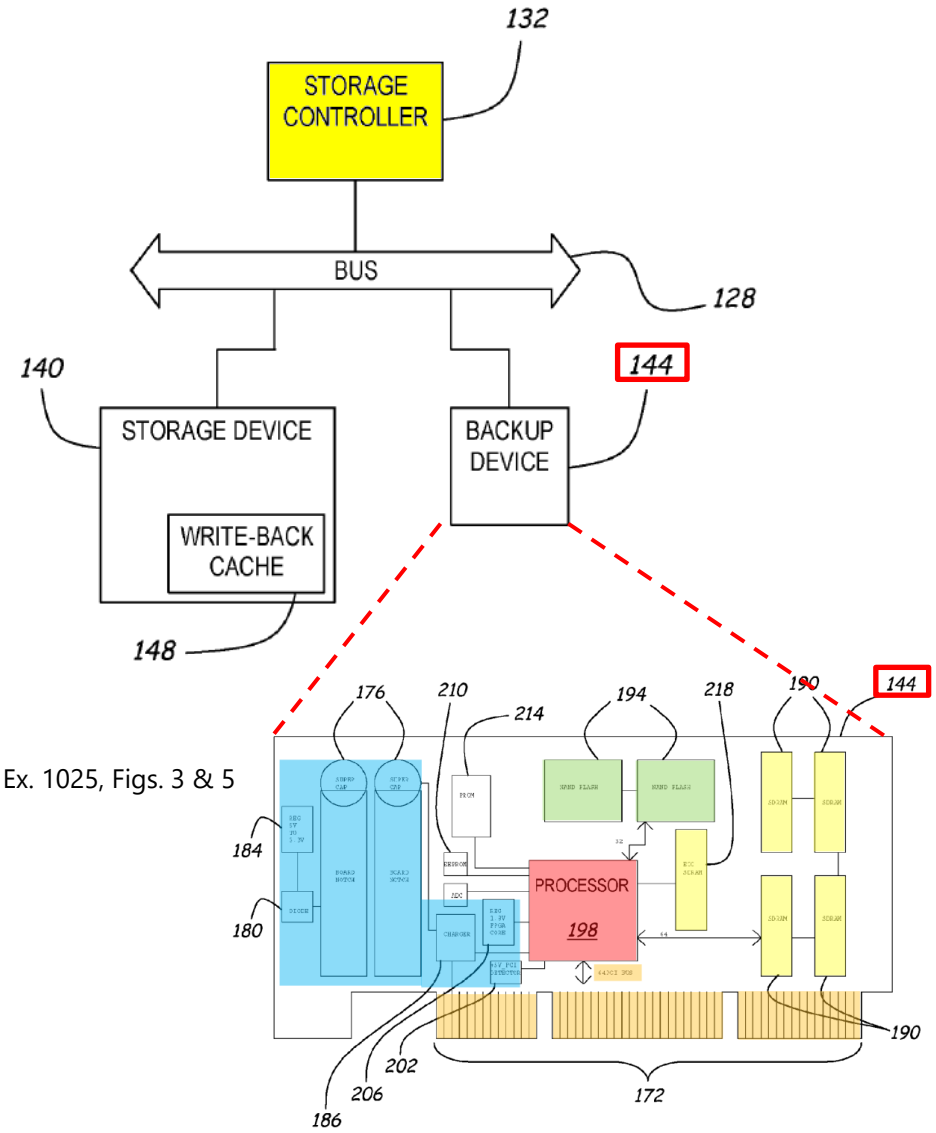
[0034] A disadvantage of using such a cache is that, if the storage device **140** loses power or has another failure that prevents the data from being written to the storage media, the data in the write-back cache **148** may be lost. Furthermore, because the storage device **140** reported that the write was complete, the entity writing the data to the storage device **140** is not aware that the data has been lost, or what data has been lost. In the embodiment of **FIG. 3**, the storage controller **132** stores a copy of the data in the backup device **144** as well as writing the data to the storage device **140**. In this embodiment, if a failure occurs which results in the

EX1025 (Spiers) at [0034]

'918: Paper 25 (Reply) at 1 and 23-26

'054: Paper 26 (Reply) at 1-2 and 24-28

The PCI card in Spiers satisfies the District Court's comments on *"memory module"*



Ex. 1025, Figs. 3 & 5

Q. Okay. So by 2007 or so, a PCI card probably would not be regarded in general as a memory module; correct? [...]

[A]: No. Like I said, it's depending on context. If it's a PCI card that's used to host memory, it would be reasonable to call it a memory module. It's just not the most common kind of memory module.

[...]

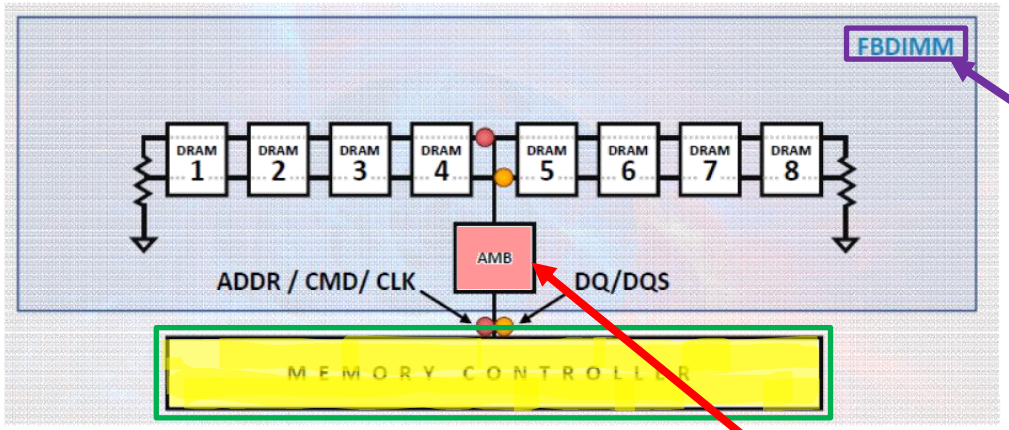
Q. So according to you then, the PCI card would always be a memory card, wouldn't it?

A. No. PCI cards that are intended to provide memory are memory modules, and PCI cards that are intended to provide peripheral input/output are I/O modules.

EX2030/EX2060 at 177:25-179:9

'918: Paper 25 (Reply) at 1 and 23-26
'054: Paper 26 (Reply) at 1-2 and 24-28

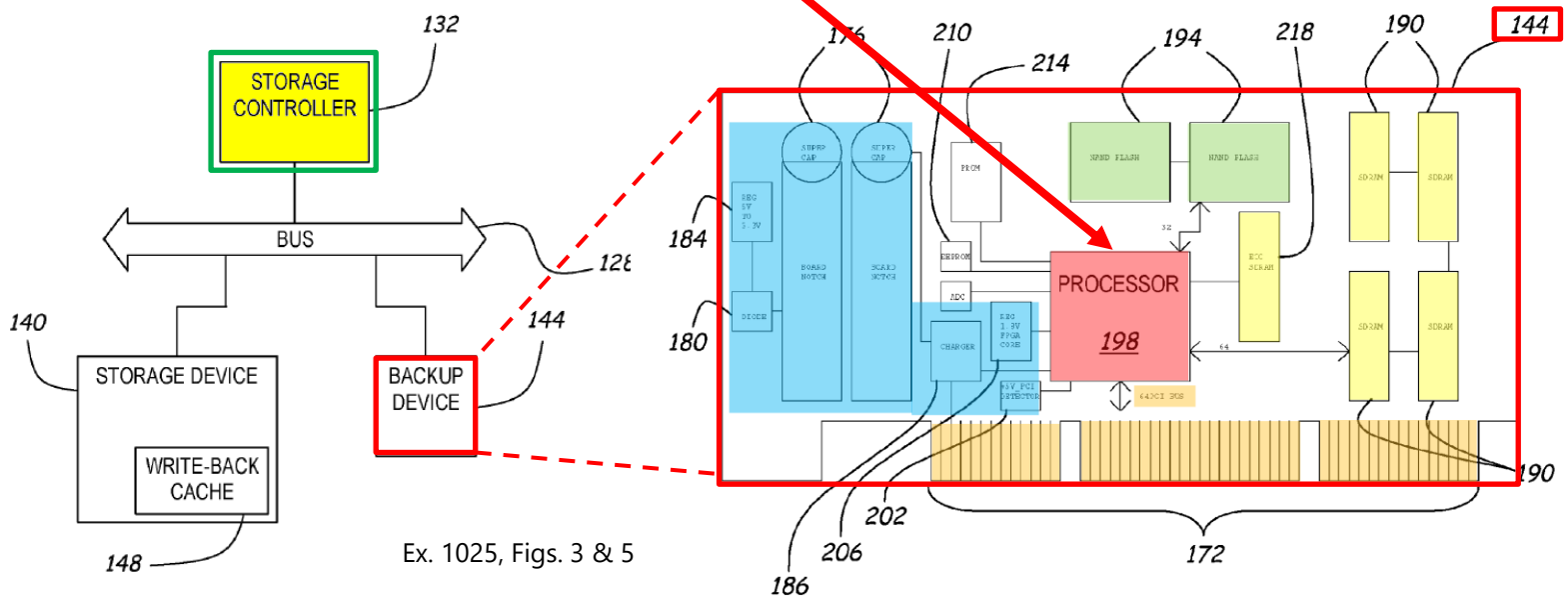
Processor 198 in Spiers is like the AMB in an FBDIMM (an embodiment of the 918/054 Patent)



EX1077, 9; *see also* EX1075 (Mangione-Smith), 97:16- 98:18

50 millimeters or more. In certain other embodiments, the PCB **1020** has a very low profile (VLP) form factor with a height of 18.3 millimeters. Other form factors including, but not limited to, small-outline (SO-DIMM), unbuffered (UDIMM), registered (RDIMM), fully-buffered (FB-DIMM), miniDIMM, mini-RDIMM, VLP mini-DIMM, micro-DIMM, and SRAM DIMM are also compatible with certain embodiments described herein. For example, in other embodiments, certain non-DIMM form factors are possible such as, for example, single in-line memory module (SIMM), multi-media card (MMC), and small computer system interface (SCSI).

EX1001, 21:47-51

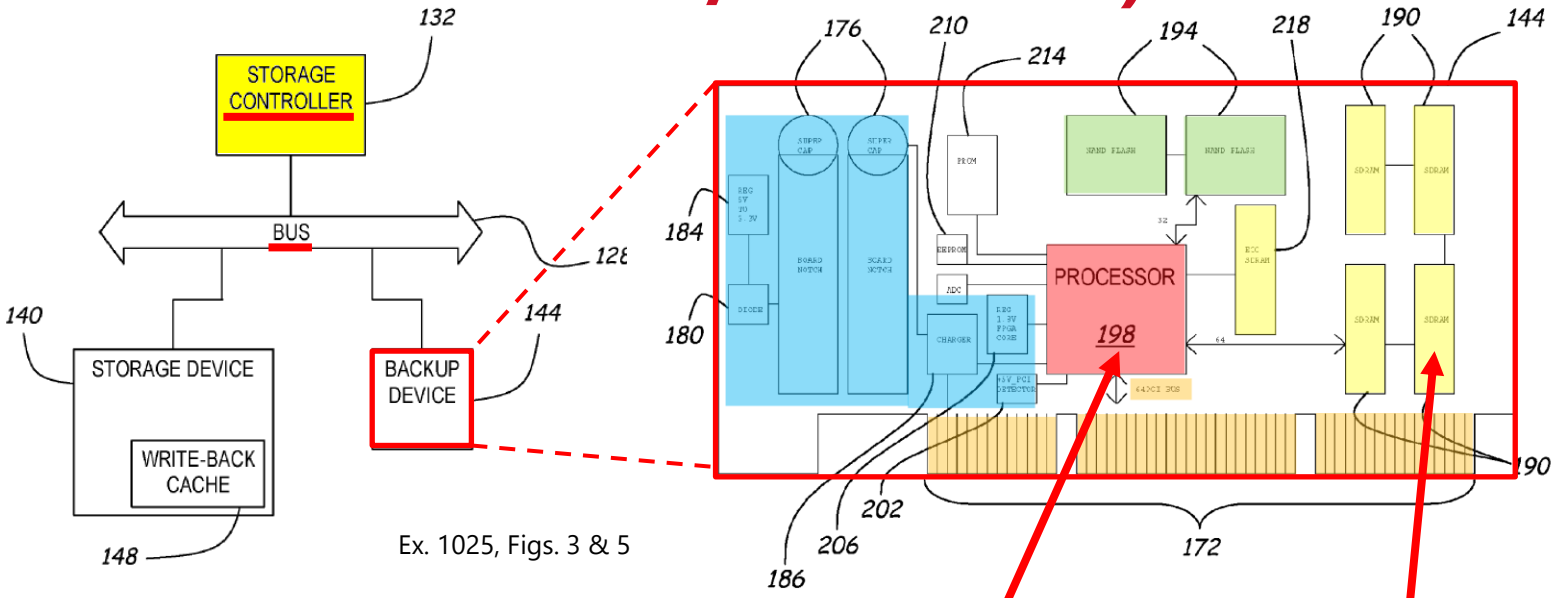


Ex. 1025, Figs. 3 & 5

FIG.3

'918: Paper 25 (Reply) at 23-25
'054: Paper 26 (Reply) at 1-2 and 24-26

Processor 198 in Spiers is like the AMB in an FBDIMM (an embodiment of the 918/054 Patent)



Ex. 1025, Figs. 3 & 5

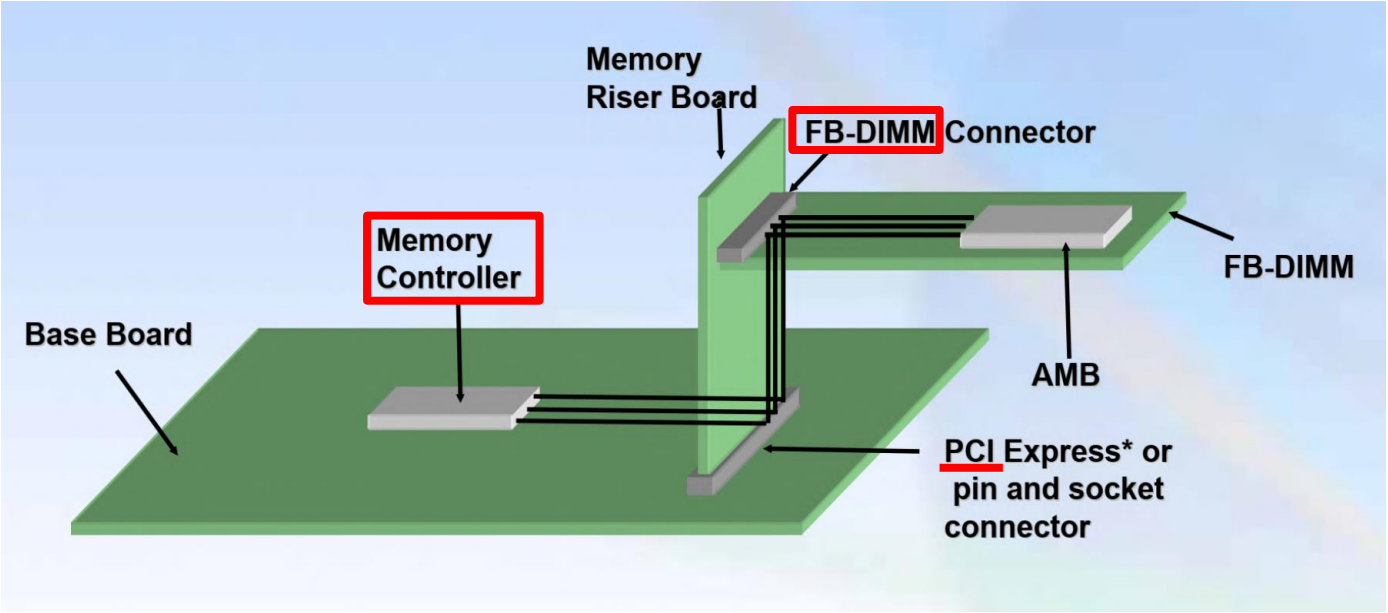
FIG.3

In the embodiment of **FIG. 5**, the volatile memory comprises a number of SDRAM modules **190**. The non-volatile memory in this embodiment comprises a number of NAND flash modules **194**. A FPGA processor **198** that provides PCI interfacing through a 64-bit PCI bus, is connected to the SDRAM modules **190** through a 64-bit bus, and is connected to the NAND flash modules **194** through a 32-bit bus. The FPGA

Ex. 1025 (Spiers), Figs. 3, 5, [0037]

'918: 918: Paper 1 (Pet.) at 83-84; Paper 25 (Reply) at 23-25
'054: Paper 1 (Pet.) at 77-78; Paper 26 (Reply) at 1-2 and 24-26

PCI cards were used as memory modules



EX2101, 14

The PCI Local Bus is a high performance 32-bit or 64-bit bus with multiplexed address and data lines. The bus is intended for use as an interconnect mechanism between highly integrated peripheral controller components, peripheral add-in boards, and processor/memory systems.

EX1031 (PCI Local Bus Specification) at 1

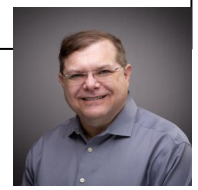
Q. Okay. So, for example, in Figure 5, you would probably refer to the SDRAM modules as memory modules but not necessarily the entire PCI card; is that right?

[A]: Again, it would depend on context. So I've heard people refer to a PCI memory card as a memory module, but in some contexts, you would not assume that if someone said memory module that that was a PCI card.

***

[A]: Why would this card be memory? Because its purpose is to hold memories. If you look at the intended use of the PCI bus in the spec, it says it's used for peripheral controllers, add-in boards and processor memory systems.

EX2030/EX2060 (Wolfe) at 177:25-178:22



'918: Paper 25 (Reply) at 25-26
'054: Paper 26 (Reply) at 26-27

OBVIOUS TO USE THREE (‘054) OR FOUR (‘918) REGULATED VOLTAGES

GROUND 4

(SPIERS + AMIDI)

The Institution Decision correctly found that Grounds 4-5 render obvious four regulated voltages

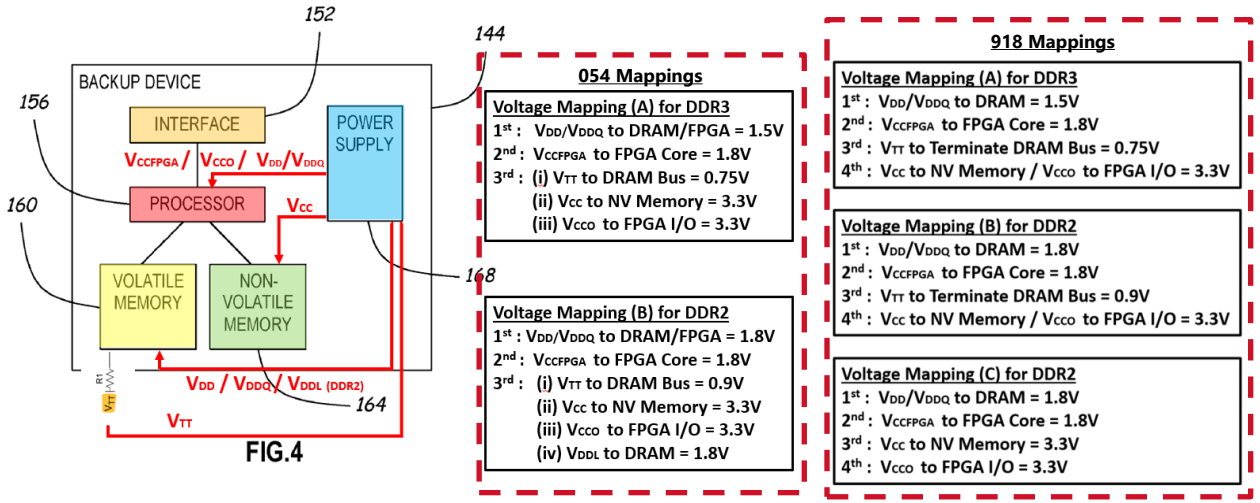


FIG.4

Petitioner further contends the person of ordinary skill in the art would have been familiar with the JEDEC standards for DDR2 and DDR3 devices, which specify the four or more voltages required for those memory devices. Id. Pet. 79 (citing Ex. 1026; Ex. 1046).

Patent Owner contends that Petitioner did not provide any evidence why one would need to use V_{TT} in the DDR2 or DDR3 standards. Prelim. Resp. 53-56. Even if Patent Owner is correct, Petitioner did not rely solely on V_{TT} as the third regulated voltage. *See* Pet. 86.

Patent Owner argues there is no evidence that one would have generated V_{TT} using a buck converter. Prelim. Resp. 53-56. Petitioner explained that the reason for using a buck converter for regulated voltages comes from Amidi. *See* Pet. 91 (citing Ex. 1024, 4:38-41, Fig. 6 (640)).

Patent Owner further argues that Petitioner provided no reason for equipping Spiers with multiple 1.8V regulators. Prelim. Resp. 59-60. Petitioner explained that the JEDEC standards provide for separate pins with the same voltage levels and that certain voltages should be isolated and separately controlled to provide independence, stability, and flexibility for power management. Pet. 30-31.

'918: ID at 46-50
See also '054: 49-50 (similar)

DDR2/DDR3 were well-known and would have motivated use of multiple voltages, including those required by JEDEC

054 Mappings

Voltage Mapping (A) for DDR3
1st : V_{DD}/V_{DDQ} to DRAM/FPGA = 1.5V
2nd : V_{CCFPGA} to FPGA Core = 1.8V
3rd : (i) V_{TT} to DRAM Bus = 0.75V
(ii) V_{CC} to NV Memory = 3.3V
(iii) V_{CCO} to FPGA I/O = 3.3V

Voltage Mapping (B) for DDR2
1st : V_{DD}/V_{DDQ} to DRAM/FPGA = 1.8V
2nd : V_{CCFPGA} to FPGA Core = 1.8V
3rd : (i) V_{TT} to DRAM Bus = 0.9V
(ii) V_{CC} to NV Memory = 3.3V
(iii) V_{CCO} to FPGA I/O = 3.3V
(iv) V_{DDL} to DRAM = 1.8V

918 Mappings

Voltage Mapping (A) for DDR3
1st : V_{DD}/V_{DDQ} to DRAM = 1.5V
2nd : V_{CCFPGA} to FPGA Core = 1.8V
3rd : V_{TT} to Terminate DRAM Bus = 0.75V
4th : V_{CC} to NV Memory / V_{CCO} to FPGA I/O = 3.3V

Voltage Mapping (B) for DDR2
1st : V_{DD}/V_{DDQ} to DRAM = 1.8V
2nd : V_{CCFPGA} to FPGA Core = 1.8V
3rd : V_{TT} to Terminate DRAM Bus = 0.9V
4th : V_{CC} to NV Memory / V_{CCO} to FPGA I/O = 3.3V

Voltage Mapping (C) for DDR2
1st : V_{DD}/V_{DDQ} to DRAM = 1.8V
2nd : V_{CCFPGA} to FPGA Core = 1.8V
3rd : V_{CC} to NV Memory = 3.3V
4th : V_{CCO} to FPGA I/O = 3.3V

2 DDR3 SDRAM Package Pinout and Addressing (Cont'd)
2.7 Pinout Description (Cont'd)

Table 1 — Input / output functional description

Symbol	Type	Function
DQU, DQL, DQS, DQS#, DQSU, DQSU#, DQSL, DQSL#	Input / Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS, DQSL, and DQSU are paired with differential signals DQS#, DQSL#, and DQSU#, respectively, to provide differential pair signaling to the system during reads and writes. DDR3 SDRAM supports differential data strobe only and does not support single-ended.
TDQS, TDQS#	Output	Termination Data Strobe: TDQS/TDQS# is applicable for x8 DRAMs only. When enabled via Mode Register A11 = 1 in MR1, the DRAM will enable the same termination resistance function on TDQS/TDQS# that is applied to DQS/DQS#. When disabled via mode register A11 = 0 in MR1, DM/TDQS will provide the data mask function and TDQS# is not used. x4/x16 DRAMs must disable the TDQS function via mode register A11 = 0 in MR1.
NC		No Connect: No internal electrical connection is present.
V_{DDQ}	Supply	DQ Power Supply: 1.5 V +/- 0.075 V
V_{SSQ}	Supply	DQ Ground
V_{DD}	Supply	Power Supply: 1.5 V +/- 0.075 V
V_{SS}	Supply	Ground
V_{REFDQ}	Supply	Reference voltage for DQ
V_{REFCA}	Supply	Reference voltage
ZQ, (ZQ0), (ZQ1)	Supply	Reference Pin for ZQ calibration
Note: Input only pins (BA0-BA2, A0-A15, RAS#, CAS#, WE#, CS#, CKE, ODT, and RESET#) do not supply termination.		

$V_{TT} = V_{DDQ}/2$

EX1046, 10, 109

'918: Paper 1 (Pet.) at 79-81; Paper 25 (Reply) at 26-27
'054: Paper 1 (Pet.) at 74-77; Paper 26 (Reply) at 27-28

DDR2/DDR3 were well-known and would have motivated use of multiple voltages, including those required by JEDEC

054 Mappings

Voltage Mapping (A) for DDR3
1st : V_{DD}/V_{DDQ} to DRAM/FPGA = 1.5V
2nd : V_{CCFPGA} to FPGA Core = 1.8V
3rd : (i) V_{TT} to DRAM Bus = 0.75V
(ii) V_{CC} to NV Memory = 3.3V
(iii) V_{CCO} to FPGA I/O = 3.3V

Voltage Mapping (B) for DDR2
1st : V_{DD}/V_{DDQ} to DRAM/FPGA = 1.8V
2nd : V_{CCFPGA} to FPGA Core = 1.8V
3rd : (i) V_{TT} to DRAM Bus = 0.9V
(ii) V_{CC} to NV Memory = 3.3V
(iii) V_{CCO} to FPGA I/O = 3.3V
(iv) V_{DDL} to DRAM = 1.8V

918 Mappings

Voltage Mapping (A) for DDR3
1st : V_{DD}/V_{DDQ} to DRAM = 1.5V
2nd : V_{CCFPGA} to FPGA Core = 1.8V
3rd : V_{TT} to Terminate DRAM Bus = 0.75V
4th : V_{CC} to NV Memory / V_{CCO} to FPGA I/O = 3.3V

Voltage Mapping (B) for DDR2
1st : V_{DD}/V_{DDQ} to DRAM = 1.8V
2nd : V_{CCFPGA} to FPGA Core = 1.8V
3rd : V_{TT} to Terminate DRAM Bus = 0.9V
4th : V_{CC} to NV Memory / V_{CCO} to FPGA I/O = 3.3V

Voltage Mapping (C) for DDR2
1st : V_{DD}/V_{DDQ} to DRAM = 1.8V
2nd : V_{CCFPGA} to FPGA Core = 1.8V
3rd : V_{CC} to NV Memory = 3.3V
4th : V_{CCO} to FPGA I/O = 3.3V

DDR2 SDRAM SPECIFICATION

V_{DDQ}	Supply	**DQ Power Supply:** 1.8V +/- 0.1V
V_{SSQ}	Supply	**DQ Ground**
V_{DDL}	Supply	**DLL Power Supply:** 1.8V +/- 0.1V

V_{DD}	Supply	**Power Supply:** 1.8V +/- 0.1V
V_{SS}	Supply	**Ground**
V_{REF}	Supply	**Reference voltage**

$V_{TT} = V_{DDQ}/2$

EX1026, Cover-1, 6-7, 71

'918: Paper 1 (Pet.) at 79-81; Paper 25 (Reply) at 26-27
'054: Paper 1 (Pet.) at 74-77; Paper 26 (Reply) at 27-28

Obvious to use DDR2/DDR3 to improve efficiency and speed

There is "'an implicit motivation to combine' to make a device 'more desirable, for example because it is…faster…or more efficient.'"

Intel Corp. v. Qualcomm Inc.,
21 F.4th 784, 797 (Fed. Cir. 2021)
(rejecting Board's contrary finding)

"[I]t's not necessary to show that a combination is the *best* option, only that it be a ***suitable*** option."

Intel Corp. v. PACT XPP Schweiz AG,
61 F.4th 1373, 1380-81 (Fed. Cir. 2023)
(reversing Board)

'918: Paper 25 (Reply) at 18 and 29-30
'054: Paper 1 (Pet.) at 29-30 and 85-86; Paper 26 (Reply) at 19 and 30-32

Using DDR2/DDR3 with a PCI board like Spiers would improve efficiency and speed

DDR1, DDR2 and DDR3 memories are powered up with 2.5, 1.8 and 1.5V supply voltages respectively, thus producing less heat and providing more efficiency in power management than normal SDRAM chipsets, which use 3.3V.

Typical Applications of DDRx Memories

Market analyses indicate that DDR is currently utilized in over 50 percent of all electronic systems, and usage is expected to increase to 80 percent over the next several years. DDR is not, and will never be, an "all things to all designs" technology. DDR memory is well suited for those designs that have a high read to write ratio. Quad-data-rate memory, for example, is designed for applications that require a 50 percent read/write ratio.

EX2012, 70 & 73

Q. Why would you use faster DDR2 DRAMs on Spiers PCI card?

A. There are a number of reasons. One is that by the time of the invention, PCI, especially in the 64-bit version that is described in Spiers, had been extended up to 1,066 megahertz, so you may need it just for the speed.

But, more importantly, DDR2 was available at higher densities. Over time, it had a lower cost per bit than older memories. It used less power per transaction than older memories, and because by 2007, DDR2 and DDR3 were the mainstream memories, they were much easier to obtain from multiple suppliers and across the supply chain, including spot markets because they had become the norm.

So all those reasons, including the improved density, the fact that you could get much more storage in a DDR2 or DDR3 than you could in an SDR would all motivate you to use the newer memory. And in fact, if we look across the industry, newer DRAM designs are almost ubiquitously used for new products.

EX2030/60, 150:20-151:16

'918: Paper 25 (Reply) at 28-29
'054: Paper 26 (Reply) at 29-30

A POSITA would be motivated to change the output of Spiers' regulator from 3.3V to the *lower* voltages of DDR2/DDR3, thus saving power

Q. So if I understand what you're saying is, you weren't personally involved so you don't personally know what the reasoning was of JEDEC lowering the voltage; but your understanding, as a technical matter, is that a consequence of the voltage getting lower with each version of the JEDEC standard, as you go from DDR1 to DDR2 to DDR3, is that the result would be less power consumption?

ATTORNEY LINDSAY: Objection; form.

THE WITNESS: I would go farther than that. As I said, all things being equal, lowering the voltage will reduce [sic] in lowering the power consumption, and that's just -- that's an incredibly consistent fact, motivation in the industry.

EX1075 (Mangione-Smith) 79:9-24

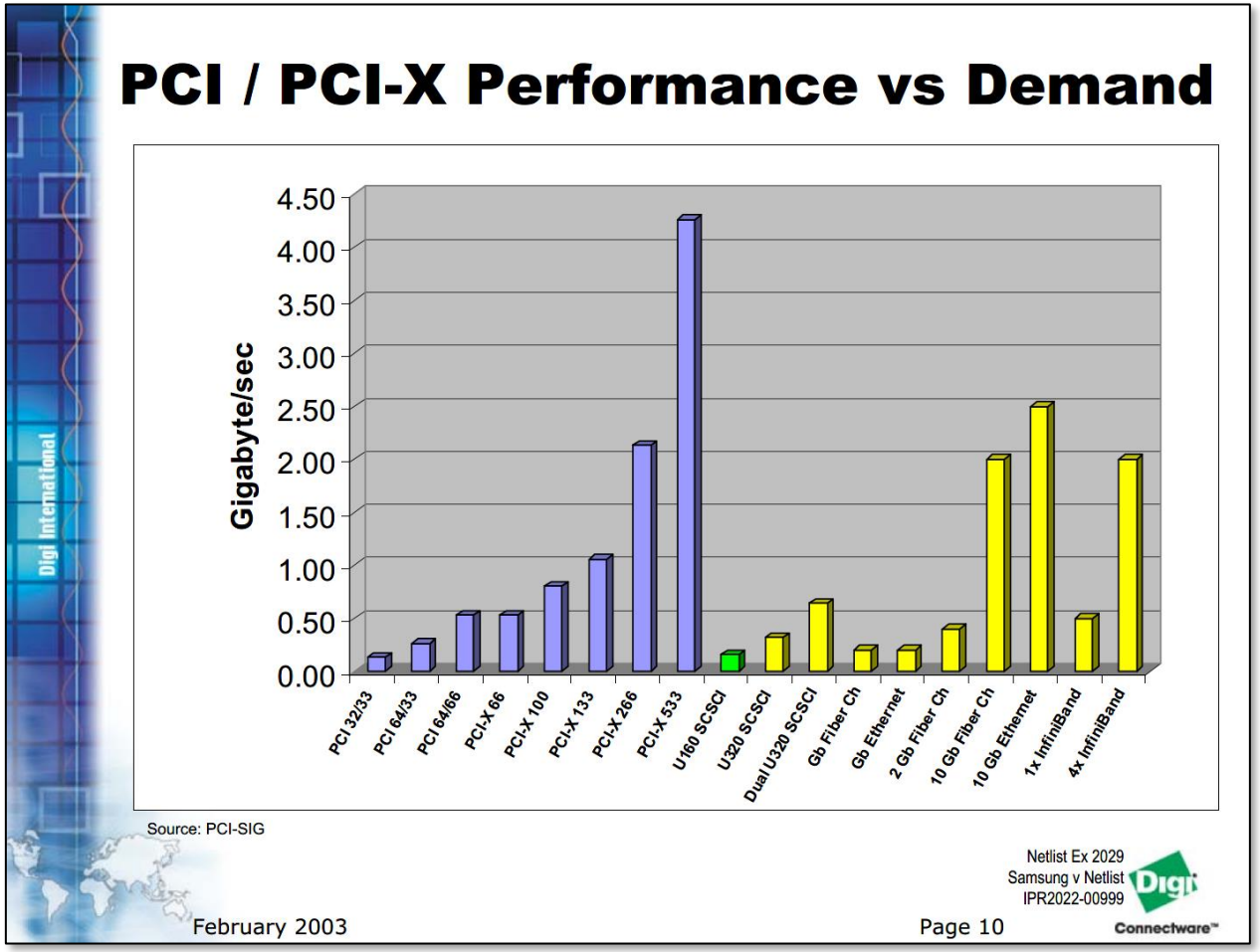
'918: Paper 25 (Reply) at 27-28
'054: Paper 26 (Reply) at 28-29

Netlist is wrong to suggest a PCI board like Spiers would not benefit from DDR2/DDR3, which is faster and more efficient

Q. And I gather the point of the graph on page 10 of Exhibit 2029 is that there are versions of PCI and PCI-X that have a throughput in gigabytes per second greater than Ethernet and SCSCI and something called InfiniBand; is that fair?

A. Yes. I think the purpose of this graph is to show that PCI-X could be used in systems that use any of those technologies without necessarily being a bottleneck and the limiting factor in system performance.

EX1075 59:13-23



EX2029, 10

'918: Paper 25 (Reply) at 28-29
'054: Paper 26 (Reply) at 29-30

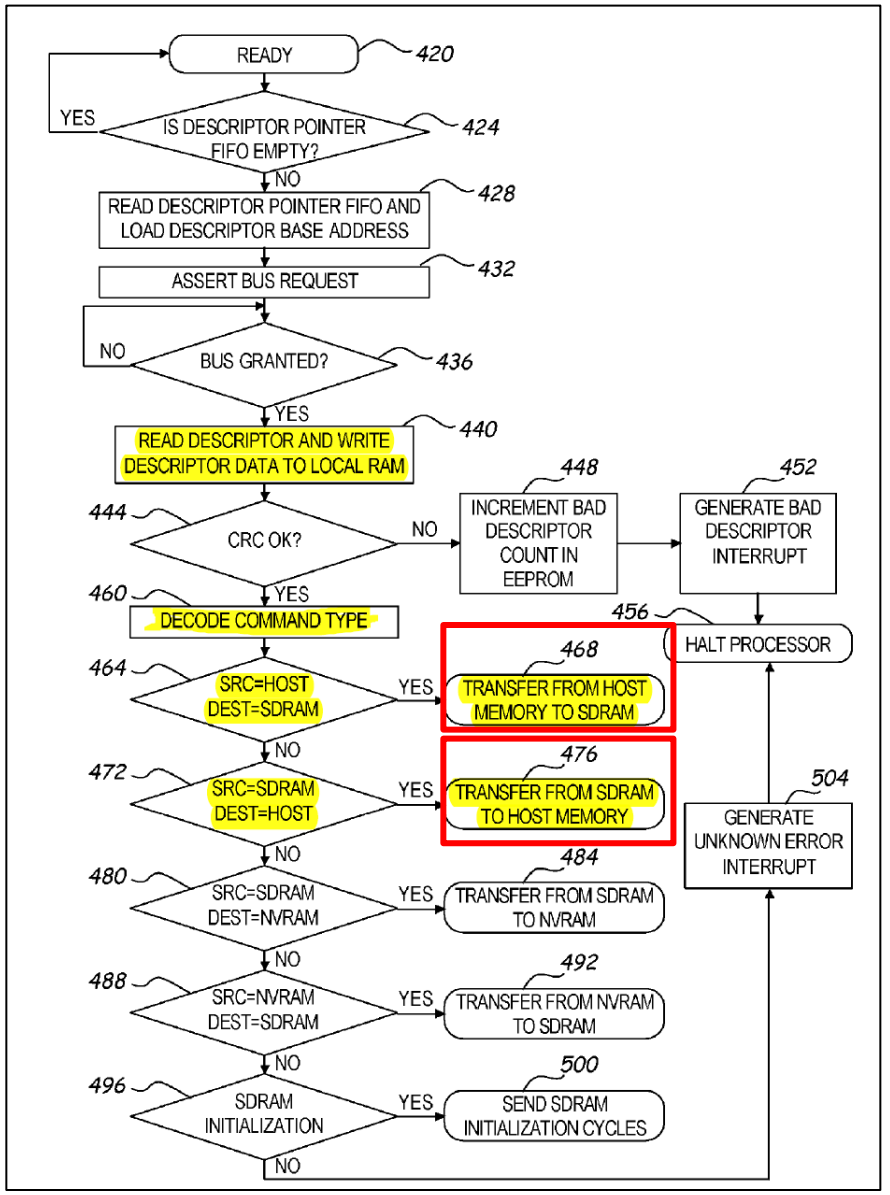
Spiers both reads and writes to DRAM

3.1.1. Command Definition

PCI bus command encodings and types are listed below, followed by a brief description of each. Note: The command encodings are as viewed on the bus where a "1" indicates a high voltage and "0" is a low voltage. Byte enables are asserted when "0".

C/BE[3::0]#	Command Type
0000	Interrupt Acknowledge
0001	Special Cycle
0010	I/O Read
0011	I/O Write
0100	Reserved
0101	Reserved
0110	Memory Read
0111	Memory Write
1000	Reserved
1001	Reserved
1010	Configuration Read
1011	Configuration Write
1100	Memory Read Multiple
1101	Dual Address Cycle
1110	Memory Read Line
1111	Memory Write and Invalidate

EX1031, 21



EX1025, Fig. 9

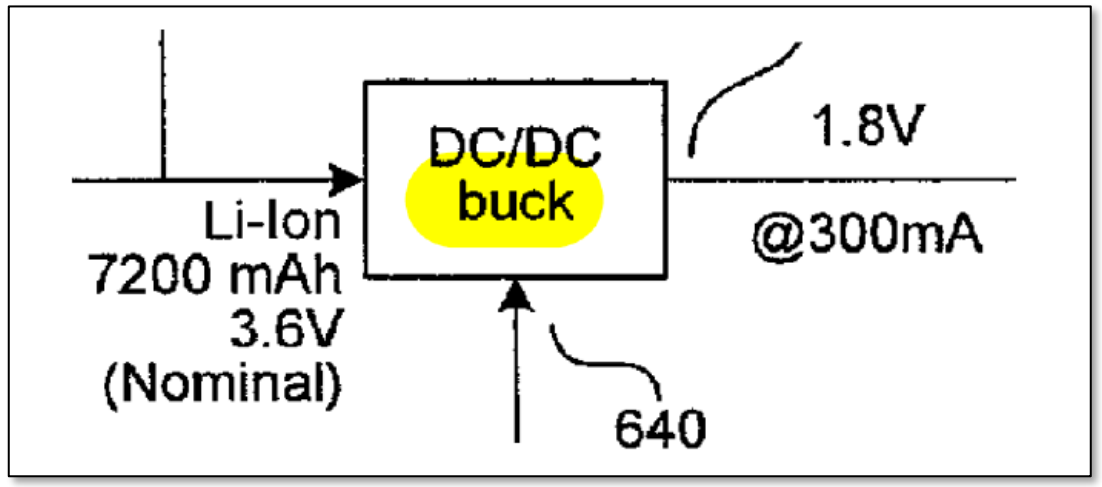
'918: Paper 1 (Petition) at 97-98
'054: Paper 1 (Petition) at 80-81

OBVIOUS TO USE THREE (‘054) OR FOUR (‘918) BUCK CONVERTERS

GROUND 4

(SPIERS + AMIDI)

The Institution Decisions correctly found that Grounds 4-5 render obvious using three or four buck converters



EX1024 (Amidi) at Fig. 6

Patent Owner further argues there are other ways to generate regulated voltages than providing a buck converter for each voltage level, and Petitioner did not show why one would not have pursued these other options. Prelim. Resp. 60-69. Petitioner did explain, however, that using a buck converter for each regulated voltage would "achieve high efficiency, reliability, and flexible power conversion." Pet. 90 (citing Pet. 29-31; Ex. 1025, Fig. 14; Ex. 1062, 11; Ex. 1003 ¶¶ 662-666).

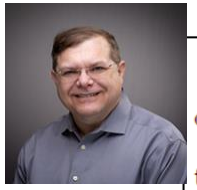
'918: ID at 50
See also '054: ID at 50 (similar)

Obvious to use buck converters to provide lower, regulated voltages

Q. All right. Would you agree that buck converters were known in the art by the time of the '918 and '054 patents?

A. Yes. For example, I was familiar with them at least as -- back in the 1996 time frame.

EX1075 (Mangione-Smith) at 104:23-105:2

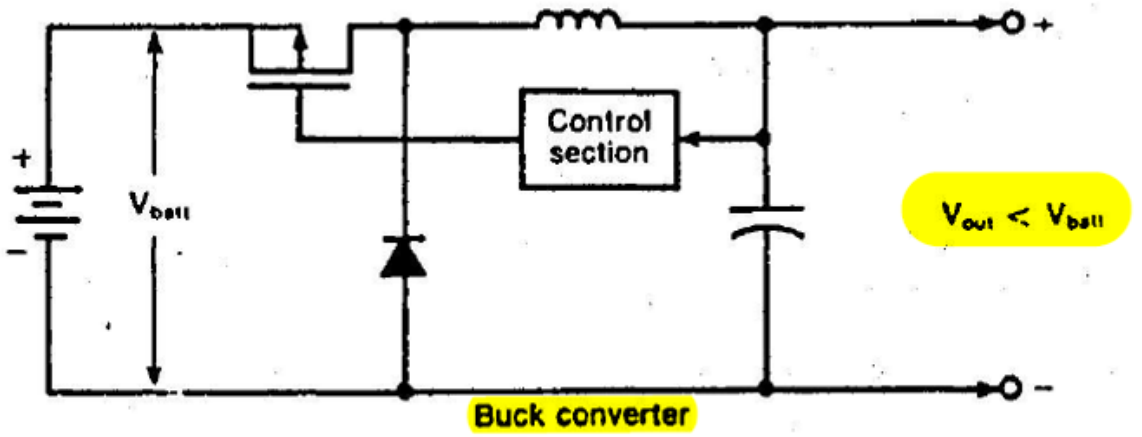


Q. And you did not provide any analysis on the cost of buck converters versus LDOs that can be used to generate the needed voltage rail; correct?

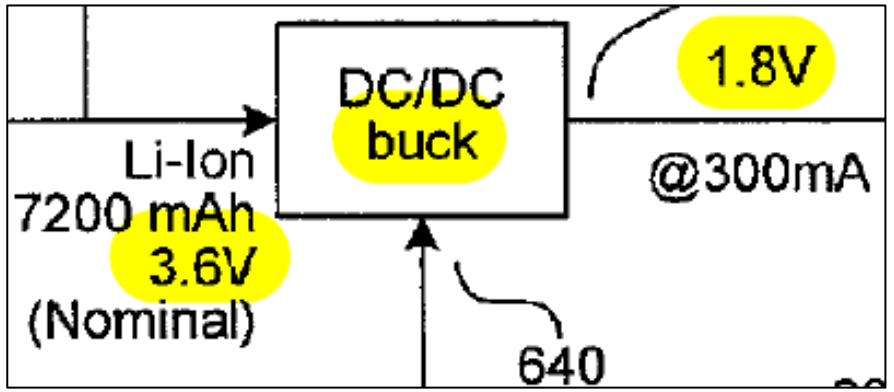
MR. CHANDLER: Object to form.

THE WITNESS: Not a specific comparison, other than to say that both are available at very low cost today and both would be feasible to provide SPD power, and that the trend over the years has been to move all computer power supplies to buck converters.

EX2030/EX2060 (Wolfe) at 140:15-24



EX1058 at p. 5 ; *see also* EX1075 (Mangione-Smith) at 103:21-111:17

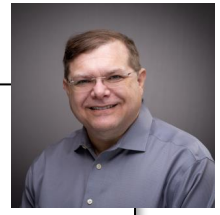


EX1024 (Amidi) at Fig. 6

'918: Paper 1 (Pet.) at 29-30 and 90-91; Paper 25 (Reply) at 10, 18 and 29-30

'054: Paper 1 (Pet.) at 29-30 and 85-86; Paper 26 (Reply) at 11, 19 and 30-31

Buck converters are highly efficient — unlike an LDO



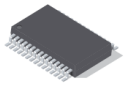
Q. And what was the efficiency of buck convertors at the time of the invention?

A. It varies from situation to situation. But typically, in the 80 to 98 percent range.

EX2030/EX2060 at 57:4-20

TEXAS INSTRUMENTS

TPS51020



SLUS564B – JULY 2003 – REVISED DECEMBER 2003

DUAL, VOLTAGE MODE, DDR SELECTABLE, SYNCHRONOUS, STEP-DOWN CONTROLLER FOR NOTEBOOK SYSTEM POWER

EX1041 at 1

The TPS51020 is a multi-function dual-synchronous step-down controller for notebook system power. The part is specifically designed for high performance, high efficiency applications where the loss associated with a current sense resistor is unacceptable. The TPS51020 utilizes feed forward voltage mode control to attain high efficiency without sacrificing line response. Efficiency at light load conditions can be maintained high as well by incorporating autoskip operation. A selectable, Suspend to RAM (STR)

Q. And what were some of the trade-offs that were known at the time between using a buck converter and an LDO linear regulator?

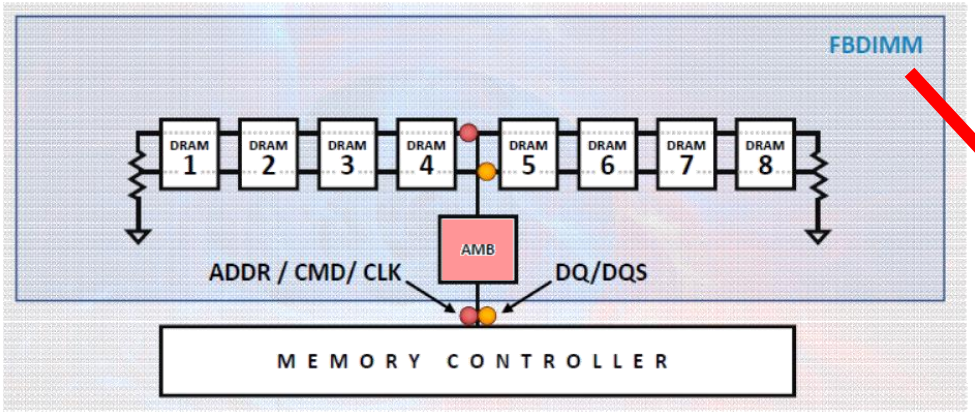
A. Well, in general, a buck converter might achieve what's referred to as higher efficiency, which is to say, all of these voltage regulators, voltage converters that we're talking about have some amount of electrical power that goes in, and a smaller amount of electrical power that's made available on the output. There's always entropy. There's always loss.

So in general, the -- it's understood that something like a switch regulator will have better efficiency than LDOs generally. On the

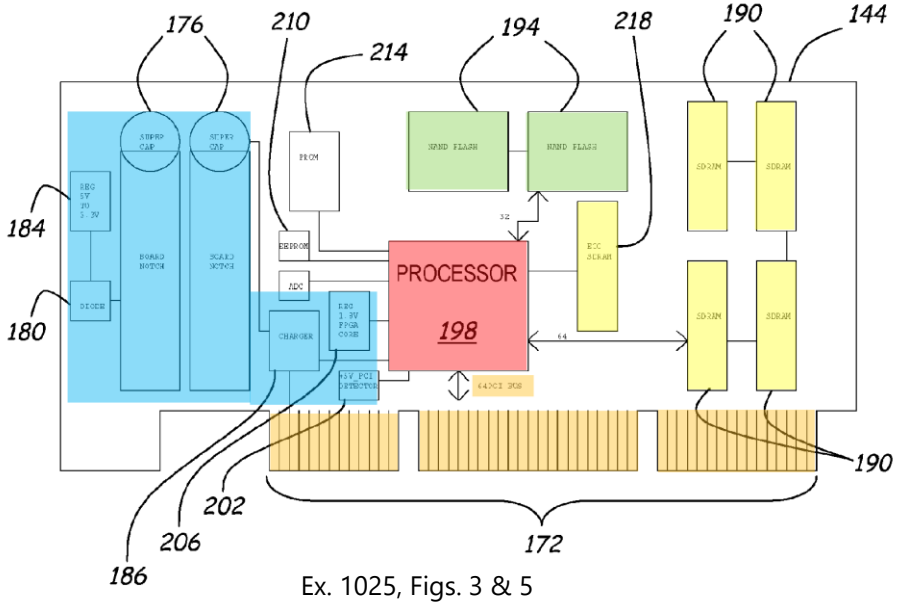
EX1075 at 112:12-25

'918: Paper 25 (Reply) at 17 and 29-30
'054: Paper 26 (Reply) at 19 and 30-31

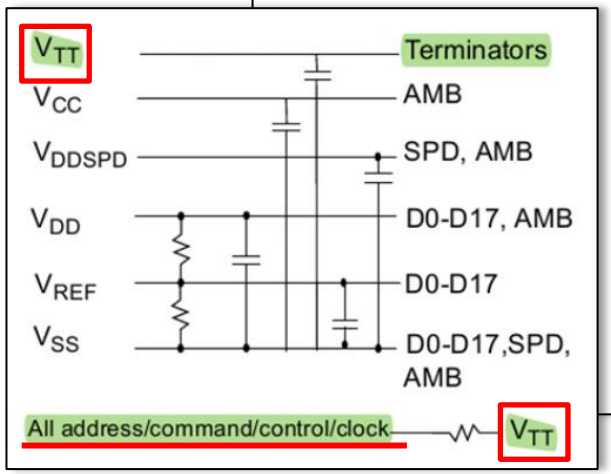
1. Obvious to use buck converter for V_{TT}, which Spiers needs to terminate address and control signals (like an FBDIMM)



EX1077, 9; EX1075 (Mangione-Smith), 97:16- 98:18



Ex. 1025, Figs. 3 & 5



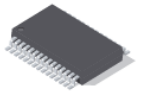
EX1028, 15 & 68

'918: Paper 1 (Pet.) at 87-88; Paper 25 (Reply) at 15-16, 29-30
'054: Paper 1 (Pet.) at 83; Paper 26 (Reply) at 16-17, 30-31

1. Obvious to use buck converter for V_{TT}, which Spiers needs to terminate address and control signals (like an FBDIMM)

TEXAS INSTRUMENTS

TPS51020



SLUS564B – JULY 2003 – REVISED DECEMBER 2003

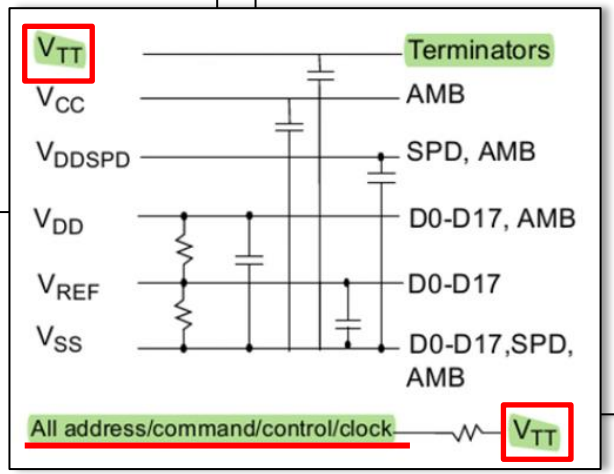
DUAL, VOLTAGE MODE, DDR SELECTABLE, SYNCHRONOUS, STEP-DOWN CONTROLLER FOR NOTEBOOK SYSTEM POWER

APPLICATIONS

- Notebook Computers System Bus and I/O
- DDR I or DDR II Termination

supported, DDR option provides a one chip solution for all switching applications from 5-V/3.3-V supply to a complete DDR termination solution.

Ex. 1040 at 1



EX1028, 15 & 68

FAIRCHILD SEMICONDUCTOR®

October 2005

FAN5026
Dual DDR/Dual-Output PWM Controller

- Complete DDR Memory power solution
  - VTT Tracks VDDQ/2

Applications

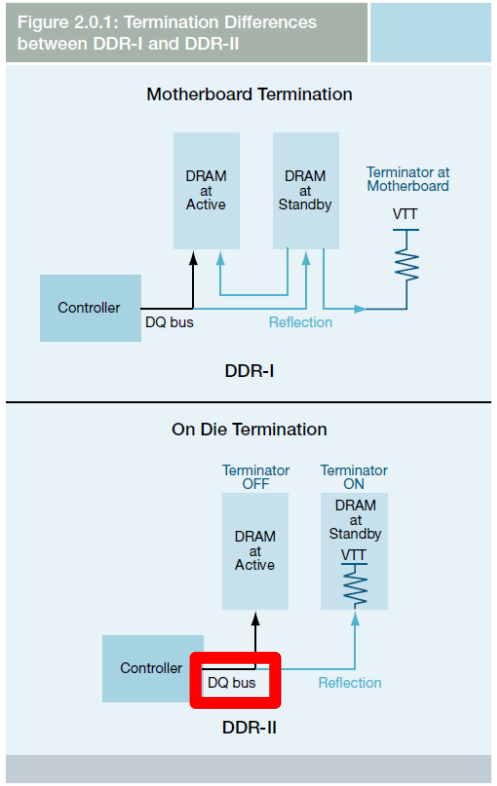
- DDR V_{DDQ} and V_{TT} voltage generation

Ex. 1041 at 1

'918: Paper 1 (Pet.) at 87-88; Paper 25 (Reply) at 15-16, 29-30
'054: Paper 1 (Pet.) at 83; Paper 26 (Reply) at 16-17, 30-31

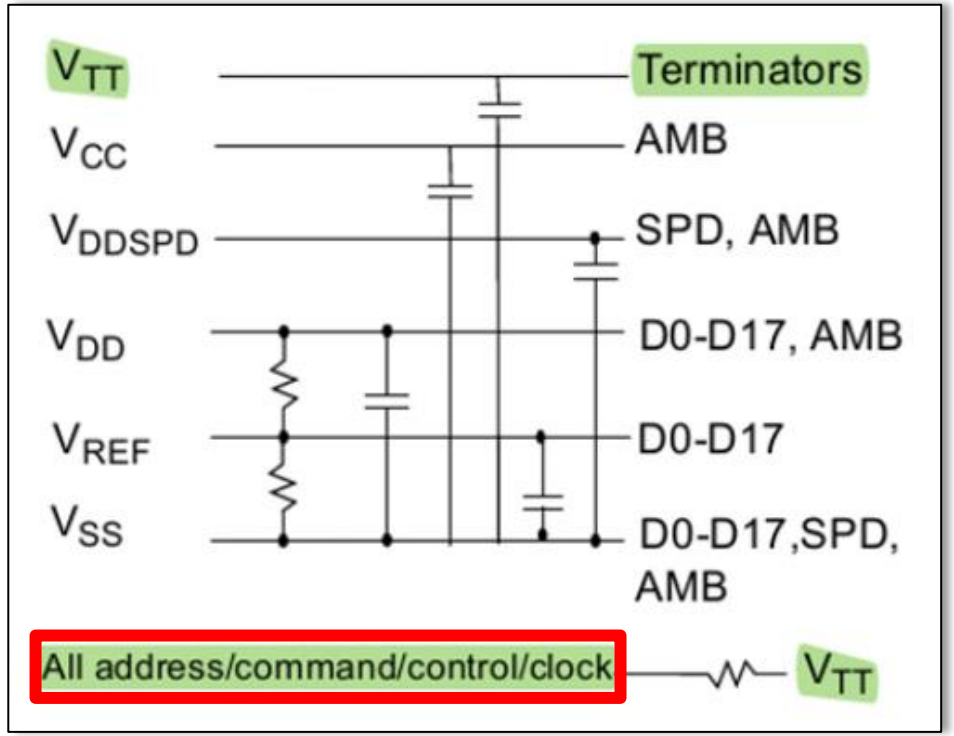
1. Obvious to use buck converter for V_{TT}, which Spiers needs to terminate address and control signals (like an FBDIMM)

Netlist argues DDR2 does not need V_{TT} for data (DQ) signals…



EX2012, 71

… but DDR2 still uses V_{TT} for address/control signals



EX1028, 15

'918: Paper 1 (Pet.) at 87-88; Paper 25 (Reply) at 15-16, 29-30
'054: Paper 1 (Pet.) at 83; Paper 26 (Reply) at 16-17, 30-31

2. Multiple 1.8 V converters for V_{CCFPGA} and V_{DD}/V_{DDQ} was obvious (e.g., for DDR2)

EX2030/EX2060 at 53:16-25

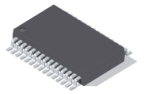
Q. Okay. And but it was well known at the time of the invention that you can have a single-voltage converter to generate two different voltage levels; correct?

MR. CHANDLER: Objection. Form.

THE WITNESS: It was possible under some circumstances, but certainly not the most common thing to do. Normally, if you need to generate multiple output voltages, you would use multiple regulators, especially in a high-current situation

TEXAS INSTRUMENTS

TPS51020



SLUS564B – JULY 2003 – REVISED DECEMBER 2003

DUAL, VOLTAGE MODE, DDR SELECTABLE, SYNCHRONOUS, STEP-DOWN CONTROLLER FOR NOTEBOOK SYSTEM POWER

supported, DDR option provides a one chip solution for all switching applications from 5-V/3.3-V supply to a complete DDR termination solution.

Ex. 1040 at 1

Power Supply Reference Guide for XILINX® FPGAs

	Spartan™-3/3E/3L	Spartan™-IIE	Spartan™-II	Virtex™-5	Virtex™-4	Virtex-II Pro™	Virtex™-II
V_{CCINT}	1.2V @0.2A-5A	1.8V @0.2A-1.5A	2.5V @0.2A-1A	1.0V @0.2A-15A	1.2V @0.2A-20A	1.5V @0.2A-20A	1.5V @0.2A-20A
V_{CCO}	1.2V-3.3V @50mA-3A	1.5V-3.3V @50mA-0.5A	1.5V-3.3V @50mA-0.5A	1.2V-3.3V @50mA-5A	1.2V-3.3V @50mA-3A	1.5V-3.3V @50mA-3A	1.5V-3.3V @50mA-3A
V_{CCAUX}	2.5V @50mA-0.3A	–	–	2.5V @50mA-0.7A	2.5V @50mA-0.7A	2.5V @50mA-0.3A	3.3V @50mA-0.3A

EX1042 at 1-2

'918: Paper 1 (Pet.) at 78-81 and 86-91; Paper 25 (Reply) at 30
'054: Paper 1 (Pet.) at 72-77 and 81-88; Paper 26 (Reply) at 31

3. Multiple converters for 1.5 V (e.g., for DDR3 V_{DD}/V_{DDQ}) and 1.8 V (e.g., for V_{CCFPGA}) was obvious

EX2030/EX2060 at 53:16-25

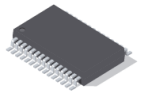
Q. Okay. And but it was well known at the time of the invention that you can have a single-voltage converter to generate two different voltage levels; correct?

MR. CHANDLER: Objection. Form.

THE WITNESS: It was possible under some circumstances, but certainly not the most common thing to do. Normally, if you need to generate multiple output voltages, you would use multiple regulators, especially in a high-current situation

TEXAS INSTRUMENTS

TPS51020



SLUS564B – JULY 2003 – REVISED DECEMBER 2003

DUAL, VOLTAGE MODE, DDR SELECTABLE, SYNCHRONOUS, STEP-DOWN CONTROLLER FOR NOTEBOOK SYSTEM POWER

supported, DDR option provides a one chip solution for all switching applications from 5-V/3.3-V supply to a complete DDR termination solution.

Ex. 1040 at 1

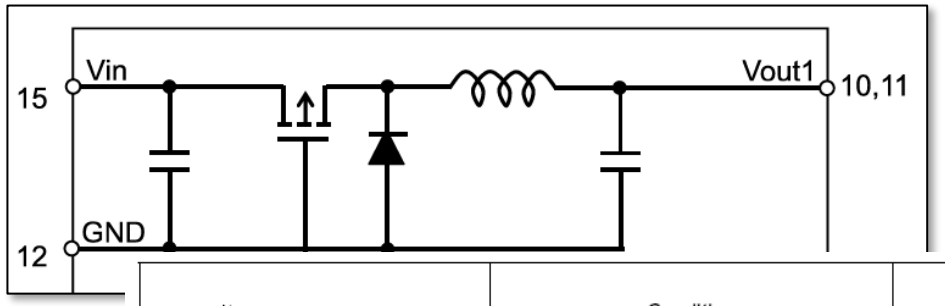
Power Supply Reference Guide for XILINX® FPGAs

	Spartan™-3/3E/3L	Spartan™-IIE	Spartan™-II	Virtex™-5	Virtex™-4	Virtex-II Pro™	Virtex™-II
V_{CCINT}	1.2V @0.2A-5A	1.8V @0.2A-1.5A	2.5V @0.2A-1A	1.0V @0.2A-15A	1.2V @0.2A-20A	1.5V @0.2A-20A	1.5V @0.2A-20A
V_{CCO}	1.2V-3.3V @50mA-3A	1.5V-3.3V @50mA-0.5A	1.5V-3.3V @50mA-0.5A	1.2V-3.3V @50mA-5A	1.2V-3.3V @50mA-3A	1.5V-3.3V @50mA-3A	1.5V-3.3V @50mA-3A
V_{CCAUX}	2.5V @50mA-0.3A	–	–	2.5V @50mA-0.7A	2.5V @50mA-0.7A	2.5V @50mA-0.3A	3.3V @50mA-0.3A

EX1042 at 1-2

'918: Paper 1 (Pet.) at 78-81 and 86-91; Paper 25 (Reply) at 30
'054: Paper 1 (Pet.) at 72-77 and 81-88; Paper 26 (Reply) at 31

4. Obvious to use buck converter for 5 V-to-3.3 V regulator



EX1048 at 2-3

Item	Symbol	Condition	Value Min.	Value Typ.	Value Max.	Unit
Input Voltage	Vin		4.5	12	13.2	V
Output Voltage Adjustable Range	Vout1	Vin=4.5-13.2V (Vin-Vo>1V)	1.0		3.3	V
	Vout2		1.8		3.6	
Load Current	Iout1	Vout1=1.0-1.8V	0	-	1.3	A
		Vout1=1.81-3.3V	0	-	1.1	
	Iout2 +Iout3	Current sum of Iout2 and Iout3 (*2)	0	-	1.0	
	Iout3	Vout2≧3.05V	0	-	0.3	
		3.05V>Vout2≧2.95V	0	-	0.25	
		2.95V>Vout2≧2.85V	0	-	0.20	

Q. And you did not provide any analysis on the cost of buck converters versus LDOs that can be used to generate the needed voltage rail; correct?

MR. CHANDLER: Object to form.

THE WITNESS: Not a specific comparison, other than to say that both are available at very low cost today and both would be feasible to provide SPD power, and that the trend over the years has been to move all computer power supplies to buck converters.

EX2030/EX2060 (Wolfe) at 140:15-24

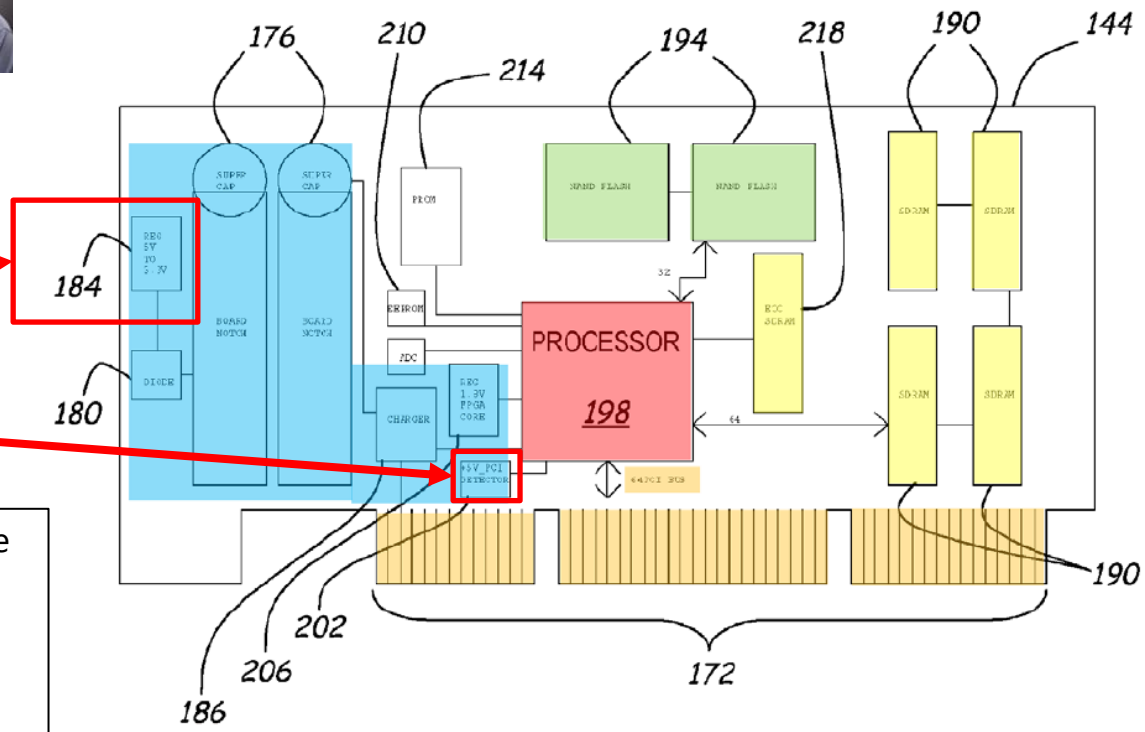
'918: Paper 25 (Reply) at 31-33
'054: Paper 26 (Reply) at 32-34

4. Obvious to use buck converter for 5 V-to-3.3 V regulator

Q. And as a designer, when would you use the 3.3 volt supply voltage that's provided directly from the connector, and when would you use a 3.3 volt coming from the regulator 184?

A. Again, you don't need to use the 3.3 volt from the bus ever. You can use the 5 volt from the bus and regulate that down to 3.3 in there, but you also could use the 3.3 volt from the PCI bus when the power supply is good, and use the 3.3 volts from 184 when the power supply fails.

The indication here is that you're always using 184 because what's being monitored is the 5 volt supply, not the 3.3 volt supply, and the 5 volt supply feeds into 184. It would not be a great idea to rely on the 3.3 volts from the bus and not monitor it..



Q. So "coupled" just means that as long as the wiring is in existence between the voltage rail and the component? [...]

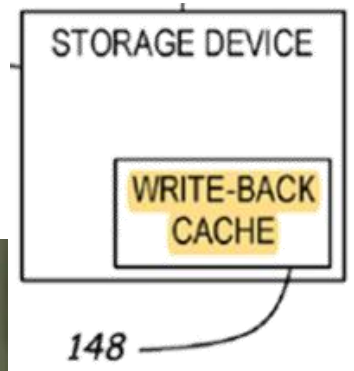
[A]: Again, that's a complex issue that the courts struggle with and this court would have to decide, but I think that that's the approach -- that's one of the approaches that I would use.

As I said, my actual opinion is that it would be obvious to use the same 3.3 regulator all the time, in which case it would clearly be coupled under I think any construction that's reasonable.

EX2030/EX2060 (Wolfe) at 149:11-150:1 and 278:17-281:17;
see also id. 154:22-156:15, 156:23-157:8, 278:5-:15, and 282:7-:14

'918: Paper 25 (Reply) at 31-33
'054: Paper 26 (Reply) at 32-34

Netlist's calculation about using an LDO for the write-back cache is flawed and irrelevant



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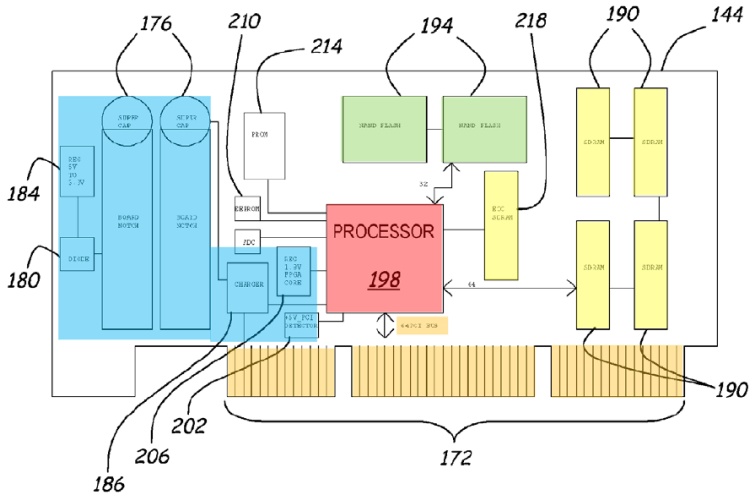


Q. And so Figure 5 in Spiers is separate from the write-back cache 148 in Figure 3; is that accurate?

A. Yes, that's accurate.

EX1075 at 208:23-209:1

"[I]t's not necessary to show that a combination is the *best* option, only that it be a ***suitable*** option."

Intel Corp. v. PACT XPP Schweiz AG, 61 F.4th 1373, 1380-81 (Fed. Cir. 2023) (reversing Board)

'918: Paper 25 (Reply) at 31-32
'054: Paper 26 (Reply) at 32-33

"PRE-REGULATED" VOLTAGES ('918 CLAIMS 16-22 & 30) ('054 CLAIMS 18-22, 26-28)

GROUND 4

(SPIERS + AMIDI)

The District Court adopted a broad construction of "*pre-regulated*" voltages (consistent with the Institution Decision)

Samsung contends the claims require the "pre-regulated voltage" to be regulated by the memory module rather than the host system to which it connects. . . .Notably, the disputed term is a small part of the "buck converter" limitations and gives context to what the buck converters do – that is, receive an input voltage and produce an output voltage. And although the claims characterize the ***input*** voltage into the buck converters as ***"pre-regulated"*** and the output voltages as "regulated," they impose ***no further limitations*** on the buck converters or, for that matter, the memory module. Although the written description discloses such structure (e.g., first and second power elements 1130, 1140), the claims do not require it. Instead, they only require what the buck converters receive, not what the other elements of the memory module provides. Accordingly, the Court rejects Samsung's proposed construction. The term will otherwise be given its plain and ordinary meaning.

EX2032 (Claim Construction Order) at 21-22

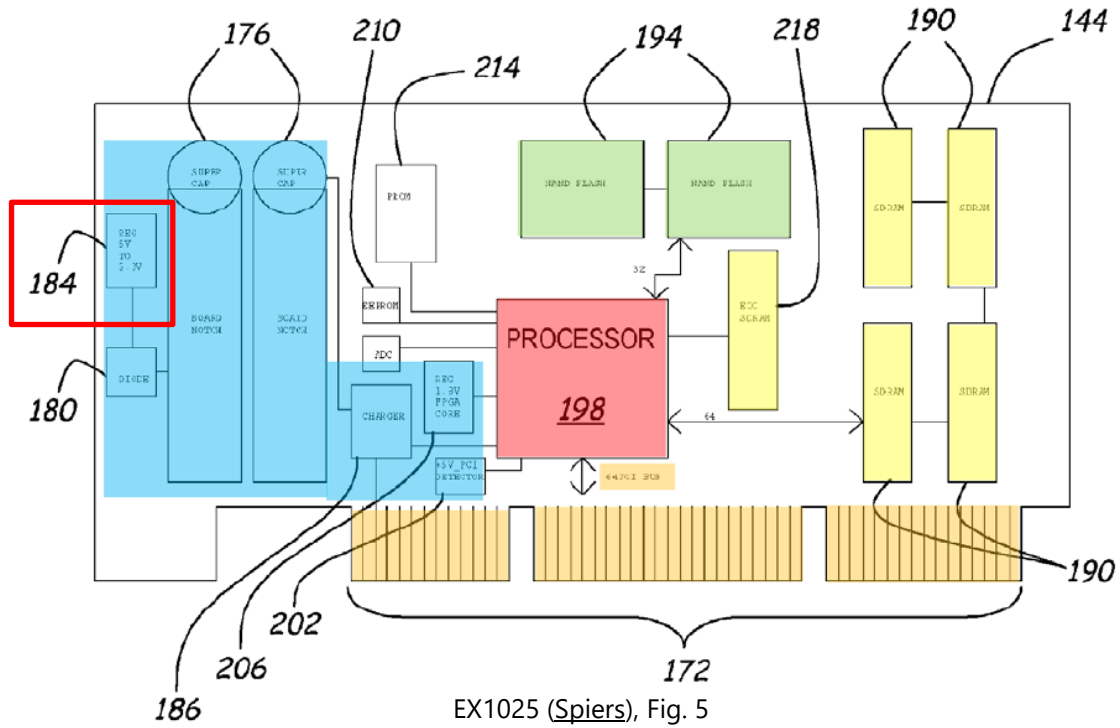
For purposes of this decision, we interpret "pre-regulated voltage" to mean that the voltage is ***regulated before conversion*** to a stepped up or down level. *See* Ex. 1001, code (57), 28:53-58, Fig. 16 (1110, 1112). Patent Owner further argues that Amidi does not disclose a "pre-regulated voltage" but offers no interpretation for the term. Prelim. Resp. 39-40. We invite development of the record at trial to explain the meaning of "pre-regulated voltage." In any case, we find Petitioner's showing of obviousness with respect to these claims sufficient for institution.

'918: ID at 38 (emphasis added)
See also '054: ID at 39 (similar)

Obvious to use pre-regulated input voltage with Spiers

4. Grounds 4-5 disclose pre-regulated input voltage (POR 69-71)

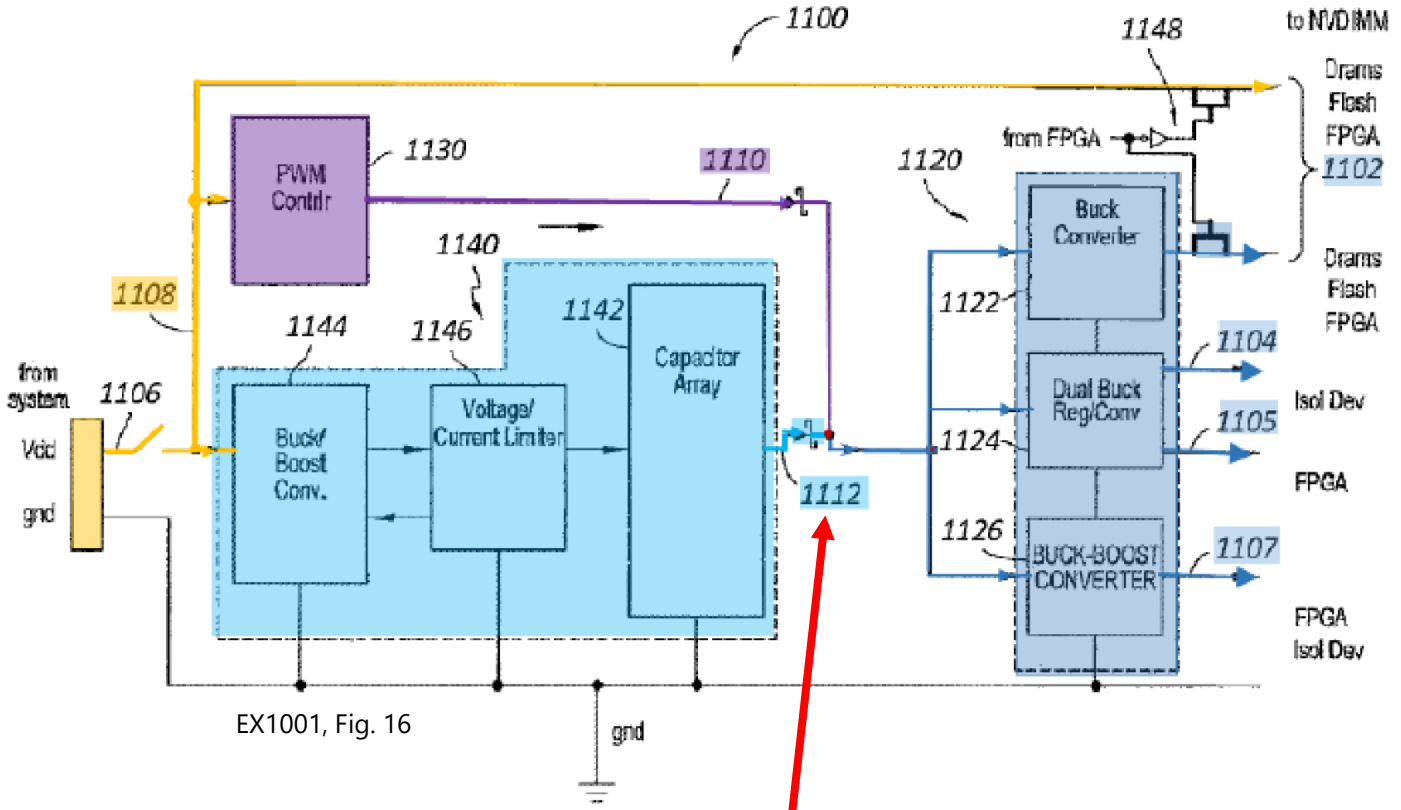
The Petition correctly identifies a "*pre-regulated input voltage*"[5] to each converter. Pet. 126-27. Netlist argues that "the 5V system voltage is not directly received by the 5V-to-3.3V regulator 184," POR 69, but that ignores the 918 Patent's implementation of indirect connection to the input voltage shown below (pp.34-35), and is incorrect as discussed above (p.31, note 4). Furthermore, as Dr. Wolfe explained, the on-board 3.3V can be generated by "another, similar voltage converter" during normal operation. EX1003, ¶¶691, 695.



EX1025 (Spiers), Fig. 5

'918: Paper 1 (Pet.) at 126-27; Paper 25 (Reply) at 10 and 33
'054: Paper 1 (Pet.) at 118-20; Paper 26 (Reply) at 36

054 claims: Obvious to select from two pre-regulated voltages (e.g., "first" during normal operation, and "second" during backup power)



EX1001, Fig. 16

In the Figure 16 embodiment, examples of **pre-regulated** input voltages are voltages 1110/1112 (output from power elements 1130/1140)

'918: Paper 31 (Sur-Reply) at 32

054 claims: Obvious to select from two pre-regulated voltages (e.g., "first" during normal operation, and "second" during backup power)

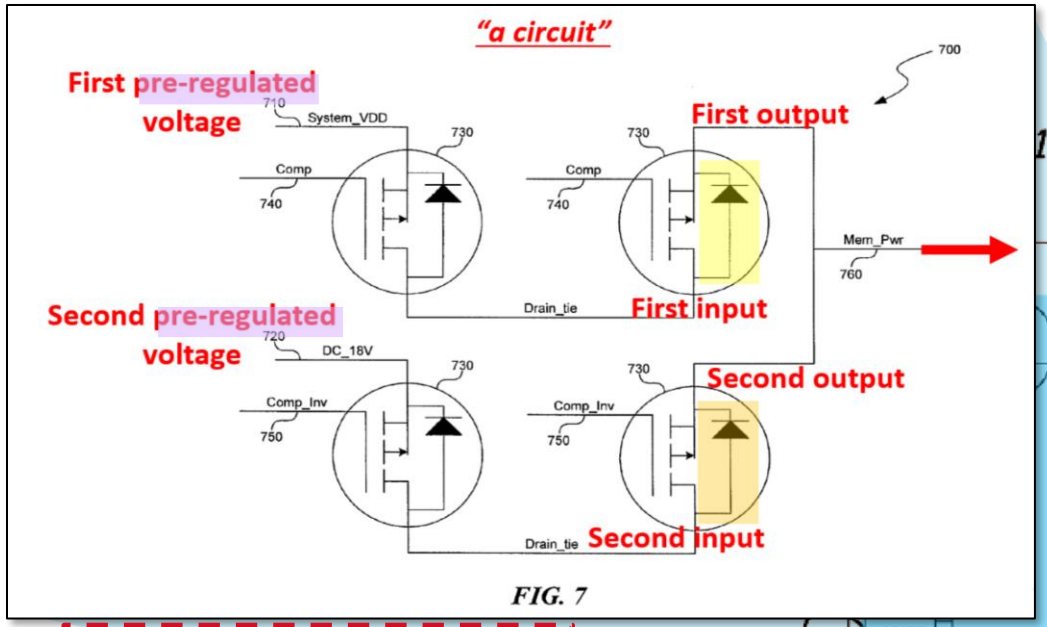
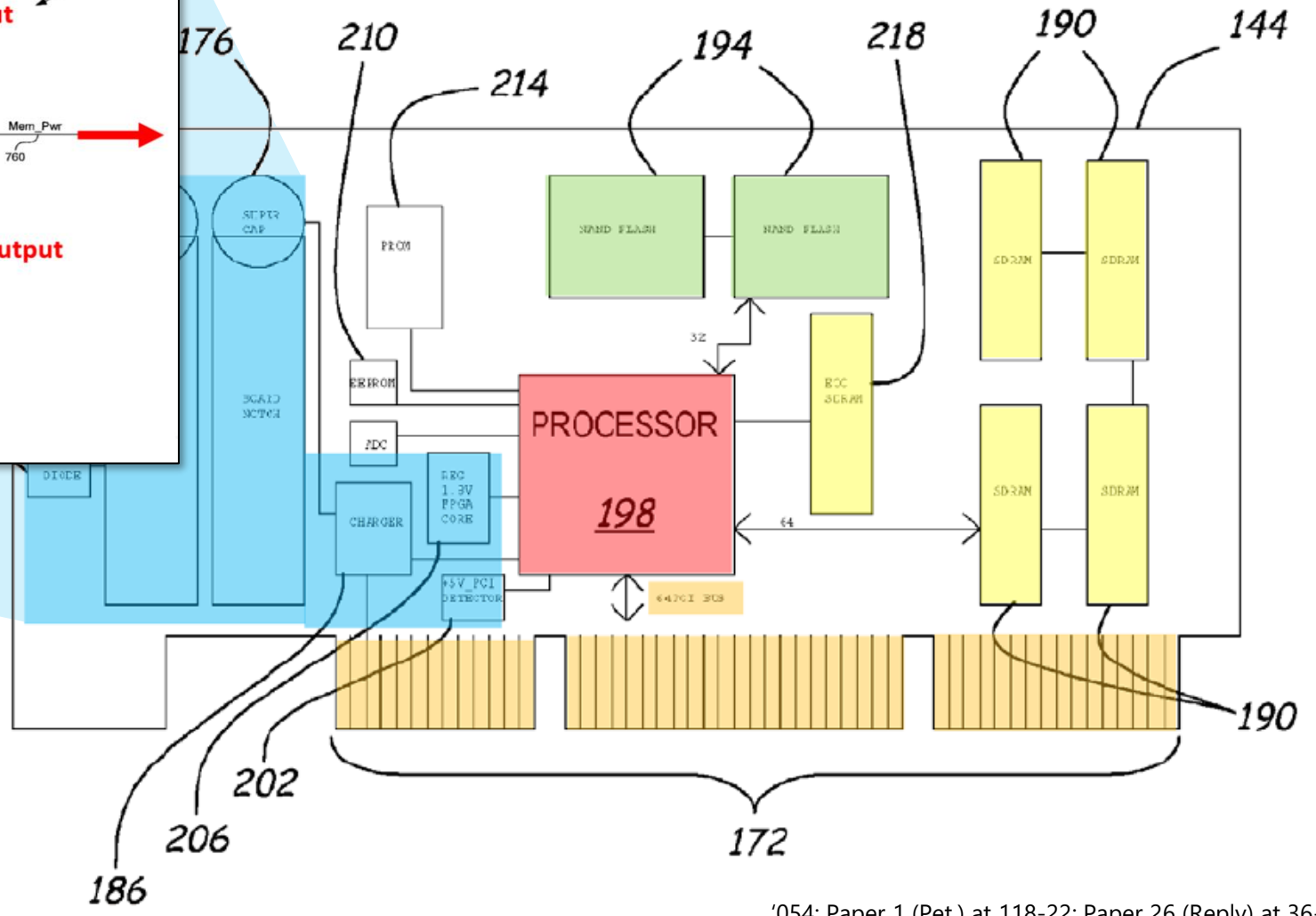


FIG. 7



054 Mappings

Voltage Mapping (A) for DDR3

1st : V_{DD}/V_{DDQ} to DRAM/FPGA = 1.5V
2nd : V_{CCFPGA} to FPGA Core = 1.8V
3rd : (i) V_{TT} to DRAM Bus = 0.75V
(ii) V_{CC} to NV Memory = 3.3V
(iii) V_{CCO} to FPGA I/O = 3.3V

Voltage Mapping (B) for DDR2

1st : V_{DD}/V_{DDQ} to DRAM/FPGA = 1.8V
2nd : V_{CCFPGA} to FPGA Core = 1.8V
3rd : (i) V_{TT} to DRAM Bus = 0.9V
(ii) V_{CC} to NV Memory = 3.3V
(iii) V_{CCO} to FPGA I/O = 3.3V
(iv) V_{DDL} to DRAM = 1.8V

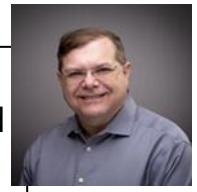
'054: Paper 1 (Pet.) at 118-22; Paper 26 (Reply) at 36-37

POWER INPUT VOLTAGE COUPLED TO CONVERTERS ('918 CLAIM 13)

GROUND 4

(SPIERS + AMIDI)

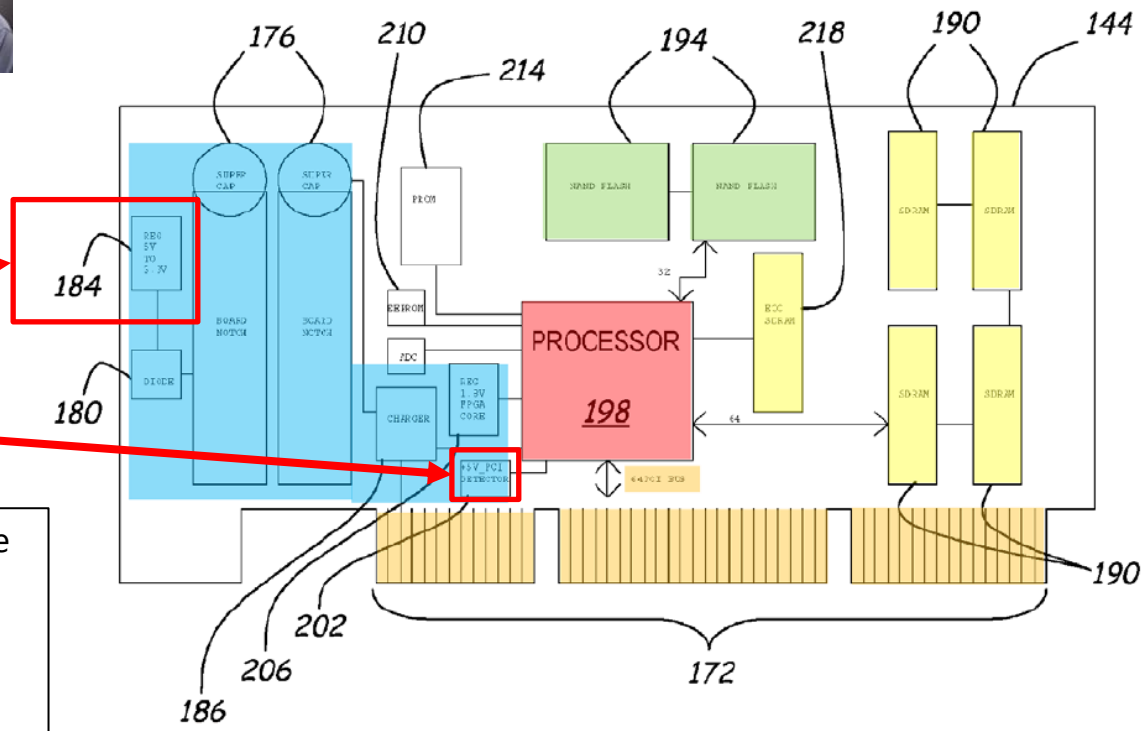
Input voltage would always be provided to buck converters



Q. And as a designer, when would you use the 3.3 volt supply voltage that's provided directly from the connector, and when would you use a 3.3 volt coming from the regulator 184?

A. Again, you don't need to use the 3.3 volt from the bus ever. You can use the 5 volt from the bus and regulate that down to 3.3 in there, but you also could use the 3.3 volt from the PCI bus when the power supply is good, and use the 3.3 volts from 184 when the power supply fails.

The indication here is that you're always using 184 because what's being monitored is the 5 volt supply, not the 3.3 volt supply, and the 5 volt supply feeds into 184. It would not be a great idea to rely on the 3.3 volts from the bus and not monitor it..



Q. So "coupled" just means that as long as the wiring is in existence between the voltage rail and the component? [...]

[A]: Again, that's a complex issue that the courts struggle with and this court would have to decide, but I think that that's the approach -- that's one of the approaches that I would use.

As I said, my actual opinion is that it would be obvious to use the same 3.3 regulator all the time, in which case it would clearly be coupled under I think any construction that's reasonable.

EX2030/EX2060 (Wolfe) at 149:11-150:1 and 278:17-281:17;
see also id. 154:22-156:15, 156:23-157:8, 278:5-:15, and 282:7-:14

'918: Paper 25 (Reply) at 31-33
'054: Paper 26 (Reply) at 32-34

"Coupled to" does not require direct connection

Q. So "coupled" just means that as long as the wiring is in existence between the voltage rail and the component? [...]

[A]: Again, that's a complex issue that the courts struggle with and this court would have to decide, but I think that that's the approach -- that's one of the approaches that I would use.

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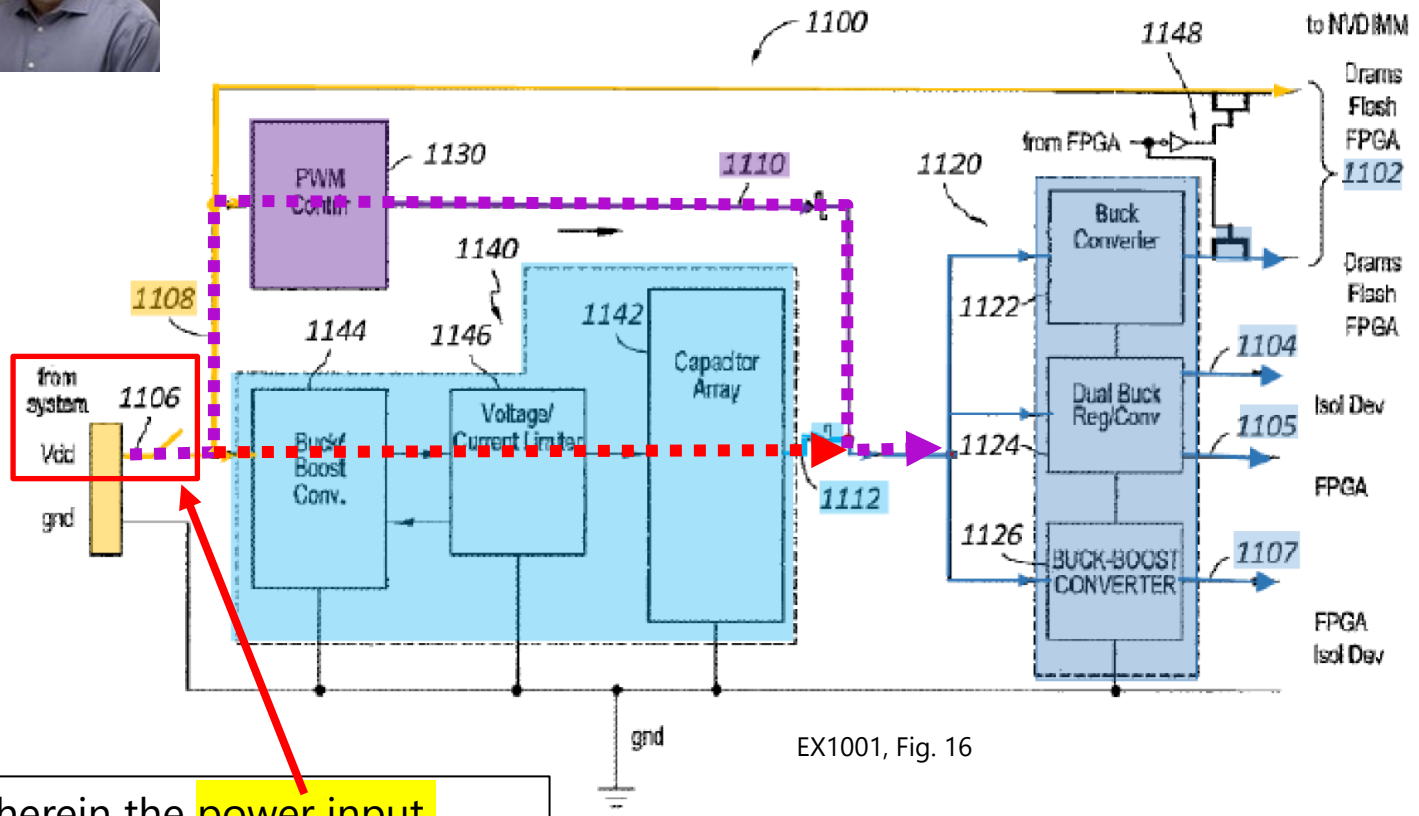
EX2030/EX2060 (Wolfe) at 278:17-281:17;



EX1001, Fig. 16

13. The memory module of claim 5, wherein the power input voltage is coupled to the first, second, and third buck converters and the converter circuit.

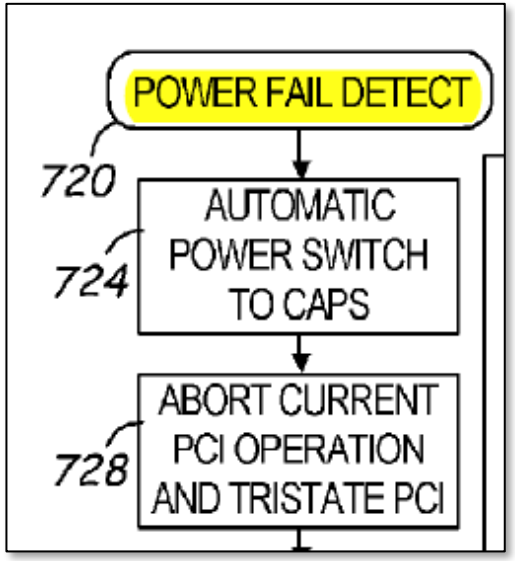
'918: Paper 1 (Pet.) at 126-27; Paper 25 (Reply) at 10 and 33, 35
'054: Paper 1 (Pet.) at 118-20; Paper 26 (Reply) at 36

OVER-VOLTAGE PROTECTION ('918 CLAIMS 5-7, 9-13, 16-22, 24-27) ('054 CLAIMS 6-7, 9-12, 17)

GROUND 4 & 5

(SPIERS + AMIDI + HAJECK)

Obvious to detect over-voltage as well as under-voltage



EX1025 (Spiers), Fig. 14 & [0002], [0030]

[0002] Data storage systems are used in numerous applications and have widely varying complexity related to the application storing the data, the amount of data required to be stored, and numerous other factors. A common requirement is that the data storage system securely store data, meaning that stored data will not be lost in the event of a power loss or other failure of the storage system. In fact, many applications store data at primary data storage systems and this data is then backed-up, or archived, at predetermined time intervals in order to provide additional levels of data security.

nected to the bus 128. In the embodiment of **FIG. 2**, the NAS device **108** includes one backup device **144**, having a non-volatile memory, in which the storage controller **132** causes a copy of data to be stored at storage devices **140** to be provided to the backup device **144** in order to help prevent data loss in the event of a power interruption or other failure within the NAS device **108**. In other embodiments, more than one backup device **144** may be utilized in the NAS device **108**.

Q. Okay. And when -- in a PCI card -- let me withdraw and ask.

In Spiers, does Spiers detect when a voltage is above the 5 volt threshold?

A. It simply tells us that there's a 5 volt PCI detector, and then it says that that responds to power failures, but it doesn't define specifically what it means by a power failure.

Q. And what is a POSITA's understanding of the term "power failure"?

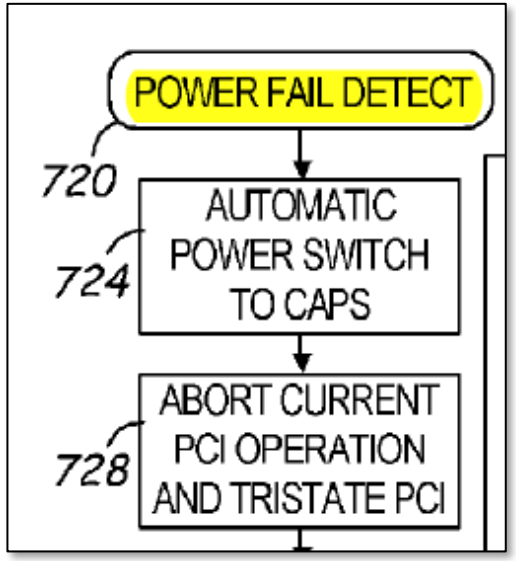
A. It could be -- I mean, the actual language here is "power failure, power interruption or other failure."

So I think in that context, you would read it to be broader than a power interruption. So it would presumably mean any failure to maintain the proper voltage levels or the proper current levels.

EX2030/EX2060 at 259:3-17

'918: Paper 1 (Pet.) at 104-05; Paper 25 (Reply) at 35-36
'054: Paper 1 (Pet.) at 107-08; Paper 26 (Reply) at 34-35

Obvious to detect over-voltage as well as under-voltage



EX1025 (Spiers), Fig. 14 & [0002], [0030]

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National Semiconductor

LMC6953

PCI Local Bus Power Supervisor

DC Electrical Characteristics

Unless otherwise specified, all **boldface** limits guaranteed for T_J = 0°C to 70°C, V_{DD} = 5V, $R_{PULL-UP}$ = 4.7 kΩ and C_{EXT} = 0.01 µF. Typical numbers are room temperature (25°C) performance.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{H5}	V_{DD} Over-Voltage Threshold	(Note 4)	**5.45**	5.6	**5.75**	V
V_{L5}	V_{DD} Under-Voltage Threshold	(Note 4)	**4.25**	4.4	**4.55**	V
$V_{H3.3}$	3.3V Over-Voltage Threshold	(Note 5)	**3.8**	3.95	**4.1**	V
$V_{L3.3}$	3.3V Under-Voltage Threshold	(Note 5)	**2.5**	2.65	**2.8**	V

EX1063, 1-2

'918: Paper 1 (Pet.) at 104-05; Paper 25 (Reply) at 35-36
'054: Paper 1 (Pet.) at 107-08; Paper 26 (Reply) at 34-35

Obvious to detect over-voltage as well as under-voltage

Q. So in the overvoltage situation, how does the charge pump operate differently?

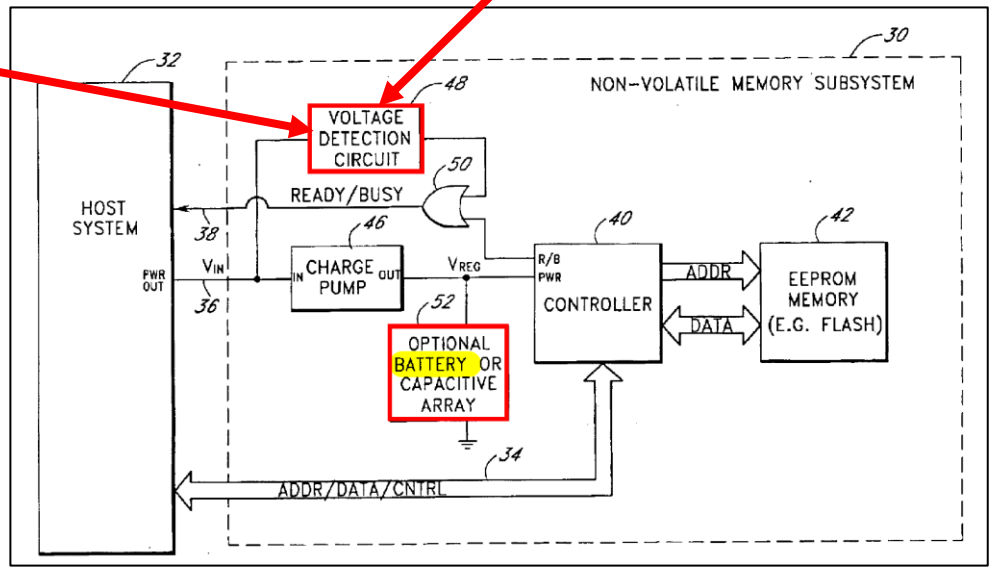
A. The charge pump gets the power signal from the host, so if the power signal from the host is cut off because an anomaly was detected and reported to the host through ready-busy, then the charge pump begins to shut down.

EX2030/EX2060 (Wolfe) at 251:10-16

Other types of power signal anomalies, such as power surges and spikes, can additionally cause permanent damage to the circuitry of the storage subsystem.

The storage subsystem in the preferred embodiment also includes a voltage detection circuit that monitors the power signal from the host system to detect anomalies. The voltage detection circuit responds to detection of a power signal anomaly by asserting a busy signal to block the host system from performing write operations to the storage subsystem. By asserting the busy signal, the voltage detection circuit substantially ensures that backup power provided by the charge pump (and by the battery and/or capacitive array, if provided) will be sufficient for the controller to complete all outstanding operations. The likelihood that data will be lost as the result of the power signal anomaly is therefore significantly reduced.

EX1038 (Hajeck) at 1:28-:31, 1:62-2:7 & Fig. 1



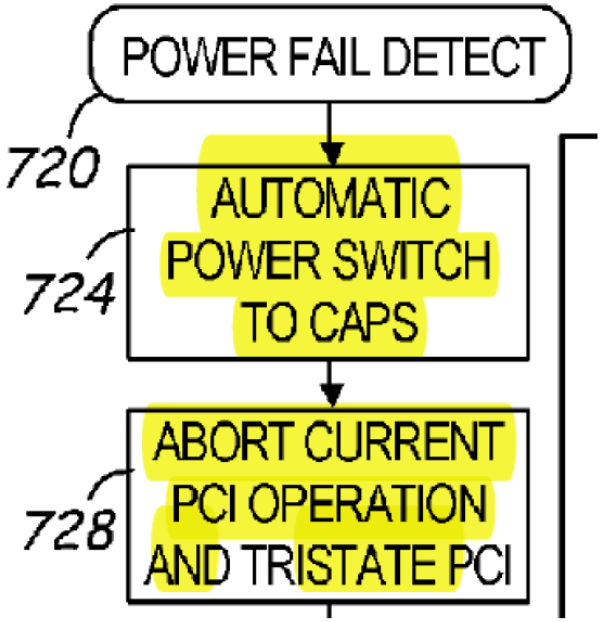
'918: Paper 1 (Pet.) at 12-13, 60-66. 75-77; Paper 25 (Reply) at 20-22
'054: Paper 1 (Pet.) at 12-13, 41-45, 53-54, 70-72; Paper 26 (Reply) at 21-23

SELECTIVELY SWITCHING A SECOND VOLTAGE ON/OFF ('918 CLAIM 23)

GROUND 4

(SPIERS + AMIDI)

The Institution Decision correctly found that Grounds 4-5 render "a second voltage…selectively switched on or off" obvious in Claim 23



EX1025 (Spiers), Fig. 14

Patent Owner contends that claim 23 requires a second voltage to be selectively switched on or off, and that Petitioner maps the second voltage as the voltage supply to the processor core. Prelim. Resp. 71 (citing Pet. 99). Patent Owner contends that Petitioner's mapping relates to turning off the supply voltage to the system bus, not the processor core. *Id*. (citing Pet. 114-15). Patent Owner does not explain why turning off the voltage supply on the system bus would not also turn off the power to the processor core. Although Patent Owner further argues that the processor must remain on while backing up data in the SDRAM, Patent Owner does not indicate what language in claim 23 requires the processor core to be switched on during data backup.

'918 ID at 53

Obvious to selectively switch off voltage to unused interface

5. Claim 23 (POR 71-72)

Netlist argues that Grounds 4-5 fail to satisfy "a 'second' voltage…selectively switched on or off" as required by claim 23. POR 71. But as correctly found by the Board, the related discussion for claim 8.b.3 shows this limitation would be obvious for at least two reasons. ID 53; Pet. 112-15. Netlist argues "Petitioner has not presented any situation in Spiers where the processor core would be off but the SDRAM remains on," POR 72, but that ignores the situation where "to conserve power during S3 sleep mode…the SDRAMs are in self-refresh mode and power to the processor is turned off," Pet. 112; EX1003, ¶¶820-22.

JEDEC

FBDIMM:
Advanced Memory Buffer (AMB)

6. Command/Address output control in S3 mode. When the Advanced Memory Buffer core logic is in S3 power mode, all command/address outputs, including CKE, ODT, CLK, and all other command/address pins, will be driven low. In S3 mode, 1.8V supply is on. 1.5V, Vtt, and 3.3V are off. DRAMs are in self refresh, and the CKE signals must be driven low.

EX1027, p. 1 & 21

'918: Paper 1 (Pet.) at 112-15; Paper 25 (Reply) at 33

"REGISTERED" ADDRESS AND CONTROL SIGNALS ('918 CLAIMS 8 & 14)

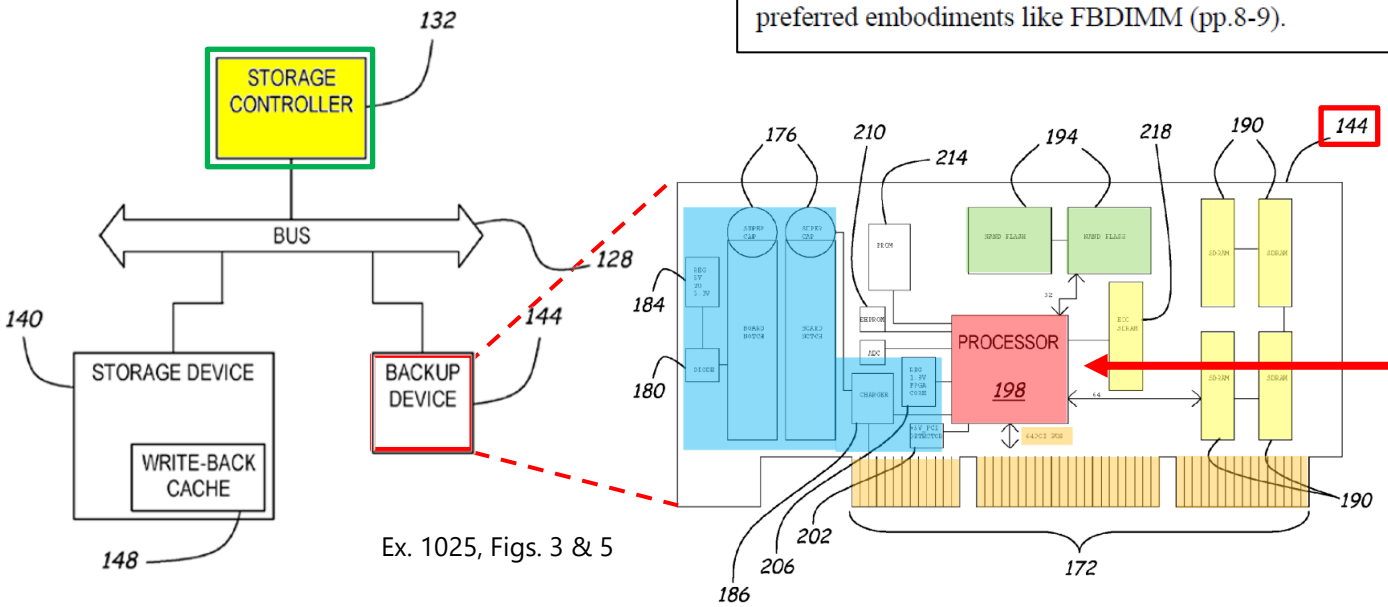
GROUND 4

(SPIERS + AMIDI)

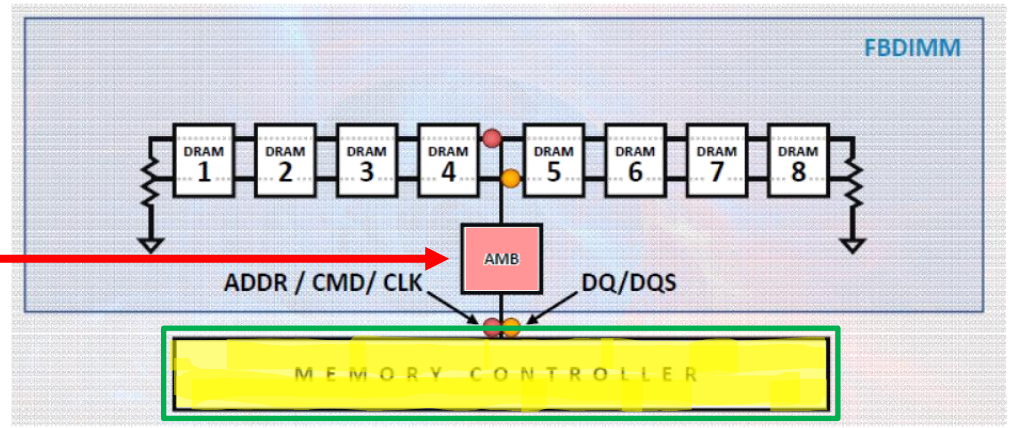
Translating signals from host to SDRAMs requires registering

8. Registered plurality of C/A signals for claims 8, 14 (POR 75-76

Netlist argues that Spiers's processor "translat[es]" the signals from the host to the SDRAMs, and thus supposedly does not "register[]" them. POR 75-76. But in order to "translate" those signals, Spiers's processor would first need to "capture" and thus "register" those signals, Pet. 108-12; EX1003, ¶807, as was standard, EX1075, 91:1-93:16; EX1077, 8. Nothing in the claims requires a direct pass-through of "registered" signals without translation, which would exclude preferred embodiments like FBDIMM (pp.8-9).



Ex. 1025, Figs. 3 & 5



EX1077, 9; *see also* EX1075 (Mangione-Smith), 97:16- 98:18

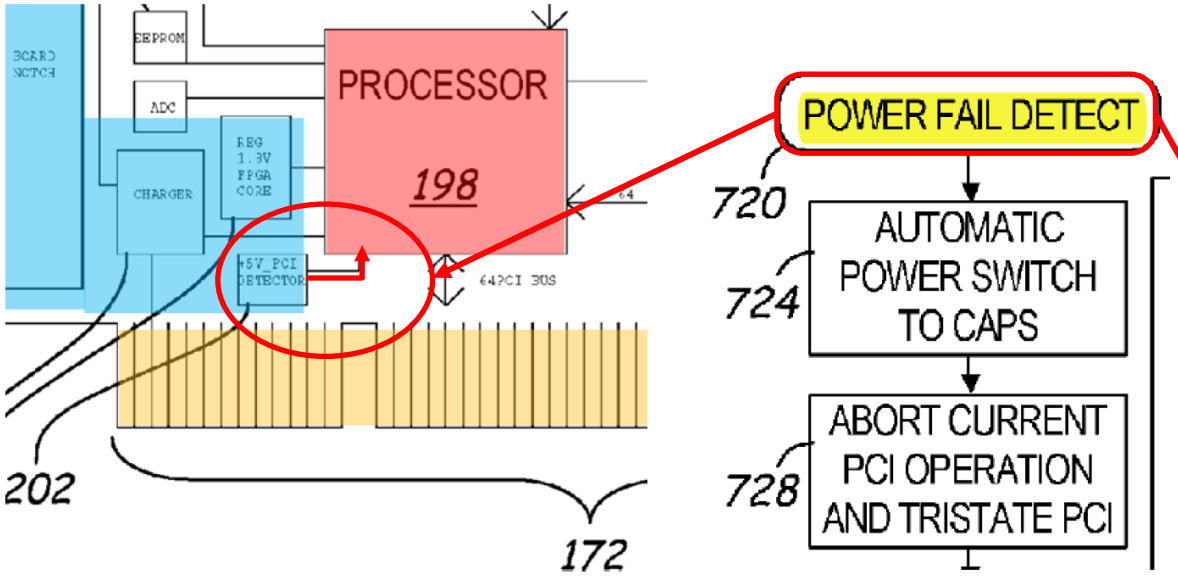
'918: Paper 1 (Pet.) at 109-11 and 120-21; Paper 25 (Reply) at 37

OVER-VOLTAGE DETECTION ('054 CLAIM 9)

GROUNDS 4-5

(SPIERS + AMIDI + HAJECK)

Sending an over-voltage detection signal was obvious



Ex. 1025 (Spiers), Figs. 5 & 14

1. Field of the Invention

The present invention relates to circuits from protecting storage subsystems, such as but not limited to flash memory cards, from damage and data loss caused by irregularities in a power signal provided by a host.

EX1038 (Hajeck) at 1:10-13

National Semiconductor

LMC6953

PCI Local Bus Power Supervisor

General Description

The LMC6953 is a voltage supervisory chip designed to meet PCI (Peripheral Component Interconnect) Specifications Revision 2.1. It monitors 5V and 3.3V power supplies. In cases of power-up, power-down, brown-out, power failure and manual reset interrupt, the LMC6953 provides an active low reset. $\overline{\text{RESET}}$ holds low for 100 ms after both 5V and 3.3V powers recover, or after manual reset signal returns to high state. The external capacitor on pin 8 adjusts the reset delay.

EX1063 at 1

'054: Paper 1 (Pet.) at 96, 107, 110-11; Paper 26 (Reply) at 34-36

MOTION TO EXCLUDE 04

BAKER BOTTS

Hyperlinks are not permissible evidence under 37 CFR § 42.63(a)

(a) *Exhibits Required.* Evidence consists of affidavits, transcripts of depositions, documents and things. **All evidence must be filed in the form of an exhibit**

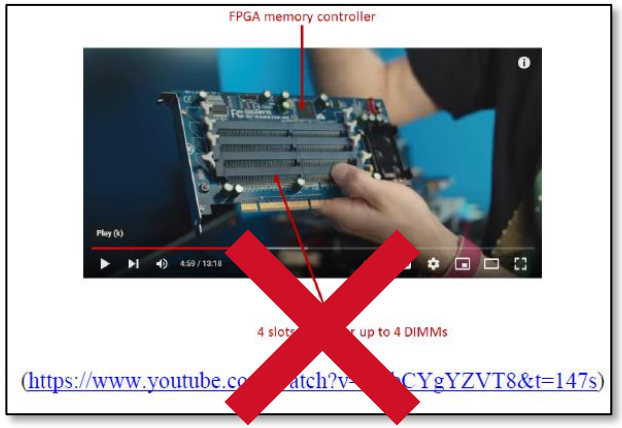
37 C.F.R. § 42.63(a) (emphasis added)

[2] "Main memory" is commonly known as RAM.

https://www.pcmag.com/encyclopedia/term/main-memory#:~:text=Main%20memory%20is%20the%20primary,to%20the%20capacity%20of%20RAM.

Sur-reply at p. 1, n.2

Sur-reply at p. 24



Sur-reply at p. 26

918: Paper 33 (Pet. MTE) at 1-3
054: Paper 35 (Pet. MTE) at 1-3

New evidence not allowed with Sur-Reply under 37 CFR § 42.23(b)

> A sur-reply may only respond to arguments raised in the corresponding reply ***and may not be accompanied by new evidence other than deposition transcripts*** of the cross-examination of any reply witness.

37 C.F.R. § 42.23(b) (emphasis added)

[2] "Main memory" is commonly known as RAM.

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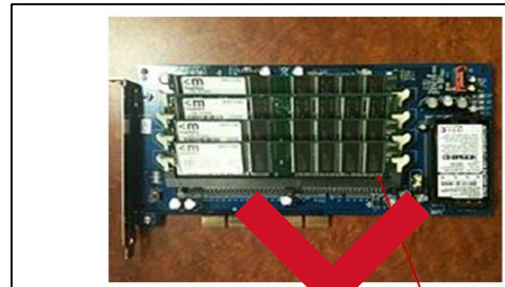
Sur-reply at p. 1, n.2



https://upload.wikimedia.org/wikipedia/commons/e/ef/IRAM13a.JPG).

Sur-reply at p. 24

(https://www.youtube.com/watch?v=[redacted]CYgYZVT8&t=147s)

Sur-reply at p. 26

918: Paper 33 (Pet. MTE) at 3-5
054: Paper 35 (Pet. MTE) at 3-5

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