UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD, MICRON TECHNOLOGY, INC.,
MICRON SEMICONDUCTOR PRODUCTS, INC., and
MICRON TECHNOLOGY TEXAS LLC
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

IPR2022-00996 (US11,016,918)
IPR2022-00999 (US11,232,054)

NETLIST

TOPICS

GROUNDS 1-3

Harris Does Not Receive Power Via Edge Connections

Harris Does Not Receive The Recited Signals From the Host

A POSITA Would Not Have Used the Required # of (Buck) Converters

Ground 2 ASSUMES Separate Converters To Supply Each FBDIMM-Required Voltage

A POSITA Would Not Have Replaced Harris' Redundant Power

Additional Reasons Why Dependent Claims Are Not Obvious

GROUNDS 4-5

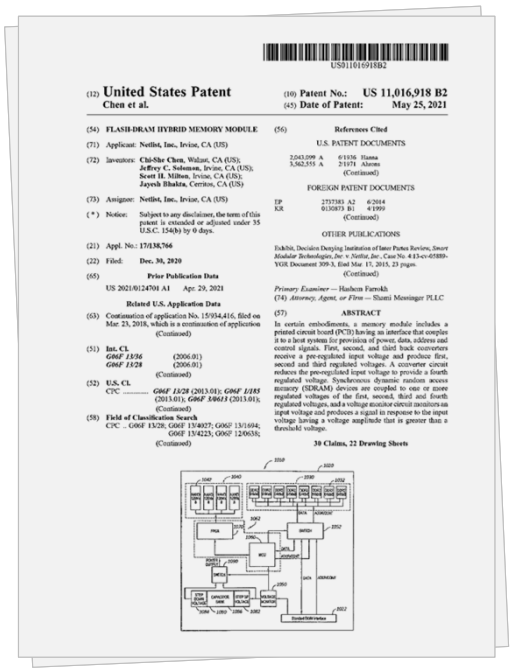
The Recited "Memory Module" Means A Main Memory Module

Spiers' PCI Card Is Not a Memory Module

POSITA Would Not Use DDR2/DDR3 or Recited # of (Buck) Converters

Additional Reasons Why Dependent Claims Are Not Obvious

The Challenged Claims Recite PCB Interface to the Host System Memory Slot



US011016918B2

(12) **United States Patent**
Chen et al.

(10) **Patent No.: US 11,016,918 B2**
(45) **Date of Patent: May 25, 2021**

(54) **FLASH-DRAM HYBRID MEMORY MODULE**

(71) Applicant: **Netlist, Inc.**, Irvine, CA (US)

(72) Inventors: **Chi-She Chen**, Walnut, CA (US); **Jeffrey C. Solomon**, Irvine, CA (US); **Scott H. Milton**, Irvine, CA (US); **Jayesh Bhakta**, Cerritos, CA (US)

(73) Assignee: **Netlist, Inc.**, Irvine, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **17/138,766**

(22) Filed: **Dec. 30, 2020**

(65) **Prior Publication Data**

US 2021/0124701 A1 Apr. 29, 2021

Related U.S. Application Data

(63) Continuation of application No. 15/934,416, filed on Mar. 23, 2018, which is a continuation of application (Continued)

(51) **Int. Cl.**
G06F 13/16 (2006.01)
G06F 13/28 (2006.01)
(Continued)

(52) **U.S. Cl.**
CPC ..... ***G06F 13/28*** (2013.01); ***G06F 13/1苏*** (2013.01); ***G06F 13/1673*** (2013.01); (Continued)

(58) **Field of Classification Search**
CPC .. G06F 13/28; G06F 13/4027; G06F 13/1694; G06F 13/4223; G06F 120638;
(Continued)

(56) **References Cited**

U.S. PATENT DOCUMENTS

2,043,099 A 6/1936 Hanna
3,562,555 A 2/1971 Ahrens
(Continued)

FOREIGN PATENT DOCUMENTS

EP 2737383 A2 6/2014
KR 0130873 B1 4/1999
(Continued)

OTHER PUBLICATIONS

Exhibit, Decision Denying Institution of Inter Partes Review, *Smart Modular Technologies, Inc. v. Netlist, Inc.*, Case No. 4:13-cv-05889-YGR Document 309-3, filed Mar. 17, 2015, 23 pages.
(Continued)

Primary Examiner — Hashem Farrokh
(74) *Attorney, Agent, or Firm* — Shumi Messinger PLLC

(57) **ABSTRACT**

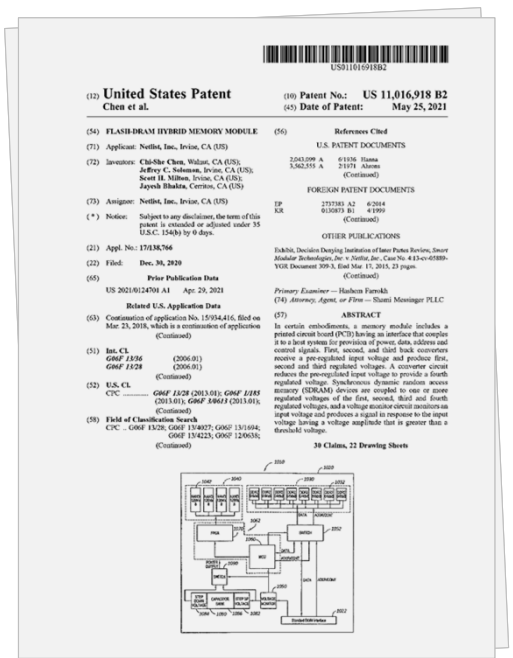
In certain embodiments, a memory module includes a printed circuit board (PCB) having an interface that couples it to a host system for provision of power, data, address and control signals. First, second, and third buck converters receive a pre-regulated input voltage and produce first, second and third regulated voltages. A converter circuit reduces the pre-regulated input voltage to provide a fourth regulated voltage. Synchronous dynamic random access memory (SDRAM) devices are coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages, and a voltage monitor circuit monitors an input voltage and produces a signal in response to the input voltage having a voltage amplitude that is greater than a threshold voltage.

30 Claims, 22 Drawing Sheets

The ’918/’054 Patents

1. A memory module comprising:
a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;

The PCB Interface (to Host Memory Slot) Has Edge Connections Coupling Power/Data/Address/Control From Host to the Memory Module



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(Continued)

(52) **U.S. Cl.**
CPC ***G06F 13/28*** (2013.01); ***G06F 1/185*** (2013.01); ***G06F 3/0613*** (2013.01);
(Continued)

(58) **Field of Classification Search**
CPC .. G06F 13/28; G06F 13/4027; G06F 13/1694; G06F 13/4226; G06F 12/0638;
(Continued)

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30 Claims, 22 Drawing Sheets

The ’918/’054 Patents

1. A memory module comprising:
a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;

Harris's Memory Module

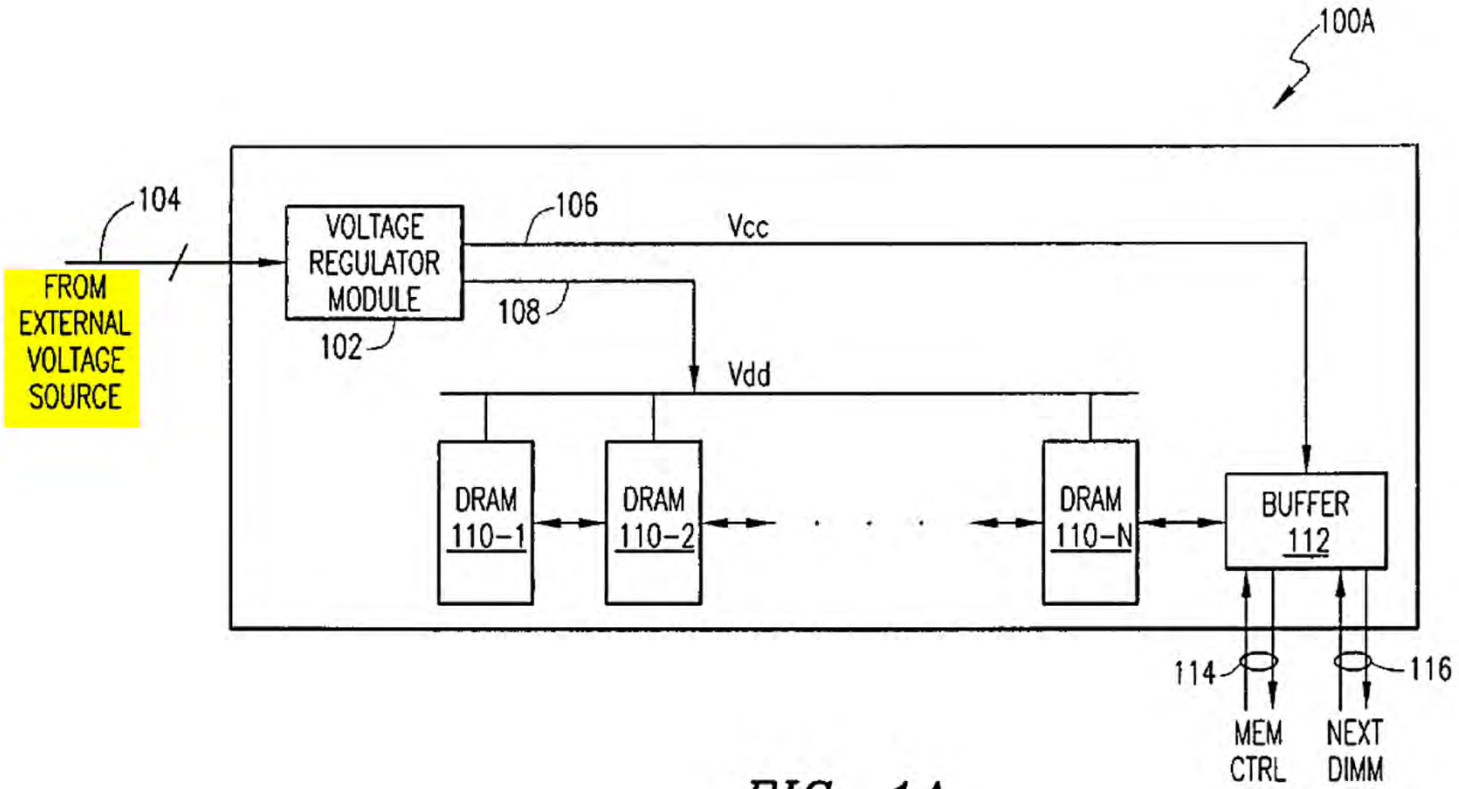


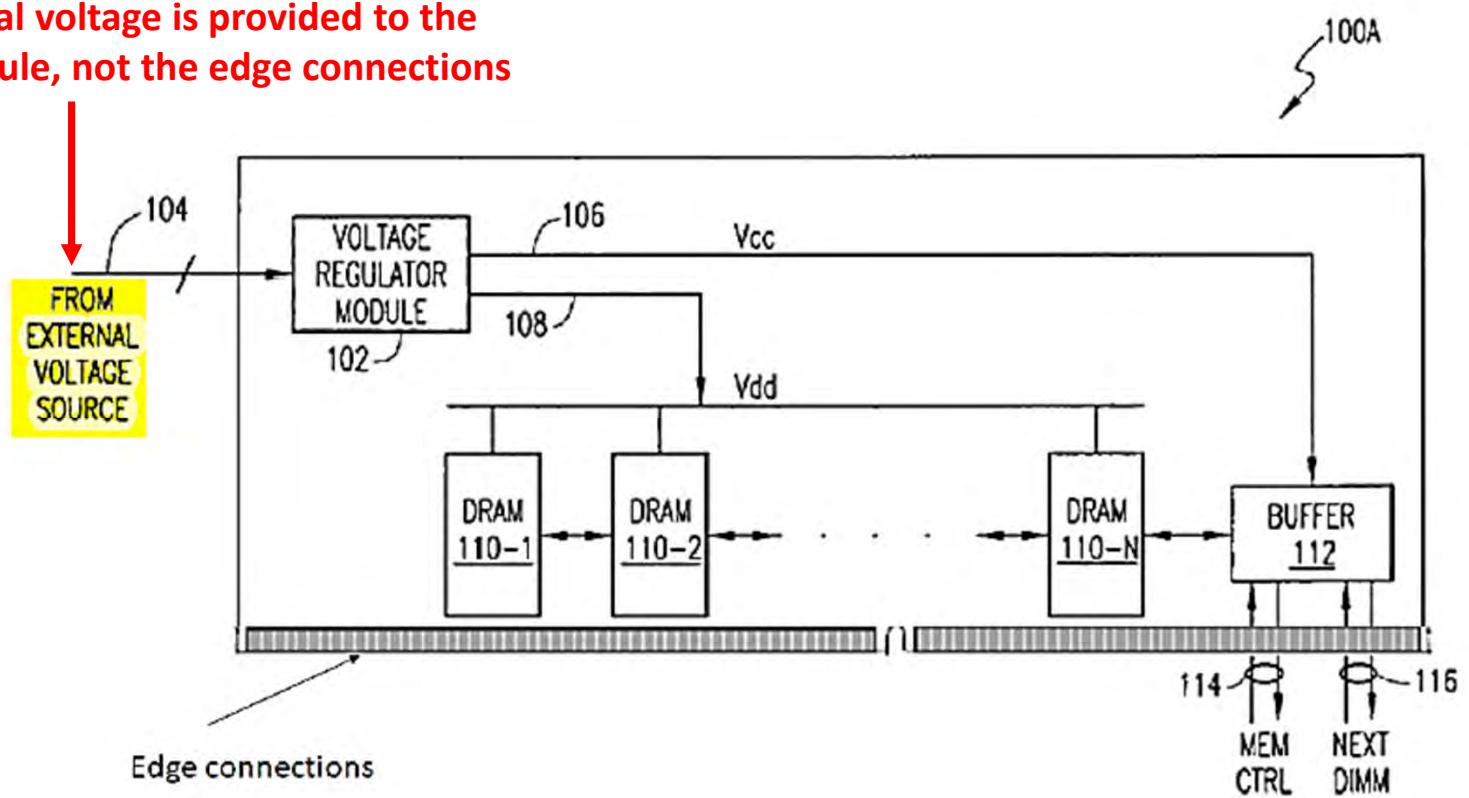
FIG. 1A

EX1023 (Harris), FIG. 1A.

Patent Owner Response (918) at 4.
Patent Owner Response (054) at 6.

Harris Does Not Provide Power to the Memory Module Via Memory Slot Edge Connections

Harris' external voltage is provided to the side of the module, not the edge connections



EX1023 (Harris), FIG. 1A (modified/annotated).

Patent Owner Response (918) at 5.
Patent Owner Response (054) at 7.

Petitioner Admits Location of Control/Data/Address Edge Connections on Harris

Harris, below, illustrates memory boards 306 coupled to the host system ***only*** through their edge connections (red), meaning power would also come from those edge connections:

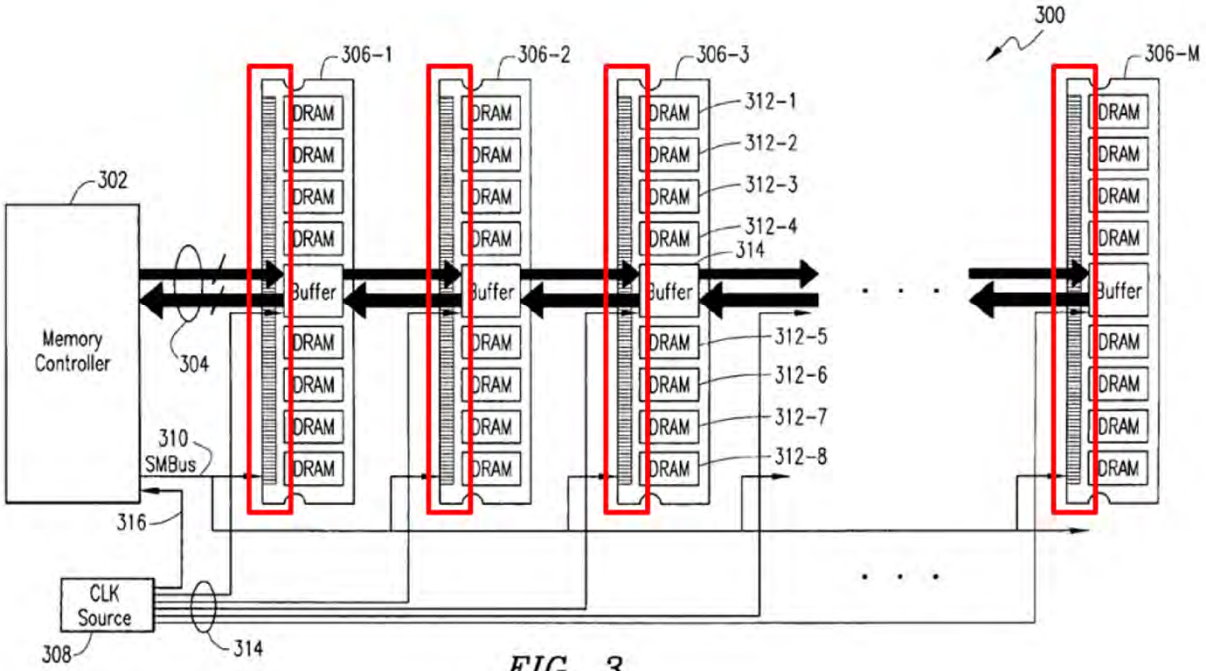
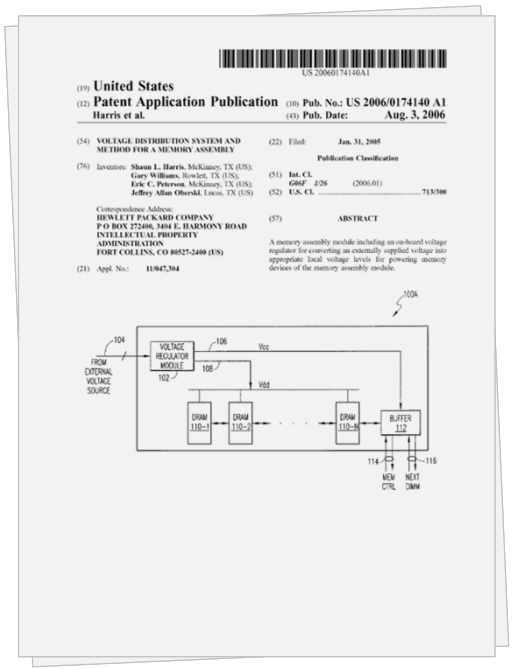


FIG. 3

Petitioner's Reply (918) at 3-4.
Petitioner's Reply (054) at 3-4.

Harris Expressly Replaces The Power Supply Pins On The Edge Connection Interface



US 20060174140A1

(19) United States

(12) Patent Application Publication (10) Pub. No.: US 2006/0174140 A1

Harris et al. (43) Pub. Date: Aug. 3, 2006

(54) VOLTAGE DISTRIBUTION SYSTEM AND METHOD FOR A MEMORY ASSEMBLY

(76) Inventors: Shaun L. Harris, McKinney, TX (US); Gary Williams, Rowlett, TX (US); Eric C. Peterson, McKinney, TX (US); Jeffrey Allan Oberski, Locus, TX (US)

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FORT COLLINS, CO 80527-2400 (US)

(21) Appl. No.: 11/047,304

(22) Filed: Jan. 31, 2005

Publication Classification

(51) Int. Cl.
G06F 1/26 (2006.01)

(52) U.S. Cl. 713/300

(57) ABSTRACT

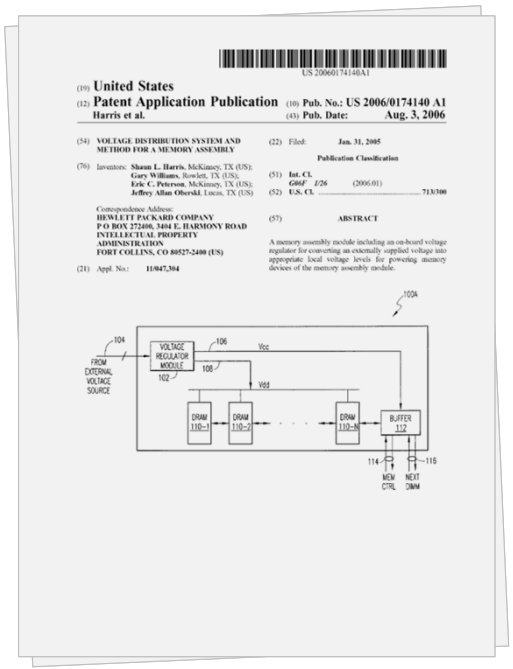
A memory assembly module including an on-board voltage regulator for converting an externally supplied voltage into appropriate local voltage levels for powering memory devices of the memory assembly module.

[0012] By way of example, a standard FBD module requires 28 V_{dd} pins (for DRAM devices) and 8 V_{cc} pins (for buffer and logic) and associated Ground returns, resulting in a total of 72 pins that provide a power supply interface for up to two x4 DRAM ranks (36 devices) and buffer logic. A voltage-independent FBD design incorporating the embodiment of **FIG. 1A** is capable of replacing these power supply interface pins with as few as six +12V pins (from an external voltage source), with local conversion to V_{dd} (to DRAM) and V_{cc} (to buffer/logic) being added. Alternatively, using

EX1023 (Harris), [0012].

Patent Owner Response (918) at 4, 6, 8.
Patent Owner Response (054) at 6, 8, 11.

Harris Expressly Replaces The Power Supply Interface Pins On The Edge Connections



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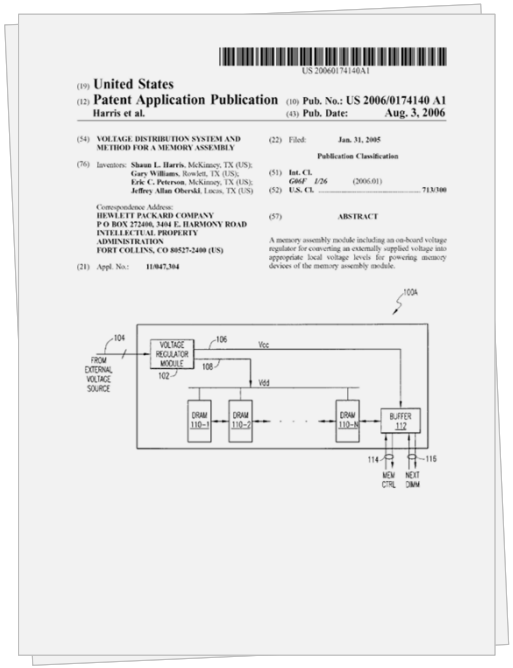
EX1023 (Harris), [0012].

Not "interface" pins

Patent Owner Response (918) at 4, 6, 8.
Patent Owner Response (054) at 6, 8, 11.

Harris Expressly Eliminates System Board Power Supply



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(21) Appl. No.: 11/047,304

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(52) U.S. Cl. 713/300

(57) ABSTRACT

A memory assembly module including an on-board voltage regulator for converting an externally supplied voltage into appropriate local voltage levels for powering memory devices of the memory assembly module.

[0019] Based on the foregoing Detailed Description, it should be appreciated that an implementation of the embodiments described herein thus provides a technology-independent voltage distribution scheme for memory devices wherein system board power supply and associated voltage plane(s) are eliminated. Accordingly, power supply design's complexity as well as the cost of memory-specific power distribution are reduced. Cost savings may include, for example, elimination of system-board-specific power supply or regulator output, associated bypass capacitor arrangements, heavy etch or power planes. Also, under the tech-

EX1023 (Harris), [0019].

If 12V were supplied from the motherboard, it would also be "system-board-specific power supply"

Patent Owner Response (918) at 4, 8, 10-11.
Patent Owner Response (054) at 6, 8, 10-11.

12V is "Unregulated"; Unregulated Voltage Never Routed Through Interface

respectively. Preferably, a high-frequency switching voltage converter capable of generating tightly-controlled voltage levels may be implemented as the on-board VRM **102** for purposes of the present patent disclosure. For instance, multi-phase synchronous Pulse-Width Modulated (PWM) controllers, Low Drop-Out (LDO) controllers, et cetera, that are capable of accepting unregulated supply voltages in a broad range may be configured to operate as a local voltage supply for the memory module **100**A.

EX1023 (Harris), [0010]

Dr. Mangione-Smith:

- Unregulated voltage never provided through interface pins or system board
- Harris does not describe alternative locations for unregulated or regulated voltage pins

EX2031 (918) (Mangione-Smith Declaration), ¶ 64.
EX2061 (054) (Mangione-Smith Declaration), ¶ 64.

Patent Owner Response (918) at 6.
Patent Owner Response (054) at 8-9.

12V is "Unregulated"; Unregulated Voltage Never Routed Through Interface

[0016] **FIG. 2** is a flowchart of a voltage distribution method for a memory module according to one embodiment. As set forth at block **202**, voltage is supplied to a memory board assembly from an external source, e.g., an unregulated source generating fairly high voltages (illustratively, at +12V) with a wide tolerance. The voltage distribution method then involves locally converting the supply voltage using an on-board VRM to generate appropriate levels of voltage for powering on-board memory devices. As pointed out earlier, the local voltage levels preferably depend on the application, e.g., DRAM type and technology. Optionally, a redundant VRM may be provided as part of the voltage distribution methodology, wherein the redundant VRM is operable to power a redundant voltage path with respect to the on-board memory devices and associated buffer/logic components (block **206**).

EX1023 (Harris), [0016].

Dr. Mangione-Smith:

- Unregulated voltage never provided through interface pins or system board
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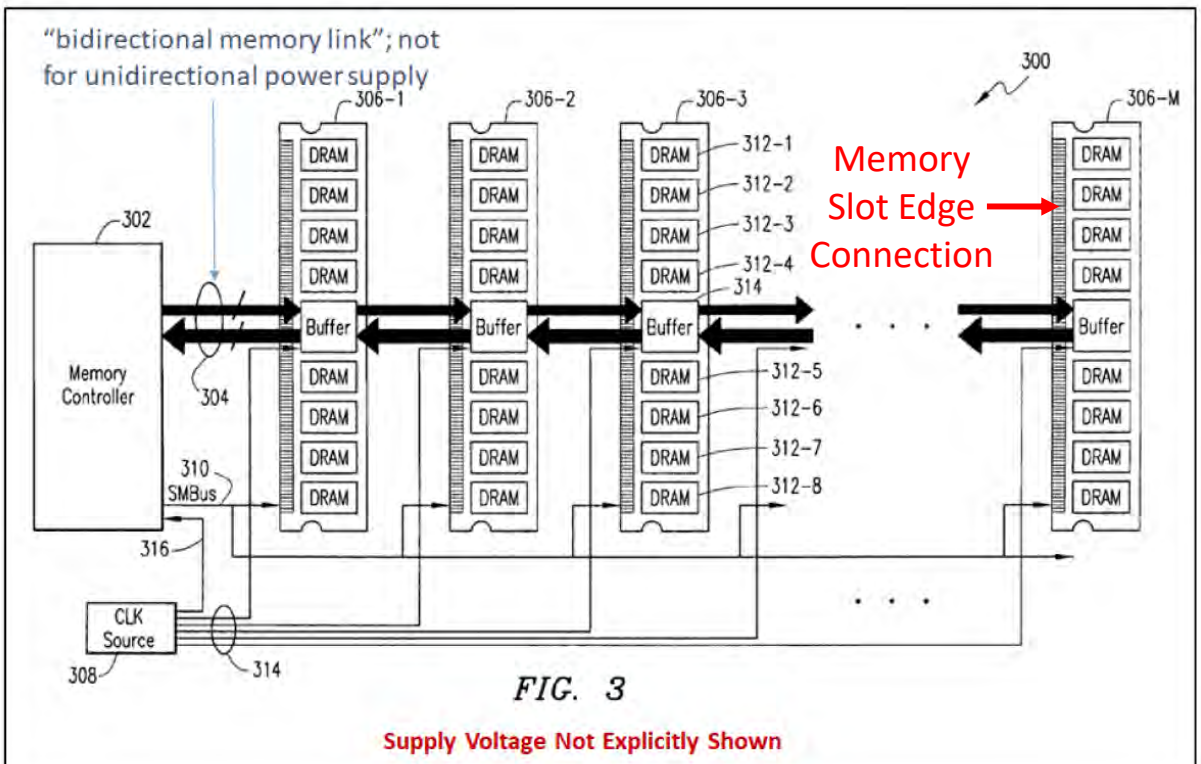
EX2031 (918) (Mangione-Smith Declaration), ¶ 64.
EX2061 (054) (Mangione-Smith Declaration), ¶ 64.

Patent Owner Response (918) at 6.
Patent Owner Response (054) at 6.

Harris Does Not Provide Power to the Memory Module Via Memory Slot Edge Connections

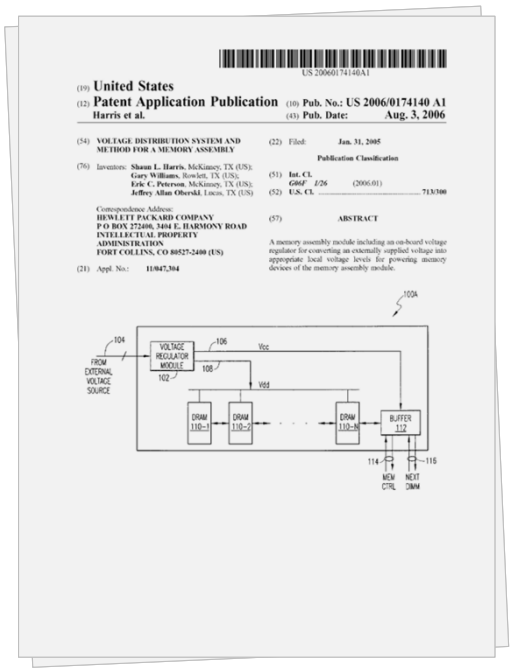


EX1023 (Harris), Fig. 3 (annotated).

Wolfe: "Figure 3 is a block diagram and it does not show the power supplies".

Patent Owner Sur-Reply (918) at 4; Patent Owner Sur-Reply (054) at 4.
EX2030, 130:19-23 (cited at POR, 8); EX2061, 130:19-23 (cited at POR, 11). DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

If Interface Pins Supplied Power in Harris, Figure 3 Would Depict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(19) United States

(12) Patent Application Publication (10) Pub. No.: US 2006/0174140 A1

Harris et al. (43) Pub. Date: Aug. 3, 2006

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(57) ABSTRACT

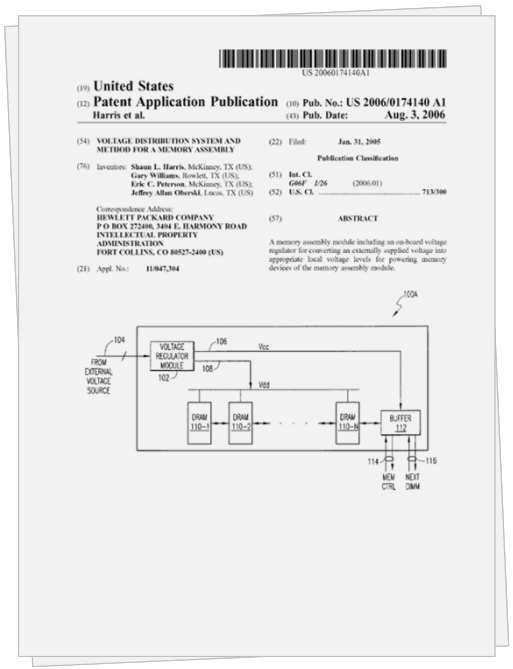
A memory assembly module including an on-board voltage regulator for converting an externally supplied voltage into appropriate local voltage levels for powering memory devices of the memory assembly module.

[0017] **FIG. 3** is a block diagram of an exemplary memory assembly **300** according to one embodiment. A memory controller **302** is operable to drive a bidirectional memory link **304** to which a plurality of memory boards **306-1** through **306**-M are coupled in a daisy-chain fashion at their respective buffers. As exemplified by the memory board **306-3**, each memory board includes eight DRAM devices **312-1** through **312-8**, with a buffer component **314**. A clock source **308** is operable to drive a plurality of clock signals to the memory boards via a clock bus **314**. Additionally, the clock source **308** is also operable to drive a clock signal **316** to the memory controller **302** for providing a time base with respect to its operations. A system management bus (SM bus) **310** coupled to the memory boards **306-1** through **306**-M is driven by the memory controller **302**. Although not explicitly shown in this FIGURE, each memory board also receives a supply voltage that is locally converted by an on-board VRM for powering the DRAM and buffer components therein. In one arrangement, the supply voltage may be sourced from the memory controller **302** or from a separate voltage source.

EX1023 (Harris), [0017].

Patent Owner Response (918) at 8; Patent Owner Response (054) at 11.
Patent Owner Sur-Reply (918) at 3, 19; Patent Owner Sur-Reply (054) at 3, 20.

Harris Touts the Benefits of Eliminating System-Board Power Supply (*i.e.*, an Internal Voltage Source)



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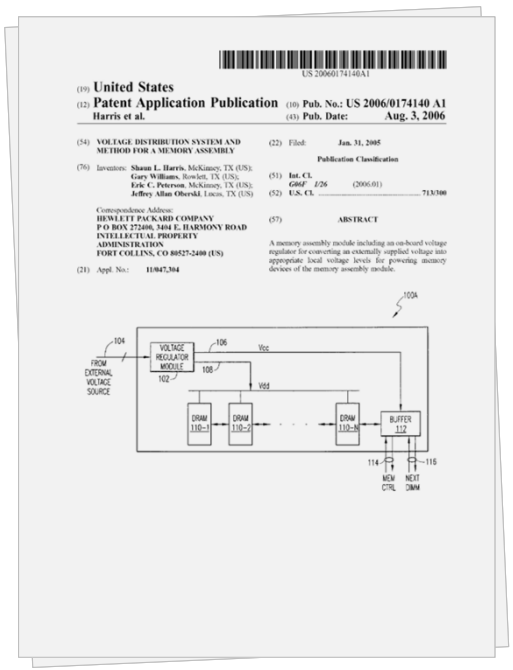
EX1023 (Harris), [0019]

[0020] Because voltage-independent embodiments disclosed herein can provide upgradeability and extensibility without changing system board power distribution, transitioning to newer DRAM technologies (e.g., at lower operating voltages) is more cost-effective as well as simpler to implement. Further, the embodiments are amenable to dual

EX1023 (Harris), [0020].

Patent Owner Response (918) at 8.
Patent Owner Response (054) at 8.

Avoiding Interface Pins for Voltage Allows System Board to Host Evolving Technology



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(21) Appl. No.: 11/047,304

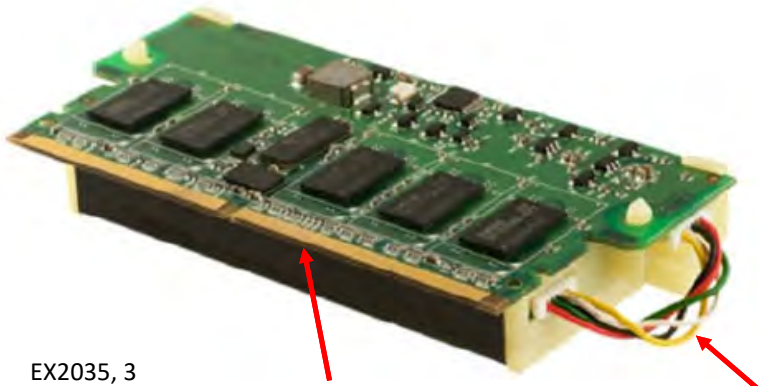
[0002] Such power supply concerns assume particular significance in advanced memory designs currently being implemented. Additionally, rising bus and processing speeds are also demanding newer memory architectures that deliver improved performance by increasing clock frequencies and available bandwidth without pushing up power consumption. To cope with power requirements, industry standard memory modules, e.g., Dual In-line Memory Modules (DIMMS) populated with dynamic random access memory (DRAM) devices, are provided with power supply rails (on a relatively large number of pins) that are powered from system board or main board voltage sources, and are specific to the memory technology. As the performance of the DRAM technology goes up, and timing margins shrink, it is becoming increasingly more difficult for the system board sources to provide tightly regulated power for the DRAM cores as well as input/output (I/O) interface buffers. Furthermore, each generation of DIMM/DRAM technology requires a different power supply which keeps getting lower (e.g., 3.3V, 2.5V, 1.8V, 1.5V and beyond), thereby making it difficult to mix memory technologies on a system board, or provide upgrades to next generation DRAM technology in a cost-effective manner. One skilled in the art will recognize, in addition, that these issues are particularly significant for systems that are deployed in infrastructure with an expected product life of over five years or so since it is difficult to accurately design a system that will be optimized over such a long life span.

EX1023 (Harris), [0002].

Patent Owner Response (918) at 3, 8, 35; Patent Owner Response (054) at 5, 10, 37.
Patent Owner Sur-Reply (918) at 5; Patent Owner Sur-Reply (054) at 5.

Providing Power to Memory Modules Via Non-Edge Connections Was Known

EX2036, 42.



EX2035, 3

Edge connections

BBvault

Backup Power Source

EX2035, 3; EX2036, 42.
Patent Owner Response (918) at 5.
Patent Owner Response (054) at 7.

The Claims Are Not Satisfied By Merely Supplying Power from the Host

Grounds 1A-1C teach the edge connections in Harris, consistent with JEDEC's FBDIMM Standards, are "*configured to couple power, data, address and control signals between the memory module and the host system*":

- "*power*": EX1023, ¶[0012] ("power"/"+12V" "pins"); *id.*, ¶¶[0010, 19] & Fig.1A (104, below).

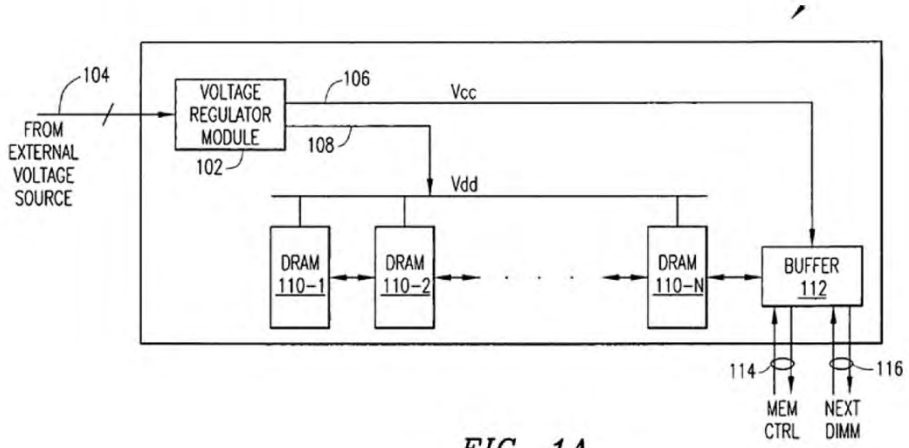


FIG. 1A

Petition (918) at 21-22.
Petition (054) at 21-22.

TOPICS

GROUNDS 1-3

Harris Does Not Receive Power Via Edge Connections

Harris Does Not Receive The Recited Signals From the Host

A POSITA Would Not Have Used the Required # of (Buck) Converters

Ground 2 ASSUMES Separate Converters To Supply Each FBDIMM-Required Voltage

A POSITA Would Not Have Replaced Harris' Redundant Power

Additional Reasons Why Dependent Claims Are Not Obvious

GROUNDS 4-5

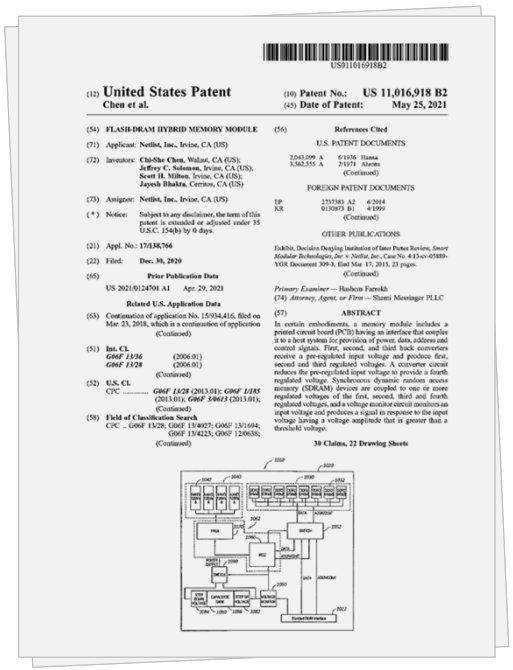
The Recited "Memory Module" Means A Main Memory Module

Spiers' PCI Card Is Not a Memory Module

POSITA Would Not Use DDR2/DDR3 or Recited # of (Buck) Converters

Additional Reasons Why Dependent Claims Are Not Obvious

Claimed PCB Interface Receives Data, Address, and Control Signals From the Host



US011016918B2

(12) **United States Patent**
Chen et al.

(10) **Patent No.: US 11,016,918 B2**
(45) **Date of Patent: May 25, 2021**

(54) **FLASH-DRAM HYBRID MEMORY MODULE**

(71) Applicant: **Netlist, Inc.**, Irvine, CA (US)

(72) Inventors: **Chi-She Chen**, Walnut, CA (US); **Jeffrey C. Solomon**, Irvine, CA (US); **Scott H. Milton**, Irvine, CA (US); **Jayesh Bhakta**, Cerritos, CA (US)

(73) Assignee: **Netlist, Inc.**, Irvine, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **17/138,766**

(22) Filed: **Dec. 30, 2020**

(65) **Prior Publication Data**

US 2021/0124701 A1 Apr. 29, 2021

Related U.S. Application Data

(63) Continuation of application No. 15/934,416, filed on Mar. 23, 2018, which is a continuation of application (Continued)

(51) **Int. Cl.**
G06F 13/16 (2006.01)
G06F 13/28 (2006.01)
(Continued)

(52) **U.S. Cl.**
CPC ***G06F 13/28*** (2013.01); ***G06F 1/185*** (2013.01); ***G06F 13/1673*** (2013.01);
(Continued)

(58) **Field of Classification Search**
CPC .. G06F 13/28; G06F 13/4027; G06F 13/1694; G06F 13/4223; G06F 120638;
(Continued)

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(Continued)

Primary Examiner — Hashem Farrokh
(74) *Attorney, Agent, or Firm* — Shumi Messinger PLLC

(57) **ABSTRACT**

In certain embodiments, a memory module includes a printed circuit board (PCB) having an interface that couples it to a host system for provision of power, data, address and control signals. First, second, and third buck converters receive a pre-regulated input voltage and produce first, second and third regulated voltages. A converter circuit reduces the pre-regulated input voltage to provide a fourth regulated voltage. Synchronous dynamic random access memory (SDRAM) devices are coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages, and a voltage monitor circuit monitors an input voltage and produces a signal in response to the input voltage having a voltage amplitude that is greater than a threshold voltage.

30 Claims, 22 Drawing Sheets

The ’918/’054 Patents

1. A memory module comprising:
a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;

FBDIMM – Advanced Memory Buffer (AMB)

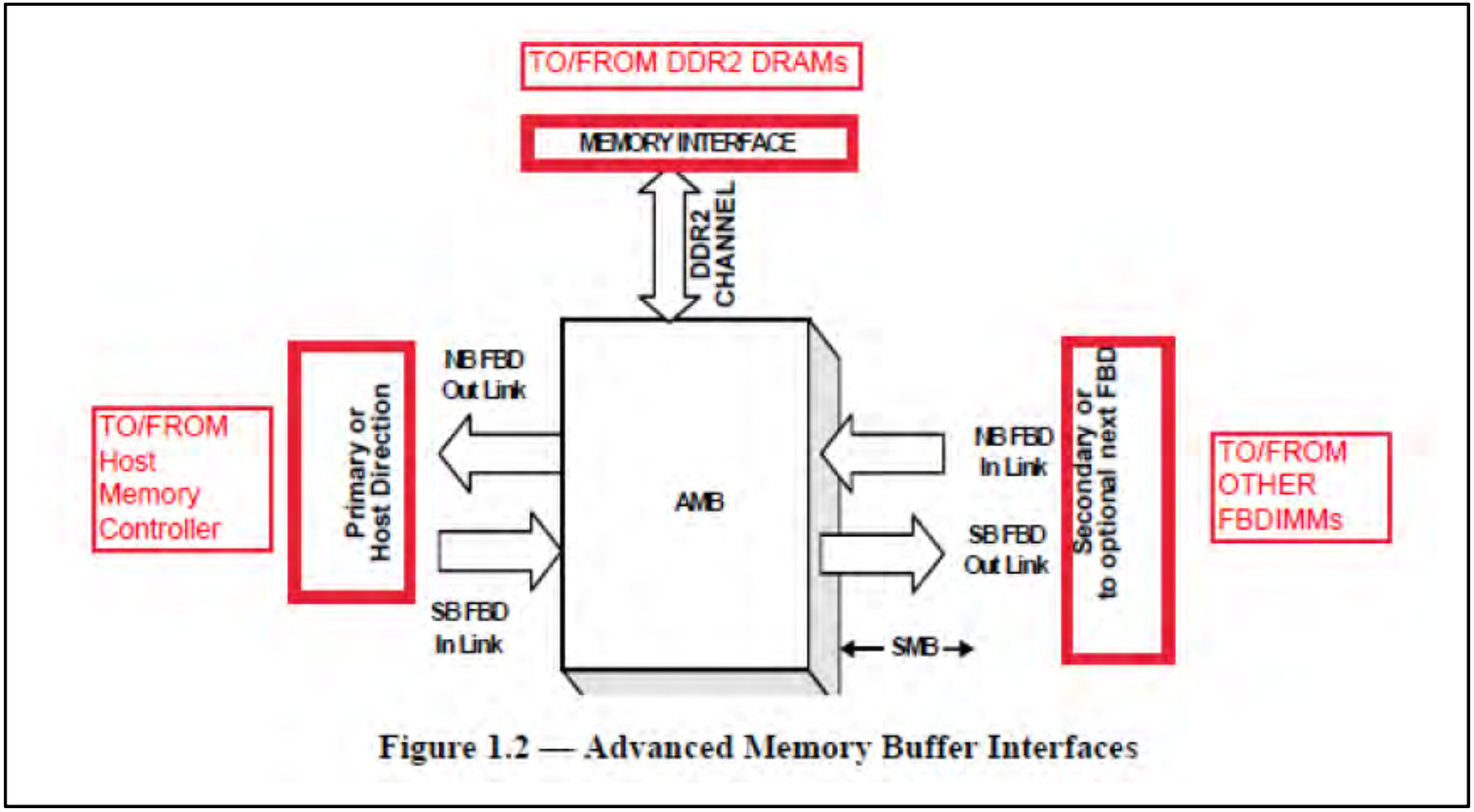


Figure 1.2 — Advanced Memory Buffer Interfaces

EX1027 at 4 (annotated).

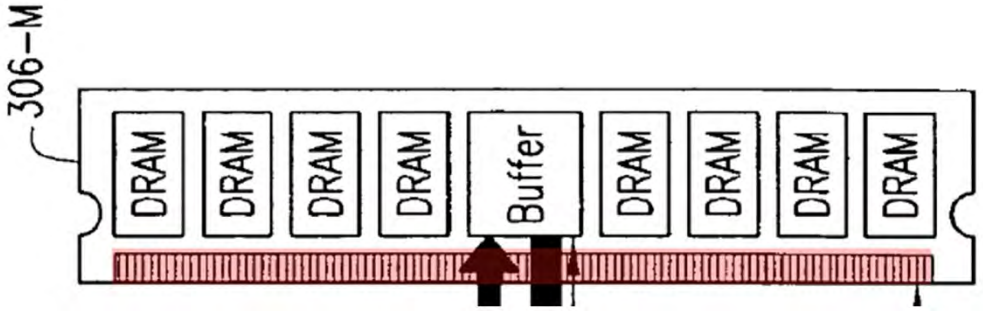
Patent Owner Response (918) at 11-12.
Patent Owner Response (054) at 14, 16.

The Petition Relies on Signals Generated On-Module By The AMB, Not Signals Received From The Host

The Petition

SAMSUNG

Grounds 1A-1C teach the PCB "*having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections*" (sometimes called "pins") as shown above for [1.a] and reprinted below from Harris's Figure 3. EX1023, ¶¶[0002, 12-13, 19], Figs. 3-4; EX1028, pp.38, 84; EX1003, ¶¶226-227.



Grounds 1A-1C teach the edge connections in Harris, consistent with JEDEC's FBDIMM Standards, are "*configured to couple power, data, address and control signals between the memory module and the host system*":

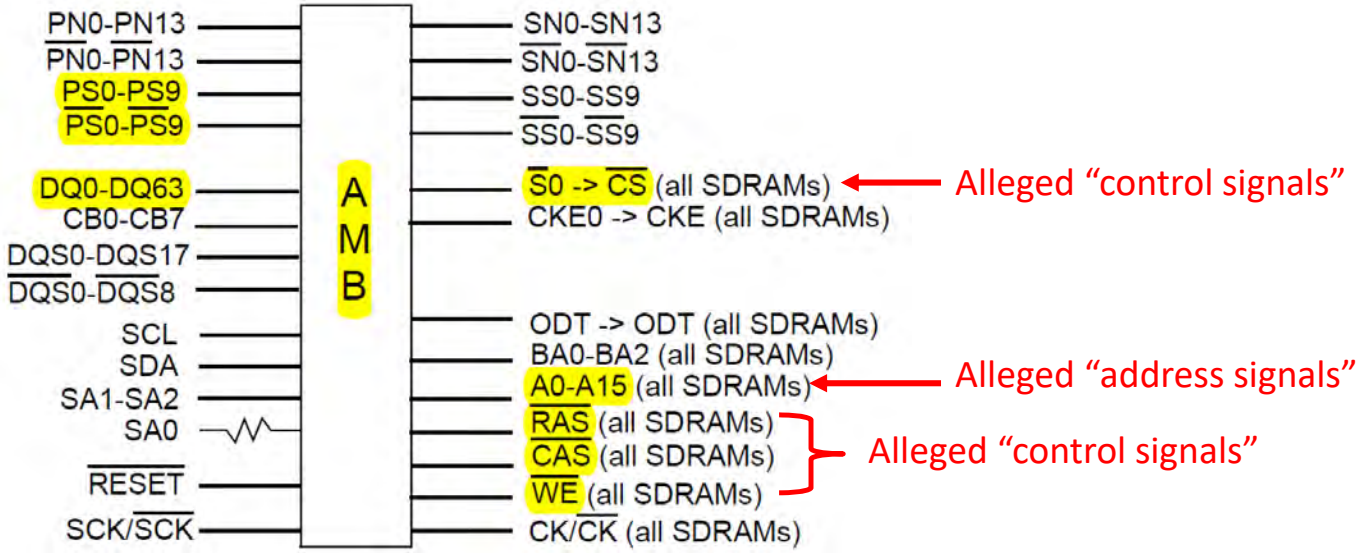
Petition (918) at 21.
Petition (054) at 21.

The Petition Relies on Signals Generated On-Module By The AMB, Not Signals Received From The Host

The Petition

SAMSUNG

- "*address*": e.g., A0-A15 (below); *id.* ("***address***")
- "*control*": e.g., RAS, CAS, WE, CS (below); *id.* & Fig.1A (114, "CTRL"). These "*control*" signals together can form a "command."



Petition (918) at 22-23.
Petition (054) at 22-23.

AMB Specification Distinguishes Data from Signals

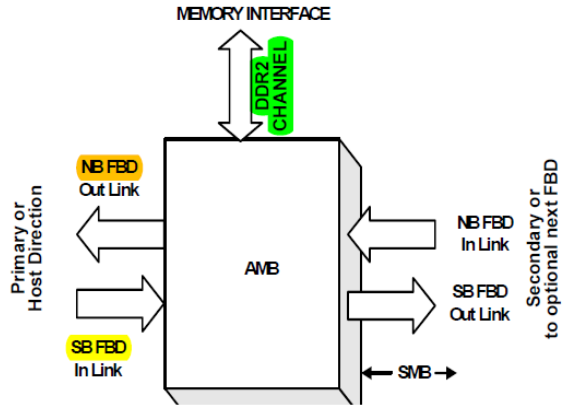


Figure 1.2 — Advanced Memory Buffer Interfaces

1.4.1 FBD High-Speed Differential Point-to-Point Link (at 1.5 V) Interfaces

The Advanced Memory Buffer supports one FBD Channel consisting of two bidirectional link interfaces using high-speed differential point-to-point electrical signaling.

The southbound input link is 10 lanes wide and carries commands and write data from the host memory controller or the adjacent DIMM in the host direction. The southbound output link forwards this same data to the next FBD.

The northbound input link is 13 to 14 lanes wide and carries read return data or status information from the next FB DIMM in the chain back towards the host. The northbound output link forwards this information back towards the host and multiplexes in any read return data or status information that is generated internally.

1.4.2 DDR2 Channel

The DDR2 channel on the Advanced Memory Buffer supports direct connection to DDR2 SDRAMs. The DDR2 channel supports two ranks of eight banks with 16 row/column request, 64 data signals, and eight check-bit signals. There are two copies of address and command signals to support DIMM routing and electrical requirements. Four-transfer bursts are driven on the data and check-bit lines at 800 MHz.

"Data" from controller to interface

"Signal" from AMB to DRAM

Patent Owner Response (918) at 12.
Patent Owner Response (054) at 16.

Harris+FBDIMM Module Receives Serialized Encoded Information

No pins on FBDIMM module to receive address or control signals from host

Pin Name	Pin Description	Count
	FB-DIMM Channel Signals	99
SCK	System Clock Input, positive line	1
$\overline{\text{SCK}}$	System Clock Input, negative line	1
PN[13:0]	Primary Northbound Data, positive lines	14
$\overline{\text{PN}}$[13:0]	Primary Northbound Data, negative lines	14
PS[9:0]	Primary Southbound Data, positive lines	10
$\overline{\text{PS}}$[9:0]	Primary Southbound Data, negative lines	10
SN[13:0]	Secondary Northbound Data, positive lines	14
$\overline{\text{SN}}$[13:0]	Secondary Northbound Data, negative lines	14
SS[9:0]	Secondary Southbound Data, positive lines	10
$\overline{\text{SS}}$[9:0]	Secondary Southbound Data, negative lines	10
FBDRES	To an external precision calibration resistor connected to Vcc	1

EX1027, 4.

Patent Owner Response (918) at 13.
Patent Owner Response (054) at 15.

Harris+FBDIMM Module Generates The Relied-on Address and Control Signals On-Module

Address and Control Signals Relied On By Petitioner Are Generated by AMB

DDR2 Interface Signals		175
DQS[8:0]	Data Strobes, positive lines	9
$\overline{\text{DQS}}$[8:0]	Data Strobes, negative lines	9
DQS[17:9]/DM[8:0]	Data Strobes (x4 DRAM only), positive lines. These signals are driven low to x8 DRAM on writes.	9
$\overline{\text{DQS}}$[17:9]	Data Strobes (x4 DRAM only), negative lines	9
DQ[63:0]	Data	64
CB[7:0]	Checkbits	8
A[15:0]A, A[15:0]B	Addresses. A10 is part of the pre-charge command	32
BA[2:0]A, BA[2:0]B	Bank Addresses	6
$\overline{\text{RASA}}$, $\overline{\text{RASB}}$	Part of command, with $\overline{\text{CAS}}$, $\overline{\text{WE}}$, and $\overline{\text{CS}}$[1:0].	2
$\overline{\text{CASA}}$, $\overline{\text{CASB}}$	Part of command, with $\overline{\text{RAS}}$, $\overline{\text{WE}}$, and $\overline{\text{CS}}$[1:0].	2
$\overline{\text{WEA}}$, $\overline{\text{WEB}}$	Part of command, with $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, and $\overline{\text{CS}}$[1:0].	2
ODTA, ODTB	On-die Termination Enable	2
CKE[1:0]A, CKE[1:0]B	Clock Enable (one per rank)	4
$\overline{\text{CS}}$[1:0]A, $\overline{\text{CS}}$[1:0]B	Chip Select (one per rank)	4
CLK[3:0]	CLK[1:0] used on 9 and 18 device DIMMs. CLK[3:0] used on 36 device DIMMs. CLK[3:2] should be output disabled when not in use.	4
$\overline{\text{CLK}}$[3:0]	Negative lines for CLK[3:0]	4
DDRC_C14	DDR Compensation: Common return pin for DDRC_B18 and DDRC_C18.	1
DDRC_B18	DDR Compensation: Resistor connected to common return pin DDRC_C14	1
DDRC_C18	DDR Compensation: Resistor connected to common return pin DDRC_C14	1
DDRC_B12	DDR Compensation: Resistor connected to V_{SS}	1
DDRC_C12	DDR Compensation: Resistor connected to V_{DD}	1

EX1027, 4.

Patent Owner Response (918) at 13.
Patent Owner Response (054) at 15.

Harris+FBDIMM Module Receives Serialized Encoded Information

Fully-Buffered DIMM Memory Architectures: Understanding Mechanisms, Overheads and Scaling

Brinda Ganesh†, Aamer Jaleel‡, David Wang†, and Bruce Jacob†

†University of Maryland, College Park, MD
‡VSSAD, Intel Corporation, Hudson, MA

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systems, which we shall refer to as DDRx systems. The serial interface is split into two uni-directional buses, one for read traffic (northbound channel) and another for write and command traffic (southbound channel), as shown in Fig 1. FBDIMMs adopts a packet-based protocol that bundles commands and data into frames that are transmitted on the channel and then converted to the DDRx protocol by the AMB.

EX2040 at 1.

Patent Owner Response (918) at 12.
Patent Owner Response (054) at 14.

Dr. Wolfe Testified That The AMB Receives Address/Control Information

Andrew Wolfe
Samsung's Expert

SAMSUNG

> Q. And the address and the control information are sent as serialized packets; is that correct?
>
> A. Serialized packets? They -- yes. They are -- the information is sent to the advanced memory buffer in the form of serialized packets.

EX2030 (918) (Wolfe Deposition), 10:7-11.
EX2060 (054) (Wolfe Deposition), 10:7-11.

Patent Owner Sur-Reply (918) at 8.
Patent Owner Sur-Reply (054) at 8.

Harris+FBDIMM Module Received Data, Address, and Control Information

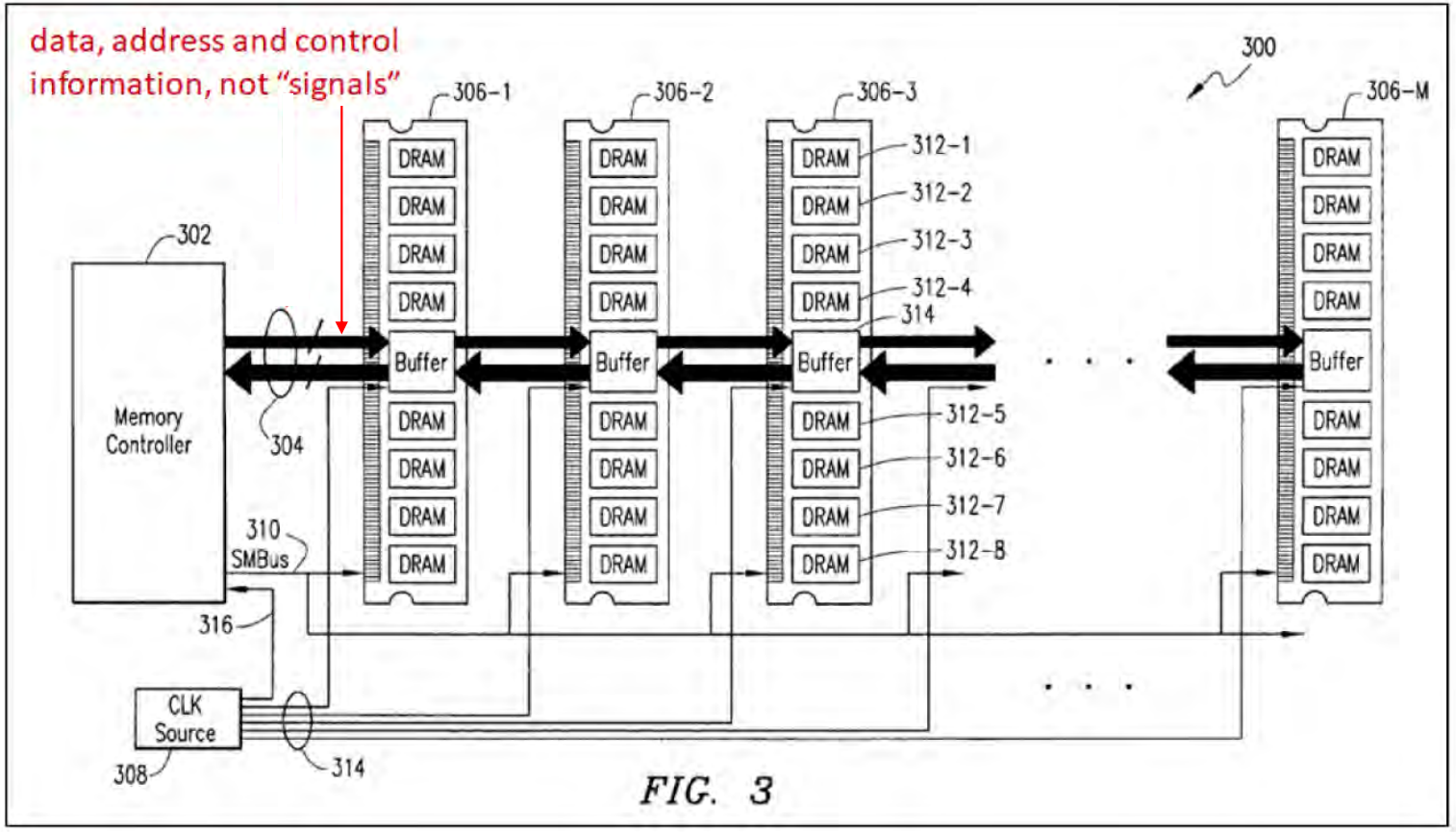
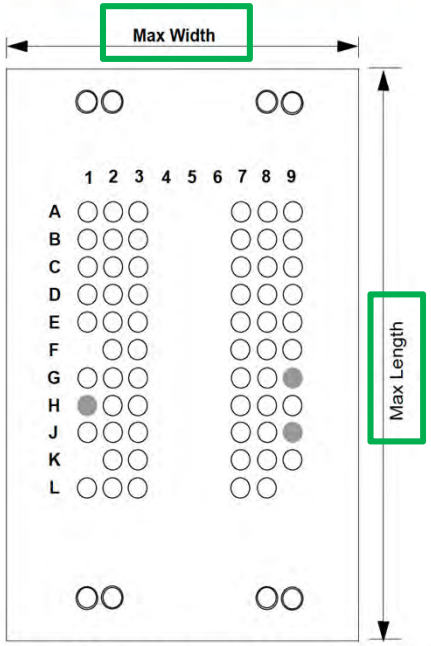


FIG. 3

Patent Owner Sur-Reply (918) at 8.
Patent Owner Sur-Reply (054) at 8.

FBDIMM Form Factor



Note: Double circles indicate the location of support balls of Variation DM-z
Gray circles indicate the balls for stacked only

Component Details

Supported SDRAM Component Maximum size for 256Mb to 4Gb, DDR2 SDRAM

Raw Card	Package Type	Supported DRAM Outline (Width x Length) max. (mm)			
		MO-207 Variation			
		DJ-z (60 pins)	DM-z (68 pins)	DL-z (92 pins)	DK-z (84 pins)
A	Planar	12.4 x 15	12.4 x 18	12.4 x 21	12.4 x 21
B,C	Planar	11.4 [2] (12.4 [1,2]) x 15	11.4 [2] (12.4 [1,2]) x 18	11.4 [2] (12.4 [1,2]) x 21[3]	11.4 [2] (12.4 [1,2]) x 21
E	Planar	11 x 11.5	--	--	--
H	Planar	12[4] x 11	--	--	--
		MO-242 Variation			
		AA (63 pins)	AD (71 pins)	AC (95 pins)	AB (87 pins)
D,J	Stacked	11.4 [2] (12.4 [1,2]) x 15	11.4 [2] (12.4 [1,2]) x 18	11.4 [2] (12.4 [1,2]) x 21[3]	11.4 [2] (12.4 [1,2]) x 21

1. supported only if no-decoupling capacitor are placed in between the DRAMs
2. 0.4 mm DRAM to DRAM spacing
3 Heat sink attachment may modify the max DRAM length that will fit to 18.6mm
4. Heat sink attachment may modify the max DRAM width that will fit to 11.5mm

5	Module Physical Attribues	30~35mm height 8~9mm thick	0x24	

Petition (918) at 11; Petition (054) at 10-11.
EX1028 (918, 054) at 25-26, 105.

TOPICS

GROUNDS 1-3

Harris Does Not Receive Power Via Edge Connections

Harris Does Not Receive The Recited Signals From the Host

A POSITA Would Not Have Used the Required # of (Buck) Converters

Ground 2 ASSUMES Separate Converters To Supply Each FBDIMM-Required Voltage

A POSITA Would Not Have Replaced Harris' Redundant Power

Additional Reasons Why Dependent Claims Are Not Obvious

GROUNDS 4-5

The Recited "Memory Module" Means A Main Memory Module

Spiers' PCI Card Is Not a Memory Module

POSITA Would Not Use DDR2/DDR3 or Recited # of (Buck) Converters

Additional Reasons Why Dependent Claims Are Not Obvious

Petitioner's Proposed Voltage Mappings for '918 Patent Based on Harris+FBDIMM

Recited Voltages of Claim 1

a first buck converter configured to provide a first regulated voltage having a first voltage amplitude;
a second buck converter configured to provide a second regulated voltage having a second voltage amplitude;
a third buck converter configured to provide a third regulated voltage having a third voltage amplitude;
a converter circuit configured to provide a fourth regulated voltage having a fourth voltage amplitude; and

	Voltage Mappings (Grounds 1-3)		
	A	B	C
"*first*":	V_{DD} or V_{DDQ} = 1.8V	V_{DD}, V_{DDQ}, or V_{DDL} = 1.8V	V_{DD}, V_{DDQ}, or V_{DDL} = 1.8V
"*second*":	V_{CC} or V_{CCFBD} = 1.5V	V_{CC}=1.5V	V_{CC} or V_{CCFBD} = 1.5V
"*third*":	V_{DDL}=1.8V	V_{CCFBD}=1.5V	V_{TT}=0.9V
"*fourth*":	V_{DDSPD}=3.3V	V_{DDSPD}=3.3V	V_{DDSPD}=3.3V

Petition (918) at 26-27.

Petitioner's Proposed Voltage Mappings for '054 Patent Based on Harris+FBDIMM

Recited Voltages of Claim 1

a voltage conversion circuit coupled to the PCB and configured to provide at least three regulated voltages, wherein the voltage conversion circuit includes at least three buck converters each of which is configured to produce a regulated voltage of the at least three regulated voltages;

	Voltage Mappings (Grounds 1-3)		
	A	B	C
"*first*":	V_{DD} or V_{DDQ} = 1.8V	V_{DD} or V_{DDQ} = 1.8V	V_{DD} or V_{DDQ} = 1.8V
"*second*":	V_{CC} or V_{CCFBD} = 1.5V	V_{CC}=1.5V	V_{CC} or V_{CCFBD} = 1.5V
"*third*":	V_{DDL}=1.8V	V_{CCFBD}=1.5V	V_{TT}=0.9V

Petition (054) at 27.

Harris Proposed Only VDD and VCC Generated On-Module In Face of DDR Specifications, Including FBDIMMs

[0012] By way of example, a standard FBD module requires 28 V_{dd} pins (for DRAM devices) and 8 V_{cc} pins (for buffer and logic) and associated Ground returns, resulting in a total of 72 pins that provide a power supply interface for up to two x4 DRAM ranks (36 devices) and buffer logic. A voltage-independent FBD design incorporating the embodiment of **FIG. 1A** is capable of replacing these power supply interface pins with as few as six +12V pins (from an external voltage source), with local conversion to V_{dd} (to DRAM) and V_{cc} (to buffer/logic) being added. Alternatively, using additional power supply pins would provide the capability to support even more devices. For instance, with 12 supply pins (at +12V), the embodiment of **FIG. 1A** can provide enough power to supply 4 ranks (i.e., 72 devices). Likewise, a memory assembly of 8 ranks (144 devices) may be powered with 24 pins at +12V.

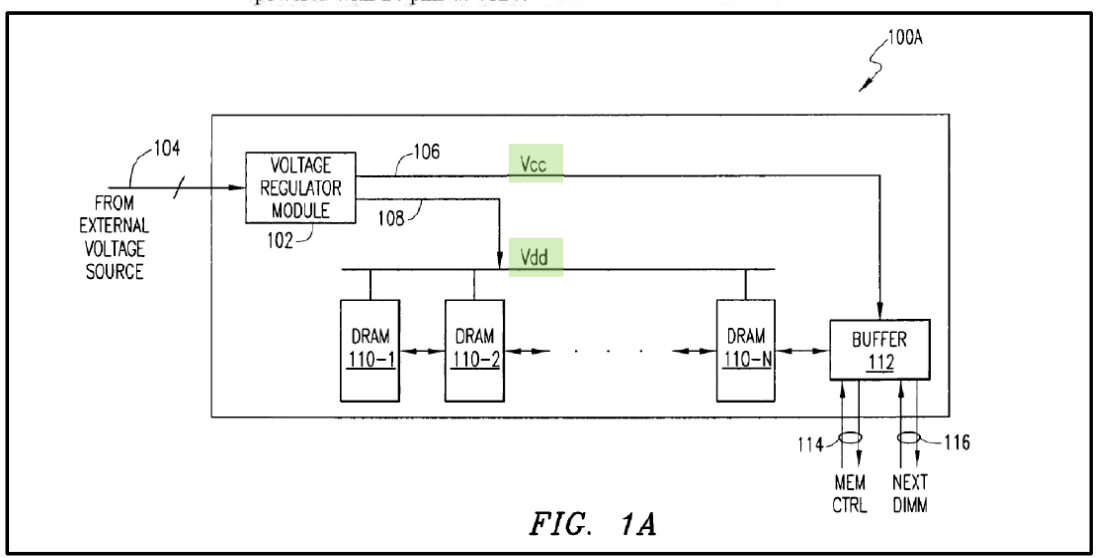


FIG. 1A

[0009] In the drawings, like or similar elements are designated with identical reference numerals throughout the several views thereof, and the various elements depicted are not necessarily drawn to scale. Referring now in particular to **FIG. 1A**, depicted therein is a block diagram of a voltage distribution system for a memory module **100**A according to one embodiment. At the outset, those skilled in the art should appreciate that although the voltage distribution system is exemplified with respect to memory module **100**A which may be embodied as a memory board assembly operable in a computer system, the teachings of the present patent disclosure may be implemented in any electronic system as will be set forth in detail hereinbelow. One or more memory devices **110-1** through **110**-N are provided as part of the memory module **100**A, each receiving a first voltage path **108**, typically referred to as a V_{dd} path, that may be energized to appropriate voltage levels depending on the type, functionality, and design of the memory devices, e.g., from about 0.5V to 3.5V or more. In one configuration, the memory module **100**A may be implemented as a Dual In-line Memory Module (DIMM) wherein each of the memory devices **110-1** through **110**-N comprises a Double Data Rate (DDR) dynamic random access memory (DRAM) device having a particular density, e.g., 256 Mb, 512 Mb, 1 Gb or 2 Gb, etc. Also, the memory devices can be of any known or heretofore unknown DDR type, e.g., DDR2 (operable with 1.8 V), DDR3 (operable with 1.35V to 1.5V), and the like. Further, the DIMM configuration of an exemplary memory module may include unbuffered DIMMs, registered DIMMs (RDIMMs), or fully buffered DIMMs (FBDs), and may be configured as having one or more ranks (e.g., 2, 4, 8, or more). In the illustrated embodiment of **FIG. 1A**, for instance, the DIMM configuration of the memory module **100**A is exemplified as a fully buffered DIMM wherein a buffer/logic component **112** is provided for buffering command/address (C/A) space as well as data space at least for a portion of the memory devices **110-1** through **110**-N. A bidirectional memory controller interface path **114** as well as a second voltage path **106**, typically referred to as a V_{cc} path, are provided with respect to the buffer component **112**, wherein the V_{cc} path may be energized to appropriate voltage levels depending on the buffer and DIMM technology, e.g., from about 0.5V to 3.5V or more. In addition, where multiple memory assemblies are daisy-chained on a single memory controller channel, a suitable daisy-chain interface **116** is provided for coupling the buffer component **112** to a next memory module.

Vdd to "memory devices"

Targets DDR-Standardized Devices

Vcc to buffer/DIMMM

Petition (918) at 10, 16; Petition (054) at 9-10, 16.
Patent Owner Response (918) at 17; Patent Owner Response (054) at 20.

EX1023 (Harris), [0009].

that the voltage distribution system for memory module **100B** is essentially similar to the system shown in **FIG. 1A**, but for the redundancy implementation of local voltage conversion. A plurality of on-board VRMs **122**-K, K=1, 2, . . . , N, are provided as part of the memory assembly/module **100B** wherein each VRM is operable with an independent voltage supply path for locally converting an external supply voltage into appropriate local voltage levels. Reference

EX1023 (Harris), [0014].

[0010] In accordance with the teachings of the present patent disclosure, at least one on-board voltage regulator module (VRM) is provided as part of the memory board assembly module **100**A for converting an externally supplied voltage level available on external source path **104** into appropriate local voltage levels that power the first and second voltage paths, i.e., the V_{dd} and V_{cc} paths **108**, **106**,

EX1023 (Harris), [0010].

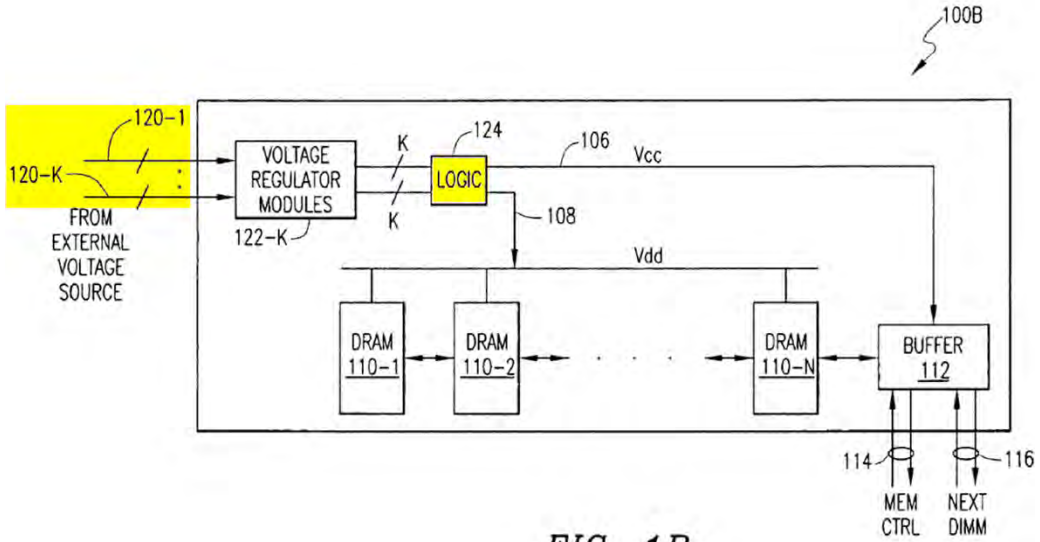


FIG. 1B

EX1023 (Harris), FIG. 1B.

Patent Owner Response (918) at 32.
Patent Owner Response (054) at 35.

Petitioner's Expert Confirms That a POSA Reading Harris Would Understand And Comply With JEDEC Standards

158. A Skilled Artisan would have been familiar with memory systems and corresponding standards, including the JEDEC standards for memory devices and memory modules already standardized, or in the process of being standardized, at the time. For example, Harris discloses Double Data Rate (DDR) memory devices, including DDR2 and DDR3 memories. *See* Ex. 1023 at [0009], [0011]. A Skilled Artisan would have understood that these memories were already standardized. *Supra* ¶139 (DDR SDRAM), ¶140 (DDR2 SDRAM), ¶141 (FBDIMM), ¶142 (DDR3 SDRAM). Harris also discloses Dual In-Line Memory Modules (DIMMs), including unbuffered DIMMs (UDIMMs), registered DIMMs (RDIMMs), and fully-buffered DIMMs (FBDIMMs). *See* Ex. 1023 at [0009]. A Skilled Artisan would have understood that these memory modules were already standardized,

EX1003 (918) (Wolfe), ¶158.
EX1003 (054) (Wolfe), ¶159.

161. In my view, a Skilled Artisan would have been familiar with the relevant JEDEC memory standards, including the FBDIMM Standards. Even if one were to argue that Harris does not sufficiently disclose a memory module in accordance with the teachings of these JEDEC memory standards or that a Skilled Artisan would not be familiar with the FBDIMM Standards, it would have been obvious to a Skilled Artisan, who would have been motivated to implement Harris's module using memory devices and/or buffer devices standardized by JEDEC, including the FBDIMM Standards, as explained below.

EX1003 (918) (Wolfe), ¶161.
EX1003 (054) (Wolfe), ¶162.

Petition (918) at 16.
Petition (054) at 16.

In FBDIMM Specification, One Source For VCC/VCCFD; One Source For VDD, VDDQ, VDDL

DIMM Connector Pin Description

Pin Name	Pin Description	Count
SCK	System Clock Input, positive line[1]	1
$\overline{SCK}$	System Clock Input, negative line[1]	1
PN[13:0]	Primary Northbound Data, positive lines	14
$\overline{PN}$[13:0]	Primary Northbound Data, negative lines	14
PS[9:0]	Primary Southbound Data, positive lines	10
$\overline{PS}$[9:0]	Primary Southbound Data, negative lines	10
SN[13:0]	Secondary Northbound Data, positive lines	14
$\overline{SN}$[13:0]	Secondary Northbound Data, negative lines	14
SS[9:0]	Secondary Southbound Data, positive lines	10
$\overline{SS}$[9:0]	Secondary Southbound Data, negative lines	10
SCL	Serial Presence Detect (SPD) Clock Input	1
SDA	SPD Data Input / Output	1
SA[2:0]	SPD Address Inputs, also used to select the DIMM number in the AMB	3
VID[1:0]	Voltage ID: These pins must be unconnected for DDR2-based Fully Buffered DIMMs VID[0] is V_{DD} value: OPEN = 1.8 V, GND = 1.5 V; VID[1] is V_{CC} value: OPEN = 1.5 V, GND = 1.2 V	2
$\overline{RESET}$	AMB reset signal	1
RFU	Reserved for Future Use[2]	16
V_{CC}	AMB Core Power and AMB Channel Interface Power (1.5 Volt)	8
V_{DD}	DRAM Power and AMB DRAM I/O Power (1.8 Volt)	24
V_{TT}	DRAM Address/Command/Clock Termination Power (V_{DD}/2)	4
V_{DDSPD}	SPD Power	1
V_{SS}	Ground	80

V_{CC} and V_{CCFBD}

V_{DD}, V_{DDQ} and V_{DDL}

88. It was also generally known that, for the "VDD (VDD, VDDL, VDDQ)" power supply, "[t]he DDR2 device requires a single power source for primary supply voltages in order to ensure that all voltage levels track each other, especially during the power ramp." EX2006 (Micron TN-47-05), 4. It was known that "VDD (device core), VDDL (device DLL), and VDDQ (device I/O) share a single power plane with the interconnecting pins labeled as VDD," and that "[a]t the initial power-up, all supply power should be stable and meet specification within ≤10ms." Id. Meeting such stability and timing specifications is made possible when the voltages (e.g., V_{DD}, V_{DDL} and V_{DDQ}) are driven from a single power converter instead of from separate converters.

EX2031 (918) (Mangione-Smith Declaration), ¶88.
EX2061 (054) (Mangione-Smith Declaration), ¶88.

Patent Owner Response (918) at 22-23.
Patent Owner Response (054) at 25-26.

Vtt Is Never Supplied to DRAM

Harris Proposes On Module Vdd to DRAM

[0012] By way of example, a standard FBD module requires 28 V_{dd} pins (for DRAM devices) and 8 V_{cc} pins (for buffer and logic) and associated Ground returns, resulting in a total of 72 pins that provide a power supply interface for up to two x4 DRAM ranks (36 devices) and buffer logic. A voltage-independent FBD design incorporating the embodiment of **FIG. 1A** is capable of replacing these power supply interface pins with as few as six +12V pins (from an external voltage source), with local conversion to V_{dd} (to DRAM) and V_{cc} (to buffer/logic) being added. Alternatively, using additional power supply pins would provide the capability to support even more devices. For instance, with 12 supply pins (at +12V), the embodiment of **FIG. 1A** can provide enough power to supply 4 ranks (i.e., 72 devices). Likewise, a memory assembly of 8 ranks (144 devices) may be powered with 24 pins at +12V.

EX1023 (Harris), [0009].

DRAM Does not receive Vtt

1.1 DDR2 SDRAM package ballout

(Top view: see balls through package)

	1	2	3	4	5	6	7	8	9	
	NC	NC						NC	NC	A
										B
										C
										D
Variation DJ-z without support balls	VDD	NC	VSS				VSSQ	$\overline{DQS}$	VDDQ	E
	NC	VSSQ	DM				DQS	VSSQ	NC	F
	VDDQ	DQ1	VDDQ				VDDQ	DQ0	VDDQ	G
	NC	VSSQ	DQ3				DQ2	VSSQ	NC	H
	VDDL	VREF	VSS				VSSDL	CK	VDD	J
		CKE	$\overline{WE}$				$\overline{RAS}$	$\overline{CK}$	ODT	K
	NC, BA2	BA0	BA1				$\overline{CAS}$	$\overline{CS}$		L
		A10/AP	A1				A2	A0	VDD	M
	VSS	A3	A5				A6	A4		N
		A7	A9				A11	A8	VSS	P
	VDD	A12	NC, A14				NC, A15	NC, A13		R
										T
										U
										V
	NC	NC						NC	NC	W

Variation DM-z with support balls

EX1026 (DDR2 SDRAM), at 1.

Patent Owner Response (918) at 28.
Patent Owner Response (054) at 31-32.

Harris Does Not Proposed Separate Module Regulators For 5 VTT/VDDSPD Pins

Architecture

DIMM Connector Pin Description

Pin Name	Pin Description	Count
SCK	System Clock Input, positive line[1]	1
$\overline{SCK}$	System Clock Input, negative line[1]	1
PN[13:0]	Primary Northbound Data, positive lines	14
$\overline{PN}$[13:0]	Primary Northbound Data, negative lines	14
PS[9:0]	Primary Southbound Data, positive lines	10
$\overline{PS}$[9:0]	Primary Southbound Data, negative lines	10
SN[13:0]	Secondary Northbound Data, positive lines	14
$\overline{SN}$[13:0]	Secondary Northbound Data, negative lines	14
SS[9:0]	Secondary Southbound Data, positive lines	10
$\overline{SS}$[9:0]	Secondary Southbound Data, negative lines	10
SCL	Serial Presence Detect (SPD) Clock Input	1
SDA	SPD Data Input / Output	1
SA[2:0]	SPD Address Inputs, also used to select the DIMM number in the AMB	3
VID[1:0]	Voltage ID: These pins must be unconnected for DDR2-based Fully Buffered DIMMs VID[0] is V_{DD} value: OPEN = 1.8 V, GND = 1.5 V; VID[1] is V_{CC} value: OPEN = 1.5 V, GND = 1.2 V	2
$\overline{RESET}$	AMB reset signal	1
RFU	Reserved for Future Use[2]	16
V_{CC}	AMB Core Power and AMB Channel Interface Power (1.5 Volt)	8
V_{DD}	DRAM Power and AMB DRAM I/O Power (1.8 Volt)	24
V_{TT}	DRAM Address/Command/Clock Termination Power (V_{DD}/2)	4
V_{DDSPD}	SPD Power	1
V_{SS}	Ground	80

single set of VCC pins for VCC/VCCFBD

single set of VDD pins for VDD/VDDQ/VDDL

EX1028 (JEDEC FBDIMM Specification), 11.

Patent Owner Response (918) at 22.
Patent Owner Response (054) at 25.

The FBDIMM Standard Uses A Single Converter For VDD/VDDQ/VDDL

2.3.1 Power-up and initialization sequence

The following sequence is required for POWER UP and Initialization.

a) Apply power and attempt to maintain CKE below 0.2*VDDQ and ODT[*1] at a low state (all other inputs may be undefined.) The power voltage ramp time must be no greater than 20mS; and during the ramp, VDD>VDDL>VDDQ and VDD-VDDQ<0.3 volts.

- VDD, VDDL and VDDQ are driven from a single power converter output, AND
- VTT is limited to 0.95 V max, AND
- Vref tracks VDDQ/2.

or

- Apply VDD without any slope reversal before or at the same time as VDDL.
- Apply VDDL without any slope reversal before or at the same time as VDDQ.
- Apply VDDQ without any slope reversal before or at the same time as VTT & Vref.

at least one of these two sets of conditions must be met.

FBDIMM Standard provides for a single converter for VDD/VDDQ/VDDL

EX1026 (JEDEC DDR2 SDRAM Specification), 9.

Patent Owner Response (918) at 25.
Patent Owner Response (054) at 28.

Petitioner's Reliance on an Alleged "Option 2" Fails To Motivate Using Separate Buck Converters For VDD/VDDQ/VDDL

2.3.1 Power-up and initialization sequence

The following sequence is required for POWER UP and Initialization.

a) Apply power and attempt to maintain CKE below 0.2*VDDQ and ODT[*1] at a low state (all other inputs may be undefined.) The power voltage ramp time must be no greater than 20mS; and during the ramp, VDD>VDDL>VDDQ and VDD-VDDQ<0.3 volts.

- VDD, VDDL and VDDQ are driven from a single power converter output, AND
- VTT is limited to 0.95 V max, AND
- Vref tracks VDDQ/2.

Option 1

or

- Apply VDD without any slope reversal before or at the same time as VDDL.
- Apply VDDL without any slope reversal before or at the same time as VDDQ.
- Apply VDDQ without any slope reversal before or at the same time as VTT & Vref.

at least one of these two sets of conditions must be met.

Option 2

EX1026 (JEDEC DDR2 SDRAM Specification), 9.

Patent Owner Response (918) at 25.
Patent Owner Response (054) at 28.

Petitioner's Alleged "Option 2" Are Actually Alternatives to Vref Tracking

2.3.1 Power-up and initialization sequence

The following sequence is required for POWER UP and Initialization.

a) Apply power and attempt to maintain CKE below 0.2*VDDQ and ODT[*1] at a low state (all other inputs may be undefined.) The power voltage ramp time must be no greater than 20mS; and during the ramp, VDD>VDDL>VDDQ and VDD-VDDQ<0.3 volts.

- VDD, VDDL and VDDQ are driven from a single power converter output, AND
- VTT is limited to 0.95 V max, AND
- Vref tracks VDDQ/2.

or

- Apply VDD without any slope reversal before or at the same time as VDDL.
- Apply VDDL without any slope reversal before or at the same time as VDDQ.
- Apply VDDQ without any slope reversal before or at the same time as VTT & Vref.

at least one of these two sets of conditions must be met.

"Options" end in periods, not "ANDs"

EX1026 (JEDEC DDR2 SDRAM Specification), 9.

Patent Owner Response (918) at 25.
Patent Owner Response (054) at 28.

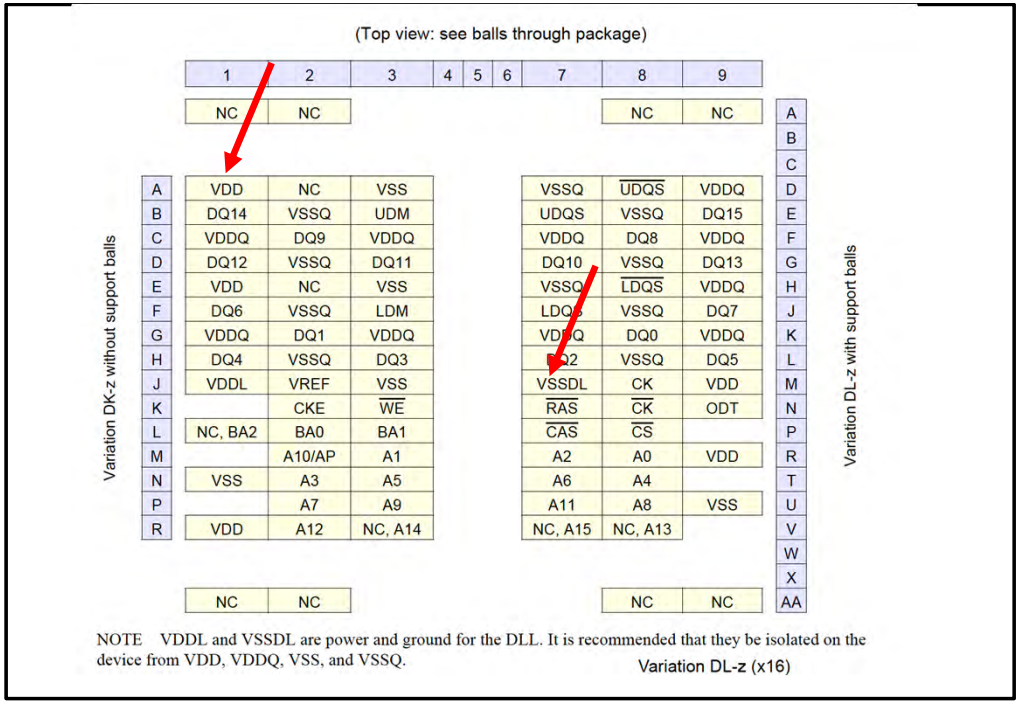
Turning Voltages On Or Off Separately Does Not Motivate Separate Converters

- Apply VDD without any slope reversal before or at the same time as VDDL.
- Apply VDDL without any slope reversal before or at the same time as VDDQ.
- Apply VDDQ without any slope reversal before or at the same time as VTT & Vref.

EX1026 (JEDEC DDR2 SDRAM Specification), 9.

Patent Owner Response (918) at 25.
Patent Owner Response (054) at 28.

“Isolation” Refers to DRAM Device Bumps



(Top view: see balls through package)

	1	2	3	4	5	6	7	8	9	
	NC	NC						NC	NC	A
										B
										C
A	VDD	NC	VSS				VSSQ	$\overline{\text{UDQS}}$	VDDQ	D
B	DQ14	VSSQ	UDM				UDQS	VSSQ	DQ15	E
C	VDDQ	DQ9	VDDQ				VDDQ	DQ8	VDDQ	F
D	DQ12	VSSQ	DQ11				DQ10	VSSQ	DQ13	G
E	VDD	NC	VSS				VSSQ	$\overline{\text{LDQS}}$	VDDQ	H
F	DQ6	VSSQ	LDM				LDQS	VSSQ	DQ7	J
G	VDDQ	DQ1	VDDQ				VDDQ	DQ0	VDDQ	K
H	DQ4	VSSQ	DQ3				DQ2	VSSQ	DQ5	L
J	VDDL	VREF	VSS				VSSDL	CK	VDD	M
K		CKE	$\overline{\text{WE}}$				$\overline{\text{RAS}}$	$\overline{\text{CK}}$	ODT	N
L	NC, BA2	BA0	BA1				$\overline{\text{CAS}}$	$\overline{\text{CS}}$		P
M		A10/AP	A1				A2	A0	VDD	R
N	VSS	A3	A5				A6	A4		T
P		A7	A9				A11	A8	VSS	U
R	VDD	A12	NC, A14				NC, A15	NC, A13		V
										W
										X
	NC	NC						NC	NC	AA

Variation DK-z without support balls

Variation DL-z with support balls

NOTE VDDL and VSSDL are power and ground for the DLL. It is recommended that they be isolated on the device from VDD, VDDQ, VSS, and VSSQ.

Variation DL-z (x16)

EX1026, 3.

89. Dr. Wolfe’s evidence regarding separate pins and control of individual voltages is also misplaced. First, Dr. Wolfe’s citation to EX1028, 17-20 (cited at EX1003, ¶ 267, for a citation to separate pins for V_{DD}, V_{DDL} and V_{DDQ} is describing pins **into** the individual SDRAM memory devices, and the three voltages were/are in practice provided from a single power converter. EX2030, 133:5-134:6, 39:11-40:24. Second, Dr. Wolfe’s citation to EX1026, 2-3 (cited at EX1003, ¶ 242) describes what is happening at DRAM device level (“isolated on the device”), not at the memory module level.

EX2031 (918) (Mangione-Smith Declaration), ¶89.
EX2061 (054) (Mangione-Smith Declaration), ¶89.

Patent Owner Response (918) at 24.
Patent Owner Response (054) at 26-27.

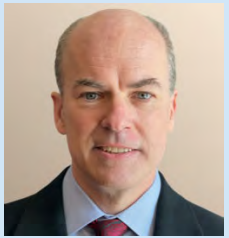
The Experts Agree: The Industry Rejected Using Multiple Converters in FBDIMMs for VDD/VDDQ/VDDL

Andrew Wolfe
Samsung's Expert

SAMSUNG

> Q. As far as you know for the FB-DIMM designs, which option did the designers choose?
>
> A. The unmodified FB-DIMMs that I'm aware of connect VDD, VDDL and VDDQ to a single power converter output.

EX2030 (918) (Wolfe Deposition), 133:5-9.
EX2060 (054) (Wolfe Deposition), 133:5-9.



William Mangione-Smith
Netlist's Expert

NETLIST

> POSITAs consistently supplied all three voltages using a single power converter.

EX2031 (918) (Mangione-Smith Declaration), ¶90.
EX2061 (054) (Mangione-Smith Declaration), ¶90.

Patent Owner Response (918) at 25; Patent Owner Response (054) at 25.
Patent Owner Sur-Reply (918) at 17; Patent Owner Sur-Reply (054) at 18.

The Industry Rejected Using Multiple Converters To Supply VDD/VDDQ/VDDL or VCC/VCCFBD For Good Reasons

Micron

TN-47-05 DDR2 POWER SOLUTIONS FOR NOTEBOOKS
Overview

Technical Note

Power Solutions for DDR2 Notebook PCs

Supply

V_{DD} (V_{DD}, V_{DDL}, V_{DDQ})

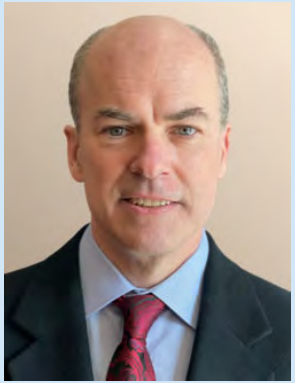
The DDR2 device requires a single power source for primary supply voltages in order to ensure that all voltage levels track each other, especially during the power ramp. At the module level, V_{DD} (device core), V_{DDL} (device DLL), and V_{DDQ} (device I/O) share a single power plane with the interconnecting pins labeled as V_{DD}. Likewise, V_{SS}, V_{SSL}, and V_{SSQ} share a common ground plane labeled as V_{SS}.

The memory supply voltage is specified as $V_{DD} = V_{DDQ} = 1.8V$ with a DC tolerance of ±100mV. DC is defined as any signal ≤20 MHz. At the initial power-up, all supply power should be stable and meet specification within ≤10ms.

EX2006 (Micron Technical Note), 4.

Patent Owner Response (918) at 23-24; Patent Owner Response (054) at 25-26.
Patent Owner Sur-Reply (918) at 17; Patent Owner Sur-Reply (054) at 18.

The Industry Rejected Using Multiple Converters To Supply VDD/VDDQ/VDDL or VCC/VCCFBD For Good Reasons



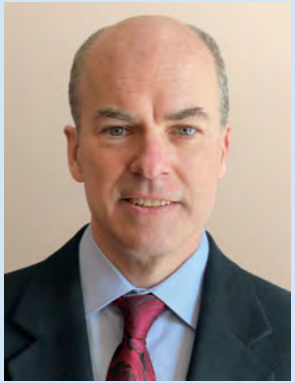
William Mangione-Smith
Netlist's Expert

NETLIST

> 88. It was also generally known that, for the "VDD (VDD, VDDL, VDDQ)" power supply, "[t]he DDR2 device requires a single power source for primary supply voltages in order to ensure that all voltage levels track each other, especially during the power ramp." EX2006 (Micron TN-47-05), 4. It was known that "VDD (device core), VDDL (device DLL), and VDDQ (device I/O) share a single power plane with the interconnecting pins labeled as VDD," and that "[a]t the initial power-up, all supply power should be stable and meet specification within ≤10ms." Id. Meeting such stability and timing specifications is made possible when the voltages (e.g., V_{DD}, V_{DDL} and V_{DDQ}) are driven from a single power converter instead of from separate converters.

EX2031 (918) (Mangione-Smith Declaration), ¶88; EX2061 (054) (Mangione-Smith Declaration), ¶88.
Patent Owner Response (918) at 23-24; Patent Owner Response (054) at 27.
Patent Owner Sur-Reply (918) at 17; Patent Owner Sur-Reply (054) at 18-19.

The Industry Rejected Using Multiple Converters To Supply VDD/VDDQ/VDDL or VCC/VCCFBD For Good Reasons



William Mangione-Smith
Netlist's Expert

NETLIST

> that the timing requirements are met. Independent voltage sources for different voltages would require specific control circuitry to delay and more precisely control each voltage source's ramping rate, adding complexity and cost. The fact is that POSITAs consistently supplied all three voltages using a single power converter. I note that Dr. Wolfe agrees. See EX2030, 133:5-134:6, 39:11-40:24. To me, this is a

EX2031 (918) (Mangione-Smith Declaration), ¶90.
EX2061 (054) (Mangione-Smith Declaration), ¶90.

Patent Owner Response (918) at 25; Patent Owner Response (054) at 28.
Patent Owner Sur-Reply (918) at 17; Patent Owner Sur-Reply (054) at 18.

Petitioner's Evidence of Alleged Motivations to Use Separate Converters Are Untethered to Harris

No evidence of analog voltages

FBDIMM does not run at hundreds of amperes

Many devices share standard voltage levels (such as 3.3 V), while others may require device-specific voltages. In addition, a particular standard voltage level may have to be independently furnished in numerous places. For example, separate analog- and digital supplies, such as 3.3 V_{ANALOG} and 3.3 $V_{DIGITAL}$, may be required. Generating the same voltage numerous times may be necessary to improve efficiency (e.g., memory rails running at hundreds of amperes) or to meet sequencing requirements (3.3 V_A and 3.3 V_B needed by separate devices at different times). All of

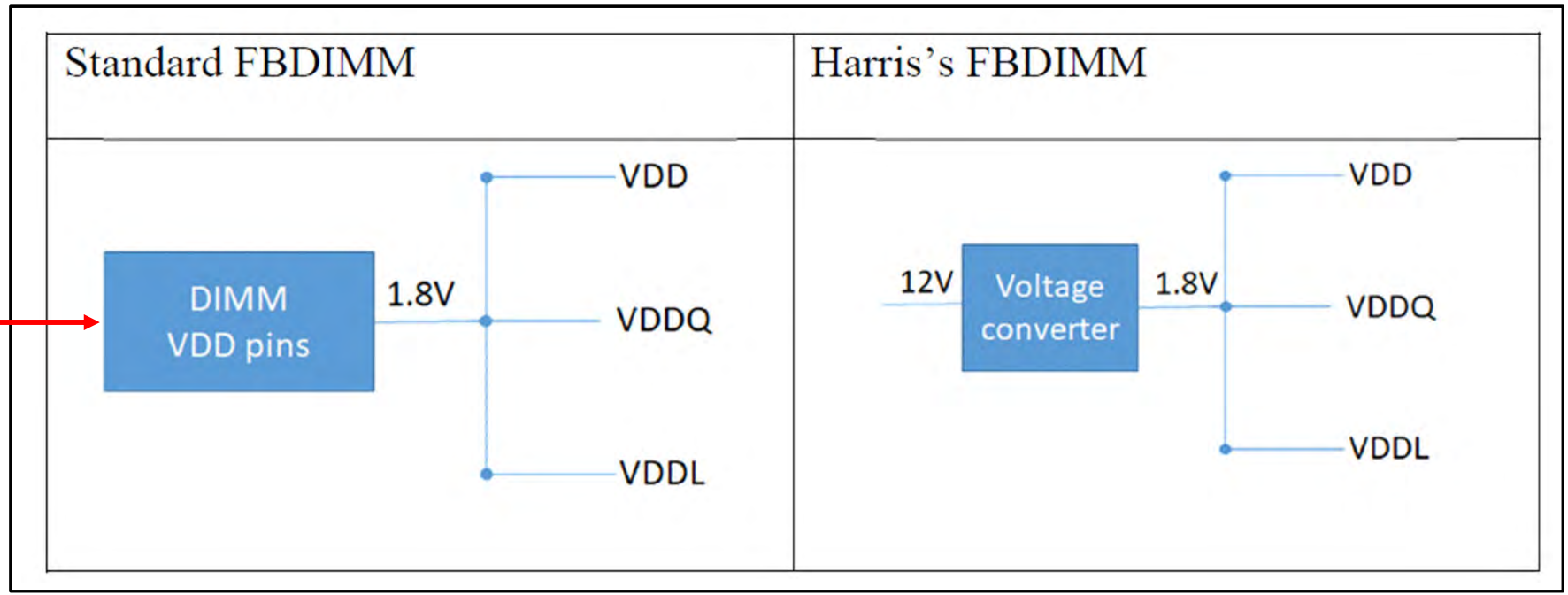
EX1062 (Power-Supply Management—Principles, Problems, and Parts) at 13.

VDD, VDDL, and VDDQ are each supplied to the same devices

Petition (918) at 31.
Petition (054) at 30.

Petitioner Has Not Established A POSITA Would Have Used Separate Buck Converters For VDD/VDDQ/VDDL or VCC/VCCFBD

System-Board-Specific Voltage Level



EX1028, 11.

Patent Owner Sur-Reply (918) at 16.
Patent Owner Sur-Reply (054) at 17.

Petitioner Has Not Established A POSITA Would Have Further Modified Harris+FBDIMM With Separate Buck Converters Given Space Constraints

[0013] It is contemplated that local supply voltage conversion for double-rank DIMMs can be accommodated with a form factor design of approximately about one square inch (both sides of the printed circuit board), and at a component

EX1026 (Harris), [0010].

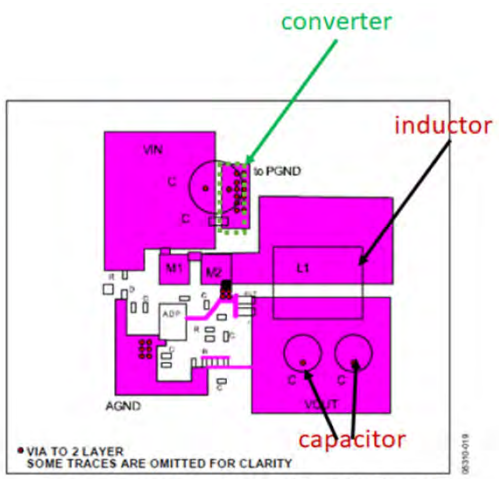
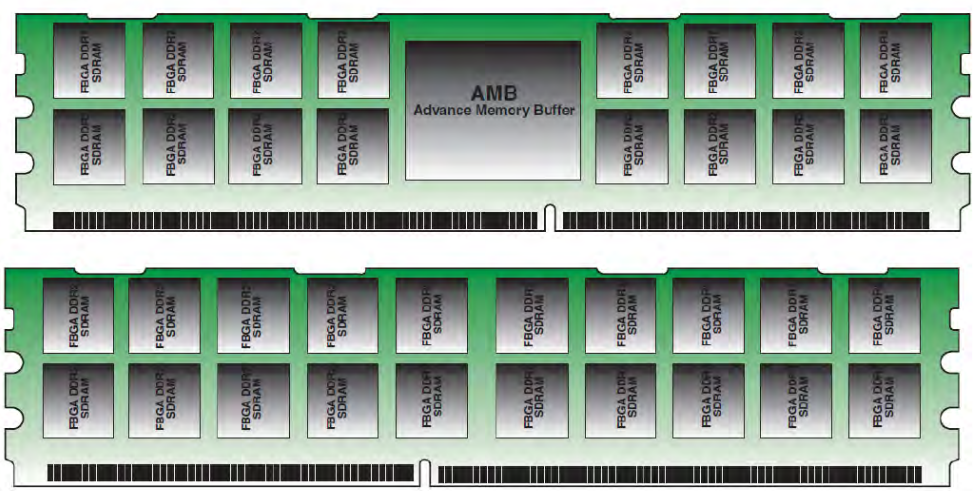


Figure 20. Top Layer Layout Example of Circuit (See Figure 23)

EX1078, 23.

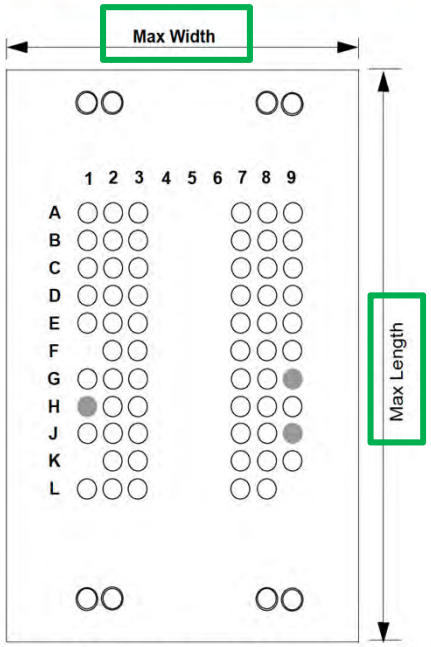
X 4



EX2042, 7.

Patent Owner Response (918) at 20; Patent Owner Response (054) at 22.
Patent Owner Sur-Reply (918) at 12; Patent Owner Sur-Reply (054) at 13.

FBDIMM Form Factor



Note: Double circles indicate the location of support balls of Variation DM-z
Gray circles indicate the balls for stacked only

Component Details

Supported SDRAM Component Maximum size for 256Mb to 4Gb, DDR2 SDRAM

Raw Card	Package Type	Supported DRAM Outline (Width x Length) max. (mm)			
		MO-207 Variation			
		DJ-z (60 pins)	DM-z (68 pins)	DL-z (92 pins)	DK-z (84 pins)
A	Planar	12.4 x 15	12.4 x 18	12.4 x 21	12.4 x 21
B,C	Planar	11.4 [2] (12.4 [1,2]) x 15	11.4 [2] (12.4 [1,2]) x 18	11.4 [2] (12.4 [1,2]) x 21[3]	11.4 [2] (12.4 [1,2]) x 21
E	Planar	11 x 11.5	--	--	--
H	Planar	12[4] x 11	--	--	--
		MO-242 Variation			
		AA (63 pins)	AD (71 pins)	AC (95 pins)	AB (87 pins)
D,J	Stacked	11.4 [2] (12.4 [1,2]) x 15	11.4 [2] (12.4 [1,2]) x 18	11.4 [2] (12.4 [1,2]) x 21[3]	11.4 [2] (12.4 [1,2]) x 21

1. supported only if no-decoupling capacitor are placed in between the DRAMs
2. 0.4 mm DRAM to DRAM spacing
3 Heat sink attachment may modify the max DRAM length that will fit to 18.6mm
4. Heat sink attachment may modify the max DRAM width that will fit to 11.5mm

5	Module Physical Attribues	30~35mm height 8~9mm thick	0x24	

Petition (918) at 11; Petition (054) at 10-11.
EX1028 (918, 054) at 25-26, 105.

The 918 Petition

Voltage mappings that require using separate converters for the same voltage level under Petitioner's theory

	Voltage Mappings (Grounds 1-3)		
	A	B	C
"first":	V_{DD} or V_{DDQ} = 1.8V	V_{DD}, V_{DDQ}, or V_{DDL} = 1.8V	V_{DD}, V_{DDQ}, or V_{DDL} = 1.8V
"second":	V_{CC} or V_{CCFBD} = 1.5V	V_{CC} = 1.5V	V_{CC} or V_{CCFBD} = 1.5V
"third":	V_{DDL} = 1.8V	V_{CCFBD} = 1.5V	V_{TT} = 0.9V
"fourth":	V_{DDSPD} = 3.3V	V_{DDSPD} = 3.3V	V_{DDSPD} = 3.3V

Petition (918) at 26.

The 054 Petition

Voltage mappings that require using separate converters for the same voltage level under Petitioner's theory

	Voltage Mappings (Grounds 1-3)		
	A	B	C
"first":	V_{DD} or V_{DDQ} = 1.8V	V_{DD} or V_{DDQ} = 1.8V	V_{DD} or V_{DDQ} = 1.8V
"second":	V_{CC} or V_{CCFBD} = 1.5V	V_{CC}=1.5V	V_{CC} or V_{CCFBD} = 1.5V
"third":	V_{DDL}=1.8V	V_{CCFBD}=1.5V	V_{TT}=0.9V

Petition (054) at 27.

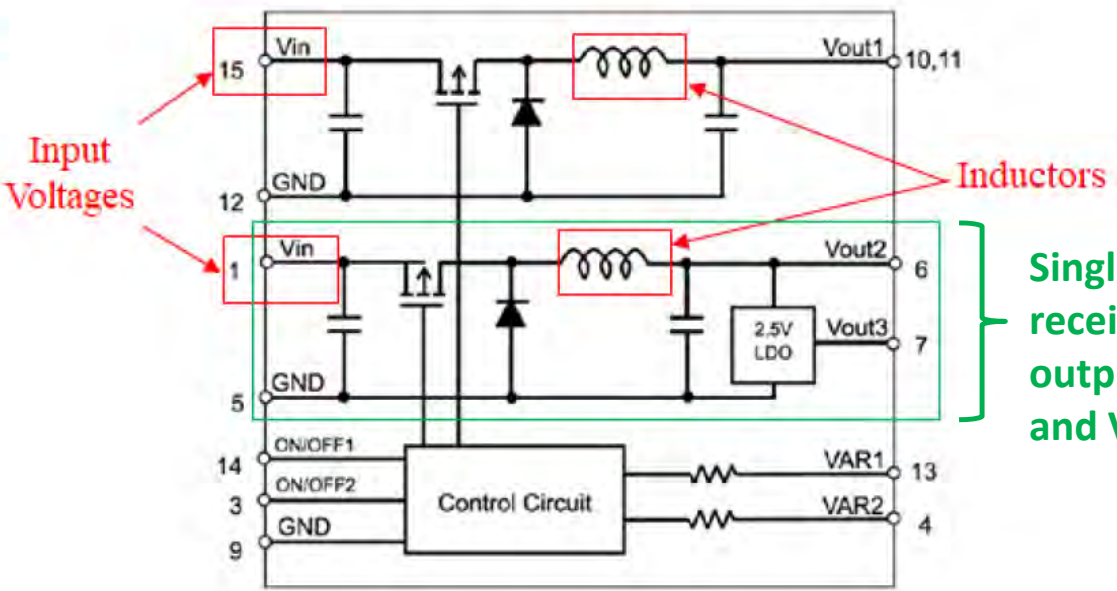
Petitioner's Own Evidence Shows that Single Buck Converter Outputting Multiple Voltages Were Known

5. Pin Number and Function

Pin No.	Function
1.	Vin
2.	N.C.(Internally Used)
3.	ON/OFF2
4.	VAR2
5.	GND
6.	Vout2(1.8V-3.6V)
7.	Vout3(2.5V)

DC-DC Converter Specification(DRAFT)

MPD4S014S



Single buck converter receiving only Vin (1) and outputting different Vout2 and Vout3

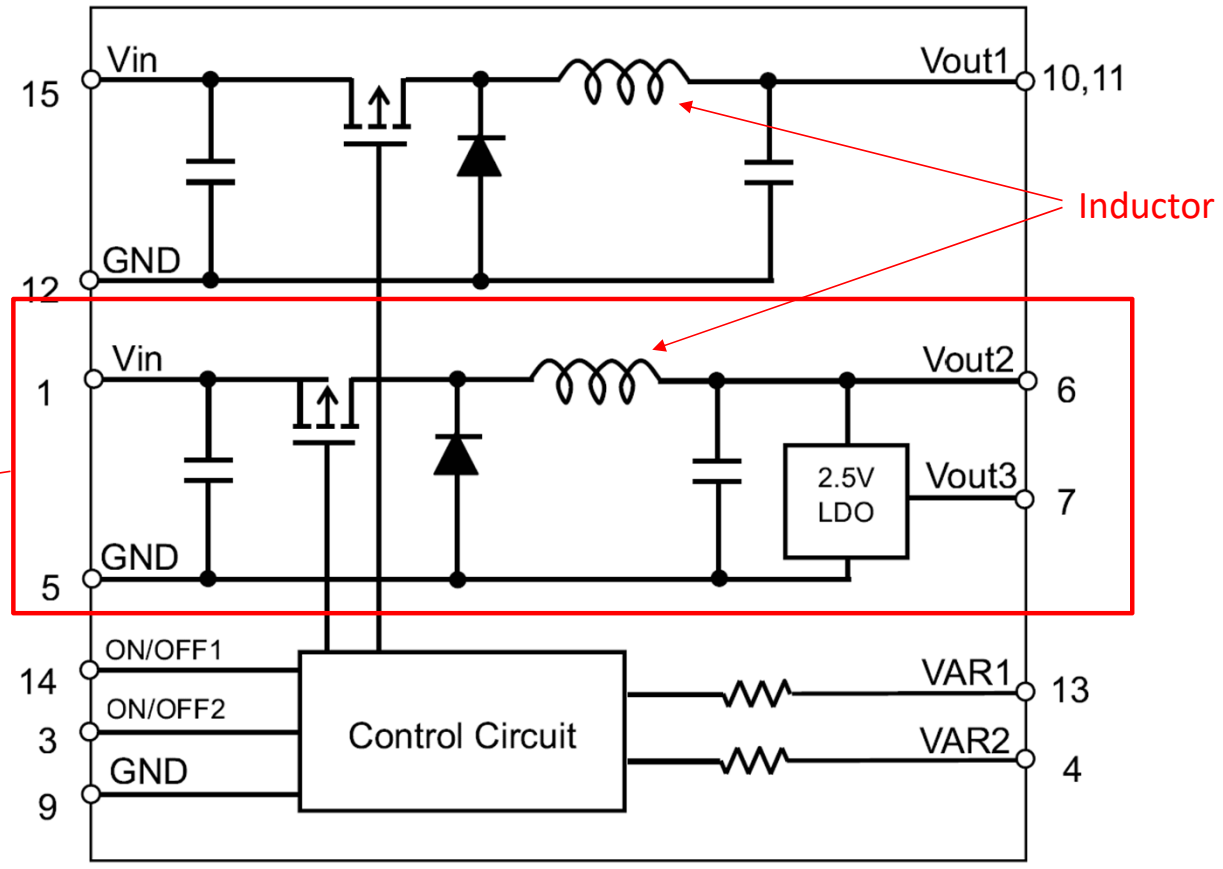
EX1048, 2 (annotated).

Patent Owner Sur-Reply (918) at 14; Patent Owner Sur-Reply (054) at 15.
Patent Owner Response (918) at 18; Patent Owner Response (054) at 20-21.

What Defines a Buck Converter

A buck converter needs “an LC-filter just after the power switch ….” EX2020, p.22. Thus, the number of inductors reflects the number of buck converters.

See EX1078, 12 (LC filter); EX1075, 129:13-19.



EX1048, 2 (shows two buck converters, each with its own inductor).

Patent Owner Sur-Reply (918) at 14.
Patent Owner Sur-Reply (054) at 15.

Single Buck Converters Can Generate Multiple Voltages

24.6 A 4-Output Single-Inductor DC-DC Buck Converter with Self-Boosted Switch Drivers and 1.2A Total Output Current

M. Belloni[1], E. Bonizzoni[1], E. Kiseliovas[2], P. Malcovati[1], F. Maloberti[1], T. Peltola[2], T. Teppo[2]

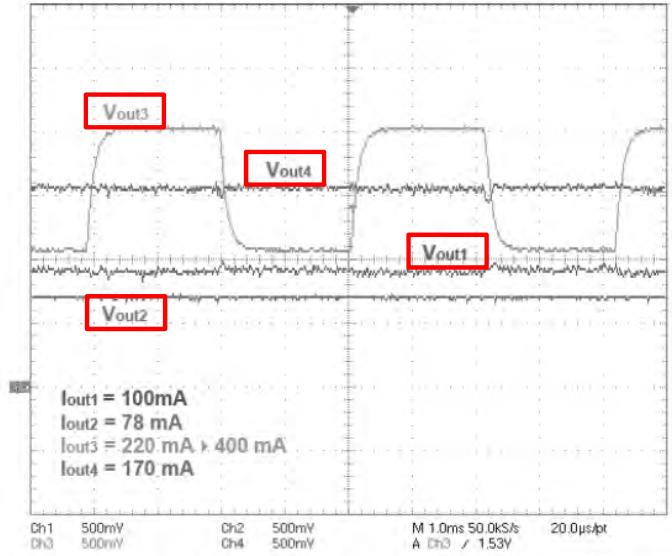


Figure 24.6.5: Measured regulated output voltages (V_{out1} = 0.9V ch. 1, V_{out2} = 0.7V ch. 2, V_{out3} = 1.1 to 2V ch. 3, V_{out4} = 1.6V ch. 4)

EX2003 at 2.

Single-Inductor Multiple-Output Switching Converters With Time-Multiplexing Control in Discontinuous Conduction Mode

Dongsheng Ma, *Student Member, IEEE*, Wing-Hung Ki, *Member, IEEE*, Chi-Ying Tsui, *Member, IEEE*, and Philip K. T. Mok, *Senior Member, IEEE*

TABLE II
PERFORMANCE SUMMARY

Supply voltage range	1.3~2.85V
Inductor	1μH (nominal)
Oscillator frequency	1MHz (nominal)
Chip area	2.4mm^2
Process	0.5μm CMOS, n-well, 3AL, 1PS
Output voltages	3.0V, 3.6V

EX2004 at 99 (pdf page 11).

Patent Owner Sur-Reply (918) at 14; Patent Owner Sur-Reply (054) at 15.
Patent Owner Response (918) at 18; Patent Owner Response (054) at 21.

Evidence of Multi-Converter Chips Cited By Petitioner

ANALOG DEVICES

Step-Down DC-to-DC Controller

ADP1821

FEATURES

Wide power-input voltage range: 1 V to 24 V
Chip supply voltage range: 3.7 V to 5.5 V
Wide output voltage range: 0.6 V to 85% of input voltage
1% accuracy, 0.6 V reference voltage
All N-channel MOSFET design for low cost
Fixed-frequency operation 300 kHz, 600 kHz, or synchronized operation up to 1.2 MHz
No current sense resistor required
Power-good output
Programmable soft start with reverse current protection
Soft start, thermal overload, current-limit protection
Undervoltage lockout
10 µA shutdown supply current
Small, 16-lead QSOP

APPLICATIONS

Telecommunications and networking systems
Set-top boxes
Printers
Servers
Medical imaging systems
Microprocessor and DSP core power supplies
Mobile communication base stations

GENERAL DESCRIPTION

The ADP1821 is a versatile and inexpensive, synchronous, pulse-width-modulated (PWM), voltage-mode, step-down controller. It drives an all N-channel power stage to regulate an output voltage as low as 0.6 V. The ADP1821 can be configured to provide output voltages from 0.6 V to 85% of the input voltage and is sized to handle large MOSFETs for point-of-load regulators.

The ADP1821 is well suited for a wide range of high power applications, such as DSP and processor core power in telecommunications, medical imaging, high performance servers, and industrial applications. It operates from a 3.7 V to 5.5 V supply with a power input voltage ranging from 1.0 V to 24 V.

The ADP1821 operates at a pin-selectable, fixed switching frequency of either 300 kHz or 600 kHz, minimizing external component size and cost. For noise sensitive applications, it can be synchronized to an external clock to achieve switching frequencies between 300 kHz and 1.2 MHz. The ADP1821 includes soft start protection to limit the inrush current from the input supply during startup, reverse current protection during soft start for precharged outputs, as well as a unique adjustable lossless current-limit scheme utilizing external MOSFET sensing.

The ADP1821 operates over the –40°C to +125°C junction temperature range and is available in a 16-lead QSOP.

EX1078, at 1.
Patent Owner's Sur-Reply (918) at 12-13; Patent Owner's Sur-Reply (054) at 12-13.

Harris Expressly Discloses Using a Single Converter to Provide Multiple Voltages

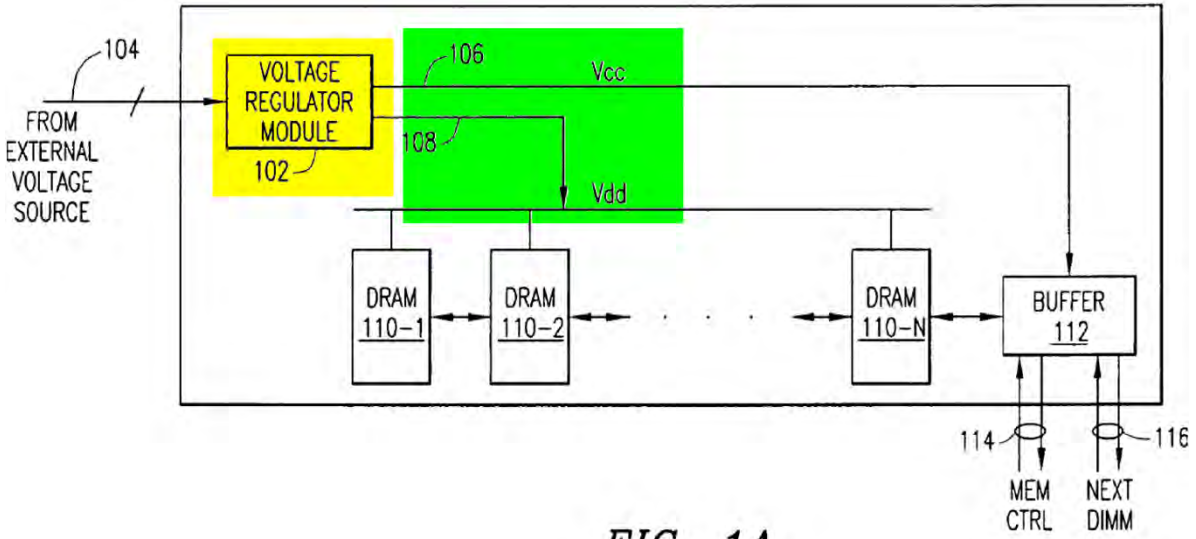


FIG. 1A

respectively. Preferably, a high-frequency switching voltage converter capable of generating tightly-controlled voltage levels may be implemented as the on-board VRM **102** for purposes of the present patent disclosure. For instance,

EX1023 (Harris), [0010].

Patent Owner Response (918) at 17.
Patent Owner Response (054) at 20.

In Netlist Patents A Dual Buck Converter Has Two Buck Converters

1. A memory module comprising:

a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;

a first buck converter configured to provide a first regulated voltage having a first voltage amplitude;

a second buck converter configured to provide a second regulated voltage having a second voltage amplitude;

a third buck converter configured to provide a third regulated voltage having a third voltage amplitude;

a converter circuit configured to provide a fourth regulated voltage having a fourth voltage amplitude; and

a plurality of components coupled to the PCB, each component of the plurality of components coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages, the plurality of components comprising:

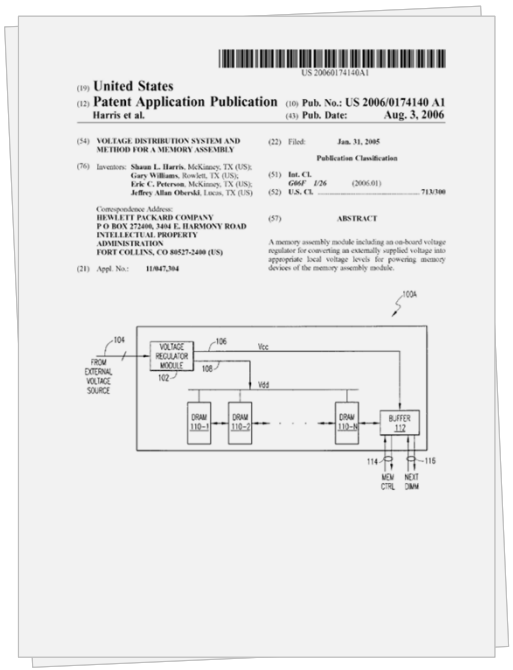
a plurality of synchronous dynamic random access memory (SDRAM) devices coupled to the first regulated voltage, and

at least one circuit coupled between a first portion of the plurality of edge connections and the plurality of SDRAM devices, the at least one circuit operable to (i) receive a first plurality of address and control signals via the first portion of the plurality of edge connections, and (ii) output a second plurality of address and control signals to the plurality of SDRAM devices, the at least one circuit coupled to both the second regulated voltage and the fourth regulated voltage, wherein a first one of the second and fourth voltage amplitudes is less than a second one of the second and fourth voltage amplitudes.

2. The memory module of claim 1, wherein the first and third buck converters are further configured to operate as a dual buck converter.

Patent Owner's Sur-Reply (918) at 13.
EX1001 (918) at 38:25, 38:29, 38:53-55.

Harris' Claims Confirm a Single Module Can Supply Multiple Voltages



US 20060174140A1

(19) United States

(12) Patent Application Publication (10) Pub. No.: US 2006/0174140 A1

Harris et al. (43) Pub. Date: Aug. 3, 2006

(54) VOLTAGE DISTRIBUTION SYSTEM AND METHOD FOR A MEMORY ASSEMBLY

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(21) Appl. No.: 11/047,304

(22) Filed: Jan. 31, 2005

Publication Classification

(51) Int. Cl.
G06F 1/26 (2006.01)

(52) U.S. Cl. 713/300

(57) ABSTRACT

A memory assembly module including an on-board voltage regulator for converting an externally supplied voltage into appropriate local voltage levels for powering memory devices of the memory assembly module.

What is claimed is:

1. A memory board assembly, comprising:

a plurality of memory devices, each receiving a first voltage path;

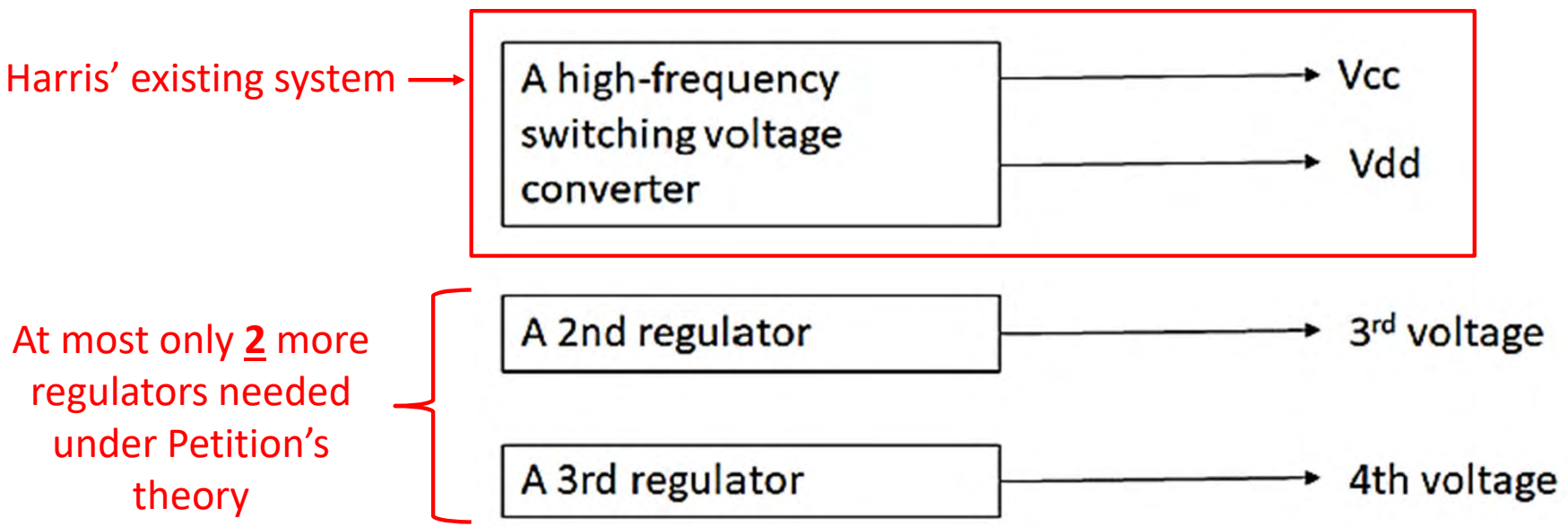
a buffer for buffering data in at least a portion of said plurality of memory devices, said buffer receiving a second voltage path and a bidirectional memory controller path; and

at least one voltage regulator module for converting an externally supplied voltage level into appropriate voltage levels that power said first and second voltage paths, respectively.

EX1023 (Harris), Claim 1.

Absent Further Modification, Harris+FBDIMM Would Not Use Separate Converters For Each Voltage

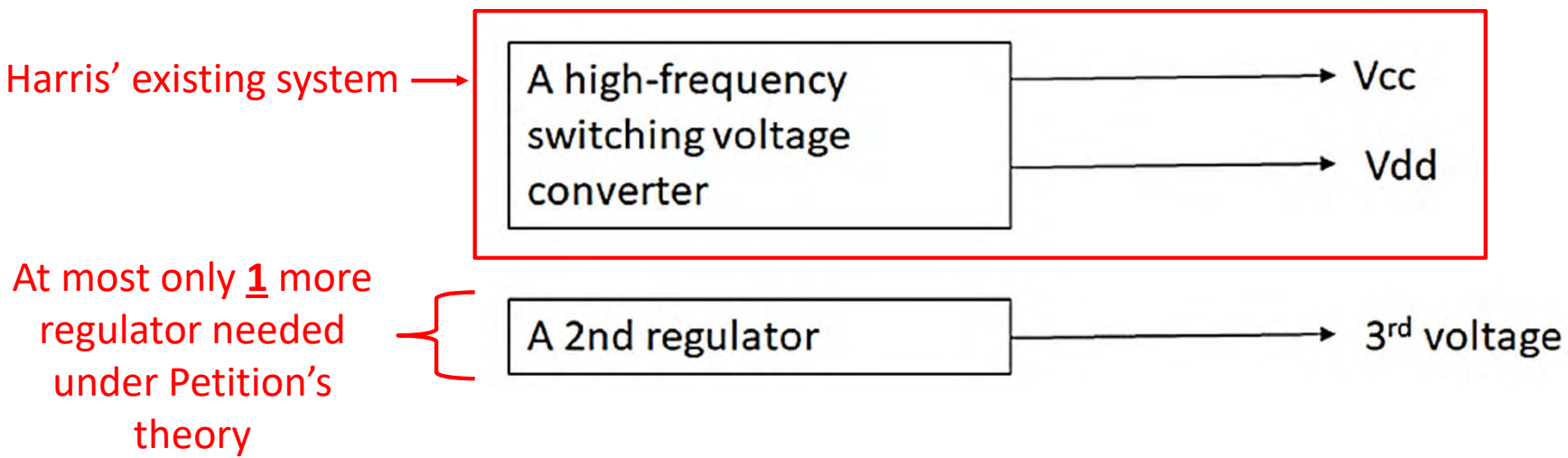
'918 IPR



Patent Owner Response (918) at 18.

Absent Further Modification, Harris+FBDIMM Would Not Use Separate Converters For Each Voltage

'054 IPR



Patent Owner Response (054) at 21.

Voltage Mapping C Fails: Harris Does Not Generate VTT On-Module And A POSA Would Not Be Motivated to Modify Harris To Do So

The 918 Petition

	Voltage Mappings (Grounds 1-3)		
	A	B	C
"*first*":	V_{DD} or V_{DDQ} = 1.8V	V_{DD}, V_{DDQ}, or V_{DDL} = 1.8V	V_{DD}, V_{DDQ}, or V_{DDL} = 1.8V
"*second*":	V_{CC} or V_{CCFBD} = 1.5V	V_{CC}=1.5V	V_{CC} or V_{CCFBD} = 1.5V
"*third*":	V_{DDL}=1.8V	V_{CCFBD}=1.5V	V_{TT}=0.9V
"*fourth*":	V_{DDSPD}=3.3V	V_{DDSPD}=3.3V	V_{DDSPD}=3.3V

Petition (918) at 26.

Voltage Mapping C Fails: Harris Does Not Generate VTT On-Module And A POSA Would Not Be Motivated to Modify Harris To Do So

The 054 Petition

	Voltage Mappings (Grounds 1-3)		
	A	B	C
"first":	V_{DD} or V_{DDQ} = 1.8V	V_{DD} or V_{DDQ} = 1.8V	V_{DD} or V_{DDQ} = 1.8V
"second":	V_{CC} or V_{CCFBD} = 1.5V	V_{CC}=1.5V	V_{CC} or V_{CCFBD} = 1.5V
"third":	V_{DDL}=1.8V	V_{CCFBD}=1.5V	V_{TT}=0.9V

Petition (054) at 27.

Harris Does Not Teach Or Suggest Generating VTT On-Module

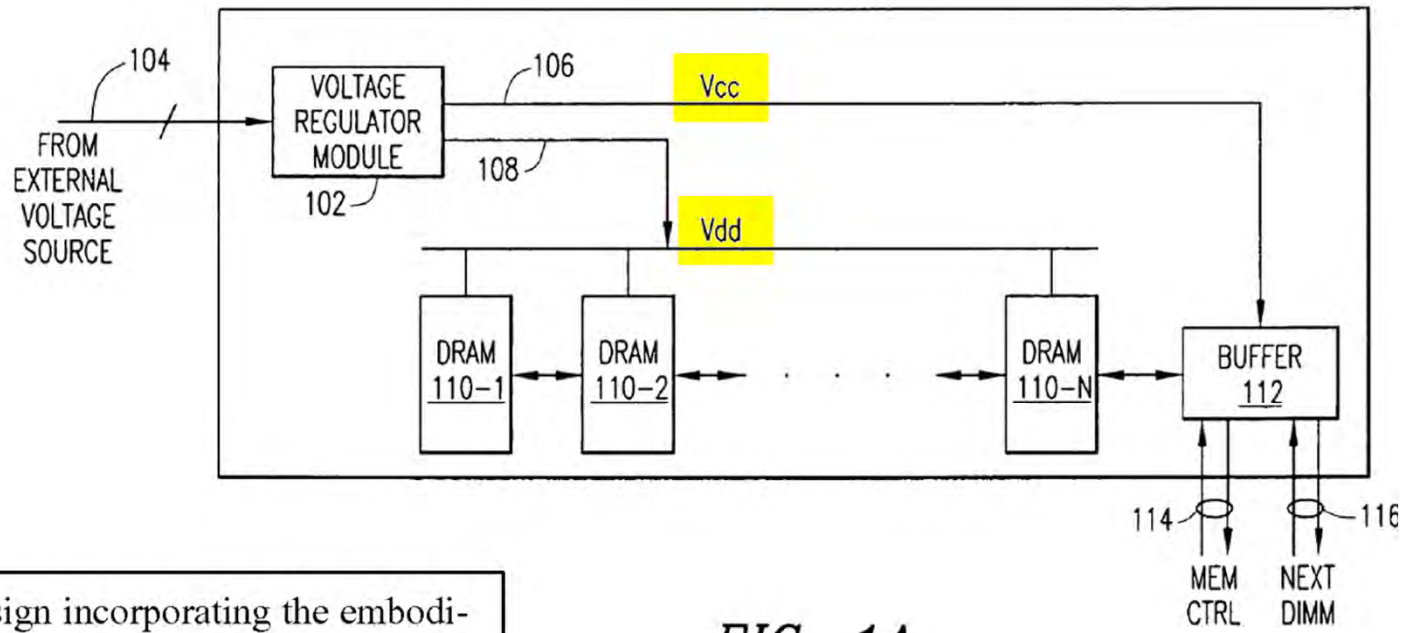


FIG. 1A

EX1023 (Harris), FIG. 1A.

voltage-independent FBD design incorporating the embodiment of **FIG. 1A** is capable of replacing these power supply interface pins with as few as six +12V pins (from an external voltage source), with local conversion to V_{dd} (to DRAM) and V_{cc} (to buffer/logic) being added. Alternatively, using

EX1023 (Harris), [0012].

Patent Owner Sur-Reply (918) at 17-18.
Patent Owner Sur-Reply (054) at 19-20.

Vtt Is Never Supplied to DRAM

Harris Proposes On Module Vdd to DRAM

[0012] By way of example, a standard FBD module requires 28 V_{dd} pins (for DRAM devices) and 8 V_{cc} pins (for buffer and logic) and associated Ground returns, resulting in a total of 72 pins that provide a power supply interface for up to two x4 DRAM ranks (36 devices) and buffer logic. A voltage-independent FBD design incorporating the embodiment of **FIG. 1A** is capable of replacing these power supply interface pins with as few as six +12V pins (from an external voltage source), with local conversion to V_{dd} (to DRAM) and V_{cc} (to buffer/logic) being added. Alternatively, using additional power supply pins would provide the capability to support even more devices. For instance, with 12 supply pins (at +12V), the embodiment of **FIG. 1A** can provide enough power to supply 4 ranks (i.e., 72 devices). Likewise, a memory assembly of 8 ranks (144 devices) may be powered with 24 pins at +12V.

EX1023 (Harris), [0009].

DRAM does not receive Vtt

1.1 DDR2 SDRAM package ballout

(Top view: see balls through package)

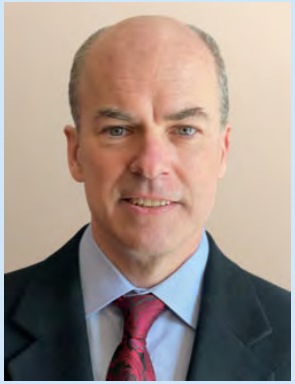
	1	2	3	4	5	6	7	8	9	
	NC	NC						NC	NC	A
										B
										C
										D
Variation DJ-z without support balls	VDD	NC	VSS				VSSQ	$\overline{DQS}$	VDDQ	E
	NC	VSSQ	DM				DQS	VSSQ	NC	F
	VDDQ	DQ1	VDDQ				VDDQ	DQ0	VDDQ	G
	NC	VSSQ	DQ3				DQ2	VSSQ	NC	H
	VDDL	VREF	VSS				VSSDL	CK	VDD	J
		CKE	$\overline{WE}$				$\overline{RAS}$	$\overline{CK}$	ODT	K
	NC, BA2	BA0	BA1				$\overline{CAS}$	$\overline{CS}$		L
		A10/AP	A1				A2	A0	VDD	M
	VSS	A3	A5				A6	A4		N
		A7	A9				A11	A8	VSS	P
	VDD	A12	NC, A14				NC, A15	NC, A13		R
										T
										U
										V
	NC	NC						NC	NC	W

Variation DM-z with support balls

EX1026 (DDR2 SDRAM), at 1.

Patent Owner Response (918) at 52.
Patent Owner Response (054) at 55-56.

A POSA Would Have Had Specific Reasons Not to Generate VTT On-Module



William Mangione-Smith
Netlist's Expert

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"[S]upplying VTT from the motherboard would ensure that all DIMMs connected to the same memory controller would have the same termination voltages …. This would also ***eliminate undesirable ground loops*** between the DIMMs, on the one hand, and between the DIMM and the motherboard, on the other hand."

EX2031 (918) (Mangione-Smith Declaration), ¶96.
EX2061 (054) (Mangione-Smith Declaration), ¶96.

"VTT supply must sink and source current…. The design complexity would favor having a single regulator for a group of DIMMs rather than one regulator per DIMM."

EX2031 (918) (Mangione-Smith Declaration), ¶97.
EX2061 (054) (Mangione-Smith Declaration), ¶97.

Patent Owner Response (918) at 28.
Patent Owner Response (054) at 31-32.

Table 16 — Recommended DC operating conditions (SSTL_1.8)

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.7	1.8	1.9	V	1
VDDL	Supply Voltage for DLL	1.7	1.8	1.9	V	5
VDDQ	Supply Voltage for Output	1.7	1.8	1.9	V	1, 5
VREF	Input Reference Voltage	0.49*VDDQ	0.50*VDDQ	0.51*VDDQ	mV	2. 3
VTT	Termination Voltage	VREF-0.04	VREF	VREF+0.04	V	4

NOTE 1 There is no specific device VDD supply voltage requirement for SSTL-1.8 compliance. However under all conditions VDDQ must be less than or equal to VDD.
NOTE 2 The value of VREF may be selected by the user to provide optimum noise margin in the system. Typically the value of VREF is expected to be about 0.5 x VDDQ of the transmitting device and VREF is expected to track variations in VDDQ.
NOTE 3 Peak to peak ac noise on VREF may not exceed +/-2% VREF (dc).
NOTE 4 VTT of transmitting device must track VREF of receiving device.
NOTE 5 VDDQ tracks with VDD, VDDL tracks with VDD. AC parameters are measured with VDD, VDDQ and VDDDL tied together

EX1026, at 49

Patent Owner Response (918) at 52.
Patent Owner Response (054) at 55-56.

A POSA Would Not Generate VTT Using A Buck Converter

VTT was typically generated by an LDO

Micron

TN-47-05 DDR2 POWER SOLUTIONS FOR NOTEBOOKS
Overview

Technical Note

Power Solutions for DDR2 Notebook PCs

TPS51116: A Solution for Complete DDR2 Power Management

Figure 6 on page 8 shows a typical application schematic for the TPS51116 and how it integrates into the complete DDR2 power-management solution with:

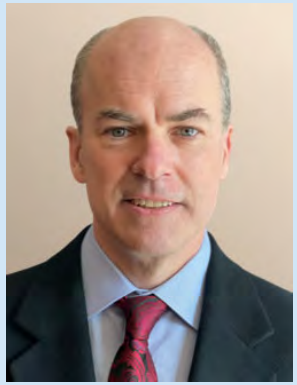
- Synchronous current mode DC/DC controller to power V_{DD}
- Buffered reference to provide V_{REF} (V_{REF} tracks one-half V_{DD})
- 3A sink/source LDO to power V_{TT} (V_{TT} tracks V_{REF})
- S3/S5 sleep-state controls

EX2006 (Micron Technical Note), at 7.

See also EX2007-2010, EX2050 (linear VTT regulators that generate VTT from VDDQ).

Patent Owner Response (918) at 29-30.
Patent Owner Response (054) at 32-33.

There Are Specific Reasons To Use An LDO To Generate VTT



William Mangione-Smith
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> regulators that generate V_{TT} from VDDQ). Indeed, LDOs are much smaller than buck converters, which requires a controller and discrete components including a larger inductor. This makes an LDO preferable in space constrained environments. LDO are also preferred when the current load is below 1A. See EX2047 [SMTsg5127fb225652] at 21 (V_{TT} current is typically 500mA and no more than 700mA); EX0248 [MT18HTF1282FDY], p.23 (same); EX2049 [SS_143851], 20 (same); EX1040, pp.23-24, Figs.22-25 (efficiency decreases at lower currents and lower output voltage).

EX2031 (918) (Mangione-Smith Declaration), ¶99.
EX2061 (054) (Mangione-Smith Declaration), ¶99.

Patent Owner Response (918) at 29-30.
Patent Owner Response (054) at 32-33.

Petitioner's VTT Examples Are For On Board Termination

TEXAS INSTRUMENTS

TPS51020

SLUS564B – JULY 2003 – REVISED DECEMBER 2003

DUAL, VOLTAGE MODE, DDR SELECTABLE, SYNCHRONOUS, STEP-DOWN CONTROLLER FOR NOTEBOOK SYSTEM POWER

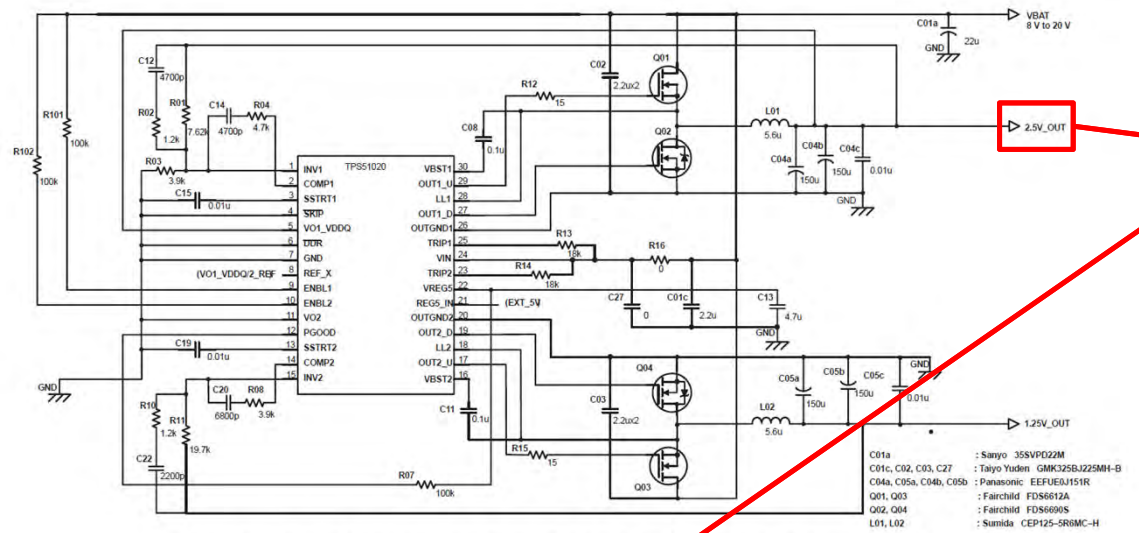


Figure 6. Typical Application Circuit: DDR(2.5V/6A + 1.25V/6A) from VBAT

VDDQ of 2.5V is for DDR1*

*EX1003 (918) Wolfe Decl., ¶139
EX1003 (054) Wolfe Decl., ¶140

Patent Owner Response (918) at 40.
Patent Owner Response (054) at 42.
Patent Owner Sur-Reply (918) at 30.
Patent Owner Sur-Reply (054) at 30-31.

EX1040, p. 18

Petitioner's VTT Examples Are For On Board Termination

FAIRCHILD SEMICONDUCTOR®

FAN5026
Dual DDR/Dual-Output PWM Controller

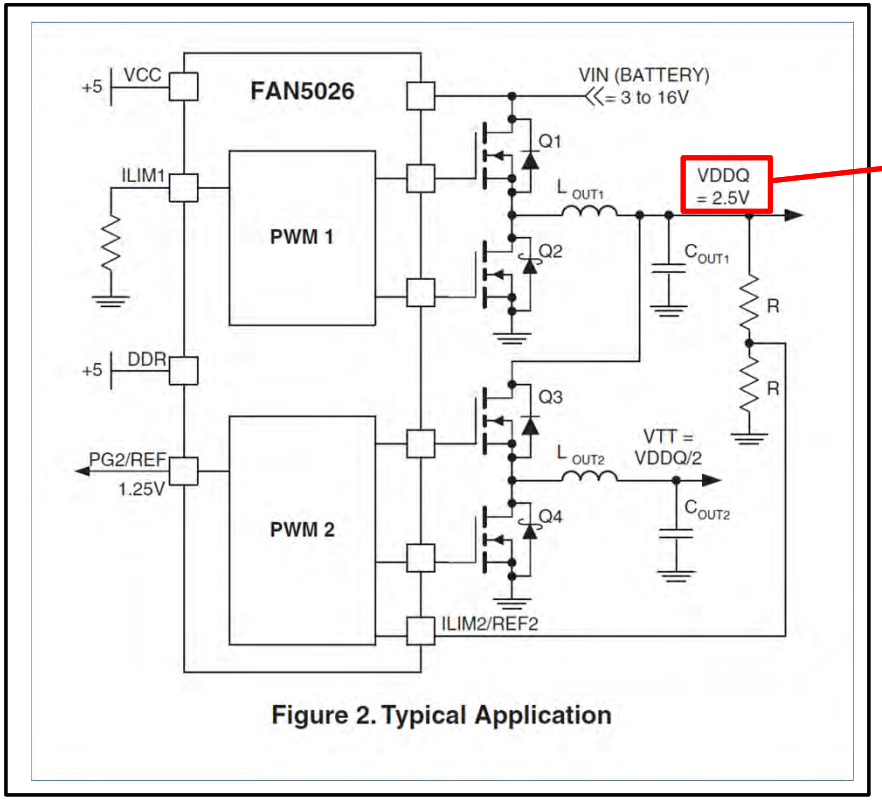


Figure 2. Typical Application

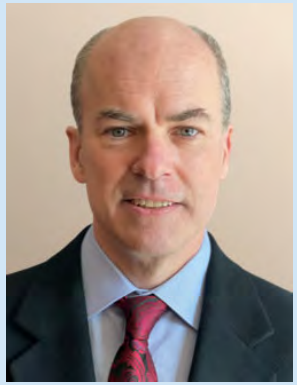
EX1041, p. 2

VDDQ of 2.5V is for DDR1*

*EX1003 (918) Wolfe Decl., ¶139
EX1003 (054) Wolfe Decl., ¶140

Patent Owner Response (918) at 40; Patent Owner Response (054) at 42.
Patent Owner Sur-Reply (918) at 30; Patent Owner Sur-Reply (054) at 30-31.

EX1040 and EX1041 Do Not Suggest Using Buck Converters in FBDIMMs



William Mangione-Smith
Netlist's Expert

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> 100. Dr. Wolfe relies on EX1040 and EX1041 as evidence that buck converters were used to generate V_{TT}. EX1003, ¶¶ 340-341. I have confirmed that Figures 6-7 of Exhibit 1040 and Figures 2 and 4 of Exhibit 1041 depict generation of V_{DDQ} and V_{TT} of DDR1, not DDR2. Unlike DDR2, DDR1 uses motherboard termination, and no on-die termination. EX2012, 71. Hence, DDR1 termination involves higher current, which might have made a buck converter more suitable.

EX2031 (918) (Mangione-Smith Declaration), ¶100.
EX2061 (054) (Mangione-Smith Declaration), ¶100.

Patent Owner Sur-Reply (918) at 18.
Patent Owner Sur-Reply (054) at 19-20.

A POSA Would Not Use a Separate On Module Converter For VDDSPD

The 918 Petition

	Voltage Mappings (Grounds 1-3)		
	A	B	C
"first":	V_{DD} or V_{DDQ} = 1.8V	V_{DD}, V_{DDQ}, or V_{DDL} = 1.8V	V_{DD}, V_{DDQ}, or V_{DDL} = 1.8V
"second":	V_{CC} or V_{CCFBD} = 1.5V	V_{CC}=1.5V	V_{CC} or V_{CCFBD} = 1.5V
"third":	V_{DDL}=1.8V	V_{CCFBD}=1.5V	V_{TT}=0.9V
"fourth":	V_{DDSPD}=3.3V	V_{DDSPD}=3.3V	V_{DDSPD}=3.3V

Petition (918) at 26.

Harris Does Not Teach Or Suggest Generating VDDSPD Using Separate Regulator

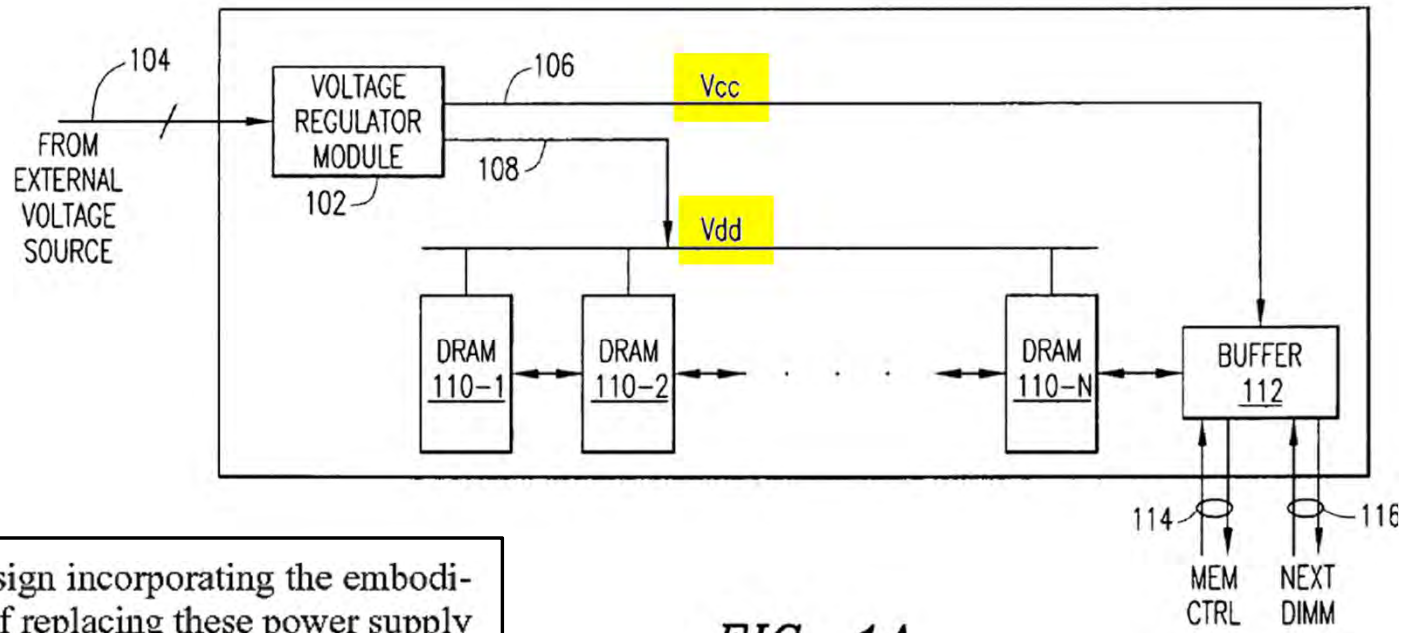


FIG. 1A

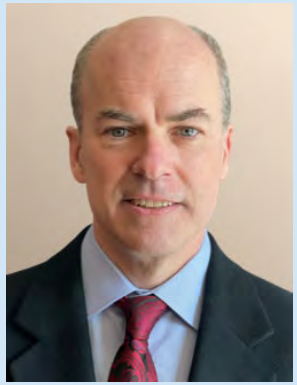
EX1023 (Harris), FIG. 1A.

voltage-independent FBD design incorporating the embodiment of **FIG. 1A** is capable of replacing these power supply interface pins with as few as six +12V pins (from an external voltage source), with local conversion to V_{dd} (to DRAM) and V_{cc} (to buffer/logic) being added. Alternatively, using

EX1023 (Harris), [0012].

Patent Owner Sur-Reply (918) at 17-18.
Patent Owner Sur-Reply (054) at 19-20.

3.3V Is a Standard Power Rail Available On System Boards



William Mangione-Smith
Netlist's Expert

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- "3.3V is a common power rail on the motherboard such that it can be supplied to FBDIMMs without the increased cost and problems associated with providing a regulator for each of Harris' modified FBDIMM memory boards" EX2031, ¶102.

Table 5. Typical Power Distribution for a 350 W ATX12V Configuration

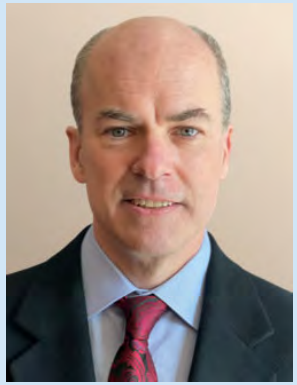
Output	Min. Current (amps)	Max. Current (amps)	Peak Current (amps)
+12 V1DC(1)	1	10	11
+12 V2DC(1, 2)	1	13	16.5
+5 VDC	0.3	12	
+3.3 VDC	0.5	20	
-12 VDC	0.0	0.3	
+5 VSB	0.0	2.5	3.5

Note: Total combined output of 3.3 V and 5 V is ≤ 130 W
Peak currents may last up to 17 seconds with not more than one occurrence per minute
(1)12V1DC and 12V2DC should have separate current limit circuits to meet 240VA safety requirements.
(2)12V2DC supports processor power requirements and must have a separate current limit and provide 16.5A peak current for 10 ms; minimum voltage during peak is > 11.0 VDC

EX2038 Intel System Board, at 17

Patent Owner Response (918) at 30-31.

Single SMBus on System Board Used for All SPDS on all FBDIMMs



William Mangione-Smith
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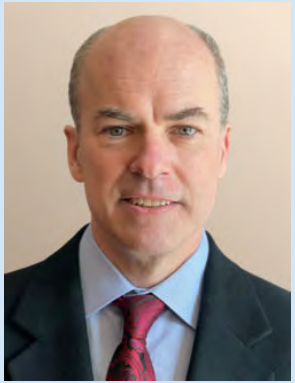
- "[I]f VDDSPD voltages are supplied by different regulators to the SMBus controller on the motherboard and individual DIMMs, they cannot track each other and would lead to communication problems when they are actually at different voltage potentials." EX2031, ¶102.

Patent Owner Response (918) at 30-31. DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

A POSA Would Not Use An On-Module Buck Converter To Generate VDDSPD



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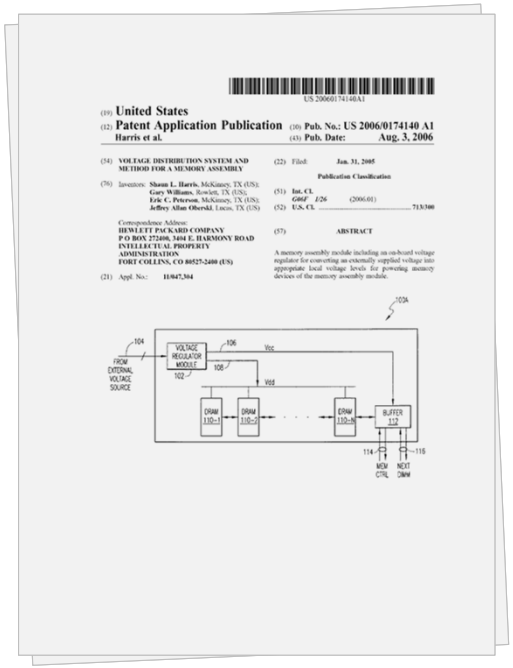
- "[T]he low current level required by components using VDDSPD means that buck converters would be very inefficient." EX2031, ¶103.
- Buck converter: "efficiency less than 20% at 10mA current"
- LDO: "An LDO with a12V-input-3.3V-output would be 26% efficient."

Patent Owner Response (918) at 30-31. DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Use of Buck Converters Is Entirely Hindsight



US 20060174140A1

(19) United States

(12) Patent Application Publication (10) Pub. No.: US 2006/0174140 A1

Harris et al. (43) Pub. Date: Aug. 3, 2006

(54) VOLTAGE DISTRIBUTION SYSTEM AND METHOD FOR A MEMORY ASSEMBLY

(76) Inventors: Shaun L. Harris, McKinney, TX (US); Gary Williams, Rowlett, TX (US); Eric C. Peterson, McKinney, TX (US); Jeffrey Allan Obersld, Lucas, TX (US)

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P O BOX 272400, 3404 E. HARMONY ROAD
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(21) Appl. No.: 11/047,304

(22) Filed: Jan. 31, 2005

Publication Classification

(51) Int. Cl.
G06F 1/26 (2006.01)

(52) U.S. Cl. 713/300

(57) ABSTRACT

A memory assembly module including an on-board voltage regulator for converting an externally supplied voltage into appropriate local voltage levels for powering memory devices of the memory assembly module.

respectively. Preferably, a high-frequency switching voltage converter capable of generating tightly-controlled voltage levels may be implemented as the on-board VRM **102** for purposes of the present patent disclosure. For instance, multi-phase synchronous Pulse-Width Modulated (PWM) controllers, Low Drop-Out (LDO) controllers, et cetera, that are capable of accepting unregulated supply voltages in a broad range may be configured to operate as a local voltage supply for the memory module **100**A.

EX1023 (Harris), [0010].

Patent Owner Response (918) at 4, 8, 16-17.
Patent Owner Response (054) at 5, 10-11, 19-20.

Petitioner Argues That General References to Step Converters Does Not Inherently Disclose Buck Converters

53. A Skilled Artisan would have understood at the time that a "buck converter" is different from a "step-down transformer" described in the 586 Provisional. To the extent the term "transformer" is meant to cover changing the voltage by any means which produces a regulated voltage, a Skilled Artisan would have understood that a step-down regulated voltage can also be provided by means other than a "buck converter," e.g., by a linear regulator, such as a low-dropout regulator (LDO). A Skilled Artisan would have understood that an LDO is different from the claimed "buck converter." *See, e.g.,* Ex. 1059 at 5:23-30 ("Switch mode buck converters have become popular due to two attractive features: first, they are more efficient than traditional low drop out regulators (LDO) (e.g., up to 95%) and second, they can provide relatively high currents with lower power dissipation on chip than an LDO can.").

EX1003 (918, 054) (Wolfe Declaration), ¶53.

Petition (918) at 4.
Petition (054) at 4.

TOPICS

GROUNDS 1-3

Harris Does Not Receive Power Via Edge Connections

Harris Does Not Receive The Recited Signals From the Host

A POSITA Would Not Have Used the Required # of (Buck) Converters

Ground 2 ASSUMES Separate Converters To Supply Each FBDIMM-Required Voltage

A POSITA Would Not Have Replaced Harris' Redundant Power

Additional Reasons Why Dependent Claims Are Not Obvious

GROUNDS 4-5

The Recited "Memory Module" Means A Main Memory Module

Spiers' PCI Card Is Not a Memory Module

POSITA Would Not Use DDR2/DDR3 or Recited # of (Buck) Converters

Additional Reasons Why Dependent Claims Are Not Obvious

Amidi Does Not Use Separate On Board Converters for Memory Module Voltages

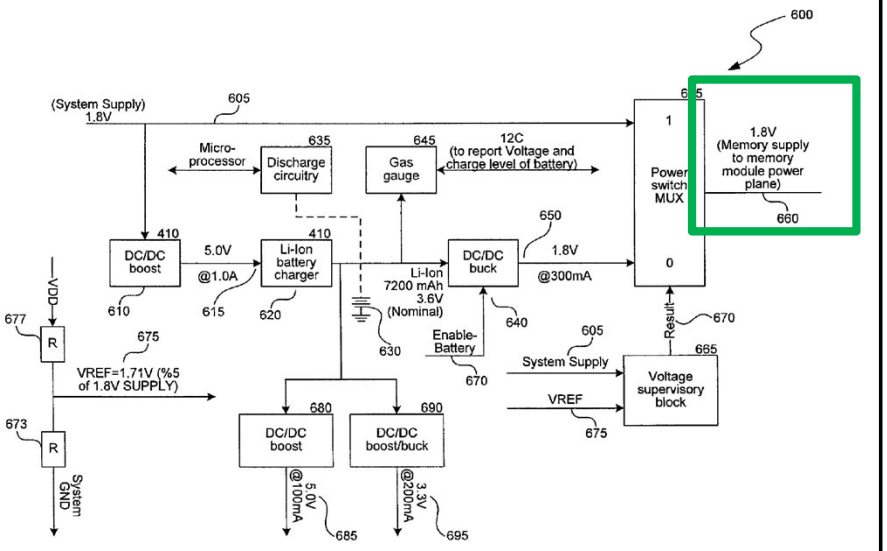


FIG. 6

EX1024 (Amidi) at FIG. 6.

While a general approach to a clock and power fault detection system provides much insight, a truth table for a specific implementation may also be useful. FIG. **13** illustrates an embodiment of a truth table. Truth table **1300** represents the values of signals to memory components of a DDR2 SDRAM memory module as would be generated to control the clock and power fault detection system and the actual memory (for write protection and refresh purposes).

EX1024 (Amidi) at 7:52-59.

Petition (918) at 6, 79 (citing EX1003 at ¶196).
Petition (054) at 6-7, 72-73 (citing EX1003 at ¶196).

Ground 2 Still Assumes Motivation to Use Separate Converters For Each FBDIMM Required Voltage

Ground 2: Ground 1 and Battery Backup of Amidi

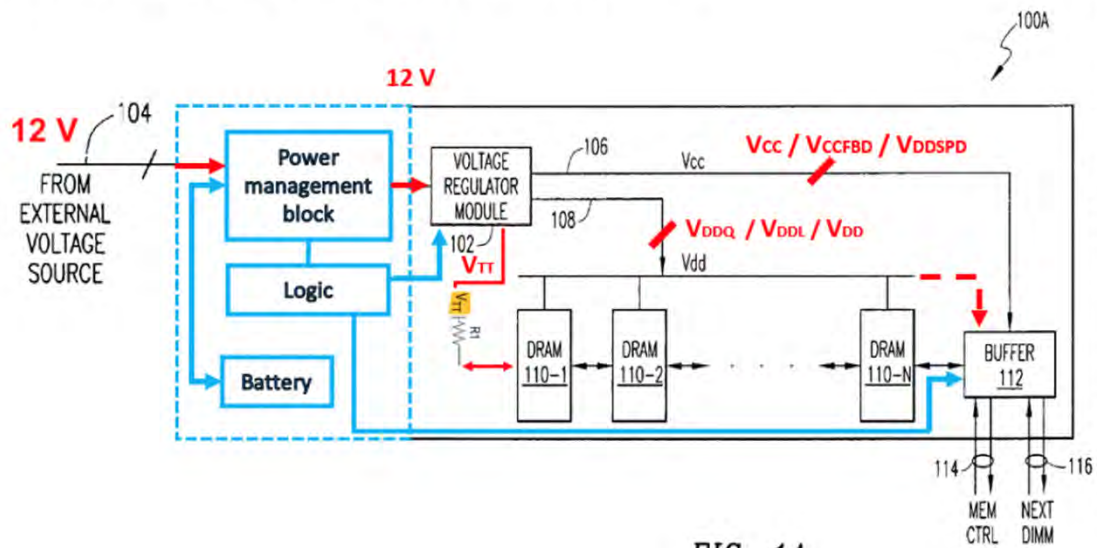


FIG. 1A

Voltage Mapping (A)
1st : V_{DD} / V_{DDQ} = 1.8V
2nd : V_{CC} / V_{CCFBD} = 1.5V
3rd : V_{DDL} = 1.8V
4th : V_{DDSPD} = 3.3V

Voltage Mapping (B)
1st : V_{DD} / V_{DDQ} / V_{DDL} = 1.8V
2nd : V_{CC} = 1.5V
3rd : V_{CCFBD} = 1.5V
4th : V_{DDSPD} = 3.3V

Voltage Mapping (C)
1st : V_{DD} / V_{DDQ} / V_{DDL} = 1.8V
2nd : V_{CC} / V_{CCFBD} = 1.5V
3rd : V_{TT} = 0.9V
4th : V_{DDSPD} = 3.3V

Petition (918) at 75.
Petition (054) at 67.

TOPICS

GROUNDS 1-3

Harris Does Not Receive Power Via Edge Connections

Harris Does Not Receive The Recited Signals From the Host

A POSITA Would Not Have Used the Required # of (Buck) Converters

Ground 2 ASSUMES Separate Converters To Supply Each FBDIMM-Required Voltage

A POSITA Would Not Have Replaced Harris' Redundant Power

Additional Reasons Why Dependent Claims Are Not Obvious

GROUNDS 4-5

The Recited "Memory Module" Means A Main Memory Module

Spiers' PCI Card Is Not a Memory Module

POSITA Would Not Use DDR2/DDR3 or Recited # of (Buck) Converters

Additional Reasons Why Dependent Claims Are Not Obvious

Harris Already Provides Redundant Power to the Memory Module

External voltage source can be battery

that the voltage distribution system for memory module **100B** is essentially similar to the system shown in **FIG. 1A**, but for the redundancy implementation of local voltage conversion. A plurality of on-board VRMs **122**-K, K=1, 2, . . . , N, are provided as part of the memory assembly/module **100B** wherein each VRM is operable with an independent voltage supply path for locally converting an external supply voltage into appropriate local voltage levels. Reference

EX1023 (Harris), [0014].

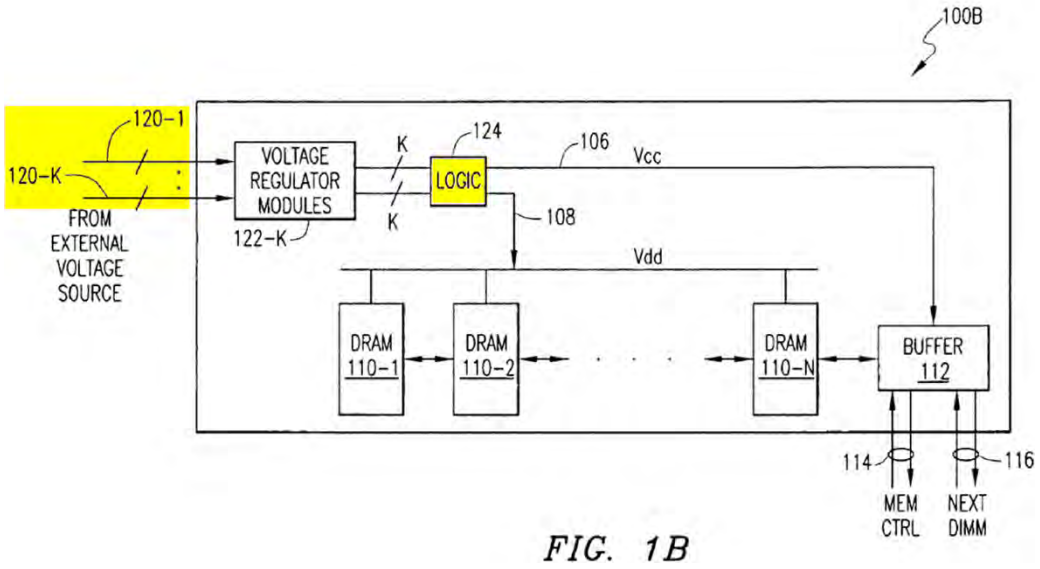


FIG. 1B

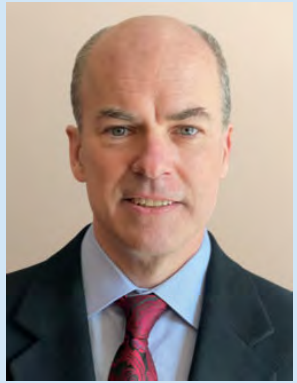
EX1023 (Harris), FIG. 1B.

system) (not shown). It should be readily recognized that the external voltage sources may comprise any combination of known or heretofore unknown voltage supplies, either regulated or unregulated, and even including variable voltages.

EX1023 (Harris), [0014].

Patent Owner Response (918) at 32.
Patent Owner Response (054) at 34-35.

Harris' Redundancy Implementation Provides Backup Power Using Redundant Input Voltages



William Mangione-Smith
Netlist's Expert

NETLIST

> 107. A POSITA would understand that the purpose of Harris' redundant power sources is to switch to an alternative voltage source in response to a power loss, in a very similar manner as Amidi. Dr. Wolfe agrees. EX1003, ¶170 ("Similar

EX2031 (918) (Mangione-Smith Declaration), ¶107.
EX2061 (054) (Mangione-Smith Declaration), ¶105.

Patent Owner Response (918) at 34.

Dr. Wolfe Agrees: Harris' Existing Redundancy Implementation is Functionally Similar to Amidi's Backup Power Supply

Andrew Wolfe
Samsung's Expert

SAMSUNG

Harris

power sources. *See* Ex. 1023 at [0014] (describing a "redundancy implementation"), [0016] (describing a "redundant VRM" to "power a redundant voltage path"), Figs. 1B, 2. Similar to the redundant implementation in Harris, Amidi teaches a redundant power source. *See, e.g.*, Ex. 1024 at Abstract. Amidi

EX1003 (918) (Wolfe Declaration), ¶170.
EX1003 (054) (Wolfe Declaration), ¶172.

Patent Owner Response (918) at 34.
Patent Owner Response (054) at 36.

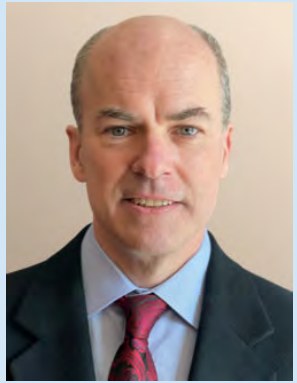
Petition: Amidi's Backup Power Supply Is Functioning "In the Same Way" As Harris' Redundant Implementation

The Petition

backup when needed. EX1003, ¶¶170-174. This straightforward modification of Harris's memory module in view of Amidi and the knowledge of a POSITA simply uses a known technique (e.g., Amidi's battery backup techniques) to improve a similar device (e.g., Harris's memory module) in the same way (e.g., to provide a backup power supply using a battery). *Id.*, ¶175. In addition, the

Petition (918) at 55.

A POSA Would Not Have Preferred On Module Battery Backup



William Mangione-Smith
Netlist's Expert

NETLIST

- "[U]sing Amidi's battery only results in **additional and unnecessary complexity**, with Harris's 12V external source having to be stepped-down with a buck converter to 5V for Amidi's battery, only to then be stepped back up with a boost converter to 12V. EX2031, ¶108.
- The '918 patent notes that "batteries may require **maintenance**, may **need to be replaced**, are not environmentally friendly, and the status of batteries can be difficult to monitor." EX1001, 4:56-58; *Id*.
- "Amidi's battery backup solution would require a **substantial amount of on-board space** …." EX2031, ¶108.
- "[A] battery backup solution would also be able to **provide backup power for only a finite period of time** based on the battery's capacity. This would represent an inadequate solution for power interrupts which last longer." *Id*., ¶109.

Patent Owner Response (918) at 30-31. DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

TOPICS

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Additional Reasons Why Dependent Claims Are Not Obvious

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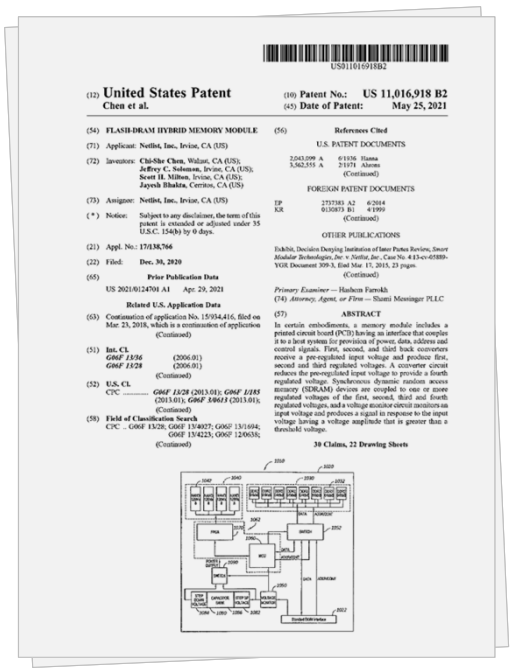
The Recited "Memory Module" Means A Main Memory Module

Spiers' PCI Card Is Not a Memory Module

POSITA Would Not Use DDR2/DDR3 or Recited # of (Buck) Converters

Additional Reasons Why Dependent Claims Are Not Obvious

’918 Claims 5-7, 9-13, 16-22, 24-27: Trigger Signal Produced In Response to Detecting Over-voltage



US011016918B2

(12) **United States Patent**
Chen et al.

(10) **Patent No.: US 11,016,918 B2**
(45) **Date of Patent: May 25, 2021**

(54) **FLASH-DRAM HYBRID MEMORY MODULE**

(71) Applicant: **Netlist, Inc.**, Irvine, CA (US)

(72) Inventors: **Chi-She Chen**, Walnut, CA (US); **Jeffrey C. Solomon**, Irvine, CA (US); **Scott H. Milton**, Irvine, CA (US); **Jayesh Bhakta**, Cerritos, CA (US)

(73) Assignee: **Netlist, Inc.**, Irvine, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **17/138,766**

(22) Filed: **Dec. 30, 2020**

(65) **Prior Publication Data**

US 2021/0124701 A1 Apr. 29, 2021

Related U.S. Application Data

(63) Continuation of application No. 15/934,416, filed on Mar. 23, 2018, which is a continuation of application (Continued)

(51) **Int. Cl.**
G06F 13/16 (2006.01)
G06F 13/28 (2006.01)
(Continued)

(52) **U.S. Cl.**
CPC ***G06F 13/28*** (2013.01); ***G06F 1/185*** (2013.01); ***G06F 3/0613*** (2013.01);
(Continued)

(58) **Field of Classification Search**
CPC .. G06F 13/28; G06F 13/4027; G06F 13/1694; G06F 13/4234; G06F 12/0638;
(Continued)

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(Continued)

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(Continued)

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Exhibit, Decision Denying Institution of Inter Partes Review, *Smart Modular Technologies, Inc v. Netlist, Inc.*, Case No. 4:13-cv-05889-YGR Document 309-3, filed Mar 17, 2015, 23 pages.
(Continued)

Primary Examiner — Hashem Farrokh
(74) *Attorney, Agent, or Firm* — Shumi Messinger PLLC

(57) **ABSTRACT**

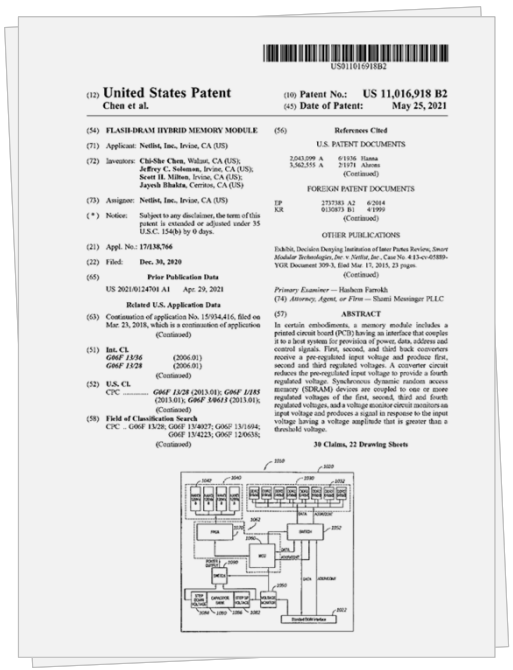
In certain embodiments, a memory module includes a printed circuit board (PCB) having an interface that couples it to a host system for provision of power, data, address and control signals. First, second, and third buck converters receive a pre-regulated input voltage and produce first, second and third regulated voltages. A converter circuit reduces the pre-regulated input voltage to provide a fourth regulated voltage. Synchronous dynamic random access memory (SDRAM) devices are coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages, and a voltage monitor circuit monitors an input voltage and produces a signal in response to the input voltage having a voltage amplitude that is greater than a threshold voltage.

30 Claims, 22 Drawing Sheets

The ’918 Patent

5. The memory module of claim **1**, further comprising:
a voltage monitor circuit configured to monitor a power input voltage received via a second portion of the plurality of edge connections, the voltage monitor circuit configured to produce a trigger signal in response to the power input voltage having a voltage amplitude that is greater than a first threshold voltage.

’054 Claims 6-7, 11-12, 17, 29: Trigger Signal Produced In Response to Detecting Over-voltage



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(73) Assignee: **Netlist, Inc.**, Irvine, CA (US)

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(51) **Int. Cl.**
G06F 13/16 (2006.01)
G06F 13/28 (2006.01)
(Continued)

(52) **U.S. Cl.**
CPC ***G06F 13/28*** (2013.01); ***G06F 1/185*** (2013.01); ***G06F 3/0613*** (2013.01);
(Continued)

(58) **Field of Classification Search**
CPC .. G06F 13/28; G06F 13/4027; G06F 13/1694; G06F 13/4234; G06F 12/0638;
(Continued)

(56) **References Cited**

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3,562,555 A 2/1971 Ahrons
(Continued)

FOREIGN PATENT DOCUMENTS

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KR 0150873 B1 4/1999
(Continued)

OTHER PUBLICATIONS

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(Continued)

Primary Examiner — Hashem Farrokh
(74) *Attorney, Agent, or Firm* — Shumi Messinger PLLC

(57) **ABSTRACT**

In certain embodiments, a memory module includes a printed circuit board (PCB) having an interface that couples it to a host system for provision of power, data, address and control signals. First, second, and third buck converters receive a pre-regulated input voltage and produce first, second and third regulated voltages. A converter circuit reduces the pre-regulated input voltage to provide a fourth regulated voltage. Synchronous dynamic random access memory (SDRAM) devices are coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages, and a voltage monitor circuit monitors an input voltage and produces a signal in response to the input voltage having a voltage amplitude that is greater than a threshold voltage.

30 Claims, 22 Drawing Sheets

The ’054 Patent

6. The memory module of claim **1**, further comprising:
a voltage monitor circuit coupled to the PCB and to a second set of edge connections of the plurality of edge connections, the voltage monitor circuit configured to monitor an input voltage received from the second set of edge connections, the voltage monitor circuit configured to produce a trigger signal in response to the input voltage having a voltage amplitude above a predetermined threshold voltage, wherein the memory module transitions from a first operable state to a second operable state in response to the trigger signal.

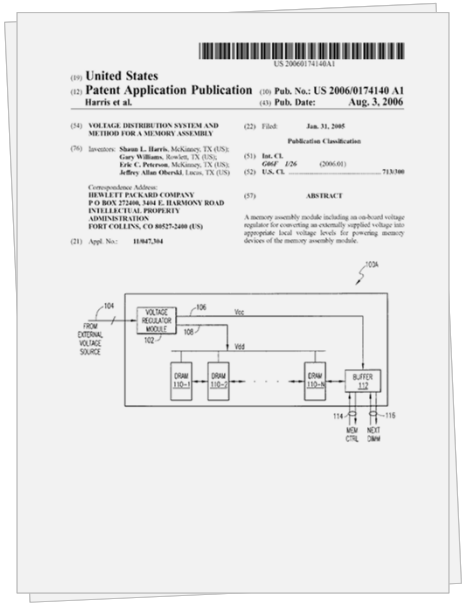
Petition: Harris Allegedly Teaches Detecting Over/Under Voltages

The Petition

> Additionally, Harris teaches ***both*** overvoltage ***and*** undervoltage protection of "+/- 15%." EX1023, ¶[0013]. Thus, in the combination of Ground 2, a

Petition (918) at 62.

Harris' ± 15% Is a Design Tolerance, Not Detection of Over/Under Voltages



US 20060174140A1

(19) United States

(12) Patent Application Publication (10) Pub. No.: US 2006/0174140 A1

Harris et al. (43) Pub. Date: Aug. 3, 2006

(54) VOLTAGE DISTRIBUTION SYSTEM AND METHOD FOR A MEMORY ASSEMBLY

(76) Inventors: Shaun L. Harris, McKinney, TX (US); Gary Williams, Rowlett, TX (US); Eric C. Peterson, McKinney, TX (US); Jeffrey Allan Oberstd, Lucas, TX (US)

Correspondence Address:
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P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400 (US)

(21) Appl. No.: 11/047,304

(22) Filed: Jan. 31, 2005

Publication Classification

(51) Int. Cl.
G06F 1/26 (2006.01)

(52) U.S. Cl. 713/300

(57) ABSTRACT

A memory assembly module including an on-board voltage regulator for converting an externally supplied voltage into appropriate local voltage levels for powering memory devices of the memory assembly module.

> Engineering Council (JEDEC) standards. Further, since the +12V power supply is not used directly by DRAM devices or buffer/logic components of the memory assembly, a wide tolerance (e.g., around +/–15%) can be accommodated, allowing low cost power distribution for system boards

EX1023 (Harris), [0013].

> low cost power distribution for system boards ...." EX1023, [0013]. A POSITA would understand that Harris' reference to "+/-15%" refers to design tolerances, not to detecting when the input voltage happens to rise above a predetermined threshold.

EX2031 (918) (Mangione-Smith Declaration), ¶116.
EX2061 (054) (Mangione-Smith Declaration), ¶113.

And no trigger signal is produced in Harris if supply voltage exceeds design tolerance

Patent Owner Response (918) at 39.
Patent Owner Response (054) at 40-41.

Petition: Allegedly Well-Known to Detect Over/Under Voltages

The Petition

> ¶¶368-374. Indeed, such circuitry for ***both*** overvoltage ***and*** undervoltage protection was well known and commercially available:

Petition (918) at 62.
Petition (054) at 54.

Petitioner's Evidence Shows That Allegedly Suitable Regulators Did Not Detect Over-Voltage

Undervoltage, but no Overvoltage detection

ANALOG DEVICES

Step-Down DC-to-DC Controller

ADP1821

SPECIFICATIONS

$V_{VCC} = V_{PVCC} = V_{\overline{SHDN}} = V_{FREQ} = 5$ V, SYNC = GND. All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC). $T_J = -40°C$ to $+125°C$, unless otherwise specified. Typical values are at $T_A = 25°C$.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
POWER SUPPLY					
Input Voltage		3.7		5.5	V
Undervoltage Lockout Threshold	V_{VCC} rising, $T_J = -40°C$ to $+125°C$	2.4	2.7	3.0	V
Undervoltage Lockout Threshold	V_{VCC} rising, $T_A = 25°C$	2.5	2.7	2.9	V
Undervoltage Lockout Hysteresis	V_{VCC}		0.1		V
Quiescent Current	$I_{VCC} + I_{VCC}$, not switching		1	2	mA
Shutdown Current	$\overline{SHDN}$ = GND			10	µA
Power Stage Supply Voltage		1.0		24	V

EX1078, 1, 3.
Patent Owner Sur-Reply (918) at 20.
Patent Owner Sur-Reply (054) at 21.

Wide Input Voltage Tolerance Obviates the Need for Over-Voltage Detection

TEXAS INSTRUMENTS

TPS51020

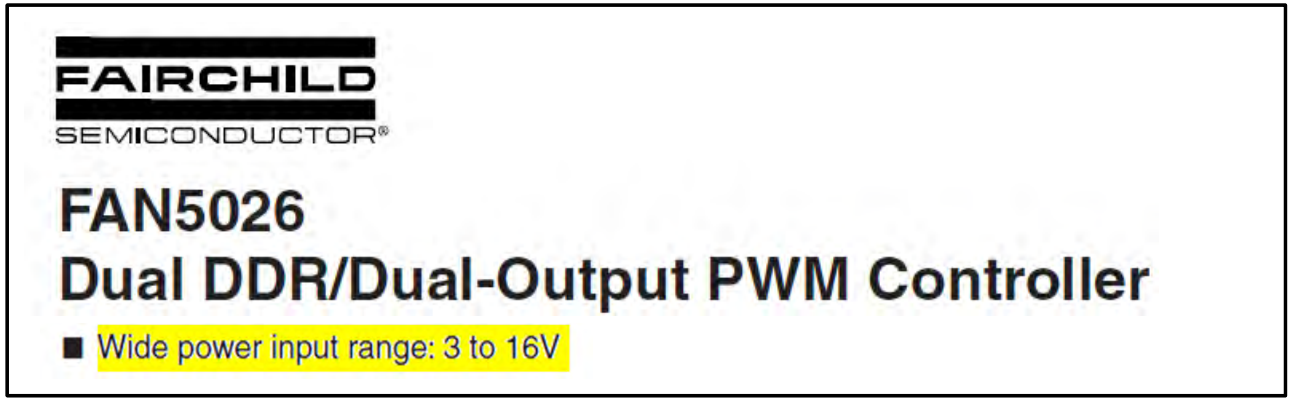
SLUS564B – JULY 2003 – REVISED DECEMBER 2003

DUAL, VOLTAGE MODE, DDR SELECTABLE, SYNCHRONOUS, STEP-DOWN CONTROLLER FOR NOTEBOOK SYSTEM POWER

FEATURES

- Wide Input Voltage Range: 4.5-V to 28-V

EX1040.



FAIRCHILD SEMICONDUCTOR®

FAN5026

Dual DDR/Dual-Output PWM Controller

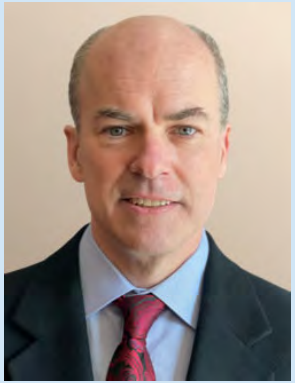
- Wide power input range: 3 to 16V

EX1041.

Patent Owner Response (918) at 40.

Patent Owner Response (054) at 42.

High Upper Limit on Input Voltage Obviates the Need for Over-Voltage Detection



William Mangione-Smith
Netlist's Expert

NETLIST

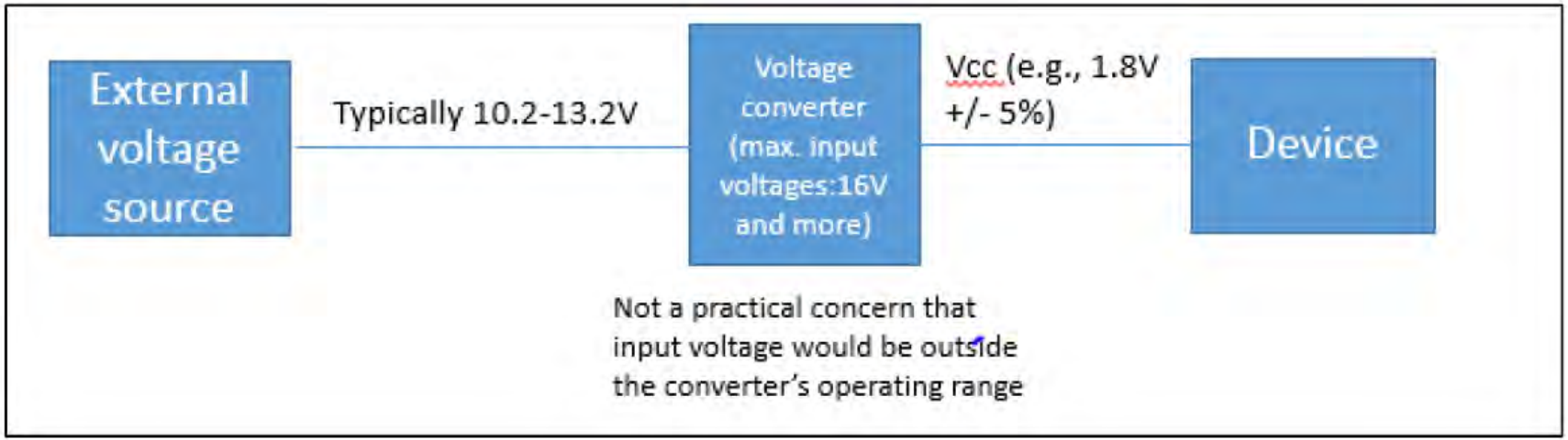
117. … [V]oltage regulators that Samsung alleges are suitable for use with Harris **do not detect input overvoltage**, as Dr. Wolfe confirmed. See EX2030, 58:24-61:12; EX1040; EX1041…. An unregulated 12V voltage source with ±15% wide tolerance has an expected voltage range of 10.2 – 13.8V. The 28V upper limit for the converters in EX1040 is well above the 13.8V upper range. So is the 16V upper limit for the converters in EX1041. Indeed, even if the +/-15% tolerance represents only a 3-sigma process, the upper limit for the converters in EX1040 would be 26.7 sigmas away; and the upper limit for the converters in EX1041 would be 6.7 sigmas away. That means the probability that the input voltage would be above the permissible operating range of these converters is extremely low (6 sigmas means **one in half a billion chance**). As such, a POSITA would have no need to include input overvoltage detection for these regulators.

EX2031 (Mangione-Smith Declaration), ¶117.

Patent Owner Response (918) at 40.

Petitioner Has Not Established Any Reason to Detect Over-Voltage in the Harris+Amidi Combination

NETLIST



Patent Owner Sur-Reply (918) at 22.
Patent Owner Sur-Reply (054) at 23.

Petition: A POSA Would Allegedly Be Motivated to Switch to Amidi's Backup Power When Over-Voltage Is Detected Based On Hajeck

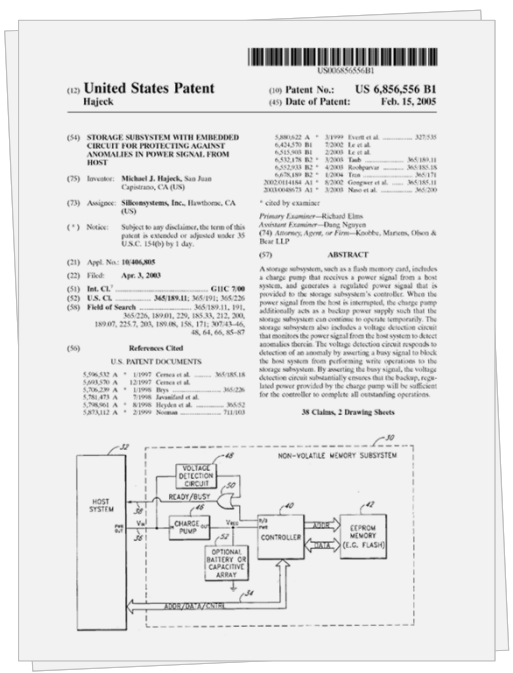
The Petition

> EX1003, ¶¶185-187. In particular, in the combination for Ground 3, Amidi's voltage supervisory block would be modified to detect voltage anomalies and switch to the backup power not only "[i]f system supply 605 has a magnitude lower than reference voltage 675" as disclosed by Amidi (EX1024, 4:44-52), but also "when the voltage exceeds a certain level" as taught by Hajeck (EX1038,

Petition (918) at 77.
Petition (054) at 72.

Hajeck Does Not Suggest Switching To Backup Power In Response To Detecting An Over-Voltage

Hajeck's voltage detection 48 circuit sends a "busy signal" 38 back to the host 32 to prevent the host 32 from performing write operations to the memory subsystem 30 when voltage anomalies are detected. EX1038, 3:30-57.



(12) **United States Patent**
Hajeck

(10) **Patent No.: US 6,856,556 B1**
(45) **Date of Patent: Feb. 15, 2005**

(54) **STORAGE SUBSYSTEM WITH EMBEDDED CIRCUIT FOR PROTECTING AGAINST ANOMALIES IN POWER SIGNAL FROM HOST**

(75) Inventor: **Michael J. Hajeck**, San Juan Capistrano, CA (US)

(73) Assignee: **Siliconsystems, Inc.**, Hawthorne, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 1 day.

(21) Appl. No.: **10/406,805**

(22) Filed: **Apr. 3, 2003**

(51) **Int. Cl.**[7] **G11C 7/00**

(52) **U.S. Cl.** **365/189.11**; 365/191; 365/226

(58) **Field of Search** 365/189.11, 191, 365/226, 189.01, 229, 185.33, 212, 200, 189.07, 225.7, 203, 189.08, 158, 171; 307/43-46, 48, 64, 66, 85-87

(56) **References Cited**

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5,798,961 A * 8/1998 Heydet et al. 365/52
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5,880,622 A * 3/1999 Everett et al. 327/535
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6,532,178 B2 * 3/2003 Taub 365/189.11
6,552,933 B2 * 4/2003 Roohparvar 365/185.18
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2003/0048673 A1 * 3/2003 Nasu et al. 365/200

* cited by examiner

Primary Examiner—Richard Elms
Assistant Examiner—Dang Nguyen
(74) *Attorney, Agent, or Firm*—Knobbe, Martens, Olson & Bear LLP

(57) **ABSTRACT**

A storage subsystem, such as a flash memory card, includes a charge pump that receives a power signal from a host system, and generates a regulated power signal that is provided to the storage subsystem's controller. When the power signal from the host is interrupted, the charge pump additionally acts as a backup power supply such that the storage subsystem can continue to operate temporarily. The storage subsystem also includes a voltage detection circuit that monitors the power signal from the host system to detect anomalies therein. The voltage detection circuit responds to detection of an anomaly by asserting a busy signal to block the host system from performing write operations to the storage subsystem. By asserting the busy signal, the voltage detection circuit substantially ensures that the backup, regulated power provided by the charge pump will be sufficient for the controller to complete all outstanding operations.

38 Claims, 2 Drawing Sheets

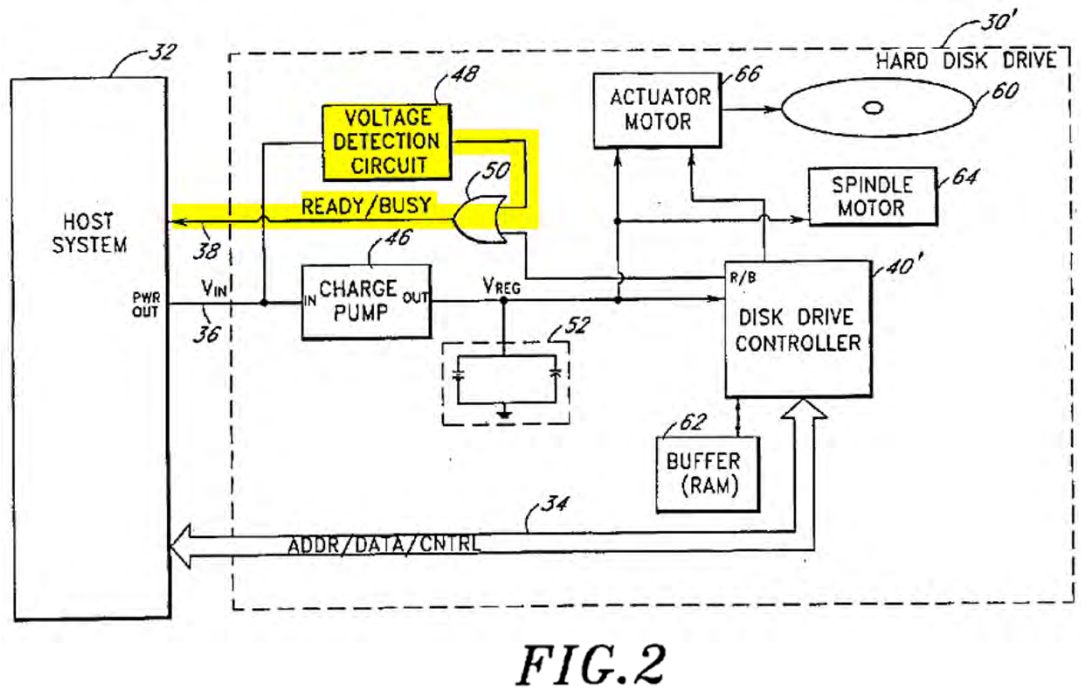
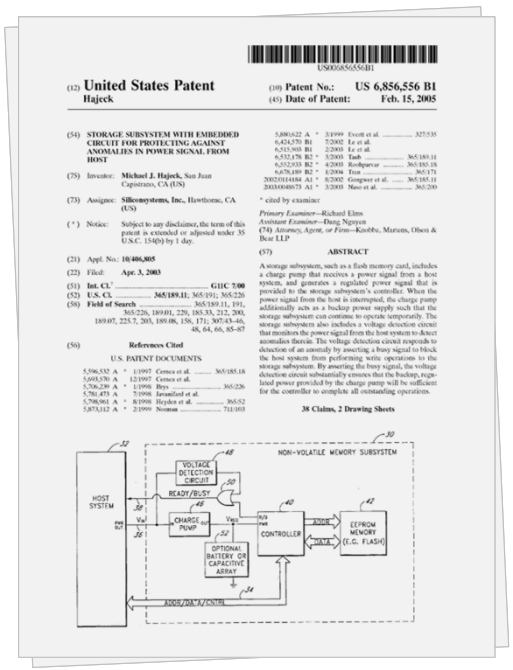


FIG.2

EX1038 (Hajeck), FIG. 2.

Patent Owner Response (918) at 41.
Patent Owner Response (054) at 43.

Hajeck Reduces The Risk Of Data Loss By Inhibiting New Write Operations, Not Switching To A Different Power Source



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(58) **Field of Search** 365/189.11, 191, 365/226, 189.01, 229, 185.33, 212, 200, 189.07, 225.7, 203, 189.08, 158, 171; 307/43–46, 48, 64, 66, 85–87

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5,880,622 A * 3/1999 Evett et al. 327/535
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38 Claims, 2 Drawing Sheets

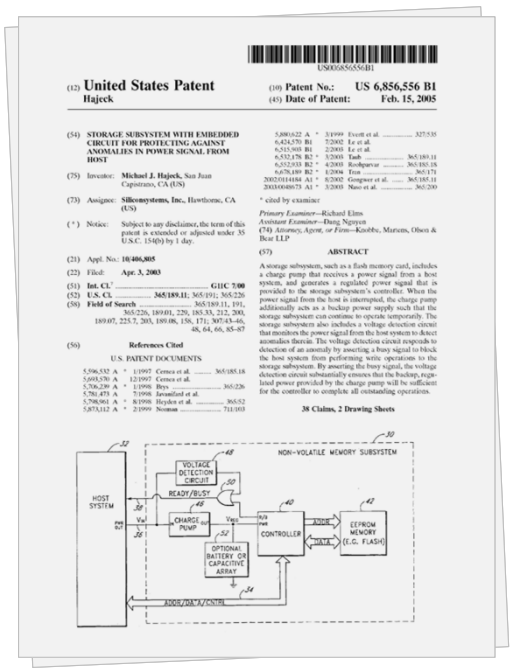
described below). Because new write operations are inhibited, and because the charge pump continues to provide a regulated power signal to the controller **40**, the possibility of data corruption (e.g., as the result of incomplete write operations) is significantly reduced. The charge pump also serves to protect the controller **40** and other circuitry from damage caused by voltage surges and spikes.

EX1038 (Hajeck), 4:3-9.

Hajeck expressly continues to provide regular power in the event of voltage anomalies

Patent Owner Response (918) at 41.

Hajeck Teaches to Use a Charge Pump To Protect Against Over-Voltages, Not To Switch to Backup Power



US006856556B1

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(10) **Patent No.: US 6,856,556 B1**
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(73) Assignee: **Silicongenius, Inc.**, Hawthorne, CA (US)

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38 Claims, 2 Drawing Sheets

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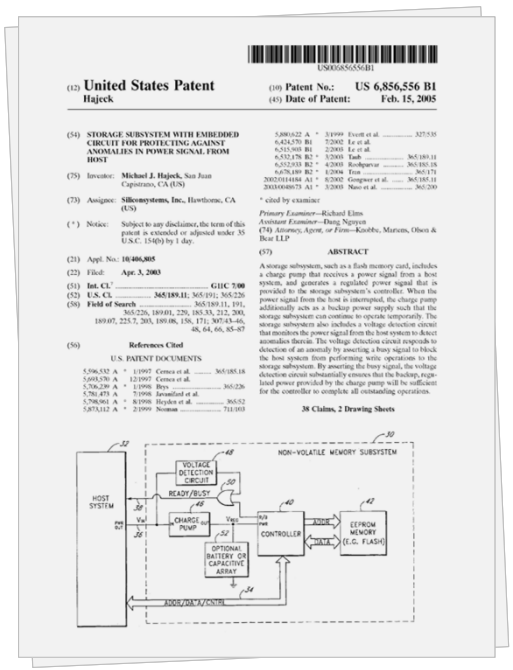
EX1038 (Hajeck), 4:3-9.

Patent Owner Response (918) at 41.

Hajeck Teaches Continued Operation With Same Power Source in Over-Voltage Condition



US006856556B1

(12) **United States Patent**
Hajeck

(10) **Patent No.: US 6,856,556 B1**
(45) **Date of Patent: Feb. 15, 2005**

(54) **STORAGE SUBSYSTEM WITH EMBEDDED CIRCUIT FOR PROTECTING AGAINST ANOMALIES IN POWER SIGNAL FROM HOST**

(75) Inventor: **Michael J. Hajeck**, San Juan Capistrano, CA (US)

(73) Assignee: **Silicongenius, Inc.**, Hawthorne, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 1 day.

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(51) **Int. Cl.**[7] **G11C 7/00**

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(58) **Field of Search** 365/189.11, 191, 365/226, 189.01, 229, 185.33, 212, 200, 189.07, 225.7, 203, 189.08, 158, 171; 307/43–46, 48, 64, 66, 85–87

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5,880,622 A * 3/1999 Evertt et al. 327/535
6,424,570 B1 7/2002 Le et al.
6,515,903 B1 2/2003 Le et al.
6,532,176 B2 * 3/2003 Tsuh 365/189.11
6,552,933 B2 * 4/2003 Roohparvar 365/185.18
6,678,189 B2 * 1/2004 Tran 365/171
2002/0114184 A1 * 8/2002 Gongwer et al. 365/185.11
2003/0048673 A1 * 3/2003 Nuo et al. 365/200

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38 Claims, 2 Drawing Sheets

V_{IN} supplied by the host 32. In addition, the charge pump is preferably designed to protect against sustained voltage drops; for example, in one embodiment, the charge pump is capable of maintaining V_{REG} at 5.4 volts indefinitely as long as V_{IN} exceeds 0.7 volts. The charge pump **46** thus allows the memory subsystem **30** to continue to operate during certain types of power anomalies, including brief power interruptions, spikes and sustained voltage drops. In addition, the charge pump **46** protects the controller **40** from being damaged by spikes and surges in the power signal provided by the host.

EX1038 (Hajeck), 3:6-15.

Patent Owner Response at 41, 44.
Patent Owner Sur-Reply at 34.

Dr. Wolfe Agrees: Hajeck's Charge Pump Would Absorb Over-Voltages

Andrew Wolfe
Samsung's Expert

SAMSUNG

"So something like a spike would be diluted in that reservoir and would not be passed through."

EX2030 (918) (Wolfe Deposition), 229:9-11.
EX2060 (054) (Wolfe Deposition), 229:9-11.

"There will be some set of spikes and surges that can be absorbed by the charge pump."

EX2030 (918) (Wolfe Deposition), 230:11-13.
EX2060 (054) (Wolfe Deposition), 230:11-13.

Patent Owner Sur-Reply (918) at 21.
Patent Owner Sur-Reply (054) at 21-22.

None Of The References Motivate Switching To Backup Power In Response To An Over-Voltage

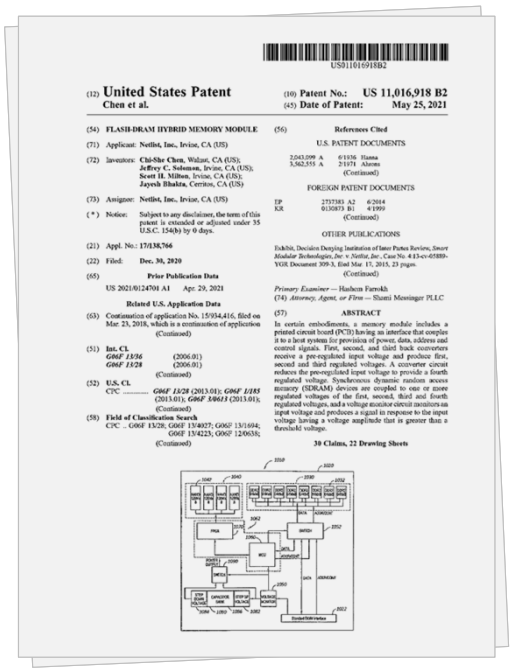
NETLIST

- **Harris**
  - discloses only a design tolerance of +/- 15% for input voltage.
  - does not disclose detecting over-voltages or switching to backup power .
- **Amidi**
  - discloses switching to backup power only in response to power loss.
- **Hajeck**
  - does not disclose/suggest switching to backup power in response to an over-voltage because, in that condition, it inhibits write operations while continuing to provide regular power from Hajeck's charge pump.
  - discloses using a charge pump to protect against over-voltage.

The alleged desire to switch to backup power supply to avoid data loss in an over-voltage condition is not found in any of prior art references, alone or in combination.

Patent Owner Response (918) at 40-42
Patent Owner Sur-Reply (918) at 20-22.

Claims 10-11, 15, 22: Non-volatile Memory Within The Logic Element



US011016918B2

(12) **United States Patent**
Chen et al.

(10) **Patent No.: US 11,016,918 B2**
(45) **Date of Patent: May 25, 2021**

(54) **FLASH-DRAM HYBRID MEMORY MODULE**

(71) Applicant: **Netlist, Inc.**, Irvine, CA (US)

(72) Inventors: **Chi-She Chen**, Walnut, CA (US); **Jeffrey C. Solomon**, Irvine, CA (US); **Scott H. Milton**, Irvine, CA (US); **Jayesh Bhakta**, Cerritos, CA (US)

(73) Assignee: **Netlist, Inc.**, Irvine, CA (US)

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(21) Appl. No.: **17/138,766**

(22) Filed: **Dec. 30, 2020**

(65) **Prior Publication Data**

US 2021/0124701 A1 Apr. 29, 2021

Related U.S. Application Data

(63) Continuation of application No. 15/934,416, filed on Mar. 23, 2018, which is a continuation of application (Continued)

(51) **Int. Cl.**
G06F 13/16 (2006.01)
G06F 13/28 (2006.01)
(Continued)

(52) **U.S. Cl.**
CPC ..... ***G06F 13/28*** (2013.01); ***G06F 13/1苏*** (2013.01); ***G06F 13/1673*** (2013.01); (Continued)

(58) **Field of Classification Search**
CPC .. G06F 13/28; G06F 13/4027; G06F 13/1694; G06F 13/4223; G06F 13/0638;
(Continued)

(56) **References Cited**

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(Continued)

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(Continued)

Primary Examiner — Hashem Farrokh
(74) *Attorney, Agent, or Firm* — Shumi Messinger PLLC

(57) **ABSTRACT**

In certain embodiments, a memory module includes a printed circuit board (PCB) having an interface that couples it to a host system for provision of power, data, address and control signals. First, second, and third buck converters receive a pre-regulated input voltage and produce first, second and third regulated voltages. A converter circuit reduces the pre-regulated input voltage to provide a fourth regulated voltage. Synchronous dynamic random access memory (SDRAM) devices are coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages, and a voltage monitor circuit monitors an input voltage and produces a signal in response to the input voltage having a voltage amplitude that is greater than a threshold voltage.

30 Claims, 22 Drawing Sheets

The ’918 Patent

10. The memory module of claim **5**, the plurality of components further comprising:

a logic element including a non-volatile memory, the non-volatile memory is configured to store configuration information.

The AMB in Harris+FBDIMM Is Alleged To Include Non-Volatile Memory

The Petition

9. Claim 10

Grounds 2A-2D teach "*claim 5, the plurality of components further comprising: a logic element* [e.g., logic in Harris's Buffer] *including a non-volatile memory, the non-volatile memory is configured to store configuration information*

Petition (918) at 67.

Petitioner Has Not Established That an AMB Includes Non-Volatile Memory

Andrew Wolfe
Samsung's Expert

SAMSUNG

Dr. Wolfe's testimony confirms Petitioner has not provided competent evidence that claims 10-11, 15, 22 are obvious:

> Q. I'm asking you specifically whether you know whether there is any non-volatile memory in the advanced memory buffer.
>
> MR. CHANDLER: Objection. Form.
>
> THE WITNESS: I don't know whether or not there is any inside, no.

EX2030 (Wolfe Deposition), 293:1-6.

Patent Owner Response (918) at 43.

Petitioner Has Not Established That an AMB Includes Non-Volatile Memory

Andrew Wolfe
Samsung's Expert

SAMSUNG

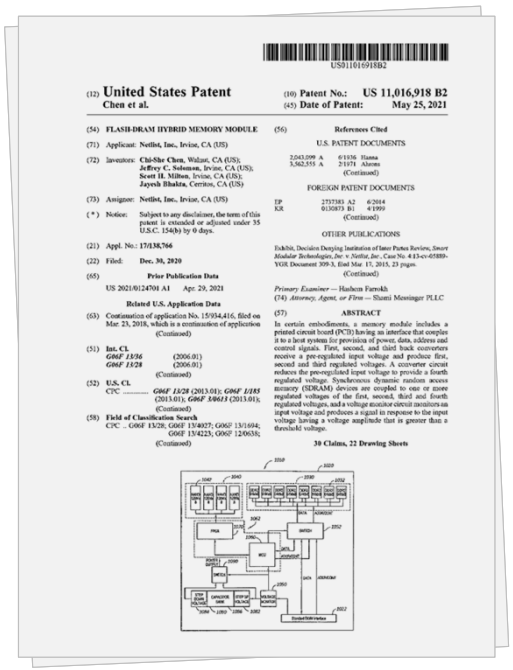
Petitioner's reference to SPD for claim 15 fails to bridge the gap because SPD and AMB are two <u>different</u> components:

> Q. But SPD is not AMB; is that right? Those are two separate components?
>
> A. Those are two separate components --
>
> Q. Okay.
>
> A. -- on the same DIMM.

EX2030 (Wolfe Deposition), 292:21-25.

Patent Owner Response (918) at 43.

Claims 11-12, 18-19, 25-26: Write Operation In Response To Over-Voltage



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G06F 13/28 (2006.01)
(Continued)

(52) **U.S. Cl.**
CPC ***G06F 13/28*** (2013.01); ***G06F 1/185*** (2013.01); ***G06F 13/1673*** (2013.01);
(Continued)

(58) **Field of Classification Search**
CPC .. G06F 13/28; G06F 13/4027; G06F 13/1694; G06F 13/4223; G06F 1206536;
(Continued)

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(Continued)

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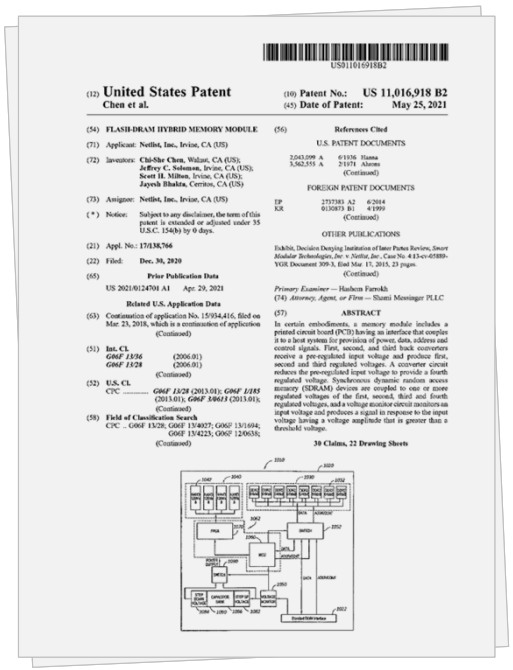
30 Claims, 22 Drawing Sheets

The ’918 Patent

11. The memory module of claim 10, wherein, in response to the trigger signal, the logic element writes information into the non-volatile memory.

The Petition relies on the AMB as the “logic element.” Pet. 67. So the AMB must write the information into non-voltage memory to satisfy the claims.

Claims 5, 7, 8, 23, 24: Write Operation In Response To Over-Voltage



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(21) Appl. No.: **17/138,766**

(22) Filed: **Dec. 30, 2020**

(65) **Prior Publication Data**

US 2021/0124701 A1 Apr. 29, 2021

Related U.S. Application Data

(63) Continuation of application No. 15/934,416, filed on Mar. 23, 2018, which is a continuation of application (Continued)

(51) **Int. Cl.**
G06F 13/16 (2006.01)
G06F 13/28 (2006.01)
(Continued)

(52) **U.S. Cl.**
CPC ..... ***G06F 13/28*** (2013.01); ***G06F 13/1苏*** (2013.01); ***G06F 13/1673*** (2013.01); (Continued)

(58) **Field of Classification Search**
CPC .. G06F 13/28; G06F 13/4027; G06F 13/1694; G06F 13/4223; G06F 120638;
(Continued)

(56) **References Cited**

U.S. PATENT DOCUMENTS

2,043,099 A 6/1936 Hanna
3,562,555 A 2/1971 Ahrens
(Continued)

FOREIGN PATENT DOCUMENTS

EP 2737383 A2 6/2014
KR 0130873 B1 4/1999
(Continued)

OTHER PUBLICATIONS

Exhibit, Decision Denying Institution of Inter Partes Review, *Smart Modular Technologies, Inc. v. Netlist, Inc.*, Case No. 4:13-cv-05889-YGR Document 309-3, filed Mar. 17, 2015, 23 pages.
(Continued)

Primary Examiner — Hashem Farrokh
(74) *Attorney, Agent, or Firm* — Shumi Messinger PLLC

(57) **ABSTRACT**

In certain embodiments, a memory module includes a printed circuit board (PCB) having an interface that couples it to a host system for provision of power, data, address and control signals. First, second, and third buck converters receive a pre-regulated input voltage and produce first, second and third regulated voltages. A converter circuit reduces the pre-regulated input voltage to provide a fourth regulated voltage. Synchronous dynamic random access memory (SDRAM) devices are coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages, and a voltage monitor circuit monitors an input voltage and produces a signal in response to the input voltage having a voltage amplitude that is greater than a threshold voltage.

30 Claims, 22 Drawing Sheets

The ’054 Patent

5. The memory module of claim **4**, further comprising:
a controller coupled to the voltage monitor circuit;
wherein, in response to the trigger signal, the controller is configured to perform one or more operations including a write operation to transfer data to non-volatile memory.

The Petitions Rely on FBDIMM's S3 Sleep Mode

The 918 Petition

9. Claim 10

Grounds 2A-2D teach "*claim 5, the plurality of components further comprising: a logic element* [e.g., logic in Harris's Buffer] *including a non-volatile memory, the non-volatile memory is configured to store configuration information* [e.g., S3 Recovery Configuration Registers as required by S3 sleep mode, EX1027,

10. Claim 11

Grounds 2A-2D teach "*claim 10, wherein, in response to the trigger signal* [see claim 5, e.g., from a power disruption], *the logic element writes information into the non-volatile memory* [e.g., S3 configuration information as discussed above in claims 10 and 15, to allow sleep mode, thus conserving power during

Petition (918) at 67-68.

The Petitions Rely on FBDIMM's S3 Sleep Mode

The 054 Petition

4. Claim 5

Grounds 2A-2C teach, at least under Netlist's apparent interpretation, EX1073, p.62, "*claim 4, further comprising: a controller* [e.g., logic for controlling S3 sleep mode, discussed above (pp.43-44)] *coupled to the voltage monitor circuit* [e.g., Amidi's voltage supervisory block, from [4.b]]; *wherein, in response to the trigger signal* [from [4.b], indicating a power disruption], *the controller is configured to perform one or more operations including a write operation to transfer data to non-volatile memory* [e.g., S3 configuration information is stored in non-volatile memory before entering S3 sleep mode]." EX1003, ¶¶322-340.

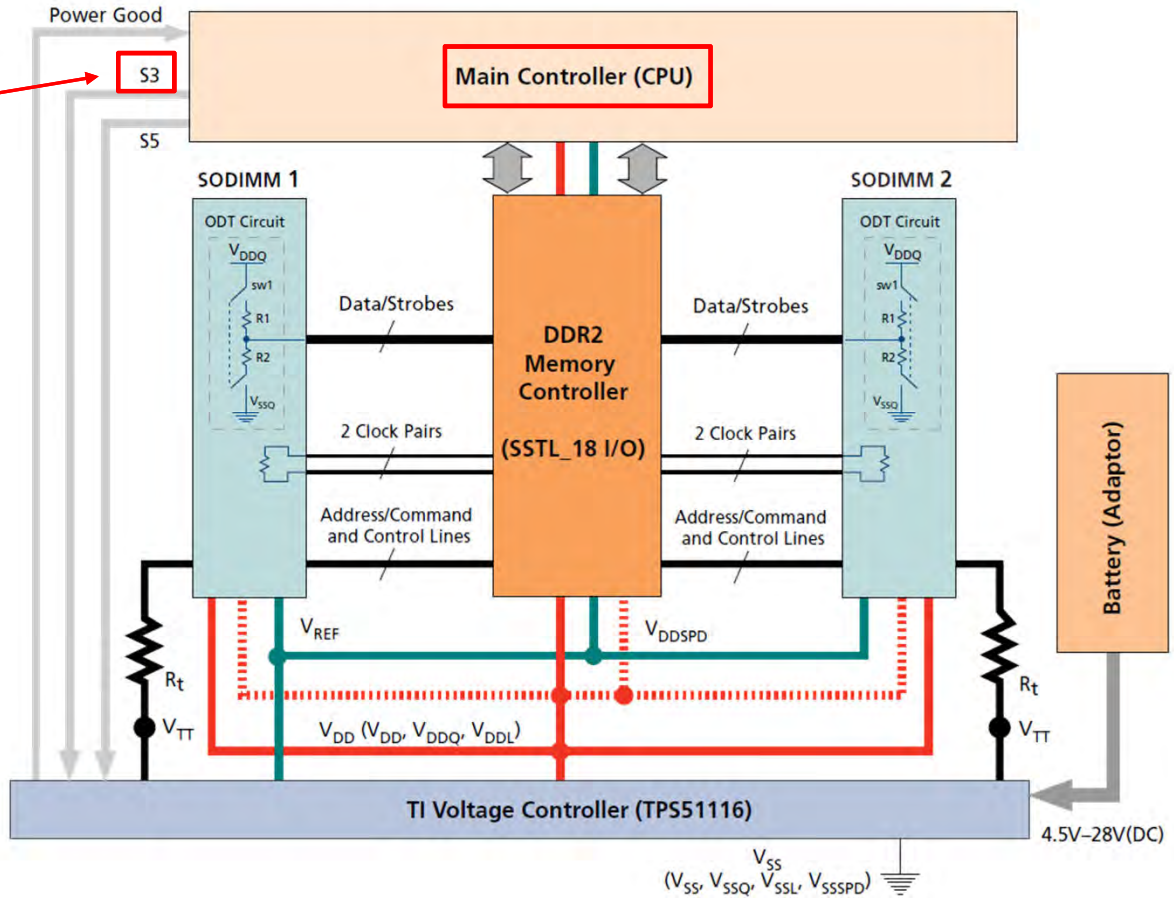
Petition (054) at 50-51.

S3 Mode Is Controlled By The Main CPU, Not The AMB

NETLIST

S3 mode is controlled by the main CPU, not by the AMB on DIMM or even the memory controller (orange)

Figure 2: Functional Block Diagram of a Dual-Channel, 2-Slot DDR2 Notebook



Patent Owner Sur-Reply (918) at 23.
Patent Owner Sur-Reply (054) at 23.

Dr. Wolfe Confirmed: S3 Is Never Determined By The Memory Module

Andrew Wolfe
Samsung's Expert

SAMSUNG

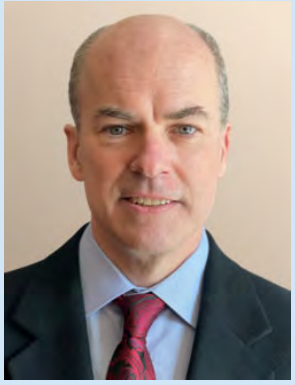
> Q. So for a standard-compliant FB-DIMM, the S3 state is entered into -- determined by the host, not by the memory module itself. Fair?
>
> MR. CHANDLER: Objection to form.
>
> THE WITNESS: It's always determined by something other than the memory module. If its

EX2030 (918) (Wolfe Deposition), 283:18-23.
EX2060 (054) (Wolfe Deposition), 283:18-23.

Because the CPU controls when S3 mode is entered, any alleged "logic element" on the module (e.g., AMB) cannot determine to enter into the S3 state upon detecting an over-voltage condition to execute the write operation in the claimed manner.

Patent Owner Sur-Reply (918) at 23.
Patent Owner Sur-Reply (054) at 23.

Petitioner Fails To Provide Any Competent Evidence That Harris+FBDIMM Could Operate In The Alleged Manner



William Mangione-Smith
Netlist's Expert

NETLIST

39:62 & 40:13, 40:65-41:4, 41:5& 41:22-42:2. The controller for controlling S3 sleep mode, however, is in the host outside the memory module. See above. Moreover, I do not believe that the memory module can be predictably modified to also include a controller that can cause the module to enter an S3 state because S3 was traditionally "determined by something other than the memory module." EX2030, 282:22-284:25. It is also unclear how the computer system could even properly operate if the memory module were allowed to just enter S3 state by itself.

EX2031 (918) (Mangione-Smith Declaration), ¶125.
EX2061 (054) (Mangione-Smith Declaration), ¶120.

Patent Owner Sur-Reply (918) at 23.
Patent Owner Sur-Reply (054) at 23.

TOPICS

GROUNDS 1-3

Harris Does Not Receive Power Via Edge Connections

Harris Does Not Receive The Recited Signals From the Host

A POSITA Would Not Have Used the Required # of (Buck) Converters

Ground 2 ASSUMES Separate Converters To Supply Each FBDIMM-Required Voltage

A POSITA Would Not Have Replaced Harris' Redundant Power

Additional Reasons Why Dependent Claims Are Not Obvious

GROUNDS 4-5

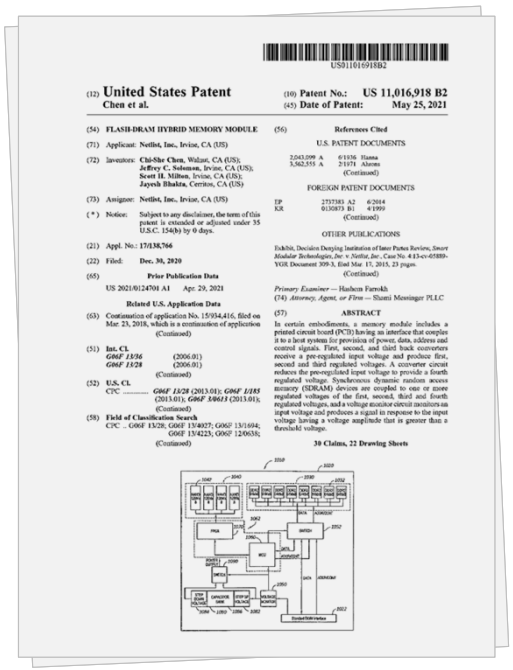
The Recited "Memory Module" Means A Main Memory Module

Spiers' PCI Card Is Not a Memory Module

POSITA Would Not Use DDR2/DDR3 or Recited # of (Buck) Converters

Additional Reasons Why Dependent Claims Are Not Obvious

The Challenged Claims Are Directed to a Memory Module



US011016918B2

(12) **United States Patent**
Chen et al.

(10) **Patent No.: US 11,016,918 B2**
(45) **Date of Patent: May 25, 2021**

(54) **FLASH-DRAM HYBRID MEMORY MODULE**

(71) Applicant: **Netlist, Inc.**, Irvine, CA (US)

(72) Inventors: **Chi-She Chen**, Walnut, CA (US); **Jeffrey C. Solomon**, Irvine, CA (US); **Scott H. Milton**, Irvine, CA (US); **Jayesh Bhakta**, Cerritos, CA (US)

(73) Assignee: **Netlist, Inc.**, Irvine, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **17/138,766**

(22) Filed: **Dec. 30, 2020**

(65) **Prior Publication Data**

US 2021/0124701 A1 Apr. 29, 2021

Related U.S. Application Data

(63) Continuation of application No. 15/934,416, filed on Mar. 23, 2018, which is a continuation of application (Continued)

(51) **Int. Cl.**
G06F 13/16 (2006.01)
G06F 13/28 (2006.01)
(Continued)

(52) **U.S. Cl.**
CPC ***G06F 13/28*** (2013.01); ***G06F 1/185*** (2013.01); ***G06F 13/4013*** (2013.01);
(Continued)

(58) **Field of Classification Search**
CPC .. G06F 13/28; G06F 13/4027; G06F 13/1694; G06F 13/4223; G06F 1206/38;
(Continued)

(56) **References Cited**

U.S. PATENT DOCUMENTS

2,043,099 A 6/1936 Hanna
3,562,555 A 2/1971 Ahrens
(Continued)

FOREIGN PATENT DOCUMENTS

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KR 0130873 B1 4/1999
(Continued)

OTHER PUBLICATIONS

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(Continued)

Primary Examiner — Hashem Farrokh
(74) *Attorney, Agent, or Firm* — Shumi Messinger PLLC

(57) **ABSTRACT**

In certain embodiments, a memory module includes a printed circuit board (PCB) having an interface that couples it to a host system for provision of power, data, address and control signals. First, second, and third buck converters receive a pre-regulated input voltage and produce first, second and third regulated voltages. A converter circuit reduces the pre-regulated input voltage to provide a fourth regulated voltage. Synchronous dynamic random access memory (SDRAM) devices are coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages, and a voltage monitor circuit monitors an input voltage and produces a signal in response to the input voltage having a voltage amplitude that is greater than a threshold voltage.

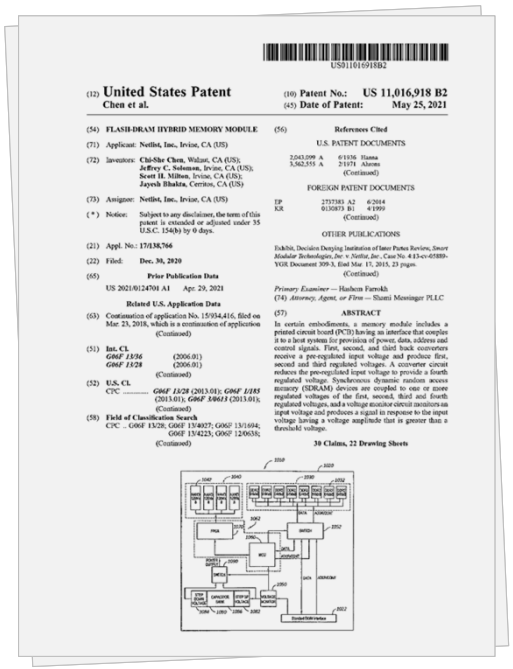
30 Claims, 22 Drawing Sheets

The ’918/’054 Patents

1. A memory module comprising:
a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;

EX1001 (Chen), Claim 1

The ’918/’054 Patents Consistently Describe Memory Modules as Connecting to The Memory Controller



US011016918B2

(12) **United States Patent**
Chen et al.

(10) **Patent No.: US 11,016,918 B2**
(45) **Date of Patent: May 25, 2021**

(54) **FLASH-DRAM HYBRID MEMORY MODULE**

(71) Applicant: **Netlist, Inc.**, Irvine, CA (US)

(72) Inventors: **Chi-She Chen**, Walnut, CA (US); **Jeffrey C. Solomon**, Irvine, CA (US); **Scott H. Milton**, Irvine, CA (US); **Jayesh Bhakta**, Cerritos, CA (US)

(73) Assignee: **Netlist, Inc.**, Irvine, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **17/138,766**

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(63) Continuation of application No. 15/934,416, filed on Mar. 23, 2018, which is a continuation of application (Continued)

(51) **Int. Cl.**
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(Continued)

(52) **U.S. Cl.**
CPC ***G06F 13/28*** (2013.01); ***G06F 1/185*** (2013.01); ***G06F 3/0613*** (2013.01);
(Continued)

(58) **Field of Classification Search**
CPC .. G06F 13/28; G06F 13/4027; G06F 13/1694; G06F 13/4223; G06F 12/0638;
(Continued)

(56) **References Cited**

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(Continued)

FOREIGN PATENT DOCUMENTS

JP 2737383 A2 6/2014
KR 0150873 B1 4/1999
(Continued)

OTHER PUBLICATIONS

Exhibit, Decision Denying Institution of Inter Partes Review, *Smart Modular Technologies, Inc v. Netlist, Inc.*, Case No. 4:13-cv-05889-YGR Document 309-3, filed May 11, 2015, 23 pages.
(Continued)

Primary Examiner — Hashem Farrokh
(74) *Attorney, Agent, or Firm* — Shumi Messinger PLLC

(57) **ABSTRACT**

In certain embodiments, a memory module includes a printed circuit board (PCB) having an interface that couples it to a host system for provision of power, data, address and control signals. First, second, and third buck converters receive a pre-regulated input voltage and produce first, second and third regulated voltages. A converter circuit reduces the pre-regulated input voltage to provide a fourth regulated voltage. Synchronous dynamic random access memory (SDRAM) devices are coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages, and a voltage monitor circuit monitors an input voltage and produces a signal in response to the input voltage having a voltage amplitude that is greater than a threshold voltage.

30 Claims, 22 Drawing Sheets

OVERVIEW

Described herein is a memory module couplable to a memory controller of a host system. The memory module

EX1001, 3:66-67

In accordance with one embodiment and as shown in FIG. **4**B, the FDHDIMM **400'** receives control signals **408** from the MCH, where the control signals may include one or more control signals specifically for the DRAM **402'** operation and one or more control signals specifically for the

EX1001, 12:44-48

FIGS. **5**A and **5**B are block diagrams of a memory module **500** that is couplable to a host system (not shown). The host system may be a server or any other system comprising a memory system controller or an MCH for providing and controlling the read/write access to one or more memory systems, wherein each memory system may include a plu-

EX1001, 12:52-57

Patent Owner Response (918) at 2.
Patent Owner Sur-Reply (918) at 1.
Patent Owner Sur-Reply (054) at 1.

The District Court: The Invention Is Directed to Memory Modules That Connect To the Memory Controller (i.e., Main Memory)

devices by the claims. To the contrary, as the Overview section explains, the invention "is couplable *to a memory controller* of a host system," '918 Patent at 3:66–67 (emphasis added), not just the host system as recited in the claims. *See also id.* at 1:66–67 ("[t]he present disclosure relates generally to computer memory devices"). Thus, a skilled artisan would understand a "memory module" is distinct from, and has essential structural requirements not necessarily found in, other modular computer accessories. That includes the structure necessary to connect to a memory controller. *See Memory Systems: Cache, DRAM, Disk*, Dkt. No. 76-17 at 319 (depicting, in FIG. 7.6, a memory controller connected to two memory modules). Accordingly, the preambles are limiting.

EX2032 (Samsung's Objections to Claim Construction Order), 28

Patent Owner Response (918) at 2; Patent Owner Response (054) at 3.
Patent Owner Sur-Reply (918) at 1; Patent Owner Sur-Reply (054) at 1.

The District Court: The Recited "Memory Module" Includes Structure Necessary To Connect To A Memory Controller

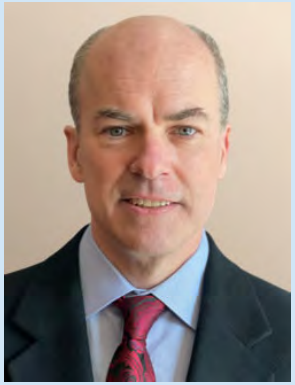
devices by the claims. To the contrary, as the Overview section explains, the invention "is coupable *to a memory controller* of a host system," '918 Patent at 3:66–67 (emphasis added), not just the host system as recited in the claims. *See also id.* at 1:66–67 ("[t]he present disclosure relates generally to computer memory devices"). Thus, a skilled artisan would understand a "memory module" is distinct from, and has essential structural requirements not necessarily found in, other modular computer accessories. That includes the structure necessary to connect to a memory controller. *See Memory Systems: Cache, DRAM, Disk*, Dkt. No. 76-17 at 319 (depicting, in FIG. 7.6, a memory controller connected to two memory modules). Accordingly, the preambles are limiting.

EX2032 (Samsung's Objections to Claim Construction Order), 28

Court cited to same FIG. 7.6 of EX2034

Patent Owner Response (918) at 2; Patent Owner Response (054) at 3.
Patent Owner Sur-Reply (918) at 1; Patent Owner Sur-Reply (054) at 1.

Memory Modules That Connect to The Memory Controller via Memory Buses Are Main Memory Modules



William Mangione-Smith
Netlist's Expert

NETLIST

JEDEC-Style Memory Architecture

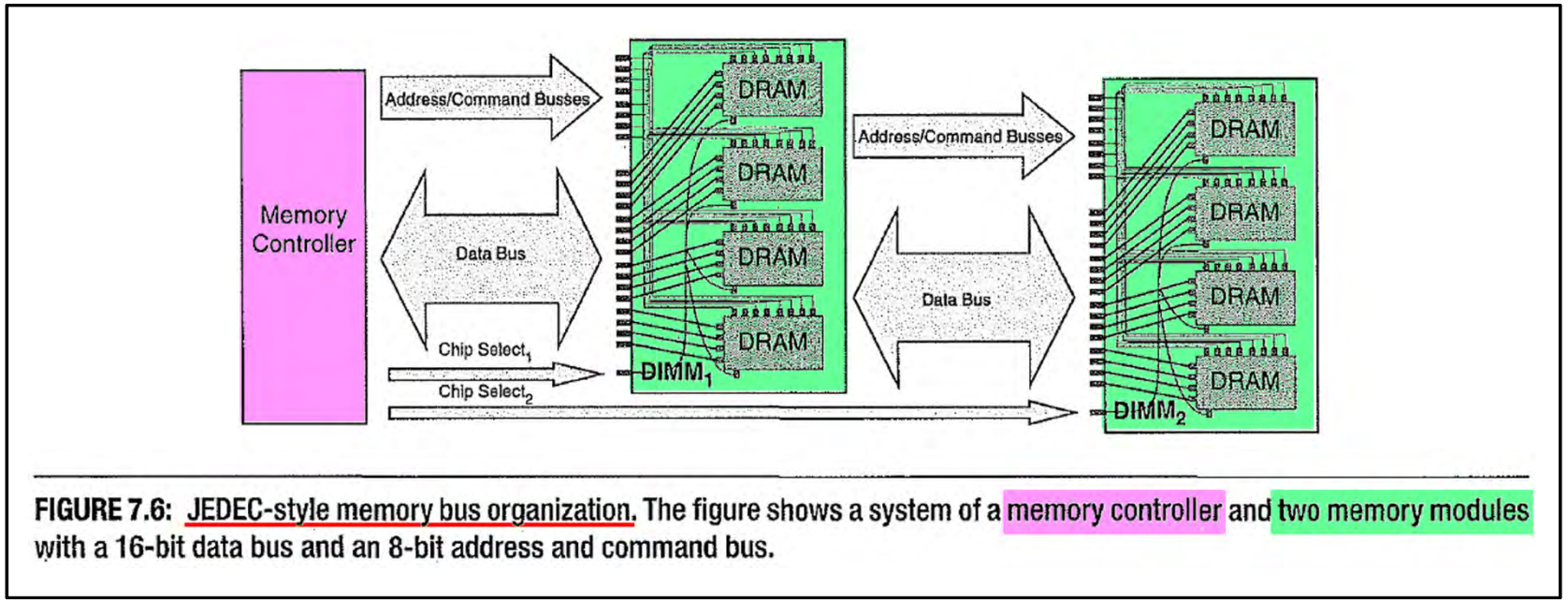


FIGURE 7.6: JEDEC-style memory bus organization. The figure shows a system of a memory controller and two memory modules with a 16-bit data bus and an 8-bit address and command bus.

EX2031 (918) (Mangione-Smith Declaration), ¶53 (citing EX2034 (Memory Systems), at 319.
EX2061 (054) (Mangione-Smith Declaration), ¶53 (citing EX2034 (Memory Systems), at 319.

Patent Owner Response (918) at 2-3.
Patent Owner Response (054) at 4.

Dr. Wolfe: Main Memory Modules Connect To The Memory Controller

Andrew Wolfe
Samsung's Expert

SAMSUNG

> Q. When you say "main memory modules," what do you mean?
>
> A. Memory modules that are designed to connect to the primary memory controller for the purpose of holding general purpose code and data in a computer system.

EX2030 (918) (Wolfe Deposition), 123:20-25.
EX2060 (054) (Wolfe Deposition), 123:20-25.

Patent Owner Response (918) at 2.
Patent Owner Response (054) at 3-4.

Petitioner Did Not Object To the Court's Findings On The Meaning of "Memory Module"

"A memory module"	
Defendants' Proposed Construction	**Order**
Preamble is non-limiting	Preamble is limiting

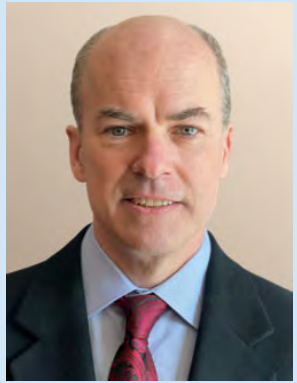
The Order erred in finding the preamble limiting. For the reasons stated in Samsung's claim construction brief, Samsung requests the Court adopt Samsung's construction. Dkt. 82 at 12-13. Each of the claims at issue recite a structurally complete invention, and as a result, the preambles are non-limiting statements of intended purpose. *See Catalina Mktg. Int'l, Inc. v. Coolsavings.com, Inc.*, 289 F.3d 801, 808 (Fed. Cir. 2002) (internal citations, quotations omitted).

EX2033 (Samsung's Objections to Claim Construction Order), 3.

Petitioner only objected to the Court's finding that the preamble is limiting, not to the Court's findings as what a "memory module means to a POSA.

Patent Owner Response (918) at 2.
Patent Owner Response (054) at 3.

The Recited "Memory Modules" Are Main Memory Modules That Connect to The Memory Controller



William Mangione-Smith
Netlist's Expert

NETLIST

and data in a computer system." EX2030, 123:14-25. I agree, and in my experience, at the time of the invention and in the context of the '918 patent, the term "memory module" would be understood by a POSITA to refer to a module that is to be inserted into a dedicated memory slots and that includes structures necessary to connect to a memory controller for use as memory. See '918, 3:66-67; see also below.

EX2031 (Mangione-Smith Declaration), ¶53.

Both the intrinsic and extrinsic evidence support interpreting "memory modules" as main memory modules that include structures to connect to a memory controller.

Patent Owner Response (918) at 2-3.

TOPICS

GROUNDS 1-3

Harris Does Not Receive Power Via Edge Connections

Harris Does Not Receive The Recited Signals From the Host

A POSITA Would Not Have Used the Required # of (Buck) Converters

Ground 2 ASSUMES Separate Converters To Supply Each FBDIMM-Required Voltage

A POSITA Would Not Have Replaced Harris' Redundant Power

Additional Reasons Why Dependent Claims Are Not Obvious

GROUNDS 4-5

The Recited "Memory Module" Means A Main Memory Module

Spiers' PCI Card Is Not a Memory Module

POSITA Would Not Use DDR2/DDR3 or Recited # of (Buck) Converters

Additional Reasons Why Dependent Claims Are Not Obvious

The Petition Relies on Spiers' PCI Card As The Recited "Memory Module"

The Petition

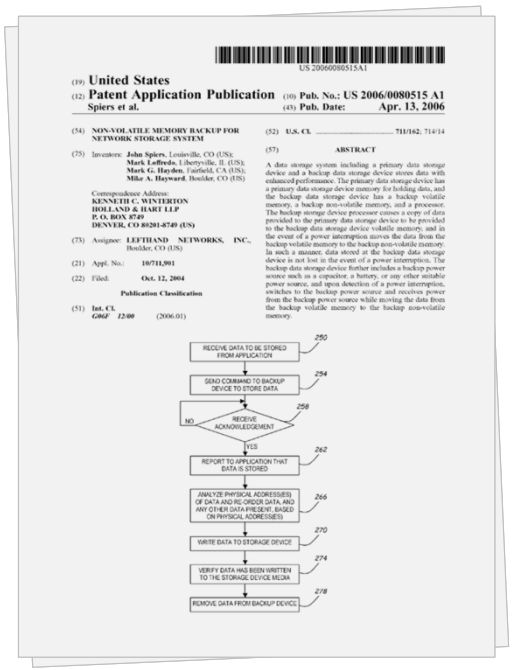
2. Independent Claim 1

a) [1.a] Preamble

To the extent the preamble is limiting, Grounds 4A-4C teach "*[a] memory module comprising* [e.g., Spiers's backup device 144 (below) implemented in a PCI card including volatile memory (SDRAMs 190, yellow) and non-volatile memory (NAND Flash 194, green), and configured to store data in a memory system]." EX1003, ¶¶643-646; EX1025, ¶¶[0034, 37], Figs. 3, 5.

Petition (918) at 82.

Spiers' Backup Device



US 20060080515A1

(19) United States
(12) Patent Application Publication (10) Pub. No.: US 2006/0080515 A1
Spiers et al. (43) Pub. Date: Apr. 13, 2006

(54) NON-VOLATILE MEMORY BACKUP FOR NETWORK STORAGE SYSTEM

(75) Inventors: John Spiers, Louisville, CO (US); Mark Loffredo, Libertyville, IL (US); Mark G. Hayden, Fairfield, CA (US); Mike A. Hayward, Boulder, CO (US)

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P. O. BOX 8749
DENVER, CO 80201-8749 (US)

(73) Assignee: LEFTHAND NETWORKS, INC., Boulder, CO (US)

(21) Appl. No.: 10/711,901

(22) Filed: Oct. 12, 2004

Publication Classification

(51) Int. Cl.
G06F 12/00 (2006.01)

(52) U.S. Cl. 711/162; 714/14

(57) ABSTRACT

A data storage system including a primary data storage device and a backup data storage device stores data with enhanced performance. The primary data storage device has a primary data storage device memory for holding data, and the backup data storage device has a backup volatile memory, a backup non-volatile memory, and a processor. The backup storage device processor causes a copy of data provided to the primary data storage device to be provided to the backup data storage device volatile memory, and in the event of a power interruption moves the data from the backup volatile memory to the backup non-volatile memory. In such a manner, data stored at the backup data storage device is not lost in the event of a power interruption. The backup data storage device further includes a backup power source such as a capacitor, a battery, or any other suitable power source, and upon detection of a power interruption, switches to the backup power source and receives power from the backup power source while moving the data from the backup volatile memory to the backup non-volatile memory.

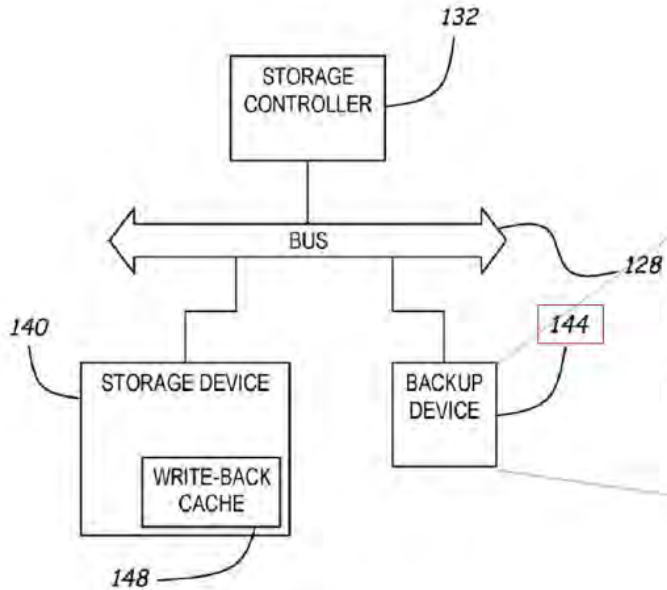


FIG.3

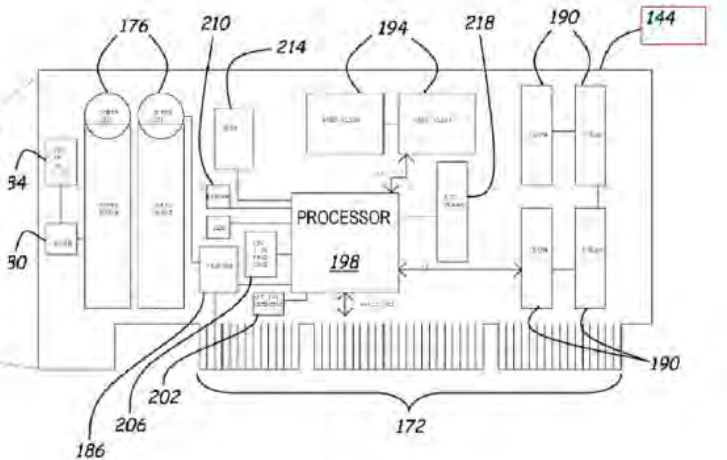


FIG.5

Dr. Wolfe: Spiers' PCI Card Is Allegedly A "Memory Module" Because It Includes Memories Mounted On It

Andrew Wolfe
Samsung's Expert

SAMSUNG

> 644. A Skilled Artisan would have understood that this backup device is a "*memory module*" because it includes a card (PCI card) with memories mounted on it and configured to store data received from the system, as shown in Figure 3 of Spiers reproduced below.

EX1003 (918) (Wolfe Declaration), ¶644.
EX1003 (054) (Wolfe Declaration), ¶598.

Every Graphics Card and System on Chip Is A Memory Module Under Dr. Wolfe's Interpretation

Petition (918) at 82.
Petition (054) at 77-78.

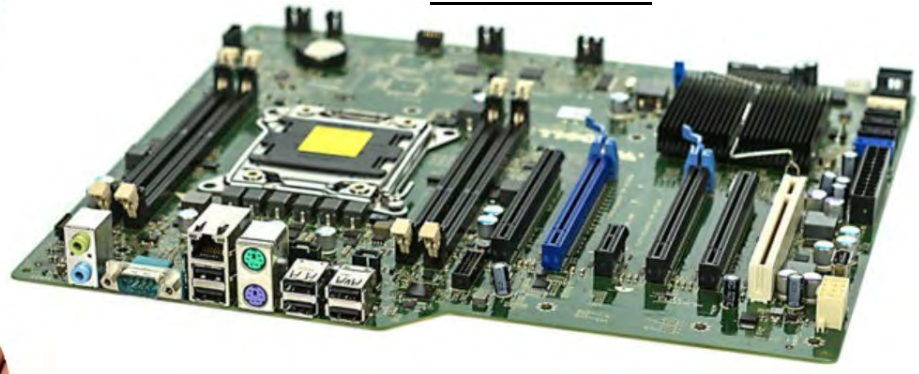
Under Dr. Wolfe's Interpretation, These Are "Memory Modules" Because They Have Memories Mounted On Them

Andrew Wolfe
Samsung's Expert

SAMSUNG

Graphics Card

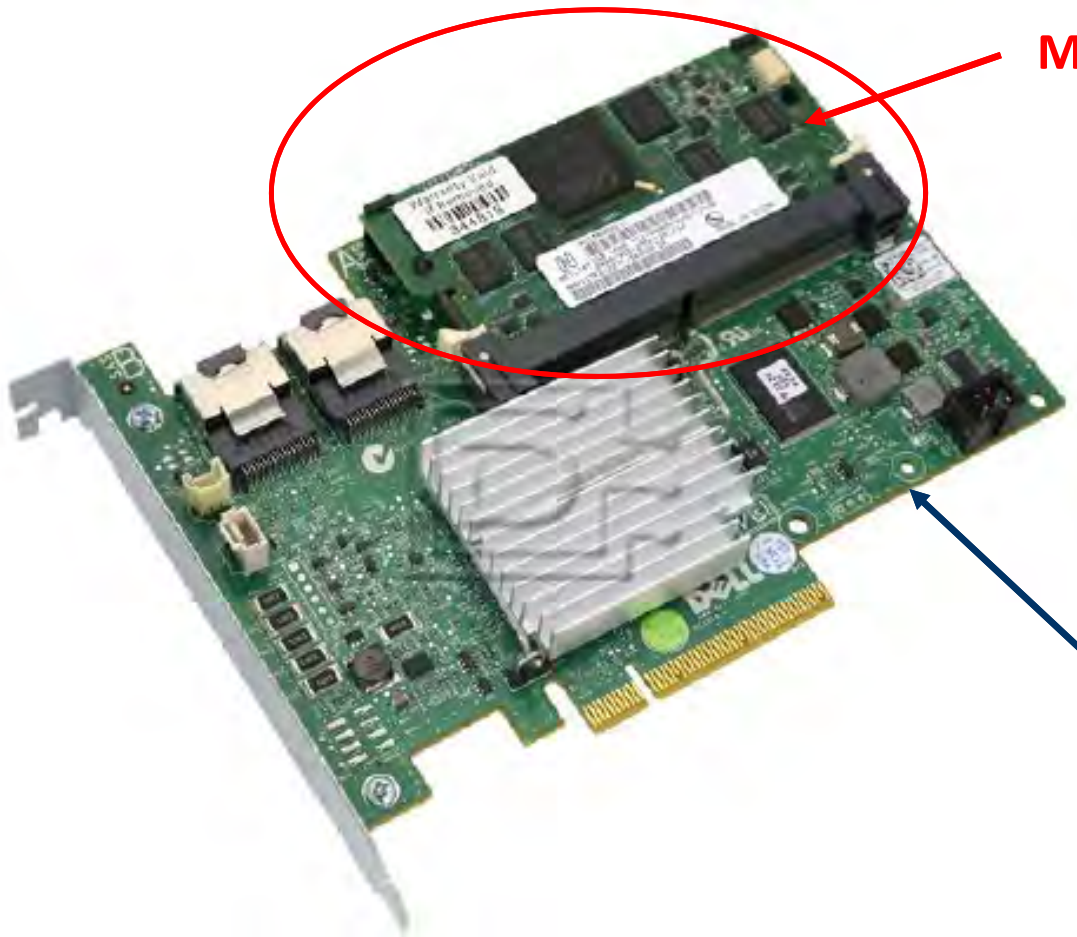
Motherboard



Gaming Console

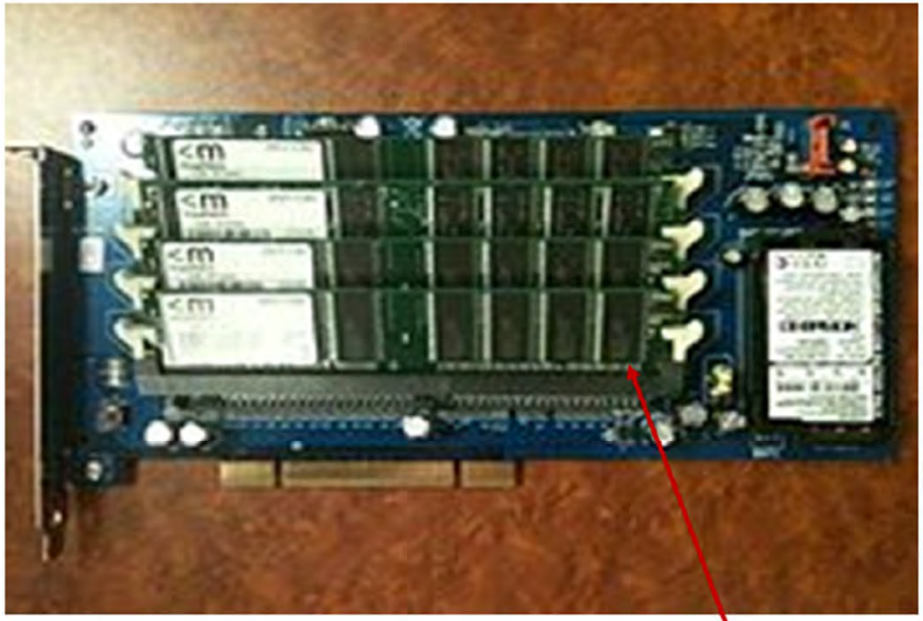
Patent Owner Response (918) at 46.
Patent Owner Response (054) at 49.

Memory Module on a PCI Card is a Separate Component



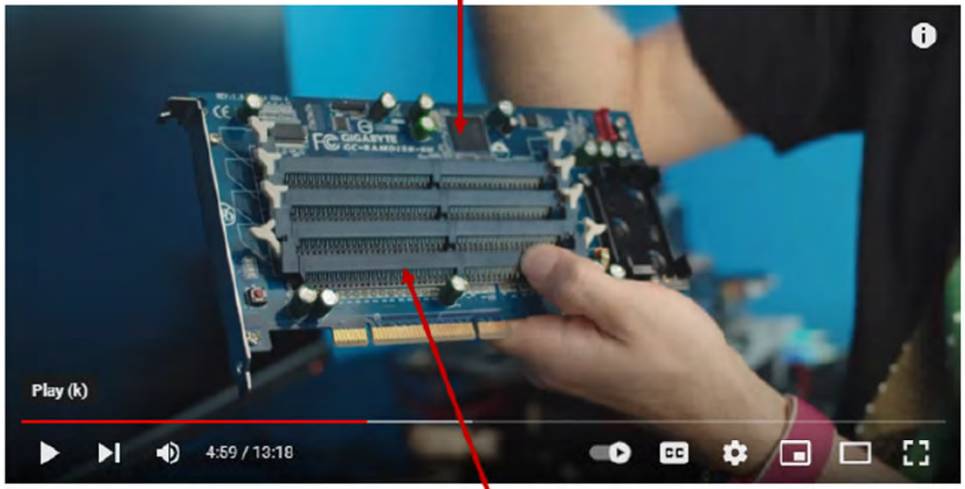
Patent Owner Response (918) at 47.
Patent Owner Response (054) at 51.

A PCI Card includes Memory Modules and Other Components



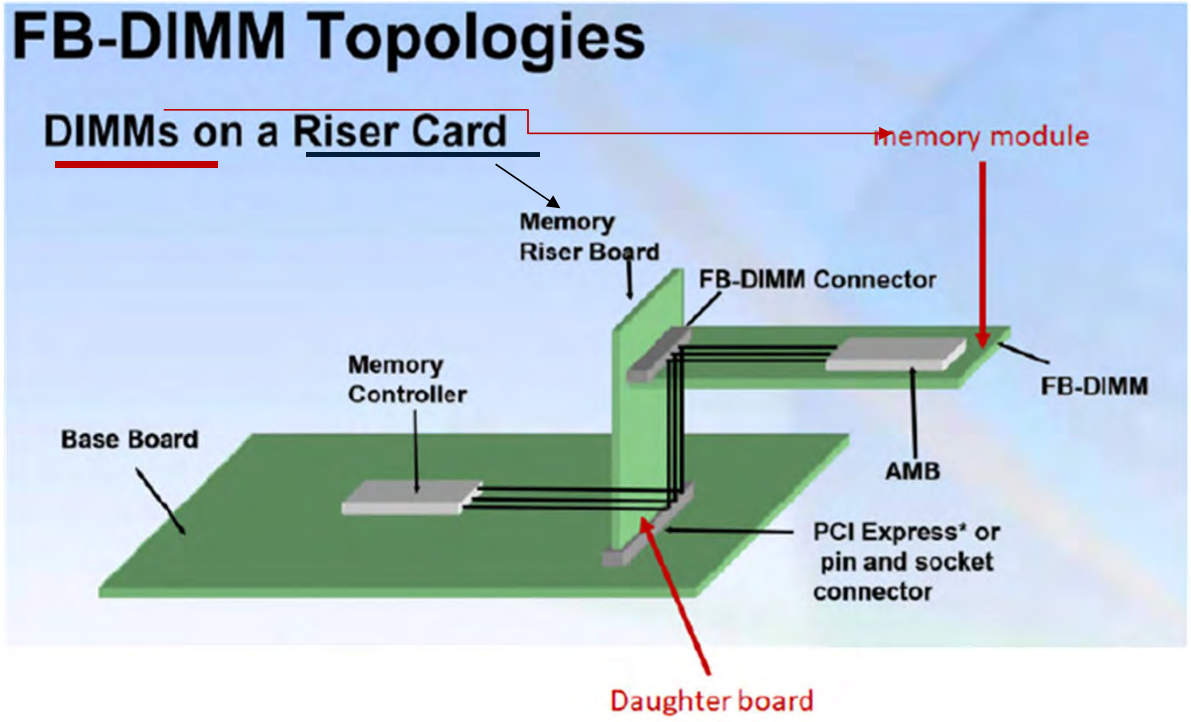
4 slots on PCI populated with 4 DIMMs

FPGA memory controller



4 slots on PCI for up to 4 DIMMs

Memory Module on a Card is a Separate Component



William Mangione-Smith

NETLIST

Q. Is the memory riser board part of that memory module?

A. No, it's not.

EX1075, 223:24-225:9 (Mangione-Smith)

Patent Owner Sur-Reply (918) at 27.
Patent Owner Sur-Reply (054) at 27-28.

Memory Modules Receive Address and Control Signals Across Interface

918 Patent

1. A memory module comprising:
a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;

054 Patent

1. A memory module comprising:
a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;

Spiers' PCI Card Is Not a "Memory Module"

NETLIST

- **<u>Control signals for memory do not come across interface.</u>**
- Spiers' PCI card is a host system for memory modules. Reply 2.

Patent Owner Response (918) at 45-47; Patent Owner Response (054) at 47-51.
Patent Owner Sur-Reply (918) at 23-27; Patent Owner Sur-Reply (054) at 24-28.

Spiers' PCI Card Does Not Receive Control Signals Across Interface For Memory

Andrew Wolfe
Samsung's Expert

SAMSUNG

Q. Does the **storage controller 132 provide timing and control signals** to the NAND flash on the PCI card?

A. **No**.

EX2030 (918), 214:23-215:2 (objections omitted)
EX2060 (054), 214:23-215:2 (objections omitted)

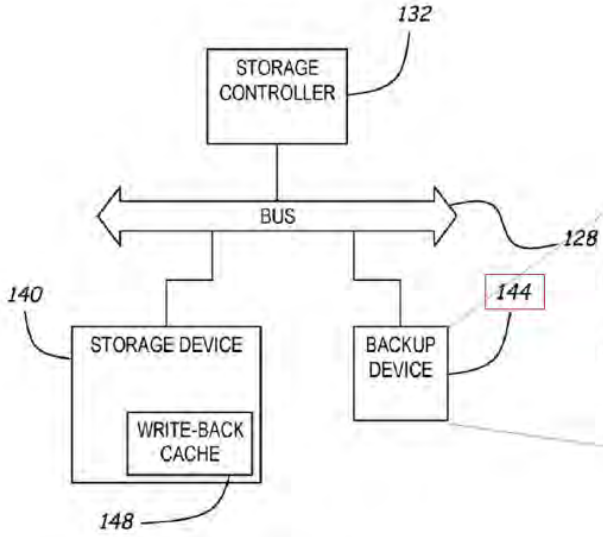


FIG.3

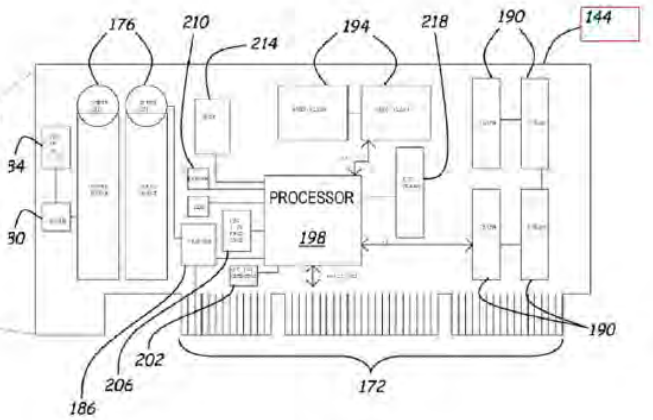


FIG.5

Patent Owner Response (918) at 45; Patent Owner Response (054) at 48.
Patent Owner Sur-Reply (918) at 25; Patent Owner Sur-Reply (054) at 25.

Spiers' PCI Card Does Not Receive Control Signals Across Interface For Memory

Andrew Wolfe
Samsung's Expert

SAMSUNG

Q. Okay. So does the **memory controller within the storage controller 132 provide the timing and control signals** to the NAND flash on the PCI card?

A. No.

Q. Does the **memory controller within the storage controller 132 provide the timing and control signals** to the SDRAM on the PCI card?

A. No.

EX2030 (918), 215:14-24 (objections omitted)
EX2060 (054), 215:14-24 (objections omitted

Patent Owner Response (918) at 45; Patent Owner Response (054) at 48.
Patent Owner Sur-Reply (918) at 25; Patent Owner Sur-Reply (054) at 25.

Petitioner's Alleged Voltage Converters Are Not On Spiers' Memory Modules

Petitioner's alleged converters providing regulated voltages VCC, VDD, VDDQ, VTT, etc.

Spiers' source of memory control signals

Spiers' memory modules

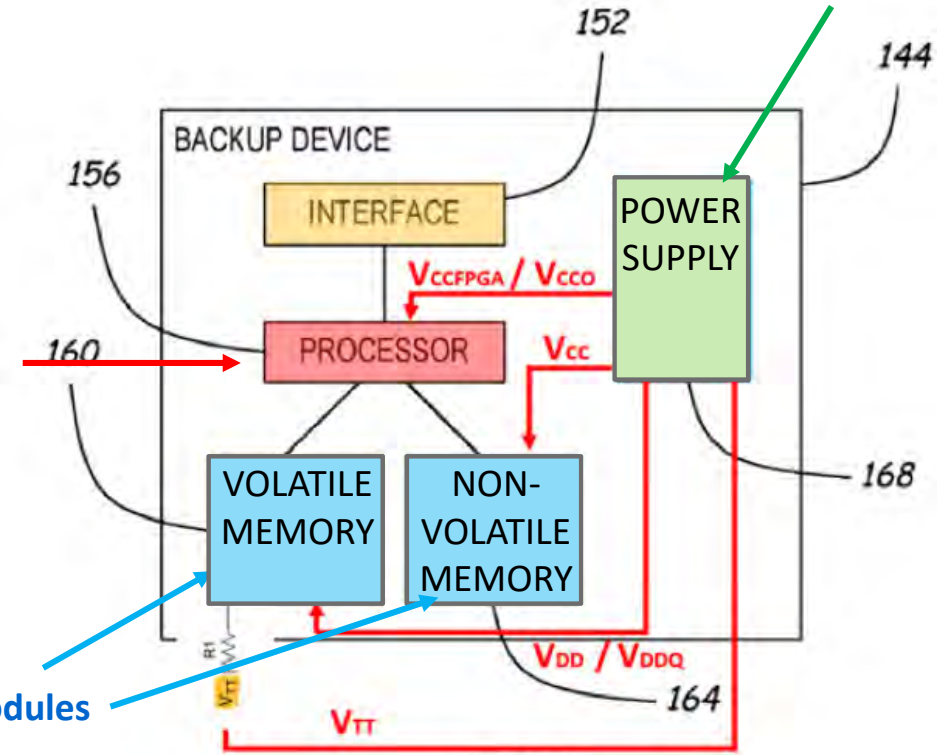


FIG.4

Petition (918) at 78.
Petition (054) at 73.

Spiers' PCI Card Does Not Receive Control Signals Across Interface For Memory

Andrew Wolfe
Samsung's Expert

SAMSUNG

Q. And so the only memory controller that provides the timing and control signals to the SDRAM and the NAND flash on the PCI card is the memory controller within processor 198 on the PCI card; is that correct?

A. There would likely be multiple memory controllers within 198, one for the NAND flash and one for the SDRAM.

***

Q. Okay. So the memory controllers that provide the timing and the control signals to the memories on the PCI card, are those residing within processor 198? Is that fair?

A. Yes.

EX2030 (918), 216:2-17 (objections omitted).
EX2060 (054), 216:2-17 (objections omitted).

Patent Owner Response (918) at 45; Patent Owner Response (054) at 48.
Patent Owner Sur-Reply (918) at 25; Patent Owner Sur-Reply (054) at 25.

Spiers' Converters Are Not On The Memory Modules

RED: Source of memory control signals

Blue:
Spiers' memory modules

Green:
Alleged converters

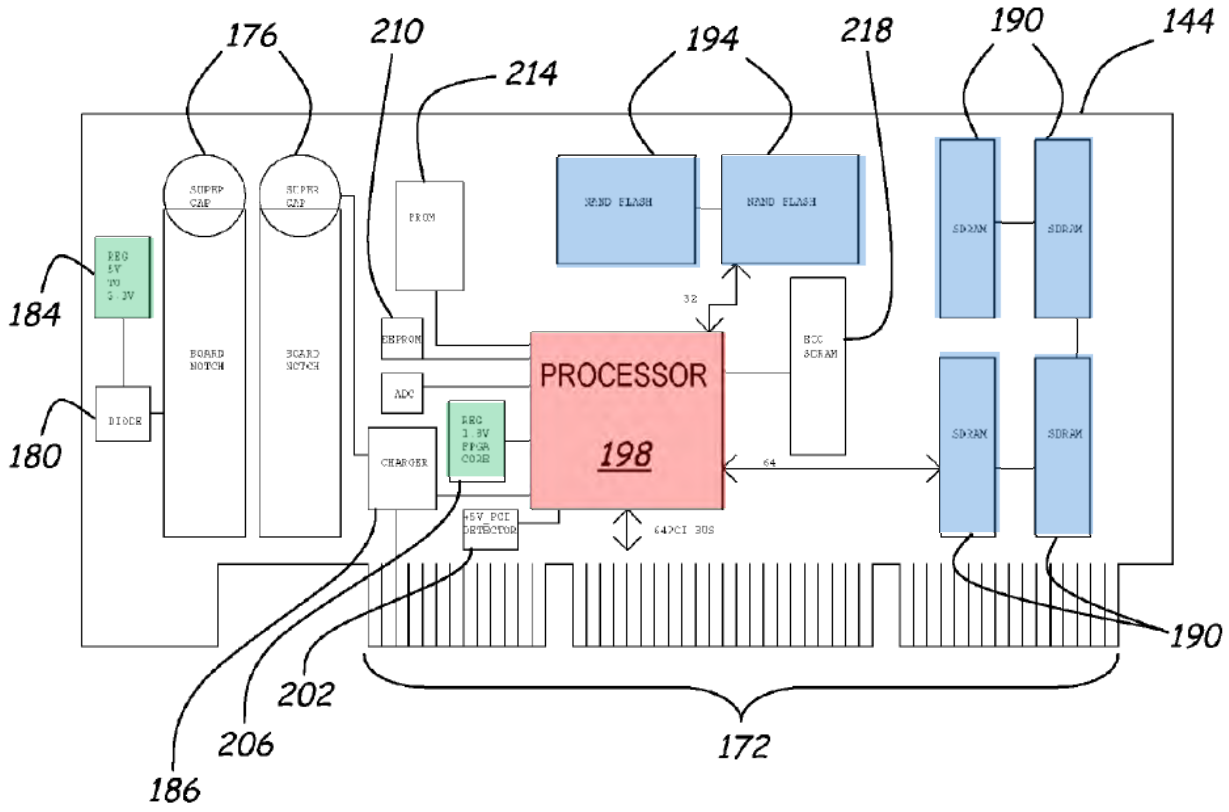


FIG.5

Patent Owner Response (918) at 45; Patent Owner Response (054) at 48-49.
Patent Owner Sur-Reply (918) at 25; Patent Owner Sur-Reply (054) at 25-26.

Spiers' PCI Card Does Not Connect To A Memory Controller

Andrew Wolfe
Samsung's Expert

SAMSUNG

Q. What is a memory controller?

A. Again, it depends on context, but in the context of an ordinary microprocessor, it's **the interface that provides the timing and control signals to memory**.

EX2030, 213:24-214:4 (objections omitted)
EX2060, 213:24-214:4 (objections omitted)

Patent Owner Response (918) at 45; Patent Owner Response (054) at 48.
Patent Owner Sur-Reply (918) at 25; Patent Owner Sur-Reply (054) at 25.

Spiers' PCI Card Does Not Need To Connect To A Memory Controller

Andrew Wolfe
Samsung's Expert

SAMSUNG

Dr. Wolfe confirmed (and the Reply does not dispute) that:

- the memory controllers that provide the timing and control signals to the memory on Spiers' PCI card reside only in the microprocessor 198 on the PCI card.

EX2030, 216:2-17, 214:6-10.
EX2060, 216:2-17, 214:6-10.

Dr. Mangione-Smith confirmed the same. EX2031, ¶129

Patent Owner Response (918) at 45; Patent Owner Response (054) at 48.
Patent Owner Sur-Reply (918) at 25; Patent Owner Sur-Reply (054) at 25.

Memory Controllers For Spiers' Memories Reside On The PCI Card

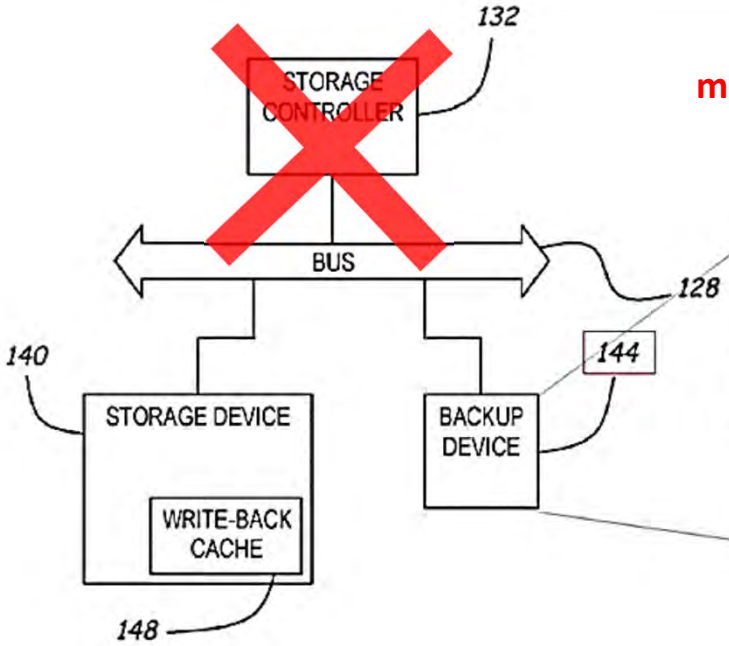


FIG.3

Onboard memory controllers for memory modules inserted into PCI card's memory slots

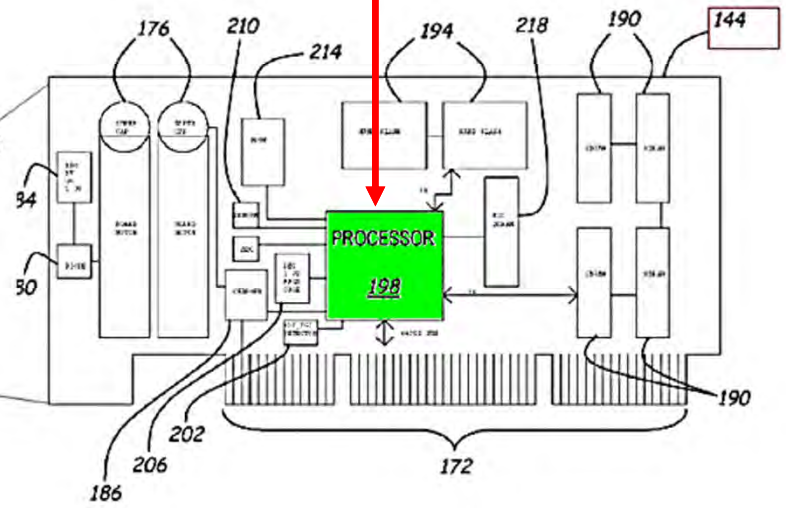


FIG.5

Because Spiers' PCI Card contains onboard memory controllers, Spiers' PCI card is not a "memory module" because it does not connect to a memory controller (nor need to)

Patent Owner Response (918) at 45; Patent Owner Response (054) at 48.
Patent Owner Sur-Reply (918) at 25; Patent Owner Sur-Reply (054) at 25.

Spiers' PCI Card Is Not a "Memory Module"

NETLIST

- Control signals for memory do not come across interface.
- **Spiers' PCI card is a host system for memory modules**. Reply 2.

Patent Owner Response (918) at 45-47; Patent Owner Response (054) at 47-51.
Patent Owner Sur-Reply (918) at 23-27; Patent Owner Sur-Reply (054) at 24-28.

Petitioner's New Construction of Memory Module In Reply

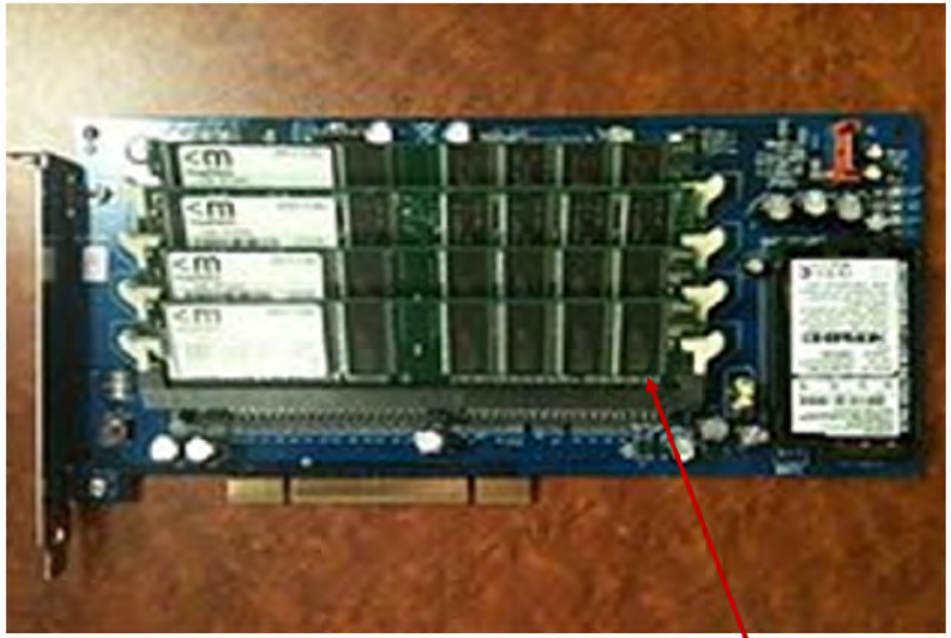
"Netlist misleadingly quotes statements by Dr. Wolfe about "***main*** memory modules," POR 3-4, but Dr. Wolfe explained that in the context of ***this*** patent, a "memory module" is ***not*** limited to main memory or to any specific connection, EX2060, 125:12-127:13 ("memory module" is "a circuit board that connects to a host computer that includes memory"); *see also* EX2056, 100:15-101:19 (similar)."

Patent Owner Sur-Reply (054) at 2.

Spiers' PCI Card Is Not a "Memory Module"

NETLIST

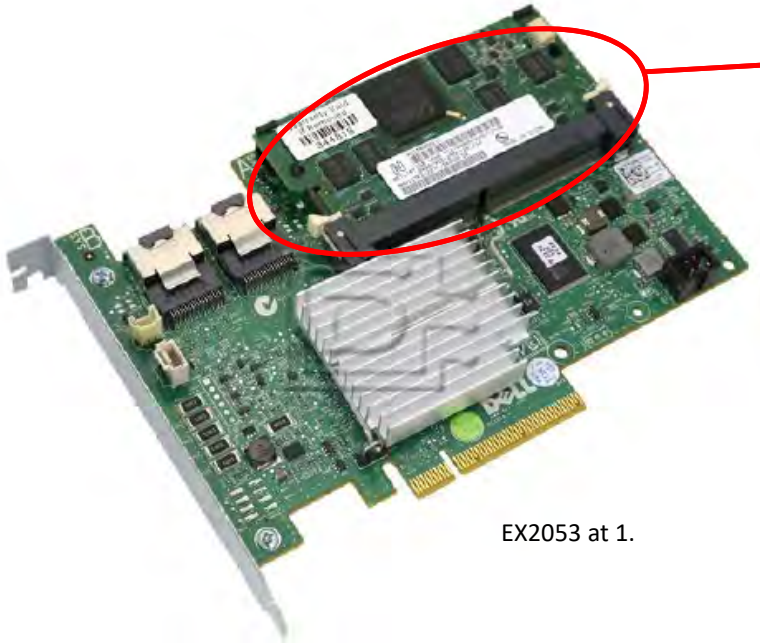
In Spier's PCI card, the memory is included on the separate SDRAM/NAND module cards, not on the PCI card.



Patent Owner Sur-Reply (918) at 23-24.
Patent Owner Sur-Reply (054) at 24-26.

Spiers' PCI Card Is Not a "Memory Module"

A PCI-Express card with a Netlist NVDIMM.



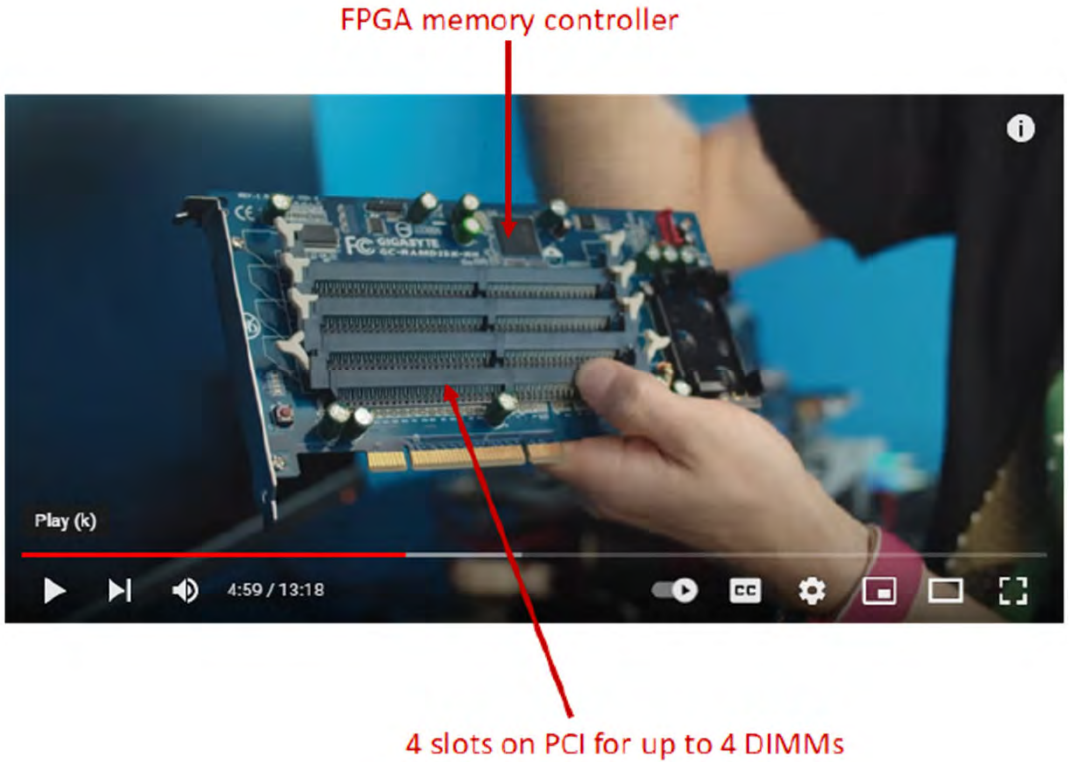
EX2053 at 1.

The "memory module" is the NVDIMM, not the PCI card).

Patent Owner Response (918) at 47; Patent Owner Response (054) at 51.
Patent Owner Sur-Reply (918) at 24; Patent Owner Sur-Reply (054) at 25.

Spiers-Type PCI Cards Were Known To Include Onboard Memory Controllers And DIMM Slots

NETLIST



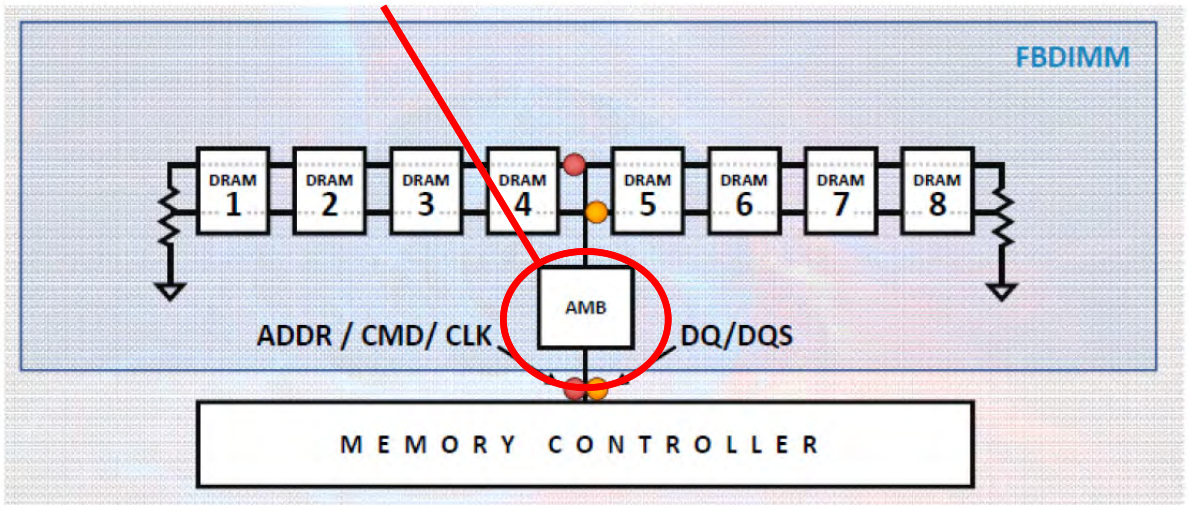
Spiers' PCI card is no more a memory module than a graphics card containing DRAM memory, a motherboard having memory slots filled by DIMMs, or a computer with DRAM modules.

Patent Owner Response (918) at 46.
Patent Owner Sur-Reply (918) at 26; Patent Owner Sur-Reply (054) at 26.

AMBs Do Not Satisfy Petitioner's Definition of Memory Controller

NETLIST

AMB Does Not Satisfy Dr. Wolfe's Definition



Andrew Wolfe
Samsung's Expert

SAMSUNG

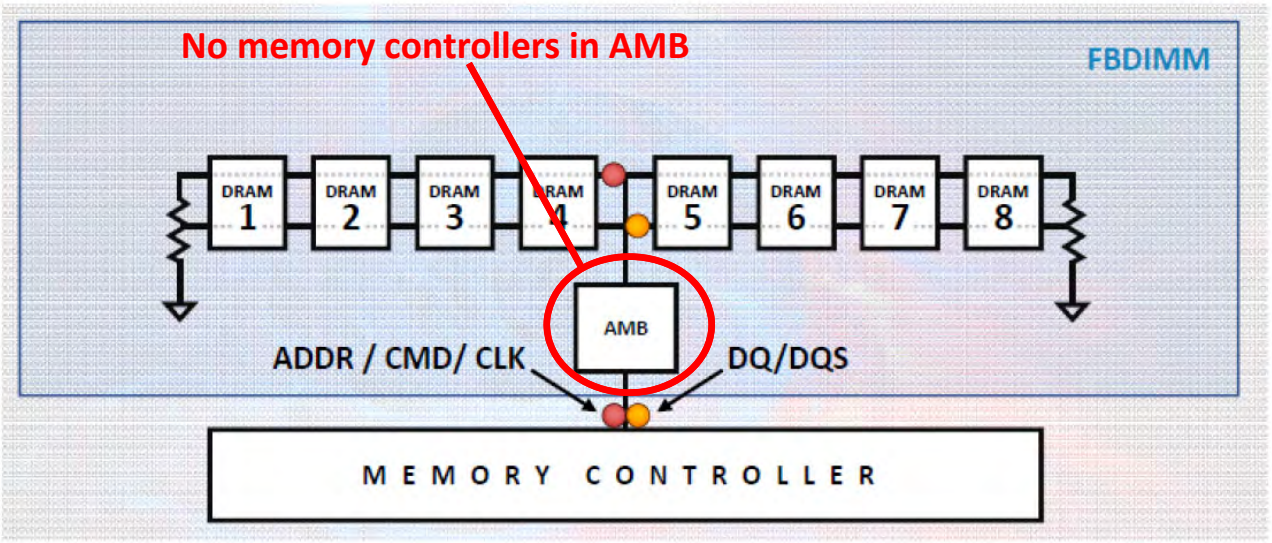
Q. What is a memory controller?

A. Again, it depends on context, but in the context of an ordinary microprocessor, it's the interface that provides the timing and control signals to memory.

EX2030 (918), 213:24-214:4 (objections omitted).
EX2060 (054), 213:24-214:4 (objections omitted).

Petitioner's Reply (918) at 25; Petitioner's Reply (054) at 25.
Patent Owner Response (918) at 45; Patent Owner Response (054) at 48.
Patent Owner Sur-Reply (918) at 26; Patent Owner Sur-Reply (054) at 26.

AMBs Do Not Satisfy Petitioner's Definition of Memory Controller



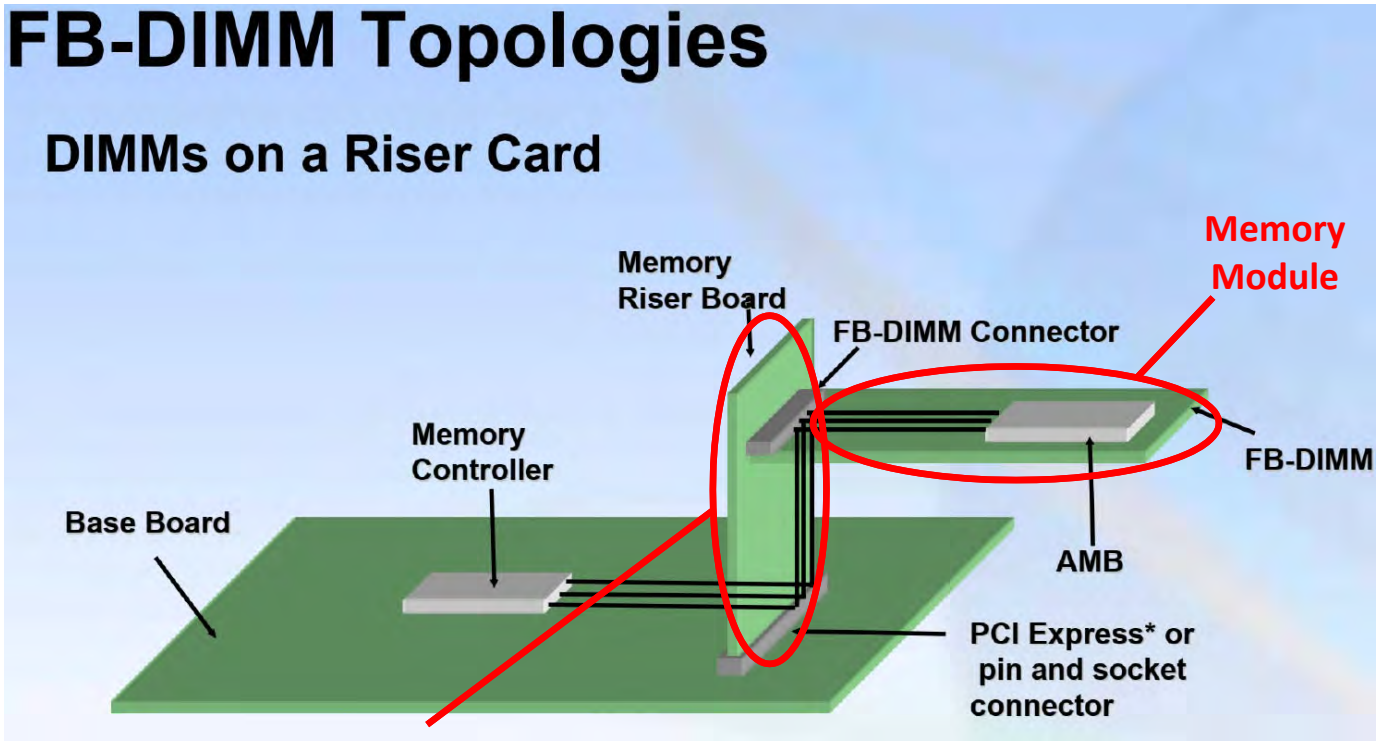
Dr. Wolfe confirmed that:

- "the memory controllers that provide the timing and control signals to the memory on Spiers' PCI card reside only in the microprocessor 198 on the PCI card."

EX2030 (918), 216:2-17, 214:6-10.
EX2060 (054), 216:2-17, 214:6-10.

Petitioner's Reply (918) at 25; Petitioner's Reply (054) at 25.
Patent Owner Response (918) at 45; Patent Owner Response (054) at 48.
Patent Owner Sur-Reply (918) at 25-26; Patent Owner Sur-Reply (054) at 26-27.

Petitioner's Reply Argument Fails: Unlike Spiers' PCI Card, The PCI Riser Board Does Not Have A Memory



EX1075 (Mangione-Smith) 223:24-225:9 (discussing EX2101, p.14, "Q: Is the memory riser board part of that memory module? A: No, it's not.").

Petitioner's Reply (918) at 25-26; Petitioner's Reply (054) at 26-27.
Patent Owner Sur-Reply (918) at 26-27; Patent Owner Sur-Reply (054) at 26-27.

TOPICS

GROUNDS 1-3

Harris Does Not Receive Power Via Edge Connections

Harris Does Not Receive The Recited Signals From the Host

A POSITA Would Not Have Used the Required # of (Buck) Converters

Ground 2 ASSUMES Separate Converters To Supply Each FBDIMM-Required Voltage

A POSITA Would Not Have Replaced Harris' Redundant Power

Additional Reasons Why Dependent Claims Are Not Obvious

GROUNDS 4-5

The Recited "Memory Module" Means A Memory Module

Spiers' PCI Card Is Not a Main Memory Module

POSITA Would Not Use DDR2/DDR3 or Recited # of (Buck) Converters

Additional Reasons Why Dependent Claims Are Not Obvious

Ground 4 Requires Modifying Spiers With DDR2/DDR3 Modules

Ground 4: Spiers in view of Amidi, with DDR2 or DDR3 DRAMs

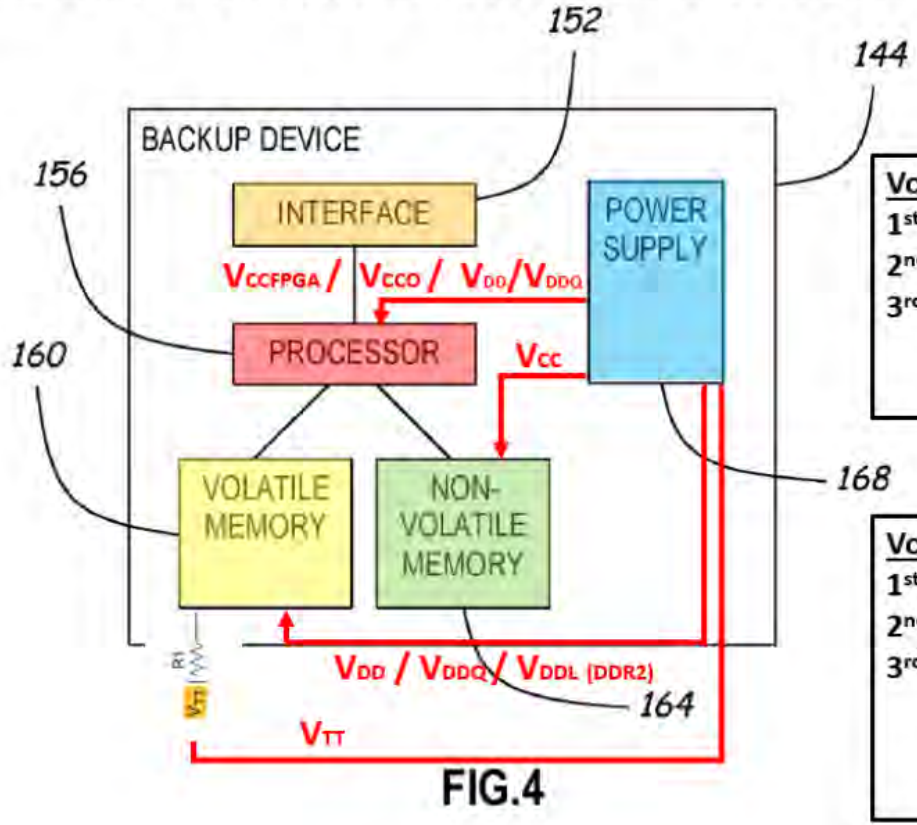


FIG.4

Voltage Mapping (A) for DDR3

1st : V_{DD}/V_{DDQ} to DRAM/FPGA = 1.5V
2nd : V_{CCFPGA} to FPGA Core = 1.8V
3rd : (i) V_{TT} to DRAM Bus = 0.75V
(ii) V_{CC} to NV Memory = 3.3V
(iii) V_{CCO} to FPGA I/O = 3.3V

Voltage Mapping (B) for DDR2

1st : V_{DD}/V_{DDQ} to DRAM/FPGA = 1.8V
2nd : V_{CCFPGA} to FPGA Core = 1.8V
3rd : (i) V_{TT} to DRAM Bus = 0.9V
(ii) V_{CC} to NV Memory = 3.3V
(iii) V_{CCO} to FPGA I/O = 3.3V
(iv) V_{DDL} to DRAM = 1.8V

Petition (054) at 73.

Ground 4 Requires Modifying Spiers With DDR2/DDR3 Modules

Ground 4: Spiers in view of Amidi, with DDR2 or DDR3 DRAMs

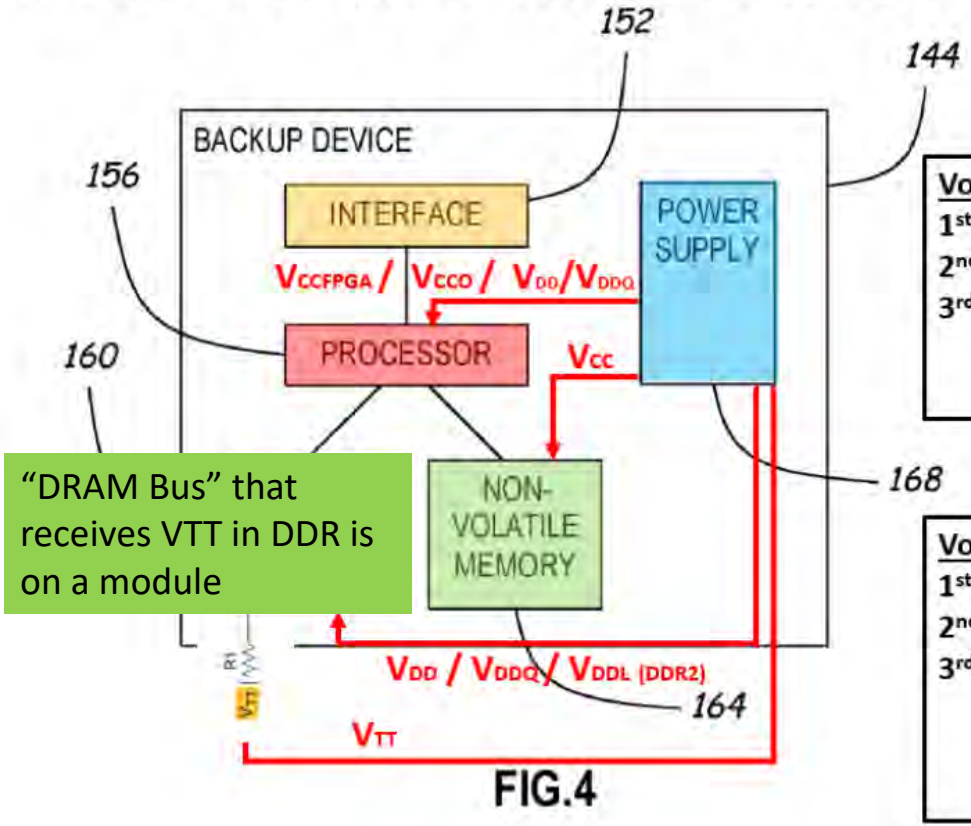


FIG.4

"DRAM Bus" that receives VTT in DDR is on a module

Voltage Mapping (A) for DDR3
1st : V_{DD}/V_{DDQ} to DRAM/FPGA = 1.5V
2nd : V_{CCFPGA} to FPGA Core = 1.8V
3rd : (i) V_{TT} to DRAM Bus = 0.75V
(ii) V_{CC} to NV Memory = 3.3V
(iii) V_{CCO} to FPGA I/O = 3.3V

Voltage Mapping (B) for DDR2
1st : V_{DD}/V_{DDQ} to DRAM/FPGA = 1.8V
2nd : V_{CCFPGA} to FPGA Core = 1.8V
3rd : (i) V_{TT} to DRAM Bus = 0.9V
(ii) V_{CC} to NV Memory = 3.3V
(iii) V_{CCO} to FPGA I/O = 3.3V
(iv) V_{DDL} to DRAM = 1.8V

Petition (054) at 73.

VTT Termination is On a DIMM

JEDEC
STANDARD

FBDIMM:
Advanced Memory Buffer (AMB)

3.3 Command / Address Outputs

The DDR2 command and address signals are terminated to 0.9V on the DIMM. In order to reduce power, this termination is performed using series resistors to a Vtt power supply, which is generated by voltage regulators on the system board and provided to the DIMM via connector pins. This power supply must be capable of sourcing and syncing current.

EX 1027, at 20.

Patent Owner Response (918) at 28.
Patent Owner Response (054) at 32.

Petition Incorporates JEDEC Specifications Into Grounds 4/5

DDR2/DDR3 not in proposed combinations

B. Identification of Challenge (§42.104(b))

Petitioner challenges claims 1-30 of the 918 Patent as follows:

Ground	Claims Challenged	35 U.S.C. §	References
1	1-3, 8, 14-15, 23	103(a)	Harris + FBDIMM Standards
2	1-30	103(a)	Ground 1 + Amidi
3	1-30	103(a)	Ground 2 + Hajeck
4	1-30	103(a)	Spiers+Amidi
5	1-30	103(a)	Ground 4 + Hajeck

a fourth voltage amplitude ["4th"/"*fourth*" below]," when backup device 144 is implemented with DDR3 or DDR2 DRAMs as shown in Voltage Mappings A and B-C, respectively, below:

Ground 4: Spiers in view of Amidi, with DDR2 or DDR3 DRAMs

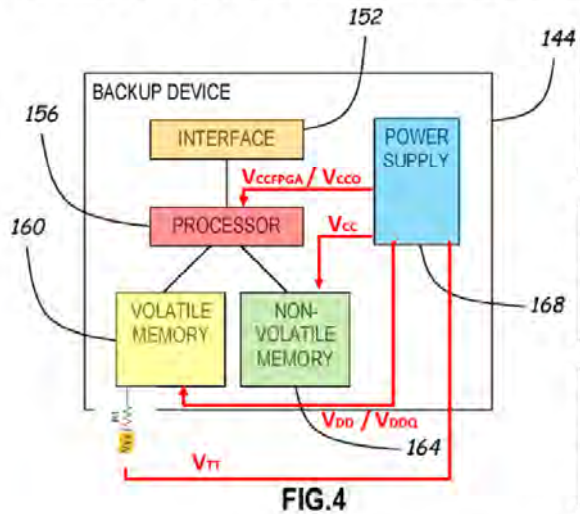


FIG.4

Voltage Mapping (A) for DDR3
1st : VDD/VDDQ to DRAM = 1.5V
2nd : VCCFPGA to FPGA Core = 1.8V
3rd : VTT to Terminate DRAM Bus = 0.75V
4th : VCC to NV Memory / VCCO to FPGA I/O = 3.3V

Voltage Mapping (B) for DDR2
1st : VDD/VDDQ to DRAM = 1.8V
2nd : VCCFPGA to FPGA Core = 1.8V
3rd : VTT to Terminate DRAM Bus = 0.9V
4th : VCC to NV Memory / VCCO to FPGA I/O = 3.3V

Voltage Mapping (C) for DDR2
1st : VDD/VDDQ to DRAM = 1.8V
2nd : VCCFPGA to FPGA Core = 1.8V
3rd : VCC to NV Memory = 3.3V
4th : VCCO to FPGA I/O = 3.3V

Discussing JEDEC Specifications

See supra pp.78-81; EX1003, ¶¶655-700.

Petition (918) at 3, 86.

Petition Incorporates JEDEC Specifications Into Grounds 4/5

660. As previously explained, a Skilled Artisan would understand that JESD79-3A specifies a VDD/VDDQ power supply voltage of 1.5 volts for DDR3 DRAMs (i.e., the "*first regulated voltage*" for Mapping A of Grounds 4 and 5). Ex. 1046 at p.10. Similarly, she would understand that JESD79-2B specifies a VDD/VDDQ of 1.8 volts for DDR2 DRAMs (i.e., the "*first regulated voltage*" for Mappings B and C of Grounds 4 and 5). Ex. 1026 at p.7.

EX1003 (918) (Wolfe Declaration), ¶660.

Petition (918) at 87.

Spiers' Discloses SDRAM On A PCI Card

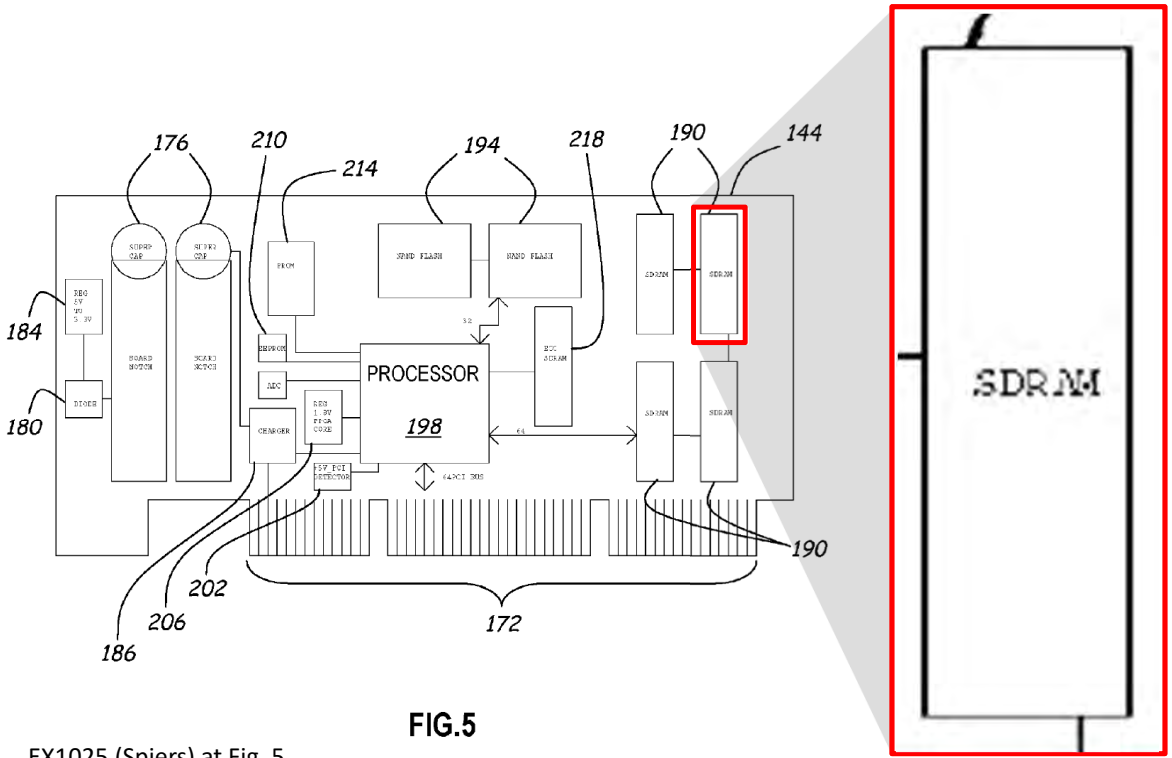


FIG.5

EX1025 (Spiers) at Fig. 5.

- **Discloses only 3.3V and 1.8V (processor)**
- **3.3V for SDR SDRAM and NAND**

Patent Owner Response (918) at 49, 54.
Patent Owner Response (054) at 52-53, 57-58.

Spiers' Discloses Only 3.3V and 1.8V

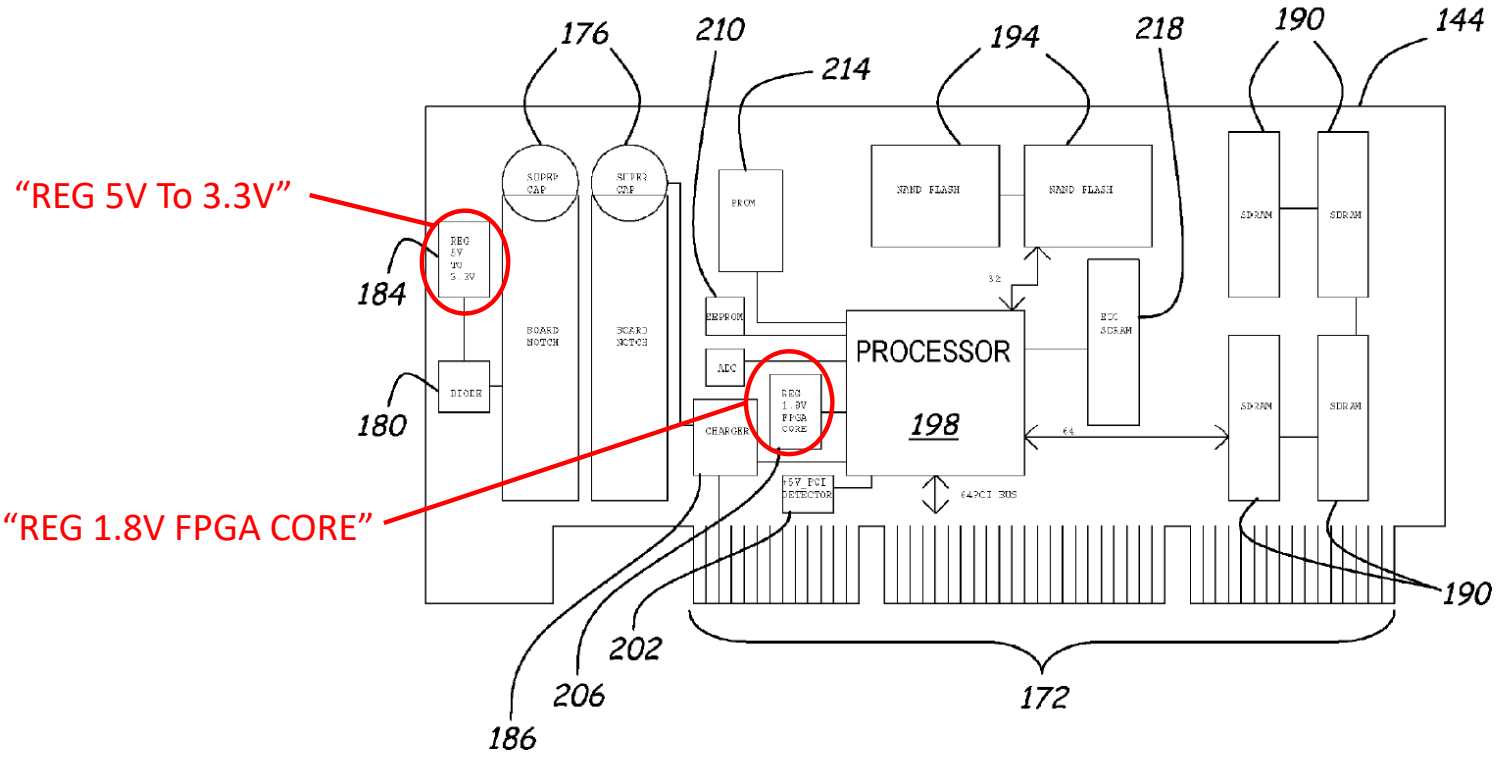


FIG.5

EX1025 (Spiers) at Fig. 5.

Patent Owner Response (918) at 49, 54.
Patent Owner Response (054) at 52-53, 57-58.

Spiers' Figure 4 Embodiment Does Not Use Regulators (And Is Not Relied On)

Patent Owner's argument assumes that Spiers is limited to a PCI interface, but a PCI backup device is described as one embodiment in Spiers. Ex. 1025 ¶ 19. Spiers also discloses an "interface 152" in more general terms, which does not appear limited to a PCI interface. *Id.* ¶ 36. Patent

Institution Decision (918) at 44.
Institution Decision (054) at 47.

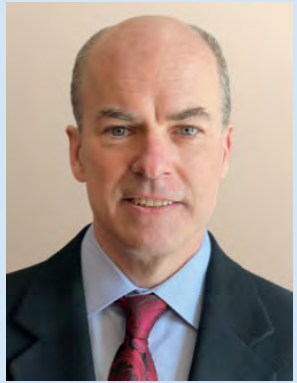
Petitioner does not rely on the FIG. 4 embodiment for any independent claims

Patent Owner Response (918) at 48.
Patent Owner Response (054) at 52.

[0036] Referring now to **FIG. 4**, a block diagram illustration of a backup device **144** of an embodiment is now described. In this embodiment, the backup device comprises an interface **152**, a backup device processor **156**, a volatile memory **160**, a non-volatile memory **164**, and a power supply **168**. The interface **152** may be any type of interface and is utilized to communicate with the storage controller **132**. The interface **152** is connected to the processor **156**, which controls operations within the backup device **144**. Connected to the processor **156** are the volatile memory **160** and the non-volatile memory **164**. The volatile memory **160**, in one embodiment, is SDRAM utilized to store data from the storage controller **132** during typical write operations. The non-volatile memory **164**, in one embodiment, is flash memory, and is utilized in the event of a power failure detection. As is understood, flash memory is a type of nonvolatile memory that may be erased and reprogrammed in units of memory referred to as blocks or pages. The processor **156**, in this embodiment, upon detecting a power failure, switches the backup device **144** to the power supply **168**, and moves the data in the volatile memory **160** to the non-volatile memory **164**. After the data from the volatile memory **160** is stored in the non-volatile memory **164**, the processor **156** shuts down the backup device **144**. The power supply **168**, in one embodiment, includes one or more capacitors that are charged when the backup device **144** is powered up. In the event of a power interruption, the backup device **144** receives power from the capacitor(s) when moving the data. After the data is securely stored in the non-volatile memory **164**, the power is switched off from the capacitor(s). In another embodiment, the power supply **168** includes one or more batteries. As will be understood, any type of power supply **168** may be utilized, so long as power may be supplied to the backup device **144** for a sufficient time period to move the data to the non-volatile memory **164**.

EX1025 (Spiers) at [0036].

Spiers' PCI interface Is The Data Transfer Bottleneck – No Reason To Use Faster DDR2/DDR3 In Place of Spiers' SDRAM



William Mangione-Smith
Netlist's Expert

NETLIST

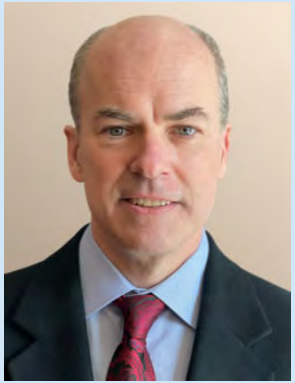
> 145. As such, during a power failure (or during data restore), the rate at which data is transferred from the SDRAM to the NAND is not limited by the SDRAMs. Therefore, for both data transfer between the host and SDRAM via the PCI interface during normal operation, as well as data transfer between SDRAM and NVRAM during power interruption, the bottleneck in data transfer is not SDRAMs.

EX2031 (918) (Mangione-Smith Declaration), ¶145.

The Reply does not dispute Dr. Mangione-Smith's detailed calculations (EX1003, ¶¶141-145) showing that Spiers' PCI interface was the bottleneck for data transfer

Patent Owner Response (918) at 56.

Dr. Mangione-Smith's Detailed Unrebutted Calculations Showing Spiers' PCI Interface Is The Bottleneck For Data Transfer



William Mangione-Smith
Netlist's Expert

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142. Given that the clock speed of PCI is up to 66 MHz, a 66MHz PCI card having a 64-bit wide bus[7] has a peak data transfer rate of 528 MB/s, because there are 8 bits per byte, so 64 bits equals 64/8 = 8 bytes. So, if we transmit 8 bytes at the rate of 66 MHz, this translates to a peak data transfer rate of 66M transfers/s × 8 byte/transfer = 528 MB/s. See EX2016 [2006 EURESYS Tech Notes] at 4 (66MHz, 64 bit PCI card, the maximum for a PCI card, has a peak data rate of 528 MB/s and a practical data rate of 360 MB/s). Some references put the peak transfer rate at a slightly higher value of 532 MB/s. EX2029 at 6. This is because 66MHz is not a precise number; and the actual clock speed is slightly higher.

EX2031 (918) (Mangione-Smith Declaration), ¶142.

Patent Owner Response (918) at 55.

Continue Dr. Mangione-Smith's Detailed Unrebutted Detailed Calculations Showing Spiers' PCI Interface Is The Bottleneck For Data Transfer

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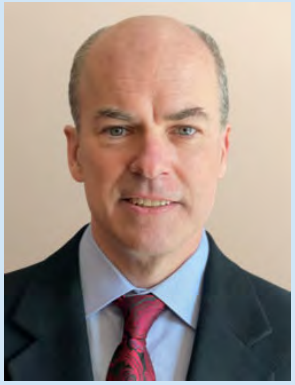
143. Compared to PCI bus peak transfer rate of 528 MB/s, at the time of the invention, SDRAMs were operating in the range of 66-166 MHz. See EX2012 [NXP 2007 Note] (describing 66-133 MHz SDRAMs); EX2014 [Qimonda PC166 datasheets] at 3 (166MHz SDRAMs); EX2017 [Qimonda] at 3 (same). These clock rates correspond to maximum transfer rates of 533-1328 MB/s. This is obtained by multiplying the SDRAM operating speed (i.e. 66.66^{8}- 166 MHz) by 8, since 8 bytes are transmitted in each transfer. See EX2012 [BeyondBits2article17.pdf (nxp.com)], Table 1) (maximum transfer rates for PC66, PC100 and PC133 SDRAMs are 533 MB/s, 800 MB/s and 1066 MB/s respectively, or 8 times the clock rates); EX2018 [Transcend FAQ296] (100-166MHz SDRAM provides data transfer rate of 0.8-1.3 GB/s or 800-1300 MB/s). As such, Spiers' SDR SDRAM's data rate would exceed that of Spiers' PCI interface. That is, when data is transferred between a host and SDRAM via PCI, the bottleneck is at the PCI interface and not at the SDR SDRAMs.

Patent Owner Response (918) at 55.
Patent Owner Response (054) at 59.

EX2031 (918) (Mangione-Smith Declaration), ¶143.
EX2061 (054) (Mangione-Smith Declaration), ¶140.

Dr. Mangione-Smith's Detailed Unrebutted Detailed Calculations Showing NAND Is The Bottleneck For Data Transfer



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144. I also note that SDRAM's data rate also far exceeds that of NAND flash. For example, according to Petitioner's submitted evidence, NAND flash can program "[t]he content of each 2,112-byte page … in 300µs." EX1049, p. 7. This translates to a data rate of about 7 MB/s, i.e., 2,112 byte ÷ 300µs = 7MB/s).

145. As such, during a power failure (or during data restore), the rate at which data is transferred from the SDRAM to the NAND is not limited by the SDRAMs. Therefore, for both data transfer between the host and SDRAM via the PCI interface during normal operation, as well as data transfer between SDRAM and NVRAM during power interruption, the bottleneck in data transfer is not SDRAMs.

EX2031 (918) (Mangione-Smith Declaration), ¶144-145.
EX2061 (054) (Mangione-Smith Declaration), ¶141-142.

Patent Owner Response (918) at 55-56.
Patent Owner Response (918) at 58-59.

No Evidence that the Application Suitable for Usage of DDR

NXP

Joaquin Romo

DDR Memories

Comparison and overview

We realize that one of the most important aspects of a computer is its capability to store large amounts of information in what we normally call "memory." Specifically, it's random access memory (RAM), and it holds volatile information that can be accessed quickly and directly. And considering the ever growing system need for speed and efficiency, understanding double-data-rate (DDR) memory is important to system developers.

With improvements in processor speeds, RAM memory has evolved into high performance RAM chipsets called DDR synchronous dynamic RAM (SDRAM). It doubles the processing rate by making a data fetch on both the rising and falling edge of a clock cycle. This is in contrast to the older single-data-rate (SDR) SDRAM that makes a data fetch on only one edge of the clock cycle.

In addition to well-known computer applications, DDR memories are widely used in other high-speed, memory-demanding applications, such as graphic cards, which need to process a large amount of information in a very short time to achieve the best graphics processing efficiency. Blade servers using many blades, or single purpose boards, powered by a single, more efficient power supply also need fast memory access. This allows the blades to quickly transmit reliable information among each other and create greater opportunities to reduce power consumption. Memory devices are also required in networking and communications applications with tasks ranging from simple address lookups to traffic shaping/policing and buffer management.

This article describes the main characteristics of DDR memories as well as the specifications of power supplies required for these types.

DDR Memory Characteristics

DDR memory's primary advantage is the ability to fetch data on both the rising and falling edge of a clock cycle, doubling the data rate for a given clock frequency. For example, in a DDR200 device the data transfer frequency is 200 MHz, but the bus speed is 100 MHz.

DDR1, DDR2 and DDR3 memories are powered up with 2.5, 1.8 and 1.5V supply voltages respectively, thus producing less heat and providing more efficiency in power management than normal SDRAM chipsets, which use 3.3V.

Temporization is another characteristic of DDR memories. Memory temporization is given through a series of numbers, such as 2-3-2-6-T1, 3-4-4-8 or 2-2-2-5 for DDR1. These numbers indicate the number of clock pulses that it takes the memory to perform a certain operation—the smaller the number, the faster the memory.

The operations that these numbers represent are the following: CL- tRCD - tRP – tRAS - CMD. To understand them, you have to keep in mind that the memory is internally organized as a matrix, where the data is stored at the intersection of the rows and columns.

- CL: Column address strobe (CAS) latency is the time it takes between the processor asking memory for data and memory returning it.
- tRCD: Row address strobe (RAS) to CAS delay is the time it takes between the activation of the row (RAS) and the column (CAS) where data is stored in the matrix.
- tRP: RAS precharge is the time between disabling the access to a row of data and the beginning of the access to another row of data.
- tRAS: Active to precharge delay is how long the memory has to wait until the next access to memory can be initiated.
- CMD: Command rate is the time between the memory chip activation and when the first command may be sent to the memory. Sometimes this value is not informed. It usually is T1 (1 clock speed) or T2 (2 clock speeds).

Table 1 is a comparison of clock and transfer rates for the RAM memory chipsets that can be found in today's computers, including SDR, DDR, DDR2 and future DDR3 modules.

Netlist Ex 2012
Samsung v Netlist
IPR2022-00996

70 freescale.com/beyondbits

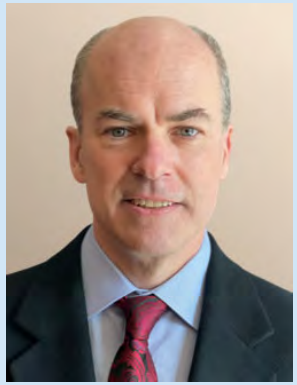
Typical Applications of DDRx Memories

Market analyses indicate that DDR is currently utilized in over 50 percent of all electronic systems, and usage is expected to increase to 80 percent over the next several years. DDR is not, and will never be, an "all things to all designs" technology. DDR memory is well suited for those designs that have a high read to write ratio. Quad-data-rate memory, for example, is designed for applications that require a 50 percent read/write ratio.

EX2012, p. 73

Patent Owner Response (918) at 57-58.
Patent Owner Response (054) at 61.

Spiers' Application Has High Write-to-Read Ratio



William Mangione-Smith
Netlist's Expert

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147. DDR2/DDR3 is not an "all things to all designs technology," but was specifically designed for high ***read-to-write*** ratio applications. See EX2012 [BeyondBits2article17.pdf (nxp.com)] at 73 ("DDR memory is well suited for those designs that have a high read to write ratio.") In contrast, Spiers' application has high write-to-read ratio, or a ***low read-to-write ratio***. First, writes to SDRAM in

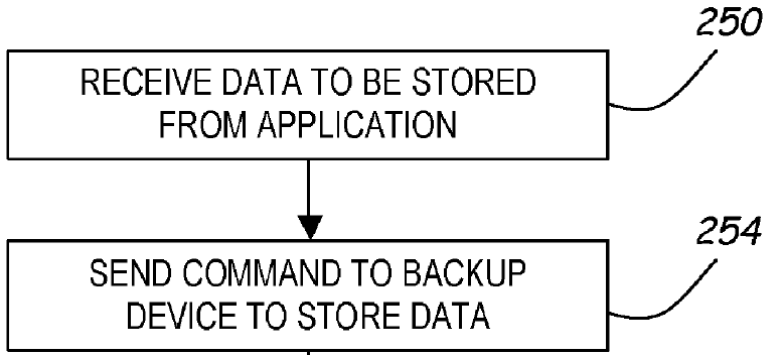
EX2031 (918) (Mangione-Smith Declaration), ¶147.
EX2061 (054) (Mangione-Smith Declaration), ¶144.

- Dr. Mangione-Smith explained that Spiers' SDRAM is only read in case of a restore or a power interruption (which is rare), but writes occur with every system write (which is frequent). Id., ¶147 (918), ¶144 (054)

Patent Owner Response (918) at 58-59.
Patent Owner Response (054) at 61-62.

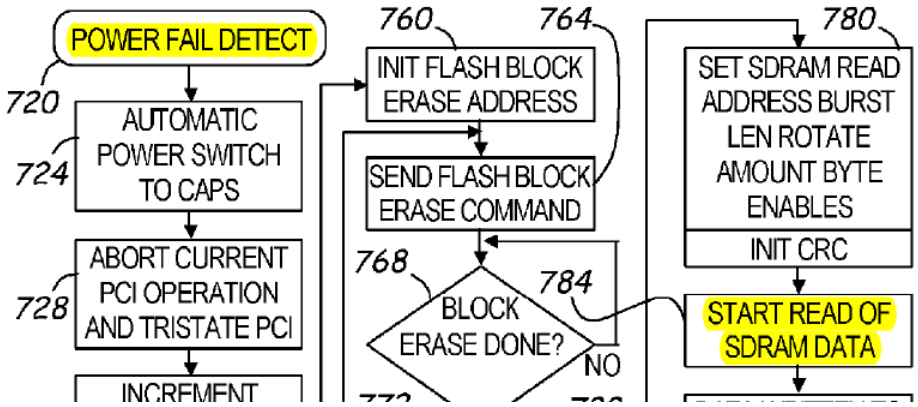
Spiers' Application Has A High Write-to-Read Ratio

Spiers' sends all received data to be stored (written) to the backup device



[0040] Referring now to the flow chart diagram of **FIG. 6**, the operational steps performed by a NAS device of an embodiment of the present invention are now described. In this embodiment, the NAS device receives data to be stored from an application, as noted at block **250**. At block **254**, the NAS device sends a command to the backup device to store the data. The NAS device, at block **258**, determines if the

Spiers' reads SDRAM data only to restore (e.g, following power failure)



[0054] Referring now to **FIG. 14**, the operational steps performed by the backup device upon detection of a power failure are now described. As discussed previously, the

Patent Owner Sur-Reply (918) at 28.
Patent Owner Sur-Reply (054) at 28-29.

Petitioner's New PCI-X Reply Argument

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- The Petition's analysis and Spiers' disclosure are specific to PCI, and neither mentions PCI-X.
- Requires a new modification of Spiers, which is impermissible
- Even with an improper new modification of Spiers to use PCI-X, there is no evidence showing all limitations are met with PCI-X.
  - Dr. Wolfe provides details only about how a PCI bus satisfies various limitations. EX1003, ¶¶604-608

Patent Owner Sur-Reply (918) at 28.

Petitioner Only Suggests Incorporating Regulators On The PCI Card, Not On The DDR2/DDR3 Memory Modules

Regulators providing alleged regulated voltages are not on Spiers' "volatile memory" or "non-volatile memory" modules

Ground 4: Spiers in view of Amidi, with DDR2 or DDR3 DRAMs

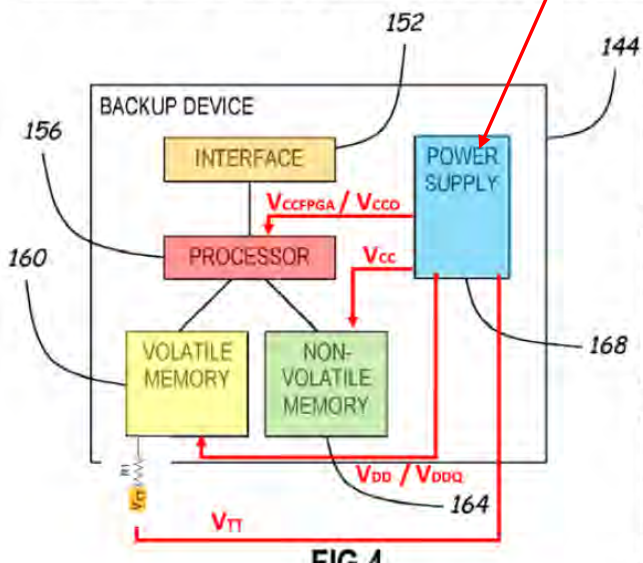


FIG.4

Voltage Mapping (A) for DDR3
1st : VDD/VDDQ to DRAM = 1.5V
2nd : VCCFPGA to FPGA Core = 1.8V
3rd : VTT to Terminate DRAM Bus = 0.75V
4th : VCC to NV Memory / VCCO to FPGA I/O = 3.3V

Voltage Mapping (B) for DDR2
1st : VDD/VDDQ to DRAM = 1.8V
2nd : VCCFPGA to FPGA Core = 1.8V
3rd : VTT to Terminate DRAM Bus = 0.9V
4th : VCC to NV Memory / VCCO to FPGA I/O = 3.3V

Voltage Mapping (C) for DDR2
1st : VDD/VDDQ to DRAM = 1.8V
2nd : VCCFPGA to FPGA Core = 1.8V
3rd : VCC to NV Memory = 3.3V
4th : VCCO to FPGA I/O = 3.3V

'918 Patent, Claim 1

1. A memory module comprising:
a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;
a first buck converter configured to provide a first regulated voltage having a first voltage amplitude;
a second buck converter configured to provide a second regulated voltage having a second voltage amplitude;
a third buck converter configured to provide a third regulated voltage having a third voltage amplitude;
a converter circuit configured to provide a fourth regulated voltage having a fourth voltage amplitude; and

Petition (918) at 101.

No Reason for Buck Converter for VTT

Petition at 90

"[I]t would have been obvious to a POSITA to use "buck converter[s]" to provide each of these regulated voltages from the +5V power supply in order to achieve high efficiency, reliability, and flexible power conversion, as discussed previously."

- **Cited EX1046, p.109 and EX1026, p.7 "relate to when there is AC output measurement and/or device-under-test condition"**
  - VTT can also be generated via passive termination (no regulator used) (FBDIMM used VTT for power saving)
- **Cited FBDIMM not suitable for PCI (Spiers' 4 memory modules would require more than 35W if FBDIMM, while PCI card can only provide up to 25W)(**EX1031, p. 137; EX2047, p. 20; EX2031, ¶150)
- **Commercially available dual buck for DDR1, not DDR2/DDR3 VDD & VTT**
  - EX1047: DDR1 VTT termination, but DDR2/DDR3 uses on-die-termination, not motherboard termination as in DDR1

Patent Owner Response (918) at 60-62
Patent Owner Sur-Reply (918) at 29-30.

Alleged Reasons for Multiple Converters for 1.8V Inapplicable to Spiers

No evidence of analog voltages

FBDIMM does not run at hundreds of amperes

> Many devices share standard voltage levels (such as 3.3 V), while others may require device-specific voltages. In addition, a particular standard voltage level may have to be independently furnished in numerous places. For example, separate analog- and digital supplies, such as 3.3 V_{ANALOG} and 3.3 $V_{DIGITAL}$, may be required. Generating the same voltage numerous times may be necessary to improve efficiency (e.g., memory rails running at hundreds of amperes) or to meet sequencing requirements (3.3 V_A and 3.3 V_B needed by separate devices at different times). All of

EX1062 (Power-Supply Management—Principles, Problems, and Parts) at 13.

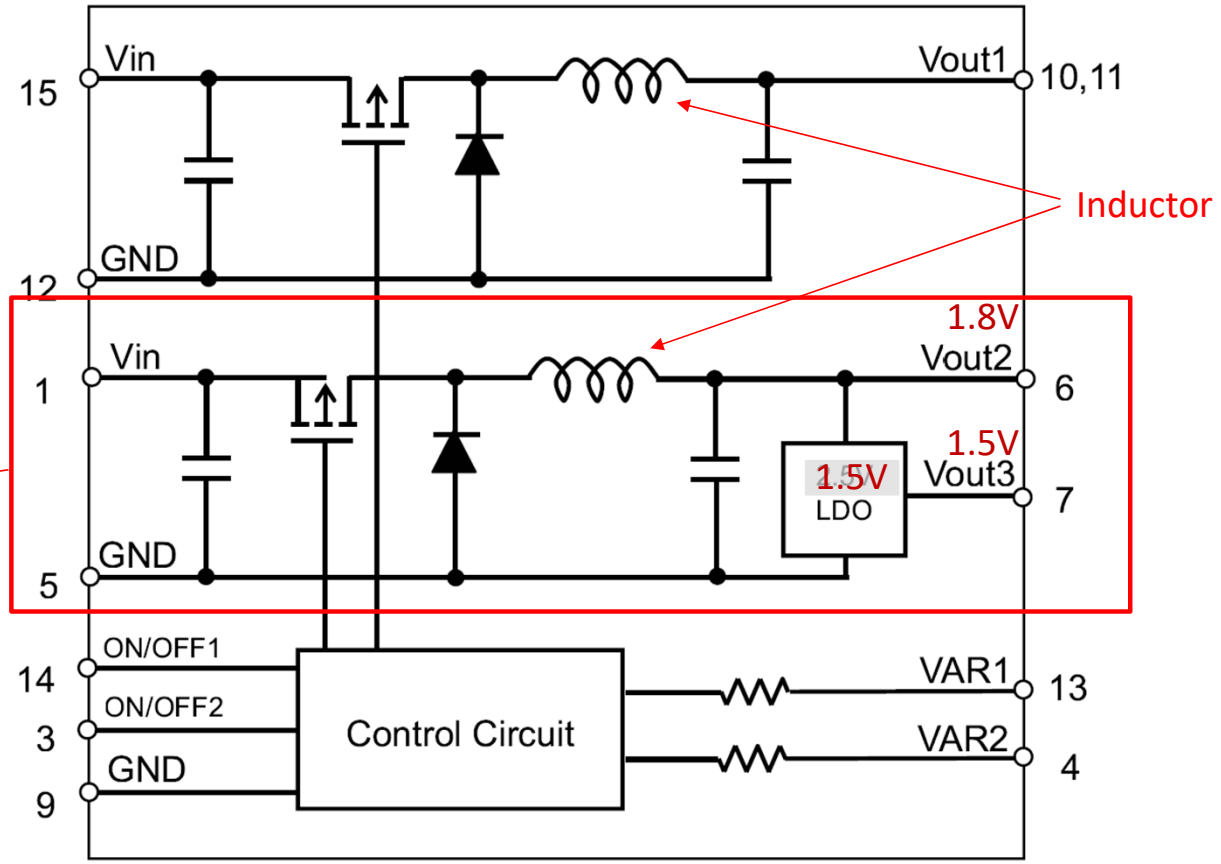
VDD, VDDL, and VDDQ are each supplied to the same devices

Patent Owner Response (918) at 27.
Patent Owner Response (054) at 30.

No Need for Multiple Buck Converters for 1.8V and 1.5V

A buck converter needs "an LC-filter just after the power switch …." EX2020, p.22. Thus, the number of inductors reflects the number of buck converters.

See EX1078, 12 (LC filter); EX1075, 129:13-19.



EX1048, 2 (shows two buck converters, each with its own inductor).

Patent Owner Sur-Reply (918) at 14.
Patent Owner Sur-Reply (054) at 15.

Evidence Shows Using LDO for 5V-1.8V and 5V-3.3 Conversion

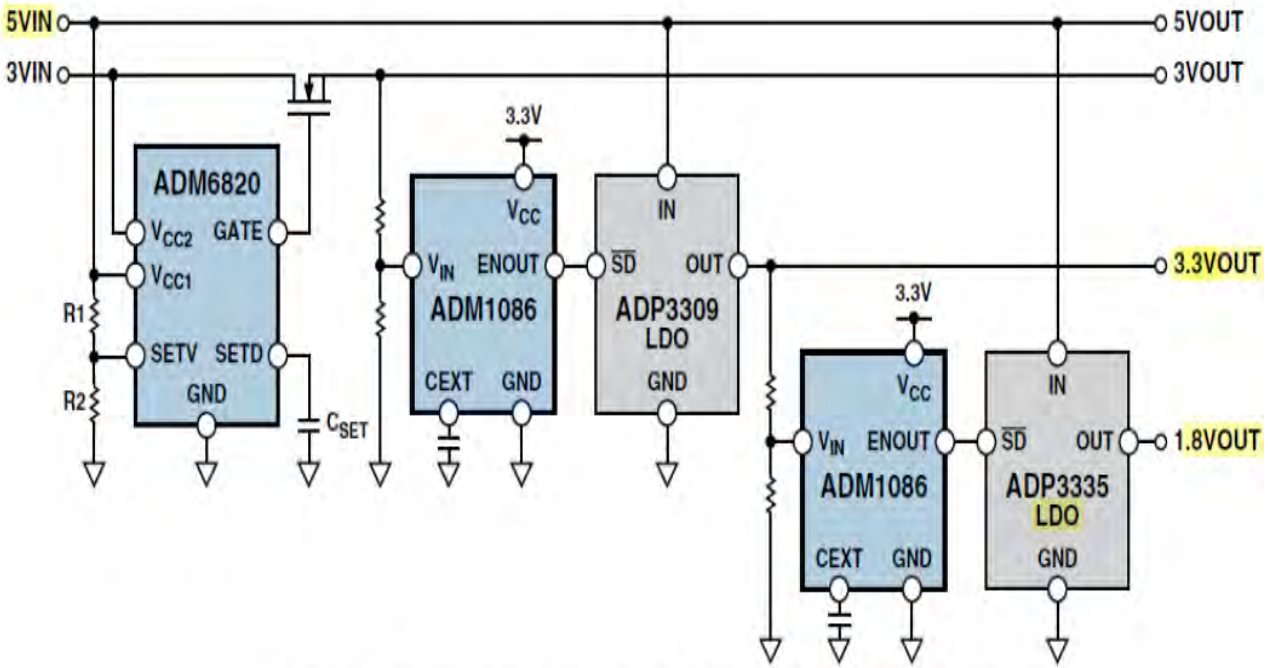


Figure 3. Sequencing a four-supply system with monitoring ICs.

EX1062 at 14.

The Petition

	Voltage Mappings (Grounds 4-5)		
	A	B	C
"first":	V_{DD}/V_{DDQ}=1.5V	V_{DD}/V_{DDQ}=1.8V	V_{DD}/V_{DDQ}=1.8V
"second":	V_{CCFPGA}=1.8V	V_{CCFPGA}=1.8V	V_{CCFPGA}=1.8V
"third":	V_{TT}=0.75V	V_{TT}=0.9V	V_{CC}=3.3V
"fourth":	V_{CC} or V_{CCO} = 3.3V	V_{CC} or V_{CCO} = 3.3V	V_{CCO}=3.3V

"it would have been obvious to a POSITA to use "buck converter[s]" to provide each of these regulated voltages from the +5V power supply in order to achieve high efficiency, reliability, and flexible power conversion …."

Petition (918) at 87, 90.

Patent Owner Response (918) at 64.
Patent Owner Response (054) at 67.

Buck Converter Unsuitable for 5V-3.3V Backup Regulator

Unrebutted:

- Voltage oscillation in low load condition (EX2021, 5; EX2031, ¶¶157-159)
- Start-up time too long to maintain the content in the DRAM cells
  - Dr. Wolfe admits that "the start time of a buck converter … may be thousands of microseconds." EX1003, ¶818; EX1041, 10 (buck converter initialization and soft start measured "in seconds"); EX2022
  - SDRAM's standard refresh rate, however, is 15.6µs. EX2025, 1; EX2031, ¶176

Petitioner's own evidence also shows buck converters are unsuitable:

- EX1048 has an "Input Voltage Range" of "4.5 to 13.2V."
- During backup, super-cap's voltage may drop below 4.5V, at which point buck converter would stop operating. EX2031, ¶164 (voltage drops during super-cap discharge)
- LDO would operate for entire 3.3V-5V range (EX2031, ¶159)(LDO operation not impacted by low voltage)

Patent Owner Response (918) at 67-69.
Patent Owner Sur-Reply (918) at 31-32.

TOPICS

GROUNDS 1-3

Harris Does Not Receive Power Via Edge Connections

Harris Does Not Receive The Recited Signals From the Host

A POSITA Would Not Have Used the Required # of (Buck) Converters

Ground 2 ASSUMES Separate Converters To Supply Each FBDIMM-Required Voltage

A POSITA Would Not Have Replaced Harris' Redundant Power

Additional Reasons Why Dependent Claims Are Not Obvious

GROUNDS 4-5

The Recited "Memory Module" Means A Main Memory Module

Spiers' PCI Card Is Not a Memory Module

POSITA Would Not Use DDR2/DDR3 or Recited # of (Buck) Converters

Additional Reasons Why Dependent Claims Are Not Obvious

Dependent Claim 13 – Dr. Wolfe Relies On The +5V PCI Supply Voltage During Normal Operation

13. The memory module of claim **5**, wherein the power input voltage is coupled to the first, second, and third buck converters and the converter circuit.

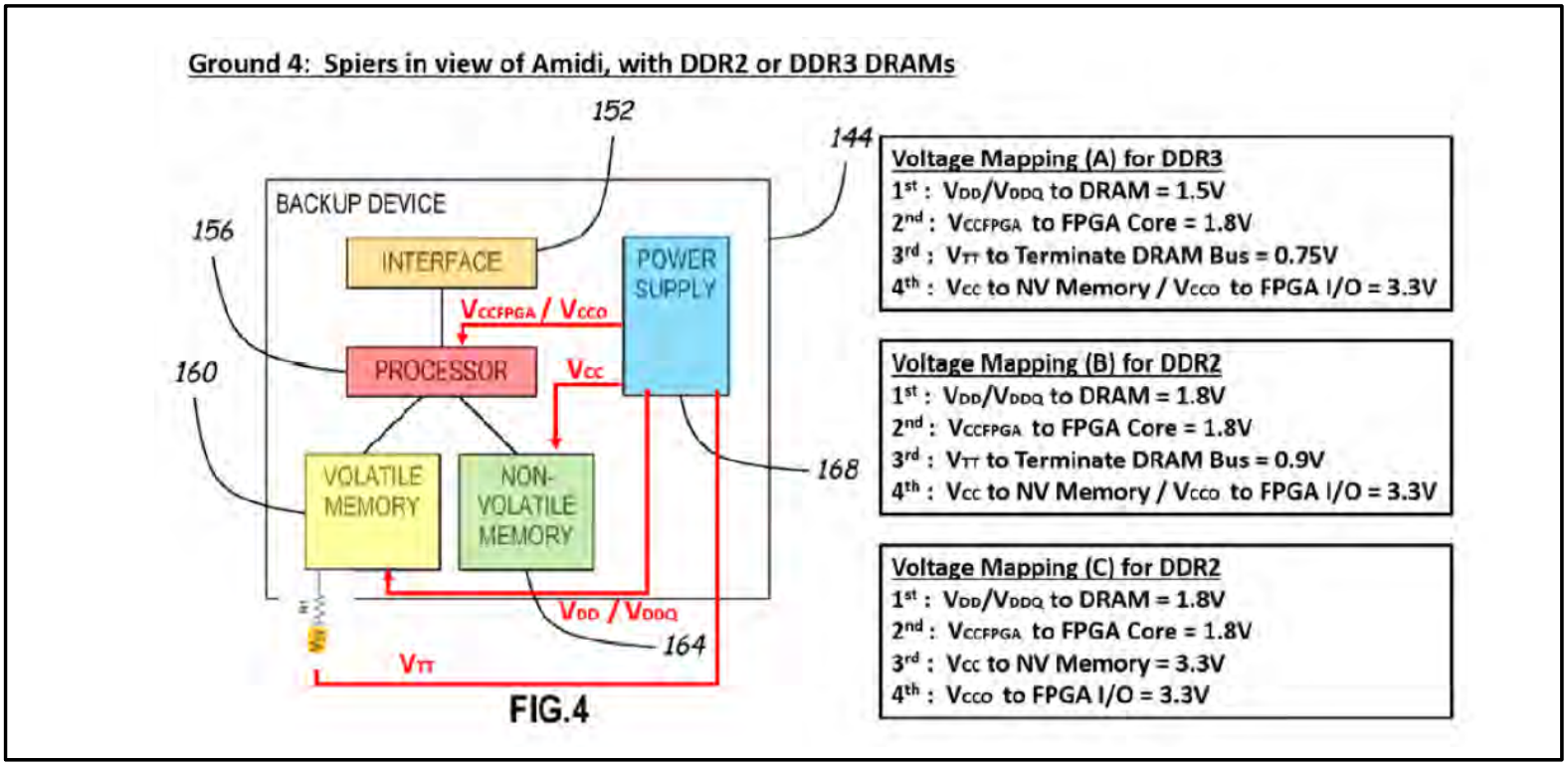
863. For the reasons discussed above with reference to claim limitations [1.c] ("*a first buck converter . . .*"), [1.d] ("*a second buck converter . . .*"), [1.e] ("*a third buck converter . . .*"), [1.f] ("*a converter circuit . . .*") and claim 5, Spiers in view of Amidi teaches and discloses to a Skilled Artisan that the +5V power input voltage is coupled to the "*first*," "*second*," and "*third buck converter[s]*" and the "*converter circuit*" when the voltage amplitude of the input voltage is in a normal operating range. *Supra* ¶¶655-666 (claim limitation [1.c]), ¶¶668-676 (claim limitation [1.d]), ¶¶677-687 (claim limitation [1.e]), ¶¶689-700 (claim limitation [1.f]), ¶¶764-780 (claim 5).

EX1003 (918) (Wolfe Declaration), ¶863.

Patent Owner Response (918) at 72-73.

Dr. Wolfe's Analysis of Claim 13 Is Inconsistent With His Voltage Mappings

Dr. Wolfe's reliance on Spiers' +5V PCI supply voltage for the "power input voltage" of claim 13 is inconsistent with the voltage mappings below, where the power supply Element 168 is used during **power failure**. EX1003, ¶¶ 657-659; EX1025, [0036].



Patent Owner Response (918) at 72-73.

Dependent Claims 5-7, 8-14, 16-22, 24-27, 30 Are *Not* Obvious

- Same reason as for Ground 1-3
- Input over-voltage not an anomaly that would have caused DRAM data loss
  - Upper limit for converters' input voltage is much higher than the expected tolerance range
- Hajeck's charge pump continues to operate when over-voltage occurs

Patent Owner Response (918) at 33-34.
Patent Owner Response (054) at 35-36.