

Step-Down DC-to-DC Controller

ADP1821

FEATURES

Wide power-input voltage range: 1 V to 24 V
Chip supply voltage range: 3.7 V to 5.5 V
Wide output voltage range: 0.6 V to 85% of input voltage
1% accuracy, 0.6 V reference voltage
All N-channel MOSFET design for low cost
Fixed-frequency operation 300 kHz, 600 kHz, or
synchronized operation up to 1.2 MHz
No current sense resistor required
Power-good output
Programmable soft start with reverse current protection
Soft start, thermal overload, current-limit protection
Undervoltage lockout
10 µA shutdown supply current
Small, 16-lead QSOP

APPLICATIONS

Telecommunications and networking systems
Set-top boxes
Printers
Servers
Medical imaging systems
Microprocessor and DSP core power supplies
Mobile communication base stations

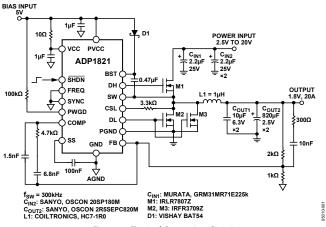


Figure 1. Typical Operating Circuit

GENERAL DESCRIPTION

The ADP1821 is a versatile and inexpensive, synchronous, pulse-width-modulated (PWM), voltage-mode, step-down controller. It drives an all N-channel power stage to regulate an output voltage as low as 0.6 V. The ADP1821 can be configured to provide output voltages from 0.6 V to 85% of the input voltage and is sized to handle large MOSFETs for point-of-load regulators.

The ADP1821 is well suited for a wide range of high power applications, such as DSP and processor core power in telecommunications, medical imaging, high performance servers, and industrial applications. It operates from a 3.7 V to 5.5 V supply with a power input voltage ranging from 1.0 V to 24 V.

The ADP1821 operates at a pin-selectable, fixed switching frequency of either 300 kHz or 600 kHz, minimizing external component size and cost. For noise sensitive applications, it can be synchronized to an external clock to achieve switching frequencies between 300 kHz and 1.2 MHz. The ADP1821 includes soft start protection to limit the inrush current from the input supply during startup, reverse current protection during soft start for precharged outputs, as well as a unique adjustable lossless current-limit scheme utilizing external MOSFET sensing.

The ADP1821 operates over the -40°C to +125°C junction temperature range and is available in a 16-lead QSOP.

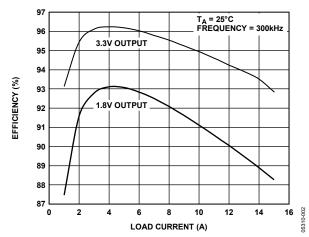


Figure 2. Efficiency vs. Load Current, 5 V Input

Rev. C
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ADP1821

IABLE UF GUNIENIS Features 1	Compensation	1.
Applications 1	•	
	Power-Good Indicator	
General Description	Thermal Shutdown	
Revision History	Shutdown Control	
Specifications	Application Information	12
Absolute Maximum Ratings 5	Selecting the Input Capacitor	12
ESD Caution	Output LC Filter	12
Simplified Block Diagram5	Selecting the MOSFETs	13
Pin Configuration and Function Descriptions6	Setting the Current Limit	14
Typical Performance Characteristics	Feedback Voltage Divider	14
Theory of Operation9	Compensating the Voltage Mode Buck Regulator	14
Soft Start9	Setting the Soft Start Period	18
Error Amplifier9	PCB Layout Guideline	19
Current-Limit Scheme	Recommended Component Manufacturers	20
MOSFET Drivers	Application Circuits	
Input Voltage Range10	Outline Dimensions	
Setting the Output Voltage	Ordering Guide	
Switching Frequency Control and Synchronization10		
REVISION HISTORY		
4/07—Rev. B to Rev. C	Changes to Theory of Operation Section	
Changes to Specifications Section	Changes to Application Information Section	
Changes to Absolute Maximum Ratings Section5	Added PCB Layout Section	
Changes to Current-Limit Scheme Section10	Changes to Application Circuits Section	
Changes to Setting the Current Limit Section14	Added Summary of Equations Section	2.
Added Figure 1514		
Changes to Compensating the Voltage Mode Buck	1/06—Rev. 0 to Rev. A	
Regulator Section15	Changes to Specifications Table	
Changes to Type II Compensator Section	Changes to Theory of Operation Section	
Changes to Type III Compensator Section18	Changes to Input Voltage Range Section	1
Changes to Application Circuits Section21	Added Equation 1	12
Changes to Figure 2221	Changes to Equation 7 and Equation 8	13
Changes to Ordering Guide	Added Equation 9	13
12/06—Rev. A to Rev. B	Changes to Equation 16	
Updated FormatUniversal	Changes to Figure 15	
Changes to Features Section	Changes to Equation 21	
Changes to Applications Section	Changes to Figure 16	
Changes to Applications Section	Changes to Equation 28	
Changes to General Description Section	Updated Outline Dimensions	18
Changes to DWM Controller	7/05—Revision 0: Initial Version	



SPECIFICATIONS

 $V_{VCC} = V_{PVCC} = V_{\overline{SHDN}} = V_{FREQ} = 5 \text{ V}$, SYNC = GND. All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC). $T_J = -40$ °C to +125°C, unless otherwise specified. Typical values are at $T_A=25$ °C.

Table 1.

Parameter	Conditions	Min	Тур	Max	Unit
POWER SUPPLY					
Input Voltage		3.7		5.5	V
Undervoltage Lockout Threshold	V_{VCC} rising, $T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	2.4	2.7	3.0	V
Undervoltage Lockout Threshold	V_{VCC} rising, $T_A = 25^{\circ}C$	2.5	2.7	2.9	V
Undervoltage Lockout Hysteresis	Vvcc		0.1		V
Quiescent Current	I _{vcc} + I _{vcc} , not switching		1	2	mA
Shutdown Current	SHDN = GND			10	μΑ
Power Stage Supply Voltage		1.0		24	V
ERROR AMPLIFIER					
FB Regulation Voltage	$T_{J} = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	594	600	606	mV
FB Regulation Voltage	$T_{J} = -40^{\circ}\text{C to } +125^{\circ}\text{C}$	588	600	606	mV
FB Input Bias Current		-100	+1	+100	nA
Error Amplifier Open-Loop Voltage Gain			70		dB
COMP Output Sink Current			600		μΑ
COMP Output Source Current			110		μΑ
COMP Clamp High Voltage			2.4		V
COMP Clamp Low Voltage			0.75		V
PWM CONTROLLER					
PWM Peak Ramp Voltage			1.25		V
DL Minimum On Time	FREQ = VCC (300 kHz)	120	170	220	ns
DL Minimum On-Time	FREQ = VCC (300 kHz), T _A = 25°C	140	170	200	ns
DH Maximum Duty Cycle	FREQ = GND (300 kHz)	85	90		%
DH Minimum Duty Cycle	FREQ = GND (300 kHz)		1	3	%
SOFT START					
SS Pull-Up Resistance	SS = GND		95		kΩ
SS Pull-Down Resistance	$V_{SS} = 0.6 V$	1.65	2.5	4.2	kΩ
OSCILLATOR					
Oscillator Frequency	FREQ = GND	250	310	375	kHz
	FREQ = VCC	470	570	720	kHz
Synchronization Range	FREQ = GND	300		600	kHz
	FREQ = VCC	600		1200	kHz
SYNC Minimum Pulse Width				80	ns
CURRENT SENSE					
CSL Threshold Voltage	Relative to PGND	-30	0	+30	mV
CSL Output Current	$V_{CSL} = 0 V$	42	50	54	μΑ
Current Sense Blanking Period			160		ns
GATE DRIVERS					
DH Rise Time	$C_{GATE} = 3 \text{ nF, } V_{DH} = V_{IN}, V_{BST} - V_{SW} = 5 \text{ V}$		16		ns
DH Fall Time	$C_{GATE} = 3 \text{ nF, } V_{DH} = V_{IN}, V_{BST} - V_{SW} = 5 \text{ V}$		12		ns
DL Rise Time	$C_{GATE} = 3 \text{ nF, } V_{DL} = V_{IN}$		19		ns
DL Fall Time	$C_{GATE} = 3 \text{ nF, } V_{DL} = 0 \text{ V}$		13		ns
DL Low to DH High Dead Time			33		ns
DH Low to DL High Dead Time			42		ns



ADP1821

Parameter	Conditions	Min	Тур	Max	Unit
LOGIC THRESHOLDS (SHDN, SYNC, FREQ)					
SHDN, SYNC, FREQ Input High Voltage	$V_{VCC} = 3.7 \text{ V to } 5.5 \text{ V}$	2.0			V
SHDN, SYNC, FREQ Input Low Voltage	$V_{VCC} = 3.7 \text{ V to } 5.5 \text{ V}$			0.8	V
SYNC, FREQ Input Leakage Current	SYNC = FREQ = GND		0.1	1	μΑ
SHDN Pull-Down Resistance			100		kΩ
THERMAL SHUTDOWN					
Thermal Shutdown Threshold			145		°C
Thermal Shutdown Hysteresis			10		°C
PWGD OUTPUT					
FB Overvoltage Threshold	V _{FB} rising		750		mV
FB Overvoltage Hysteresis			35		mV
FB Undervoltage Threshold	V _{FB} rising		550		mV
FB Undervoltage Hysteresis			35		mV
PWGD Off Current	$V_{PWGD} = 5 V$			1	μΑ
PWGD Low Voltage	$I_{PWGD} = 10 \text{ mA}$		150	500	mV



ABSOLUTE MAXIMUM RATINGS

Table 2.

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Parameter	Rating
VCC, SHDN, SYNC, FREQ, COMP, SS, FB to	−0.3 V to +6 V
GND, PVCC to PGND, BST to SW	
BST to GND	-0.3 V to +30 V
CSL to GND	−1 V to +30 V
DH to GND	$(V_{SW} - 0.3 V)$ to
	$(V_{BST} + 0.3 V)$
DL to PGND	-0.3 V to
	$(V_{PVCC} + 0.3 V)$
SW to GND	−2 V to +30 V
PGND to GND	±2 V
θ _{JA} , 2-Layer (SEMI Standard Board)	150°C/W
θ_{JA} , 4-Layer (JEDEC Standard Board)	105°C/W
Operating Ambient Temperature Range	−40°C to +85°C
Operating Junction Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Maximum Soldering Lead Temperature	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings apply individually only, not in combination. Unless otherwise specified, all other voltages are referenced to GND.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

SIMPLIFIED BLOCK DIAGRAM

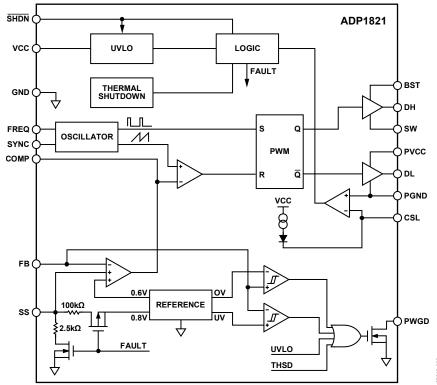


Figure 3. Simplified Block Diagram



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