



US010672458B1

(12) **United States Patent**
Shaeffer et al.

(10) **Patent No.:** **US 10,672,458 B1**
(45) **Date of Patent:** ***Jun. 2, 2020**

(54) **MEMORY SYSTEM TOPOLOGIES INCLUDING A BUFFER DEVICE AND AN INTEGRATED CIRCUIT MEMORY DEVICE**

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,621,339 A 11/1986 Wagner et al.
4,631,666 A 12/1986 Harris et al.
(Continued)

FOREIGN PATENT DOCUMENTS

CN 1540665 10/2004
CN 1577633 2/2005
(Continued)

OTHER PUBLICATIONS

“Draft Standard for a High-Speed Memory Interface (SyncLink),” Draft 0.99 IEEE P1596.7-199X, pp. 1-56 (1996), Microprocessor and Microcomputer Standards Subcommittee of the IEEE Computer Society. 66 pages.

(Continued)

Primary Examiner — Vu A Le

(57) **ABSTRACT**

Systems, among other embodiments, include topologies (data and/or control/address information) between an integrated circuit buffer device (that may be coupled to a master, such as a memory controller) and a plurality of integrated circuit memory devices. For example, data may be provided between the plurality of integrated circuit memory devices and the integrated circuit buffer device using separate segmented (or point-to-point link) signal paths in response to control/address information provided from the integrated circuit buffer device to the plurality of integrated circuit buffer devices using a single fly-by (or bus) signal path. An integrated circuit buffer device enables configurable effective memory organization of the plurality of integrated circuit memory devices. The memory organization represented by the integrated circuit buffer device to a memory controller may be different than the actual memory organization behind or coupled to the integrated circuit buffer device. The buffer device segments and merges the data transferred between the memory controller that expects a

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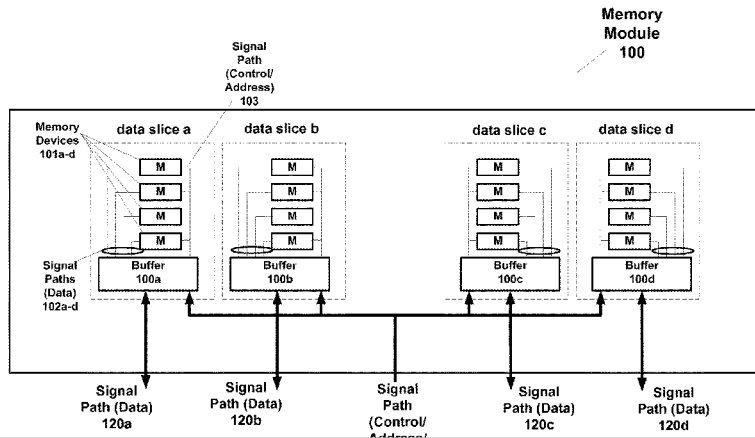
Related U.S. Application Data

(60) Continuation of application No. 16/214,986, filed on Dec. 10, 2018, now Pat. No. 10,535,398, which is a (Continued)

(51) **Int. Cl.**
G11C 7/00 (2006.01)
G11C 11/4093 (2006.01)
(Continued)

(52) **U.S. Cl.**
CPC **G11C 11/4093** (2013.01); **G06F 13/16** (2013.01); **G06F 13/4027** (2013.01);
(Continued)

(58) **Field of Classification Search**
CPC . G11C 11/4093; G06F 13/16; G06F 13/4027; G06F 13/4068
(Continued)



(56)

References Cited

U.S. PATENT DOCUMENTS

5,898,863	A	4/1999	Ofer et al.	6,502,161	B1	12/2002	Perego et al.
5,900,017	A	5/1999	Gendusio et al.	6,510,503	B2	1/2003	Gillingham et al.
5,901,294	A	5/1999	Tran et al.	6,510,506	B2	1/2003	Nagapudi et al.
5,910,921	A	6/1999	Beffa et al.	6,513,080	B1	1/2003	Haq
5,911,052	A	6/1999	Singhal et al.	6,513,091	B1	1/2003	Blackmon et al.
5,913,044	A	6/1999	Tran et al.	6,516,365	B2	2/2003	Horowitz et al.
5,917,760	A	6/1999	Millar	6,526,469	B1	2/2003	Drehmel et al.
5,923,893	A	7/1999	Moyer et al.	6,530,006	B1	3/2003	Dodd et al.
5,926,839	A	7/1999	Katayama	6,530,033	B1	3/2003	Raynham et al.
5,953,215	A	9/1999	Karabatsos	6,553,450	B1	4/2003	Dodd et al.
5,977,806	A	11/1999	Kikuchi	6,557,069	B1	4/2003	Drehmel et al.
5,982,238	A	11/1999	Soderquist	6,587,912	B2	7/2003	Leddige et al.
5,987,576	A	11/1999	Johnson et al.	6,604,180	B2	8/2003	Jeddeloh
6,006,318	A	12/1999	Hansen et al.	6,622,224	B1	9/2003	Cloud
6,016,282	A	1/2000	Keeth	6,625,687	B1	9/2003	Halbert et al.
6,034,878	A	3/2000	Osaka et al.	6,633,947	B1	10/2003	Holman et al.
6,038,682	A	3/2000	Norman	6,639,820	B1	10/2003	Khandekar et al.
6,065,092	A	5/2000	Roy	6,643,752	B1	11/2003	Donnelly et al.
6,092,229	A	7/2000	Boyle et al.	6,684,263	B2	1/2004	Horowitz et al.
6,097,883	A	8/2000	Dell et al.	6,690,191	B2	2/2004	Wu et al.
6,104,417	A	8/2000	Nielsen et al.	6,690,726	B1	2/2004	Yavits et al.
6,108,731	A	8/2000	Suzuki et al.	6,701,446	B2	3/2004	Tsern et al.
6,125,419	A	9/2000	Umemura et al.	6,708,248	B1	3/2004	Garrett, Jr. et al.
6,128,756	A	10/2000	Beffa	6,714,433	B2	3/2004	Doblar et al.
6,142,830	A	11/2000	Loeffler	6,720,643	B1	4/2004	Fox et al.
6,151,648	A	11/2000	Haq	6,742,098	B1	5/2004	Halbert et al.
6,154,821	A	11/2000	Barth et al.	6,754,117	B2	6/2004	Jeddeloh
6,154,826	A	11/2000	Wulf et al.	6,759,884	B2	7/2004	Tomita
6,154,855	A	11/2000	Norman	6,820,163	B1	11/2004	McCall et al.
6,160,423	A	12/2000	Haq	6,842,864	B1	1/2005	Barth et al.
6,182,257	B1	1/2001	Gillingham	6,853,938	B2	2/2005	Jeddeloh
6,185,644	B1	2/2001	Farmwald et al.	6,854,042	B1	2/2005	Karabatsos
6,185,654	B1	2/2001	Van Doren	6,864,524	B2	3/2005	Masleid et al.
6,208,273	B1	3/2001	Dye et al.	6,877,079	B2	4/2005	Yoo et al.
6,226,723	B1	5/2001	Gustayson et al.	6,889,284	B1	5/2005	Nizar et al.
6,247,100	B1	6/2001	Drehmel et al.	6,968,419	B1	11/2005	Holman
6,255,859	B1	7/2001	Haq	6,970,968	B1	11/2005	Holman
6,263,413	B1	7/2001	Motomura et al.	7,007,130	B1	2/2006	Holman
6,263,448	B1	7/2001	Tsern et al.	7,010,629	B1	3/2006	Frame et al.
6,266,252	B1	7/2001	Karabatsos	7,010,642	B2	3/2006	Perego et al.
6,272,034	B1	8/2001	Kinoshita et al.	7,038,956	B2	5/2006	Beer
6,272,609	B1	8/2001	Jeddeloh	7,110,400	B2	9/2006	Hronik
6,276,844	B1	8/2001	Coteus et al.	7,123,497	B2	10/2006	Matsui et al.
6,292,877	B1	9/2001	Ryan	7,127,022	B1	10/2006	Dieguez
6,317,252	B1	11/2001	Vahala et al.	7,254,075	B2	8/2007	Woo et al.
6,317,352	B1	11/2001	Halbert et al.	7,275,189	B2	9/2007	Ruckerbauer et al.
6,321,282	B1	11/2001	Horowitz et al.	7,320,047	B2	1/2008	Perego et al.
6,327,205	B1	12/2001	Haq	7,321,997	B2	1/2008	Zimmerman et al.
6,330,667	B1	12/2001	Klein	7,339,840	B2	3/2008	Wallner et al.
6,330,687	B1	12/2001	Griffith	7,404,050	B2	7/2008	Gregorius
6,345,321	B1	2/2002	Litaize et al.	7,519,894	B2	4/2009	WeiB et al.
6,349,051	B1	2/2002	Klein	7,523,244	B2	4/2009	Liaw et al.
6,369,605	B1	4/2002	Bonella et al.	7,615,857	B1	11/2009	Jouppi
6,401,167	B1	6/2002	Barth et al.	7,949,931	B2	5/2011	Lastras-Montano
6,408,402	B1	6/2002	Norman	8,060,774	B2	11/2011	Smith et al.
6,414,868	B1	7/2002	Wong et al.	2001/0000693	A1	5/2001	Hamamoto et al.
6,414,899	B2	7/2002	Afghahi et al.	2001/0039606	A1	11/2001	Jeddeloh
6,414,904	B2	7/2002	So	2001/0048616	A1	12/2001	Ayukawa et al.
6,425,064	B2	7/2002	Soderquist	2002/0024833	A1	2/2002	Song et al.
6,434,035	B2	8/2002	Miersch et al.	2002/0024834	A1	2/2002	Jeon et al.
6,442,057	B1	8/2002	Song et al.	2002/0083287	A1	6/2002	Zumkehr et al.
6,442,644	B1	8/2002	Gustavson et al.	2002/0112119	A1	8/2002	Halbert et al.
6,442,742	B1	8/2002	Sugibayashi	2002/0124153	A1	9/2002	Litaize et al.
6,446,158	B1	9/2002	Karabatsos	2002/0124203	A1	9/2002	Fang
6,449,213	B1	9/2002	Dodd et al.	2002/0129215	A1	9/2002	Yoo et al.
6,449,679	B2	9/2002	Ryan	2002/0135394	A1	9/2002	Ahn et al.
6,449,703	B2	9/2002	Jeddeloh	2002/0144071	A1	10/2002	Williams et al.
6,449,727	B1	9/2002	Toda	2002/0184462	A1	12/2002	Jeddeloh
6,466,496	B2	10/2002	Kuge	2003/0012229	A1	1/2003	Braun
6,477,592	B1	11/2002	Chen et al.	2003/0018880	A1	1/2003	Litaize et al.
6,477,614	B1	11/2002	Leddige et al.	2003/0043613	A1	3/2003	Doblar et al.
6,480,409	B2	11/2002	Park et al.	2003/0074490	A1	4/2003	Pochmuller
6,480,927	B1	11/2002	Bauman	2003/0090879	A1	5/2003	Doblar et al.
				2003/0120895	A1	6/2003	Litaize et al.
				2003/0177313	A1	9/2003	Iyer et al.
				2003/0204783	A1	10/2003	Kuroda
				2004/0015650	A1	1/2004	Zumkehr et al.

(56)

References Cited

U.S. PATENT DOCUMENTS

2004/0085795	A1	5/2004	Braun et al.	
2004/0095838	A1	5/2004	Li	
2004/0105292	A1	6/2004	Matsui	
2004/0125666	A1	7/2004	Lee et al.	
2004/0133736	A1	7/2004	Kyung	
2004/0143773	A1	7/2004	Chen	
2004/0145935	A1	7/2004	Jakobs	
2004/0151038	A1	8/2004	Ruckerbauer et al.	
2004/0164334	A1	8/2004	Masleid et al.	
2004/0221106	A1	11/2004	Perego et al.	
2004/0150024	A1	12/2004	Mazoyer et al.	
2004/0246767	A1	12/2004	Vogt	
2004/0246785	A1	12/2004	Vogt	
2004/0246786	A1	12/2004	Vogt	
2004/0250024	A1	12/2004	Vogt	
2004/0250153	A1	12/2004	Vogt	
2004/0250181	A1	12/2004	Vogt et al.	
2004/0256638	A1	12/2004	Perego et al.	
2004/0257847	A1	12/2004	Matsui et al.	
2004/0260991	A1	12/2004	Vogt et al.	
2004/0267481	A1	12/2004	Resnick et al.	
2005/0108469	A1	5/2005	Freeman et al.	
2005/0236703	A1	10/2005	Kazi et al.	
2006/0095592	A1	5/2006	Borkenhagen	
2007/0070669	A1	3/2007	Tsern	
2008/0082763	A1	4/2008	Rajan et al.	
2008/0294838	A1*	11/2008	Houston	G06F 9/4403 711/103
2009/0198924	A1	8/2009	Tsern et al.	
2009/0321893	A1	12/2009	Somasekhar et al.	
2010/0074038	A1	3/2010	Ruckerbauer et al.	
2010/0217915	A1	8/2010	O'Connor et al.	

FOREIGN PATENT DOCUMENTS

DE	10208726	4/2010
EP	0198429	10/1986
EP	0282070	A2 9/1988
EP	0811916	A2 12/1997
EP	0813204	A2 12/1997
EP	0947070	10/1999
EP	1069509	A2 1/2001
GB	2383656	7/2003
JP	04-186599	7/1992
JP	10-207785	8/1998
JP	10-207786	8/1998
JP	11-297092	10/1999
JP	11-317503	11/1999
JP	2000-030487	1/2000
JP	2000-040035	2/2000
JP	2002-064145	2/2002
JP	2003-324155	11/2003
JP	2004-055100	2/2004
JP	2004-139552	A2 5/2004
JP	2004-327474	11/2004
JP	2006-302129	11/2006
WO	WO-1998-012637	3/1998
WO	WO-1999-030240	A1 6/1999
WO	WO-99/41666	A1 8/1999
WO	WO-1999-041667	A1 8/1999
WO	WO-2002-025454	A2 3/2002
WO	WO-2004/025663	3/2004
WO	WO-2004-111856	12/2004
WO	WO-2005/066965	7/2005
WO	WO-2007-028109	A2 3/2007
WO	WO-2007-038225	4/2007

OTHER PUBLICATIONS

"Intel 82804AA Memory Repeater Hub for SDRAM (MRH-S)", Datasheet, Intel Corp., pp. 1-48 (Nov. 1999).

"Inter Partes Reexamination Communication," issued in Inter Partes Reexam Control No. 95/000,166, mail date (from USPTO) Oct. 19, 2007, 23 pages.

"Order Granting/Denying Request for Inter Partes Reexamination," issued in Inter Partes Reexam Control No. 95/000,183, mail date (from USPTO) Oct. 19, 2007, 21 pages.

"SLDRAM 400 Mb/s/pin Command/Address Repeater", SLD10400 Rev. 5, SLDDRAM Consortium, pp. 1-12, (Jan. 7, 1998).

Intel Developer Forum, "DDR2 Memory in 2004 Servers—Recipes for Successful Designs", Sep. 2003. 33 pages.

Allan, Graham, "DDR SDRAM/SGRAM: An Interpretation of the JEDEC Standard," MOSAID Technologies Inc., Sep. 25, 1998. 73 pages.

AMD letter entitled "Re: Patent and Patent Applications Declaration Concerning Fully Buffered DIMMs," dated Apr. 12, 2004, referenced in Excel Spreadsheet, entitled "Patents.xls." 1 page.

Cataldo, A., "TI Fields DSP-Based Media Processor on a DIMM", EE Times (Jan. 2000). 2 pages.

Chakraborty, Kanad, "BISRAMGEN: A Silicon Compiler for Built-In Self-Repairable Random-Access Memories," University of Michigan, The Sciences and Engineering, vol. 58-02B, 1997. 145 pages. Chinese Office Action dated Nov. 6, 2009, The Patent Office of the People's Republic of China, Chinese Patent Application No. 200680041998.3 filed Sep. 21, 2006, 10 pages.

CN First Office Action dated Mar. 19, 2012 re CN Application No. 200880016745.X. 25 pages.

CN First Office Action dated Nov. 6, 2009 re CN Application No. 200680041998.3. 10 pages.

CN Office Action dated Apr. 2, 2011 re CN Application No. 201010184674.3. 34 pages.

CN Office Action dated Jan. 29, 2012 in CN Application No. 200680041998.3, Includes English Translation. 30 pages.

CN Office Action dated Oct. 26, 2011 in CN Application No. 200680041998.3. 3 pages.

CN Rejection Decision dated Jan. 29, 2012 re CN Application No. 200680041998.3. 30 pages.

CN Response dated Aug. 16, 2011 to the Third Office Action dated Jun. 9, 2011 re CN Application No. 200680041998.3. 4 Pages.

CN Response dated Aug. 17, 2011 to the Office Action dated Apr. 2, 2011 re CN Application No. 201010184674.3. 19 Pages.

CN Response dated Jun. 25, 2012 to the Third Office Action dated Apr. 12, 2012 in CN Application No. 201010184674.3. 19 pages.

CN Response dated May 20, 2010 re Cn Application No. 200680041993.3 no translation. 20 Pages.

CN Response submitted on Mar. 21, 2011 to the Second Office Action of Jan. 7, 2011 re CN Application No. 200680041998.3. 26 pages.

CN Response to Office Action dated May 20, 2010, Chinese Patent Application No. 200680041998.3 Filed Sep. 21, 2006. 20 Pages.

CN Second Office Action dated Jan. 7, 2011 re CN Application No. 200680041998.3. 22 pages.

CN Second Office Action dated Oct. 26, 2011 re CN Application No. 201010184674.3. 8 Pages.

CN Third Office Action dated Apr. 12, 2012 re CN Application No. 201010184674.3. 6 pages.

CN Third Office Action dated Jun. 9, 2011 re CN Application No. 200680041998.3. 27 pages.

Communication from European Patent Office dated Mar. 9, 2007 in EP Application No. 05001739.8-2210. 4 pages.

David, Howard Intel Developer Forum, "Fully Buffered Dimm (FB-DIMM) Design Considerations", Feb. 18, 2004. 37 pages.

Doettling et al., "S390 Parallel Enterprise Server Generation 3: A Balanced System and Cache Structure," IBM J. Res. Develop., vol. 41 (No. 4/5), Jul./Sep. 1997, pp. 405-428. 24 pages.

EP Office Action dated Jul. 6, 2012 in EP Application No. 06815141.4-2210. 5 pages.

EP Office Action dated Sep. 17, 2010, EP Patent Application No. 06815141.4, filed Sep. 2006. 5 Pages.

EP Office Communication pursuant to Article 94(3) EPC, dated Sep. 17, 2010, in EP Application No. 06815141.4-2210. 5 pages.

(56)

References Cited

OTHER PUBLICATIONS

EP Search Report dated May 18, 2006 re EP Application No. 05001769.8. 3 Pages.

Excel Spreadsheet, entitled "Patents and Patent Applications that May be Related to FB-DIMM," available at "<http://www.jedec.org/download/search/FBDIMM/patents.xls>," Jan. 23, 2006. 2 pages.

Exhibit AH, Tab 1—In the matter of Rambus, Inc., FTC Docket No. 9302, Opinion of the Commission, re Request for Inter Partes Reexamination of U.S. Pat. No. 6,426,916, Aug. 2, 2006 (date shown on page from FTC website for Docket No. 9302). 121 pages.

Expert Report of Robert J. Murphy Regarding Patent Validity, dated Apr. 13, 2005, from *Hynix Semiconductor Inc. et al. v. Rambus Inc.*, No. 00-20905 RMW (N.D. Cal.) 112 pages.

Extended European Search Report, dated Apr. 13, 2006, from European Application No. 05 02 6720. 7 pages.

Extended European Search Report, dated Aug. 24, 2007, from European Application No. 06 12 5946. 4 pages.

Extended European Search Report, dated Aug. 6, 2007, from European Application No. 06 12 5958.6. 4 pages.

Extended European Search Report, dated Jul. 18, 2007, from European Application No. 06 12 5954.5. 4 pages.

Farmwald, M. et al., (Rambus Inc.) "A fast path to one memory," *IEEE Spectrum*, Oct. 1992, pp. 50-51. 2 pages.

Gibson, Jerry D., Editor-in-Chief, "The Mobile Communications Handbook," copyright 1996 CRC Press, Inc., p. 24. 3 pages.

Gillingham et al., "SLDRAM: High Performance Open-Standard Memory," *IEEE Micro*, Nov./Dec. 1997, pp. 29-39, vol. 17, No. 6, Institute of Electrical and Electronics Engineers, Inc., Los Alamitos, California. 11 pages.

Gillingham, Peter, "SLDRAM Architectural and Functional Overview," SLDRAM Consortium, Aug. 29, 1997, pp. 1-14. 14 pages.

Gjessing, S. et al., "A RAM link for high speed", *IEEE Spectrum*, Oct. 1992, pp. 52-53.

Graham Allan, MOSAID Technologies Inc., "DDR SDRAM/SGRAM an Interpretation of the JEDEC Standard", Sep. 25, 1998 72 pages.

Gustavson et al., "The Scalable Coherent Interface Project (Superbus)," *SCI* Aug. 22, 1988, Draft, Rev. 14. 16 pages.

Gustavson, David B., "Scalable Coherent Interface", Nov. 28, 1988, Invited paper presented at COMPCON Spring 89, San Francisco, CA, *IEEE* pp. 536-538, Feb. 24-Mar. 3, 1989. 3 pages.

Gustavson, David B., P1596: *SCI*, A Scalable Coherent Interface Bus Specification Components (Nov. 28, 1988). 3 pages.

Gustavson, David et al., "Macintosh HD: Desktop Folder: SLDRAMrepeaterConcerns", Sunday, Nov. 23, 1997, 4 pages.

Herriot, J., "Software is the Key to Wafer-Scale RAM," *High Performance Systems*, vol. 11, No. 1, Jan. 1990, pp. 36-37.

Hynix's Motion for Leave to File Motion for Partial Reconsideration of Claim Construction and Summary Judgment Orders, dated Aug. 5, 2005, from *Hynix Semiconductor Inc. et al. v. Rambus Inc.*, No. 00-20905 RMW (N.D. Cal.) 6 pages.

Hynix's Motion for Reconsideration of Construction of "Device" and Related Summary Judgment Orders, dated Oct. 18, 2005, from *Hynix Semiconductor Inc. et al. v. Rambus Inc.*, No. 00-20905 RMW (N.D. Cal.) 31 pages.

Hynix's Opposition to Rambus's Motion for Summary Judgment of Infringement by Hynix's Counterclaim Products, dated Nov. 2, 2007, from *Rambus Inc. v. Hynix Semiconductor Inc. et al.*, No. 05-00334 RMW (N.D. Cal.) 16 pages.

Hynix's Reply in Support of its Motion for Reconsideration of Construction of "Device" and Related Summary Judgment Orders, dated Nov. 7, 2005, from *Hynix Semiconductor Inc. et al. v. Rambus Inc.*, No. 00-20905 RMW (N.D. Cal.) 11 pages.

Hynix's Reply Re: Motion for a New Trial on Invalidity Based on Prior Art, dated Jun. 27, 2006, Case No. CV 00-20905 RMW. 8 pages.

Hynix's Supplemental Brief in Support of its Motion for New Trial on Invalidity (KSR), dated Jul. 6, 2007, from *Hynix Semiconductor*

IBM, "184 Pin DIMM Design Updates/Ramifications for Unbuffered and Registered DDR DIMMs," *JC-42.5*, Dec. 1999, pp. 1-12. 13 pages.

IBM, "Application Note DDR SDRAM Module Serial Presence Detect Definitions", Oct. 1999, pp. 1-34. 35 pages.

IBM, Micron Technology and Reliance Computer Corporation, "DDR SDRAM Registered DIMM," Design Specification, Revision 0.6, Nov. 1999. 62 pages.

IEEE Standard for Scalable Coherent Interface (SCI), "Microprocessor and Microcomputer Standards Subcommittee of the IEEE Computer Society," *IEEE Std. 1596-1992*, Aug. 2, 1993. 270 pages.

Inphi letter entitled "Re: License assurance for patents and applications essential to Fully Buffered DIMM proposal," dated Mar. 3, 2005, referenced in Excel Spreadsheet, entitled "Patents.xls." 1 page.

Inphi letter entitled "Re: License assurance for patents relevant to FBDIMM," dated Jun. 6, 2005, referenced in Excel Spreadsheet, entitled "Patents.xls." 1 page.

Institute of Electrical and Electronics Engineers, "802.3ab—A Tutorial Presentation," Slides, Mar. 1998. 63 pages Duplicate.

Intel Developer Forum, "Fully Buffered DIMM (FB-DIMM) Server Memory Architecture: Capacity, Performance, Reliability, and Longevity", Feb. 18, 2004. 106 pages.

Interlocutory Decision in Opposition Proceedings, dated Nov. 27, 2002, from European Patent No. EP 0 525 068. 38 pages.

International Preliminary Report dated Oct. 15, 2009, Patent Cooperation Treaty; International Application No. PCT/US2008/059268 filed Apr. 3, 2008. 11 pages.

International Search Report & The Written Opinion of the International Searching Authority, Patent Cooperation Treaty, Application No. PCT/US2008/059268 filed on Apr. 3, 2008, dated Sep. 23, 2008. 13 pages.

International Search Report and Written Opinion dated May 2, 2007 in International Application No. PCT/US2006/036894. 15 pages.

International Search Report in PCT/US05/17066, dated Nov. 2, 2005. 2 pages.

James, David V., "Scalable I/O Architecture for Buses," *COMPCON Spring 1989*, *SCI*, Nov. 28, 1988. 7 pages.

JC-42.3 Task Group Minutes, "Meeting on Synchronous DRAM Ballots," Las Vegas, Nevada, Jan. 21, 1993. 19 pages.

Jeddeloh, Joe, "Fully Buffered DIMM (FB-DIMM)," *Advanced Systems Technology*, Micron Technology, Inc. Apr. 15-16, 2004. 32 pages.

JEDEC Standard No. 21-C, pp. 4.20-4-1 through 4.20.4-69, 4.20.4-184 Pin, PC1600/2100 DDR SDRAM Registered DIMM Design Specification, Revision 1.2, Feb. 2002. 68 pages.

JEDEC Standard- "FBDIMM Specification: High Speed Differential PTP Link at 1.5V," *JESD8-18*, Sep. 2006, available at "<http://www.jedec.org/download/search/JESD8-18.pdf>". 60 pages.

John, Lizzy Kurian, "VaWiRAM: A Variable Width Random Access Memory Module," 1995 *IEEE*, 9th International Conference on VLSI Design—1996. pp. 219-224. 6 pages.

Johnson, B., "Direct RDRAM Basic Architecture and Program Overview", Intel Developer Forum, pp. 1-14, (Sep. 1998). 28 pages.

Johnson, Dave et al., "Intel iAPX 432-VLSI Building Blocks for a Fault-Tolerant Computer," *AFIPS Conference Proceedings*, 1983 National Computer Conference, pp. 531-537 (May 16-19, 1983). 9 pages.

Joint Claim Construction and Prehearing Statement Pursuant to Patent Local Rule 4-3, dated Jul. 11, 2007, from *Rambus Inc. v. Micron Technology, Inc. et al.*, No. 06-00244 RMW (N.D. Cal.) 233 pages.

Jones, F. (United Memories, Inc.) "A new era of fast dynamic RAMs", *IEEE Spectrum*, Oct. 1992, pp. 43-49.

JP Office Action dated Dec. 27, 2011 in JP Application No. 2008-532397. 6 pages.

JP Office Action dated Jul. 11, 2012 in JP Application No. 2008-532397. 6 pages.

JP Office Action dated Jul. 6, 2012 in JP Application No. 2010-502293. 4 pages.

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