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TI unveils next-generation 3-A DDR termination regulatorLinear regulator supports DDR3 power requirements for

Posted on August 6, 2008 by [Electronic Products](#)

TI unveils next-generation 3-A DDR termination
regulatorLinear regulator supports DDR3 power requirements
for low-power-mode memory termination

DALLAS (Aug. 4, 2008) – Texas Instruments Incorporated (TI) (NYSE:TXN) introduced today a sink/source double data rate (DDR) termination regulator that supports all power management requirements for DDR, DDR2, DDR3 and DDR4 low-power memory termination. The new easy-to-use regulator requires only 20 uF of ceramic output capacitance, nearly 80 percent less capacitance than competitive solutions. Designers can therefore use the device to achieve smaller and lower-cost

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electronics, including digital TVs, Set-Top boxes, VGA cards, telecom, datacom, notebook and desktop computers, and an increasingly wide range of consumer electronics. See: www.ti.com/tps51200-pr.

The wide-bandwidth internal transconductance, Gm amplifier and integral dynamic voltage positioning enables ultra-fast transient response with minimal external output capacitance. In a typical application with a -1.5-A to +1.5-A load step, the output voltage variation is less than 25 mV. TPS51200 is designed to work with bias voltage between 2.375 and 3.5V, which makes it very attractive in the systems where only 2.5 or 3.3V rail is available. Additionally, the device includes the S3 sleep-state control during suspend to RAM.

The TPS51200 can also be used as a general-purpose, high-performance low dropout (LDO) regulator with an input range of 1.1 to 3.5V. The device supports tracking start-up and shutdown features when the enable pin is connected to the system bus voltage, which simplifies the design process by allowing the designer to easily implement sequencing in multi-rail systems.

The TPS51200 enhances TI's broad portfolio of DDR memory power solutions, including the TPS51100 DDR termination regulator, TPS51116 DDR Power Switcher with integrated sink/source LDO and TPS40042 low-voltage tracking switching regulator for DDR termination. The TPS51200 also complements TI's broad portfolio of DDR, DDR2 and DDR3 phase-locked loops (PLLs) and LDOs for memory technologies, including the SN74SSQE32882, PLL integrated DDR3 register for registered dual in-line memory modules, which is available in full production.

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Pricing and availability

TPS51200 is currently available in volume from TI and its authorized distributors in a thermally-enhanced SON-10 PowerPAD™ integrated circuit package. Suggested resale price is \$0.90 in quantities of 1,000 units. Evaluation modules are \$49 each and can be ordered through www.power.ti.com.

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