COMPLETE DDR, DDR2 AND DDR3 MEMORY POWER SOLUTION SYNCHRONOUS BUCK CONTROLLER, 3-A LDO, BUFFERED REFERENCE

FEATURES

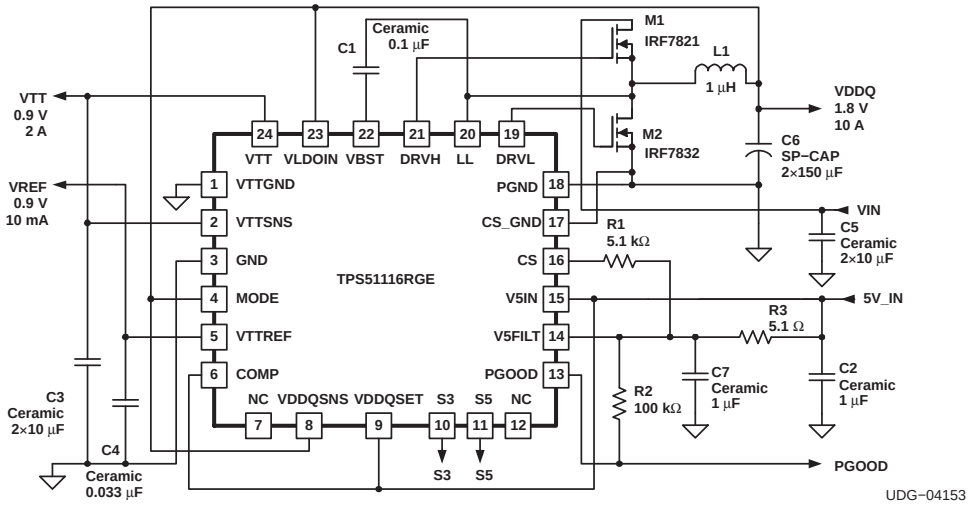
- **Synchronous Buck Controller (VDDQ)**
  - **Wide-Input Voltage Range: 3.0-V to 28-V**
  - **D−CAP™ Mode with 100-ns Load Step Response**
  - **Current Mode Option Supports Ceramic Output Capacitors**
  - **Supports Soft-Off in S4/S5 States**
  - **Current Sensing from $R_{DS(on)}$ or Resistor**
  - **2.5-V (DDR), 1.8-V (DDR2), Adjustable to 1.5-V (DDR3) or Output Range 0.75-V to 3.0-V**
  - **Equipped with Powergood, Overvoltage Protection and Undervoltage Protection**
- **3-A LDO (VTT), Buffered Reference (VREF)**
  - **Capable to Sink and Source 3 A**
  - **LDO Input Available to Optimize Power Losses**
  - **Requires only 20-µF Ceramic Output Capacitor**
  - **Buffered Low Noise 10-mA VREF Output**
  - **Accuracy 20 mV for both VREF and VTT**
  - **Supports High-Z in S3 and Soft-Off in S4/S5**
  - **Thermal Shutdown**

DESCRIPTION

The TPS51116 provides a complete power supply for DDR/SSTL-2, DDR2/SSTL-18, and DDR3 memory systems. It integrates a synchronous buck controller with a 3-A sink/source tracking linear regulator and buffered low noise reference. The TPS51116 offers the lowest total solution cost in systems where space is at a premium. The TPS51116 synchronous controller runs fixed 400kHz pseudo-constant frequency PWM with an adaptive on-time control that can be configured in D-CAP™ Mode for ease of use and fastest transient response or in current mode to support ceramic output capacitors. The 3-A sink/source LDO maintains fast transient response only requiring 20-µF (2 × 10 µF) of ceramic output capacitance. In addition, the LDO supply input is available externally to significantly reduce the total power losses. The TPS51116 supports all of the sleep state controls placing VTT at high-Z in S3 (suspend to RAM) and discharging VDDQ, VTT and VTTREF (soft-off) in S4/S5 (suspend to disk). TPS51116 has all of the protection features including thermal shutdown and is offered in both a 20-pin HTSSOP PowerPAD™ package and 24-pin 4″ QFN.

APPLICATIONS

- **DDR/DDR2/DDR3 Memory Power Supplies**
- **SSTL-2 SSTL-18 and HSTL Termination**



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

T_A	PACKAGE	ORDERABLE PART NUMBER	PINS	OUTPUT SUPPLY	MINIMUM ORDER QUANTITY
-40°C to 85°C	PLASTIC HTSSOP PowerPAD (PWP)	TPS51116PWP	20	Tube	70
		TPS51116PWPR		Tape-and-reel	2000
		TPS51116PWPRG4		Tape-and-reel	2000
	PLASTIC QUAD FLAT PACK (QFN)	TPS51116RGE	24	Tube	90
		TPS51116RGER		Large tape-and-reel	3000
		TPS51116RGET		Small tape-and-reel	250

(1) All packaging options have Cu NIPDAU lead/ball finish.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range unless otherwise noted

			TPS51116	UNITS
V_{IN}	Input voltage range	VBST	-0.3 to 36	V
		VBST wrt LL	-0.3 to 6	
		CS, MODE, S3, S5, VTTSNS, VDDQSNS, V5IN, VLDOIN, VDDQSET, V5FILT	-0.3 to 6	
		PGND, VTTGND, CS_GND	-0.3 to 0.3	
V_{OUT}	Output voltage range	DRVH	-1.0 to 36	V
		LL	-1.0 to 30	
		COMP, DRVL, PGOOD, VTT, VTTREF	-0.3 to 6	
T_A	Operating ambient temperature range		-40 to 85	°C
T_{stg}	Storage temperature		-55 to 150	

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.

DISSIPATION RATINGS

PACKAGE	T_A < 25°C POWER RATING (W)	DERATING FACTOR ABOVE T_A = 25°C (mW/°C)	T_A = 85°C POWER RATING (W)
20-pin PWP	2.53	25.3	1.01
24-pin RGE	2.20	22.0	0.88

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RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
Supply voltage, V5IN, V5FILT		4.75	5.25	V
Voltage range	VBST, DRVH	-0.1	34	V
	LL	-0.6	28	
	VLDOIN, VTT, VTTSNS, VDDQSNS	-0.1	3.6	
	VTTREF	-0.1	1.8	
	PGND, VTTGND, CS_GND	-0.1	0.1	
	S3, S5, MODE, VDDQSET, CS, COMP, PGOOD, DRVL	-0.1	5.25	
Operating free-air temperature, T_A		-40	85	°C

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ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, V_{V5IN} = 5 V(1), VLDOIN is connected to VDDQ output (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{V5IN1}	Supply current 1, V5IN(1)	T_A = 25°C, No load, V_{S3} = V_{S5} = 5 V, COMP connected to capacitor		0.8	2	mA
I_{V5IN2}	Supply current 2, V5IN(1)	T_A = 25°C, No load, V_{S3} = 0 V, V_{S5} = 5 V, COMP connected to capacitor		300	600	µA
I_{V5IN3}	Supply current 3, V5IN(1)	T_A = 25°C, No load, V_{S3} = 0 V, V_{S5} = 5 V, V_{COMP} = 5 V		240	500	
$I_{V5INSDN}$	Shutdown current, V5IN(1)	T_A = 25°C, No load, V_{S3} = V_{S5} = 0 V		0.1	1.0	
$I_{VLDOIN1}$	Supply current 1, VLDOIN	T_A = 25°C, No load, V_{S3} = V_{S5} = 5 V		1	10	
$I_{VLDOIN2}$	Supply current 2, VLDOIN	T_A = 25°C, No load, V_{S3} = 5 V, V_{S5} = 0 V,		0.1	10	
$I_{VLDOINSDN}$	Standby current, VLDOIN	T_A = 25°C, No load, V_{S3} = V_{S5} = 0 V		0.1	1.0	
VTTREF OUTPUT						
V_{VTTREF}	Output voltage, VTTREF			$V_{VDDQSNS}$/2		V
$V_{VTTREFTOL}$	Output voltage tolerance	-10 mA < I_{VTTREF} < 10 mA, $V_{VDDQSNS}$ = 2.5 V, Tolerance to $V_{VDDQSNS}$/2	-20		20	mV
		-10 mA < I_{VTTREF} < 10 mA, $V_{VDDQSNS}$ = 1.8 V, Tolerance to $V_{VDDQSNS}$/2	-18		18	
		-10 mA < I_{VTTREF} < 10 mA, $V_{VDDQSNS}$ = 1.5 V, Tolerance to $V_{VDDQSNS}$/2	-15		15	
$V_{VTTREFSRC}$	Source current	$V_{VDDQSNS}$ = 2.5 V, V_{VTTREF} = 0 V	-20	-40	-80	mA
$V_{VTTREFSNK}$	Sink current	$V_{VDDQSNS}$ = 2.5 V, V_{VTTREF} = 2.5 V	20	40	80	
VTT OUTPUT						
V_{VTTSNS}	Output voltage, VTT	V_{S3} = V_{S5} = 5 V, V_{VLDOIN} = $V_{VDDQSNS}$ = 2.5 V		1.25		V
		V_{S3} = V_{S5} = 5 V, V_{VLDOIN} = $V_{VDDQSNS}$ = 1.8 V		0.9		
		V_{S3} = V_{S5} = 5 V, V_{VLDOIN} = $V_{VDDQSNS}$ = 1.5 V		0.75		
$V_{VTTTOL25}$	VTT output voltage tolerance to VTTREF	V_{S3} = V_{S5} = 5 V, I_{VTT} = 0 A	-20		20	mV
		V_{S3} = V_{S5} = 5 V, $\|I_{VTT}\|$ < 1.5 A	-30		30	
		V_{S3} = V_{S5} = 5 V, $\|I_{VTT}\|$ < 3 A	-40		40	
$V_{VTTTOL18}$	VTT output voltage tolerance to VTTREF	V_{S3} = V_{S5} = 5 V, I_{VTT} = 0 A	-20		20	
		V_{S3} = V_{S5} = 5 V, $\|I_{VTT}\|$ < 1 A	-30		30	
		V_{S3} = V_{S5} = 5 V, $\|I_{VTT}\|$ < 2 A	-40		40	
$V_{VTTTOL15}$	VTT output voltage tolerance to VTTREF	V_{S3} = V_{S5} = 5 V, I_{VTT} = 0 A	-20		20	
		V_{S3} = V_{S5} = 5 V, $\|I_{VTT}\|$ < 1 A	-30		30	
		V_{S3} = V_{S5} = 5 V, $\|I_{VTT}\|$ < 2 A	-40		40	
$I_{VTTTOCLSRC}$	Source current limit, VTT	V_{VLDOIN} = $V_{VDDQSNS}$ = 2.5 V, V_{VTT} = V_{VTTSNS} = 1.19 V, PGOOD = HI	3.0	3.8	6.0	A
		V_{VLDOIN} = $V_{VDDQSNS}$ = 2.5 V, V_{VTT} = 0 V	1.5	2.2	3.0	
$I_{VTTTOCLSNK}$	Sink current limit, VTT	V_{VLDOIN} = $V_{VDDQSNS}$ = 2.5 V, V_{VTT} = V_{VTTSNS} = 1.31 V, PGOOD = HI	3.0	3.6	6.0	
		V_{VLDOIN} = $V_{VDDQSNS}$ = 2.5 V, V_{VTT} = V_{VDDQ}	1.5	2.2	3.0	
I_{VTTLK}	Leakage current, VTT	V_{S3} = 0 V, V_{S5} = 5 V, V_{VTT} = $V_{VDDQSNS}$ /2	-10		10	µA
$I_{VTTBIAS}$	Input bias current, VTTSNS	V_{S3} = 5 V, V_{VTTSNS} = $V_{VDDQSNS}$ /2	-1	-0.1	1	
$I_{VTTSNSLK}$	Leakage current, VTTSNS	V_{S3} = 0 V, V_{S5} = 5 V, V_{VTT} = $V_{VDDQSNS}$ /2	-1		1	
$I_{VTTDisch}$	Discharge current, VTT	T_A = 25°C, V_{S3} = V_{S5} = $V_{VDDQSNS}$ = 0 V, V_{VTT} = 0.5 V	10	17		mA

(1) V5IN references to PWP packaged devices should be interpreted as V5FILT references to RGE packaged devices.

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ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range, V_{V5IN} = 5 V, VLDOIN is connected to VDDQ output (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDDQ OUTPUT						
V_{VDDQ}	Output voltage, VDDQ	T_A = 25°C, $V_{VDDQSET}$ = 0 V, No load	2.465	2.500	2.535	V
		0°C ≤ T_A ≤ 85°C, $V_{VDDQSET}$ = 0 V, No load (2)	2.457	2.500	2.543	
		-40°C ≤ T_A ≤ 85°C, $V_{VDDQSET}$ = 0 V, No load (2)	2.440	2.500	2.550	
		T_A = 25°C, $V_{VDDQSET}$ = 5 V, No load(2)	1.776	1.800	1.824	
		0°C ≤ T_A ≤ 85°C, $V_{VDDQSET}$ = 5V, No load(2)	1.769	1.800	1.831	
		-40°C ≤ T_A ≤ 85°C, $V_{VDDQSET}$ = 5V, No load(2)	1.764	1.800	1.836	
		-40°C ≤ T_A ≤ 85°C, Adjustable mode, No load(2)	0.75		3.0	
$V_{VDDQSET}$	VDDQSET regulation voltage	T_A = 25°C, Adjustable mode	742.5	750.0	757.5	mV
		0°C ≤ T_A ≤ 85°C, Adjustable mode	740.2	750.0	759.8	
		-40°C ≤ T_A ≤ 85°C, Adjustable mode	738.0	750.0	762.0	
$R_{VDDQSNS}$	Input impedance, VDDQSNS	$V_{VDDQSET}$ = 0 V		215		kΩ
		$V_{VDDQSET}$ = 5 V		180		
		Adjustable mode		460		
$I_{VDDQSET}$	Input current, VDDQSET	$V_{VDDQSET}$ = 0.78 V, COMP = Open		-0.04		µA
		$V_{VDDQSET}$ = 0.78 V, COMP = 5 V		-0.06		
$I_{VDDQDisch}$	Discharge current, VDDQ	V_{S3} = V_{S5} = 0 V, $V_{VDDQSNS}$ = 0.5 V, V_{MODE} = 0 V	10	40		mA
$I_{VLDOINDisch}$	Discharge current, VLDOIN	V_{S3} = V_{S5} = 0 V, $V_{VDDQSNS}$ = 0.5 V, V_{MODE} = 0.5 V		700		
TRANSCONDUCTANCE AMPLIFIER						
gm	Gain	T_A = 25°C	240	300	360	µS
$I_{COMPSNK}$	COMP maximum sink current	V_{S3} = 0 V, V_{S5} = 5 V, $V_{VDDQSET}$ = 0 V, $V_{VDDQSNS}$ = 2.7 V, V_{COMP} = 1.28 V		13		µA
$I_{COMPSRC}$	COMP maximum source current	V_{S3} = 0 V, V_{S5} = 5 V, $V_{VDDQSET}$ = 0 V, $V_{VDDQSNS}$ = 2.3 V, V_{COMP} = 1.28 V		-13		
V_{COMPHI}	COMP high clamp voltage	V_{S3} = 0 V, V_{S5} = 5 V, $V_{VDDQSET}$ = 0 V, $V_{VDDQSNS}$ = 2.3 V, V_{CS} = 0 V	1.31	1.34	1.37	V
V_{COMPLO}	COMP low clamp voltage	V_{S3} = 0 V, V_{S5} = 5 V, $V_{VDDQSET}$ = 0 V, $V_{VDDQSNS}$ = 2.7 V, V_{CS} = 0 V	1.18	1.21	1.24	
DUTY CONTROL						
T_{ON}	Operating on-time	V_{IN} = 12 V, $V_{VDDQSET}$ = 0 V		520		ns
T_{ON0}	Startup on-time	V_{IN} = 12 V, $V_{VDDQSNS}$ = 0 V		125		
$T_{ON(min)}$	Minimum on-time	T_A = 25°C(2)		100		
$T_{OFF(min)}$	Minimum off-time	T_A = 25°C(2)		350		
ZERO CURRENT COMPARATOR						
V_{ZC}	Zero current comparator offset		-6	0	6	mV
OUTPUT DRIVERS						
R_{DRVH}	DRVH resistance	Source, I_{DRVH} = -100 mA		3	6	Ω
		Sink, I_{DRVH} = 100 mA		0.9	3	
R_{DRVL}	DRVL resistance	Source, I_{DRVL} = -100 mA		3	6	
		Sink, I_{DRVL} = 100 mA		0.9	3	
T_D	Dead time	LL-low to DRVL-on (2)		10		ns
		DRVL-off to DRVH-on(2)		20		

(2) Ensured by design. Not production tested.

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