DDR2 Fully Buffered DIMM

240pin FBDIMMs based on 1Gb C-die

60FBGA with Lead-Free
(RoHS compliant)

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Revision History

Revision	Month	Year	History
1.0	March	2007	- First Released.
1.1	April	2007	- Added 2GB density
1.2	April	2007	- Changed AMB device operation temperature symbol(Tj to Tcase)
1.3	April	2007	- Corrected Typo
1.4	June	2007	- Added 800 FBD
1.5	November	2007	- Changed Ordering Information and Added AL Feature
1.52	April	2008	- Corrected mechanical Dimension

1.0 FEATURES

- 240pin fully buffered dual in-line memory module (FB-DIMM)
- 3.2Gb/s, 4.0Gb/s, 4.8Gb/s link transfer rate
- 1.8V +/- 0.1V Power Supply for DRAM V_{DD}/V_{DDQ}
- 1.5V +0.075/-0.045V Power Supply for AMB V_{CC}
- 3.3V +/- 0.3V Power Supply for V_{DDSPD}
- Buffer Interface with high-speed differential point-to-point Link at 1.5 volt
- Channel error detection & reporting
- Channel fail over mode support
- Serial presence detect with EEPROM
- 8 Banks
- Posted CAS
- Programmable CAS Latency: 3, 4, 5, 6
- Programmable Additive Latency: 0, 1, 2, 3, 4, 5
- Automatic DDR2 DRAM bus and channel calibration
- MBIST and IBIST Test functions
- Hot add-on and Hot Remove Capability
- Transparent mode for DRAM test support

Table 1 : Ordering Information

Part Number	Density	Organization	Component Composition	Number of Rank	AMB	Type of Heat Spreader	Height
M395T5663CZ4-CD56/E66	2GB	256M x 72	128Mx8(K4T1G084QC) *18EA	2	IDT C1	Full Module	30.35mm
M395T5663CZ4-CD51/E61					IDT A1.5		
M395T5160CZ4-CD56/E66/F76	4GB	512M x 72	256Mx4(K4T1G044QC) *36EA	2	IDT C1		
M395T5160CZ4-CD55/E65					Intel D1		
M395T5160CZ4-CD51/E61					IDT A1.5		

Note :
1. “Z” of Part number(11th digit) stands for Lead-free products.
2. The last digit stands for AMB.

Table 2 : Performance range

	F7(DDR2-800)	E6(DDR2-667)	D5(DDR2-533)	Unit
DDR2 DRAM Speed	800	667	533	Mbps
CL-tRCD-tRP	6-6-6	5-5-5	4-4-4	CK

Table 3 : Address Configuration

Organization	Row Address	Column Address	Bank Address	Auto Precharge
128Mx8(1Gb) based Module	A0-A13	A0-A9	BA0-BA2	A10
256Mx4(1Gb) based Module	A0-A13	A0-A9, A11	BA0-BA2	A10

2.0 FBDIMM GENERALS

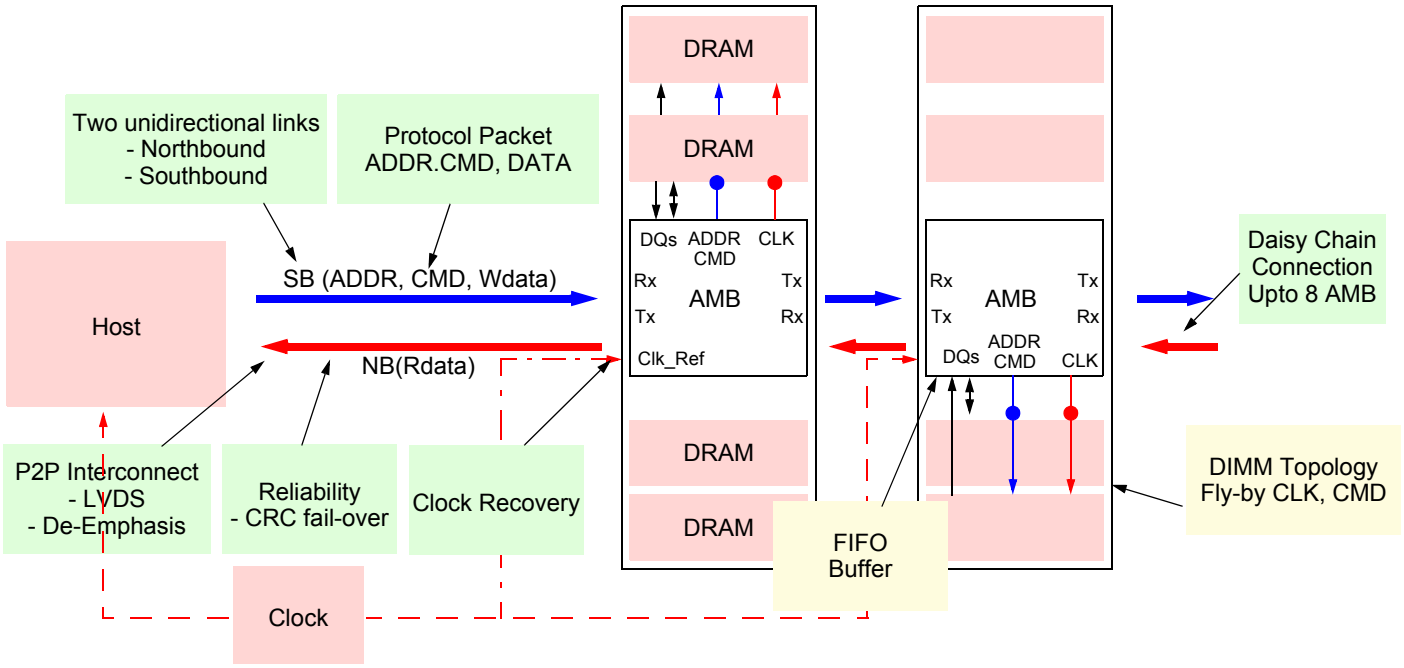
2.1 FB-DIMM Operation Overview

FB-DIMM (Fully Buffered Dual in Line Memory Module) is designed for the applications which require higher data transfer bandwidth and scalable memory capacity. The memory slot access rate per channel decreases as the memory bus speed increases, resulting in limited density build-up as channel speeds increase with memory system having the stub-bus architecture. FB-DIMM solution is intended to eliminate this stub-bus channel bottleneck by using point-to-point links that enable multiple memory modules to be connected serially to a given channel.

Memory system architecture perspective, FB-DIMM is fully differentiated from Registered DIMM and Unbuffered DIMM. A lot of new technologies are integrated into this solution in order to achieve this scalable higher speed memory solution. Serial link interface with packet data format and dedicated read/write paths are key attribute in FB-DIMM protocol. Point to Point interconnect with fully differential signaling and de-emphasis scheme are key attribute in FBD channel link. Clock recovery by using data stream is key attribute in FBD clocking. FB-DIMM supports both clock resync and resampling mode options. CRC (Cyclic Redundancy Check) bits are transferred with data stream for reliability at high speed data transaction. Failover mechanism supports system running with dynamic IO failure. Finally all FB-DIMM is connected in daisy chain manner. Thus, every interconnection between AMB (advanced memory buffer) to AMB, AMB to Host and AMB to DRAM, is point to point interconnection which allows higher data transfer bandwidth.

Figure 1 shows a lot of new technologies integrated with FBD solution.

Figure 1 : FB-DIMM Memory System Overview



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