SG5127FBD225652-SA

March 20, 2007

Ordering Information			
Part Numbers	**Description**	**AMB Vendor**	**Device Vendor**
SG5127FBD225652-SA	512Mx72 (4GB), DDR2, 240-pin Fully Buffered DIMM, ECC, 512Mx4 Based (Stacked - two 256Mx4), PC2-5300, DDR2-667-555, 30.35mm, Green Module (RoHS Compliant). Label: 4GB 2Rx4 PC2-5300F-555-11-D_*	IDT, Rev. A1.5 AMB0480A5RJ	Samsung, Rev. A K4T2G264QA-ZCE6

* This character defines PCB revision.

(All specifications of this module are subject to change without notice.)

Revision History

- **March 20, 2007**
  Datasheet released.

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4GByte (512Mx72) DDR2 SDRAM Module - 512Mx4 Based (Stacked - two 256Mx4) 240-pin Fully Buffered DIMM, ECC

Features:

Device Speed	CL (Device)	Cycle Time	Link Speed
DDR2-667	3.0/4.0/5.0	3.0ns	4.0Gb/s

- High-Speed differential PTP link between Controller & AMB
- SMBus Interface access to AMB Configuration Registers
- AMB allows upto 8 Double-Rank DIMMs/Channel (288 devices) Transparent Mode for DRAM Test
- MEMBIST and IBIST Test Functions
- $V_{DD} = V_{DDQ}$ = 1.8V +/- 0.1V (for DDR2 SDRAM)
- V_{CC} = 1.5V +/- 0.045V (for AMB)
- V_{TT} = 0.9V +/- 0.036V (DRAM Interface Termination)
- V_{DDSPD} = 3.3V +/- 0.3V
- Dual Rank Module (JEDEC Raw Card “D”)
- Lead Finish : Gold

FBD/AMB Specifications:

Fully Buffered DIMM (FBD) provides a high memory bandwidth, large capacity channel solution that has a narrow host interface. Fully Buffered DIMMs use commodity DRAMs isolated from the channel behind a buffer (AMB) on the DIMM. The memory capacity is 288 devices per channel and total memory capacity scales with DRAM bit density. Currently, FBD/AMB specification is broken-out into the following specifications:

1. FBD Design Specification: This specification defines the electrical and mechanical requirements for 240-pin, PC2-4200/PC2-5300/PC2-6400, 72 bit-wide, Fully Buffered Double Data Rate Synchronous DRAM Dual In-Line Memory Modules (DDR2 SDRAM FBDs).

2. FBD Architecture and Protocol Specification: This specification covers Overview, Channel Initialization, Channel Protocol, and Reliability, Availability, and Serviceability (RAS) features of FBDIMM architecture.

3. FBD AMB Specification: The Advanced Memory Buffer allows buffering of memory traffic to support large memory capacities. This specification covers information about various AMB interfaces (Channel/DRAM), Test & Initialization functions, SMBus Interface, Clocking, Registers, etc.

4. FBD High-Speed Differential PTP Link Specification: This specification defines the high-speed differential point-to-point signaling link for FB-DIMM, operating at the buffer supply voltage of 1.5V that is provided at the FBDIMM connector. This specification also applies to FBD host chips which may operate with a different supply voltage. The link consists of a transmitter and a receiver and the interconnect in between them. The transmitter sends serialized bits into a lane and the receiver accepts the electrical signals of the serialized bits and transforms them into a serialized bit-stream.The link utilizes a derived clock approach and transmitter de-emphasis to compensate for channel loss characteristics.

5. FBD SPD Specification: This specification describes the Serial Presence Detect (SPD) values for FBD.

6. FBD DFx Specification: The FB-DIMM DFx spec covers Design for Test (DFT), Design for Manufacturing (DFM) and Design for Validation (DFV) requirements and implementation guidelines for Fully Buffered DIMM technology.

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DDR2 240-Pin FB-DIMM Pin List

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{DD}	31	PN3	61	PN9#	91	PS9#	121	V_{DD}	151	SN3	181	SN9#	211	SS9#
2	V_{DD}	32	PN3#	62	V_{SS}	92	V_{SS}	122	V_{DD}	152	SN3#	182	V_{SS}	212	V_{SS}
3	V_{DD}	33	V_{SS}	63	PN10	93	PS5	123	V_{DD}	153	V_{SS}	183	SN10	213	SS5
4	V_{SS}	34	PN4	64	PN10#	94	PS5#	124	V_{SS}	154	SN4	184	SN10#	214	SS5#
5	V_{DD}	35	PN4#	65	V_{SS}	95	V_{SS}	125	V_{DD}	155	SN4#	185	V_{SS}	215	V_{SS}
6	V_{DD}	36	V_{SS}	66	PN11	96	PS6	126	V_{DD}	156	V_{SS}	186	SN11	216	SS6
7	V_{DD}	37	PN5	67	PN11#	97	PS6#	127	V_{DD}	157	SN5	187	SN11#	217	SS6#
8	V_{SS}	38	PN5#	68	V_{SS}	98	V_{SS}	128	V_{SS}	158	SN5#	188	V_{SS}	218	V_{SS}
9	V_{CC}	39	V_{SS}	69	V_{SS}	99	PS7	129	V_{CC}	159	V_{SS}	189	V_{SS}	219	SS7
10	V_{CC}	40	PN13	70	PS0	100	PS7#	130	V_{CC}	160	SN13	190	SS0	220	SS7#
11	V_{SS}	41	PN13#	71	PS0#	101	V_{SS}	131	V_{SS}	161	SN13#	191	SS0#	221	V_{SS}
12	V_{CC}	42	V_{SS}	72	V_{SS}	102	PS8	132	V_{CC}	162	V_{SS}	192	V_{SS}	222	SS8
13	V_{CC}	43	V_{SS}	73	PS1	103	PS8#	133	V_{CC}	163	V_{SS}	193	SS1	223	SS8#
14	V_{SS}	44	RFU	74	PS1#	104	V_{SS}	134	V_{SS}	164	RFU	194	SS1#	224	V_{SS}
15	V_{TT}	45	RFU	75	V_{SS}	105	RFU	135	V_{TT}	165	RFU	195	V_{SS}	225	RFU
16	VID1	46	V_{SS}	76	PS2	106	RFU	136	VID0	166	V_{SS}	196	SS2	226	RFU
17	RESET#	47	V_{SS}	77	PS2#	107	V_{SS}	137	DNU/M_Test	167	V_{SS}	197	SS2#	227	V_{SS}
18	V_{SS}	48	PN12	78	V_{SS}	108	V_{DD}	138	V_{SS}	168	SN12	198	V_{SS}	228	SCK
19	RFU	49	PN12#	79	PS3	109	V_{DD}	139	RFU	169	SN12#	199	SS3	229	SCK#
20	RFU	50	V_{SS}	80	PS3#	110	V_{SS}	140	RFU	170	V_{SS}	200	SS3#	230	V_{SS}
21	V_{SS}	51	PN6	81	V_{SS}	111	V_{DD}	141	V_{SS}	171	SN6	201	V_{SS}	231	V_{DD}
22	PN0	52	PN6#	82	PS4	112	V_{DD}	142	SN0	172	SN6#	202	SS4	232	V_{DD}
23	PN0#	53	V_{SS}	83	PS4#	113	V_{DD}	143	SN0#	173	V_{SS}	203	SS4#	233	V_{DD}
24	V_{SS}	54	PN7	84	V_{SS}	114	V_{SS}	144	V_{SS}	174	SN7	204	V_{SS}	234	V_{SS}
25	PN1	55	PN7#	85	V_{SS}	115	V_{DD}	145	SN1	175	SN7#	205	V_{SS}	235	V_{DD}
26	PN1#	56	V_{SS}	86	RFU	116	V_{DD}	146	SN1#	176	V_{SS}	206	RFU	236	V_{DD}
27	V_{SS}	57	PN8	87	RFU	117	V_{TT}	147	V_{SS}	177	SN8	207	RFU	237	V_{TT}
28	PN2	58	PN8#	88	V_{SS}	118	SA2	148	SN2	178	SN8#	208	V_{SS}	238	V_{DDSPD}
29	PN2#	59	V_{SS}	89	V_{SS}	119	SDA	149	SN2#	179	V_{SS}	209	V_{SS}	239	SA0
30	V_{SS}	60	PN9	90	PS9	120	SCL	150	V_{SS}	180	SN9	210	SS9	240	SA1

Pin Description:

DIMM Connector Pin Description

Symbol	Type	Polarity	Function
SCK	Input	Positive Edge	Positive line of the differential pair of system clock inputs.
SCK#	Input	Negative Edge	Negative line of the differential pair of system clock inputs.
PN0 ~ PN13	Output	Positive Edge	Primary Northbound Data, positive lines.
PN0# ~ PN13#	Output	Negative Edge	Primary Northbound Data, negative lines.
PS0 ~ PS9	Input	Positive Edge	Primary Southbound Data, positive lines.
PS0# ~ PS9#	Input	Negative Edge	Primary Southbound Data, negative lines.
SN0 ~ SN13	Input	Positive Edge	Secondary Northbound Data, positive lines.
SN0# ~ SN13#	Input	Negative Edge	Secondary Northbound Data, negative lines.
SS0 ~ SS9	Output	Positive Edge	Secondary Southbound Data, positive lines.
SS0# ~ SS9#	Output	Negative Edge	Secondary Southbound Data, negative lines.
SCL	Input/Output	-	Serial Presence Detect (SPD) for Clock Input.
SDA	Input/Output	-	SPD Data Input/Output.
SA0 ~ SA2	Input	-	SPD Address Inputs, also used to select the DIMM number in the AMB.
VID0 ~ VID1	Supply	-	Voltage ID: These pins must be unconnected for DDR2-based Fully Buffered DIMMs. VID0 is V_{DD} value: OPEN = 1.8V, GND = 1.5V; VID1 is V_{CC} value: OPEN = 1.5V, GND = 1.2V;
V_{CC}	Supply	-	AMB Core Power and AMB Channel Interface Power(1.5 Volt).
V_{DD}	Supply	-	DRAM Power and AMB DRAM I/O Power(1.8 Volt).
V_{SS}	Supply	-	Ground.
V_{TT}	Supply	-	DRAM Address/Command/Clock termination Power (V_{DD}/2).
V_{DDSPD}	Supply	-	SPD Power (3.3 Volt).
RESET#	Input	Active Low	Advanced Memory Buffer (AMB) reset signal.
RFU	-	-	Reserved for Future Use.
DNU/M_Test	-	-	The DNU/M_Test pin provides an external connection for testing the margin of V_{REF} which is produced by a voltage divider on the module. It is not intended to be used in normal system operation and must not be connected (DNU) in a system.

Note: System Clock Signals (SCK & SCK#) switch at one-half the DRAM CK/CK# frequency.

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