

**4.20.11 - 200-Pin DDR2 SDRAM Unbuffered SO-DIMM Design  
Specification**

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**PC2-6400/PC2-5300/PC2-4200/PC2-3200  
DDR2 Unbuffered SO-DIMM**

**Reference Design Specification**

**Revision 2.5**

**July, 2008**

Netlist Inc.

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## 1. Product Description

This reference specification defines the electrical and mechanical requirements for the PC2-6400 memory module, a 200-pin, 400MHz clock (800 MT/s data rate), 64-bit wide, Unbuffered Synchronous Double Data Rate 2 (DDR2) DRAM Small Outline Dual In-Line Memory Module (DDR2 SDRAM SO-DIMMs). It also defines slower versions, the PC2-5300, PC2-4200 and PC2-3200 with a 333MHz 267MHz and 200MHz clock (667 MT/s, 533 MT/s and 400 MT/s data rate) DDR2 SDRAMs. These DDR2 SDRAM SO-DIMMs are intended for use as main memory when installed in systems such as mobile personal computers.

Reference design examples are included which provide an initial basis for Unbuffered SO-DIMM designs. Any modifications to these reference designs must meet all system timing, signal integrity and thermal requirements for 333MHz clock rate support. Other designs are acceptable, and all Unbuffered DDR2 SO-DIMM implementations must use simulations and lab verification to ensure proper timing requirements and signal integrity in the design.

### Product Family Attributes

| Attribute:               | Values:  | Notes: |
|--------------------------|--|--------|
| SO-DIMM Organization     | x 64   |        |
| Dimensions (nominal)     | 30.0 mm high, 67.60 mm wide / MO-224 variation CB<br>25.4 mm high, 67.60 mm wide / MO-224 variation AB |        |
| SO-DIMM Types Supported  | Unbuffered   |        |
| Pin Count                | 200  |        |
| SDRAMs Supported         | 256 Mb, 512 Mb, 1 Gb, 2 Gb, 4 Gb   |        |
| Capacity                 | 128 MB, 256 MB, 512 MB, 1 GB, 2GB, 4 GB, 8 GB  |        |
| Serial Presence Detect   | Consistent with JEDEC latest Rev.  |        |
| Voltage Options, Nominal | 1.8 V $V_{DD}$<br>1.8 V $V_{DDQ}$<br>1.8 V to 3.3 V $V_{DDSPD}$  | 1, 2   |
| Interface                | SSTL_18  |        |

Note 1:  $V_{DDSPD}$  is not tied to  $V_{DD}$  or  $V_{DDQ}$  on the DDR2 SO-DIMM.

Note 2: SO-DIMMs that include an optional temperature sensor may require a restricted VDDSPD operating voltage range for proper operation of the temperature sensor. Refer to the thermal sensor specification for details regarding the supported voltage range. All other functions of the SO-DIMM SPD are supported across the full VDDSPD range.

## Raw Card Summary

| Raw Card | Number of DDR2 SDRAMs | SDRAM Organization | Number of Ranks | Comments  |
|----------|-----------------------|--------------------|-----------------|---|
| A, G     | 8                     | x16                | 2               | G is low profile version(maximum DRAM size, W x L) 11.0 mm x 13.0mm |
| B        | 8                     | x8                 | 1               |   |
| C, H     | 4                     | x16                | 1               | H is low profile version(maximum DRAM size, W x L) 11.0 mm x 13.0mm |
| D        | 16                    | x8                 | 2               | Uses stacked memory   |
| E        | 16                    | x8                 | 2               | Planar (maximum DRAM size, W x L) 12.0 mm x 11.5 mm                 |
| F        | 16                    | x8                 | 2               | Planar (maximum DRAM size, W x L) 11.0 mm x 13.65 mm                |

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