DDR2 SDRAM RDIMM

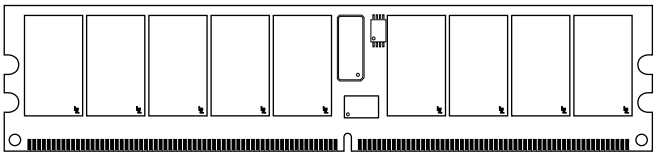
MT9HTF3272Y – 256MB
MT9HTF6472PY – 512MB
MT9HTF12872PY – 1GB

Features

- 240-pin, registered dual in-line memory module
- Fast data transfer rates: PC2-3200, PC2-4200, PC2-5300, or PC2-6400
- 256MB (32 Meg x 72), 512MB (64 Meg x 72), or 1GB (128 Meg x 72)
- Supports ECC error detection and correction
- $V_{DD} = V_{DDQ} = 1.8V$
- $V_{DDSPD} = 1.7–3.6V$
- JEDEC-standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- 4*n*-bit prefetch architecture
- Multiple internal device banks for concurrent operation
- Programmable CAS# latency (CL)
- Posted CAS# additive latency (AL)
- WRITE latency = READ latency - 1 ^{t}CK
- Programmable burst lengths (BL): 4 or 8
- Adjustable data-output drive strength
- 64ms, 8192-cycle refresh
- On-die termination (ODT)
- Serial presence-detect (SPD) with EEPROM
- Single rank
- Gold edge contacts

Figure 1: 240-Pin RDIMM (MO-237 R/C A, Nonparity; R/C F, Parity)

Module height: 30mm (1.18in)



Options	Marking
• Parity	P
• Operating temperature	
– Commercial (0°C ≤ T_A ≤ +70°C)	None
– Industrial (–40°C ≤ T_A ≤ +85°C)[1]	I
• Package	
– 240-pin DIMM (lead-free)	Y
• Frequency/CL[2]	
– 2.5ns @ CL = 5 (DDR2-800)[3]	-80E
– 2.5ns @ CL = 6 (DDR2-800)[3]	-800
– 3.0ns @ CL = 5 (DDR2-667)	-667
– 3.75ns @ CL = 4 (DDR2-533)	-53E
– 5.0ns @ CL = 3 (DDR2-400)	-40E

Notes:
1. Contact Micron for industrial temperature module offerings.
2. CL = CAS (READ) latency; registered mode will add one clock cycle to CL.
3. Not available in 256MB module density.

Table 1: Key Timing Parameters

Speed Grade	Industry Nomenclature	Data Rate (MT/s)				^{t}RCD (ns)	^{t}RP (ns)	^{t}RC (ns)
		CL = 6	CL = 5	CL = 4	CL = 3			
-80E	PC2-6400	800	800	533	400	12.5	12.5	55
-800	PC2-6400	800	667	533	400	15	15	55
-667	PC2-5300	–	667	553	400	15	15	55
-53E	PC2-4200	–	–	553	400	15	15	55
-40E	PC2-3200	–	–	400	400	15	15	55

Table 2: Addressing

Parameter	256MB	512MB	1GB
Refresh count	8K	8K	8K
Row address	8K A[12:0]	16K A[13:0]	16K A[13:0]
Device bank address	4 BA[1:0]	4 BA[1:0]	8 BA[2:0]
Device configuration	256Mb (32 Meg x 8)	512Mb (64 Meg x 8)	1Gb (128 Meg x 8)
Column address	1K A[9:0]	1K A[9:0]	1K A[9:0]
Module rank address	S0#	S0#	S0#

Table 3: Part Numbers and Timing Parameters – 256MB

Base device: MT47H32M8,[1] 256Mb DDR2 SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-^{t}RCD-^{t}RP)
MT9HTF3272(I)Y-667__	256MB	32 Meg x 72	5.3 GB/s	3.0ns/667 MT/s	5-5-5
MT9HTF3272(I)Y-53E__	256MB	32 Meg x 72	4.3 GB/s	3.75ns/533 MT/s	4-4-4
MT9HTF3272(I)Y-40E__	256MB	32 Meg x 72	3.2 GB/s	5.0ns/400 MT/s	3-3-3

Table 4: Part Numbers and Timing Parameters – 512MB

Base device: MT47H64M8,[1] 512Mb DDR2 SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-^{t}RCD-^{t}RP)
MT9HTF6472P(I)Y-80E__	512MB	64 Meg x 72	6.2 GB/s	2.5ns/800 MT/s	5-5-5
MT9HTF6472P(I)Y-800__	512MB	64 Meg x 72	6.2 GB/s	2.5ns/800 MT/s	6-6-6
MT9HTF6472P(I)Y-667__	512MB	64 Meg x 72	5.3 GB/s	3.0ns/667 MT/s	5-5-5
MT9HTF6472P(I)Y-53E__	512MB	64 Meg x 72	4.3 GB/s	3.75ns/533 MT/s	4-4-4
MT9HTF6472P(I)Y-40E__	512MB	64 Meg x 72	3.2 GB/s	5.0ns/400 MT/s	3-3-3

Table 5: Part Numbers and Timing Parameters – 1GB

Base device: MT47H128M8,[1] 1Gb DDR2 SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-^{t}RCD-^{t}RP)
MT9HTF12872P(I)Y-80E__	1GB	128 Meg x 72	6.2 GB/s	2.5ns/800 MT/s	5-5-5
MT9HTF12872P(I)Y-800__	1GB	128 Meg x 72	6.2 GB/s	2.5ns/800 MT/s	6-6-6
MT9HTF12872P(I)Y-667__	1GB	128 Meg x 72	5.3 GB/s	3.0ns/667 MT/s	5-5-5
MT9HTF12872P(I)Y-53E__	1GB	128 Meg x 72	4.3 GB/s	3.75ns/533 MT/s	4-4-4
MT9HTF12872P(I)Y-40E__	1GB	128 Meg x 72	3.2 GB/s	5.0ns/400 MT/s	3-3-3

Notes:
1. Data sheets for the base device can be found on Micron's Web site.
2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes. Example: MT9HTF6472Y-667D2.

Pin Assignments

Table 6: Pin Assignments

240-Pin RDIMM Front								240-Pin RDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{REF}	31	DQ19	61	A4	91	V_{SS}	121	V_{SS}	151	V_{SS}	181	V_{DDQ}	211	DM5/ DQS14
2	V_{SS}	32	V_{SS}	62	V_{DDQ}	92	DQS5#	122	DQ4	152	DQ28	182	A3	212	NC/ DQS14#
3	DQ0	33	DQ24	63	A2	93	DQS5	123	DQ5	153	DQ29	183	A1	213	V_{SS}
4	DQ1	34	DQ25	64	V_{DD}	94	V_{SS}	124	V_{SS}	154	V_{SS}	184	V_{DD}	214	DQ46
5	V_{SS}	35	V_{SS}	65	V_{SS}	95	DQ42	125	DM0/ DQS9	155	DM3/ DQS12	185	CK0	215	DQ47
6	DQS0#	36	DQS3#	66	V_{SS}	96	DQ43	126	NC/ DQS9#	156	NC/ DQS12#	186	CK0#	216	V_{SS}
7	DQS0	37	DQS3	67	V_{DD}	97	V_{SS}	127	V_{SS}	157	V_{SS}	187	V_{DD}	217	DQ52
8	V_{SS}	38	V_{SS}	68	NC/ Par_In[2]	98	DQ48	128	DQ6	158	DQ30	188	A0	218	DQ53
9	DQ2	39	DQ26	69	V_{DD}	99	DQ49	129	DQ7	159	DQ31	189	V_{DD}	219	V_{SS}
10	DQ3	40	DQ27	70	A10	100	V_{SS}	130	V_{SS}	160	V_{SS}	190	BA1	220	RFU
11	V_{SS}	41	V_{SS}	71	BA0	101	SA2	131	DQ12	161	CB4	191	V_{DDQ}	221	RFU
12	DQ8	42	CB0	72	V_{DDQ}	102	NC	132	DQ13	162	CB5	192	RAS#	222	V_{SS}
13	DQ9	43	CB1	73	WE#	103	V_{SS}	133	V_{SS}	163	V_{SS}	193	S0#	223	DM6/ DQS15
14	V_{SS}	44	V_{SS}	74	CAS#	104	DQS6#	134	DM1/ DQS10	164	DM8/ DQS17	194	V_{DDQ}	224	NC/ DQS15#
15	DQS1#	45	DQS8#	75	V_{DDQ}	105	DQS6	135	NC/ DQS10#	165	NC/ DQS17#	195	ODT0	225	V_{SS}
16	DQS1	46	DQS8	76	S1#	106	V_{SS}	136	V_{SS}	166	V_{SS}	196	NC/A13[3]	226	DQ54
17	V_{SS}	47	V_{SS}	77	ODT1	107	DQ50	137	RFU	167	CB6	197	V_{DD}	227	DQ55
18	RESET#	48	CB2	78	V_{DDQ}	108	DQ51	138	RFU	168	CB7	198	V_{SS}	228	V_{SS}
19	NC	49	CB3	79	V_{SS}	109	V_{SS}	139	V_{SS}	169	V_{SS}	199	DQ36	229	DQ60
20	V_{SS}	50	V_{SS}	80	DQ32	110	DQ56	140	DQ14	170	V_{DDQ}	200	DQ37	230	DQ61
21	DQ10	51	V_{DDQ}	81	DQ33	111	DQ57	141	DQ15	171	CKE1	201	V_{SS}	231	V_{SS}
22	DQ11	52	CKE0	82	V_{SS}	112	V_{SS}	142	V_{SS}	172	V_{DD}	202	DM4/ DQS13	232	DM7/ DQS16
23	V_{SS}	53	V_{DD}	83	DQS4#	113	DQS7#	143	DQ20	173	NC/A15[4]	203	NC/ DQS13#	233	NC/ DQS16#
24	DQ16	54	NC/BA2	84	DQS4	114	DQS7	144	DQ21	174	NC/A14[4]	204	V_{SS}	234	V_{SS}
25	DQ17	55	NC/[1] Err_Out#	85	V_{SS}	115	V_{SS}	145	V_{SS}	175	V_{DDQ}	205	DQ38	235	DQ62
26	V_{SS}	56	V_{DDQ}	86	DQ34	116	DQ58	146	DM2/ DQS11	176	A12	206	DQ39	236	DQ63
27	DQS2#	57	A11	87	DQ35	117	DQ59	147	NC/ DQS11#	177	A9	207	V_{SS}	237	V_{SS}
28	DQS2	58	A7	88	V_{SS}	118	V_{SS}	148	V_{SS}	178	V_{DD}	208	DQ44	238	V_{DDSPD}

Table 6: Pin Assignments (Continued)

240-Pin RDIMM Front								240-Pin RDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
29	V_{SS}	59	V_{DD}	89	DQ40	119	SDA	149	DQ22	179	A8	209	DQ45	239	SA0
30	DQ18	60	A5	90	DQ41	120	SCL	150	DQ23	180	A6	210	V_{SS}	240	SA1

Notes:
1. Pin 55 is NC for nonparity and Err_Out# for parity.
2. Pin 68 is NC for nonparity and Par_In for parity.
3. Pin 196 is NC for 256MB or A13 for 512MB, 1GB, and parity.
4. Pin 173 and 174 are NC or A15 and A14 for parity.

Pin Descriptions

The pin description table below is a comprehensive list of all possible pins for all DDR2 modules. All pins listed may not be supported on this module. See Pin Assignments for information specific to this module.

Table 7: Pin Descriptions

Symbol	Type	Description
Ax	Input	**Address inputs:** Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BAx) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. See the Pin Assignments Table for density-specific addressing information.
BAx	Input	**Bank address inputs:** Define the device bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA define which mode register (MR0, MR1, MR2, and MR3) is loaded during the LOAD MODE command.
CKx, CK#x	Input	**Clock:** Differential clock inputs. All control, command, and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#.
CKEx	Input	**Clock enable:** Enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DDR2 SDRAM.
DMx,	Input	**Data mask (x8 devices only):** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with that input data, during a write access. Although DM pins are input-only, DM loading is designed to match that of the DQ and DQS pins.
ODTx	Input	**On-die termination:** Enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR2 SDRAM. When enabled in normal operation, ODT is only applied to the following pins: DQ, DQS, DQS#, DM, and CB. The ODT input will be ignored if disabled via the LOAD MODE command.
Par_In	Input	**Parity input:** Parity bit for Ax, RAS#, CAS#, and WE#.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with S#) define the command being entered.
RESET#	Input	**Reset:** Asynchronously forces all registered outputs LOW when RESET# is LOW. This signal can be used during power-up to ensure that CKE is LOW and DQ are High-Z.
S#x	Input	**Chip select:** Enables (registered LOW) and disables (registered HIGH) the command decoder.
SAx	Input	**Serial address inputs:** Used to configure the SPD EEPROM address range on the I^2C bus.
SCL	Input	**Serial clock for SPD EEPROM:** Used to synchronize communication to and from the SPD EEPROM on the I^2C bus.
CBx	I/O	**Check bits.** Used for system error detection and correction.
DQx	I/O	**Data input/output:** Bidirectional data bus.
DQSx, DQS#x	I/O	**Data strobe:** Travels with the DQ and is used to capture DQ at the DRAM or the controller. Output with read data; input with write data for source synchronous operation. DQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.

DOCKET ALARM

Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

Real-Time Litigation Alerts

Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

Advanced Docket Research

With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

Analytics At Your Fingertips

Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

LAW FIRMS
Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

FINANCIAL INSTITUTIONS
Litigation and bankruptcy checks for companies and debtors.

E-DISCOVERY AND LEGAL VENDORS
Sync your system to PACER to automate legal marketing.