NVDIMM Hands on Lab

Presented by:
AgigA Tech, Netlist, SMART

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SNIA

Hands-On Lab Acknowledgements

Participating Companies:

AGIGA TECH
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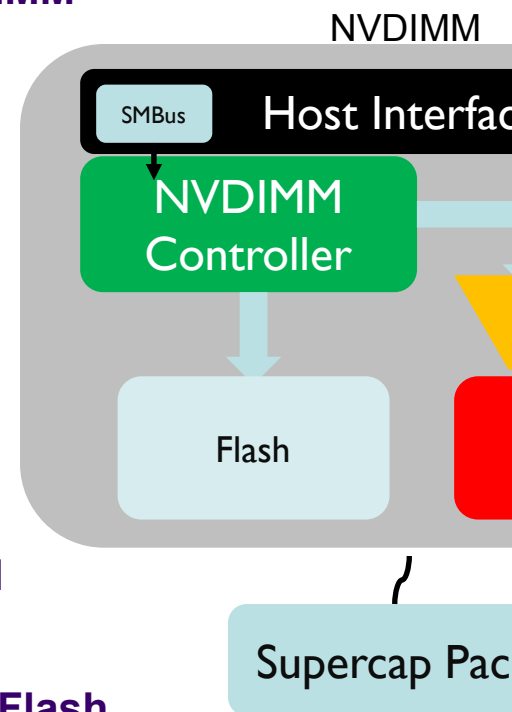
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Agenda

◆ **Part I**

  ◆ NVDIMMs – Overview of how they work

◆ **Part II**

  ◆ NVDIMM Demonstration

◆ **Part III**

  ◆ Ultracapacitors – Overview of how they work
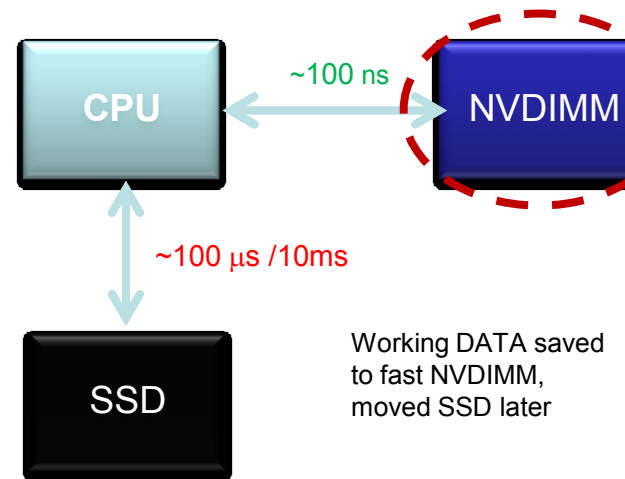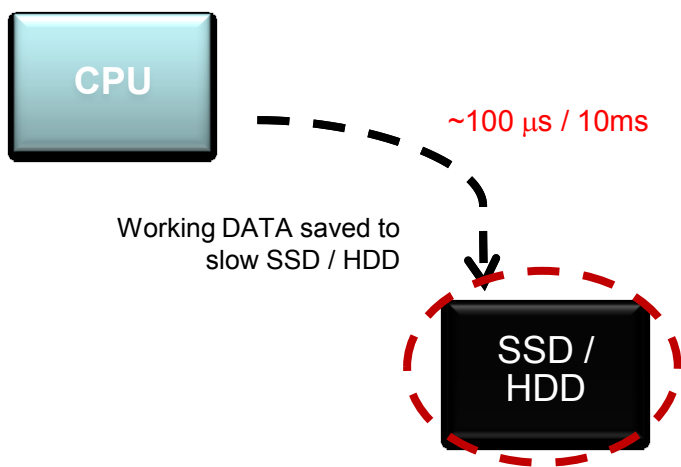
◆ **Part IV**

  ◆ Ultracapacitor Demonstration

NVDIMM – How it Works

- **NVDIMM combines DRAM and Flash onto a single DIMM**
- **Operates as standard DRAM RDIMM**
  - *Fast, low latency performance.*
- **Host only addresses the DRAM and has no direct access to the flash (NVDIMM-N classification)**
- **NVDIMM contains switches to switch control back and forth between host and NVDIMM controller**
- **NVDIMM controller moves data from DRAM to flash upon power loss or other trigger; can back up portions or all of DRAM upon command**
- **If power fails, Supercaps (or other power source) provide back up power while DRAM is backed up to Flash**
- **MRC (Memory Reference Code) configures NVDIMM controller to move data b Flash to DRAM when recovery is needed**

NVDIMM

SMBus

Host Interfac

NVDIMM Controller

Flash

Supercap Pac

NVDIMM Application Scenario

CPU

~100 μs / 10ms

Working DATA saved to
slow SSD / HDD

SSD /
HDD

CPU

~100 ns

NVDIMM

~100 μs /10ms

SSD

Working DATA saved
to fast NVDIMM,
moved SSD later

SSD/HDD has low throughput	> 10X higher throughput for persistent data
Software Overhead slows effective performance	No software overhead. Runs at HW speeds

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