IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

NETLIST, INC.,	§	
	§	
Plaintiff,	§	
	§	
v.	§	
	§	CIVIL ACTION NO. 2:21-CV-00463-JRG
SAMSUNG ELECTRONICS CO., LTD.,	§	
SAMSUNG ELECTRONICS AMERICA,	§	
INC., and SAMSUNG SEMICONDUCTOR,	§	
INC.,	§	
	§	
Defendants.	§	

CLAIM CONSTRUCTION ORDER

Netlist asserts claims from six patents relating to computer memory against Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., and Samsung Semiconductor, Inc. (together, "Samsung"). U.S. Patent 10,949,339, entitled "Memory Module with Controlled Byte-Wise Buffers," relates to improving the performance and memory capacity of memory subsystems. '339 Patent at 1:18–23. U.S. Patent 10,860,506, entitled "Memory Module With Timing-Controlled Data Buffering," generally concerns "multi-rank memory modules and methods of operation." '506 Patent at 1:37–39. U.S. Patents 11,016,918 and 11,232,054, which are related and share a common specification, concern computer memory devices that use different types of memory. '918 Patent at 1:66–2:2; *see also* '054 Patent at 1:66–2:2. Finally, U.S. Patents 8,787,060 and 9,318,160, which are related and share a common specification, concern "systems and methods for reducing the load of drivers of memory packages included on memory modules." '060 Patent at 1:19–21; *see also* '160 Patent at 1:21–23.

The parties dispute the proper constructions of fourteen terms from the patents. Having considered the parties' briefing, along with arguments of counsel during the November 4, 2022 *Markman* Hearing, the Court resolves the disputes as follows.

I.   LEGAL STANDARDS

A.   Generally

"'[T]he claims of a patent define the invention to which the patentee is entitled the right to exclude.'" *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (quoting *Innova/Pure-Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1115 (Fed. Cir. 2004)). As such, if the parties dispute the scope of the claims, the court must determine their meaning. *See, e.g., Verizon Servs. Corp. v. Vonage Holdings Corp.*, 503 F.3d 1295, 1317 (Fed. Cir. 2007); *see also Markman v. Westview Instruments, Inc.*, 517 U.S. 370, 390 (1996), *aff'g*, 52 F.3d 967, 976 (Fed. Cir. 1995) (en banc).

Claim construction, however, "is not an obligatory exercise in redundancy." *U.S. Surgical Corp. v. Ethicon, Inc.*, 103 F.3d 1554, 1568 (Fed. Cir. 1997). Rather, "[c]laim construction is a matter of [resolving] disputed meanings and technical scope, to clarify and when necessary to explain what the patentee covered by the claims . . . ." *Id.* A court need not "repeat or restate every claim term in order to comply with the ruling that claim construction is for the court." *Id.*

When construing claims, "[t]here is a heavy presumption that claim terms are to be given their ordinary and customary meaning." *Aventis Pharm. Inc. v. Amino Chems. Ltd.*, 715 F.3d 1363, 1373 (Fed. Cir. 2013) (citing *Phillips*, 415 F.3d at 1312–13). Courts must therefore "look to the words of the claims themselves . . . to define the scope of the patented invention." *Id.* (citations omitted). "[T]he ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as

of the effective filing date of the patent application." *Phillips*, 415 F.3d at 1313. This "person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification." *Id.*

Intrinsic evidence is the primary resource for claim construction. *See Power-One, Inc. v. Artesyn Techs., Inc.*, 599 F.3d 1343, 1348 (Fed. Cir. 2010) (citing *Phillips*, 415 F.3d at 1312). For certain claim terms, "the ordinary meaning of claim language as understood by a person of skill in the art may be readily apparent even to lay judges, and claim construction in such cases involves little more than the application of the widely accepted meaning of commonly understood words." *Phillips*, 415 F.3d at 1314; *see also Medrad, Inc. v. MRI Devices Corp.*, 401 F.3d 1313, 1319 (Fed. Cir. 2005) ("We cannot look at the ordinary meaning of the term . . . in a vacuum. Rather, we must look at the ordinary meaning in the context of the written description and the prosecution history."). But for claim terms with less-apparent meanings, courts consider "'those sources available to the public that show what a person of skill in the art would have understood disputed claim language to mean[,] [including] the words of the claims themselves, the remainder of the specification, the prosecution history, and extrinsic evidence concerning relevant scientific principles, the meaning of technical terms, and the state of the art.'" *Phillips*, 415 F.3d at 1314 (quoting *Innova*, 381 F.3d at 1116).

II.   THE LEVEL OF ORDINARY SKILL IN THE ART

The level of ordinary skill in the art is the skill level of a hypothetical person who is presumed to have known the relevant art at the time of the invention. *In re GPAC*, 57 F.3d 1573, 1579 (Fed. Cir. 1995). In resolving the appropriate level of ordinary skill, courts consider the types of and solutions to problems encountered in the art, the speed of innovation, the sophistication of the

technology, and the education of workers active in the field. *Id.* Importantly, "[a] person of ordinary skill in the art is also a person of ordinary creativity, not an automaton." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 421 (2007).

Here, neither party proffers a level of ordinary skill in the art in its briefing. Elsewhere, however, Samsung asserted:

> [a] POSITA in the field of the 054 Patent in 2008 would have had an advanced degree in electrical or computer engineering, or a related field, and two years working or studying in the field of design or development of memory systems, or a bachelor's degree in such engineering disciplines and at least three years working in the field. . . . Such a hypothetical person would have been familiar with the JEDEC industry standards, and knowledgeable about the design and operation of standardized DRAM and SDRAM memory devices and memory modules and how they interacted with a memory controller and other parts of a computer system, including standard communication busses and protocols, such as PCI and SMBus busses and protocols. Such a hypothetical person would also have been familiar with the structure and operation of circuitry used to access and control computer memories, including sophisticated circuits such as ASICs, FPGAs, and CPLDs, and more low-level circuits such as tri-state buffers. Such a hypothetical person would further have been familiar with voltage supply requirements of such structures (e.g., memory modules, memory devices, memory controller, and associated access and control circuitry), including voltage conversion and voltage regulation circuitry.

Pet. for *Inter Partes* Review of U.S. Patent No. 11,232,054, Dkt. No. 82-1 at 7–8. *See also* Pet. for *Inter Partes* Review of U.S. Patent No. 11,016,918, Dkt. No. 87-2 at 8–9; Pet. for *Inter Partes* Review of U.S. Patent No. 9,318,160, Dkt. No. 87-3 at 5 (similar); Pet. for *Inter Partes* Review of U.S. Patent No. 10,949,339, Dkt. No. 87-3 at 5 (similar).

III.   U.S. PATENT 10,949,339

A.   Background

According to the '339 Patent, designing memory subsystems requires balancing memory density, power dissipation, speed, and cost. '339 Patent at 2:5–7. Adjusting one of these may

negatively affect the others. *Id.* at 2:7–12. For example, the '339 Patent notes two ways of increas-

ing memory space: (1) an address decoding scheme, and (2) combining chip-select and address

signals "to increase the number of physically addressable memory spaces . . . ." *Id.* at 5: 15–25.

But because both ways add memory chips, the system outputs have a heavier load. That, in turn,

slows the system and increases the necessary power. *Id.* at 4:27–33. Moreover, it results in uneven

propagation delay, which can negatively affect internal timing of accessing memory. *Id.* at 4:38–

44. As examples, FIGS. 1–2 show prior-art systems in which differences in trace lengths or com-

plexity of the memory controllers affect system speed.

       As shown in FIG. 3A (below), the '339 Patent teaches arranging the memory devices 412

in multiple ranks A, B, C, D, and a module controller 430 configured to receive and register input

control signals from a memory controller 420. The address and control signals select one of the

multiple ranks to perform a read or write operation. In response, the module controller 430 outputs

a set of control signals that drive data signals between the memory controller 420 and the selected

rank. *See generally id.* fig.3A.
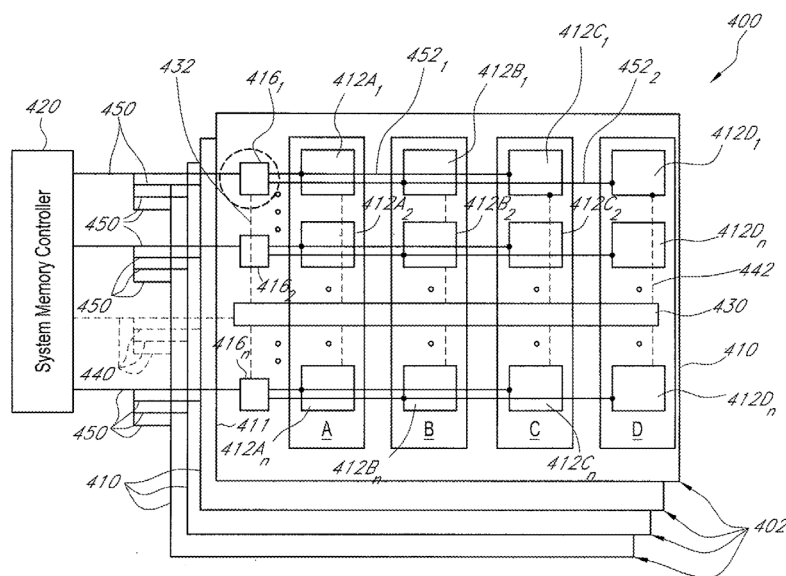
FIG. 3A

DOCKET ALARM

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