UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APPLE INC.
Petitioner

v.

TELEFONAKTIEBOLAGET LM ERICSSON,
Patent Owner

Case No. IPR2022-00716
U.S. Patent No. 9,705,400

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 9,705,400

TABLE OF CONTENTS

I. INTRODUCTION 1

II. SUMMARY OF THE '400 PATENT 1

A. THE '400 PATENT'S ALLEGED INVENTION 1
B. THE '400 PATENT'S PROSECUTION 6
C. A PERSON HAVING ORDINARY SKILL IN THE ART 8

III. REQUIREMENTS FOR IPR UNDER 37 C.F.R. § 42.104 8

A. STANDING UNDER 37 C.F.R. § 42.104(A) 8
B. CHALLENGE UNDER 37 C.F.R. § 42.104(B) AND RELIEF REQUESTED 9
C. CLAIM CONSTRUCTION UNDER 37 C.F.R. § 42.104(B)(3) 9

IV. DISCRETIONARY CONSIDERATIONS 10

A. THE *FINTIV* FACTORS FAVOR INSTITUTION 10

V. THE CHALLENGED CLAIMS ARE UNPATENTABLE 13

A. GROUND 1: CLAIMS 1, 2, 8, AND 10 ARE OBVIOUS UNDER AIA 35 U.S.C. § 103 OVER *SMITH* 13
i. Claim 1. 16
ii. Claim 2. 32
iii. Claim 8. 35
iv. Claim 10. 53
B. GROUND 2: CLAIM 14 IS OBVIOUS UNDER AIA 35 U.S.C. § 103 OVER *SMITH IN VIEW OF STENGEL* 55
i. Claim 14. 59

VI. CONCLUSION 81

VII. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8(A)(1) 82

A. REAL PARTY-IN-INTEREST 82
B. RELATED MATTERS 82
C. LEAD AND BACK-UP COUNSEL 82

I. INTRODUCTION

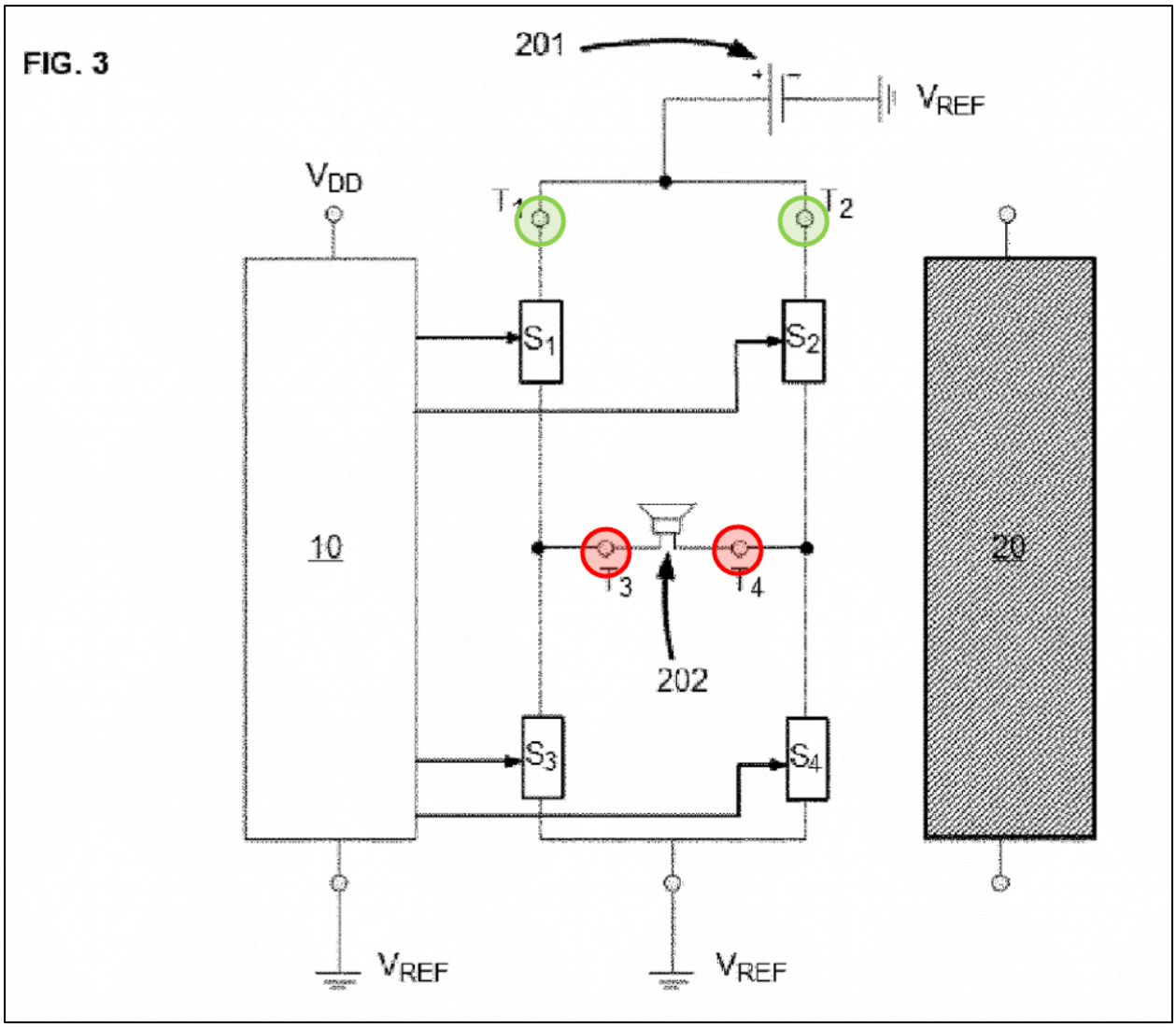
Petitioner Apple Inc. ("Petitioner") requests an *Inter Partes* Review ("IPR") of claims 1, 2, 8, 10, and 14 (the "Challenged Claims") of U.S. Patent No. 9,705,400 ("the '400 Patent").

II. SUMMARY OF THE '400 PATENT

A. The '400 Patent's Alleged Invention

The '400 Patent generally describes a circuit structure that includes an output stage that can be adapted to work with at least two subsystem circuit components, such as a Class-D amplifier and a DC-DC boost converter. *'400 Patent* (Ex. 1001), 1:44-56. As described in the '400 Patent, these disclosed circuit configurations purport to solve the problem of wasted circuit die area. *See id.* at 5:61-6:8. Instead of a control stage and an output stage dedicated for use with either a Class-D amplifier or a DC-DC boost converter, the circuit described in the '400 Patent can "operate in at least a first operating state and a second operating state, such that the output stage may be shared by at least two circuit components such as the Class-D amplifier and the DC-DC boost converter." *See id.* Because the output stage may be shared by at least two circuit components, the proposed control stage would "always be in [sic] used in all associated audio configurations." *Id.* at 6:1-8.

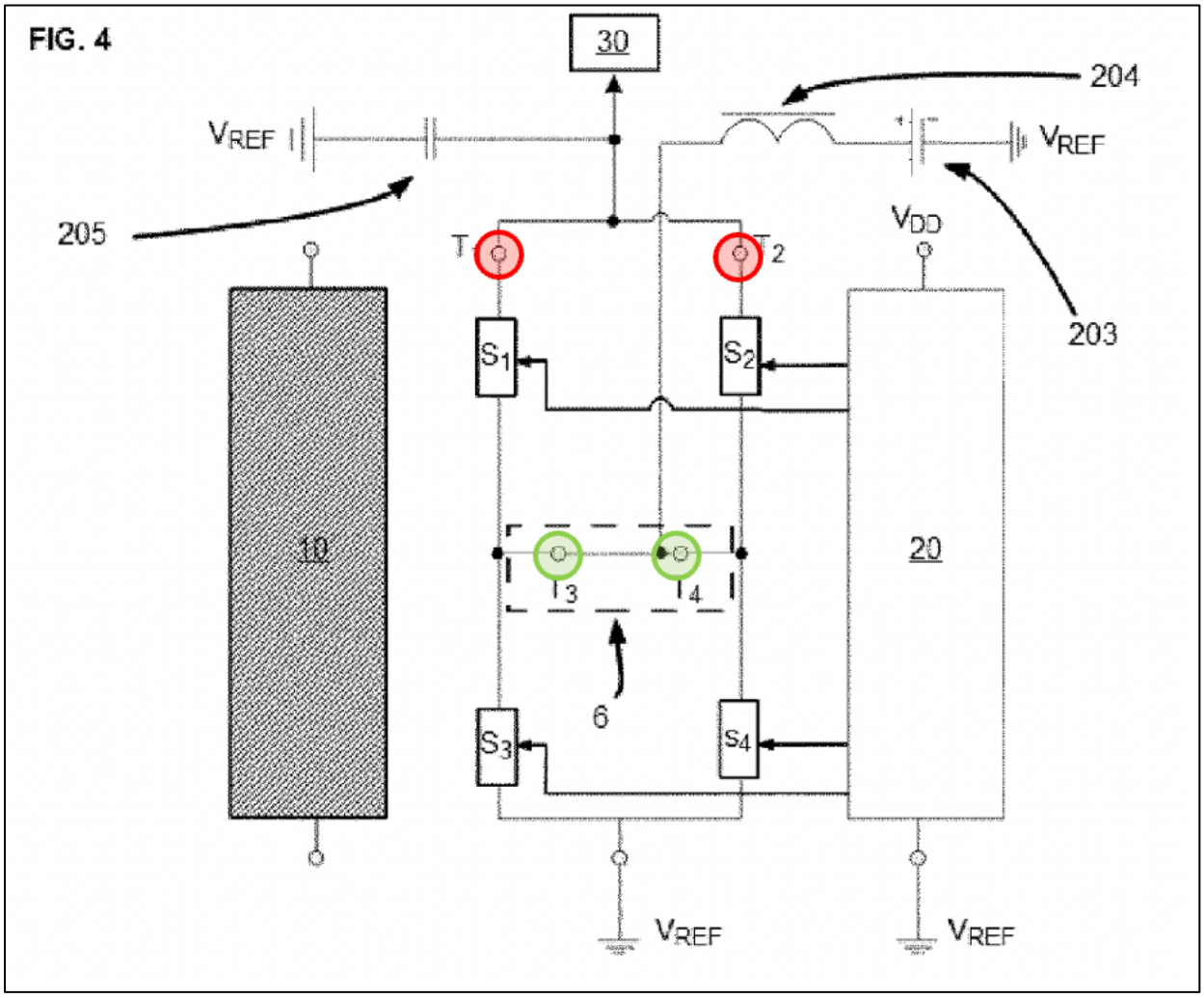
In one embodiment described and illustrated in Figure 3, the '400 Patent describes using an H-bridge circuit structure to function as a Class-D amplifier used with an audio speaker:



Id. at Fig. 3 (color emphasis added). As illustrated and described, there are four "configurable input/output terminals" labeled T_1-T_4. *See id.* at 6:66-7:24. There are also four switches S_1-S_4 controlled by the H-bridge control stage 10. *See id.* In this embodiment, the first and second input/output terminals T_1 and T_2 are configured as

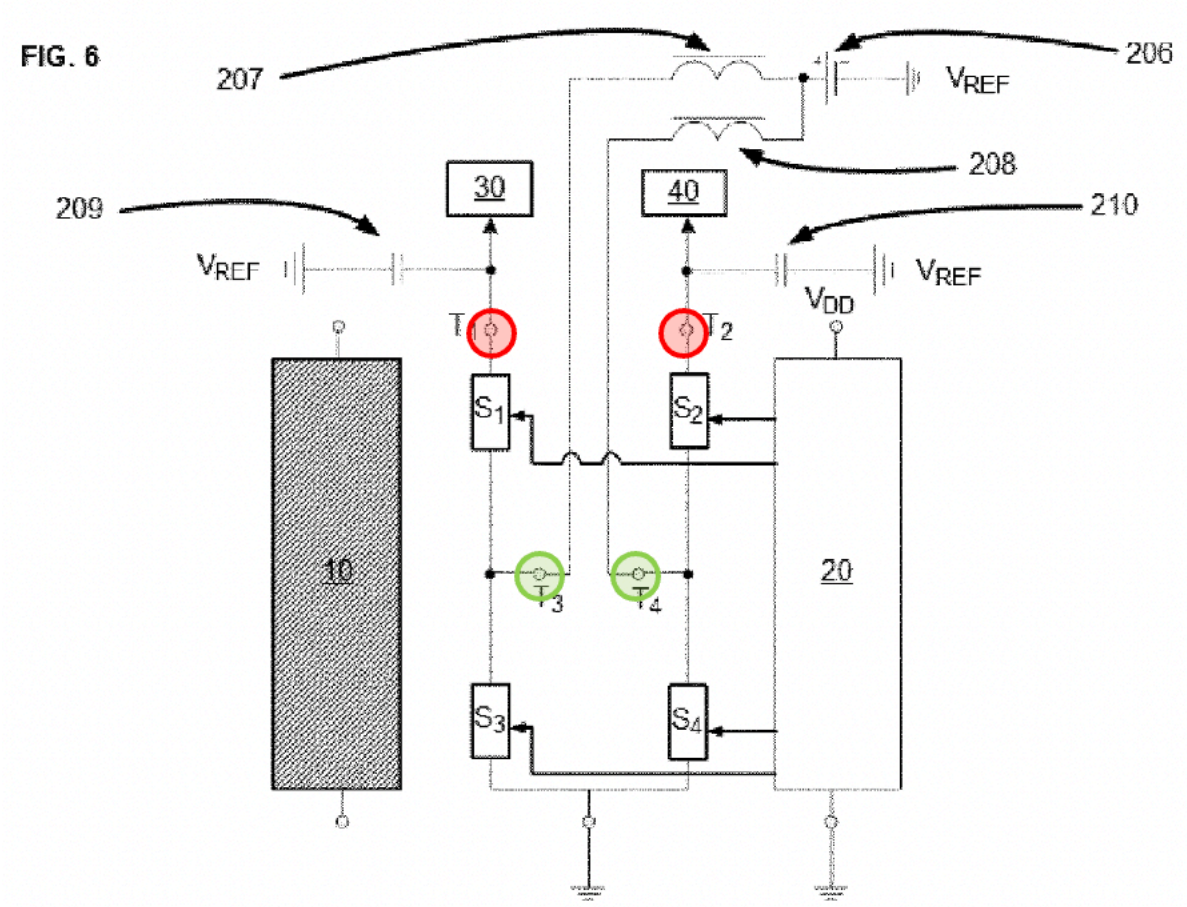
input terminals (shown in green) and connected to a common node receiving a supply potential. *See id.* And the third and fourth input/output terminals T_3 and T_4 are configured as output terminals (shown in red) and connected to a first and second end of a load element, which is illustrated here as an audio speaker 202. *See id.* Also as illustrated in this embodiment, control stage 10 is connected to the circuit and control stage 20 is disconnected. *See id.*

In another embodiment, the ’400 Patent describes modifying the circuit for use as a DC-DC boost converter configured to step up an input voltage. *See id.* at 7:29-60. That embodiment is illustrated in Figure 4:



Id. at Fig. 4 (color emphasis added). In this embodiment, the load on the central branch between terminals T_3 and T_4 is removed, creating a "short-circuit." *See id.* at 7:29-60. Instead, the load is connected to a common node that connects to terminals T_1 and T_2. *See id.* The terminals T1 and T2 are now configured as output terminals (shown in red), while the terminals T3 and T4 are configured as input terminals (shown in green). *See id*. Also as illustrated in this embodiment, control stage 20 is connected to the circuit and control stage 10 is disconnected. *See id.*

In another embodiment, the '400 Patent describes modifying the circuit for use as a double DC-DC boost converter configured to step up an input voltage to two load elements. *See id.* at 8:30-67. That embodiment is illustrated in Figure 6:



Id. at Fig. 6 (color emphasis added). As illustrated and described, there are two separate load elements 30 and 40 in this embodiment that are each in series with a respective terminal T_1 and T_2 (shown in red) and in parallel to a respective capacitor 209 and 210. *See id.* at 8:30-67. In this embodiment, unlike Figure 4 discussed above, there is no longer a "short-circuit" between terminals T_3 and T_4 (shown in green) and, instead, each of those terminals is connected through an independent inductor

to a common node receiving a supply potential 206. *See id.* In this configuration, as described in the '400 Patent, each branch of the structure leading to load elements 30 and 40 can be controlled independently by the control stage 20. *See id.*

B. The '400 Patent's Prosecution

The Application that issued in the '400 Patent was filed on November 9, 2015, as a national phase in the United States claiming priority to International Application No. PCT/EP2014/061350 with an International Filing Date of June 2, 2014. *See File History* (Ex. 1002) at 1. In the United States, the Application received a first action allowance, and there are no substantive rejections on the record here. *See generally id.* Apart from clerical changes to the claims in a Preliminary Amendment and additional changes to address minor formalities and claim dependency in an Amendment After Allowance, no changes were made to the claims during prosecution in the national phase in the United States. *See id.* at 12-19, 215-236. However, in the Notice of Allowance, the Examiner's reason for allowance indicated that the prior art of record (EP 1526643) failed to teach the claimed output stage as a whole and, more specifically, "fail[ed] to disclose wherein, when the first and second input/output terminals are configured to operate as input terminals, the third and fourth input/output terminals are configured to operate as output terminals; and, when the first and second input/output terminals are configured to operate as output

terminals, the third and fourth input/output terminals are configured to operate as input terminals." *Id*. at 199–200.

In the counterpart application in the European Patent Office (from which the same International Application No. PCT/EP2014/061350 claims priority), the applicant submitted a claim set similar in scope to those issued in the '400 Patent. *Compare*, *e.g.*, EPO File History (Ex. 1003) at 240-244, Claim 1 *with* '400 Patent at Claim 1. In contrast to the USPTO examiner, the EPO examiner there noted that "the present claims are too broad and too ambiguous to be allowable." EPO File History at 231-232. In order to position the EPO counterpart application for allowability, the applicant there was prompted to limit the scope of the claims to an integrated circuit that switches between a Class-D amplifier and a DC-DC converter. *See id.* To that end, the applicant submitted a claim amendment adding the following limitations to claim 1:

> wherein the integrated circuit further comprising a Class-D control stage and a DC-DC converter control stage wherein,
>
> If Class-D control stage is connected to the output stage, the DC-DC converter control stage is electrically disconnected from the output stage, the output stage being configured to operate as a Class-D amplifier output stage; and,
>
> If the DC-DC converter control stage is connected to the output stage, the Class-D control stage is electronically disconnected from the output stage, the output stage being configured to operate as a DC-DC converter.

Id. at 117. These limitations were found to be "essential" to the definition of the invention by the EPO. *See id.* at 148-49. And, notably, these limitations that were required in the EPO are absent from the Challenged Claims, and there are no similar limitations that limit the Challenged Claims to the subject matter found patentable there.

C. A Person Having Ordinary Skill in the Art

A person having ordinary skill in the art ("PHOSITA") at the time of the '400 Patent would have had a bachelor's degree in electrical engineering or equivalent with one year of experience in the field of electronic circuit design. Additional education or experience might substitute for the above requirements. *Hassoun Decl.* (Ex. 1006), ¶¶ 47-48.

III. REQUIREMENTS FOR IPR UNDER 37 C.F.R. § 42.104

A. Standing Under 37 C.F.R. § 42.104(A)

Petitioner certifies that the '400 Patent is available for IPR and that Petitioner is not barred or estopped from requesting an IPR challenging the claims of the '400 Patent. Specifically, (1) Petitioner is not the owner of the '400 Patent, (2) Petitioner has not filed a civil action challenging the validity of any claim of the '400 Patent, and (3) this Petition is filed less than one year after the Petitioner was served with a complaint alleging infringement of the '400 Patent.

B. Challenge Under 37 C.F.R. § 42.104(B) and Relief Requested

In view of the prior art and evidence presented, claims 1, 2, 8, 10, and 14 of the '400 Patent are unpatentable and should be cancelled. 37 C.F.R. § 42.104(b)(1). Further, based on the prior art references identified below, IPR of the Challenged Claims should be granted. 37 C.F.R. § 42.104(b)(2).

Proposed Ground of Unpatentability	Exhibits
Ground 1: Claims 1, 2, 8, and 10 are obvious under AIA 35 U.S.C. § 103 over International Publication WO 2010/111433 A2 ("Smith").	Ex. 1004
Ground 2: Claim 14 is obvious under AIA 35 U.S.C. § 103 over International Publication WO 2010/111433 A2 ("Smith") in view of United States Patent No. 5,506,493 (Stengel).	Ex. 1004 Ex. 1005

Section V identifies where each element of the Challenged Claims is found in the prior art. 37 C.F.R. § 42.104(b)(4). The exhibit numbers of the evidence relied upon to support the challenges are provided above and the relevance of the evidence to the challenges raised is provided in Section V. 37 C.F.R. § 42.104(b)(5). **Exhibits 1001-1014** are also attached.

C. Claim Construction Under 37 C.F.R. § 42.104(B)(3)

In this proceeding, claims are interpreted under the same standard applied by Article III courts (i.e., the *Phillips* standard). *See* 37 C.F.R § 42.100(b); *see also* 83 Fed. Reg. 197 (Oct. 11, 2018); *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (*en banc*). Under this standard, words in a claim are given their plain meaning which is the meaning understood by a person of ordinary skill in the art in

view of the patent and file history. *Phillips*, 415 F.3d 1303, 1212-13. For purposes of the proposed grounds below, Petitioner proposes no terms require express construction.

In the related ITC investigation and district court litigation, no claim constructions have been exchanged, no claim construction briefs have been filed, and no claim construction order has been issued.

IV. DISCRETIONARY CONSIDERATIONS

A. The *Fintiv* Factors Favor Institution

The ’400 Patent is the subject of complaints filed in district court and ITC by Patent Owner on January 17, 2022, and January 18, 2022, respectively. As set forth below, the *Fintiv* factors, and recent Board decisions applying them, weigh against discretionary denial. IPR2020-00019, Paper 11, 5–6 (Mar. 20, 2020) (precedential).

Factor 1: Institution Supports Stays in Parallel Proceedings

The district court litigation is stayed pending finality of the ITC investigation. While it is unlikely the ITC investigation will be stayed, as explained herein, the efficiency and integrity of the system are best served by instituting review.

Factor 2: Timing of Final Written Decision and ITC Conclusion

The currently scheduled ITC hearing is set to conclude on January 12, 2023, and an Initial Determination is not due until April 24, 2023. *Proposed Scheduling Order* (Ex. 1014), 1. After the Initial Determination issues, months will pass before a final determination issues on August 24, 2023, which is not appealable (i.e., not

final from a procedural standpoint) until after the presidential review period expires—60 days later on October 23, 2023. 19 U.S.C. § 1137(c), (j)(4).

A Final Written Decision will likely issue early October 2023, which is approximately the time the ITC investigation becomes final from a procedural standpoint.

Factor 3: Early Stage of Parallel Proceedings

By any standard, Apple filed this petition at very early stages of both parallel proceedings, a fact that "has weighed against exercising the authority to deny institution under *NHK*." IPR2020-00156, Paper 10, 11–12 (June 15, 2020). Moreover, this petition was filed well before the one-year statutory bar date. IPR2018-01680, Paper 22, 18 (Apr. 3, 2019) ("weighing heavily in [petitioner's] favor").

Factor 4: The Petition Raises Unique Issues

The parallel proceedings are in their infancy, and there is at present no overlap of issues between the parallel proceedings and any IPR resulting from this petition. A lack of such overlap weighs "against exercising discretion to deny institution." IPR2020-00019, Paper 11, 12-14.

This petition also raises issues unique to unpatentability of the Challenged Claims because, as the Board has acknowledged, "the burden of proof in demonstrating that a patent claim is invalid differs between the ITC and an *inter*

partes review." IPR2020-00223, Paper 12, 33–34 (May 26, 2020). Institution also provides an opportunity for the Challenged Claims to be found unpatentable because, even if the claims are demonstrated to be invalid in the ITC, "the ITC does not have the power to cancel a patent claim." *Id*. at 33. Denying institution for discretionary reasons could therefore permit Patent Owner to continue asserting these claims in the district court litigation even after a finding of invalidity in the ITC, further counseling against discretionary denial.

Moreover, to eliminate any doubt as to the absence of meaningful overlap between the proceedings, Apple stipulates that upon institution of the instant petition, Apple will not seek resolution in the parallel proceedings of invalidity based on *Smith*—the base reference relied upon herein. Consequently, upon institution, the PTAB alone will consider patentability in view of *Smith*, eliminating concerns over duplicative effort or conflicting decisions.

Factor 5: Apple's Involvement in Parallel Proceedings

With respect to Factor 5, the *Fintiv* decision "says nothing about situations in which the Petitioner is the same as, or is related to, the district court defendant." IPR2020-00122, Paper 15, 10 (May 15, 2020) ("the factor is neutral.") *Id*. at 11.

Factor 6: Other Considerations Support Institution

As evidenced from the below analysis, Apple's patentability challenge is unusually strong, which favors institution. IPR2020-00156, Paper 10, 20–21.

V. THE CHALLENGED CLAIMS ARE UNPATENTABLE

A. Ground 1: Claims 1, 2, 8, and 10 are obvious under AIA 35 U.S.C. § 103 over *Smith*

Overview of Smith

International Publication WO 2010/111433 A2 to Smith ("*Smith*") was published on September 30, 2010, and is prior art to the '400 Patent under at least 35 U.S.C. § 102(a)(1) (AIA). *See generally Smith* (Ex. 1004). *Smith* was not cited or considered during prosecution of the '400 Patent. *'400 Patent* (Ex. 1001).

Smith is generally directed to a bidirectional converter that functions in some embodiments "as a DC to AC energy converter and/or an AC to DC energy converter within the same device or component." *Smith* (Ex. 1004), at [0005]. A circuit is described for bidirectional conversion and, "[w]ithin the circuit, current may flow in opposite directions, depending on the mode of operation." *Id.* Thus, *Smith* describes that this circuit "may operate in an AC generation mode, where the bidirectional converter may function as an inverter to convert DC to AC." *Id.* at [0043]. Further, the circuit "may also operate in a charge mode, where the bidirectional converter may function as a rectifier to convert AC to DC." *Id. Smith* emphasizes that "[t]he bidirectional converter may be able to operate in both modes within the same device or component, rather than utilizing two separate circuits or components for each mode." *Id.* "For different modes, the same circuit with the same paths may be operating in forward or reverse." *Id.*

Smith also describes embodiments that utilize an H-bridge circuit in various operating states with various configurations. For instance, this H-bridge circuit is illustrated in Figures 19 and 22:

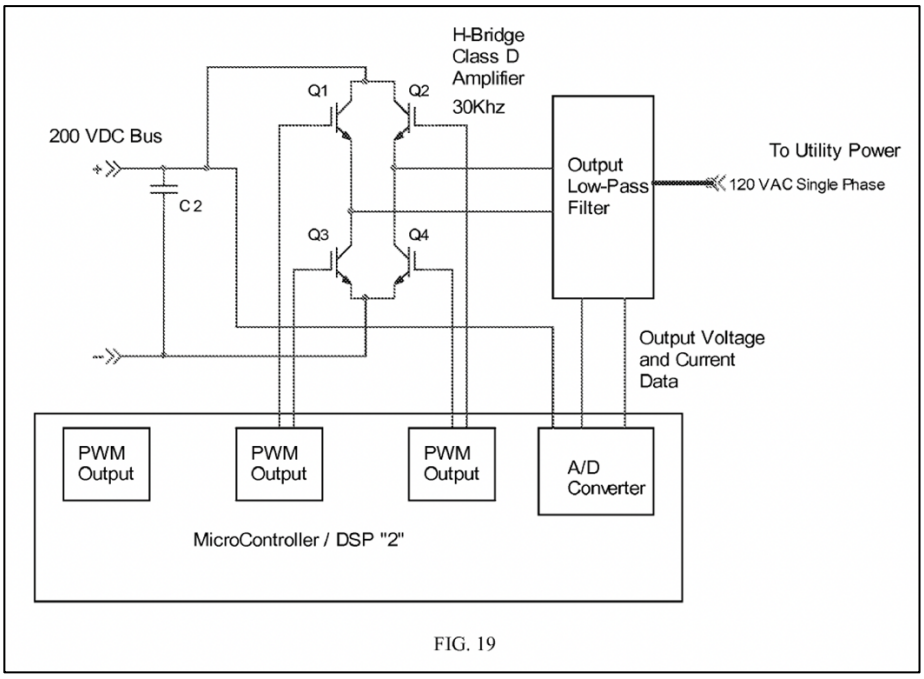


FIG. 19

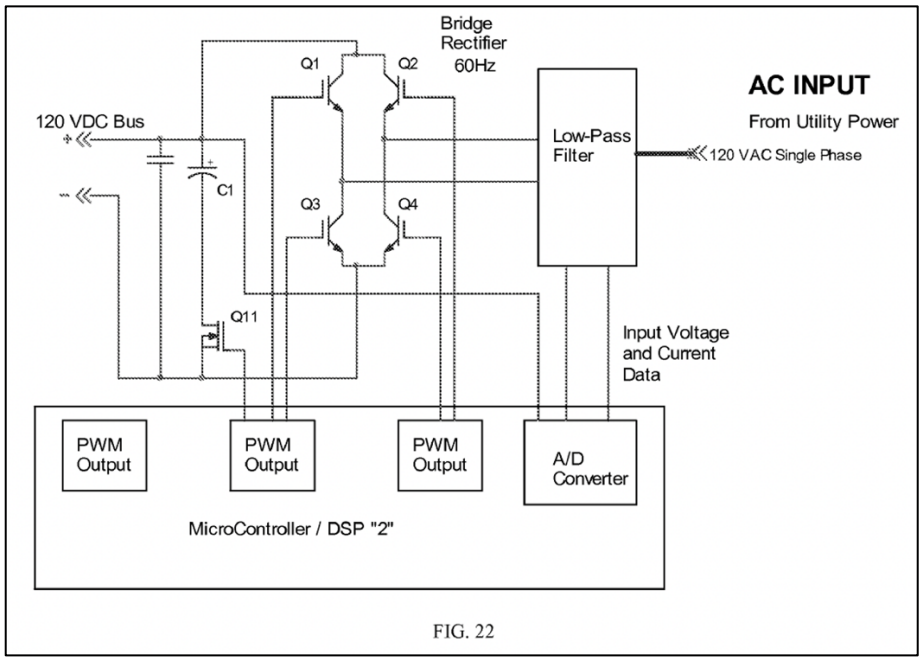


FIG. 22

Id. at Figs. 19 and 22. The embodiment illustrated in Figure 19 uses the H-bridge circuit to operate as a Class D amplifier that receives a DC input and converts it to an amplified AC output. *Id.* at [0097]. The embodiment illustrated in Figure 22 uses the same H-bridge circuit, but reverses the input and output terminals to create a bridge rectifier that converts an AC supply voltage to a DC output. *Id.* at [0099].

Smith is analogous art because it is in the same field of endeavor as the '400 Patent. *Hassoun Decl.* (Ex. 1006), at ¶¶ 53-54. The field of endeavor for the '400 Patent is reconfigurable output stage circuits. *See '400 Patent* (Ex. 1001) at 1:5-7 (defining the technical field as "relat[ing] generally to output stage circuits, and more especially to a reconfigurable output stage."). *Smith* is within this same field of endeavor. *See*, *e.g.*, *Smith* (Ex. 1004) at Abstract; [0004]-[0013] (describing the bidirectional converter circuit that is configurable in different operating modes); [0034] (describing Fig. 19 as "an 'H' bridge AC output stage"), [0037] (describing Fig. 22 as "an example of where Q1-Q4 may reverse roles and serve as a bridge rectifier"); Fig. 19; Fig. 22; *see also Hassoun Decl.* (Ex. 1006), at ¶¶ 53-54.

Smith is also analogous art because it is reasonably pertinent to the problem that the '400 Patent purports to solve. *Hassoun Decl.* (Ex. 1006), at ¶¶ 53-54. The '400 Patent describes a problem in that prior art is purportedly inefficient and costly because special purpose circuitry is used for different output needs. *See '400 Patent* (Ex. 1001) at 1:19-40. The '400 Patent purports to solve this problem with a circuit

that can be shared by multiple components, such as a Class-D amplifier and a DC-DC boost converter. *See id.* at 1:44-56. *Smith* teaches the same solution to this purported problem. *See Smith* (Ex. 1004) at [0043] (noting that "[a] single circuit may be utilized to form the bidirectional converter," and that "[f]or different modes, the same circuit with the same paths may be operating in forward or reverse."); Fig. 17 (illustrating a DC-DC converter); Fig. 19 (illustrating a Class-D amplifier); *see also Hassoun Decl.* (Ex. 1006), at ¶¶ 53-54.

i. Claim 1.

1[P] An output stage adapted to operate in at least a first operating state and a second operating state, the output stage comprising:

To the extent the preamble is limiting, *Smith* teaches an output stage adapted as claimed. As a general matter, *Smith* describes a bidirectional converter circuit that has multiple modes of operation. *See Smith* (Ex. 1004) at [0005]-[0006]. In particular, *Smith* describes and illustrates an H-bridge "output stage" that functions, in at least one mode of operation, as a "class 'D' amplifier" that produces an AC output at a desired frequency. *See Smith* at [0097]. *Smith* also describes and illustrates another mode of operation, in which the H-bridge output stage functions, in at least one mode of operation, as a "bridge rectifier" that converts AC line voltage to a DC output. *See id.* at [0099]. The circuitry of the output stage for each of these two operating states is illustrated and highlighted in Figures 19 and 22 below:

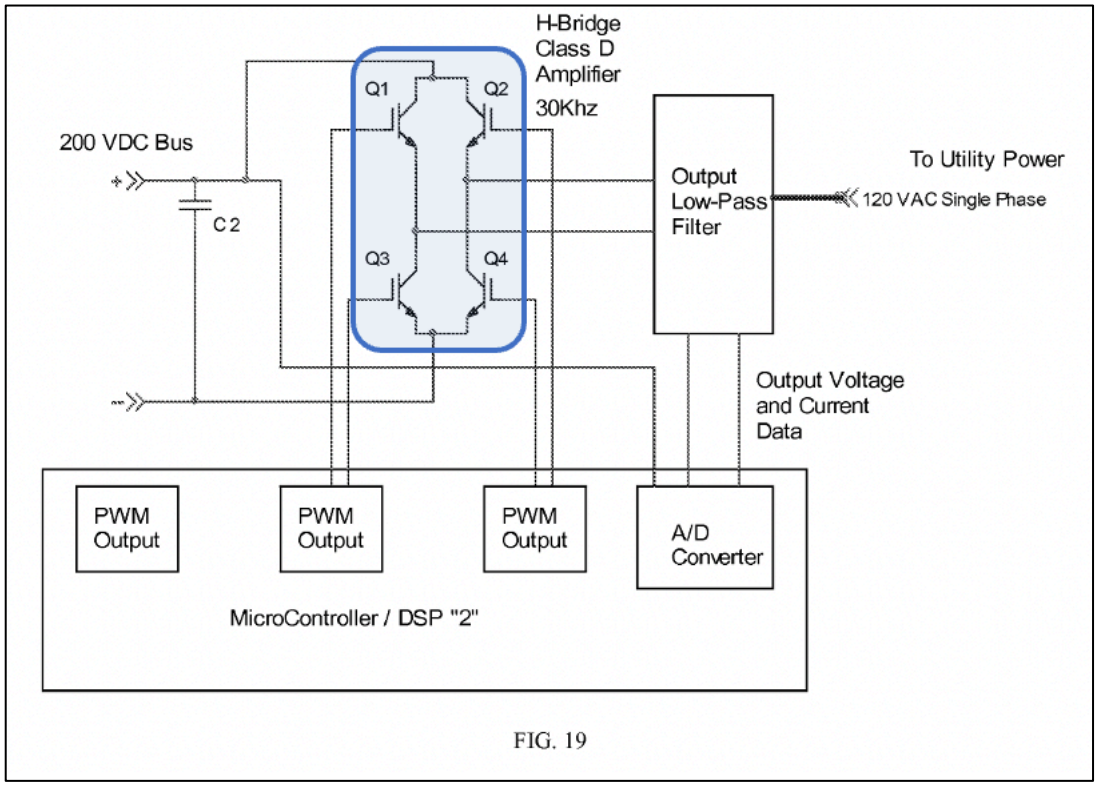


FIG. 19

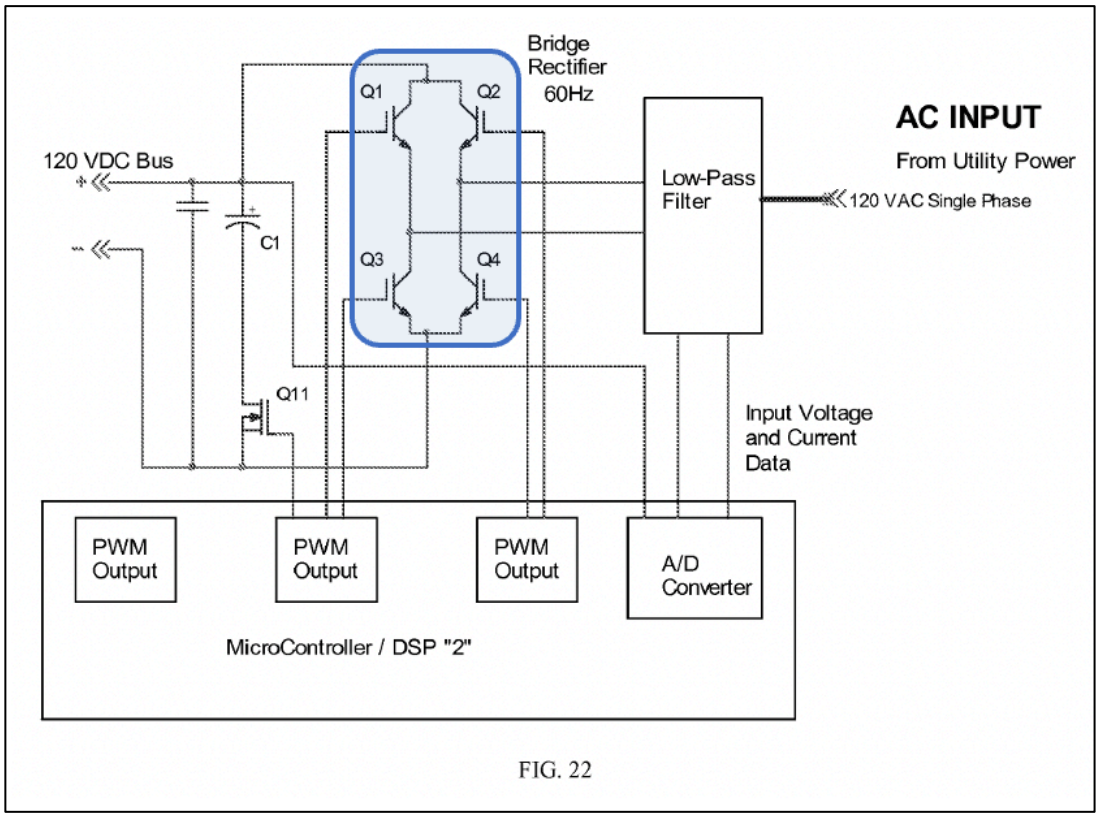


FIG. 22

Id. at Figs. 19, 22 (color emphasis added).

[1(a)] a first, a second, a third and a fourth configurable input/output terminals; and

Smith discloses four configurable input/output terminals. *See id.* at [0097], [0099]; *see also id.* at Figs. 19, 22. In the first operating state, the input/output terminals at the top of the H-bridge are used as input from a DC power source, and the input/output terminals on the branches of the H-bridge are used as AC output. *See id.* One operating state is illustrated in Figure 19, which is annotated below to highlight the relevant portions of the circuit, with the input terminals in green, and the output terminals in red:

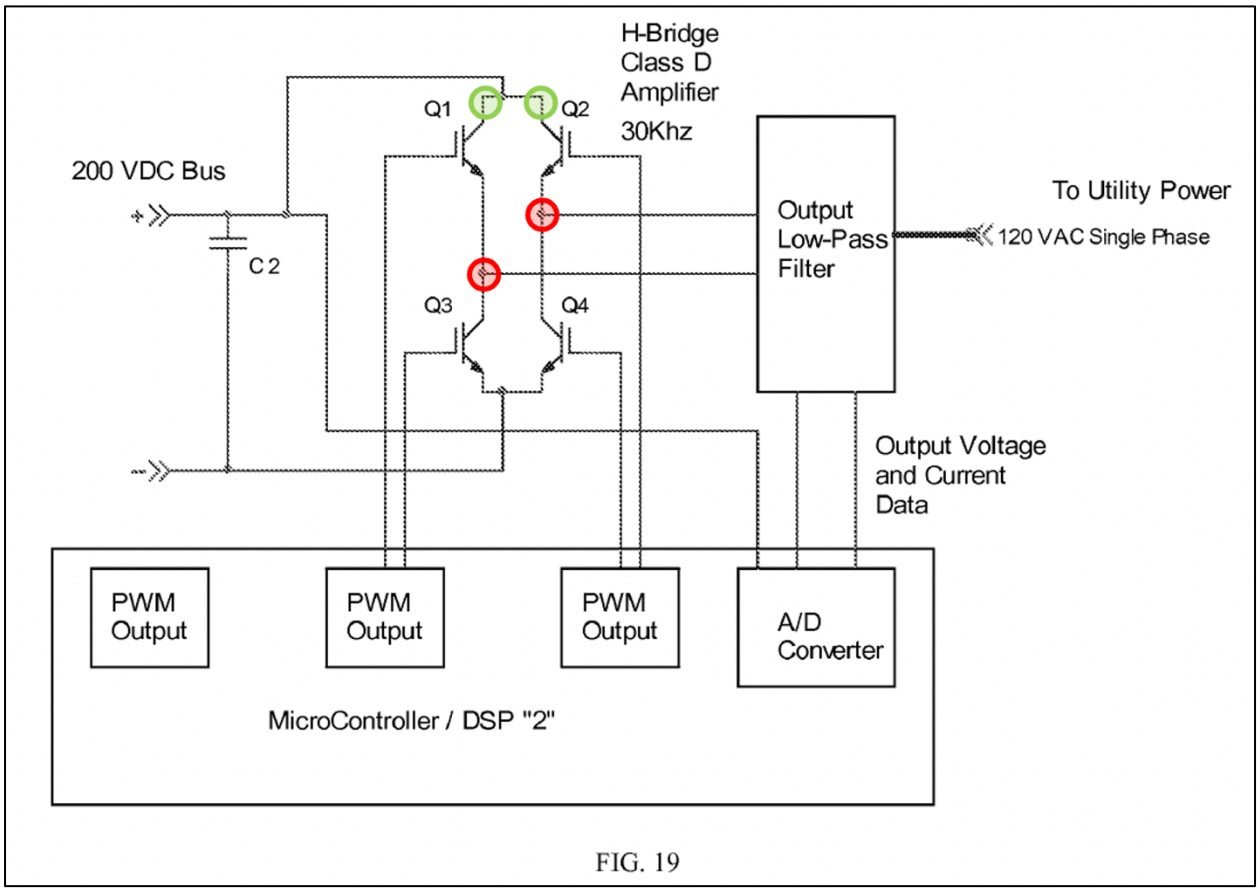


FIG. 19

Id. at Fig. 19 (color emphasis added).

Another operating state where the output stage is used as a bridge rectifier is illustrated in Figure 22. *See id.* at [0099]; Fig. 22. Here, the same input/output terminals are now reconfigured, with the terminals on the top of the H-bridge used as DC output (annotated in red), and the terminals on the branches of the H-bridge used as AC input (annotated in green):

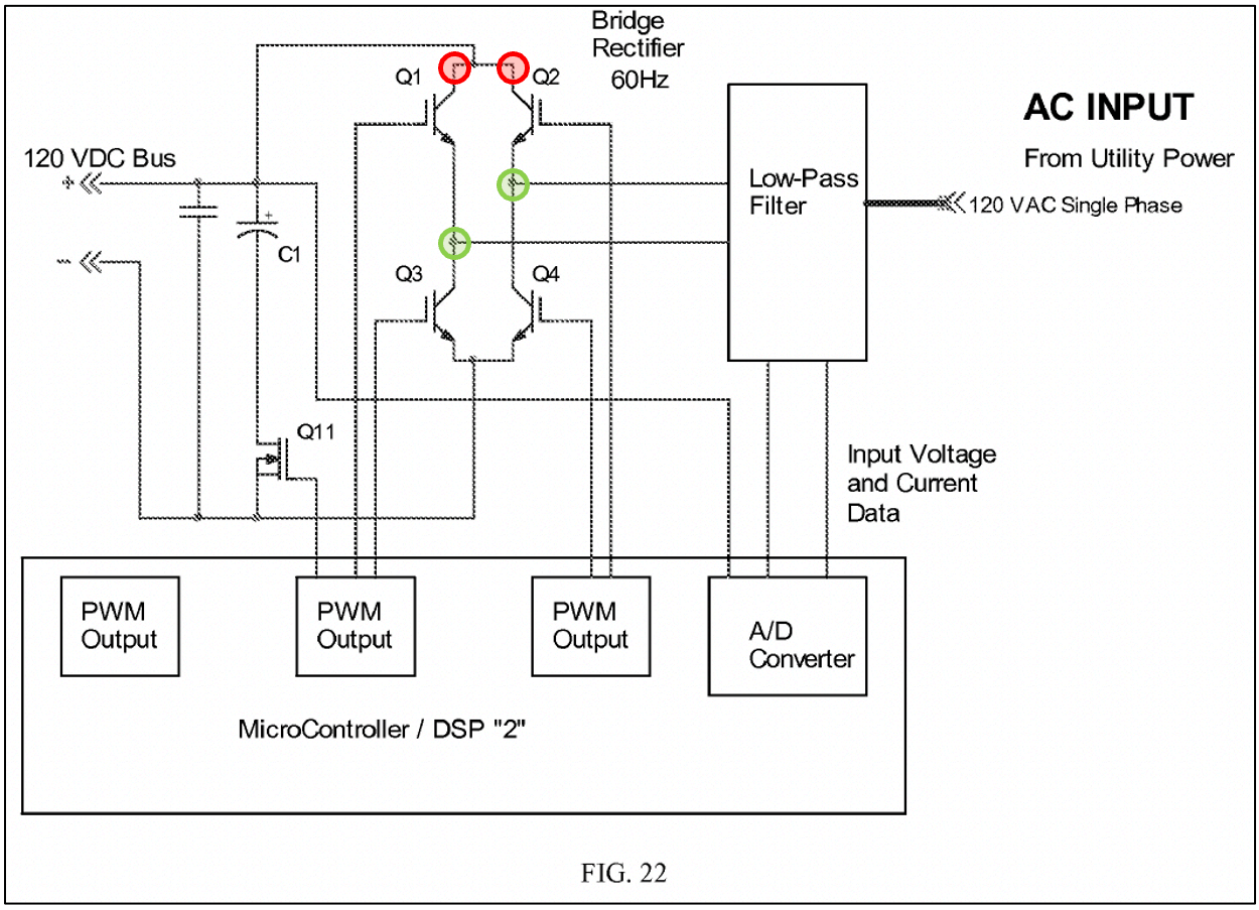


FIG. 22

Id. at Fig 22 (color emphasis added). A PHOSITA would understand and appreciate that the terminals disclosed in *Smith* and illustrated in both red and green in the figures above would be terminals, because they are the end point of a wire as it connects to a transistor. *See Hassoun Decl.* (Ex. 1006), at ¶¶ 60-63. Further, these

terminals are configurable input/output terminals because they can be used for input or for output depending upon the operating state. *See id.*

[1(b)] a first, a second, a third and a fourth switches, each having a first main terminal, a second main terminal and a control terminal, the control terminal being adapted to receive a control signal for controlling the open or closed state of the switch,

Smith discloses four switches, labeled Q1-Q4. *See Smith* (Ex. 1004) at [0097], [0099]; *see also id.* at Figs. 19, 22. Each of the four switches includes a first and a second main terminal, and also a control terminal. *See id.* In the annotated Figure 19 shown below, each of the switches' main terminals is shown with a blue circle, and each of the control terminals is shown with a purple circle:

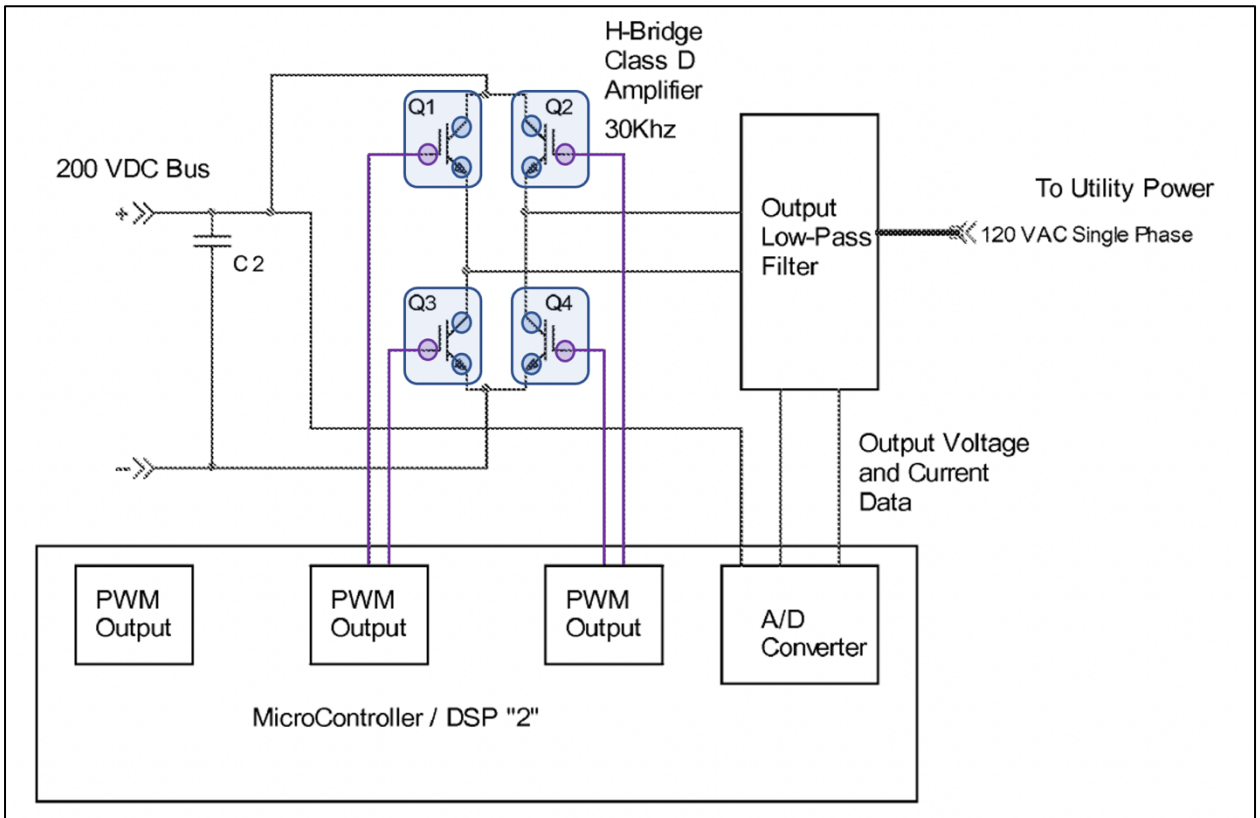


FIG. 19

Id. at Fig 19 (color emphasis added). Additionally, each of the switches Q1-Q4 described and illustrated in *Smith* receives a control signal (through a line highlighted in purple in the annotated Figure 19) at the control terminal for controlling the open or closed state of the switch. *See id.* As illustrated in Figure 19, the switches Q1-Q4 are shown as Insulated-Gate Bipolar Transistors, although MOSFFETs may also be used. *See id.*; *see also Hassoun Decl.* (Ex. 1006), at ¶¶ 64-66. It is well understood that the gate terminal, highlighted in a purple circle in each of the switches above, is what is used to control the open or closed state of the switch. *See id.* As *Smith* describes, the switches Q1-Q4 "may receive PWM [pulse width modulation] outputs from a DSP [digital signal processor] … may control the drive signals provided to the 'H' bridge." *Smith* (Ex. 1004) at [0097].

[1(c)(i)] wherein, the first input/output terminal is connected to the first main terminal of the first switch;

Smith shows that in the output stage circuit, the first input/output terminal is connected to the first main terminal of the first switch:

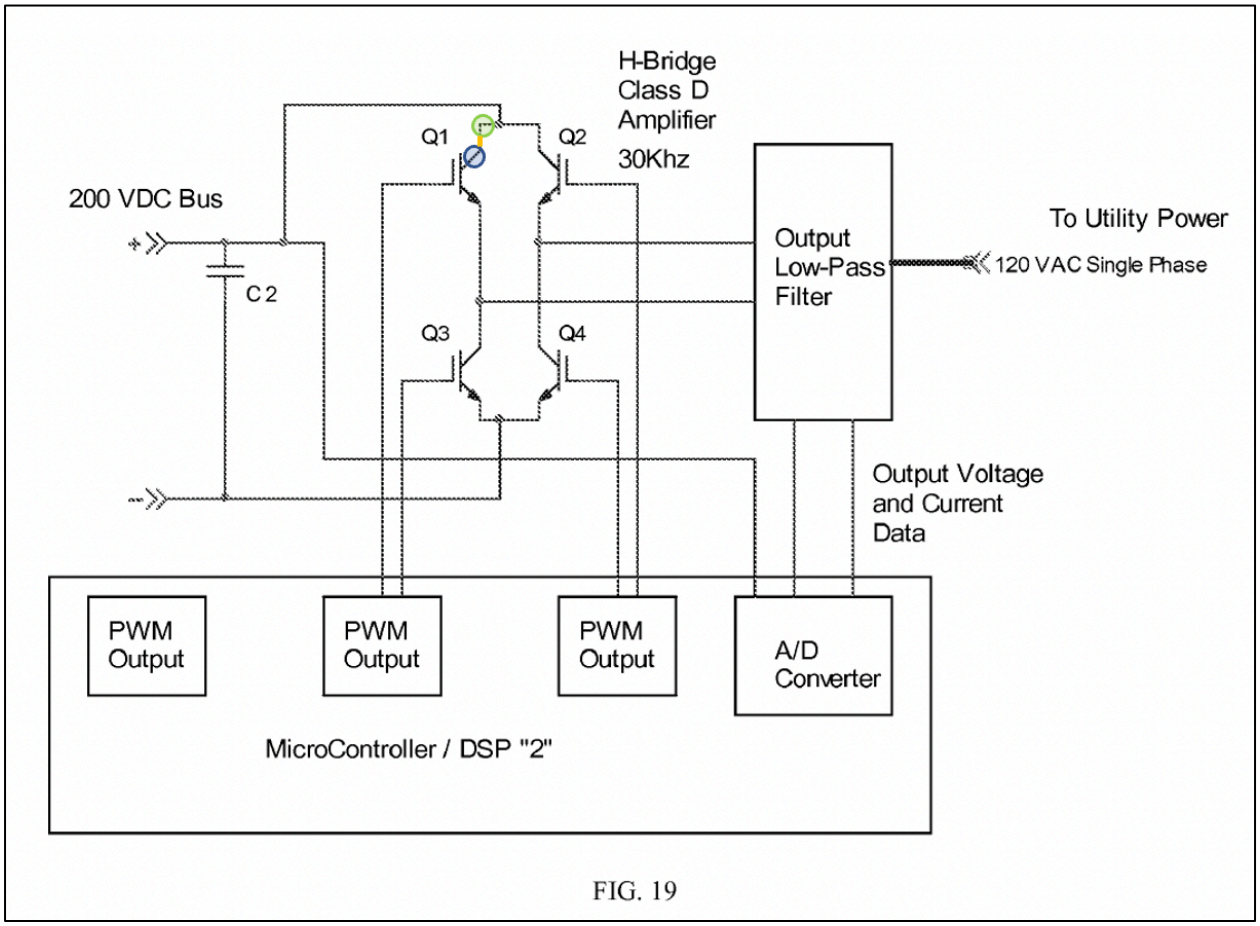


FIG. 19

Id. at Fig. 19 (color emphasis added); *see also id.* at [0097], [0099], Fig. 22.

[1(c)(ii)] the second input/output terminal is connected to the first main terminal of the second switch;

Smith shows that in the output stage circuit, the second input/output terminal is connected to the first main terminal of the second switch:

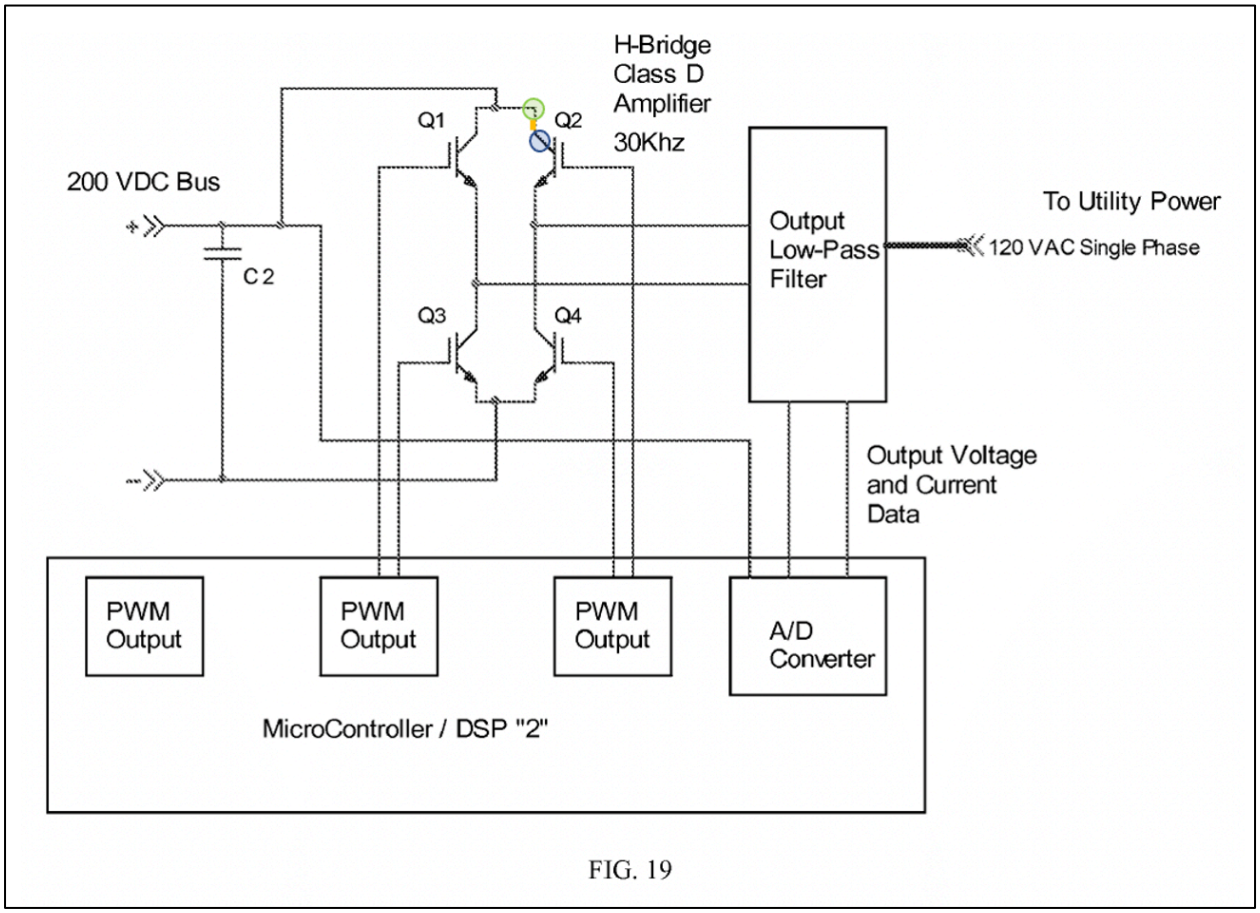


FIG. 19

Id. at Fig. 19 (color emphasis added); *see also id.* at [0097], [0099], Fig. 22.

[1(c)(iii)] the second main terminal of the first switch is connected to the first main terminal of the third switch through a first branch;

Smith shows that the second main terminal of the first switch is connected to the first main terminal of the third switch through a first branch, annotated below in orange:

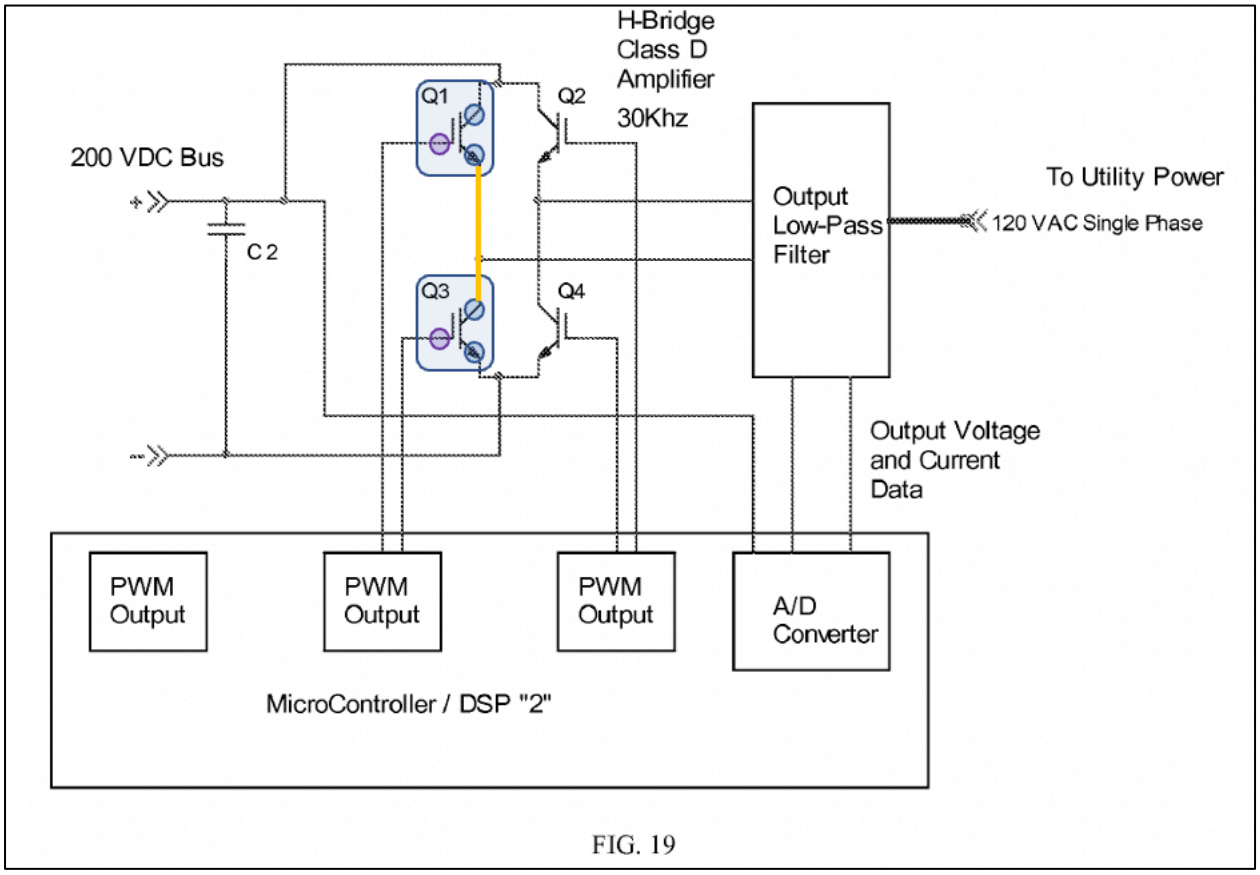


FIG. 19

Id. at Fig. 19 (color emphasis added); *see also id.* at [0097], [0099], Fig. 22.

[1(c)(iv)] the second main terminal of the second switch is connected to the first main terminal of the fourth switch through a second branch;

Smith shows that the second main terminal of the second switch is connected to the first main terminal of the fourth switch through a second branch, annotated below in orange:

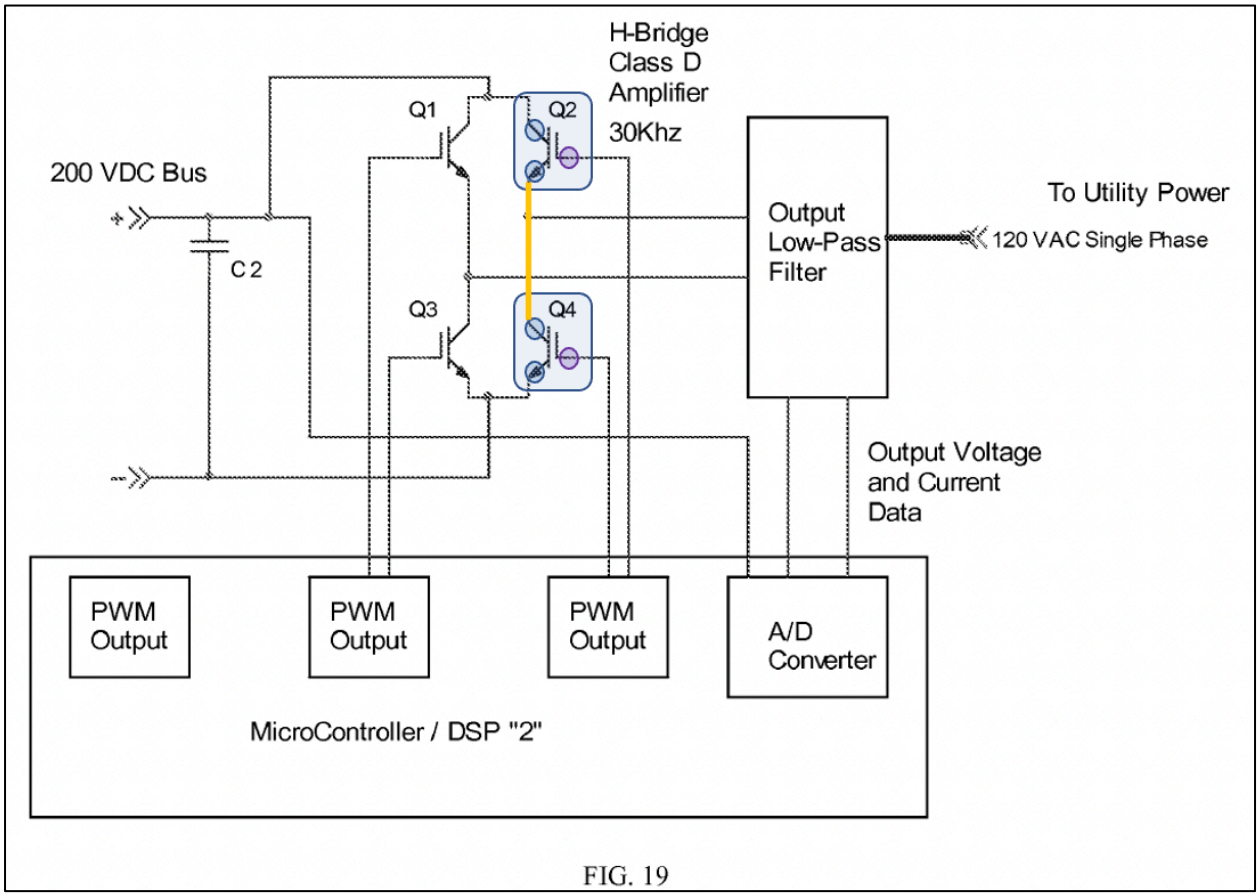


FIG. 19

Id. at Fig. 19 (color emphasis added); *see also id.* at [0097], [0099], Fig. 22.

[1(c)(v)] the third input/output terminal is connected to the first branch and the fourth input/output terminal is connected to the second branch;

Smith shows that the third input/output terminal is connected to the first branch and that the fourth input output terminal is connected to the second branch:

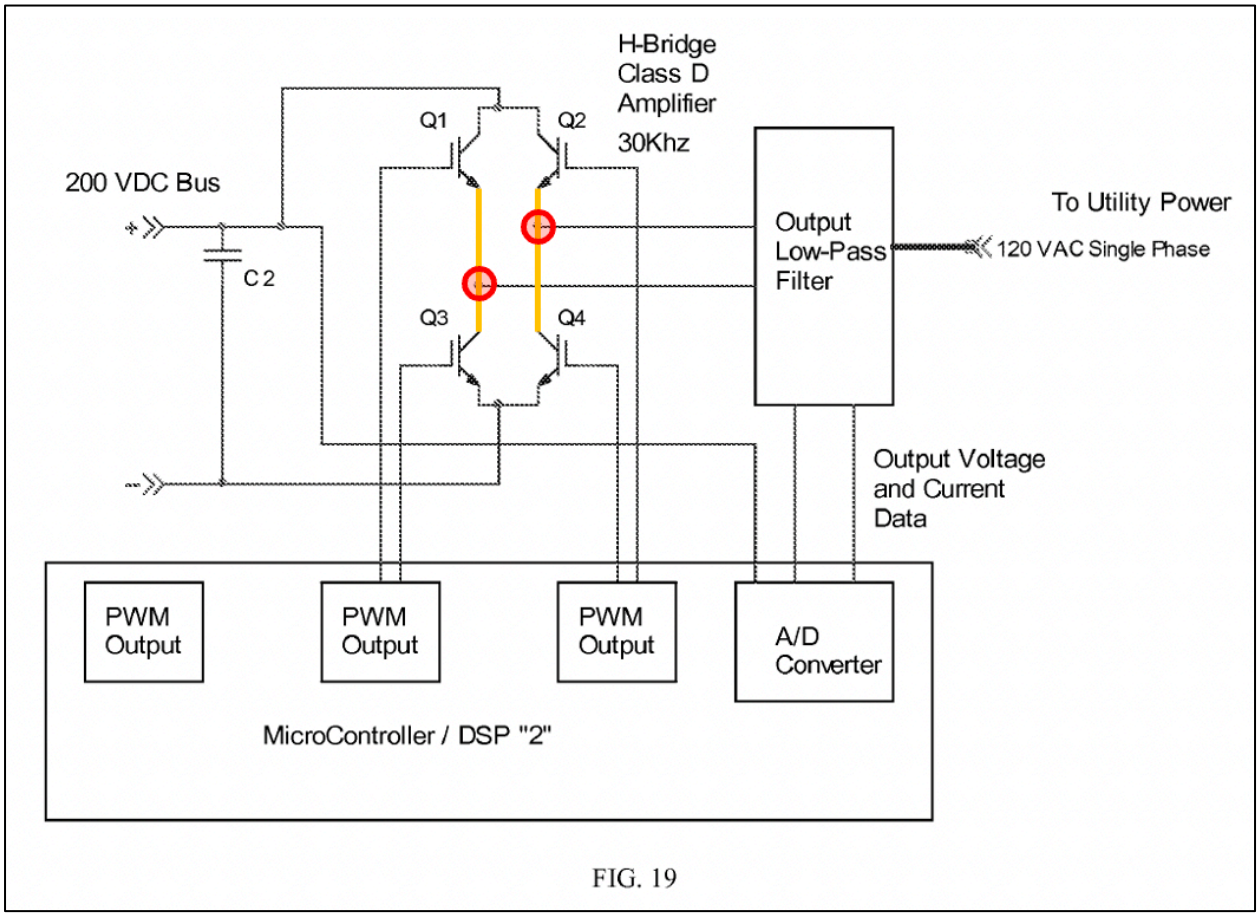


FIG. 19

Id. at Fig. 19 (color emphasis added); *see also id.* at [0097], [0099], Fig. 22.

[1(c)(vi)] the second main terminals of the third and fourth switches are both connected to a common node receiving a reference potential; and,

Smith shows that the second main terminals of the third and fourth switches are both connected to a common node, and *Smith* also shows that the common node receives a reference potential (illustrated in Fig. 19) as a connection to the VDC bus:

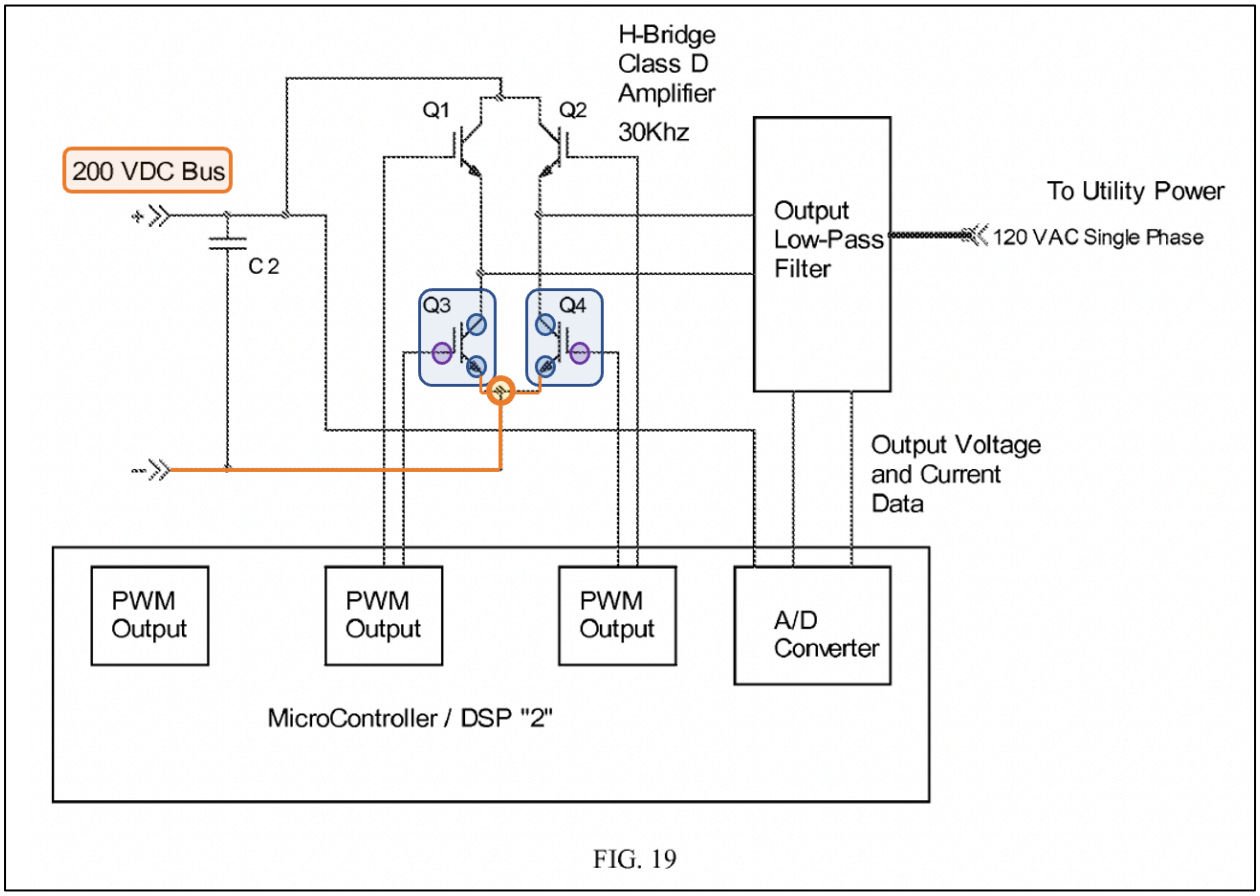


FIG. 19

Id. at Fig. 19 (color emphasis added); *see also id.* at [0097], [0099], Fig. 22. A PHOSITA would understand and appreciate that this connection to the negative terminal on the VDC bus illustrated in Figure 19 through a common node is a connection to a reference potential. *See Hassoun Decl.* (Ex. 1006), at ¶¶ 67-69. The purpose of a reference potential is to give a circuit a steady voltage against which to measure other voltages in the circuit. *See id.* Here, as would be understood and appreciated by a PHOSITA, the connection to the VDC bus would provide the circuit this reference potential. *See id.*

[1(c)(vii)] wherein, when the first and second input/output terminals are configured to operate as input terminals, the third and fourth input/output terminals are configured to operate as output terminals; and,

Smith describes and illustrates multiple operating states. For instance, in one operating state illustrated in Figure 19 and described in the corresponding disclosure, the first and second input/output terminals (annotated in green) are configured to operate as input terminals and the third and fourth input/output terminals (annotated in red) are configured to operate as output terminals:

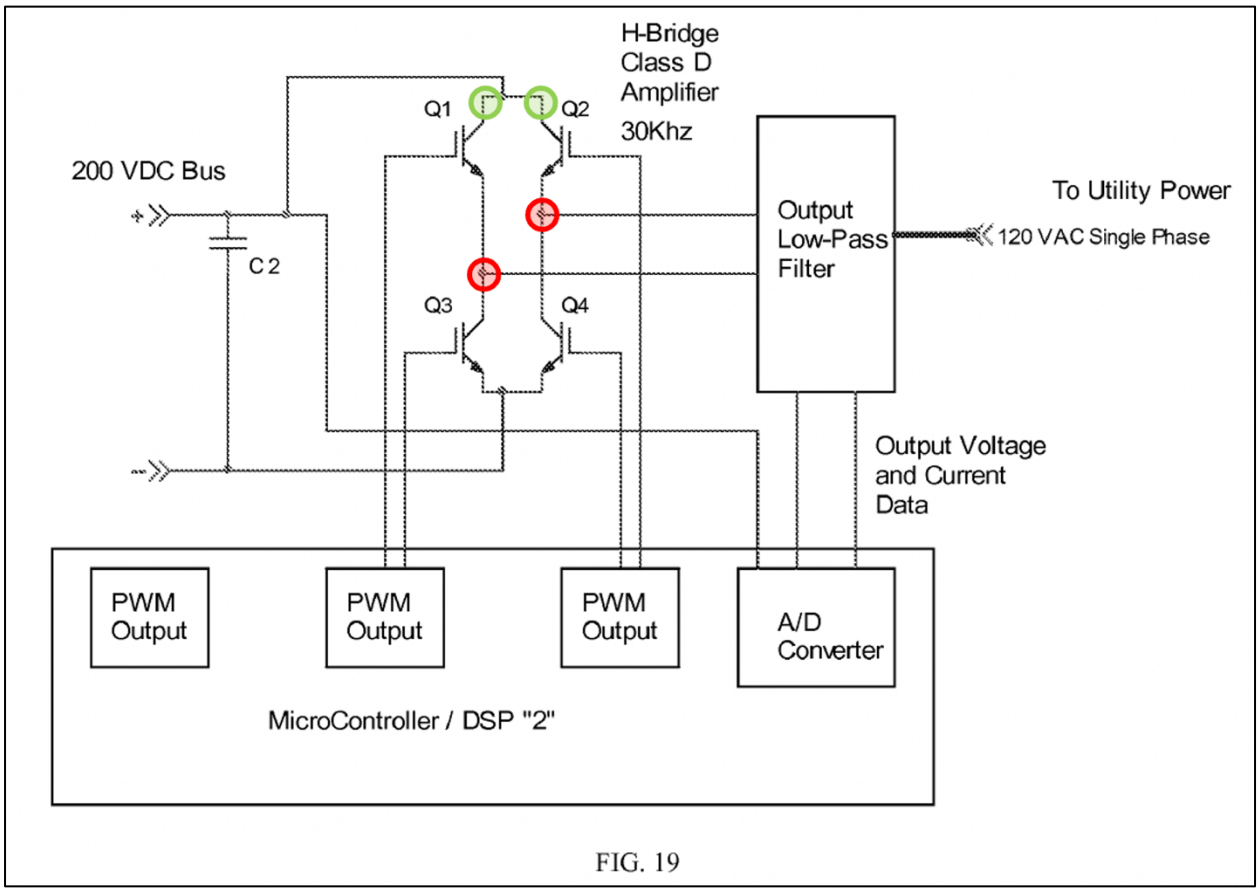


FIG. 19

Smith (Ex. 1004) at Fig. 19 (color emphasis added). In this operating state, the first and second input/output terminals that are configured as input terminals to "receive

a DC from a prior stage," such as "a half wave pulsating DC." *Id.* at [0097]. From this, the H-bridge circuit provides AC output through the third and fourth input/output terminals that are configured as output terminals. *Id.* In this operating state, the circuit illustrated in Figure 19 functions as a Class D amplifier, and "result[s] in a pure or substantially pure sine wave [AC] output." *Id.*

[1(c)(viii)] when the first and second input/output terminals are configured to operate as output terminals, the third and fourth input/output terminals are configured to operate as input terminals; and,

Smith describes and illustrates other operating states. For instance, in one operating state illustrated in Figure 22 and described in the corresponding disclosure, the first and second input/output terminals (annotated now in red) are configured to operate as output terminals and the third and fourth input/output terminals (annotated now in green) are configured to operate as input terminals:

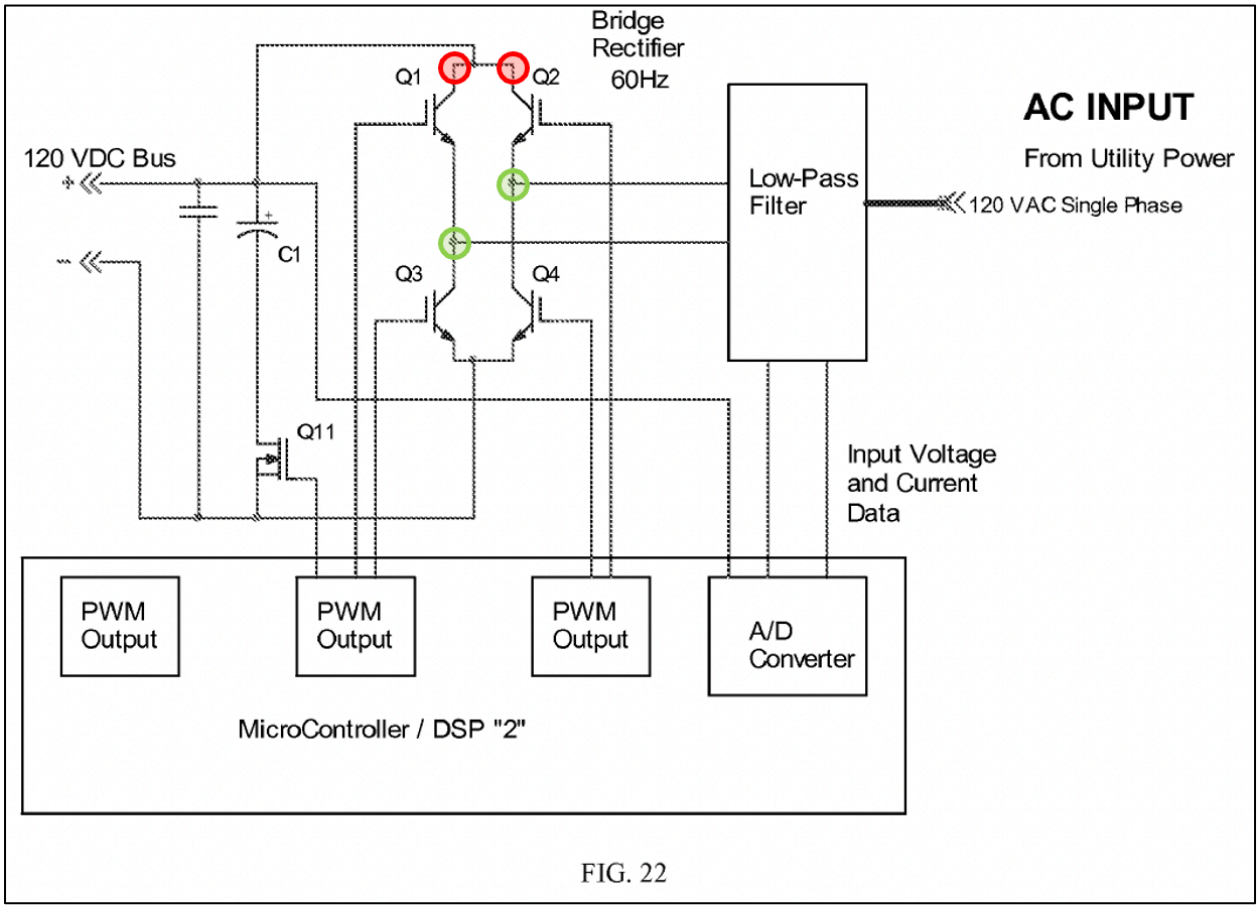


FIG. 22

Id. at Fig 22 (color emphasis added). In this operating state, the switches Q1-Q4 "reverse roles and serve as a bridge rectifier." *Id.* at [0099]. The bridge rectifier receives AC input through the third and fourth input/output terminals that are configured as input terminals. *Id.* Then the bridge rectifier outputs a DC signal through the first and second input/output terminals that are now configured as output terminals. *See id.*; *see also* Fig. 22.

[1(c)(ix)] wherein, in the first operating state, the output stage is arranged in a first electrical configuration; and

Smith illustrates and describes a first operating state where the output stage is arranged in a first electrical configuration, as shown in Figure 19:

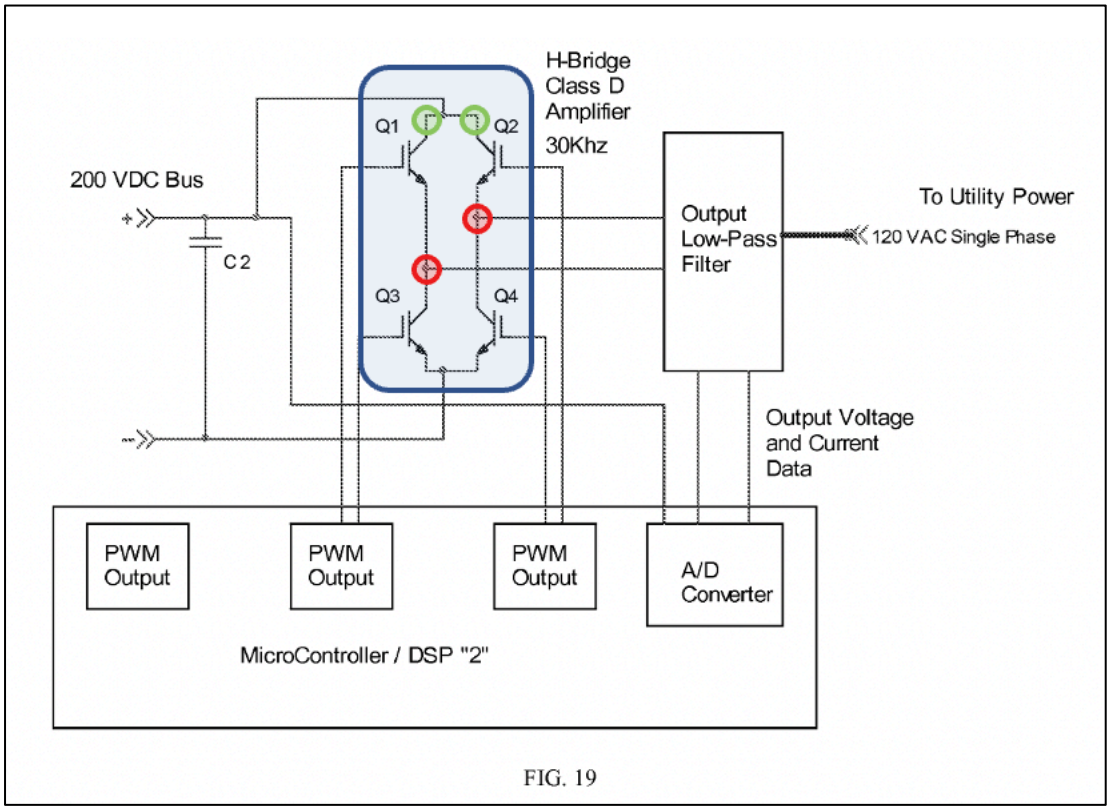


FIG. 19

Id. at Fig 19 (color emphasis added). In this first operating state, the output stage is arranged in an electrical configuration that results in a Class D amplifier that takes input from a 200 VDC Bus and provides 120 VAC output. *See id.*; *see also id.* at [0097]. In this configuration, the first and second configurable input/output terminals (annotated in green) function as inputs, and the third and fourth configurable input/output terminals (annotated in red) function as outputs. *See id.*

[1(c)(x)] in the second operating state wherein the output stage is arranged in a second electrical configuration different from the first configuration.

Smith illustrates and describes a second operating state where the output stage is arranged in a second electrical configuration, as shown in Figure 22:

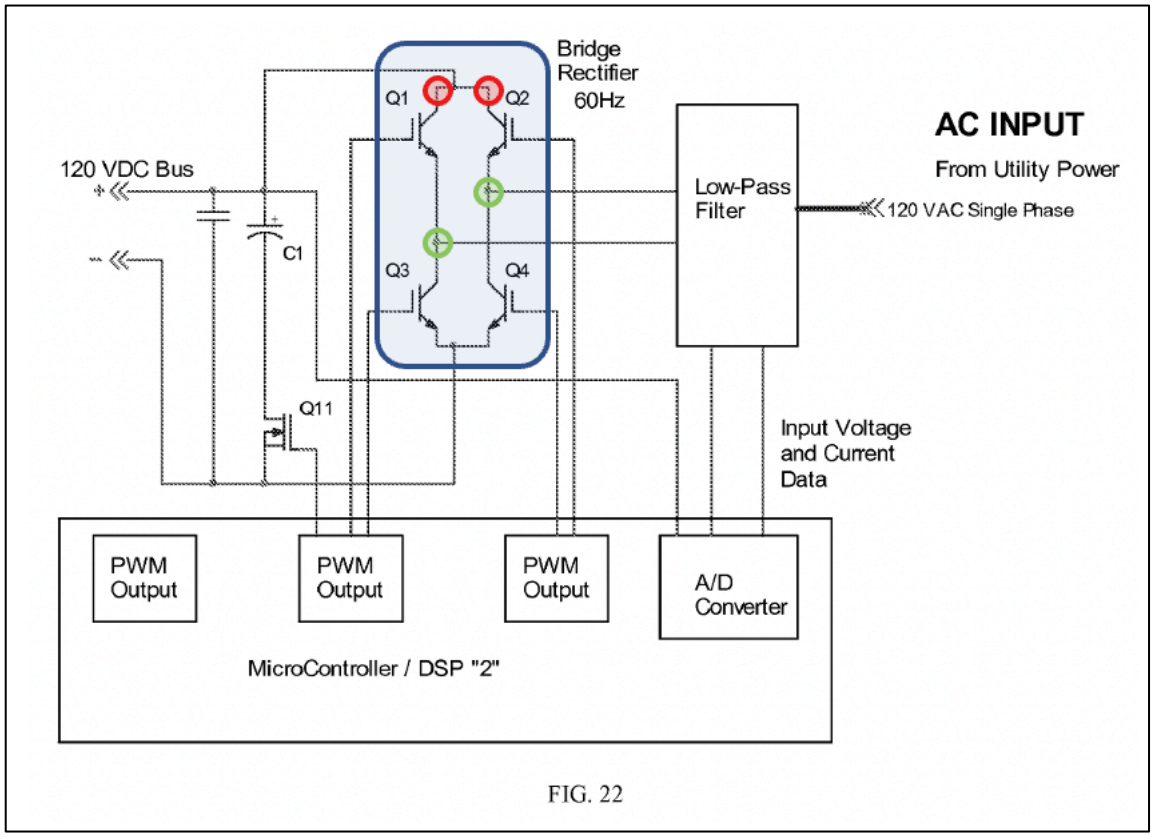


FIG. 22

Id. at Fig 22 (color emphasis added). In this second operating state, the output stage is arranged in an electrical configuration that results in a bridge rectifier that takes input from a 120 VAC source and provides output to a 120 VDC bus. *See id.*; *see also id.* at [0097]. In this configuration, the first and second configurable input/output terminals (annotated in red) function as outputs, and the third and fourth configurable input/output terminals (annotated in green) function as inputs. *See id.*

ii. Claim 2.

2[P] The output stage of claim 1, wherein, in the first operating state:

See supra at Claim 1.

[2(a)] the first and second input/output terminals are configured to operate as input terminals and are configured to be connected to a common node receiving a supply potential; and,

Smith illustrates and describes a first operating state where the first and second input/output terminals are configured to operate as input terminals and are configured to be connected to a common node receiving a supply potential, as showing in Figure 19:

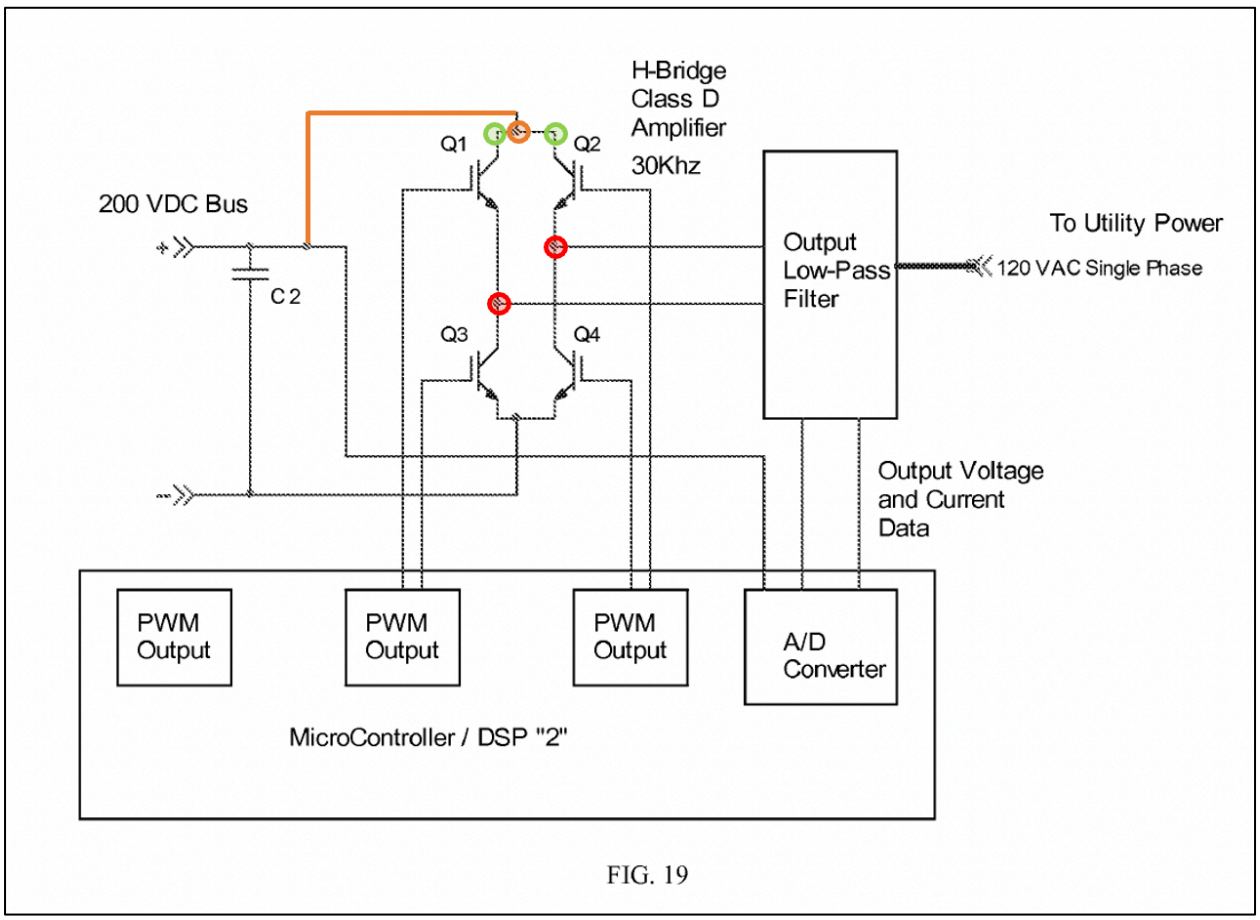


FIG. 19

Id. at Fig 19 (color emphasis added); *see also id.* at [0097]. Here, the supply potential provided to the first and second input/output terminals (annotated in green) comes from the VDC bus via the common node (annotated in orange). *See id.*

[2(b)] the third and fourth input/output terminals are configured to be connected to a load element.

Smith describes and illustrates an operating state where the disclosed circuit is used as a Class-D amplifier. *See id.* at [0097]. In that operating state described in *Smith*, and illustrated in Figure 19, the third and fourth input/output terminals are configured to be output terminals for the Class-D amplifier. *See id.*

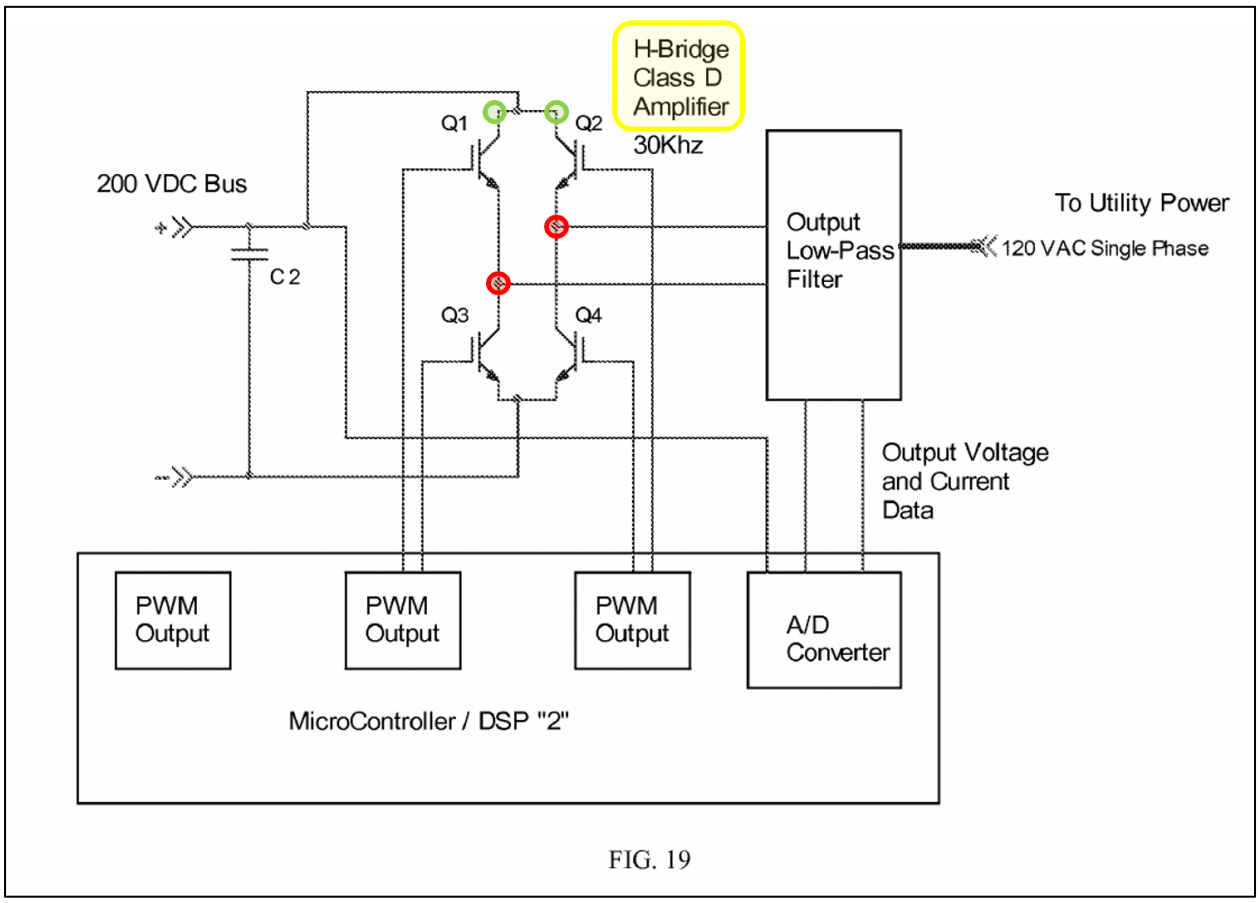


FIG. 19

See id. at Fig. 19 (color emphasis added). As illustrated here, the third and fourth input/output terminals (annotated in red) are connected through a low-pass filter to a 120 VAC output. It would be well understood and appreciated by a PHOSITA that this connection to the 120 VAC output is a connection to a load element on the

circuit. *See Hassoun Decl.* (Ex. 1006), at ¶¶ 70-73; *see also Smith* (Ex. 1005) at [0008] (noting that "the bidirectional converter may be controlled very precisely so as to enable precise delivery of power and energy to the desired load….).

iii. Claim 8.

8[P] A control apparatus comprising:

To the extent the preamble is limiting, *Smith* teaches a control apparatus as claimed and, in particular, a microcontroller with digital signal processing functionality. *See Smith* (Ex. 1005) at [0097], [0099], Figs. 19, 22; *see also supra* at Claim 1[P].

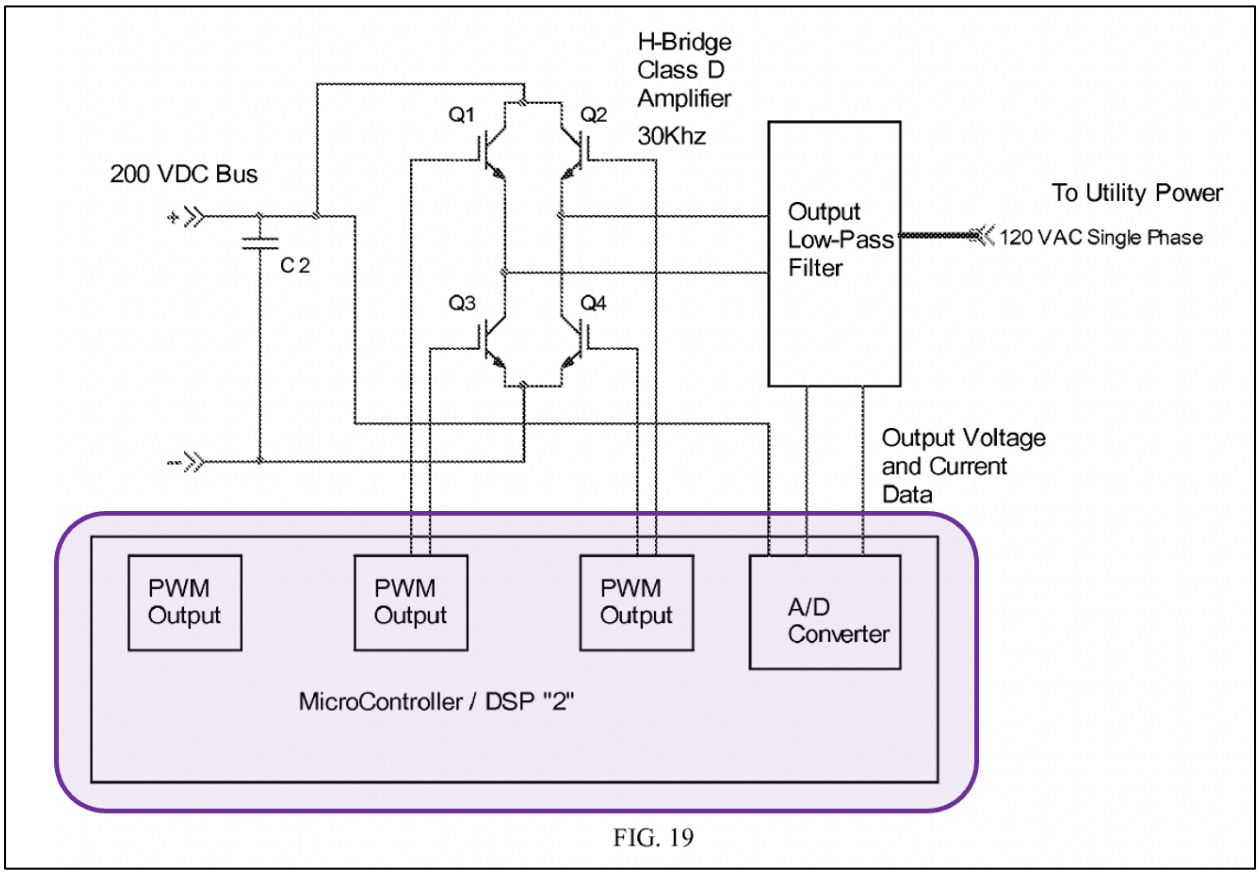


FIG. 19

See id. at Fig. 19 (color emphasis added).

[8(a)] a control stage configured to control an output stage adapted to operate in at least a first operating state and a second operating state, the output stage including:

Smith describes and illustrates at least one control stage as part of the control apparatus, and the control stage is configured to control the output stage. *See id.* at [0097], [0099]; *see also id.* at Figs. 19, 22. In particular, *Smith* describes and illustrates the microcontroller, which provides PWM outputs (shown in purple below) that are used to control the switches in the output stage (shown in blue below) of the circuit:

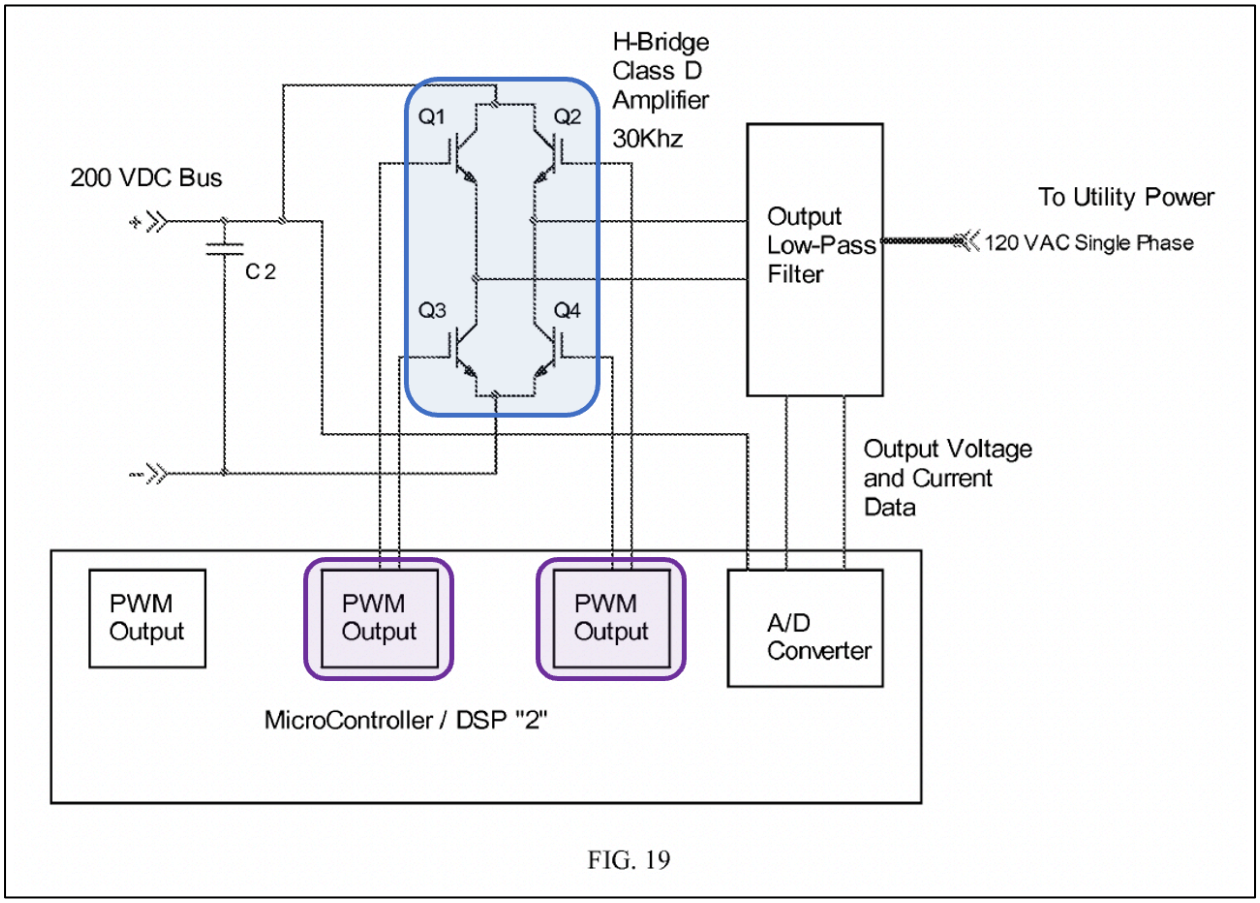


FIG. 19

See id. at Fig. 19 (color emphasis added). As already discussed above with respect to Claim 1, *Smith* also describes and illustrates two operating states. In the first operating state, the input/output terminals at the top of the H-bridge are used as input from a DC power source, and the input/output terminals on the branches of the H-bridge are used as AC output. *See id; see supra* at Claim 1[P]. One operating state is illustrated in Figure 19, which is annotated below to highlight the relevant portions of the circuit, with the input terminals in green, and the output terminals in red:

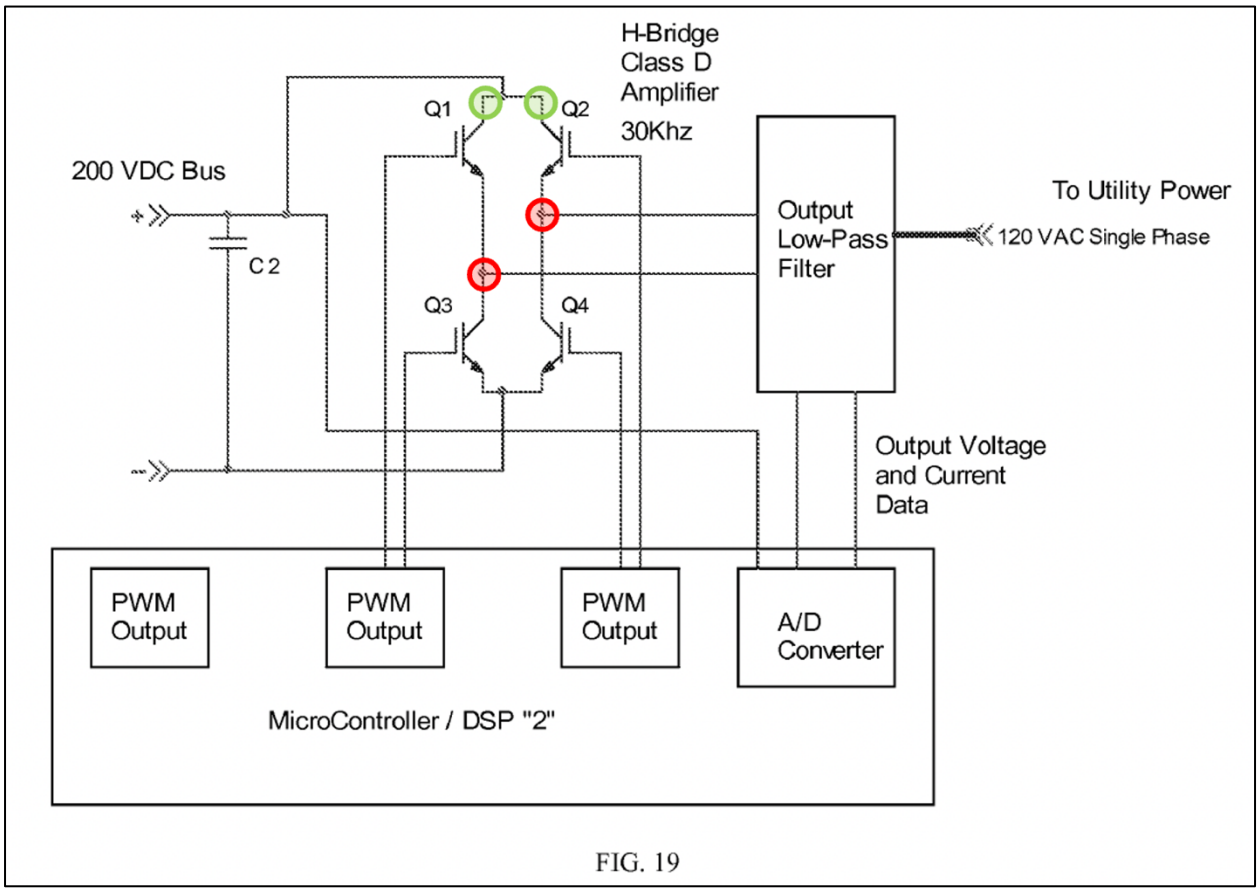


FIG. 19

Smith. at Fig. 19 (color emphasis added).

Another operating state where the output stage is used as a bridge rectifier is illustrated in Figure 22. *See id.* at [0099]; Fig. 22. Here, the input/output are now reversed, with the terminals on the top of the H-bridge used as DC output (shown in red below), and the terminals on the branches of the H-bridge used as AC input (shown in green below):

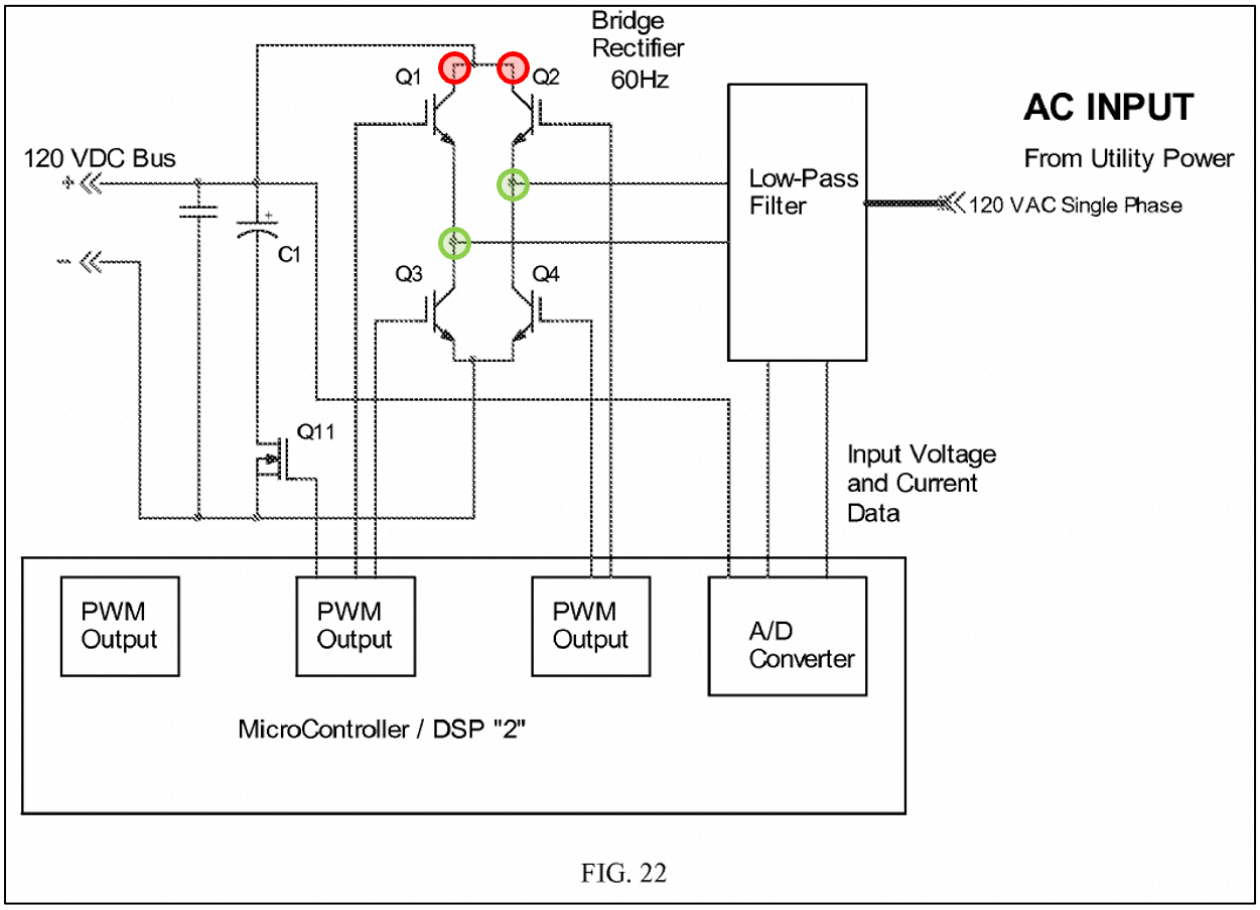


FIG. 22

Id. at Fig 22 (color emphasis added).

[8(a)(i)] a first, a second, a third and a fourth configurable input/output terminals; and

Smith discloses the claimed input/output terminals. *See supra* at Claim 1(a); *see also Smith* at [0097], [0099]; Figs. 19, 22.

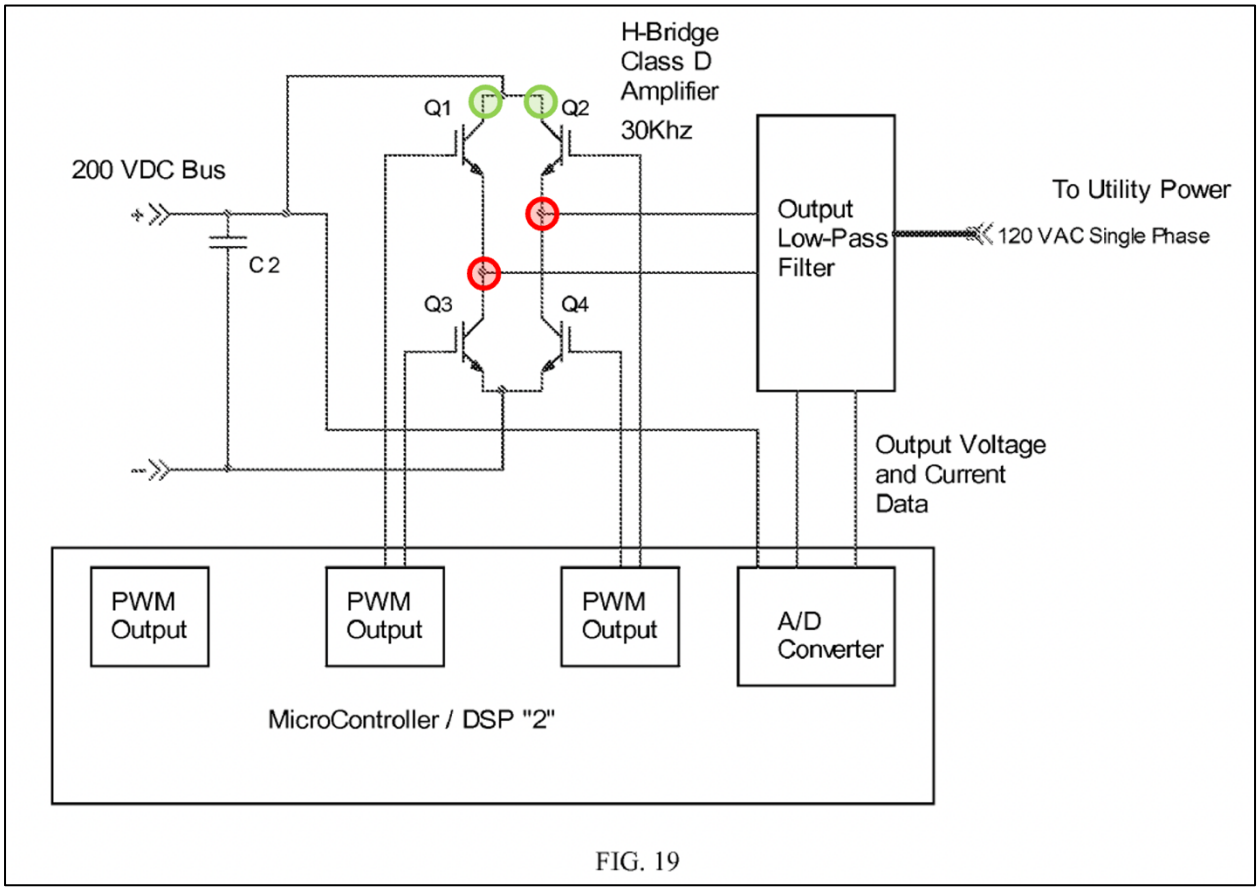


FIG. 19

Id. at Fig. 19 (color emphasis added).

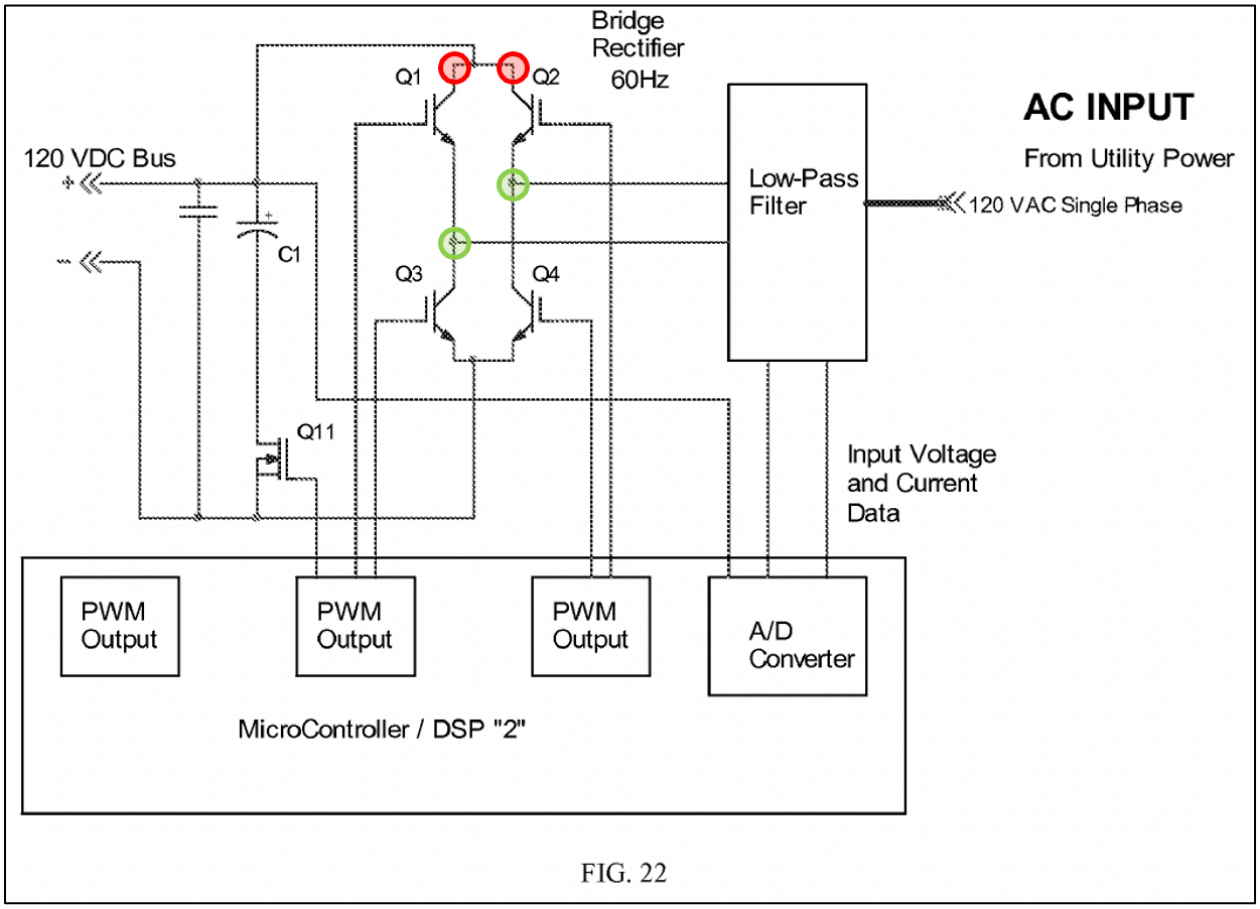


FIG. 22

Id. at Fig 22 (color emphasis added).

[8(a)(i)] a first, a second, a third, and a fourth switches, each having a first main terminal, a second main terminal and a control terminal, the control terminal being adapted to receive a control signal for controlling the open or closed state of the switch,

Smith discloses the claimed switches. *See supra* at Claim 1(b); *see also Smith* at [0097], [0099]; Figs. 19, 22.

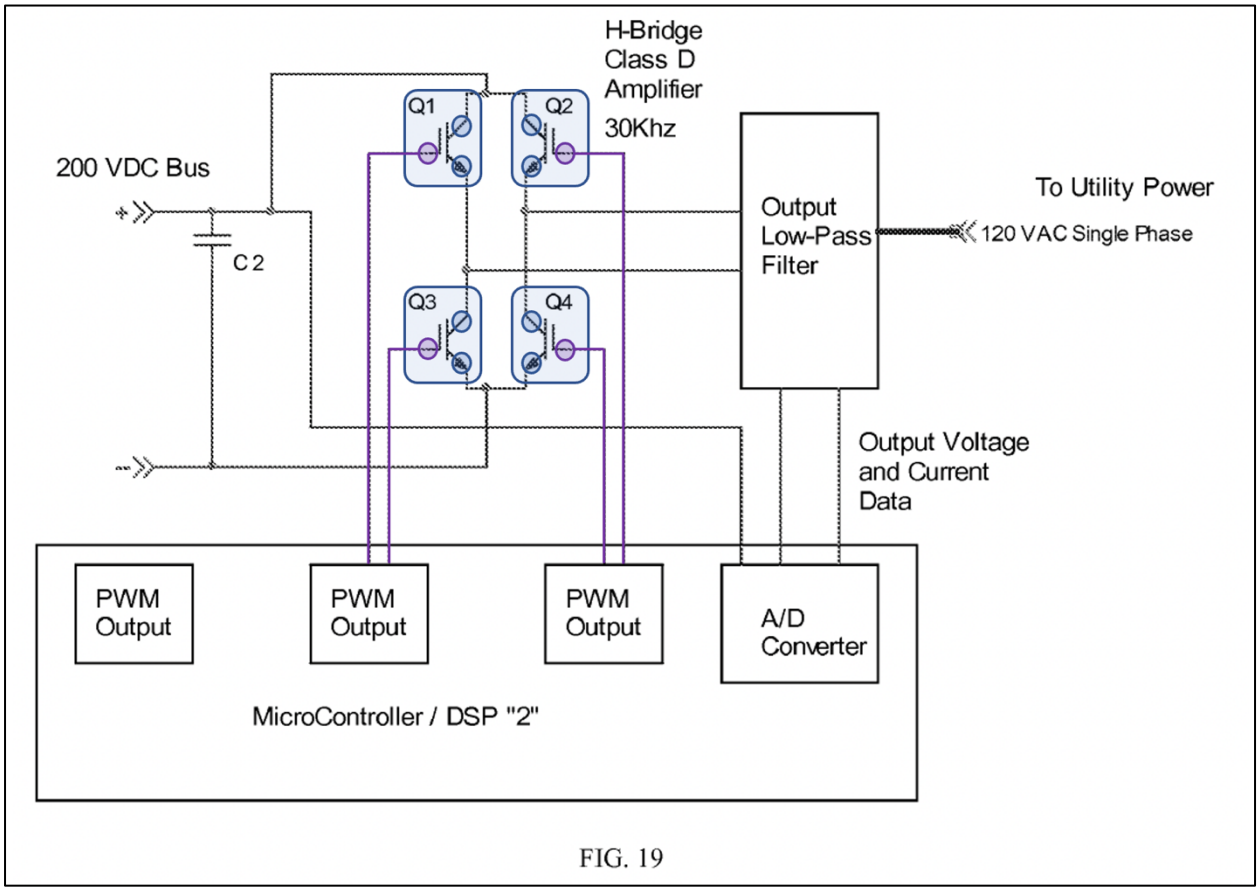


FIG. 19

Id. at Fig 19 (color emphasis added).

[8(b)(i)] wherein, the first input/output terminal is connected to the first main terminal of the first switch;

Smith discloses this limitation. *See supra* at Claim 1(c)(i); *see also Smith* at [0097], [0099]; Figs. 19, 22.

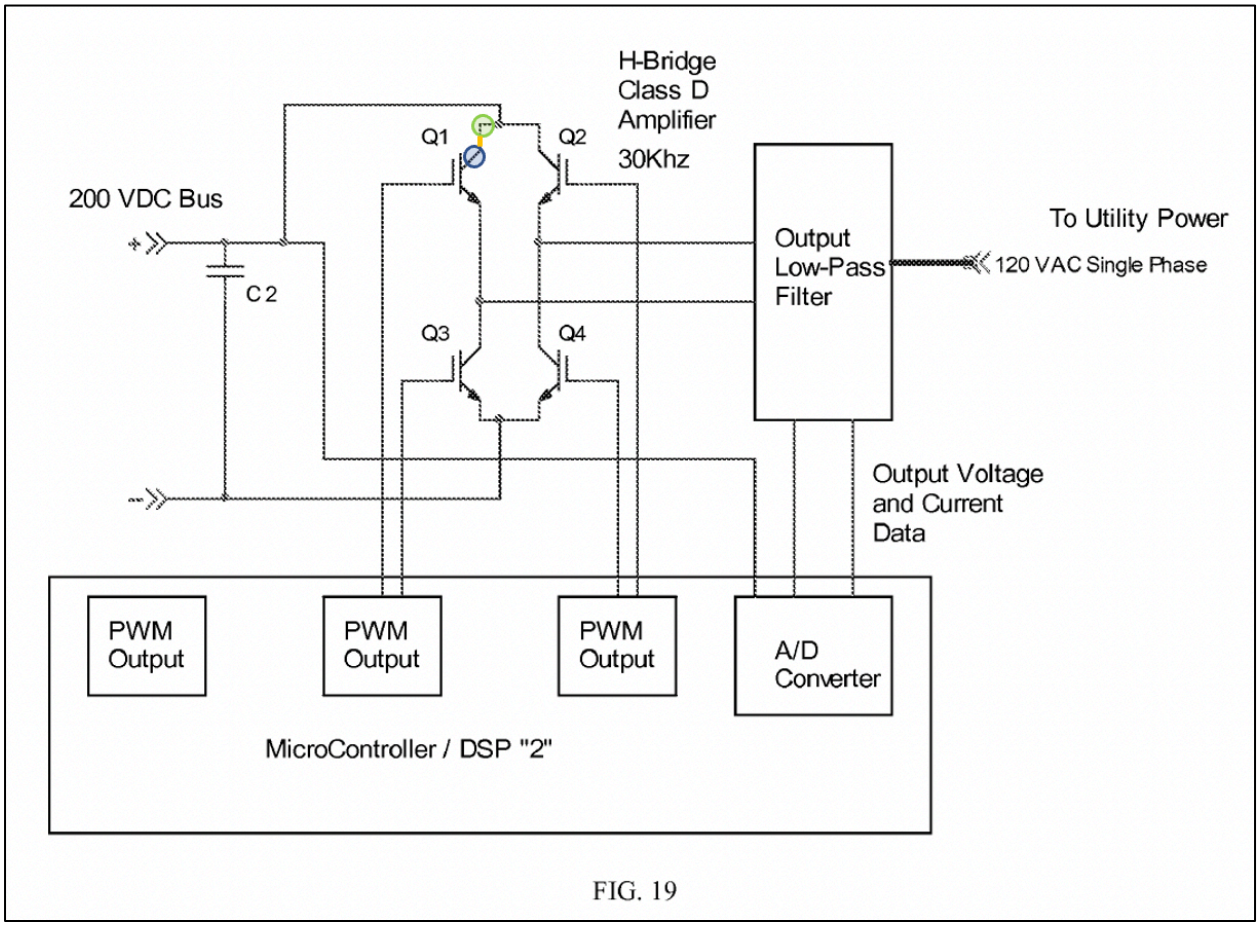


FIG. 19

Id. at Fig. 19 (color emphasis added).

[8(b)(ii)] the second input/output terminal is connected to the first main terminal of the second switch;

Smith discloses this limitation. *See supra* at Claim 1(c)(ii); *see also Smith* at [0097], [0099]; Figs. 19, 22.

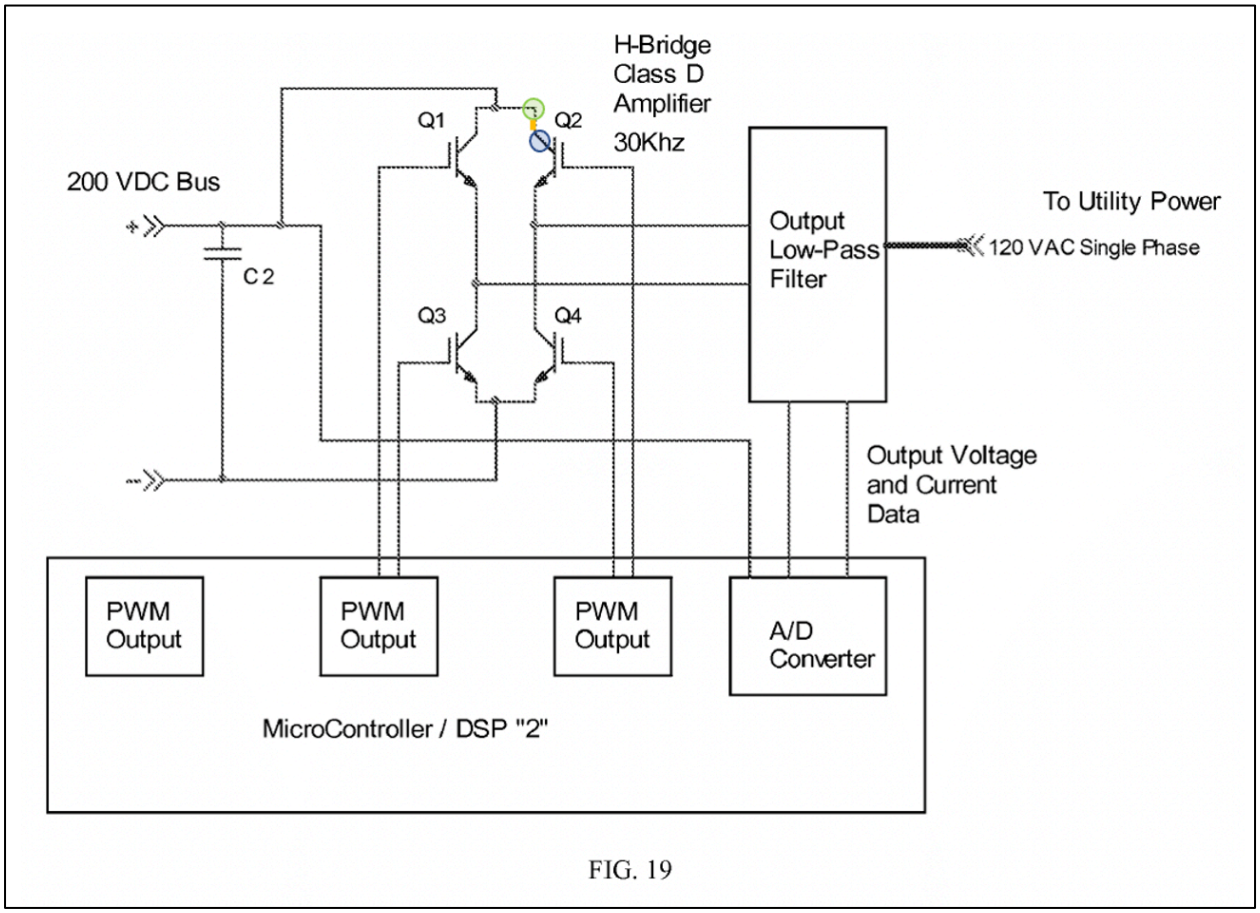


FIG. 19

Id. at Fig. 19 (color emphasis added).

[8(b)(iii)] the second main terminal of the first switch is connected to the first main terminal of the third switch through a first branch,

Smith discloses this limitation. *See supra* at Claim 1(c)(iii); *see also Smith* at [0097], [0099]; Figs. 19, 22.

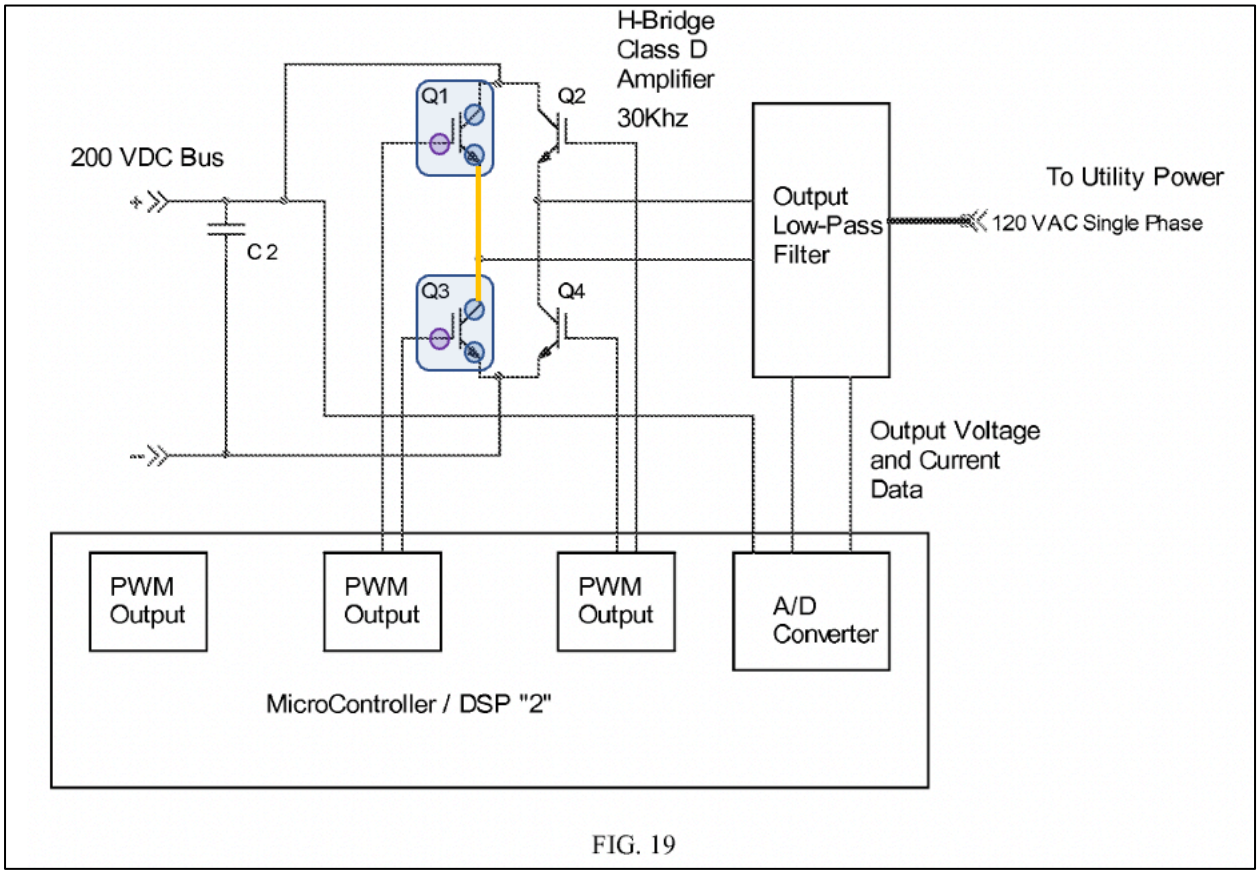


FIG. 19

Id. at Fig. 19 (color emphasis added).

[8(b)(iv)] the second main terminal of the second switch is connected to the first main terminal of the fourth switch through a second branch;

Smith discloses this limitation. *See supra* at Claim 1(c)(iv); *see also Smith* at [0097], [0099]; Figs. 19, 22.

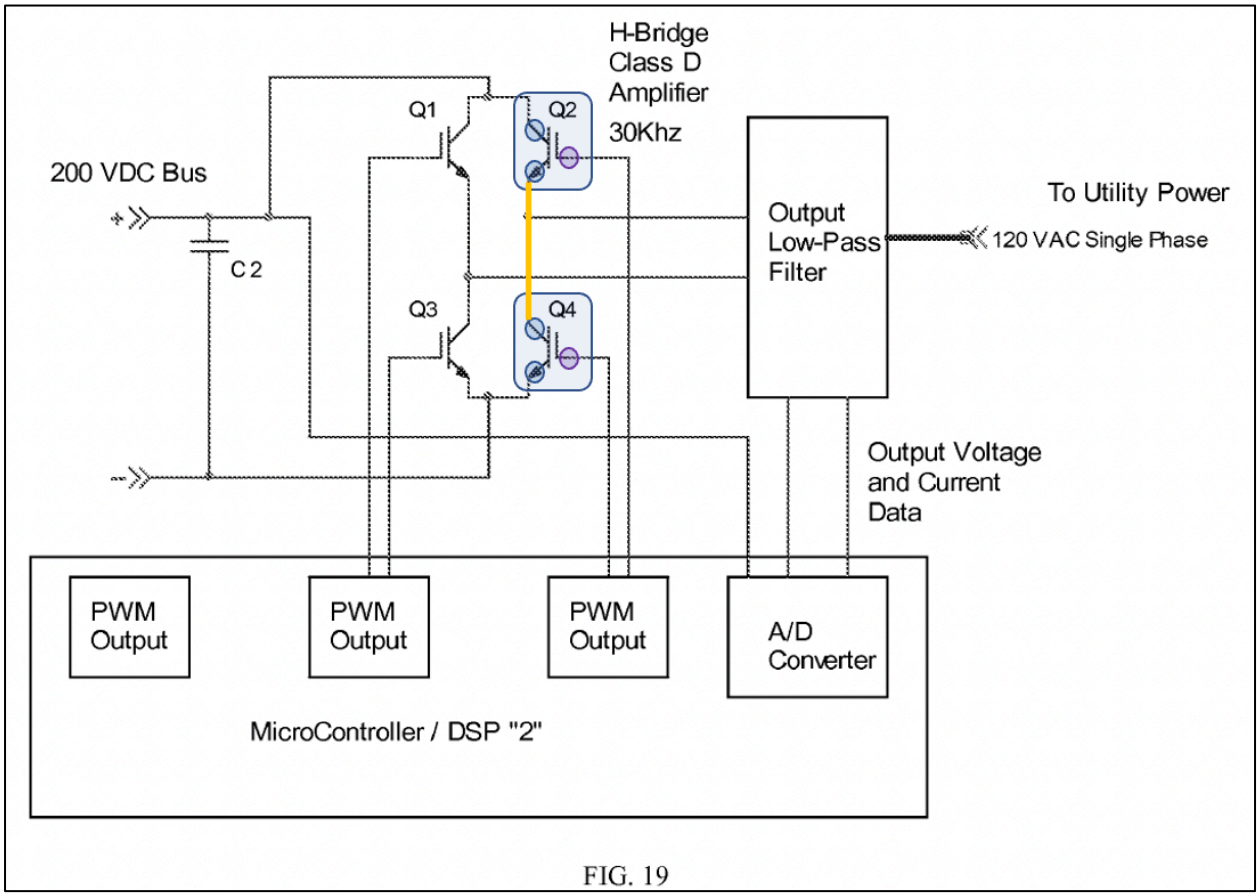


FIG. 19

Id. at Fig. 19 (color emphasis added).

[8(b)(v)] the third input/output terminal is connected to the first branch and the fourth input/output terminal is connected to the second branch;

Smith discloses this limitation. *See supra* at Claim 1(c)(v); *see also Smith* at [0097], [0099]; Figs. 19, 22.

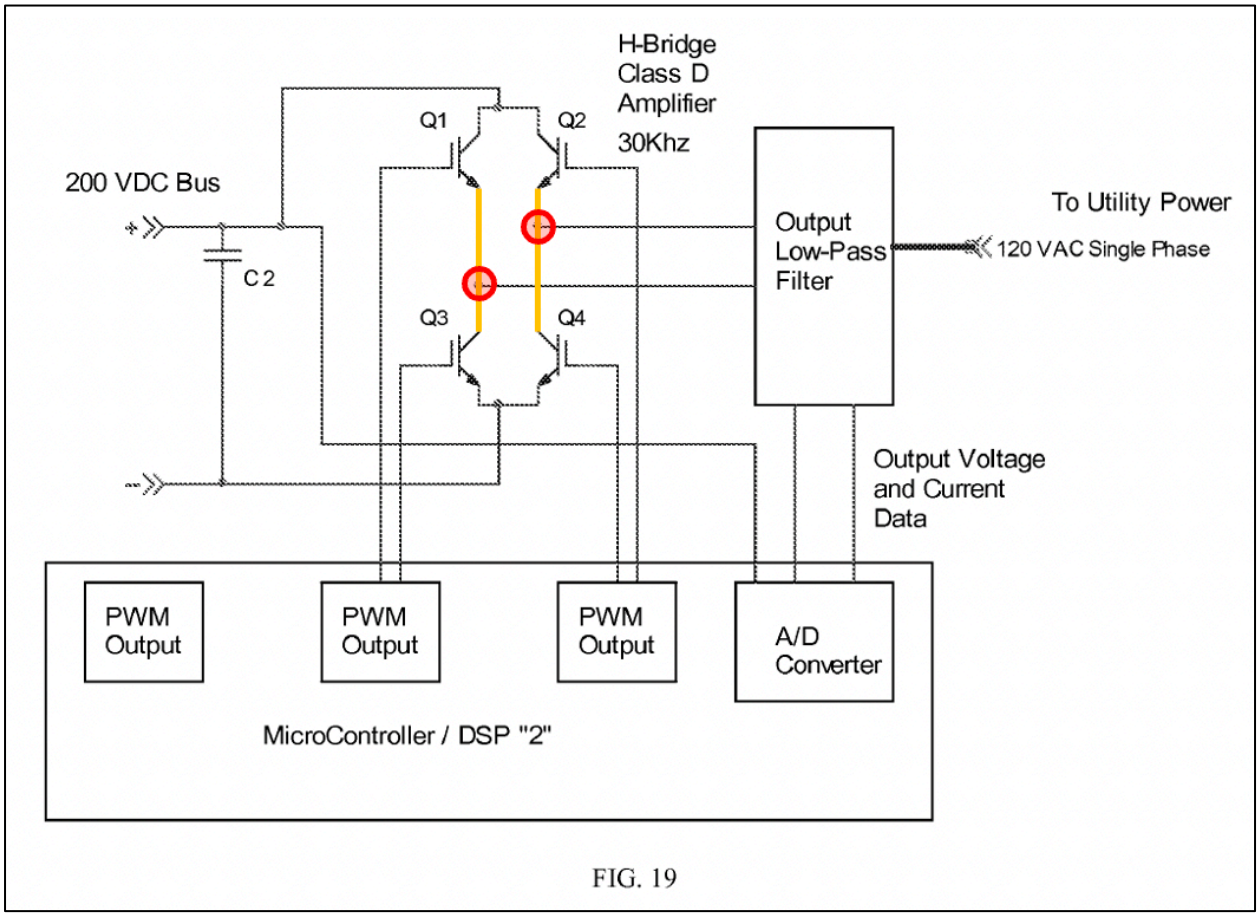


FIG. 19

Id. at Fig. 19 (color emphasis added).

[8(b)(vi)] the second main terminals of the third and fourth switches are both connected to a common node receiving a reference potential; and, wherein

Smith discloses this limitation. *See supra* at Claim 1(c)(vi); *see also Smith* at [0097], [0099]; Figs. 19, 22.

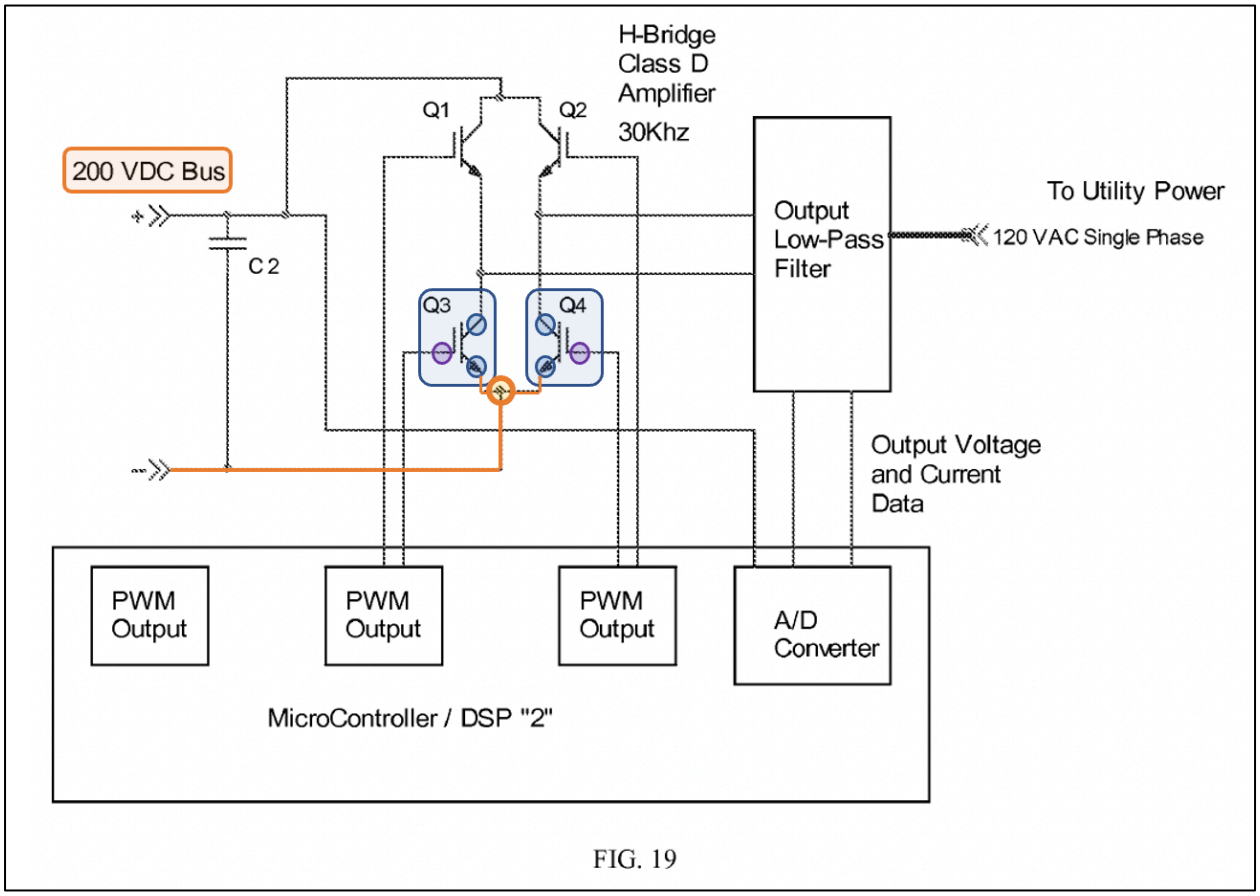


FIG. 19

Id. at Fig. 19 (color emphasis added).

[8(b)(vii)] when the first and second input/output terminals are configured to operate as input terminals, the third and fourth input/output terminal are configured to operate as output terminals; and,

Smith discloses this limitation. *See supra* at Claim 1(c)(vii); *see also Smith* at [0097], [0099]; Figs. 19, 22.

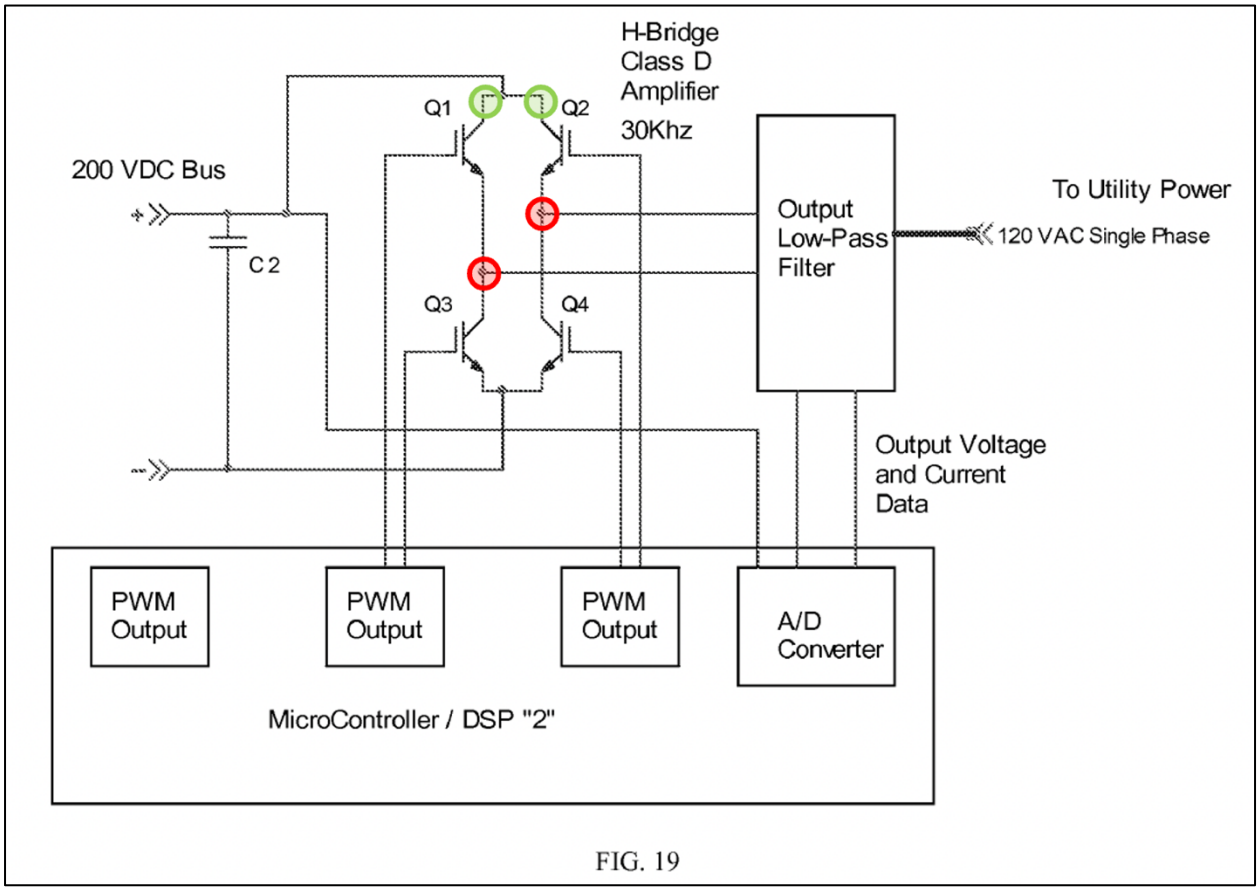


FIG. 19

Id. at Fig. 19 (color emphasis added).

[8(b)(viii)] when the first and second input/output terminals are configured to operate as output terminals, the third and fourth input/output terminals are configured to operate as input terminals; and, wherein,

Smith discloses this limitation. *See supra* at Claim 1(c)(viii); *see also Smith* at [0097], [0099]; Figs. 19, 22.

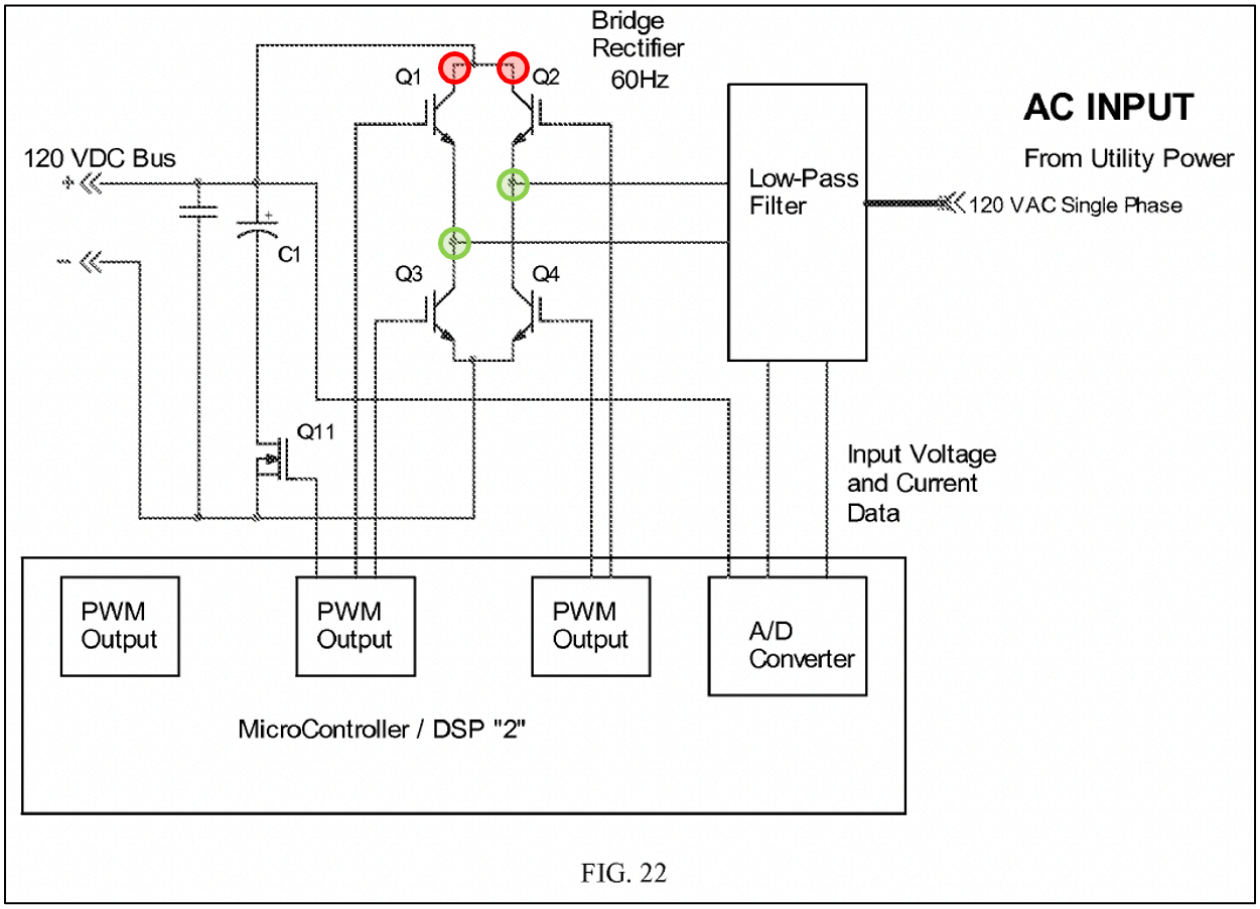


FIG. 22

Id. at Fig 22 (color emphasis added).

[8(b)(ix)] in the first operating state, the output stage is arranged in a first electrical configuration; and

Smith discloses this limitation. *See supra* at Claim 1(c)(ix); *see also Smith* at [0097], [0099]; Figs. 19, 22.

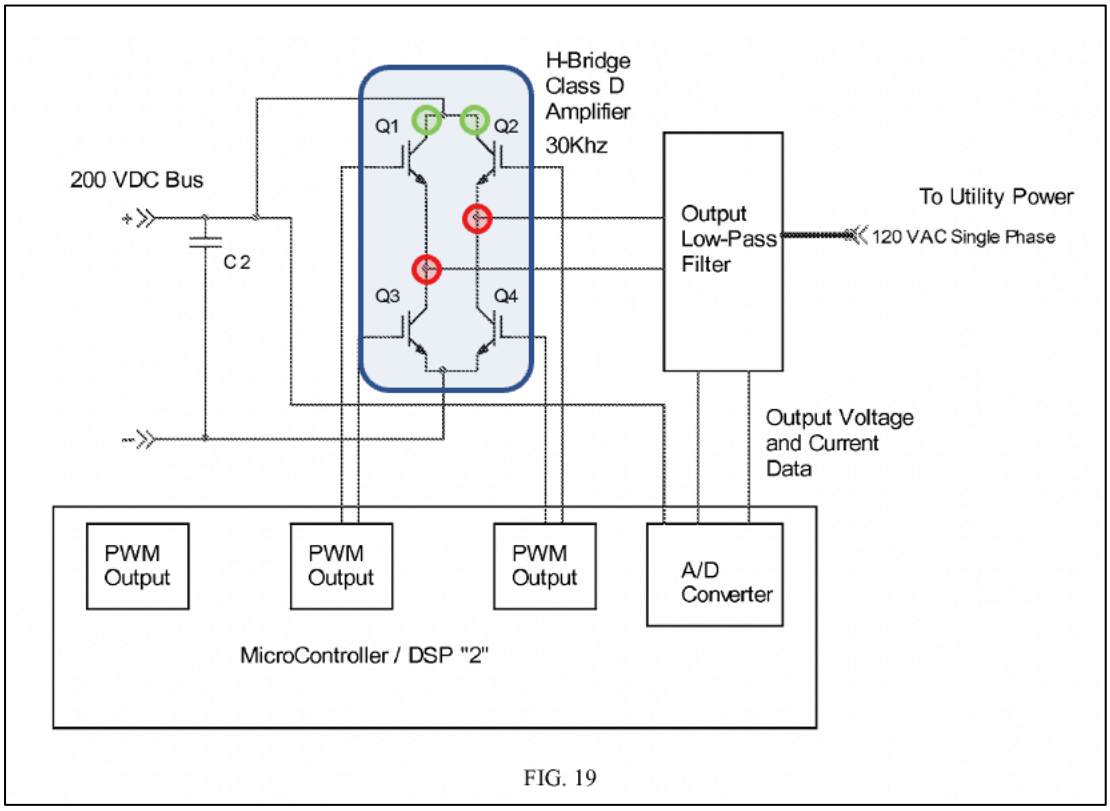


FIG. 19

Id. at Fig 19 (color emphasis added).

[8(b)(x)] in the second operating state wherein the output stage is arranged in a second electrical configuration different from the first configuration, and

Smith discloses this limitation. *See supra* at Claim 1(c)(x); *see also Smith* at [0097], [0099]; Figs. 19, 22.

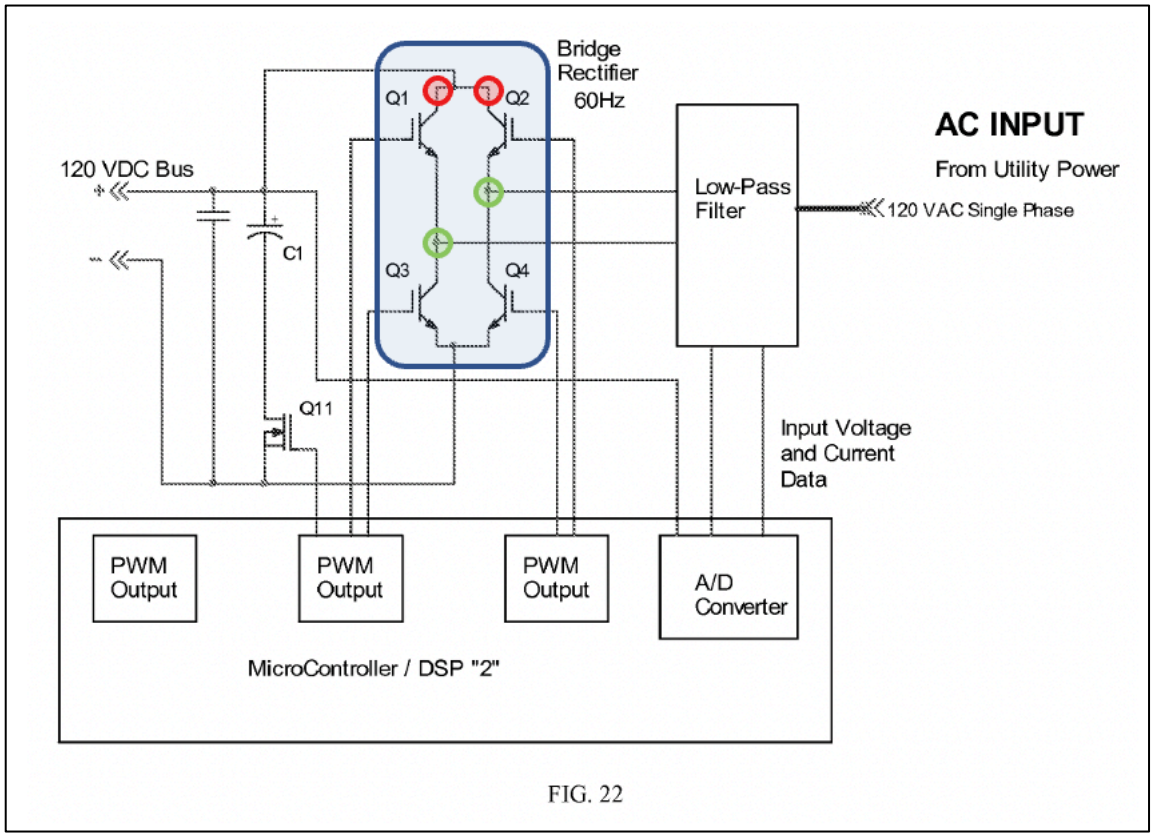


FIG. 22

Id. at Fig 22 (color emphasis added).

[8(b)(xi)] further wherein, in the first operating stage, the first and second input/output terminals are configured to operate as input terminals and are configured to be connected to a common node receiving a supply potential; and

Smith discloses this limitation. *See supra* at Claim 2(a); *see also Smith* at [0097], [0099]; Figs. 19, 22.

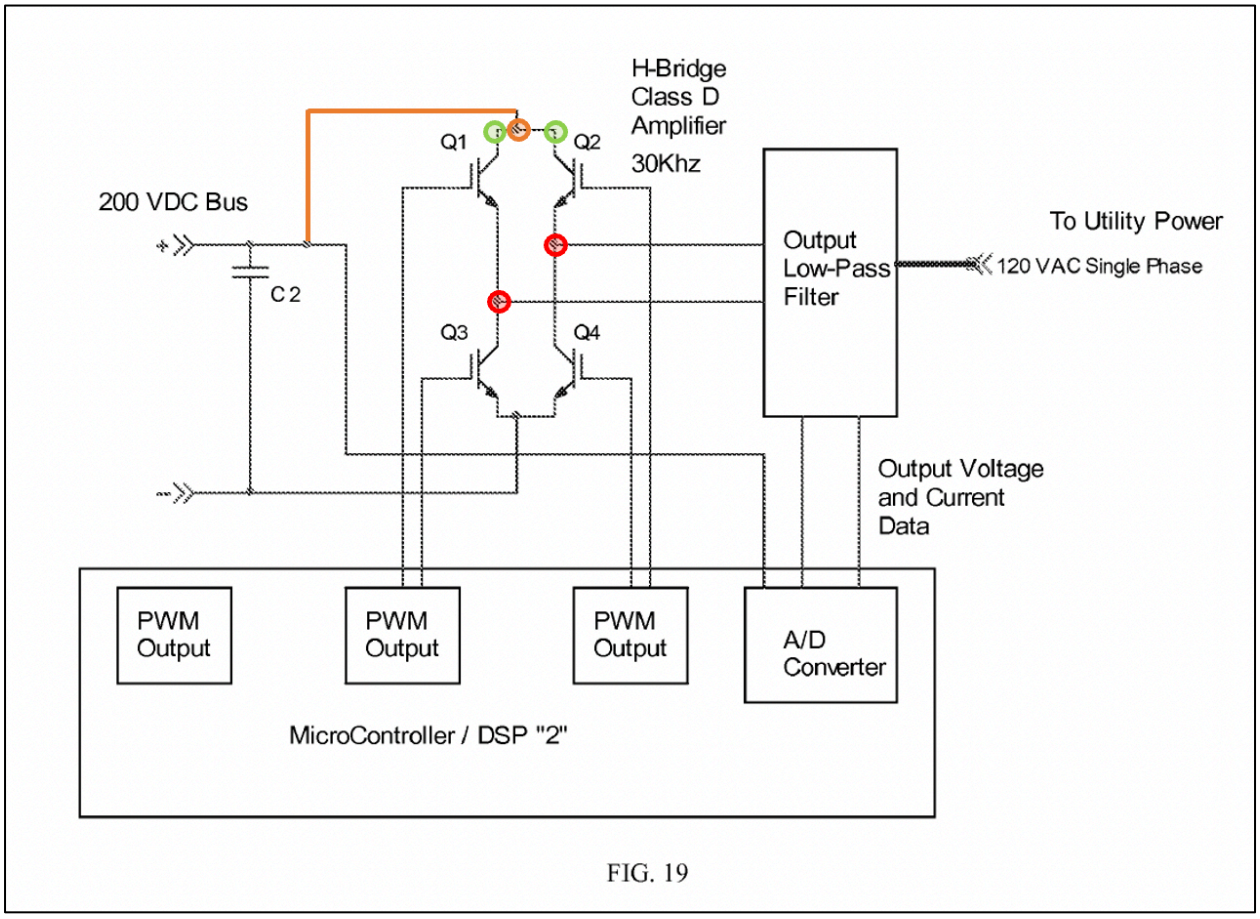


FIG. 19

Id. at Fig 19 (color emphasis added).

[8(b)(xii)] the third and fourth input/output terminals are configured to be connected to a load element.

Smith discloses this limitation. *See supra* at Claim 2(b); *see also Smith* at [0097], [0099]; Figs. 19, 22.

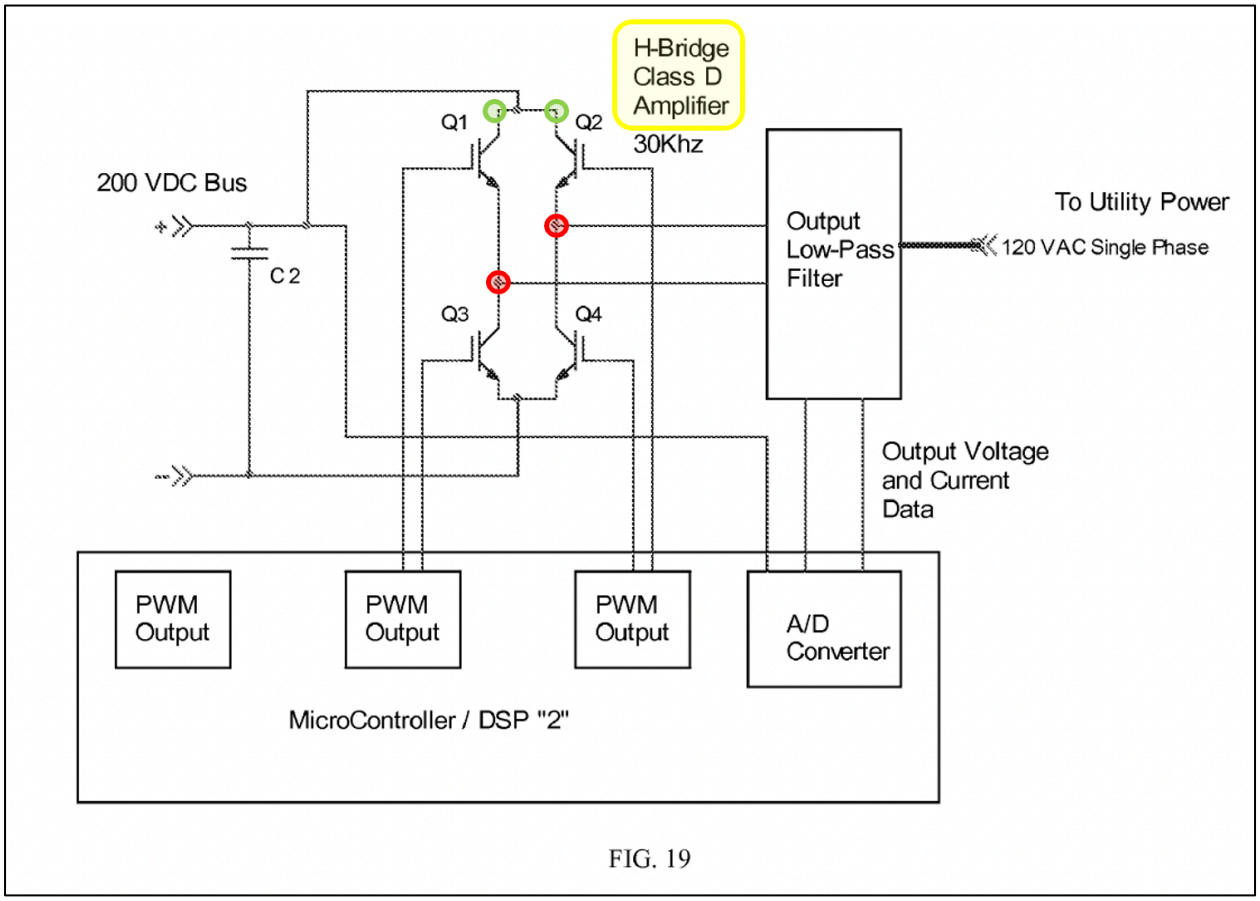


FIG. 19

See id. at Fig. 19 (color emphasis added).

iv. Claim 10.

10. The control apparatus of claim 8, wherein the control stage is adapted to control the output stage by generating control signals for controlling the first, second, third and fourth switches through their respective control terminals.

Smith illustrates and describes a control stage that is adapted to control the output stage by generating control signals (through the Pulse Width Modulator (PWM Outputs) for controlling the switches through their respective control terminals.

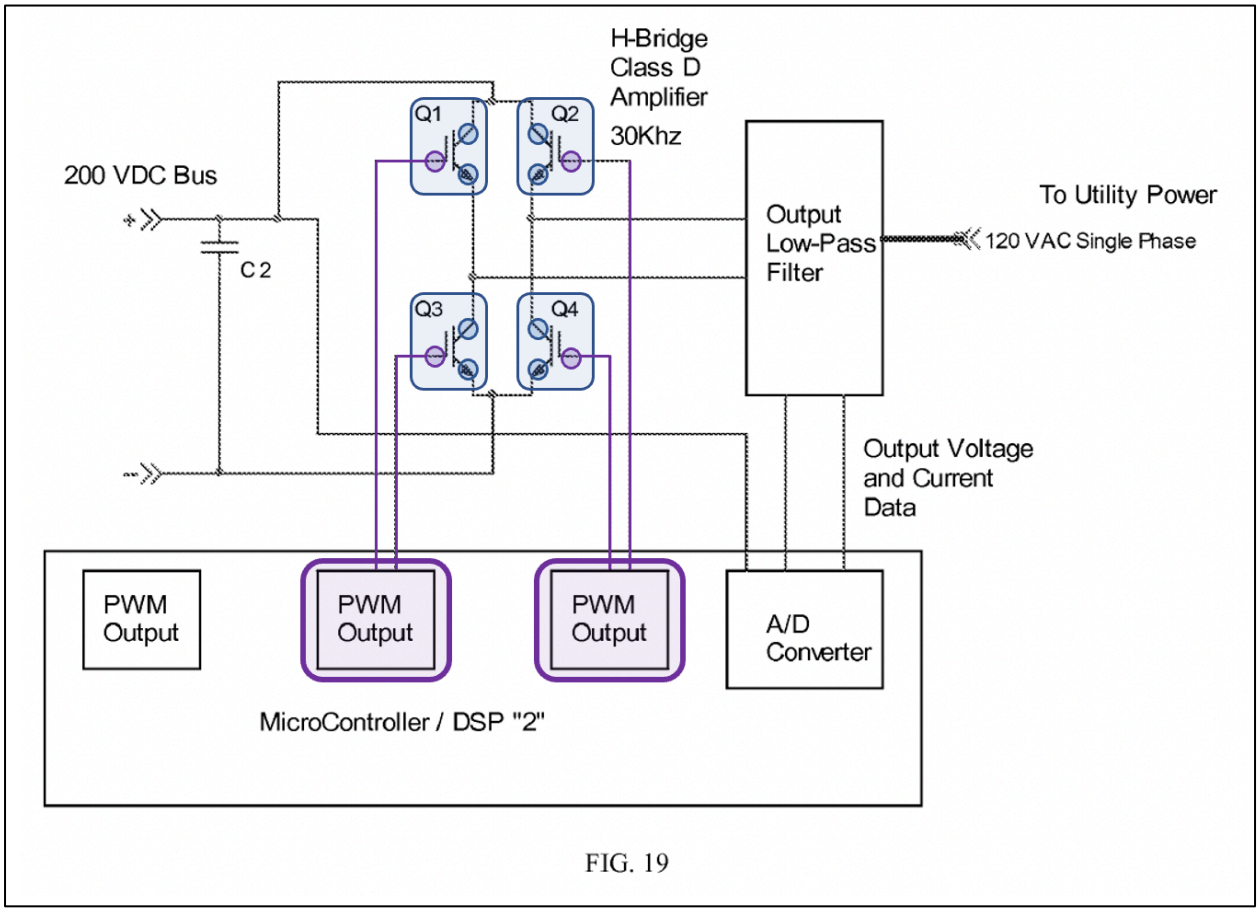


FIG. 19

See id. at Fig. 19 (color emphasis added); *see also id.* at [0097], [0099]. As described in *Smith* the H-bridge output stage "may also include Q1-Q4, which may receive PWM [Pulse Width Modulator] outputs from a DSP [Digital Signal Processor]." *Id.* at [0097]. "The DSP may control the drive signals provided to the 'H' bridge." *Id.*; *see also Hassoun Decl.* at ¶¶ 76-79 (describing control functionality for illustrated transistors). Similarly, with respect to the second operating state described and illustrated in *Smith* in Figure 22, *Smith* notes that the switches Q1-Q4 "may receive PWM outputs from one or more DSP, such as DSP 2. DSP 2 may thus control the 'H' bridge DC output." *Id.* at [0099]. As illustrated in Figures 19 and 22, the signal

coming from the control stage to switches Q1-Q4 is communicated through the respective control terminals of the switches. *See id.* at Figs. 19, 22.

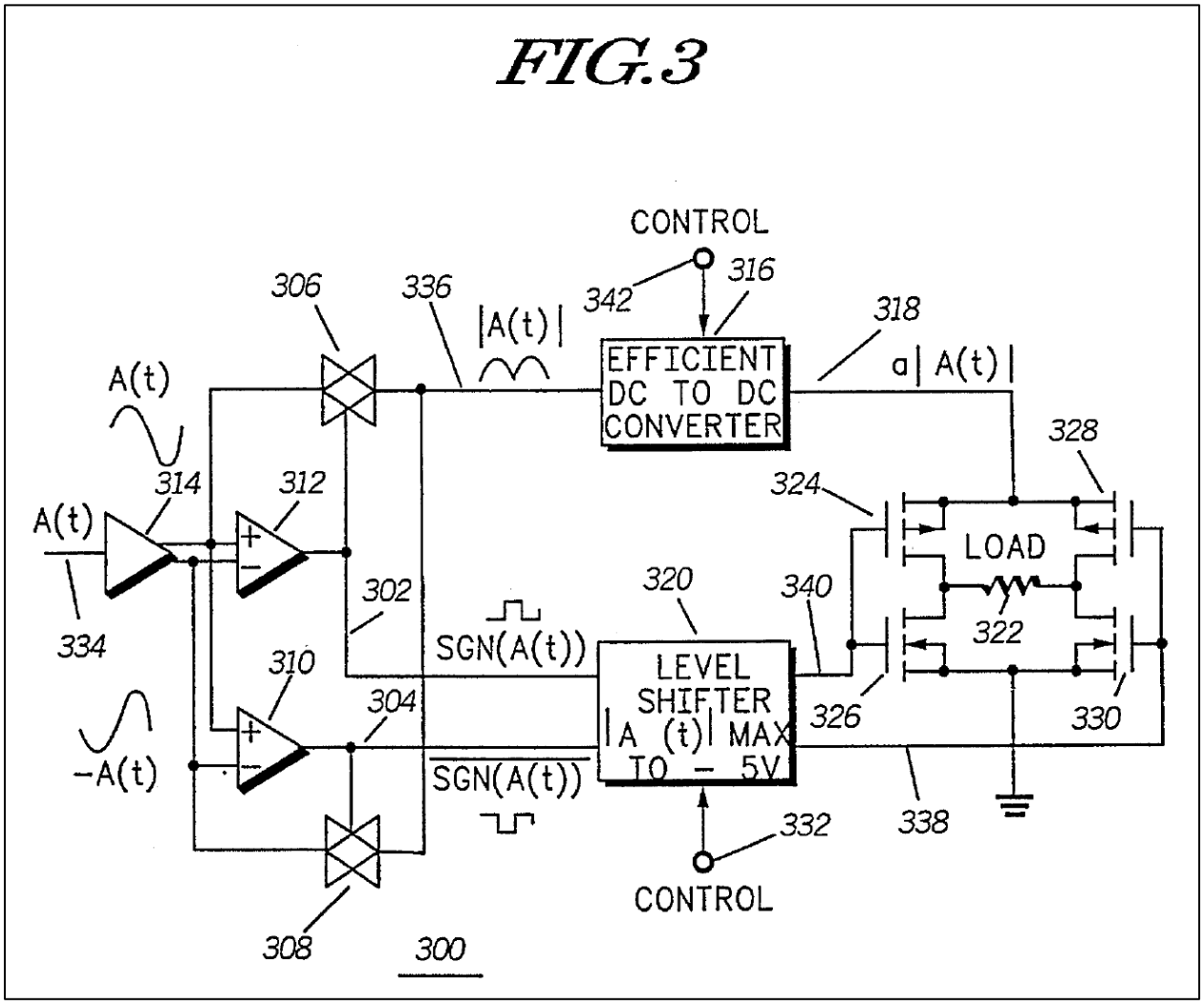
B. Ground 2: Claim 14 is obvious under AIA 35 U.S.C. § 103 over *Smith* in view of *Stengel*

Overview of Stengel

United States Patent No. 5,506,493 to Stengel ("*Stengel*") was filed on March 10, 1995, and issued on April 9, 1996, and is prior art to the '400 Patent under at least 35 U.S.C. § 102(a)(1) (AIA). *See generally Stengel* (Ex. 1005). *Stengel* was not cited or considered during prosecution of the '400 Patent. *See generally '400 Patent* (Ex. 1001).

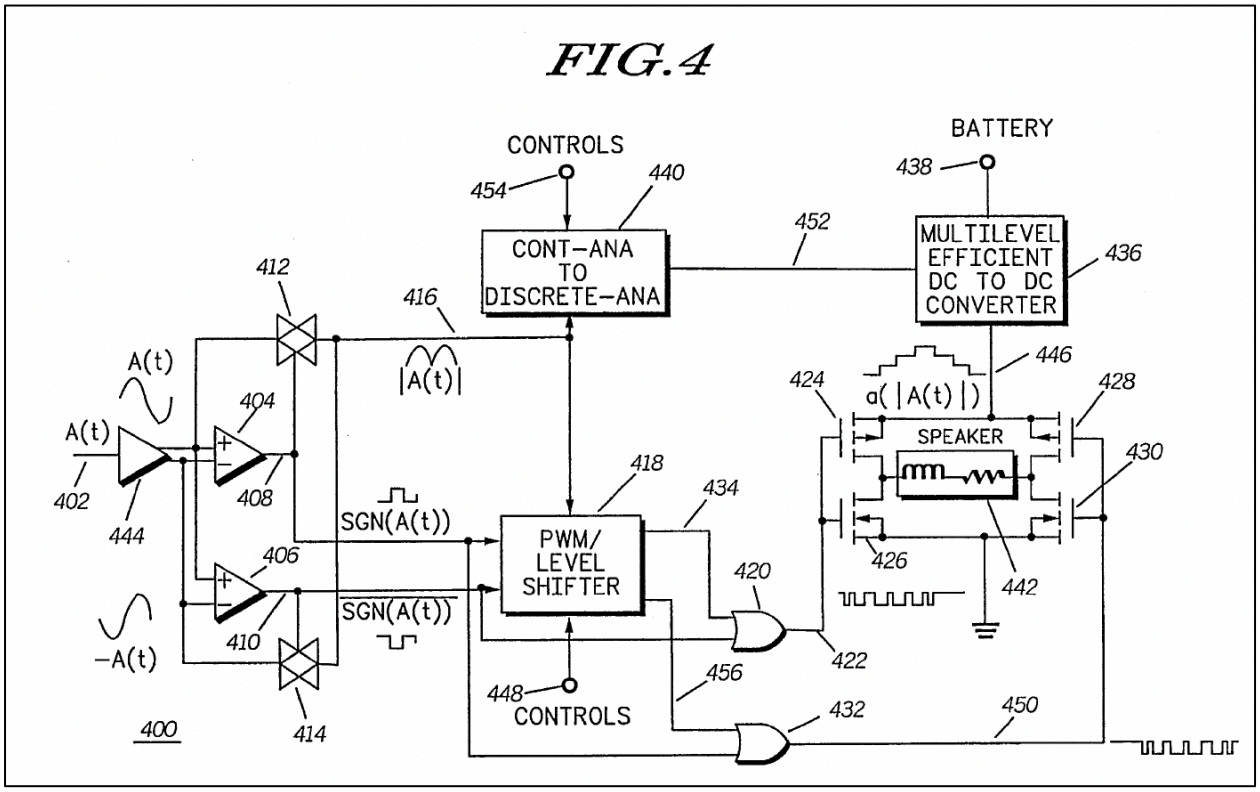
Stengel is generally directed to an audio amplifier that uses a switching voltage regulator. *See Stengel* (Ex. 1005) at 1:14-16. In particular, *Stengel* describes a voltage regulator that includes a controller connected to several switches used to "select between a first current loop in which an energy storage device is charged by an input supply and a second loop in which the energy storage device is coupled to the output terminal . . . ." *Id.* at Abstract. *Stengel* also describes using this voltage regulator with a first switching audio amplifier that "provide[s] a continuously variable output voltage in order to provide for high quality amplification which is independent of the volume setting," and a second switching audio amplifier that "provides discrete voltage levels to a full wave bridge in order to provide improved audio output." *Id.* (internal component numbers omitted).

The first audio amplifier described in *Stengel* is illustrated in Figure 3:



Id. at Fig. 3. This first audio amplifier circuit is a first operating state that "provides for improvements in both dynamic range and audio distortion without the need of an isolating transformer." *Id.* at 5:36-38.

The second audio amplifier described in *Stengel* is illustrated in Figure 4:



Id. at Fig. 4. This second audio amplifier circuit illustrates a second operating state of the circuit. *See id.* at 5:39-47. Unlike the first operating state, which continuously changes the input voltage being sent into the bridge, the second operating state provides for discrete voltage level to be sent to the bridge that are dependent on the input audio signal, the desired volume, and the supply voltage level. *Id.*

Stengel is analogous art because it is in the same field of endeavor as the ’400 Patent. *Hassoun Decl.* (Ex. 1006) at ¶¶ 58-59. As noted above, the field of endeavor for the ’400 Patent is reconfigurable output stage circuits. *See ’400 Patent* (Ex. 1001) at 1:5-7 (defining the technical field as “relat[ing] generally to output stage circuits, and more especially to a reconfigurable output stage.”). *Stengel* is within this same

field of endeavor. *See*, *e.g.*, *Stengel* (Ex. 1005) at Abstract (discussing output stage circuits that can be configured into multiple states using a switching means); 4:35-5:38 (describing a first switching audio amplifier); 5:39-7:20 (describing a second switching audio amplifier circuit); Figs. 3-4 (illustrating first and second audio amplifier circuit configurations); *see also Hassoun Decl.* (Ex. 1006), at ¶¶ 58-59. *Stengel* is also analogous art because it is reasonably pertinent to the problem that the '400 Patent purports to solve. *Hassoun Decl.* (Ex. 1006), at ¶¶ 58-59. The '400 Patent describes a problem in that the prior art is purportedly inefficient and costly because special purpose circuitry is used for different output needs. *See '400 Patent* (Ex. 1001) at 1:19-40. The '400 Patent purports to solve this problem with a circuit that can be shared by multiple systems, such as a Class-D amplifier and a DC-DC boost converter. *See id.* at 1:44-56. *Stengel* identifies a similar problem and teaches a similar solution using H-bridge circuitry to accommodate various audio amplifier operating states. *See Stengel* (Ex. 1005) at 1:56-67 (noting the benefit of the described solution in decreasing the expense and size of the audio amplifier circuit); 4:35-5:38 (describing a first switching audio amplifier); 5:39-7:20 (describing a second switching audio amplifier circuit); Figs. 3-4 (illustrating first and second audio amplifier circuit configurations); *see also Hassoun Decl.* (Ex. 1006), at ¶¶ 58-59.

i. Claim 14.

14[P] A device comprising:

To the extent the preamble is limiting, *Smith* teaches a device as claimed. *See id.* at [0097], [0099], Figs. 19, 22; *see also supra* at Claim 1[P].

[14(a)] a circuit comprising a control apparatus that includes a control stage configured to control an output stage adapted to operate in at least a first operating state and a second operating state, the output stage including:

Smith teaches a control apparatus as claimed and, in particular, a microcontroller with digital signal processing functionality. *See id.* at [0097], [0099], Figs. 19, 22; *see also supra* at Claim 1[P].

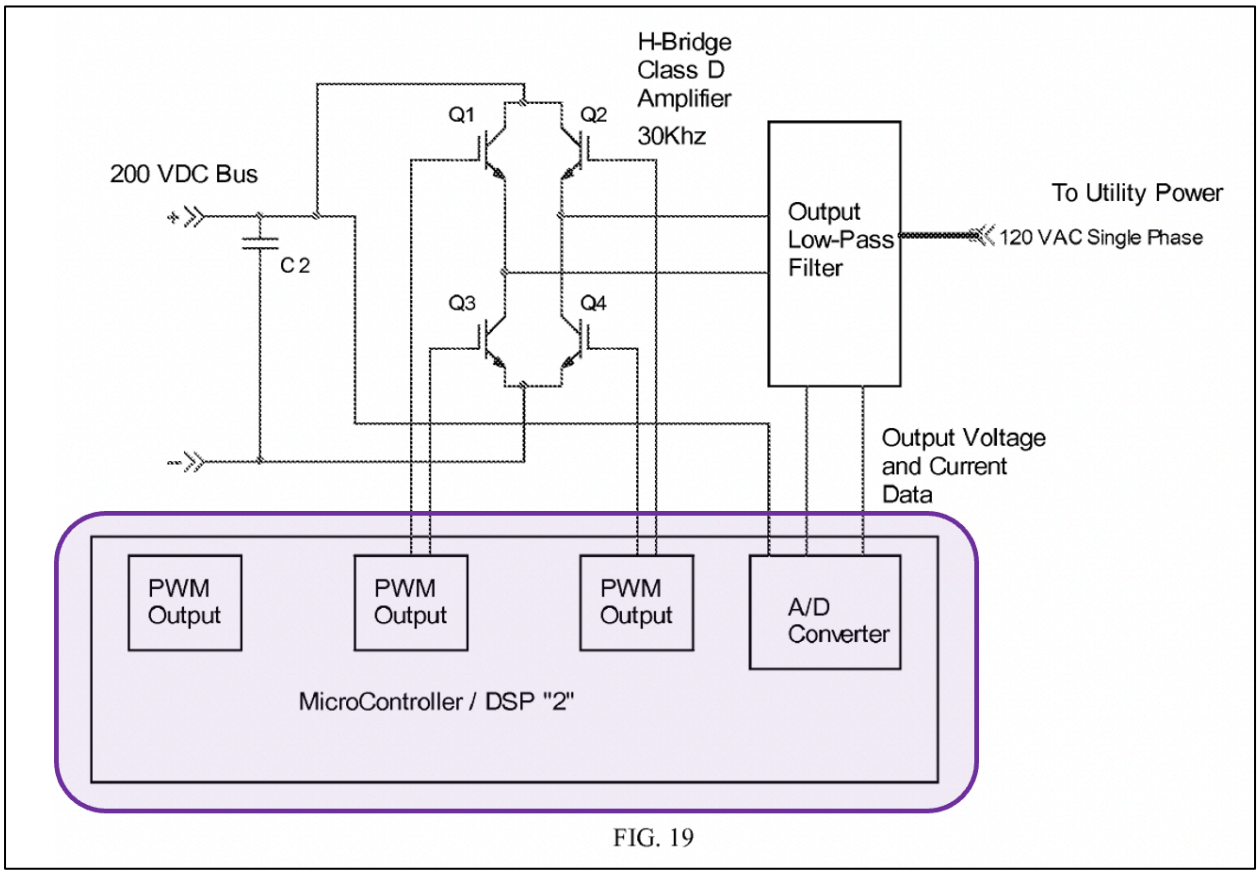


FIG. 19

See id. at Fig. 19 (color emphasis added).

Smith also describes and illustrates at least one control stage as part of the control apparatus, and the control stage is configured to control the output stage. *See id.* at [0097], [0099]; *see also id.* at Figs. 19, 22. In particular, *Smith* describes and illustrates the microcontroller providing PWM outputs (shown in purple below) that are used to control the switches in the output stage (shown in blue below) of the circuit:

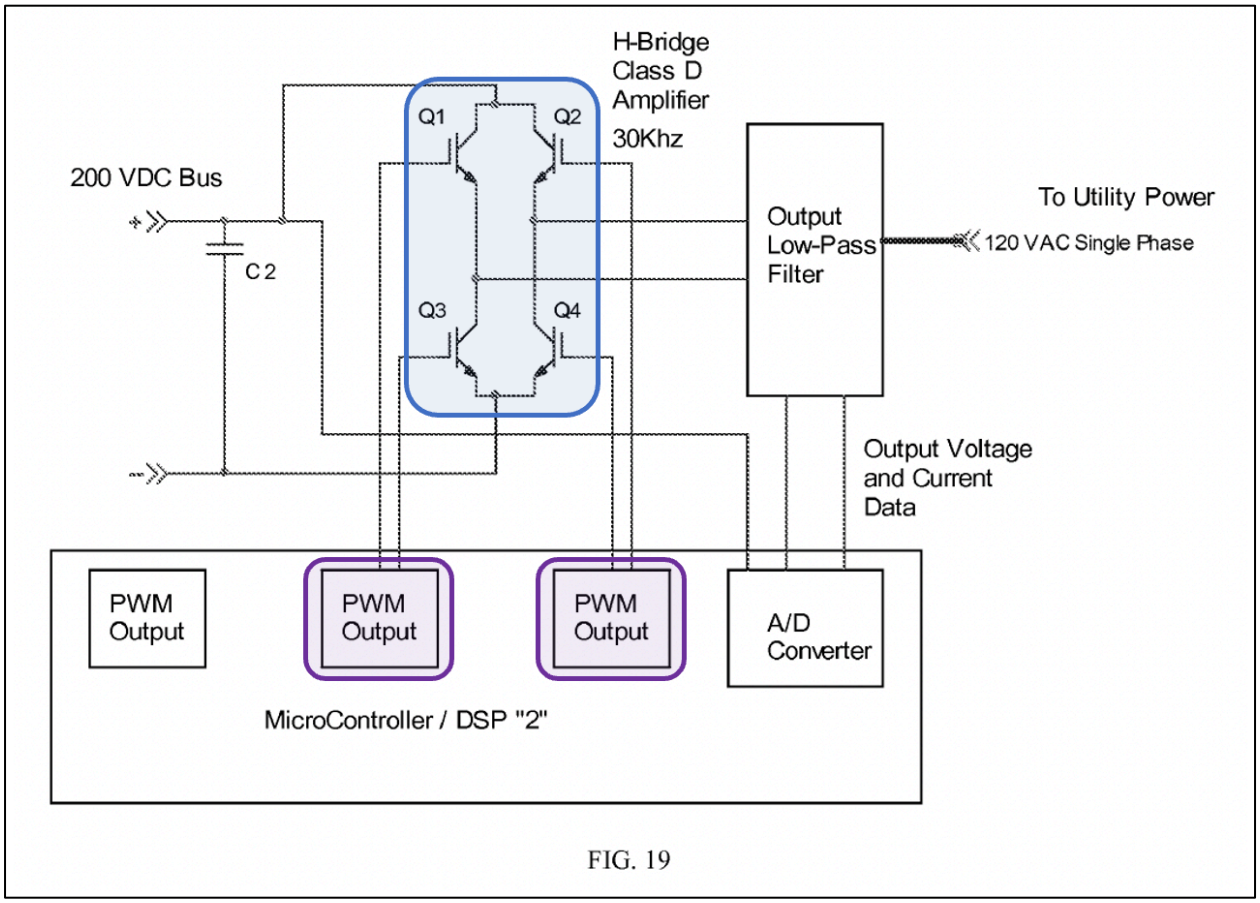


FIG. 19

See id. at Fig. 19 (color emphasis added). *Smith* also describes and illustrates two operating states. In the first operating state, the input/output terminals at the top of the H-bridge are used as input from a DC power source, and the input/output

terminals on the branches of the H-bridge are used as AC output. *See id.* One operating state is illustrated in Figure 19, which is annotated below to highlight the relevant portions of the circuit, with the input terminals in green, and the output terminals in red:

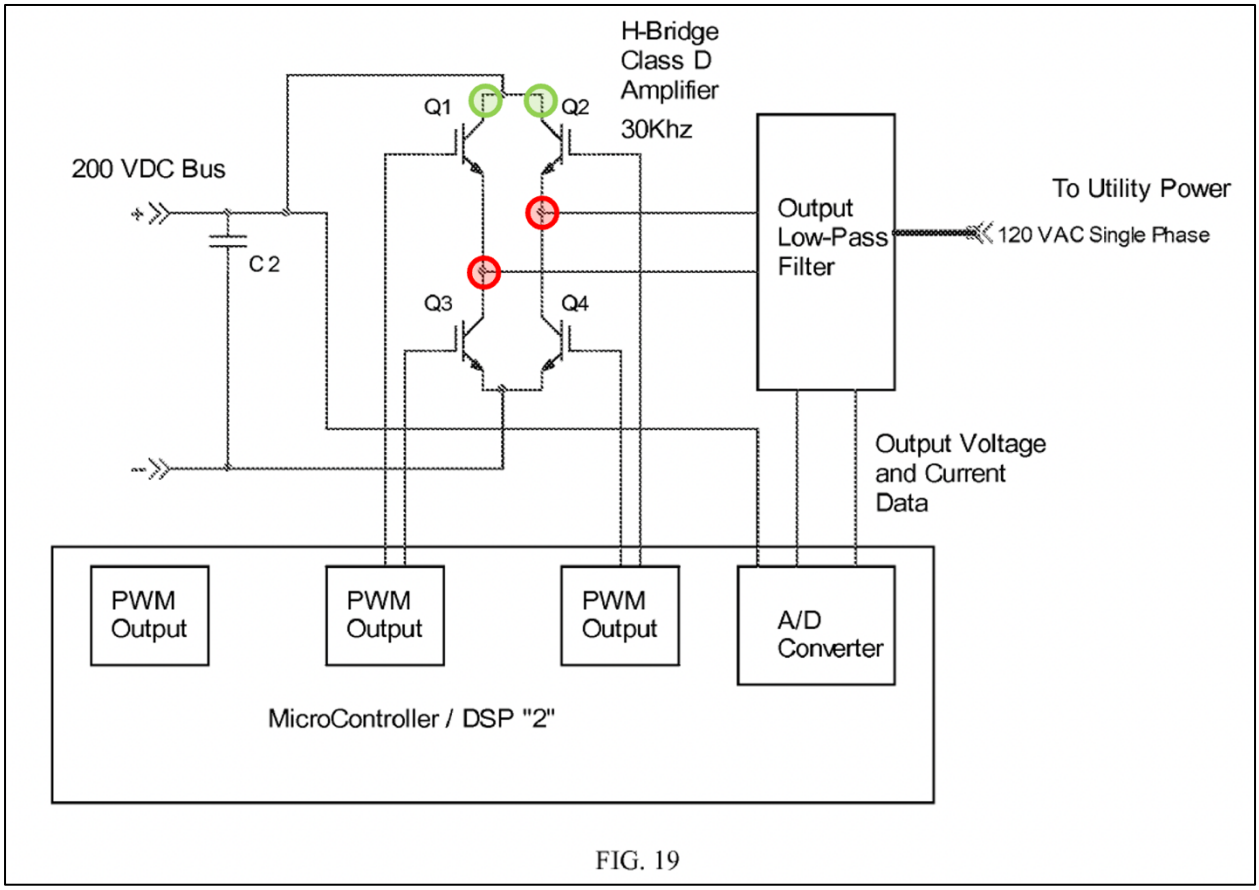


FIG. 19

Id. at Fig. 19 (color emphasis added).

Another operating state where the output stage is used as a bridge rectifier is illustrated in Figure 22. *See id.* at [0099]; Fig. 22. Here, the input/output are now reversed, with the terminals on the top of the H-bridge used as DC output, and the terminals on the branches of the H-bridge used as AC input:

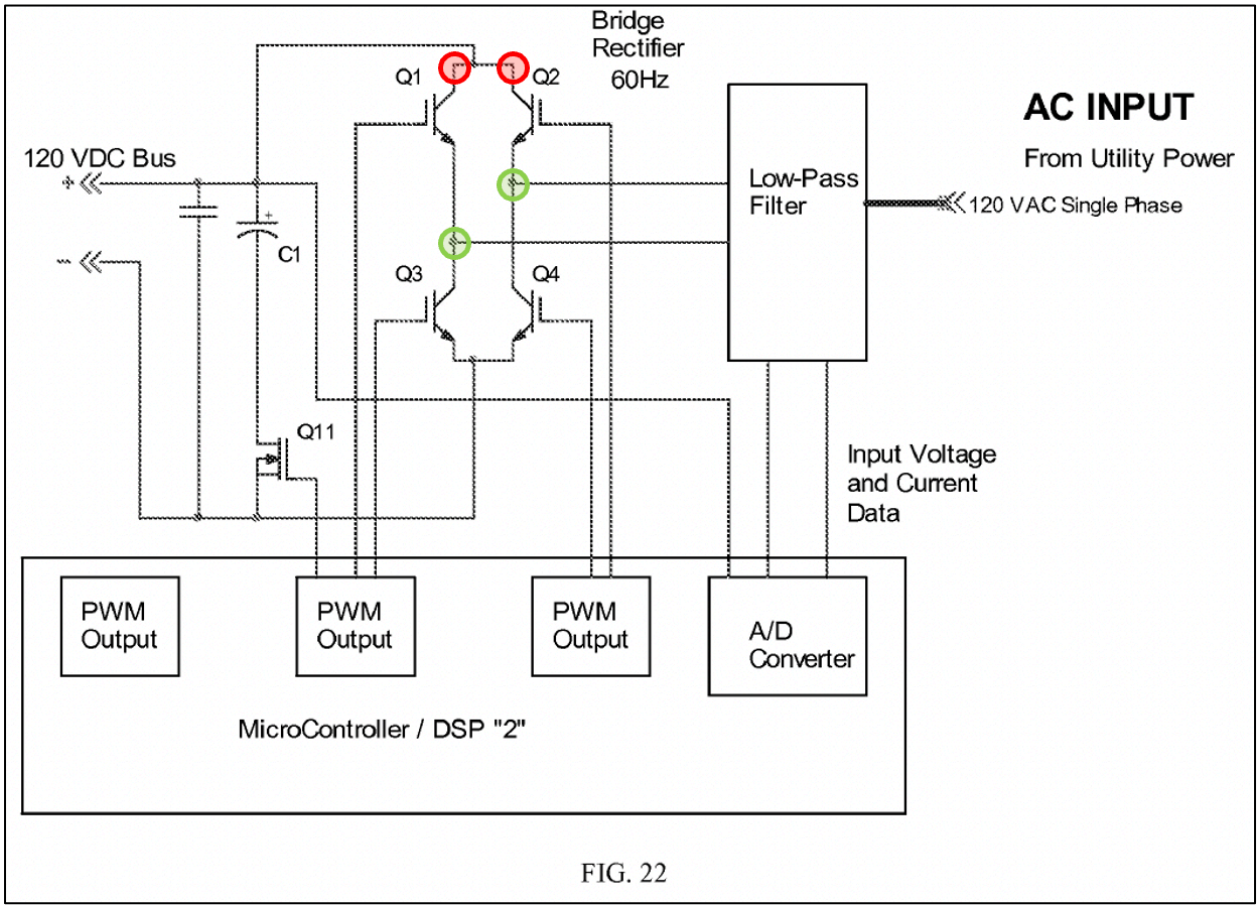


FIG. 22

Id. at Fig 22 (color emphasis added).

[14(a)(i)] a first, a second, a third and a fourth configurable input/output terminals; and

Smith discloses the claimed configurable input/output terminals. *See supra* at Claim 1(a); *see also Smith* at [0097], [0099]; Figs. 19, 22.

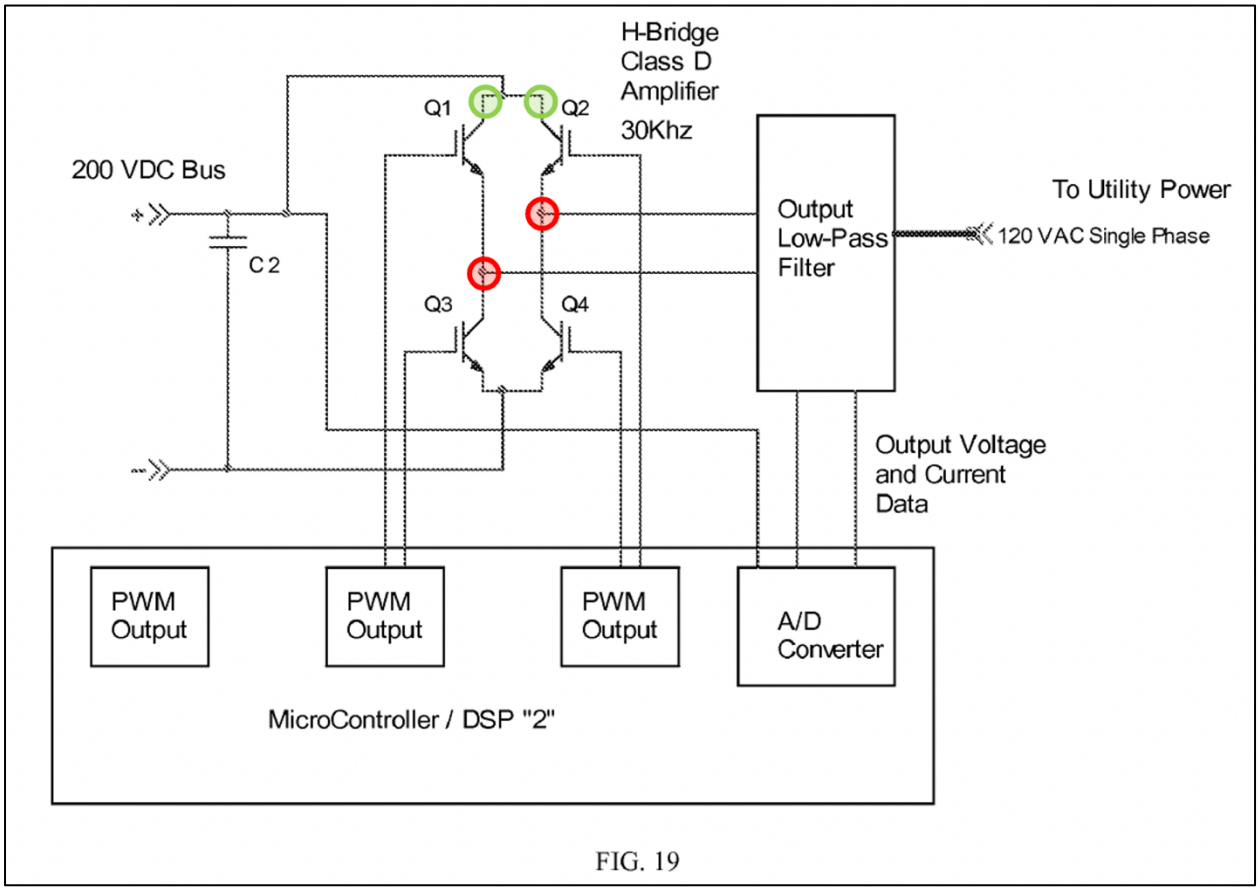


FIG. 19

Id. at Fig. 19 (color emphasis added).

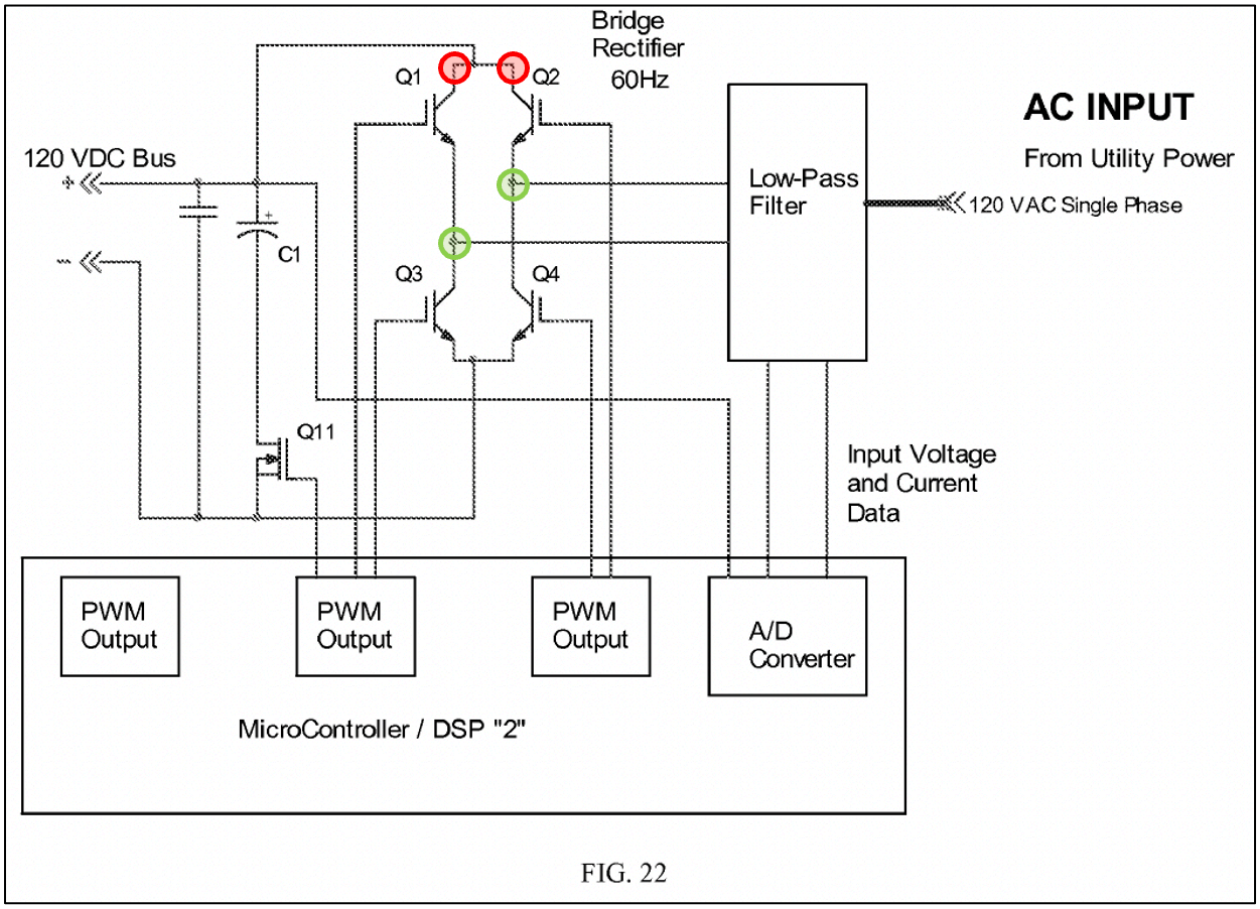


FIG. 22

Id. at Fig 22 (color emphasis added).

[14(a)(ii)] a first, a second, a third and a fourth switches, each having a first main terminal, a second main terminal and a control terminal, the control terminal being adapted to receive a control signal for controlling the open or closed state of the switch, wherein,

Smith discloses the claimed switches. *See supra* at Claim 1(b); *see also Smith* at [0097], [0099]; Figs. 19, 22.

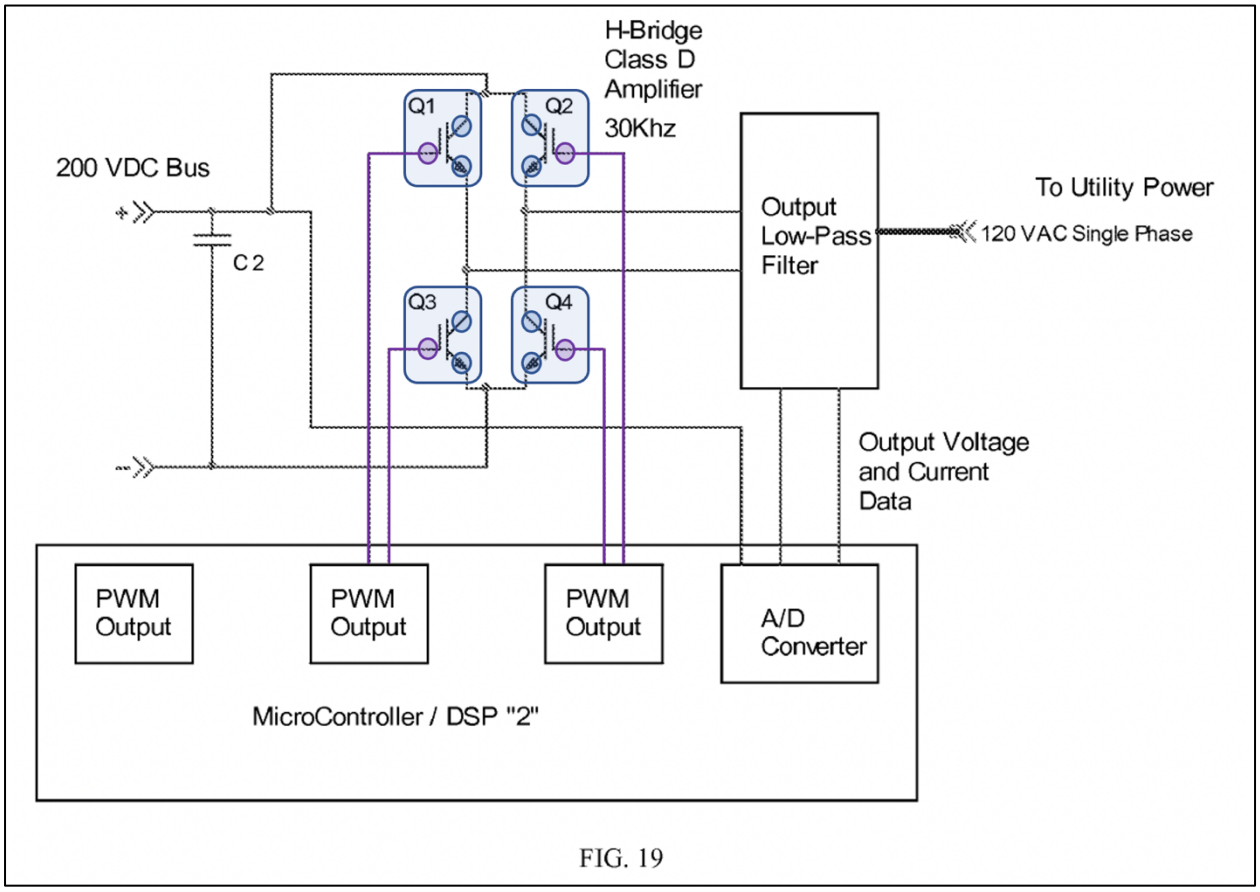


FIG. 19

Id. at Fig 19 (color emphasis added).

[14(b)(i)] the first input/output terminal is connected to the first main terminal of the first switch;

Smith discloses this limitation. *See supra* at Claim 1(c)(i); *see also Smith* at [0097], [0099]; Figs. 19, 22.

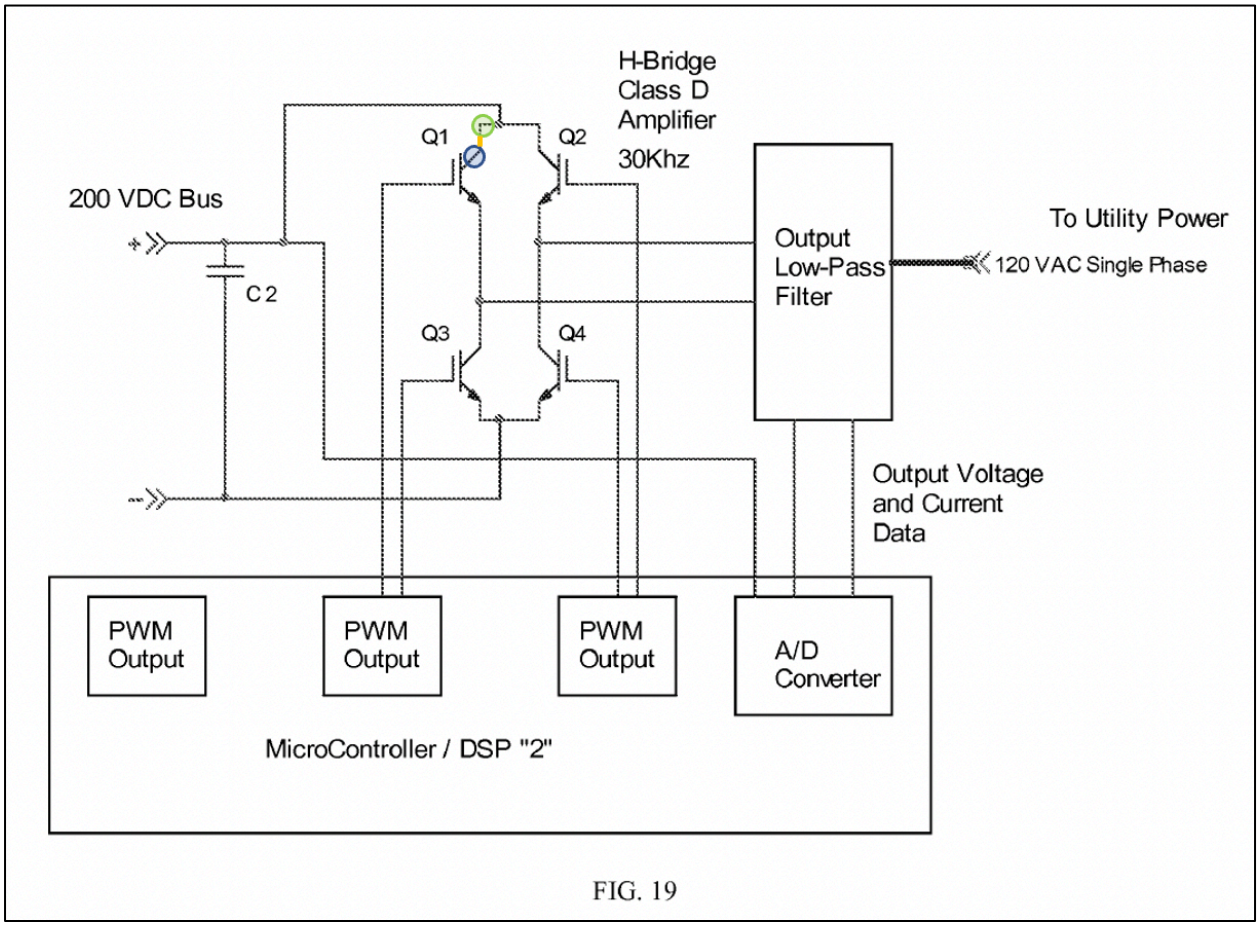


FIG. 19

Id. at Fig. 19 (color emphasis added).

[14(b)(ii)] the second input/output terminal is connected to the first main terminal of the second switch;

Smith discloses this limitation. *See supra* at Claim 1(c)(ii); *see also Smith* at [0097], [0099]; Figs. 19, 22.

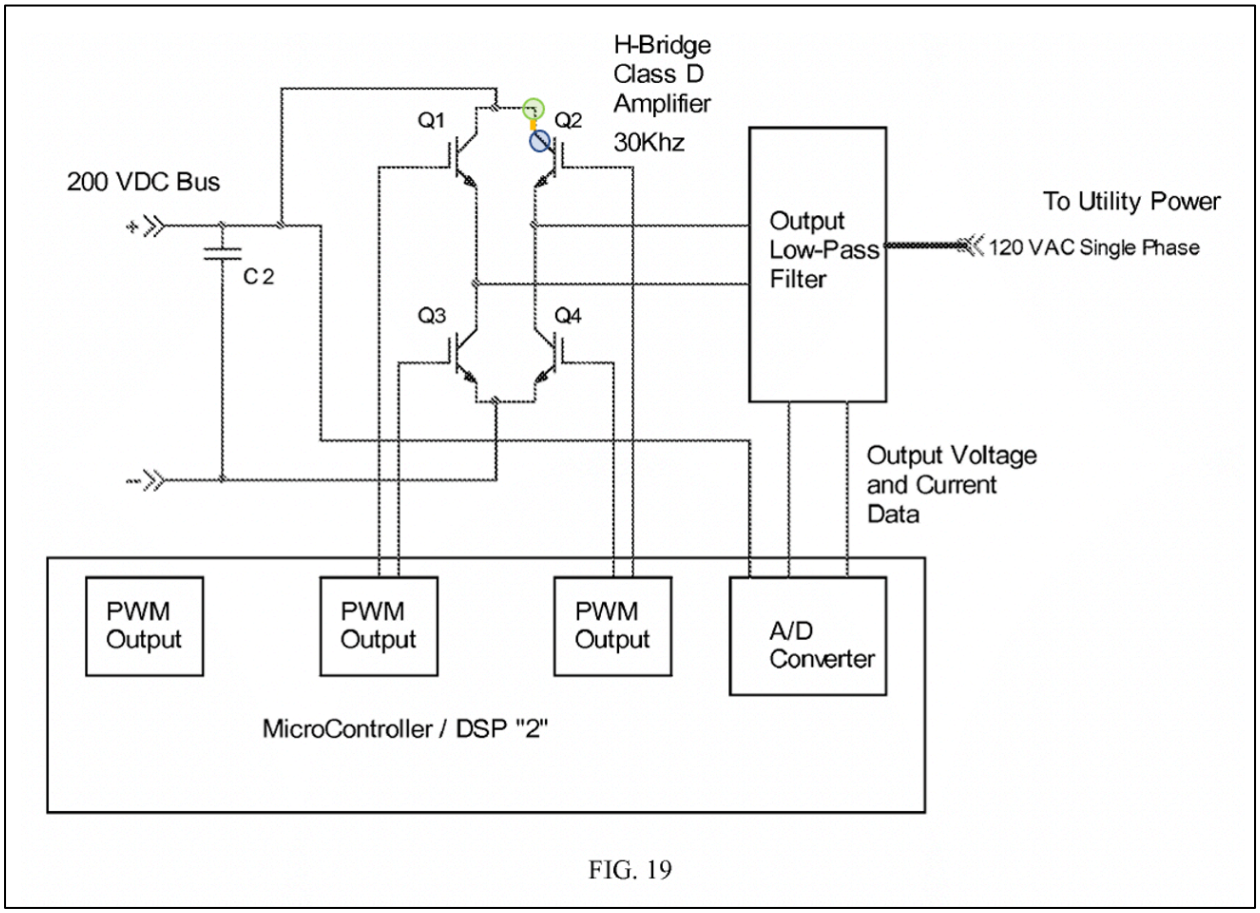


FIG. 19

Id. at Fig. 19 (color emphasis added); *see also id.* at [0097], [0099], Fig. 22.

[14(b)(iii)] the second main terminal of the first switch is connected to the first main terminal of the third switch through a first branch,

Smith discloses this limitation. *See supra* at Claim 1(c)(iii); *see also Smith* at [0097], [0099]; Figs. 19, 22.

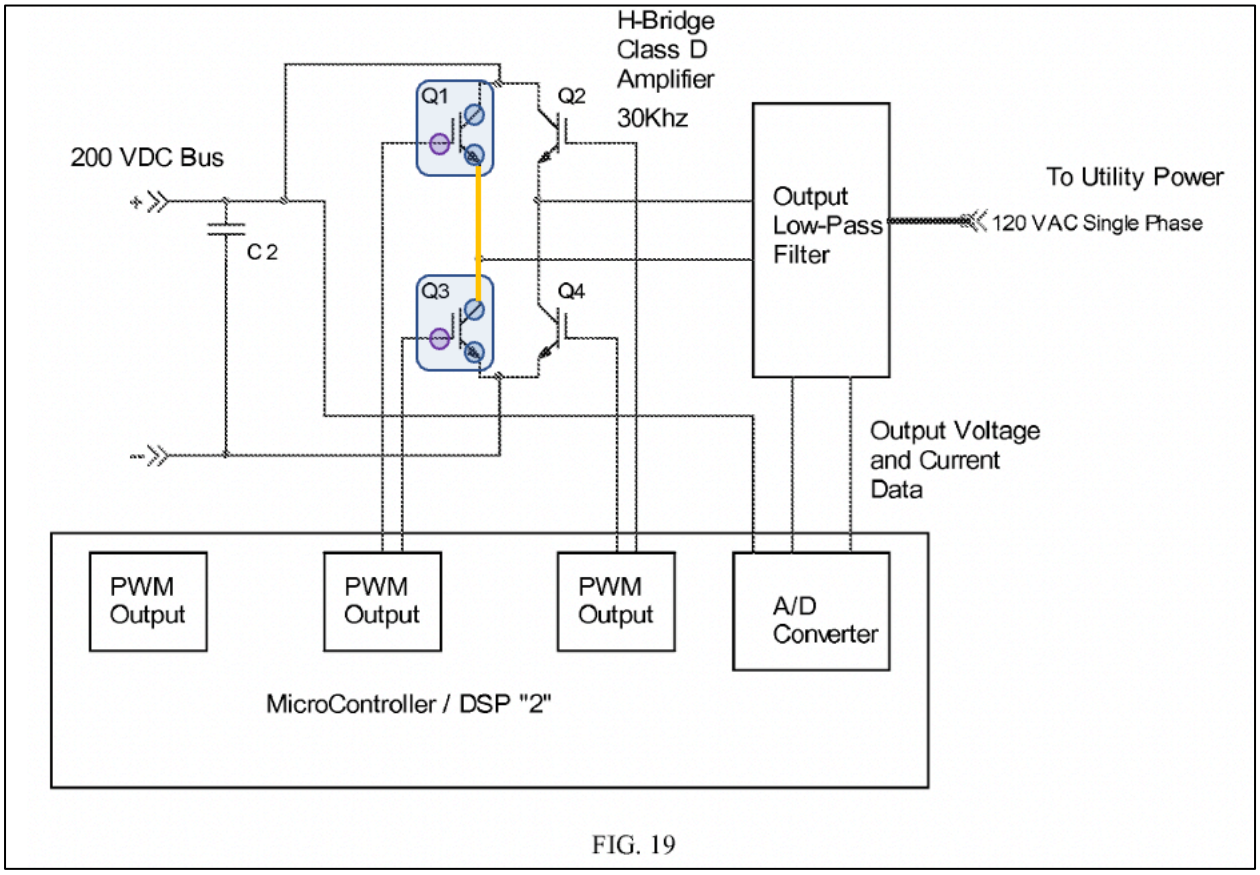


FIG. 19

Id. at Fig. 19 (color emphasis added).

[14(b)(iv)] the second main terminal of the second switch is connected to the first main terminal of the fourth switch through a second branch;

Smith discloses this limitation. *See supra* at Claim 1(c)(iv); *see also Smith* at [0097], [0099]; Figs. 19, 22.

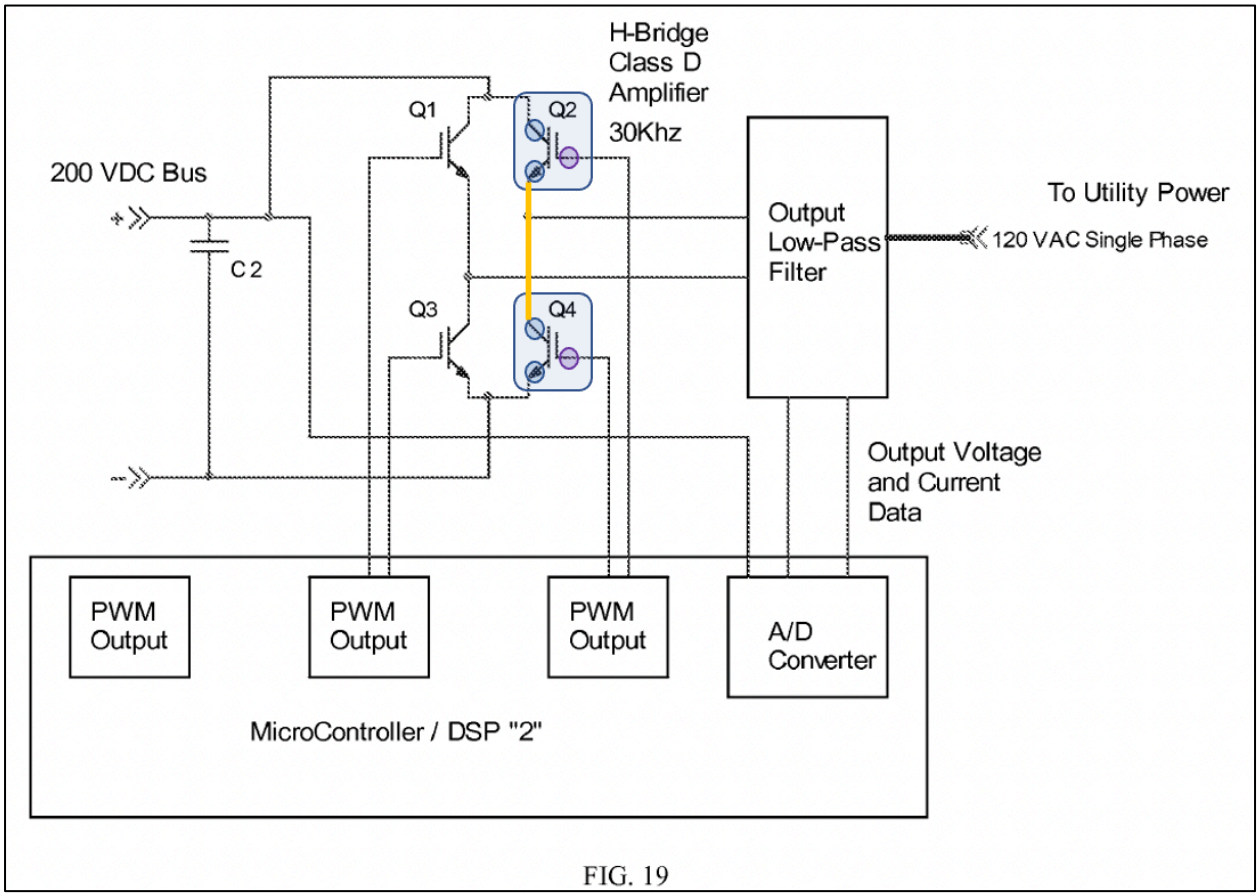


FIG. 19

Id. at Fig. 19 (color emphasis added).

[14(b)(v)] the third input/output terminal is connected to the first branch and the fourth input/output terminal is connected to the second branch;

Smith discloses this limitation. *See supra* at Claim 1(c)(v); *see also Smith* at [0097], [0099]; Figs. 19, 22.

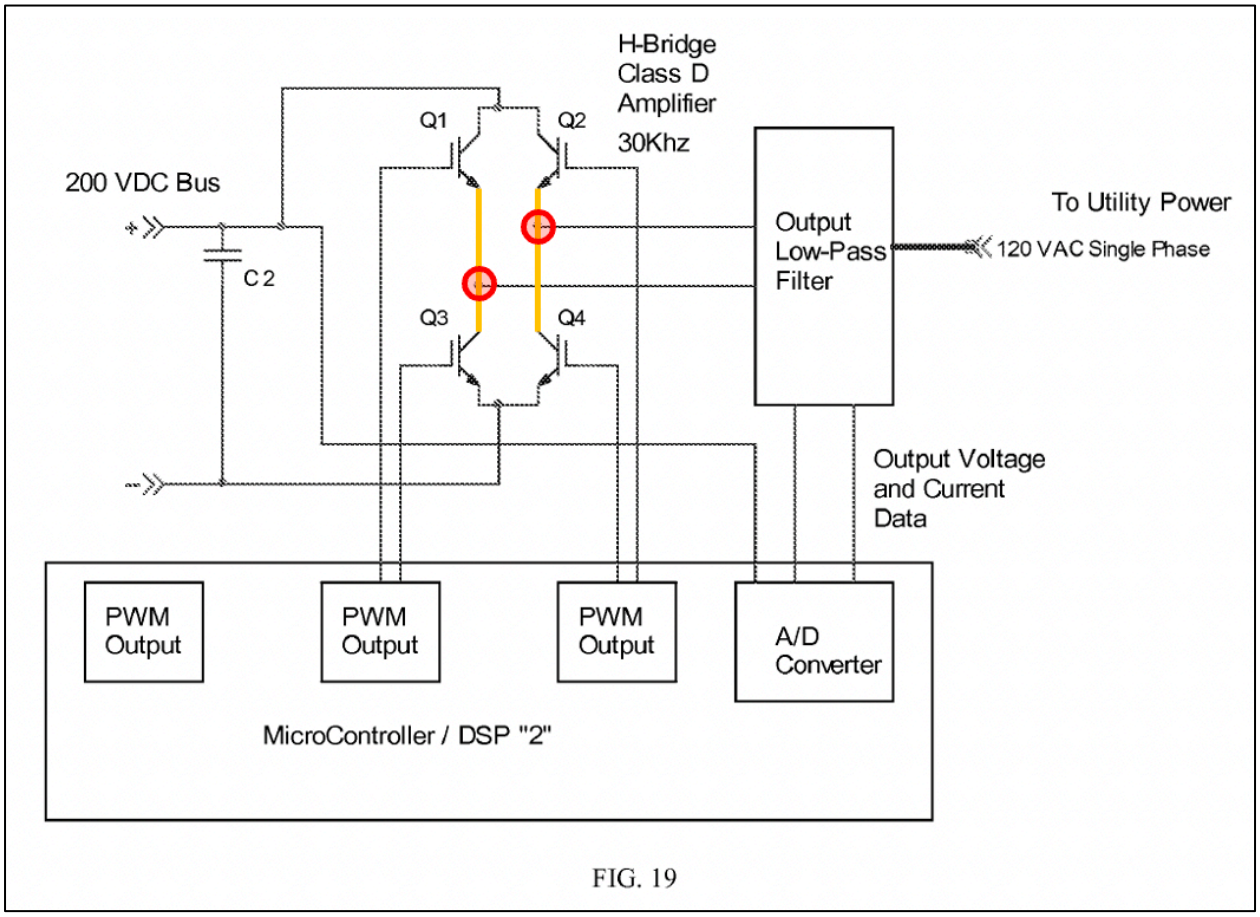


FIG. 19

Id. at Fig. 19 (color emphasis added).

[14(b)(vi)] the second main terminals of the third and fourth switches are both connected to a common node receiving a reference potential; and, wherein

Smith discloses this limitation. *See supra* at Claim 1(c)(vi); *see also Smith* at [0097], [0099]; Figs. 19, 22.

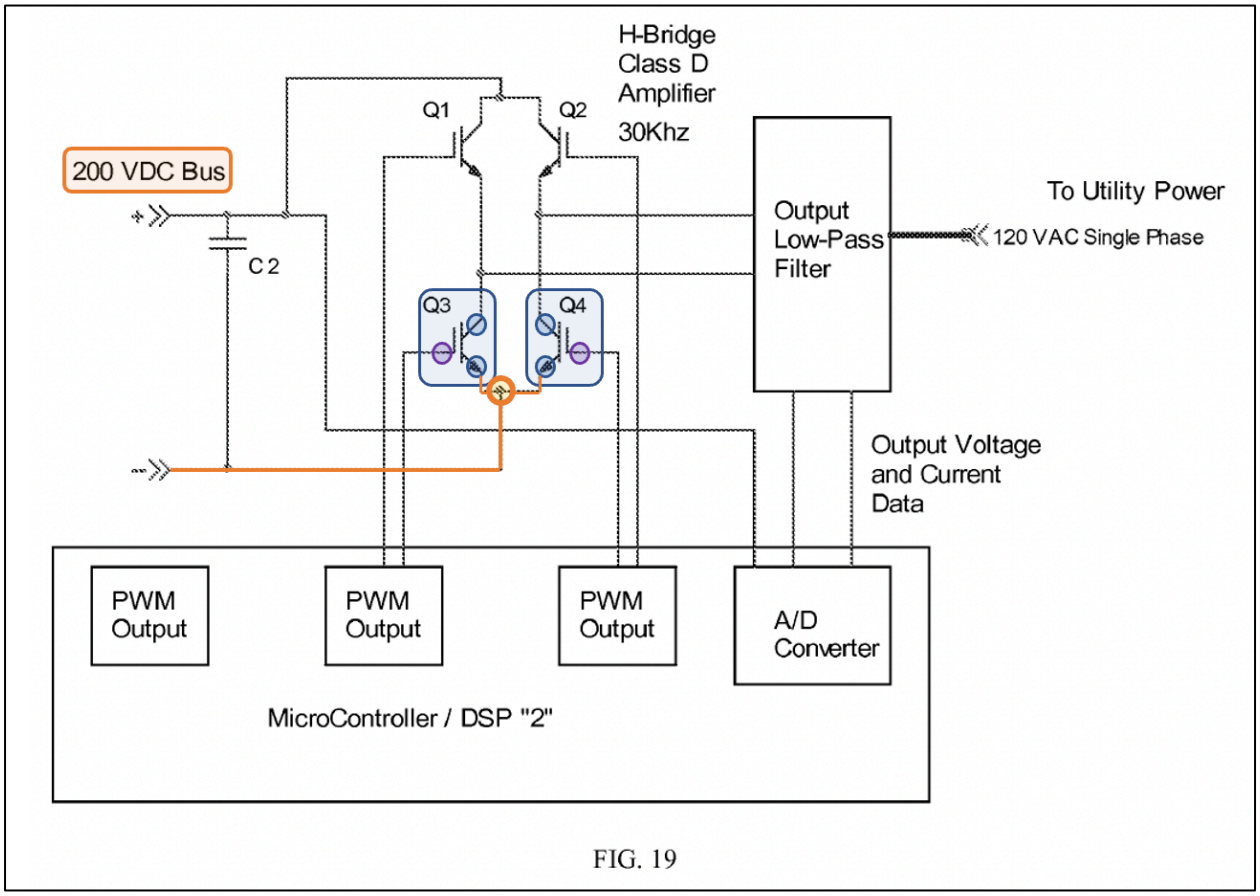


FIG. 19

Id. at Fig. 19 (color emphasis added).

[14(b)(vii)] when the first and second input/output terminals are configured to operate as input terminals, the third and fourth input/output terminal are configured to operate as output terminals; and,

Smith discloses this limitation. *See supra* at Claim 1(c)(vii); *see also Smith* at [0097], [0099]; Figs. 19, 22.

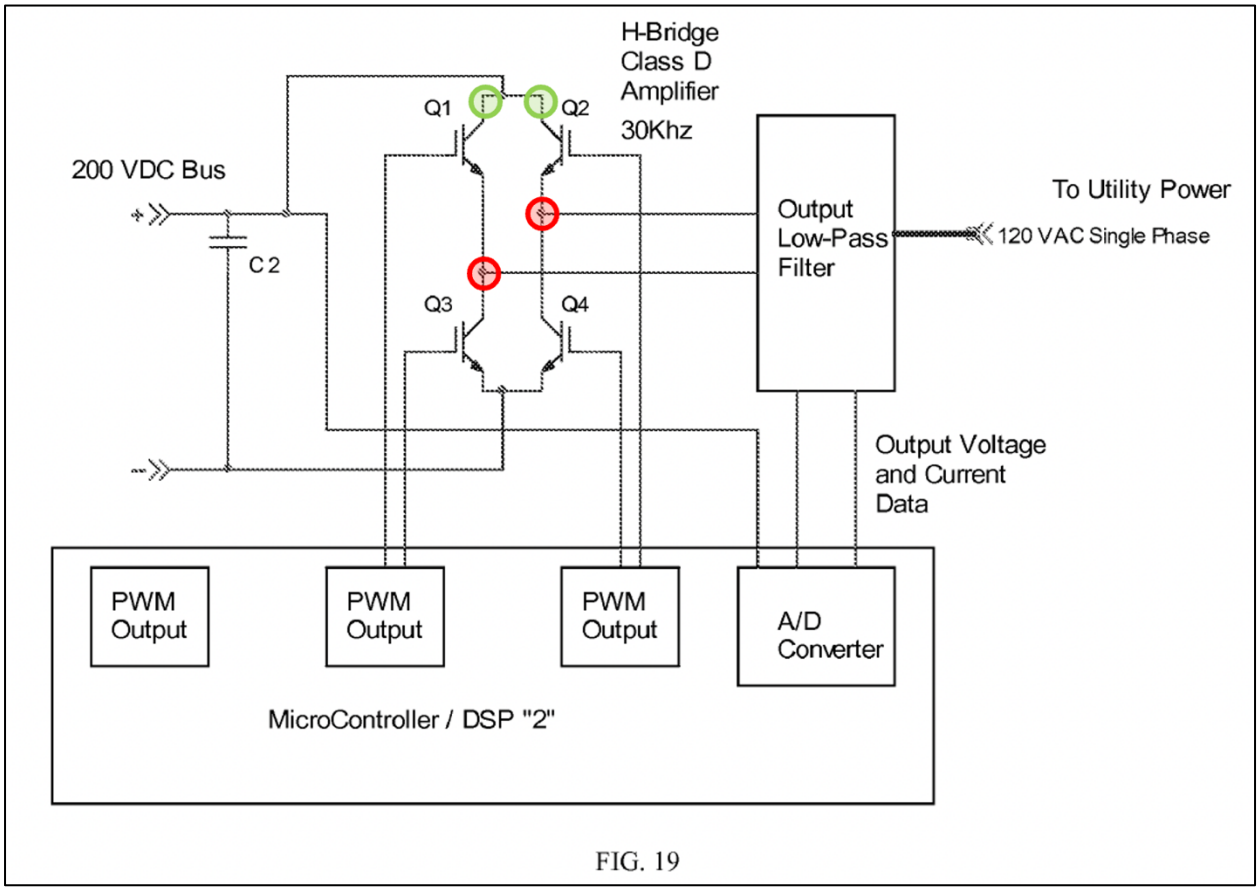


FIG. 19

Id. at Fig. 19 (color emphasis added).

[14(b)(viii)] when the first and second input/output terminals are configured to operate as output terminals, the third and fourth input/output terminals are configured to operate as input terminals; and, wherein

Smith discloses this limitation. *See supra* at Claim 1(c)(viii); *see also Smith* at [0097], [0099]; Figs. 19, 22.

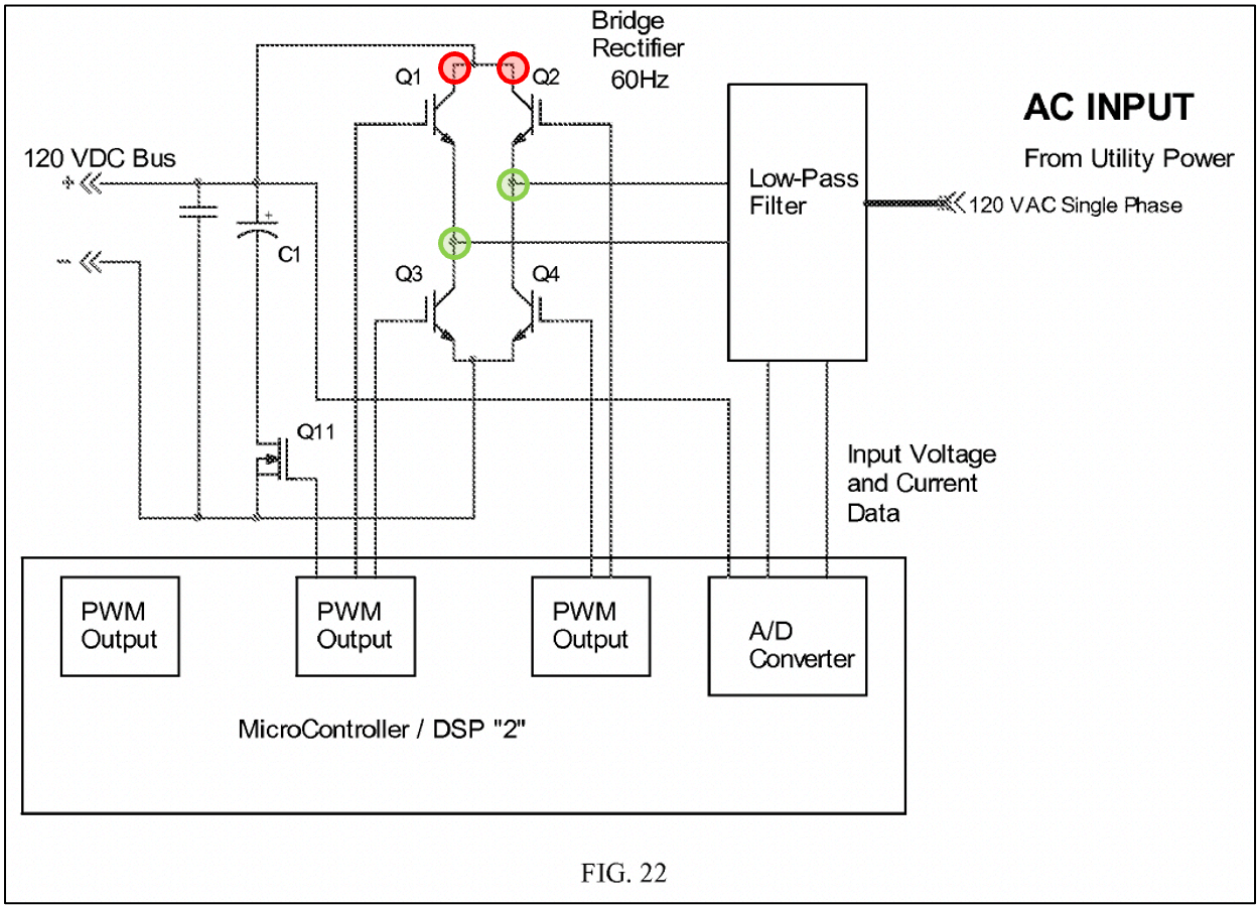


FIG. 22

Id. at Fig 22 (color emphasis added).

[14(b)(ix)] in the first operating state, the output stage is arranged in a first electrical configuration; and

Smith discloses this limitation. *See supra* at Claim 1(c)(ix); *see also Smith* at [0097], [0099]; Figs. 19, 22.

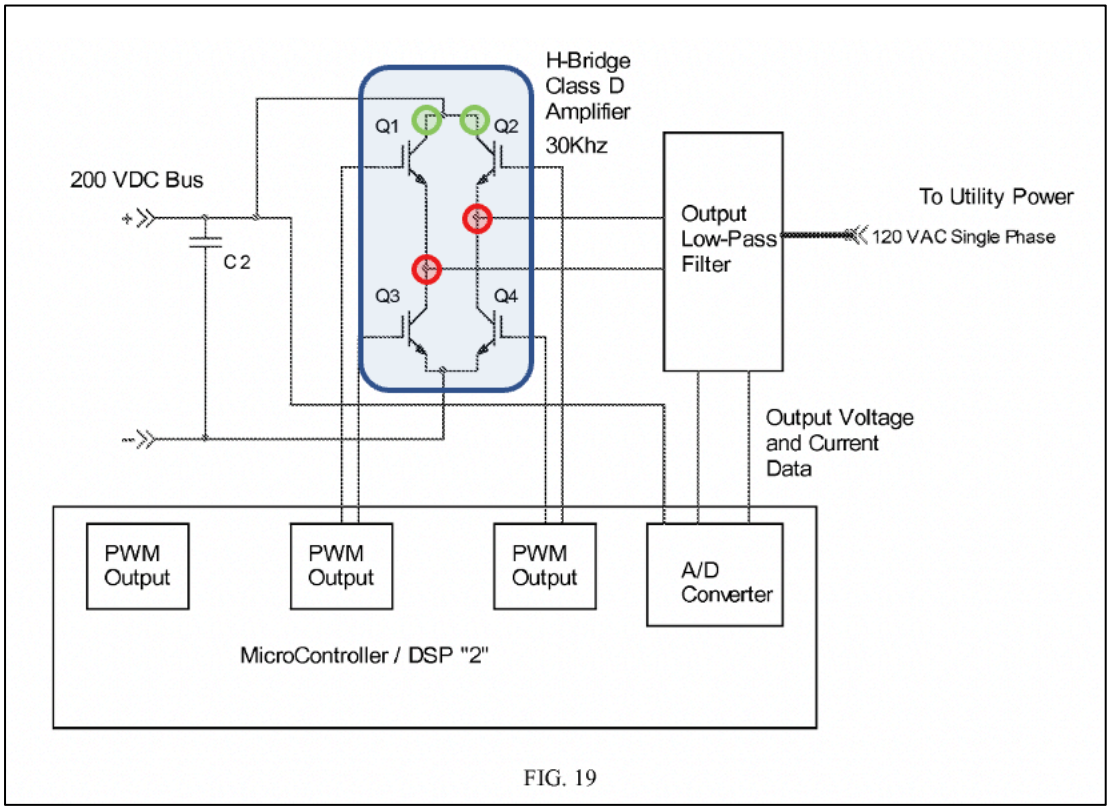


FIG. 19

Id. at Fig 19 (color emphasis added).

[14(b)(x)] in the second operating state wherein the output stage is arranged in a second electrical configuration different from the first configuration, and,

Smith discloses this limitation. *See supra* at Claim 1(c)(x); *see also Smith* at [0097], [0099]; Figs. 19, 22.

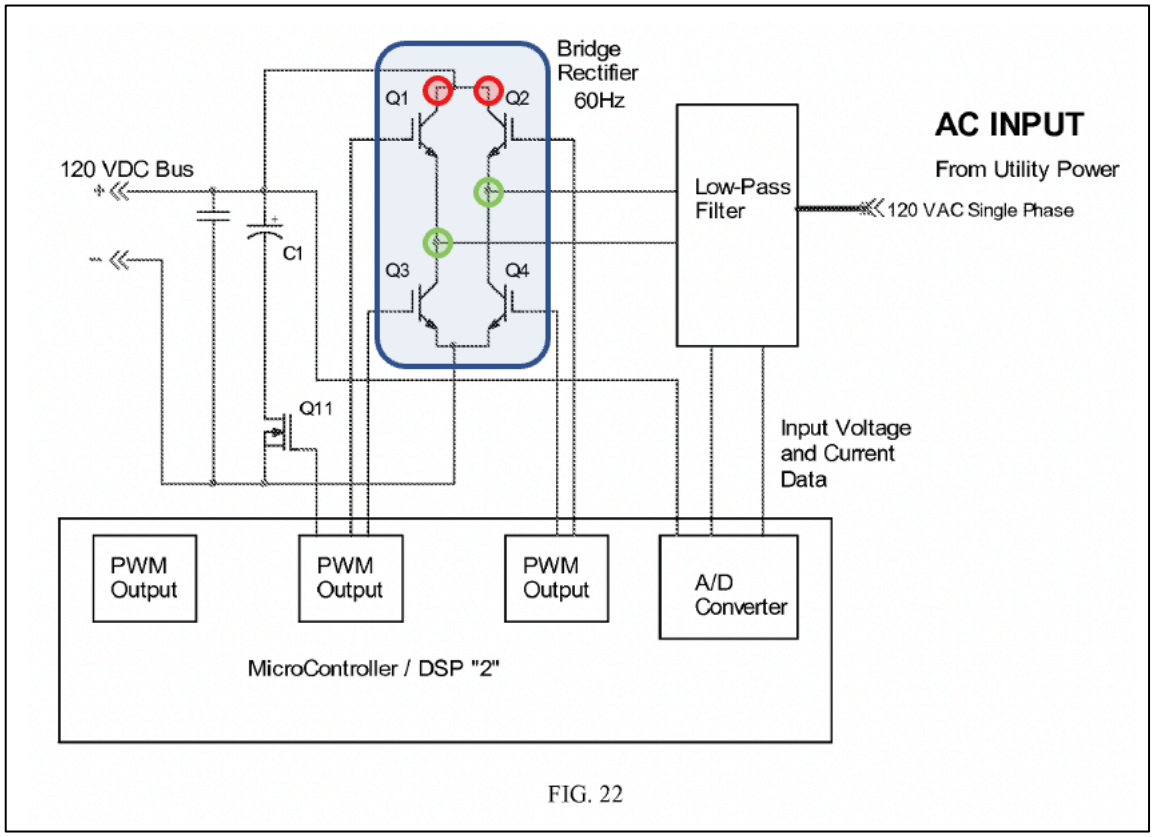


FIG. 22

Id. at Fig 22 (color emphasis added).

[14(b)(xi)] further wherein, in the first operating state, the first and second input/output terminals are configured to operate as input terminals and are configured to be connected to a common node receiving supply potential; and

Smith discloses this limitation. *See supra* at Claim 2(a); *see also Smith* at [0097], [0099]; Figs. 19, 22.

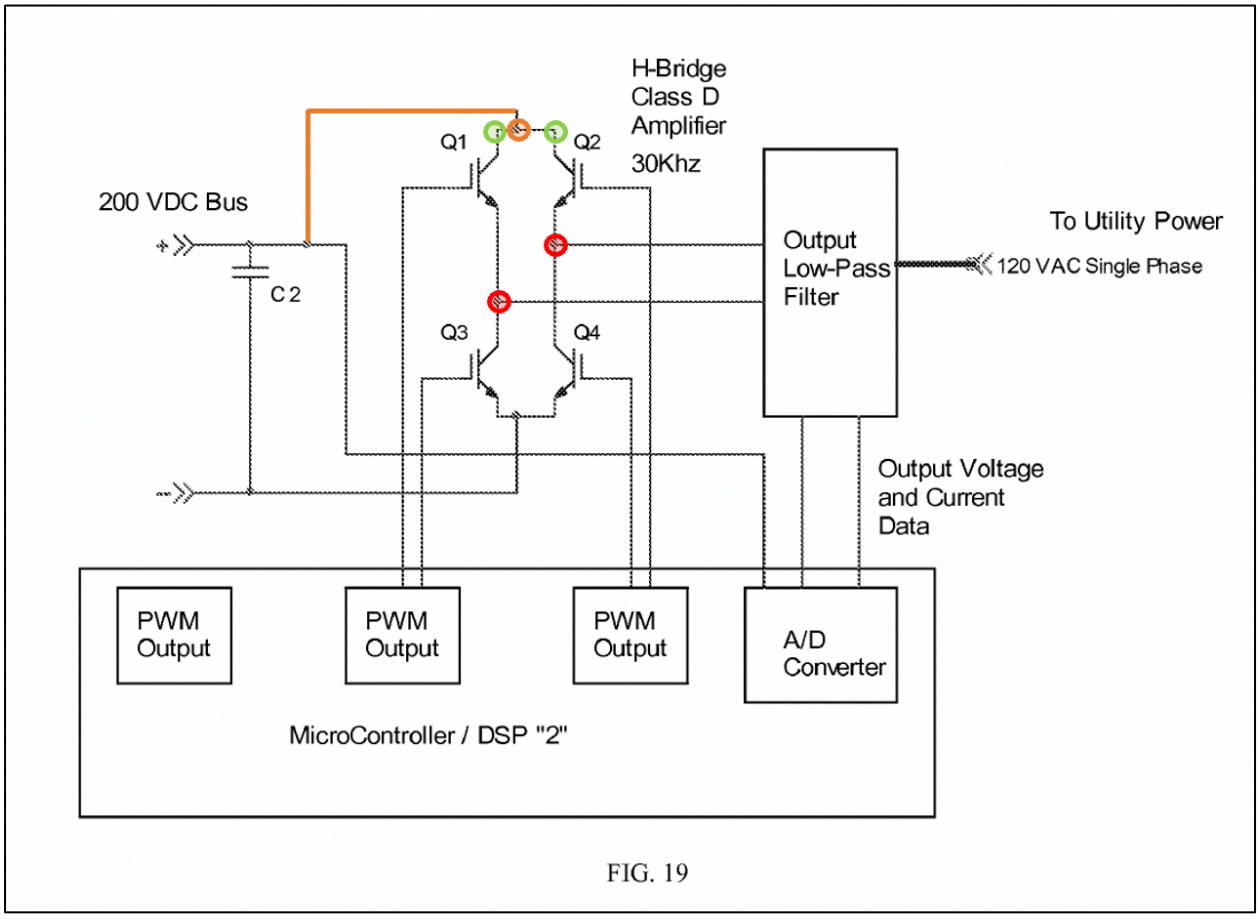


FIG. 19

Id. at Fig 19 (color emphasis added).

[14(b)(xii)] the third and fourth input/output terminals are configured to be connected to a load element, and

Smith discloses this limitation. *See supra* at Claim 2(b); *see also Smith* at [0097], [0099]; Figs. 19, 22.

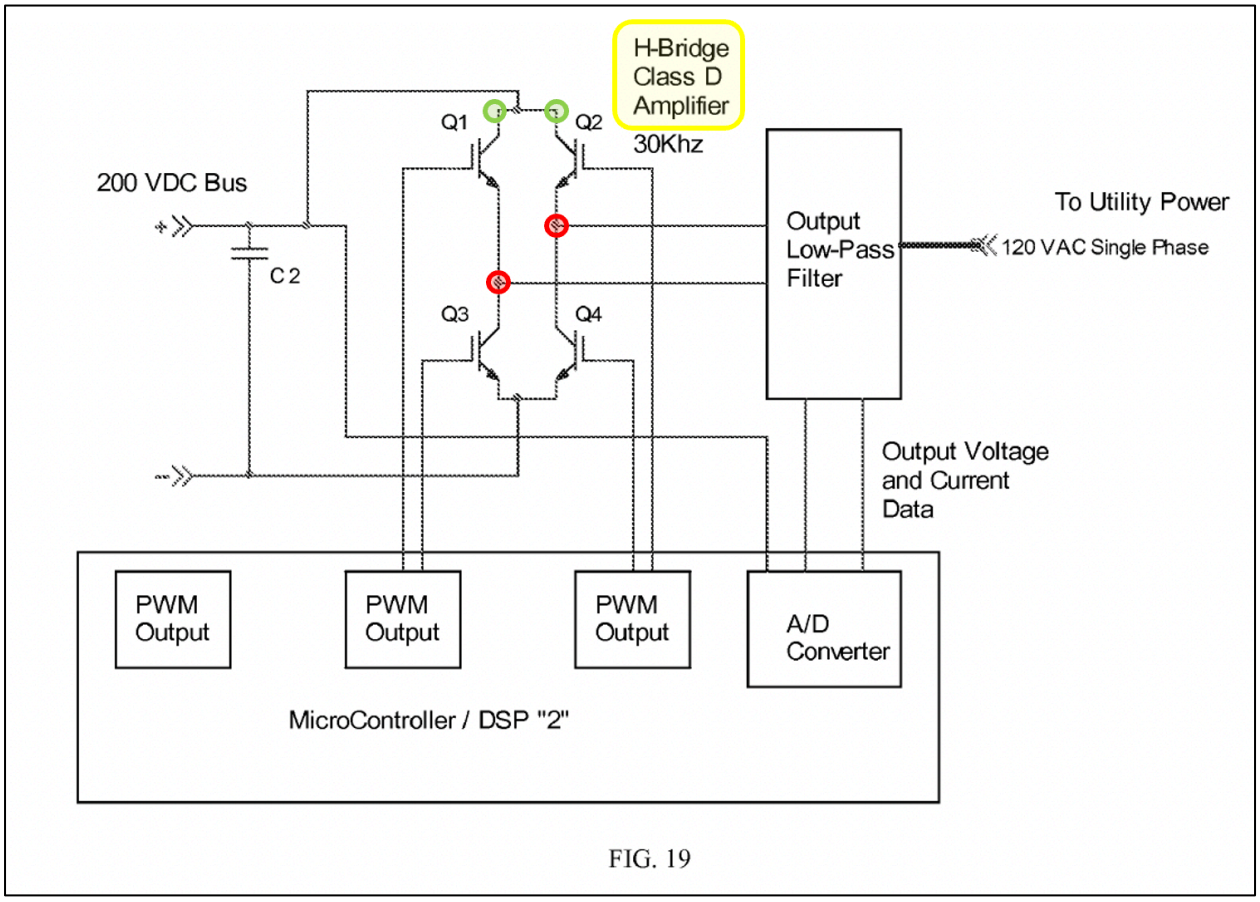


FIG. 19

See id. at Fig. 19 (color emphasis added).

[14(b)(xiii)] wherein the control stage is adapted to control the output stage by generating control signals for controlling the first, second, third and fourth switches through their respective control terminals;

Smith illustrates and describes a control stage that is adapted to control the output stage by generating control signals (through the PWM Outputs) for controlling the switches through their respective control terminals.

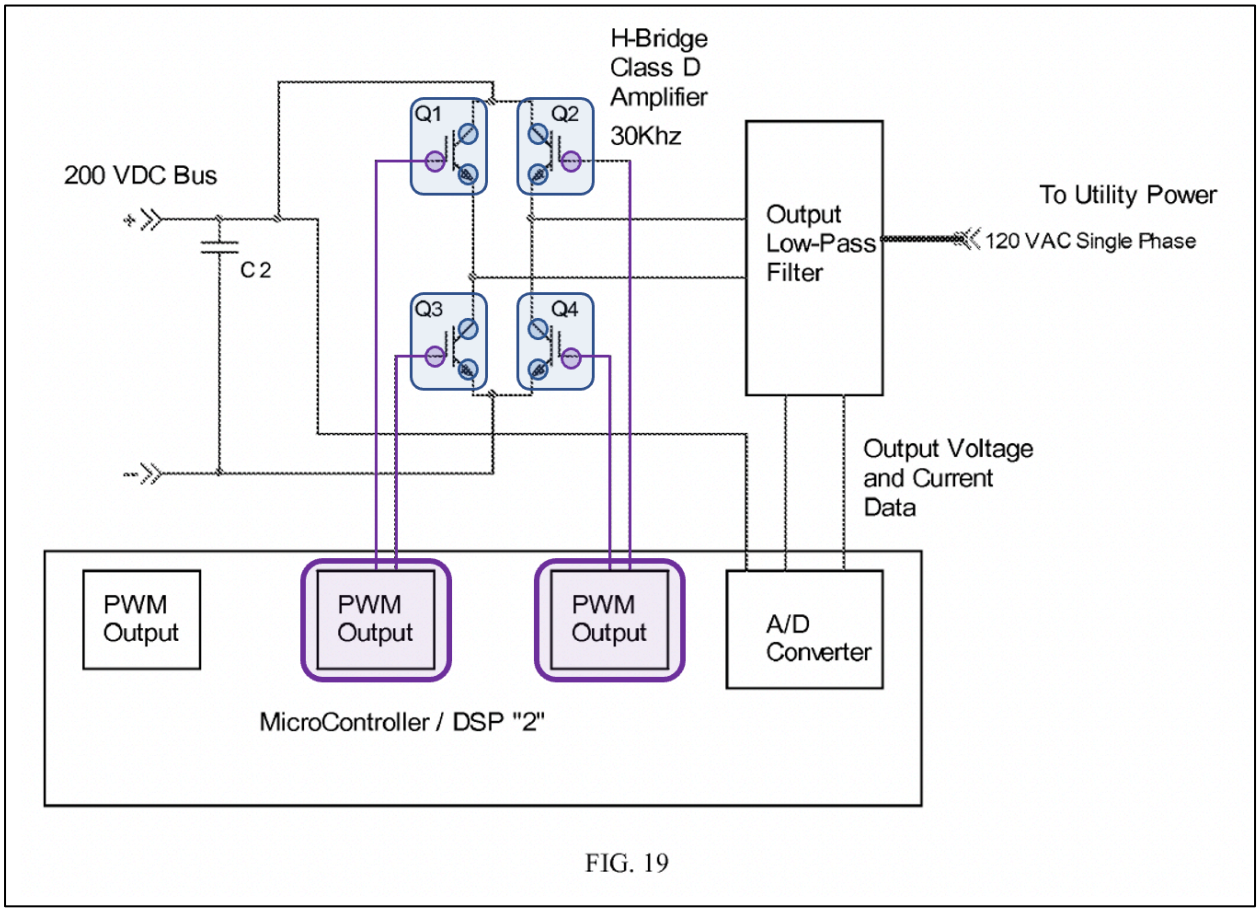


FIG. 19

See id. at Fig. 19 (color emphasis added); *see also id.* at [0097], [0099]. As described in *Smith* the H-bridge output stage "may also include Q1-Q4, which may receive PWM [Pulse Width Modulator] outputs from a DSP [Digital Signal Processor]." *Id.* at [0097]. "The DSP may control the drive signals provided to the 'H' bridge." *Id.*; *see also Hassoun Decl.* at ¶¶ 76-79, 88 (describing control functionality for illustrated transistors). Similarly, with respect to the second operating state described and illustrated in *Smith* in Figure 22, *Smith* notes that the switches Q1-Q4 "may receive PWM outputs from one or more DSP, such as DSP 2. DSP 2 may thus control the 'H' bridge DC output." *Id.* at [0099]. As illustrated in Figures 19 and 22, the

signal coming from the control stage to switches Q1-Q4 is communicated through the respective control terminals of the switches. *See id.* at Figs. 19, 22.

[14(c)] a battery configured to be connected to the input terminals of the circuit; and

Smith describes and illustrates a power source configured to be connected to the input terminals of the circuit, and that power source can be a battery. *See id.* at Figs. 19, 22; *see also id.* at [0097], [0099]. *Smith* states that "[i]n AC generation mode, DC input power from an energy source such as a battery or capacitor may be converted to AC." *Id.* at [0006]. The operating state illustrated in Figure 19 shows an AC generation mode. *See id.* at Fig. 19; *see also id.* at [0093]-[0094], [0097] (discussing Figure 19 and the H-Bridge AC output stage with AC Generation Mode). *Smith* also describes batteries extensively throughout (*see*, *e.g.*, *id.* at [0085]-[0092]). *See generally Smith*. It would have been obvious for a PHOSITA to use a battery to provide the power to the circuit described and illustrated in *Smith*. *See Hassoun Decl.* (Ex. 1006) at ¶¶ 89-90.

[14(d] a loudspeaker configured to be connected to the output terminals of the circuit.

As discussed above with respect to Claim 14(b)(xii), *Smith* describes a Class D amplifier. A PHOSITA would understand that the purpose of a Class D amplifier is to provide output to a speaker, which would be a load element in the circuit. *See Hassoun Decl.* (Ex. 1006) at ¶¶ 91-95. Thus, it would be well understood and

appreciated by a PHOSITA, based on the illustrations and descriptions in *Smith*, that in the Class D amplifier operating state the third and fourth input/output terminals would be configured to be connected to a load element and, namely, a speaker. *See id.*

Further, a speaker is expressly disclosed in *Stengel* to be used with an audio amplifier (*see*, *e.g.*, *Stengel* (Ex. 1005), Figs. 3, 6; Col. 5:3-26), and it would have been obvious for a PHOSITA to use the speaker disclosed in *Stengel* with the Class-D amplifier circuit disclosed in *Smith* at least because a PHOSITA would understand that Class-D amplifiers are designed to be used with speakers. *See Hassoun Decl.* (Ex. 1006) at ¶¶ 91-95. A PHOSITA would have been motivated to combine the speaker from *Stengel* with the circuit described and illustrated in *Smith* at least because both references describe full bridge output circuits connected to the output of DC-DC regulation circuits. *See Smith* (Ex. 1004), Figs. 1, 2, 21, [0050],[0097]–[0099]; *Stengel* (Ex. 1005), Figs 2–4, 2:20–24, 2:53–56, 4:58–67, 5:3–6, 5:60–65). The substitution of one type of load element, namely a speaker from *Stengel*, for the load elements already disclosed in *Smith* would have been the simple substitution of one known element for another, and would have yielded predictable results, namely, driving a current to the load. *See Hassoun Decl.* (Ex. 1006) at ¶¶ 91-95.

VI. CONCLUSION

For the forgoing reasons, Petitioner respectfully requests *inter partes* review of claims 1, 2, 8, 10, and 14 of the '400 Patent.

Respectfully submitted,
By: /s/ Adam P. Seitz
Adam P. Seitz, Reg. No. 52,206
Paul R. Hart, Reg. No. 59,646
COUNSEL FOR PETITIONER

VII. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8(A)(1)

A. Real Party-In-Interest

Petitioner is the real party-in-interest. 37 C.F.R. § 42.8(b)(1).

B. Related Matters

Pursuant to 37 C.F.R. § 42.8(b)(2), Petitioner is aware of the following matters involving the '400 Patent:

1. *Ericsson Inc. et al. v. Apple Inc.*, No. 6:22-cv-00061 (W.D. Tex.);
2. *Ericsson Inc. et al. v. Apple Inc.*, 337-TA-1300 (ITC).

C. Lead and Back-Up Counsel

Petitioner provides the following designation and service information for lead and back-up counsel. 37 C.F.R. § 42.8(b)(3) and (b)(4).

Lead Counsel	**Back-Up Counsel**
Adam P. Seitz (Reg. No. 52,206) Adam.Seitz@eriseip.com PTAB@eriseip.com Postal and Hand-Delivery Address: Erise IP, P.A. 7015 College Blvd., Ste. 700 Overland Park, Kansas 66211 Telephone: (913) 777-5600 Fax: (913) 777-5601	Paul R. Hart (Reg. No. 59,646) Paul.Hart@eriseip.com Postal and Hand-Delivery Address: Erise IP, P.A. 5299 DTC Blvd., Ste. 1340 Greenwood Village, Colorado 80111 Telephone: (913) 777-5600 Fax: (913) 777-5601

APPENDIX OF EXHIBITS

Exhibit 1001	U.S. Patent No. 9,705,400
Exhibit 1002	File History of U.S. Patent No. 9,705,400
Exhibit 1003	File History of European Patent No. EP2811646
Exhibit 1004	International Publication WO 2010/111433 A2 ("Smith")
Exhibit 1005	United States Patent No. 5,506,493 (Stengel)
Exhibit 1006	Declaration of Dr. Marwan Hassoun, Ph.D. in Support of Petition for *Inter Partes* Review
Exhibit 1007	Curriculum Vitae of Dr. Marwan Hassoun, Ph.D.
Exhibit 1008	Hart, Daniel W., "*Power Electronics*," McGraw-Hill, 2011
Exhibit 1009	Maxim Integrated, "*Fundamentals of Class D Amplifiers*," Application Note 3977, Jan. 31, 2007
Exhibit 1010	Honda, Jun et al. "*Class D Audio Amplifier Basics*," Application Note AN-1071, Internal Rectifier, Feb. 8, 2005
Exhibit 1011	Sattar, Abdus, "*Insulated Gate Bipolar Transistor (IGBT) Basics*," IXYS Corp., 2008
Exhibit 1012	Dodge, Jonathan, "*IGBT Tutorial*," Application Note APT0201 Rev. B, Advanced Power Technology, July 1, 2002
Exhibit 1013	*In the Matter of Certain Mobile Phones and Tablet Computers, All With Switchable Connectivity*, ITC-337-TA-1300, Exhibit 15A to Complaint, Complainant's Proof of Infringement (ITC Jan. 18, 2022)
Exhibit 1014	*In the Matter of Certain Mobile Phones and Tablet Computers, All with Switchable Connectivity*, ITC-337-TA-1300, Proposed Scheduling Order (ITC Mar. 11, 2022)

CERTIFICATION OF WORD COUNT

The undersigned certifies pursuant to 37 C.F.R. §42.24 that the foregoing Petition for *Inter Partes* Review, excluding any table of contents, mandatory notices under 37 C.F.R. §42.8, certificates of service or word count, or appendix of exhibits, contains 8,634 words according to the word-processing program used to prepare this document (Microsoft Word).

Dated: April 6, 2022

BY: /s/ *Adam P. Seitz*
Adam P. Seitz, Reg. No. 52,206

COUNSEL FOR PETITIONER

CERTIFICATE OF SERVICE ON PATENT OWNER UNDER 37 C.F.R. § 42.105

Pursuant to 37 C.F.R. §§ 42.6(e) and 42.105, the undersigned certifies that on April 6, 2022, a complete and entire copy of this Petition for *Inter Partes* Review including exhibits was provided via Federal Express to the Patent Owner by serving the correspondence address of record for the '400 Patent as listed on PAIR:

The Danamraj Law Group, P.C.
Turley Law Center, Suite 810
6440 N. Central Expressway
Dallas, TX 75206

Further, a courtesy copy of this Petition for *Inter Partes* Review was sent via email to Patent Owner's litigation counsel:

M. Brett Johnson, mbjohnson@winston.com
Michael A. Bittner, mbittner@winston.com
Thomas M. Melsheimer, tmelsheimer@winston.com

BY: /s/ *Adam P. Seitz*
Adam P. Seitz, Reg. No. 52,206

COUNSEL FOR PETITIONER