PTO-1390 (03-13)
Approved for use through 4/30/2013. OMB 0651-0021
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A SUBMISSION UNDER 35 U.S.C. 371

Attorney Docket No.	
0112-301/C03308 US1	
U.S. Application No. (if known, see 37 CFR 1.5)	

International Application No.	International Filing Date	Priority Date Claimed
PCT/EP2014/061350	June 2, 2014	June 3, 2013

Title of Invention
Reconfigurable Output Stage

First Named Inventor
Philippe SIRITO-OLIVIER

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information.

1. ☑ This is an express request to begin national examination procedures (35 U.S.C. 371(f)). NOTE: The express request under 35 U.S.C. 371(f) will not be effective unless the requirements under 35 U.S.C. 371(c)(1), (2), and (4) for payment of the basic national fee, copy of the International Application and English translation thereof (if required), and the oath or declaration of the inventor(s) have been received.
2. ☑ A copy of the International Application (35 U.S.C. 371(c)(2)) is attached hereto (not required if the International Application was previously communicated by the International Bureau or was filed in the United States Receiving Office (RO/US)).
3. An English language translation of the International Application (35 U.S.C. 371(c)(2))
   a. ☐ is attached hereto.
   b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4).
4. An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4))
   a. ☐ is attached.
   b. ☐ was previously filed in the international phase under PCT Rule 4.17(iv).

Items 5 to 8 below concern amendments made in the international phase.

PCT Article 19 and 34 amendments

5. ☐ Amendments to the claims under PCT Article 19 are attached (not required if communicated by the International Bureau) (35 U.S.C. 371(c)(3)).
6. ☐ English translation of the PCT Article 19 amendment is attached (35 U.S.C. 371(c)(3)).
7. ☐ English translation of annexes (Article 19 and/or 34 amendments only) of the International Preliminary Examination Report is attached (35 U.S.C. 371(c)(5)).

Cancellation of amendments made in the international phase

8a. ☐ Do not enter the amendment made in the international phase under PCT Article 19.

8b. ☐ Do not enter the amendment made in the international phase under PCT Article 34.

NOTE: A proper amendment made in English under Article 19 or 34 will be entered in the U.S. national phase application absent a clear instruction from applicant not to enter the amendment(s).

The following items 9 to 17 concern a document(s) or information included.

9. ☑ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
10. ☑ A preliminary amendment.
11. ☑ An Application Data Sheet under 37 CFR 1.76.
12. ☐ A substitute specification. NOTE: A substitute specification cannot include claims. See 37 CFR 1.125(b).
13. ☐ A power of attorney and/or change of address letter.
14. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13*ter*.3 and 37 CFR 1.821-1.825.
15. ☐ Assignment papers *(cover sheet and document(s))*. Name of Assignee: _____
16. ☐ 37 CFR 3.73(c) Statement *(when there is an Assignee)*.

U.S. APPLN. No. (if known – see 37 CFR 1.5)	INTERNATIONAL APPLICATION No.	ATTORNEY DOCKET No.
	PCT/EP2014/061350	0112-301/C03308 US1

17. ☐ Other items or information:

The following fees have been submitted.	CALCULATIONS	PTO USE ONLY
18. ☑ Basic national fee (37 CFR 1.492(a)) **$280**	$ 280.00	
19. ☑ Examination fee (37 CFR 1.492(c)) If the written opinion prepared by ISA/US or the international preliminary examination report prepared by IPEA/US indicates all claims satisfy provisions of PCT Article 33(1)-(4) ..... **$0** All other situations **$720**	$ 720.00	
20. ☑ Search fee (37 CFR 1.492(b)) If the written opinion prepared by ISA/US or the international preliminary examination report prepared by IPEA/US indicates all claims satisfy provisions of PCT Article 33(1)-(4) ..... **$0** Search fee (37 CFR 1.445(a)(2)) has been paid on the international application to the USPTO as an International Searching Authority .....**$120** International Search Report prepared by an ISA other than the US and provided to the Office or previously communicated to the US by the IB .....**$480** All other situations **$600**	$ 480.00	
TOTAL OF 18, 19, and 20 =	$ 1,480.00	
☐ Additional fee for specification and drawings filed in paper over 100 sheets (excluding sequence listing in compliance with 37 CFR 1.821(c) or (e) in an electronic medium or computer program listing in an electronic medium) (37 CFR 1.492(j)). Fee for each additional 50 sheets of paper or fraction thereof **$400**		

Total Sheets	Extra Sheets	Number of each addition 50 or fraction thereof (round **up** to a whole number)	RATE	
- 100 =	/ 50 =		x **$400**	$

Surcharge of **$140.00** for furnishing any of the search fee, examination fee, or the oath or declaration after the date of commencement of the national stage (37 CFR 1.492(h)).	$

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	15 - 20 =	0	x **$80**	$ 0.00	
Independent claims	1 - 3 =	0	x **$420**	$ 0.00	
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			**+ $780**	$	
Processing fee of **$140.00** for furnishing the English translation later than 30 months from the earliest claimed priority date (37 CFR 1.492(i)). **+**				$	
TOTAL OF ABOVE CALCULATIONS =				$ 0.00	
☐ **Applicant asserts small entity status.** See 37 CFR 1.27. Fees above are reduced by ½.					
☐ **Applicant certifies micro entity status.** See 37 CFR 1.29. Fees above are reduced by ¾. Applicant must attach form PTO/SB/15A or B or equivalent.					
TOTAL NATIONAL FEE =				$ 1,480.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00** per property. **+**				$	
TOTAL FEES ENCLOSED =				$ 1,480.00	
				Amount to be refunded:	$
				Amount to be charged:	$

a. ☐ A check in the amount of $_____ to cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account No. _____ in the amount of $_____ to cover the above fees.

c. ☑ The Director is hereby authorized to charge additional fees which may be required, or credit any overpayment, to Deposit Account No. 50-5835 as follows:

i. ☑ any required fee.

ii. ☐ any required fee except for excess claims fees required under 37 CFR 1.492(d) and (e) and multiple dependent claim fee required under 37 CFR 1.492(f).

d. ☐ Fees are to be charged to a credit card. **WARNING:** Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038. The PTO-2038 should only be mailed or faxed to the USPTO. However, when paying the basic national fee, the PTO-2038 may NOT be faxed to the USPTO.

ADVISORY: If filing by EFS-Web, do **NOT** attach the PTO-2038 form as a PDF along with your EFS-Web submission. Please be advised that this is **not** recommended and by doing so your **credit card information may be displayed via PAIR**. To protect your information, it is recommended to pay fees online by using the electronic payment method.

NOTE: Where an appropriate time limit under 37 CFR 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the International Application to pending status.

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File)Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013, and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.

NOTE: A U.S. national stage application may not claim priority to the international application of which it is the national phase. The filing date of a U.S. national stage application is the international filing date. See 35 U.S.C. 363.

Correspondence Address

☑ The address associated with Customer Number: 113648 **OR** ☐ Correspondence address below

Name					
Address					
City		State		Zip Code	
Country		Telephone			
Email					

Signature	/stevenmdubois/	Date	November 9, 2015
Name (Print/Type)	Steven M. duBois	Registration No. (Attorney/Agent)	35,023

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/AIA/14 (07-14)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0112-301/C03308 US1
	Application Number	
Title of Invention	Reconfigurable Output Stage	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Philippe		SIRITO-OLIVIER	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Saint Egreve	Country of Residence [i]	FR

Mailing Address of Inventor:

Address 1	2bis rue de Bellevue Parc symphonie 13		
Address 2			
City	Saint Egreve	State/Province	
Postal Code	F-38120	Country [i]	FR

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Patrizia		MILAZZO	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	S. Agata Li Battiati	Country of Residence [i]	IT

Mailing Address of Inventor:

Address 1	Via J.F. Kennedy 23		
Address 2			
City	S. Agata Li Battiati	State/Province	
Postal Code	I-95030	Country [i]	IT

Inventor 3 Remove

Legal Name

PTO/AIA/14 (07-14)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0112-301/C03308 US1
	Application Number	
Title of Invention	Reconfigurable Output Stage	

Prefix	Given Name	Middle Name	Family Name	Suffix
	Angelo		NAGARI	

Residence Information (Select One) ◯ US Residency ◉ Non US Residency ◯ Active US Military Service

City	Grenoble	Country of Residence [i]	FR

Mailing Address of Inventor:

Address 1	12 Rue de la Poste		
Address 2			
City	Grenoble	**State/Province**	
Postal Code	F-38000	**Country** [i]	FR

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	113648		
Email Address		Add Email	Remove Email

Application Information:

Title of the Invention	Reconfigurable Output Stage		
Attorney Docket Number	0112-301/C03308 US1	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	4	**Suggested Figure for Publication (if any)**	2

Filing By Reference :

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country [i]

PTO/AIA/14 (07-14)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0112-301/C03308 US1
	Application Number	
Title of Invention	Reconfigurable Output Stage	

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	113648		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the application number blank.

Prior Application Status			Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	a 371 of international	PCT/EP2014/061350	2014-06-02

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX) [i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

Application Number	Country [i]	Filing Date (YYYY-MM-DD)	Access Code [j] (if applicable)
13305740.6	EP	2013-06-03	

PTO/AIA/14 (07-14)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0112-301/C03308 US1
	Application Number	
Title of Invention	Reconfigurable Output Stage	

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Authorization to Permit Access:

☒ Authorization to Permit Access to the Instant Application by the Participating Offices

If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application.

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date o f filing this Authorization.

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

PTO/AIA/14 (07-14)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0112-301/C03308 US1
	Application Number	
Title of Invention	Reconfigurable Output Stage	

Applicant 1 Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

(●) Assignee	( ) Legal Representative under 35 U.S.C. 117	( ) Joint Inventor
( ) Person to whom the inventor is obligated to assign.	( ) Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor :

If the Applicant is an Organization check here. [X]

Organization Name	ST-Ericsson SA		
Mailing Address Information For Applicant:			
Address 1	39 Chemin du Champ-des-Filles		
Address 2			
City	Plan-Les-Ouates	**State/Province**	
Country [i]	CH	Postal Code	CH-1228
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not subsitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication . An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

Remove

If the Assignee or Non-Applicant Assignee is an Organization check here. [ ]

PTO/AIA/14 (07-14)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0112-301/C03308 US1
	Application Number	
Title of Invention	Reconfigurable Output Stage	

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. Add

Signature:

Remove

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Signature	/stevenmdubois/			Date (YYYY-MM-DD)	2015-11-09
First Name	Steven	Last Name	duBois	Registration Number	35023

Additional Signature may be generated within this form by selecting the Add button. Add

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent C o o p eration Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Patent
Attorney's Docket No. 0112-301/C03308 US1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	)	
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Philippe SIRITO-OLIVIER *et al*.	)	
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	)	
For: RECONFIGURABLE OUTPUT STAGE	)	

PRELIMINARY AMENDMENT

Commissioner for Patents
Alexandria, VA 22313-1450

Sir:

Prior to examination of the above-identified application, please enter the following amendments:

AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (Currently Amended) An output stage adapted to operate in at least a first operating state and a second operating state, the output stage comprising:

– a first, a second, a third and a fourth configurable input/output terminals ~~(T1, T2, T3, T4)~~; and,

– a first, a second, a third and a fourth switches ~~(S1, S2, S3, S4)~~, each having a first main terminal ~~(1)~~, a second main terminal ~~(2)~~ and a control terminal ~~(3)~~, the control terminal being adapted to receive a control signal for controlling the open or closed state of the switch;

wherein,

– the first input/output terminal is connected to the first main terminal of the first switch;

– the second input/output terminal is connected to the first main terminal of the second switch;

– the second main terminal of the first switch is connected to the first main terminal of the third switch through a first branch,

– the second main terminal of the second switch is connected to the first main terminal of the fourth switch through a second branch;

– the third input/output terminal is connected to the first branch and the fourth input/output terminal is connected to the second branch;

– the second main terminals of the third and fourth switches are both connected to a common node receiving a reference potential; and,

wherein,

– when the first and second input/output terminals are configured to operate as input terminals, the third and fourth input/output terminals are configured to operate as output terminals; and,

– when the first and second input/output terminals are configured to operate as output terminals, the third and fourth input/output terminals are configured to operate as input terminals; and,

wherein,

– in the first operating state, the output stage is arranged in a first electrical configuration; and

– in the second operating state wherein the output stage is arranged in a second electrical configuration different from the first configuration..

2. (Currently Amended) The output stage of claim 1, wherein, in the first operating state:

– the first and second input/output terminals are configured to operate as input terminals and are configured to be connected to a common node receiving a supply potential; and,

– the third and fourth input/output terminals are configured to be connected to a load element ~~(202)~~.

3. (Currently Amended) The output stage of claim 1 further comprising an inductor ~~(204)~~ and a decoupling capacitor ~~(205)~~, wherein, in the second operating state:

– the first and second input/output terminals are configured to operate as output terminals and are configured to be connected, in series with a load element ~~(30)~~ and in parallel with the decoupling capacitor;

– the third and fourth input/output terminals are short-circuited;

– one end of the inductor is configured to be connected to the short-circuited third and fourth input/output terminals and another end the inductor is configured to be connected to a common node receiving a supply potential.

4. (Currently Amended) The output stage of claim 1 further comprising an inductor ~~(212)~~ and a decoupling capacitor ~~(213)~~, wherein, in the second operating state:

– the first and second input/output terminals are configured to operate as input terminals and are configured to be connected to a common node receiving a supply potential;

– the third and fourth input/output terminals are short-circuited;

– one end of the inductor is configured to be connected to the short-circuited third and fourth input/output terminals and another end the inductor is configured to be connected, in series with a load element ~~(30)~~ and in parallel with the decoupling capacitor.

5. (Currently Amended) The output stage of claim 1 further comprising a first and second inductors ~~(207, 208)~~ and a first and second decoupling capacitors ~~(209, 210)~~, wherein, in the second operating state:

– the first and second input/output terminals are configured to operate as output terminals;

– the first input/output terminal is configured to be connected, in series with a first load element ~~(30)~~ and in parallel with the first decoupling capacitor;

– the second input/output terminal is configured to be connected, in series with a second load element ~~(40)~~ and in parallel with the second decoupling capacitor;

– one end of the first inductor is configured to be connected to the third input/output terminal and another end of the first inductor is configured to be connected to a common node receiving a supply potential; and

– one end of the second inductor is configured to be connected to the fourth input/output terminal and another end of the second inductor is configured to be connected to the common node receiving a supply potential.

6. (Currently Amended) The output stage of claim 1 further comprising a first and second inductors ~~(215, 217)~~ and a first and second decoupling capacitors ~~(216, 218)~~, wherein, in the second operating state:

– the first and second input/output terminals are configured to operate as input

terminals and are configured to be connected to a common node receiving a supply potential;

– one end of the first inductor is configured to be connected to the third input/output terminal and another end of the first inductor is configured to be connected, in series with a first load element ~~(30)~~ and in parallel with the first decoupling capacitor; and

– one end of the second inductor is configured to be connected to the fourth input/output terminal and another end of the second inductor is configured to be connected, in series with a second load element ~~(40)~~ and in parallel with the second decoupling capacitor.

7. (Currently Amended) The output stage of claim 1 further comprising a first and second inductors ~~(220, 223)~~ and a first and second decoupling capacitors ~~(221, 224)~~, wherein, in the second operating state:

– the first and second input/output terminals are configured to operate as input terminals;

– the third input/output terminal is configured to be connected, in series with a first load element ~~(30)~~ and in parallel with the first decoupling capacitor;

– one end of the first inductor is configured to be connected to the first input/output terminal and another end of the first inductor is configured to be connected to a first node receiving a supply potential; and

– one end of the second inductor is configured to be connected to the fourth input/output terminal and another end of the second inductor is configured to be connected, in series with a second load element ~~(40)~~ and in parallel with the second decoupling capacitor.

8. (Currently Amended) A control apparatus ~~(10)~~ comprising:

– a control stage configured to control an output stage according to claim 2.

9. (Original) The control apparatus of claim 8 wherein the control stage is a Class-D control stage.

10. (Currently Amended) A control apparatus ~~(20)~~ comprising:

– a control stage configured to control an output stage according to ~~any one of claims 3 to 7~~claim 3.

11. (Original) The control apparatus of claim 10 wherein the control stage is a DC-DC converter control stage.

12. (Currently Amended) The control apparatus of ~~anyone of claims 8 to 11~~claim 8, wherein the control stage is adapted to control the output stage by generating control signals for controlling the first, second, third and fourth switches through their respective control terminals.

13. (Currently Amended) A circuit comprising:

– an output stage according to ~~any one of claims 2 to 7~~claim 2;

– a first control apparatus ~~according to any one of claims 8 to 9 and 12~~ wherein the control stage of the first control apparatus is connected to the output stage; and,

– a second control apparatus ~~according to any one of claims 10 to 11 and 12~~ wherein the control stage of the second control apparatus is connected to the output stage;

wherein,

– when the control stage of the first control apparatus is connected to the output stage, the control stage of the second control apparatus is electrically disconnected from the output stage, the output stage being configured to operate in the first operating state; and,

– when the control stage of the second control apparatus is connected to the output stage, the control stage of the first control apparatus is electrically disconnected from the output stage, the output stage being configured to operate in the second operating state.

14. (Original) A device comprising:

– the circuit of claim 12;

– a battery configured to be connected to the input terminals of the circuit; and,

– a loudspeaker configured to be connected to the output terminals of the circuit.

15. (Currently Amended) Use of an output stage according to ~~any one of claims 2 to 7~~claim 2, in conjunction with:

– a first control apparatus ~~according to any one of claims 8 to 9 and 12~~ wherein the control stage of the first control apparatus is connected to the output stage; and,

– a second control apparatus ~~according to any one of claims 10 to 11 and 12~~ wherein the control stage of the second control apparatus is connected to the output stage;

wherein,

– when the control stage of the first control apparatus is connected to the output stage, the control stage of the second control apparatus is electrically disconnected from the output stage, the output stage being configured to operate in the first operating state; and,

– when the control stage of the second control apparatus is connected to the output stage, the control stage of the first control apparatus is electrically disconnected from the output stage, the output stage being configured to operate in the second operating state.

REMARKS

By this preliminary amendment, the claims have been amended to remove any multi-dependencies and place them in better form for U.S. examination. No new matter has been added. Prompt examination on the merits is respectfully requested.

Respectfully submitted,

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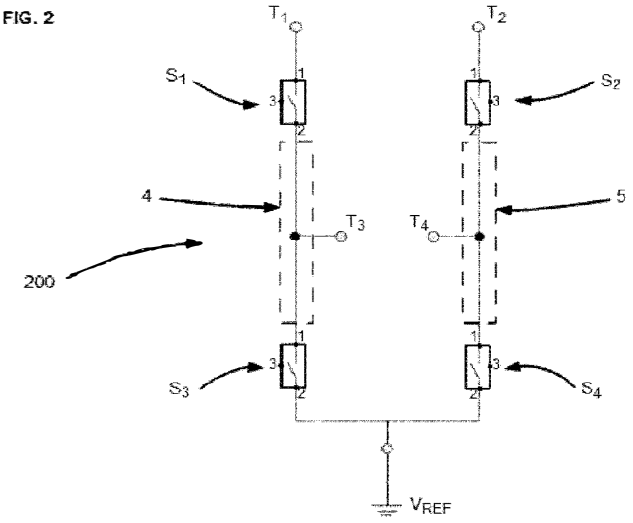
(54) **Title**: RECONFIGURABLE OUTPUT STAGE

FIG. 2



(57) **Abstract**: A circuit comprising: – an output stage according to the invention; – a first control apparatus comprising a control stage of the first control apparatus is connected to the output stage; and, – a second control apparatus comprising a control stage of the second control apparatus is connected to the output stage; wherein, – when the control stage of the first control apparatus is connected to the output stage, the control stage of the second control apparatus is electrically disconnected from the output stage, the output stage being configured to operate in a first operating state; and, – when the control stage of the second control apparatus is connected to the output stage, the control stage of the first control apparatus is electrically disconnected from the output stage, the output stage being configured to operate in a second operating state. The output stage and the use of the output stage are also claimed.

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Description

RECONFIGURABLE OUTPUT STAGE

Technical Field

[0001] The proposed solution relates generally to output stage circuits, and more especially to a reconfigurable output stage.

Background Art

[0002] Recently, designers of portable and other low power electronic devices have devised multimedia features in order for their products to attract more attention from potential customers. Internally to these devices, subsystem circuits such as audio subsystems have an increasingly important role on the realisation of these features and, thus, on user experience.

[0003] A typical audio subsystem, for instance, may combine in a single integrated circuit, various audio configurations for driving multiple output speakers such as a headphone, a hands-free loudspeaker and a receiver speaker, each of these audio configurations potentially having respective output power requirements. For instance, an audio subsystem may use a Class-D amplifier in different audio configurations for driving a circuit such as a hands–free loudspeaker. In fact, depending on the user's need and due to its high power and high efficiency, a Class-D amplifier may provide different levels of loudness. For example, when a medium loudness is required, e.g. 1W, the Class-D amplifier may be powered by the battery of the device. In this configuration the sound loudness would depend on the battery charge state. In another example, when a high loudness is required, e.g. 2W, the Class-D amplifier may be powered by a DC-DC boost converter. In this configuration, the sound loudness could be constant whatever the battery charge state.

[0004] However, with such type of audio subsystems, when only the medium loudness audio configuration is used the DC-DC boost converter is not used. This is inefficient and represents extra subsystems costs due to the unused die area.

Summary

[0005] There is thus a need for an improved subsystem circuit structure which maximises the die area usage and thus reduce the subsystem costs.

Therefore, it is proposed an output stage suitable for use in a subsystem circuit which can be shared between at least two subsystem circuit components. Namely, the proposed output stage may be adapted to work with particular subsystem circuit components. Hence, with the above example of the audio subsystem and contrary to the prior art, only one output stage is needed for both the Class-D amplifier and the DC-DC boost converter within an audio subsystem circuit structure. In fact in the prior art, two output stages are needed, i.e. one output stage for each of the Class-D amplifier and the DC-DC boost converter.

[0006] In a first aspect of the solution described herein, there is proposed an electronic circuit output stage adapted to operate in at least a first operating state and a second operating state, the output stage comprising:

– a first, a second, a third and a fourth configurable input/output terminals; and,

– a first, a second, a third and a fourth switches, each having a first main terminal, a second main terminal and a control terminal, the control terminal being adapted to receive a control signal for controlling the open or closed state of the switch;

wherein,

– the first input/output terminal is connected to the first main terminal of the first switch; – the second input/output terminal is connected to the first main terminal of the second switch;

– the second main terminal of the first switch is connected to the first main terminal of the third switch through a first branch,

– the second main terminal of the second switch is connected to the first main terminal of the fourth switch through a second branch;

– the third input/output terminal is connected to the first branch and the fourth input/output terminal is connected to the second branch;

– the second main terminals of the third and fourth switches are both connected to a common node receiving a reference potential; and,

wherein,

– when the first and second input/output terminals are configured to

operate as input terminals, the third and fourth input/output terminals are configured to operate as output terminals; and,

– when the first and second input/output terminals are configured to operate as output terminals, the third and fourth input/output terminals are configured to operate as input terminals; and,

wherein,

– in the first operating state, the output stage is arranged in a first electrical configuration; and

– in the second operating state wherein the output stage is arranged in a second electrical configuration different from the first configuration

[0007] In a first embodiment of the first aspect, in the first operating state:

– the first and second input/output terminals are configured to operate as input terminals and are configured to be connected to a common node receiving a supply potential; and,

– the third and fourth input/output terminals are configured to be connected to a load element.

[0008] Advantageously, this embodiment may allow creating a class-D configuration.

[0009] In a second embodiment of the first aspect, in the second operating state, the output stage may further comprise an inductor and a decoupling capacitor, wherein:

– the first and second input/output terminals are configured to operate as output terminals and are configured to be connected, in series with a load element and in parallel with the decoupling capacitor;

–the third and fourth input/output terminals are short-circuited ;

– one end of the inductor is configured to be connected to the short circuited third and fourth input/output terminals and another end the inductor is configured to be connected to a node receiving a supply potential.

[0010] Advantageously, this embodiment may allow creating a boost DCDC configuration.

[0011] In a third, alternative embodiment of the first aspect, in the second operating state, the output stage may further comprise an inductor and a

decoupling capacitor, wherein:

– the first and second input/output terminals are configured to operate as input terminals and are configured to be connected to a common node receiving a supply potential;

–the third and fourth input/output terminals are short-circuited;

– one end of the inductor is configured to be connected to the short-circuited third and fourth input/output terminals and another end the inductor is configured to be connected, in series with a load element and in parallel with the decoupling capacitor.

[0012] Advantageously, this embodiment may allow creating a buck DCDC configuration.

[0013] In a fourth possible embodiment of the first aspect, in the second operating state, the output stage may further comprise a first and second inductor and a first and second decoupling capacitor, wherein:

– the first and second input/output terminals are configured to operate as output terminals;

– the first input/output terminal is configured to be connected, in series with a first load element and in parallel with the first decoupling capacitor;

– the second input/output terminal is configured to be connected, in series with a second load element and in parallel with the second decoupling capacitor;

– one end of the first inductor is configured to be connected to the third input/output terminal and another end of the first inductor is configured to be connected to a common node receiving a supply potential;

– one end of the second inductor is configured to be connected to the fourth input/output terminal and another end of the second inductor is configured to be connected to the node receiving a supply potential.

[0014] Advantageously, this embodiment may allow creating a double boost DCDC.

[0015] In a fifth embodiment of the first aspect, in the second operating state, the output stage may further comprise a first and second inductor and a first and second decoupling capacitor, wherein:

– the first and second input/output terminals are configured to operate as

input terminals and are configured to be connected to a common node receiving a supply potential;

– one end of the first inductor is configured to be connected to the third input/output terminal and another end of the first inductor is configured to be connected, in series with a first load element and in parallel with the first decoupling capacitor;

– one end of the second inductor is configured to be connected to the fourth input/output terminal and another end of the second inductor is configured to be connected, in series with a second load element and in parallel with the second decoupling capacitor.

[0016] Advantageously, this embodiment may allow creating a double buck DCDC.

[0017] For instance, in a sixth embodiment of the first aspect, in the second operating state, the output stage may further comprise a first and second inductor and a first and second decoupling capacitor, wherein:

– the first and second input/output terminals are configured to operate as input terminals;

– the third input/output terminal is configured to be connected, in series with a first load element and in parallel with the first decoupling capacitor;

– one end of the first inductor is configured to be connected to the first input/output terminal and another end of the first inductor is configured to be connected to a first node receiving a supply potential;

– one end of the second inductor is configured to be connected to the fourth input/output terminal and another end of the second inductor is configured to be connected, in series with a second load element and in parallel with the second decoupling capacitor.

[0018] Advantageously, this embodiment may allow creating a double DCDC, comprising a buck configuration, and a boost configuration.

[0019] In a second aspect of the solution, there is proposed a control apparatus comprising:

– a control stage configured to control an output stage according to the first embodiment of the first aspect.

[0020] In an embodiment of the second aspect, the control stage is a Class-D control stage.

[0021] In a third aspect of the solution, there is proposed a control apparatus comprising:

– a control stage configured to control an output stage according to any one of the second to sixth embodiments of the first aspect.

[0022] In an embodiment of the third aspect, the control stage is a DC-DC converter control stage.

[0023] In an embodiment of second and/or third aspects, the control stage is adapted to control the output stage by generating control signals for controlling the first, second, third and fourth switches through their respective control terminals.

[0024] In a fourth aspect of the solution, there is proposed a circuit comprising:

– an output stage according to any one of the first to the sixth embodiments of the first aspect;

– a first control apparatus according to the second aspect wherein the control stage of the first control apparatus is connected to the output stage; and,

– a second control apparatus according to the third aspect wherein the control stage of the second control apparatus is connected to the output stage, wherein:

– when the control stage of the first control apparatus is connected to the output stage, the control stage of the second control apparatus is electrically disconnected from the output stage, the output stage being configured to operate in the first operating state; and,

– when the control stage of the second control apparatus is connected to the output stage, the control stage of the first control apparatus is electrically disconnected from the output stage, the output stage being configured to operate in the second operating state.

[0025] In a fifth aspect of the solution, there is proposed a device comprising:

– the circuit of the fourth aspect;

– a battery configured to be connected to the input terminals of the circuit; and,

– a loudspeaker configured to be connected to the output terminals of the circuit.

[0026] In a sixth aspect of the solution, there is proposed the use of an output stage according to any one of the first to the sixth embodiments of the first aspect in conjunction with:

– a first control apparatus according to the second aspect wherein the control stage of the first control apparatus is connected to the output stage; and,

– a second control apparatus according to the third aspect wherein the control stage of the second control apparatus is connected to the output stage, wherein:

– when the control stage of the first control apparatus is connected to the output stage, the control stage of the second control apparatus is electrically disconnected from the output stage, the output stage being configured to operate in the first operating state; and,

– when the control stage of the second control apparatus is connected to the output stage, the control stage of the first control apparatus is electrically disconnected from the output stage, the output stage being configured to operate in the second operating state.

Brief description of drawings

[0027] A more complete understanding of the proposed solution may be obtained from a consideration of the following description in conjunction with the drawings, in which like reference numbers indicate same or similar elements. In the drawings:

[0028] FIG. 1 is a block diagram illustrating an audio subsystem;

[0029] FIG. 2 is a block diagram illustrating an exemplary output stage of the proposed solution;

[0030] FIGs. 3-8 are a block diagrams illustrating embodiments of the proposed solution.

Description of embodiments

[0031] The following detailed description is exemplary in nature and is not intended to limit the scope, applicability, or configuration of the invention in any way. Rather, the following description provides practical illustrations

for implementing exemplary embodiments of the present invention. Examples of constructions, materials, dimensions, and manufacturing processes are provided for selected elements, and all other elements employ that which is known to those of skill in the field of the invention. Those skilled in the art will recognize that many of the examples provided have suitable alternatives that can be utilized.

[0032] FIG. 1 is a block diagram schematically illustrating an audio subsystem 100.

[0033] In FIG. 1, there is shown therein the audio subsystem 100 comprising one audio DAC unit 110 (i.e. Digital to Analog Converter), one gain matrix unit 120, one class-AB amplifiers 130 , two class-AB amplifiers 150, one Class-D amplifier 140, one ear speaker 160, one hands-free speaker 170 and one headphone 180. It is considered herein that there are two class-AB amplifiers 150 that can drive a stereo headphone.

[0034] Referring to FIG. 1, the audio DAC 110 is coupled to the gain matrix 120, which is coupled to the amplifiers 130, 140, 150, which are respectively coupled to the ear speaker 160, the hands-free speaker 170 and the headphone 180.

[0035] The DAC 110 aims at generating at least one audio signal which gain may be modified by the gain matrix 120 prior being amplified by an amplifier 130, 140, 150 and being reproduced by a speaker 160, 170, 180.

[0036] As stated above, the Class-D amplifier 140 may be used in different audio configurations depending on the user's need of loudness. However, different circuit components may be used in different audio configurations thus resulting in a waste of circuit die area when only one or more of the circuit components are in used while the others are not.

[0037] By way of example, let's consider a case where the Class-D amplifier 140 and a DC-DC boost converter are the circuit components used in one or more audio configurations to drive a speaker, 170. It is indicated that other configurations and other components may be used herein. Each of the Class-D amplifier 140 and the DC-DC boost converter is usually organised into two parts:

- a output stage providing the required output; and,

- a control stage for controlling the output stage .

However in the proposed example, when the Class-D is used alone in the audio configuration (e.g. for a medium output loudness), only the control stage and output stage of the Class-D amplifier are used while the control stage and output stage of the DC-DC boost converter are not used. As stated above, this situation results in wastage of the circuit die area.

[0038] In order to solve this problem, it is proposed an electronic circuit output stage adapted to operate in at least a first operating state and a second operating state, such that the output stage may be shared by at least two circuit components such as the Class-D amplifier and the DC-DC boost converter. This way in the example proposed above, the proposed control stage would always be in used in all associated audio configurations.

[0039] FIG. 2 is a block diagram schematically illustrating an exemplary output stage 200 according to the proposed solution.

[0040] In FIG. 2, there is shown therein the output stage 200 comprising:

– a first configurable input/output terminal T_1, a second configurable input/output terminal T_2, a third configurable input/output terminal T_3 and a fourth configurable input/output terminal T_4; and,

– a first switch S_1, a second switch S_2, a third switch S_3 and a fourth switch S_4. The switches S1, S2, S3, S4 may be MOS transistors, NMOS transistors or other transistors of the same or different kind.

[0041] Referring to FIG. 2, the configurable input/output terminal T_1, T_2, T_3, T_4 are configured to operate as input or output terminals such that:

– when the first input/output terminal T1 and second input/output terminal T2 are configured to operate as input terminals, the third input/output terminal T3 and fourth input/output terminal T4 are configured to operate as output terminals; and,

– when the first input/output terminal T1 and second input/output terminal T2 are configured to operate as output terminals, the third input/output terminal T3 and fourth input/output terminal T4 are configured to operate as input terminals.

[0042] Further in FIG. 2, each of the switches S_1, S_2, S_3, S_4 has a first main terminal 1, a second main terminal 2 and a control terminal 3 wherein the

control terminal 3 is adapted to receive a control signal for controlling the open or closed state of the associated switch.

[0043] Structurally, the output stage 200 is organised as follows. The first input/output terminal T1 is connected to the first main terminal 1 of the first switch S1. The second input/output terminal T2 is connected to the first main terminal 1 of the second switch S2. The second main terminal 2 of the first switch S1 is connected to the first main terminal 1 of the third switch S3. The latter connection is forming a first branch 4 of the output stage 200. The second main terminal 2 of the second switch S2 is connected to the first main terminal 1 of the fourth switch s4. The latter connection is forming a second branch 5 of the output stage 200. The third input/output terminal T3 is connected to the first branch 4 of the output stage 200 and the fourth input/output terminal T4 is connected to the second branch 5 of the output stage 200. The second main terminal 2 of the third switch S3 and the second main terminal 2 of fourth switches S4 are both connected to a common node receiving a reference potential VREF of the output stage 200.

[0044] Referring to FIG. 2, when in the first operating state, the output stage is arranged in a first electrical configuration, and when in the second operating state wherein the output stage is arranged in a second electrical configuration different from the first configuration.

[0045] FIG. 3 is a block diagram schematically illustrating a first exemplary embodiment of the proposed solution wherein the output stage 200 of FIG.2 is used, in the first operating state.

[0046] In the example of FIG. 3, the first input/output terminal T1 and second input/output terminal T2 are configured to operate as input terminals and are also configured to be connected to a common node receiving a supply potential 201. The common node receiving a supply potential 201 may be a battery, a DC-DC boost converter or any similar DC power source which needs to be recharged on a periodic basis. Further, in FIG. 3, the third input/output terminal T3 and fourth input/output terminal T4 are configured to be connected to a load element. For example, the load element may be an audio speaker 202. In such case, the third input/output terminal T3 and

fourth input/output terminal T4 may be connected respectively with a first and second end of the audio speaker 202. In another example, the load element may be a motor such as a vibration motor usually used in mobile phone. It is indicated that other components may be used herein. As can be seen, the structure of the output stage 200 in the example of FIG. 3 is an H-bridge circuit structure, thus the output stage 200 may be controlled by an H-bridge control stage 10. Namely, the switches S1, S2, S3, S4 of the output stage 200 may be controlled by the H-bridge control stage 10. In the case of audio subsystems, the H-bridge control stage 10 may be the control stage of a Class-D amplifier. If it is the case, the combination of a Class-D amplifier control stage and the output stage 200 of the FIG. 3 would correspond to the realisation of a Class-D amplifier.

[0047] FIG. 4 is a block diagram schematically illustrating a second exemplary embodiment of the proposed solution wherein the output stage 200 of FIG.2 is used, in the second operating state.

[0048] In the example of FIG. 4, the output stage 200 may further comprise one inductor 204 and one decoupling capacitor 205. Further, in FIG. 4, the first input/output terminal T1 and second input/output terminal T2 are configured to operate as output terminals and are also configured to be connected, in series with a load element 30 and, in parallel with the decoupling capacitor 205. In this configuration, the decoupling capacitor 205 is used for removing on-chip high frequency noise. Also, in FIG. 4, the third input/output terminal T3 and fourth input/output terminal T4 are short-circuited 6. Additionally, in FIG. 4, one end of the inductor 204 is configured to be connected to the short-circuit 6 and another end the inductor 204 is configured to be connected to a common node receiving a supply potential 203 similar to those already presented in FIG. 3. As can be seen, the structure of the output stage 200 in the example of FIG. 4 is not an H-bridge circuit structure since the load element is not on the central branch of the structure. Rather, the structure of the output stage 200 in the example of FIG. 4 may be seen as two branches 4, 5 which are arranged in parallel. Therefore, any control stage 20 that may control such structure may be used. In one embodiment, the control stage 20 may use

the same signal to control two switches S1, S2, S3, S4 which are situated on parallel branches of the output stage 200 of the FIG. 4. In this case, the output stage 200 would be similar to a circuit structure comprising only a single branch. In this case, a DC-DC control stage may be used to control the output stage 200 in the example of FIG. 4. If it is the case, the combination of a DC-DC control stage and the output stage 200 of the FIG. 4 would correspond to the realisation of a DC-DC boost converter configured to, at least, step-up an input voltage.

[0049] FIG. 5 is a block diagram schematically illustrating a third exemplary embodiment of the proposed solution wherein the output stage 200 of FIG.2 is used, in the second operating state.

[0050] In the example of FIG. 5, the output stage 200 may further comprise one inductor 212 and one decoupling capacitor 213 similar to those already presented in FIG 4. Further, in FIG. 5, the first input/output terminal T1 and second input/output terminal T2 are configured to operate as input terminals and are also configured to be connected to a common node receiving a supply potential 203 similar to those already presented in FIG. 3. Also, in FIG. 5, a short circuit 6 is created between the third input/output terminal T3 and fourth input/output terminal T4. Additionally, in FIG. 5, one end of the inductor 212 is configured to be connected to the short circuit 6 and another end the inductor 212 is configured to be connected, in series with a load element 30 and, in parallel with the decoupling capacitor 213. As can be seen, the structure of the output stage 200 in the example of FIG. 4 is not an H-bridge circuit structure since the load element 30 is not directed connected to the central branch of the structure. Rather, the structure of the output stage 200 in the example of FIG. 5 may be seen as having, mutatis mutandis, the same structure presented in FIG. 4. Thus, in one embodiment, the control stage 20 may be a DC-DC control stage which may be used to control the output stage 200 in the example of FIG. 5. If it is the case, the combination of a DC-DC control stage and the output stage 200 of the FIG. 5 would correspond to the realisation of a DC-DC buck converter configured to, at least, step-down an input voltage.

[0051] FIG. 6 is a block diagram schematically illustrating a fourth exemplary embodiment of the proposed solution wherein the output stage 200 of FIG.2 is used, in the second operating state.

[0052] In the example of FIG. 6, the output stage 200 may further comprise one first inductor 207, one second inductor 208, one first decoupling capacitor 209 and one second decoupling capacitor 210. Further, in FIG. 6, the first input/output terminal T1 and second input/output terminal T2 are configured to operate as output terminals. The first input/output terminal T1 is further configured to be connected, in series with a first load element 30 and in parallel with the first decoupling capacitor 209. The second input/output terminal T2 is further configured to be connected, in series with a second load element 40 and in parallel with the second decoupling capacitor 210. Also, one end of the first inductor 207 is configured to be connected to the third input/output terminal T3 and another end of the first inductor 207 is configured to be connected to a common node receiving a supply potential 206 similar to those already presented in FIG. 3. Additionally, one end of the second inductor 208 is configured to be connected to the fourth input/output terminal T4 and another end of the second inductor 208 is configured to be connected to the above-mentioned common node receiving a supply potential 206. As can be seen, the structure of the output stage 200 in the example of FIG. 6 is not an H-bridge circuit structure since the load elements 30, 40 are not directed connected to the central branch of the structure. Rather, the structure of the output stage 200 in the example of FIG. 6 may be seen as having, mutatis mutandis, the same structure presented in FIG. 4. Thus, in one embodiment, the control stage 20 may be a DC-DC control stage which may be used to control the output stage 200 in the example of FIG. 6. If it is the case, the combination of a DC-DC control stage and the output stage 200 of the FIG. 6 would correspond to the realisation of a double DC-DC boost converter configured to, at least, step-up an input voltage. Also, due to the fact that each branch of the structure may be controlled independently by the control stage 20, using a DC-DC control stage enables to generate different voltage on each branch 4,5 of the

output stage that may be used to supply in voltage the load elements 30, 40.

[0053] FIG. 7 is a block diagram schematically illustrating a fifth exemplary embodiment of the proposed solution wherein the output stage 200 of FIG.2 is used, in the second operating state.

[0054] In the example of FIG. 7, the output stage 200 may further comprise one first inductor 215, one second inductor 217, one first decoupling capacitor 216 and one second decoupling capacitor 218. Further, in FIG. 7, the first input/output terminal T1 and second input/output terminal T2 are configured to operate as input terminals and are configured to be connected to a common node receiving a supply potential 214 similar to those already presented in FIG. 3. Also, one end of the first inductor 215 is configured to be connected to the third input/output terminal T3 and another end of the first inductor 215 is configured to be connected, in series with a first load element 30 and in parallel with the first decoupling capacitor 216. Additionally, one end of the second inductor 217 is configured to be connected to the fourth input/output terminal T4 and another end of the second inductor 217 is configured to be connected, in series with a second load element 40 and in parallel with the second decoupling capacitor 218. As can be seen, the structure of the output stage 200 in the example of FIG. 7 is not an H-bridge circuit structure since the load elements 30, 40 are not directed connected to the central branch of the structure. Rather, the structure of the output stage 200 in the example of FIG. 7 may be seen as having, mutatis mutandis, the same structure presented in FIG. 4. Thus, in one embodiment, the control stage 20 may be a DC-DC control stage which may be used to control the output stage 200 in the example of FIG. 7. If it is the case, the combination of a DC-DC control stage and the output stage 200 of the FIG. 7 would correspond to the realisation of a double DC-DC buck converter configured to, at least, step-down an input voltage. Also, due to the fact that each branch of the structure may be controlled independently by the control stage 20, using a DC-DC control stage enables to generate

different voltage on each branch 4,5 of the output stage that may be used to supply in voltage the load elements 30, 40.

[0055] FIG. 8 is a block diagram schematically illustrating a sixth exemplary embodiment of the proposed solution wherein the output stage 200 of FIG.2 is used, in the second operating state. Actually, the example of FIG.8 may correspond to a mix between the circuit structures of the examples of FIGs. 6-7.

[0056] Namely, in the example of FIG. 8, the output stage 200 may further comprise one first inductor 220, one second inductor 223, one first decoupling capacitor 221 and one second decoupling capacitor 224. Further, in FIG. 8, the first input/output terminal T1 and second input/output terminal T2 are configured to operate as input terminals. The third input/output terminal T3 is configured to be connected, in series with a first load element 30 and in parallel with the first decoupling capacitor 221. Also, one end of the first inductor 220 is configured to be connected to the first input/output terminal T1 and another end of the first inductor 220 is configured to be connected to a first node receiving a supply potential 219 similar to those already presented in FIG. 3. Additionally, one end of the second inductor 223 is configured to be connected to the fourth input/output terminal T4 and another end of the second inductor 223 is configured to be connected, in series with a second load element 40 and in parallel with the second decoupling capacitor 224. As can be seen, the structure of the output stage 200 in the example of FIG. 8 is not an H-bridge circuit structure al already explained above. Rather, the structure of the output stage 200 in the example of FIG. 6 may be seen as having, mutatis mutandis, the same structure presented in FIGs. 6-7. Thus, in one embodiment, the control stage 20 may be a DC-DC control stage which may be used to control the output stage 200 in the example of FIG. 6. If it is the case, the combination of a DC-DC control stage and the output stage 200 of the FIG. 6 would correspond to the realisation of a DC-DC buck-boost converter configured to, at least, step-up an input voltage in the first branch 4 of the output stage 200 and step-down an input voltage in the second branch 5 of the output stage 200. This is mainly due to the

fact that each branch of the structure may be controlled independently by the control stage 20, using a DC-DC control stage enables to generate different voltage on each branch 4,5 of the output stage that may be used to supply in voltage the load elements 30, 40.

[0057] In one embodiment, the switches S1, S2, S3, S4 may be controlled trough their respective control terminals based on control signals such a PWM signal which may be generated by a control stage 10, 20.

[0058] Several apparatuses such as control apparatuses may be realized based on the proposed solution. For example, a first control apparatus may comprise a control stage configured to control an output stage according to example of FIG. 3. In another example, a second control apparatus may comprise a control stage configured to control an output stage according to at least one of the examples of FIGs. 4-8.

[0059] Several uses and circuits may also be realized based on the proposed solution. In an example, a first circuit may comprise:

– an output stage according to at least one of the examples of FIGs. 3-8;

– the first control apparatus wherein the control stage of the first control apparatus is connected to the output stage; and,

– the second control apparatus wherein the control stage of the second control apparatus is connected to the output stage;

wherein,

– when the control stage of the first control apparatus is connected to the output stage, the control stage of the second control apparatus is electrically disconnected from the output stage, the output stage being configured to operate in the first operating state; and,

– when the control stage of the second control apparatus is connected to the output stage, the control stage of the first control apparatus is electrically disconnected from the output stage, the output stage being configured to operate in the second operating state.

[0060] In an example, such circuit may be used to drive a stereo hands free speaker. In that case, the first control apparatus may be a class-D controller and the second control apparatus may be a DC-DC controller.

This way, in a first operating state of the output stage, the circuit may be configured to behave as a class-D amplifier according for instance to FIG.3 wherein the load would be the stereo hands free speaker. In this case, the second control apparatus may be deactivated. In a second operating state of the output stage, the circuit may be configured to behave as a DC-DC converter. According to FIG.4, for instance, the circuit may be a DC-DC boost converter where the load 30 would be the stereo hands free speaker. According to FIG.5, for instance, the circuit may be a DC-DC buck converter where the load 30 would be the stereo hands free speaker. According to FIG.6, for instance, the circuit may be a double DC-DC boost converter where the loads 30, 40 may be different terminals of the stereo hands free speaker. According to FIG.7, for instance, the circuit may be a double DC-DC buck converter where the loads 30, 40 may be different terminals of the stereo hands free speaker. Finally, according to FIG.8, for instance, the circuit may be a DC-DC buck-boost converter able to drive different loads 30, 40 for voltage step-up or step-down wherein at least one may be the stereo hands free speaker.

[0061] Several devices, such as portable devices, may also be realized based on the proposed solution. For example, a device may comprise:

– the first circuit;

– a battery configured to be connected to the input terminals of the circuit; and,

– a loudspeaker configured to be connected to the output terminals of the circuit.

[0062] Although the proposed solution is described above in terms of various exemplary embodiments and implementations, it should be understood that the various features, aspects and functionality described in one or more of the individual embodiments are not limited in their applicability to the particular embodiment with which they are described, but instead may be applied, alone or in various combinations, to one or more of the other embodiments of the proposed solution, whether or not such embodiments are described and whether or not such features are presented as being a part of a described embodiment. Thus, the breadth and scope of the

present proposed solution should not be limited by any of the above-described exemplary embodiments. For instance, it is to appreciated that the output and the circuit may be used in other industries different from the audio that has been presented throughout the description. For example, the DC-DC feature of the circuit may be used in motor-based applications.

[0063] Terms and phrases used in this document, and variations thereof, unless otherwise expressly stated, should be construed as open ended as opposed to limiting. As examples of the foregoing: the term “including” should be read as meaning “including, without limitation” or the like; the term “example” is used to provide exemplary instances of the item in discussion, not an exhaustive or limiting list thereof; the terms “a” or “an” should be read as meaning “at least one,” “one or more” or the like; and adjectives such as “conventional,” “traditional,” “normal,” “standard,” “known” and terms of similar meaning should not be construed as limiting the item described to a given time period or to an item available as of a given time, but instead should be read to encompass conventional, traditional, normal, or standard technologies that may be available or known now or at any time in the future. Likewise, where this document refers to technologies that would be apparent or known to one of ordinary skill in the art, such technologies encompass those apparent or known to the skilled artisan now or at any time in the future.

[0064] The presence of broadening words and phrases such as “one or more, least,” “but not limited to” or other like phrases in some instances shall not be read to mean that the narrower case is intended or required in instances where such broadening phrases may be absent. Additionally, the various embodiments set forth herein are described in terms of exemplary block diagrams, flow charts and other illustrations. As will become apparent to one of ordinary skill in the art after reading this document, the illustrated embodiments and their various alternatives may be implemented without confinement to the illustrated examples. These illustrations and their accompanying description should not be construed as mandating a particular architecture or configuration.

Claims

1. An output stage adapted to operate in at least a first operating state and a second operating state, the output stage comprising:

– a first, a second, a third and a fourth configurable input/output terminals (T1, T2, T3, T4); and,

– a first, a second, a third and a fourth switches (S1, S2, S3, S4), each having a first main terminal (1), a second main terminal (2) and a control terminal (3), the control terminal being adapted to receive a control signal for controlling the open or closed state of the switch;

wherein,

– the first input/output terminal is connected to the first main terminal of the first switch;

– the second input/output terminal is connected to the first main terminal of the second switch;

– the second main terminal of the first switch is connected to the first main terminal of the third switch through a first branch,

– the second main terminal of the second switch is connected to the first main terminal of the fourth switch through a second branch;

– the third input/output terminal is connected to the first branch and the fourth input/output terminal is connected to the second branch;

– the second main terminals of the third and fourth switches are both connected to a common node receiving a reference potential; and,

wherein,

– when the first and second input/output terminals are configured to operate as input terminals, the third and fourth input/output terminals are configured to operate as output terminals; and,

– when the first and second input/output terminals are configured to operate as output terminals, the third and fourth input/output terminals are configured to operate as input terminals; and,

wherein,

– in the first operating state, the output stage is arranged in a first electrical configuration; and

– in the second operating state wherein the output stage is arranged in a second electrical configuration different from the first configuration..

2. The output stage of claim 1, wherein, in the first operating state:

– the first and second input/output terminals are configured to operate as input terminals and are configured to be connected to a common node receiving a supply potential; and,

– the third and fourth input/output terminals are configured to be connected to a load element (202).

3. The output stage of claim 1 further comprising an inductor (204) and a decoupling capacitor (205), wherein, in the second operating state:

– the first and second input/output terminals are configured to operate as output terminals and are configured to be connected, in series with a load element (30) and in parallel with the decoupling capacitor;

– the third and fourth input/output terminals are short-circuited;

– one end of the inductor is configured to be connected to the short-circuited third and fourth input/output terminals and another end the inductor is configured to be connected to a common node receiving a supply potential.

4. The output stage of claim 1 further comprising an inductor (212) and a decoupling capacitor (213), wherein, in the second operating state:

– the first and second input/output terminals are configured to operate as input terminals and are configured to be connected to a common node receiving a supply potential;

– the third and fourth input/output terminals are short-circuited;

– one end of the inductor is configured to be connected to the short-circuited third and fourth input/output terminals and another end the inductor is configured to be connected, in series with a load element (30) and in parallel with the decoupling capacitor.

5. The output stage of claim 1 further comprising a first and second inductors (207, 208) and a first and second decoupling capacitors (209, 210), wherein, in the second operating state:

– the first and second input/output terminals are configured to operate as output terminals;

– the first input/output terminal is configured to be connected, in series with a

first load element (30) and in parallel with the first decoupling capacitor;

– the second input/output terminal is configured to be connected, in series with a second load element (40) and in parallel with the second decoupling capacitor;

– one end of the first inductor is configured to be connected to the third input/output terminal and another end of the first inductor is configured to be connected to a common node receiving a supply potential;

– one end of the second inductor is configured to be connected to the fourth input/output terminal and another end of the second inductor is configured to be connected to the common node receiving a supply potential.

6. The output stage of claim 1 further comprising a first and second inductors (215, 217) and a first and second decoupling capacitors (216, 218), wherein, in the second operating state:

– the first and second input/output terminals are configured to operate as input terminals and are configured to be connected to a common node receiving a supply potential;

– one end of the first inductor is configured to be connected to the third input/output terminal and another end of the first inductor is configured to be connected, in series with a first load element (30) and in parallel with the first decoupling capacitor;

– one end of the second inductor is configured to be connected to the fourth input/output terminal and another end of the second inductor is configured to be connected, in series with a second load element (40) and in parallel with the second decoupling capacitor.

7. The output stage of claim 1 further comprising a first and second inductors (220, 223) and a first and second decoupling capacitors (221, 224), wherein, in the second operating state:

– the first and second input/output terminals are configured to operate as input terminals;

– the third input/output terminal is configured to be connected, in series with a first load element (30) and in parallel with the first decoupling capacitor;

– one end of the first inductor is configured to be connected to the first input/output terminal and another end of the first inductor is configured to be

connected to a first node receiving a supply potential;

– one end of the second inductor is configured to be connected to the fourth input/output terminal and another end of the second inductor is configured to be connected, in series with a second load element (40) and in parallel with the second decoupling capacitor.

8. A control apparatus (10) comprising:

– a control stage configured to control an output stage according to claim 2.

9. The control apparatus of claim 8 wherein the control stage is a Class-D control stage.

10. A control apparatus (20) comprising:

– a control stage configured to control an output stage according to any one of claims 3 to 7.

11. The control apparatus of claim 10 wherein the control stage is a DC-DC converter control stage.

12. The control apparatus of anyone of claims 8 to 11, wherein the control stage is adapted to control the output stage by generating control signals for controlling the first, second, third and fourth switches through their respective control terminals.

13. A circuit comprising:

– an output stage according to any one of claims 2 to 7;

– a first control apparatus according to any one of claims 8 to 9 and 12 wherein the control stage of the first control apparatus is connected to the output stage; and,

– a second control apparatus according to any one of claims 10 to 11 and 12 wherein the control stage of the second control apparatus is connected to the output stage;

wherein,

– when the control stage of the first control apparatus is connected to the output stage, the control stage of the second control apparatus is electrically disconnected from the output stage, the output stage being configured to operate in the first operating state; and,

– when the control stage of the second control apparatus is connected to the output stage, the control stage of the first control apparatus is electrically

disconnected from the output stage, the output stage being configured to operate in the second operating state.

14. A device comprising:

– the circuit of claim 12;

– a battery configured to be connected to the input terminals of the circuit; and,

– a loudspeaker configured to be connected to the output terminals of the circuit.

15. Use of an output stage according to any one of claims 2 to 7, in conjunction with:

– a first control apparatus according to any one of claims 8 to 9 and 12 wherein the control stage of the first control apparatus is connected to the output stage; and,

– a second control apparatus according to any one of claims 10 to 11 and 12 wherein the control stage of the second control apparatus is connected to the output stage;

wherein,

– when the control stage of the first control apparatus is connected to the output stage, the control stage of the second control apparatus is electrically disconnected from the output stage, the output stage being configured to operate in the first operating state; and,

– when the control stage of the second control apparatus is connected to the output stage, the control stage of the first control apparatus is electrically disconnected from the output stage, the output stage being configured to operate in the second operating state.

Drawings

FIG. 1

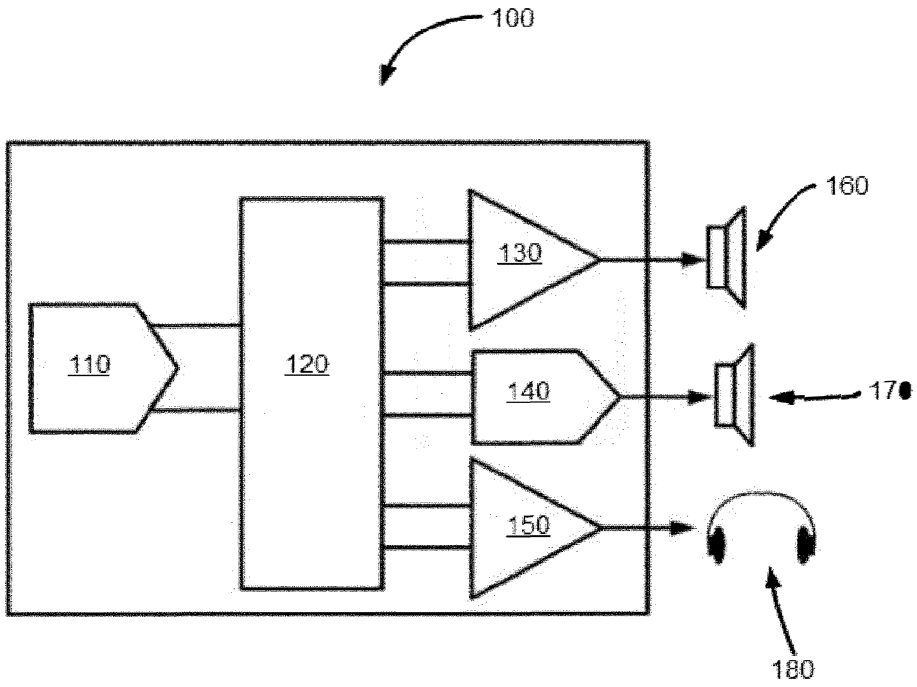


FIG. 2

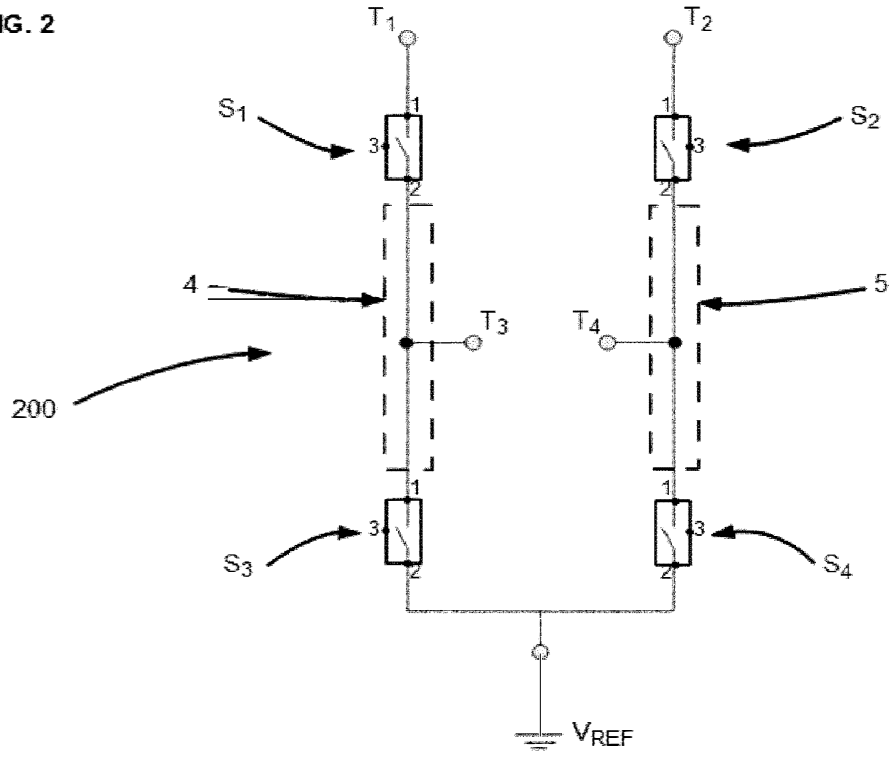
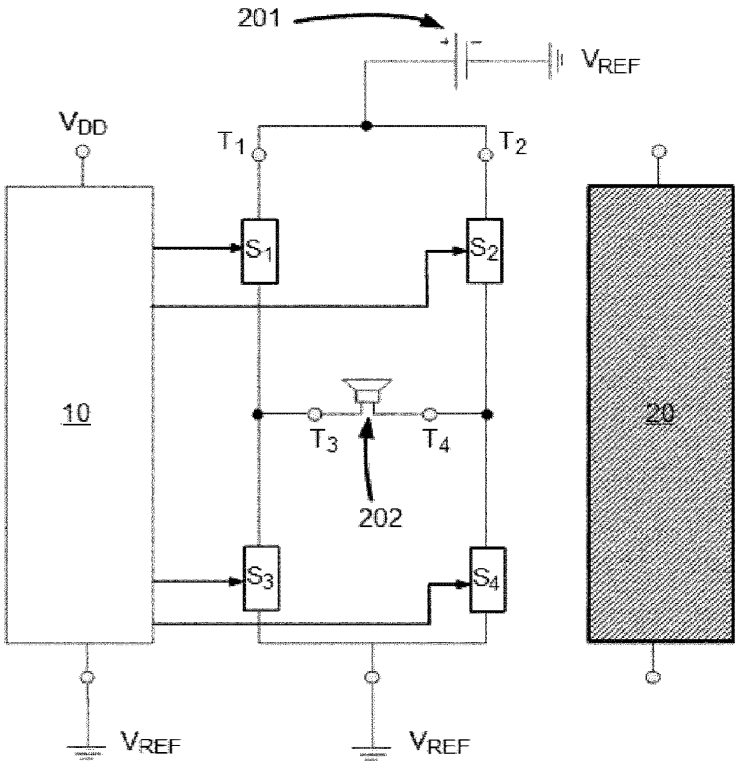


FIG. 3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T_1
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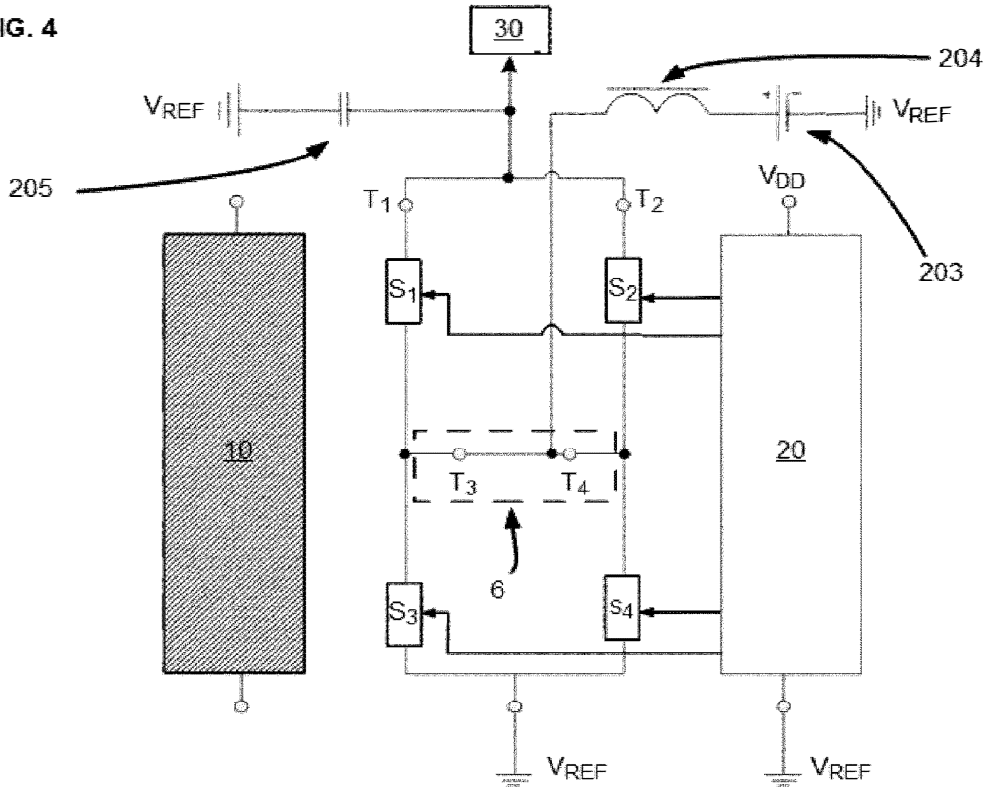
V_{REF}

FIG. 4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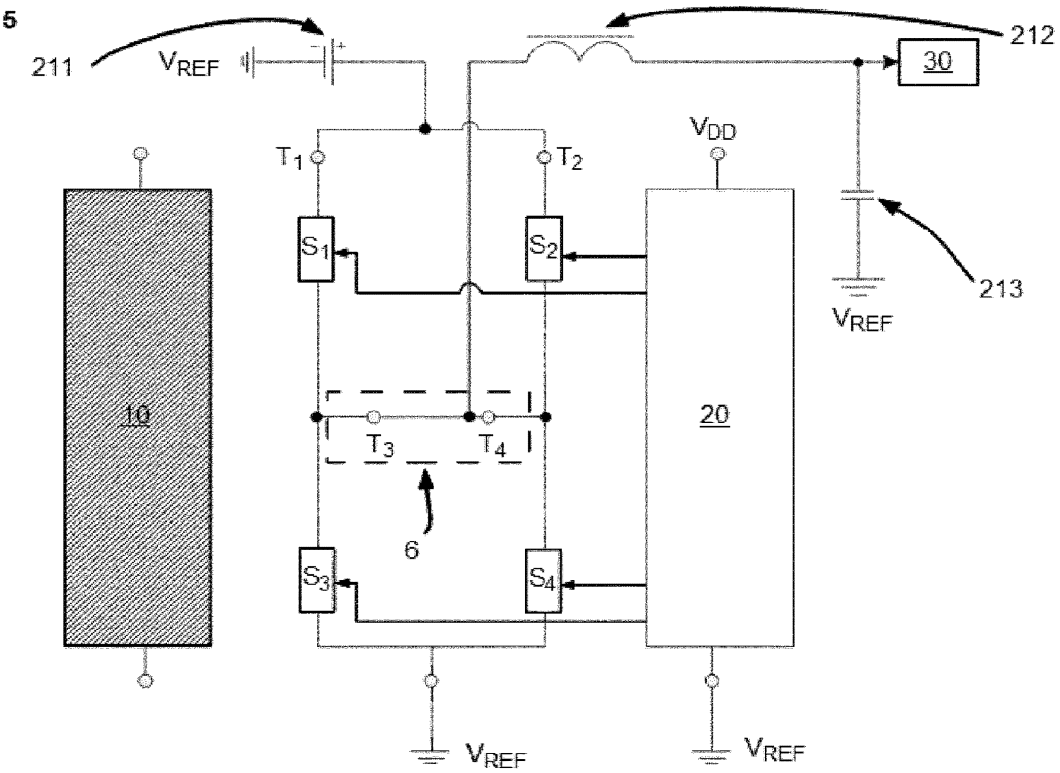
V_{REF}

FIG. 5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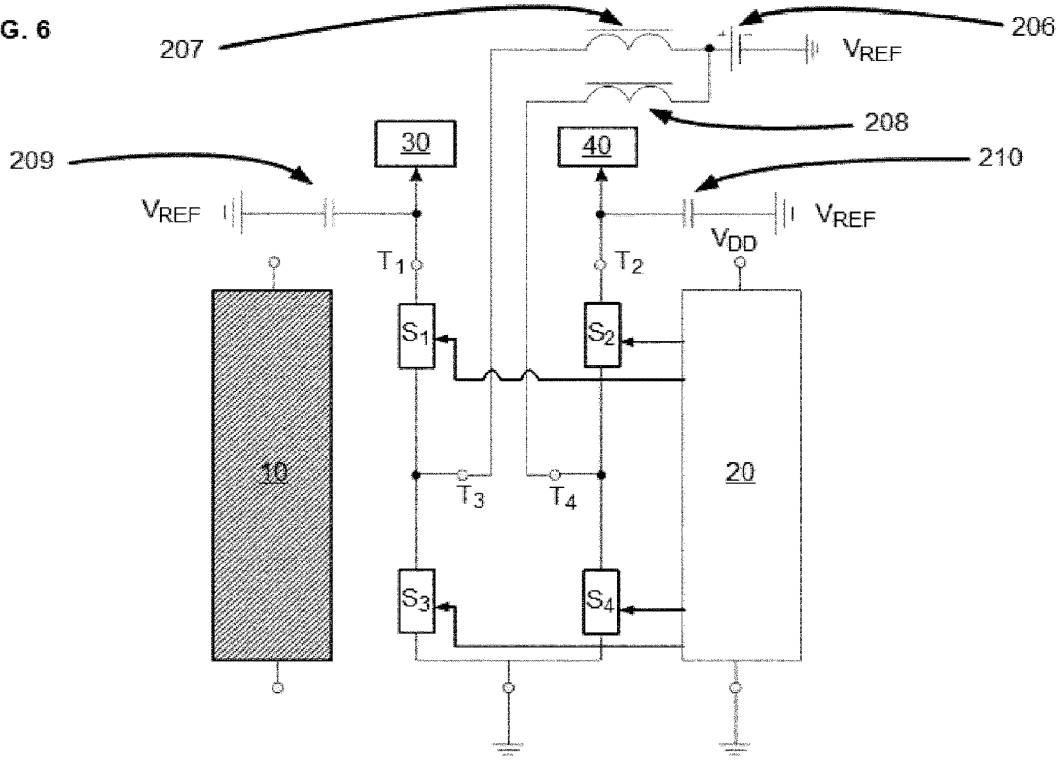
V_{REF}

FIG. 6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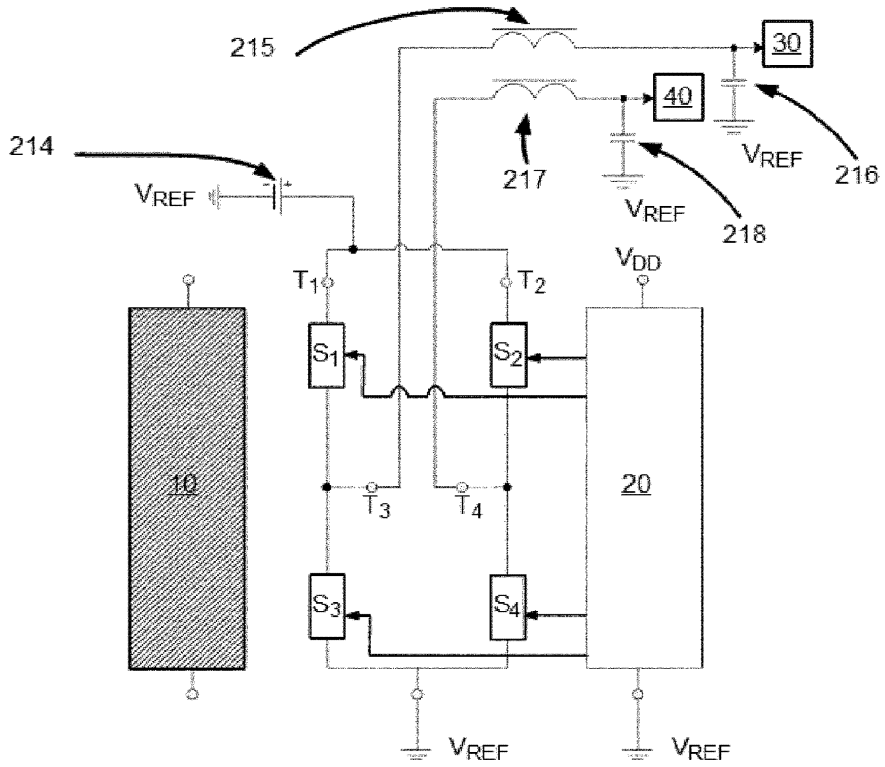
S_4

FIG. 7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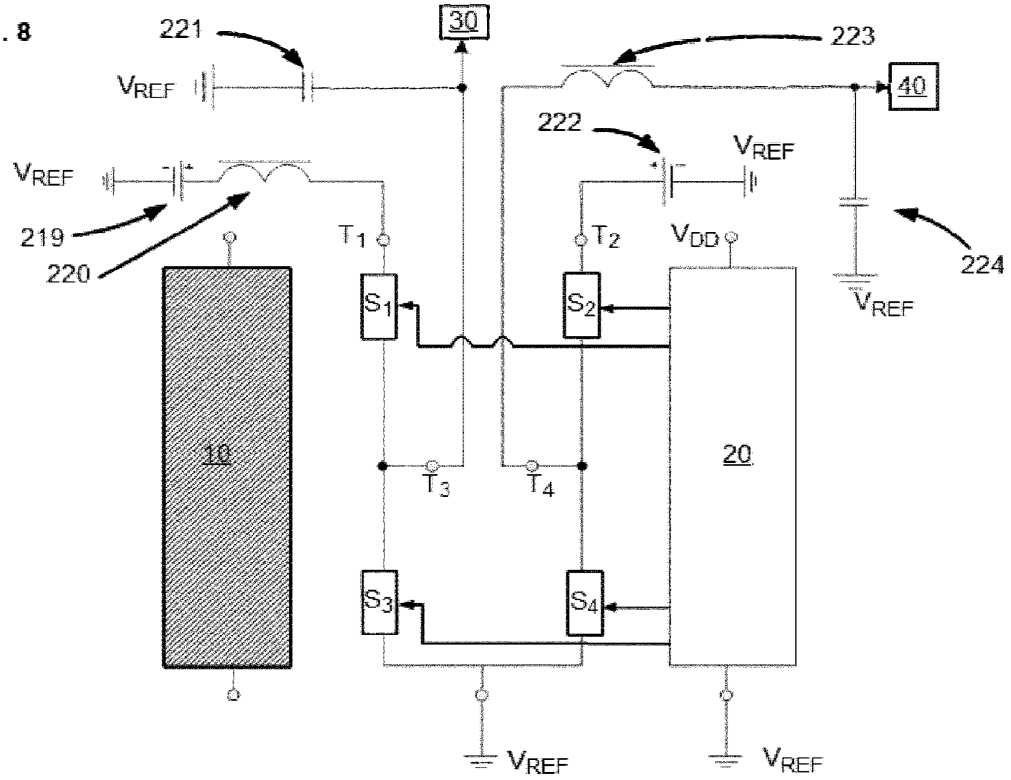
V_{REF}

FIG. 8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T_3
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S_4
V_{REF}
V_{REF}

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First Named Inventor	Philippe SIRITO-OLIVIER
Art Unit	TBD
Examiner Name	TBD
Attorney Docket Number	0112-301/C03308 US1

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	Application Number	
	Filing Date	2015-11-09
	First Named Inventor	Philippe SIRITO-OLIVIER
	Art Unit	TBD
	Examiner Name	TBD
	Attorney Docket Number	0112-301/C03308 US1

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	1	International Search Report issued in corresponding International application no. PCT/EP2014/061350, date of completion of the International search June 30, 2014.	☐
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Signature	/stevenmdubois/	Date (YYYY-MM-DD)	2015-11-09
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(54) Configurable H-bridge circuit

(57) In a configurable H-bridge circuit (100), a high switch (102(1)) is connected to a voltage source (106) and a low switch (102(3)) is connected to ground (110). The configurable H-bridge circuit (100) has a first configuration (Fig. 1B) as a motor drive circuit (104) in which the high switch (102(2)) and the low switch (102(3)) are connected together and coupled to drive a motor (116). The configurable H-bridge circuit (100) also has a second configuration (Fig. 1A) in which the high switch (102(1)) and the low switch (102(3)) are each configured as a discrete switch that can be coupled as a competent switch.

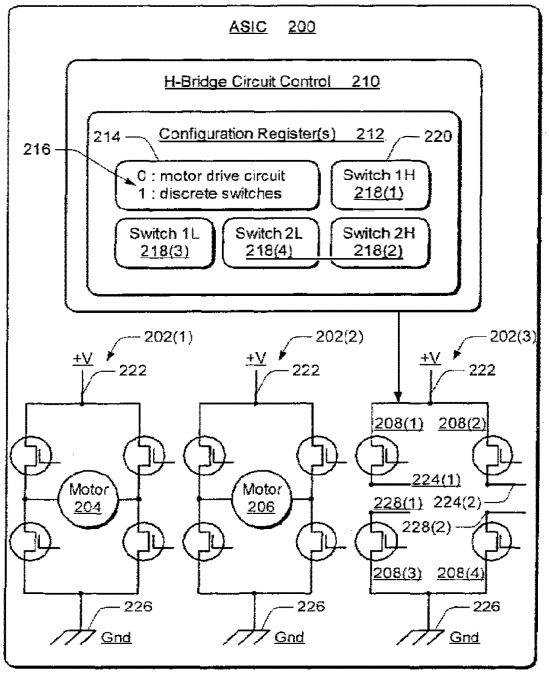

Fig. 2

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Description

[0001] This invention relates to configurable H-bridge circuit(s).

[0002] Imaging devices, such as printing devices and all-in-one devices that scan, print, and copy, utilize motors to drive paper feed mechanisms, move imaging, scanning, and printing units, and/or enable servicing systems such as printhead wipers, printhead capping devices, and printhead cleaning systems. These are only a few examples of how motors may be utilized within an imaging device. Many such devices are designed such that more than one system function is coupled to the same motor so that fewer motors are needed to support the multiple system functions. Typically, imaging devices have been developed with three motors and with a corresponding application specific integrated circuit (ASIC) configured to control the three motors.

[0003] The motor control ASIC is implemented with an H-bridge circuit structure that enables a microprocessor or controller to independently control each motor in an imaging device. The ASIC includes one H-bridge circuit for each motor being controlled, and for a typical three-motor device, the ASIC will include three H-bridge circuits. With the advent of two-motor imaging devices, two H-bridge circuits of the ASIC will be utilized to control the two motors while the third H-bridge circuit goes unutilized.

[0004] The motor control ASIC with the three H-bridge circuit structure continues to be implemented in two-motor imaging devices because it would not be cost effective to design a specialized ASIC with only two H-bridge circuit motor drives, particularly when taking into account the large volume purchase discounts for high volume devices. The small savings in component costs, as well as the savings that would otherwise be incurred for additional engineering and design costs to produce a specialized ASIC, are significant with the high volume sales of such devices. It is cost effective and beneficial to design and utilize an ASIC which can be implemented for similar, yet different devices, such as two-motor and three-motor imaging devices. However, it would also be beneficial if the third H-bridge circuit of an ASIC in a two-motor device could be utilized for component and/or system functionality in the device rather than go unutilized as a motor control.

[0005] The same numbers are used throughout the drawings to reference like features and components:

Figs. 1A and 1B illustrate an exemplary H-bridge circuit that can be configured as discrete switches or as a motor drive circuit.

Fig. 2 illustrates an exemplary application-specific integrated circuit (ASIC) in which configurable H-bridge circuits can each be implemented as discrete switches or as a motor drive circuit.

Fig. 3 is a flow diagram that illustrates a method for a configurable H-bridge circuit.

Fig. 4 is a flow diagram that illustrates a method for a configurable H-bridge circuit.

Fig. 5 illustrates various components of an exemplary printing device in which a configurable H-bridge circuit can be implemented.

[0006] The following describes a configurable H-bridge circuit that can be implemented as independent switches or as a motor drive circuit. In an exemplary implementation, an application-specific integrated circuit (ASIC) includes three H-bridge motor drive circuits. The ASIC can be implemented in an imaging device, such as a printer for example, that utilizes only two motors to drive mechanisms and components of the device.

[0007] The third H-bridge circuit of the ASIC which is not utilized as a motor drive in a two-motor device can be configured as two high side and two low side discrete switches. The two high side switches are connected to an input voltage and can each be utilized to provide switched power to components in the imaging device. The two low side switches are connected to ground and can each be utilized as pull-down devices to provide excess current, such as for LED operation to scan and copy for example.

[0008] It would not be cost effective to design a specialized ASIC with two H-bridge motor drive circuits for newly developed two-motor devices, particularly when large purchase discounts help to keep down manufacturing costs for high volume devices. Utilizing the third H-bridge circuit as discrete switches also provides design flexibility during manufacture of a device and is cost effective in that extra discrete switches do not have to be purchased and added to a device during manufacture.

[0009] Figs. 1A and 1B illustrate an exemplary configurable H-bridge circuit 100 that can be configured as discrete switches 102(1) through 102(4) (Fig. 1A), or can be configured as a motor drive circuit 104 (Fig. 1B). When the configurable H-bridge circuit 100 is implemented as discrete switches (Fig. 1A), a first high switch 102(1) and a second high switch 102(2) are each connected to a voltage source 106. The first and second high switches 102(1) and 102(2) each have an output connection 108(1) and 108(2), respectively. Additionally, a first low switch 102(3) and a second low switch 102(4) are each connected to ground 110 and have an output connection 112(1) and 112(2), respectively. Any of the discrete switches 102 can be independently coupled to a device component to provide switched power and/or a connection to ground. An example of an imaging device is described below with reference to the exemplary printing device 500 shown in Fig. 5. Printing device 500 includes examples of components that may be coupled to a discrete switch 102 of the H-bridge circuit 100.

[0010] The discrete switches 102 can be implemented as any one or more of field effect transistors (FETs), bipolar transistors, relays, and/or any other type of switching device. A gate drive voltage can be applied to

gates 114(1) and 114(2) of the high switches 102(1) and 102(2), respectively. The gate drive voltage enables a particular voltage range on each of the high side switches 102(1) and 102(2) and turns on the high side switches such that they can be implemented as series switches that pass a voltage.

[0011] When the configurable H-bridge circuit is implemented as a motor drive circuit 104 (Fig. 1B), an output of the first high switch 102(1) is connected to an input of the first low switch 102(3) and the two switches are coupled to drive a motor 116 in a first direction. Similarly, an output of the second high switch 102(2) is connected to an input of the second low switch 102(4) and the two switches are coupled to drive the motor 116 in an opposite, second direction. Printing device 500 (Fig. 5) also includes examples of components that may be driven by motor 116 when the configurable H-bridge circuit 100 is implemented as a motor drive circuit 104.

[0012] Fig. 2 illustrates an exemplary application-specific integrated circuit (ASIC) 200 in which configurable H-bridge circuits 202(1), 202(2), and 202(3) can each be configured and implemented as discrete switches or as a motor drive circuit. In this example, configurable H-bridge circuits 202(1) and 202(2) are implemented as motor drive circuits to drive motor 204 and motor 206, respectively. The configurable H-bridge circuit 202(3) is configured as discrete switches 208 each of which can be independently coupled to a device component to provide switched power and/or a connection to ground as described above with reference to Fig. 1A.

[0013] The ASiC 200 also includes an H-bridge circuit control 210 that includes configuration register(s) 212 which include configuration indicators of the configurable H-bridge circuit 202(3) implementation. For example, a configuration register 214 maintains an indicator 216 (e.g., a zero data bit) that indicates configurable H-bridge circuit 202(3) is to be implemented as a motor drive circuit. Alternatively, configuration register 214 maintains indicator 216 (e.g., a one data bit) that indicates configurable H-bridge circuit 202(3) is to be implemented as discrete switches 208. Configuration register(s) 212 also include switch indicators 218(1) through 218(4) that each correspond to a discrete switch 208 of the configurable H-bridge circuit 202(3). The switch indicators 218 indicate a configuration of a discrete switch of the configurable H-bridge circuit 202(3) when the H-bridge circuit is implemented as discrete switches. For example, configuration register 220 includes switch indicator 218(1) that indicates a component switch configuration of the first high switch 208(1) of the configurable H-bridge circuit 202(3).

[0014] The configuration registers 212 are controlled by an integrated circuit serial bus (not shown) which connects the components of ASIC 200. The serial bus is used to communicate data bits (e.g., read and write data) to establish the register indicators, such as indicator 216, to enable and/or disable current limits and to set up gate drive voltages for the switches 208, and the like. The H-bridge circuit control 210 and the configuration registers 212 are programmable at a time of manufacture and can be programmed with firmware, for example, to configure and/or implement the configurable H-bridge circuit 202(3) as a motor drive circuit or as discrete switches.

[0015] When the configurable H-bridge circuit 202(3) is implemented as discrete switches 208 (as shown in this example), the first high switch 208(1) and the second high switch 208(2) are each connected to a voltage source 222 and have an output connection 224(1) and 224(2), respectively. A high side switch 208(1) can be implemented to turn a pen voltage on and off for an ink printhead in a printing device, for example. Further, the two high side switches 208(1) and 208(2) can be coupled in parallel to reduce the effective impedance such that a high side switch can pass a higher current.

[0016] Additionally, the first low switch 208(3) and the second low switch 208(4) are each connected to ground 226 and have an output connection 228(1) and 228(2), respectively. A low side switch 208(3) can be implemented as a general purpose input/output device, a programmable current sink, a fan drive, a solenoid drive, and the like.

[0017] Fig. 3 illustrates a method 300 for a configurable H-bridge circuit that can be implemented as discrete switches or as a motor drive circuit. The order in which the method is described is not intended to be construed as a limitation, and any number of the described method blocks can be combined in any order to implement the method. Furthermore, the method can be implemented in any suitable hardware, software, firmware, or combination thereof. A method for a configurable H-bridge circuit may also be described in the general context of computer executable instructions. Generally, computer executable instructions include routines, programs, objects, components, data structures, and the like that perform particular function(s) or implement data type(s).

[0018] At block 302, an indicator is written to a configuration register to indicate a configuration of a configurable H-bridge circuit. For example, an indicator 216 (Fig. 2) indicates that the configurable H-bridge circuit 202(3) is to be implemented as a motor drive circuit (e. g., a zero data bit) or as discrete switches 208 (e.g., a one data bit). At block 304, the indicator is maintained to indicate the configuration of the configurable H-bridge circuit.

[0019] At block 306, a determination is made as to whether the configurable H-bridge circuit is to be implemented as a motor drive circuit (or as discrete switches). If the configurable H-bridge circuit is to be implemented as a motor drive circuit (i.e., "yes" from block 306), then an H-bridge circuit control is configured at block 308 according to the implementation indicator (as a motor drive). At block 310, the configurable H-bridge circuit is coupled to drive the motor. For example, configurable H-bridge circuit 100 is implemented as a motor drive circuit 104 to drive motor 116 (Fig. 1B).

[0020] If the configurable H-bridge circuit is to be implemented as discrete switches (i.e., "no" from block 306), then a switch indicator is written to a configuration register at block 312 to indicate a configuration of a component switch. For example, switch indicator 218(1) (Fig. 2) is written to configuration register 220 to indicate a configuration of discrete switch 208(1) of the configurable H-bridge circuit 202(3). At block 314, the H-bridge circuit control is configured according to the implementation indicator (as discrete switches). At block 316, a switch of the configurable H-bridge circuit is coupled as a component switch.

[0021] Fig. 4 illustrates a method 400 for a configurable H-bridge circuit that can be implemented as discrete switches or as a motor drive circuit. The order in which the method is described is not intended to be construed as a limitation, and any number of the described method blocks can be combined in any order to implement the method. Furthermore, the method can be implemented in any suitable hardware, software, firmware, or combination thereof. A method for a configurable H-bridge circuit may also be described in the general context of computer executable instructions. Generally, computer executable instructions include routines, programs, objects, components, data structures, and the like that perform particular function(s) or implement data type(s).

[0022] At block 402, a first movable component is controlled with a first motor driven by a first H-bridge circuit of a multiple H-bridge circuit. For example, a first motor 204 (Fig. 2) is driven by a first H-bridge circuit 202(1) of the ASIC 200. At block 404, a second movable component is controlled with a second motor driven by a second H-bridge circuit of the multiple H-bridge circuit. For example, a second motor 206 is driven by a second H-bridge circuit 202(2) of the ASIC 200.

[0023] At block 406, an indicator is written to a configuration register to indicate a configuration of a third H-bridge circuit of the multiple H-bridge circuit. For example, an indicator 216 (Fig. 2) indicates that the configurable H-bridge circuit 202(3) is to be implemented as a motor drive circuit (e.g., a zero data bit) or as discrete switches 208 (e.g., a one data bit).

[0024] At block 408, a determination is made as to whether the third H-bridge circuit is to be implemented as discrete switches (or as a motor drive circuit). If the third H-bridge circuit is not implemented as discrete switches (i.e., "no" from block 408), then the third H-bridge circuit is configured as a motor drive circuit at block 410 according to the indicator maintained in the configuration register. At block 412, the third H-bridge circuit of the multiple H-bridge circuit is coupled to drive a third motor.

[0025] If the third H-bridge circuit is to be implemented as discrete switches (i.e., "yes" from block 408), then the third H-bridge circuit is configured as discrete switches at block 414 according to the indicator maintained in the configuration register. At block 416, a switch of the third H-bridge circuit is coupled as a component switch.

[0026] Fig. 5 illustrates various components of an exemplary printing device 500 in which a configurable H-bridge circuit can be implemented as a motor drive circuit or as discrete switches. General reference is made herein to one or more printing devices, such as printing device 500. As used herein, "printing device" means any electronic device having data communications, data storage capabilities, and/or functions to render printed characters, text, graphics, and/or images on a print media. A printing device may be a printer, fax machine, copier, plotter, and the like. The term "printer" includes any type of printing device using a transferred imaging medium, such as ejected ink, to create an image on a print media. Examples of such a printer can include, but are not limited to, inkjet printers, electrophotographic printers, plotters, portable printing devices, as well as all-in-one, multi-function combination devices.

[0027] Printing device 500 includes one or more processors 502 (e.g., any of microprocessors, controllers, and the like) which process various instructions to control the operation of printing device 500 and to communicate with other electronic and computing devices.

[0028] Printing device 500 can be implemented with one or more memory components, examples of which include random access memory (RAM) 504, a disk drive 506, and non-volatile memory 508 (e.g., any one or more of a ROM 510, flash memory, EPROM, EEPROM, etc.). The one or more memory components store various information and/or data such as configuration information, print job information and data, graphical user interface information, fonts, templates, menu structure information, and any other types of information and data related to operational aspects of printing device 500.

[0029] Printing device 500 includes a firmware component 512 that is implemented as a permanent memory module stored on ROM 510, or with other components in printing device 500, such as a component of a processor 502. Firmware 512 is programmed and distributed with printing device 500 to coordinate operations of the hardware within printing device 500 and contains programming constructs used to perform such operations.

[0030] An operating system 514 and one or more application programs 516 can be stored in non-volatile memory 508 and executed on processor(s) 502 to provide a runtime environment. A runtime environment facilitates extensibility of printing device 500 by allowing various interfaces to be defined that, in turn, allow application programs 516 to interact with printing device 500.

[0031] Printing device 500 further includes one or more communication interfaces 518 which can be implemented as any one or more of a serial and/or parallel interface, a wireless interface, any type of network interface, and as any other type of communication interface. A wireless interface enables printing device 500 to receive control input commands and other information

from an input device, such as from an infrared (IR), 802.11, Bluetooth, or similar RF input device. A network interface provides a connection between printing device 500 and a data communication network which allows other electronic and computing devices coupled to a common data communication network to send print jobs, menu data, and other information to printing device 500 via the network. Similarly, a serial and/or parallel interface provides a data communication path directly between printing device 500 and another electronic or computing device.

[0032] Printing device 500 also includes a print unit 520 that includes mechanisms arranged to selectively apply an imaging medium such as liquid ink, toner, and the like to a print media in accordance with print data corresponding to a print job. The print media can include any form of media used for printing such as paper, plastic, fabric, Mylar, transparencies, and the like, and different sizes and types such as 8½ x 11, A4, roll feed media, etc.

[0033] Printing device 500, when implemented as an all-in-one device for example, can also include a scan unit 522 that can be implemented as an optical scanner to produce machine-readable image data signals that are representative of a scanned image, such as a photograph or a page of printed text. The image data signals produced by scan unit 522 can be used to reproduce the scanned image on a display device or with a printing device.

[0034] Printing device 500 also includes a user interface and menu browser 524 and a display panel 526. The user interface and menu browser 524 allows a user of printing device 500 to navigate the device's menu structure. User interface 524 can be indicators or a series of buttons, switches, or other selectable controls that are manipulated by a user of the printing device. Display panel 526 is a graphical display that provides information regarding the status of printing device 500 and the current options available to a user through the menu structure.

[0035] Although shown separately, some of the components of printing device 500 can be implemented in an application specific integrated circuit (ASIC). Additionally, a system bus (not shown) typically connects the various components within printing device 500. A system bus can be implemented as one or more of any of several types of bus structures, including a memory bus or memory controller, a peripheral bus, an accelerated graphics port, or a local bus using any of a variety of bus architectures.

[0036] Although configurable H-bridge circuit(s) have been described in language specific to structural features and/or methods, it is to be understood that the subject of the appended claims is not necessarily limited to the specific features or methods described. Rather, the specific features and methods are disclosed as exemplary implementations of configurable H-bridge circuit (s).

Claims

1. A configurable H-bridge circuit (100), comprising:

   a high switch (102(1)) connected to a voltage source (106);
   a low switch (102(3)) connected to ground (110);
   a first configuration (Fig. 1B) of the high switch (102(1)) and the low switch (102(3)); and
   a second configuration (Fig. 1A) in which the high switch (102(1)) and the low switch (102(3)) are each configured as a discrete switch that can be coupled as a component switch, the second configuration (Fig. 1A) being different than the first configuration (Fig. 1B).

2. A configurable H-bridge circuit (100) as recited in claim 1, wherein the first configuration (Fig. 1B) includes the high switch (102(1)) and the low switch (102(3)) connected together and coupled to drive a motor (116).

3. A printing device (500), comprising:

   a first motor (204) configured for movable control of at least a first component (520) in the printing device (500);
   a second motor (206) configured for movable control of at least a second component (522) in the printing device (500);
   a multiple H-bridge circuit (202) including:

      a first H-bridge circuit (202(1)) configured to drive the first motor (204);
      a second H-bridge circuit (202(2)) configured to drive the second motor (206); and
      a third H-bridge circuit (202(3)) that includes a first configuration (Fig. 1B) as a motor drive circuit (104) to drive a third motor (116), and includes a second configuration (Fig. 1A) as discrete switches (208) that can each be coupled as a component switch.

4. A printing device (500) as recited in claim 3, further comprising a configuration register (214) configured to maintain an indicator (216) of the third H-bridge circuit (202(3)) configuration.

5. A printing device (500) as recited in claim 3, wherein the third H-bridge circuit (202(3)) includes a high switch (208(1)) connected to a voltage source (222) and includes a low switch (208(3)) connected to ground (226), and wherein the first configuration (Fig. 1 B) includes the high switch (208(1)) and the low switch (208(3)) connected together and coupled to drive the third motor (116).

6. A printing device (500) as recited in claim 3, wherein the third H-bridge circuit (202(3)) includes a high switch (208(1)) connected to a voltage source (222) and includes a low switch (208(3)) connected to ground, and wherein the second configuration (Fig. 1A) includes at least one of the high switch (208(1)) and the low switch (208(3)) coupled as the component switch.

7. A method (300), comprising:

writing (302) an indicator (216) to a configuration register (214) to indicate an implementation of a configurable H-bridge circuit (202(3));
coupling (310) the configurable H-bridge circuit (202(3)) to drive a motor (116) in an event that the configurable H-bridge circuit (202(3)) is implemented as a motor drive circuit (Fig. 1B); and
coupling (316) a switch (208(1)) of the configurable H-bridge circuit (202(3)) as a component switch in an event that the configurable H-bridge circuit (202(3)) is implemented as discrete switches (208(1-4)).

8. A method (300) as recited in claim 7, further comprising maintaining (304) the indicator (216) of the implementation of the configurable H-bridge circuit (202(3)), wherein the indicator (216) indicates at least one of a first configuration (Fig. 1B) of the configurable H-bridge circuit (202(3)) as the motor drive circuit (104) and a second configuration (Fig. 1A) of the configurable H-bridge circuit (202(3)) as the discrete switches (208(1-4).

9. A method (300) as recited in claim 7, further comprising writing (312) a switch indicator (218(1) to the configuration register (220) to indicate a configuration of the component switch (208(1).

10. A method (300) as recited in claim 7, wherein coupling (310) the configurable H-bridge circuit (202 (3)) to drive the motor (116) includes:

connecting an output (224(1)) of a high switch (208(1)) of the configurable H-bridge circuit (202(3)) to an input (228(1)) of a low switch (208(3)) of the configurable H-bridge circuit (202(3)), the high switch (208(1)) connected to a voltage source (222) and the low switch (208 (3)) connected to ground (226); and
coupling the high switch (208(1)) and the low switch (208(3)) to the motor (116).

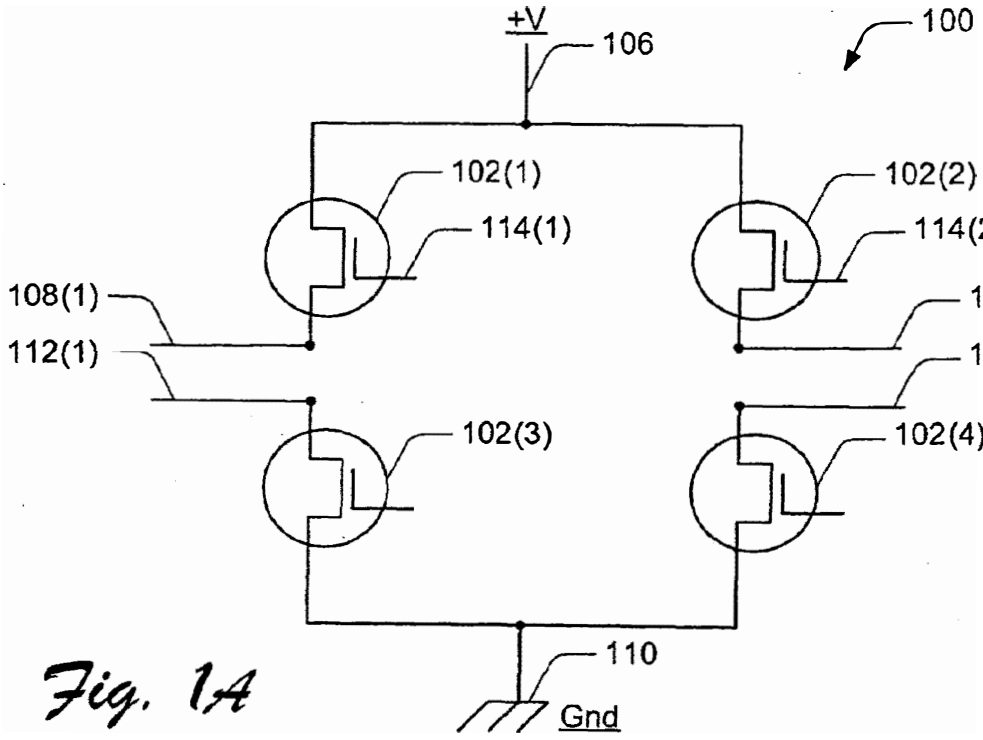

Fig. 1A

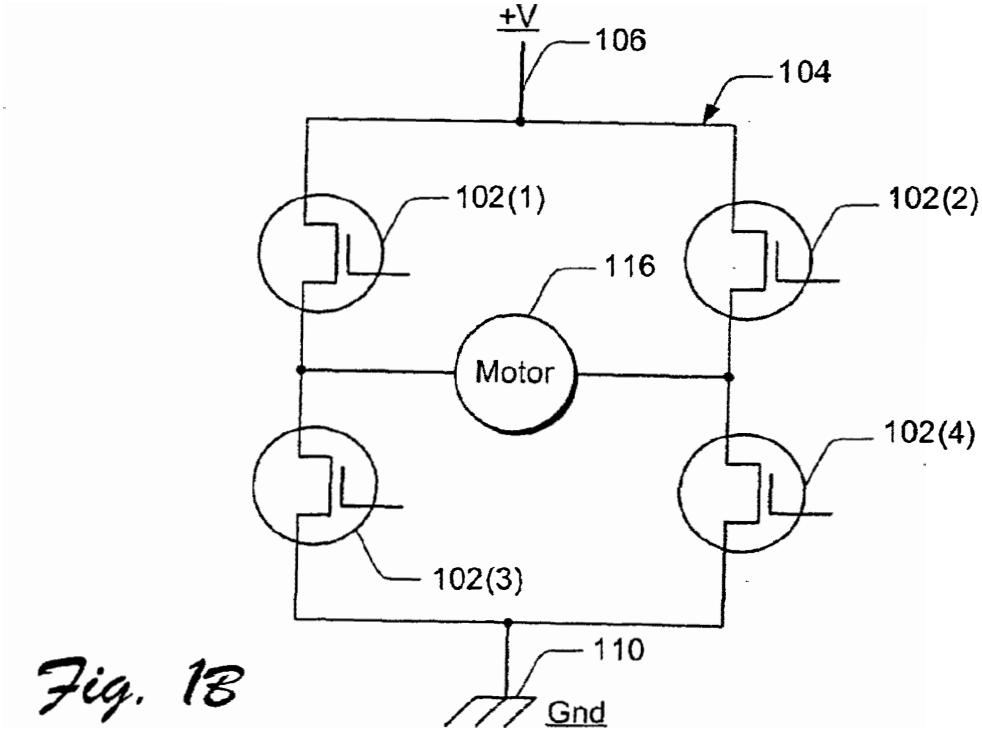

Fig. 1B

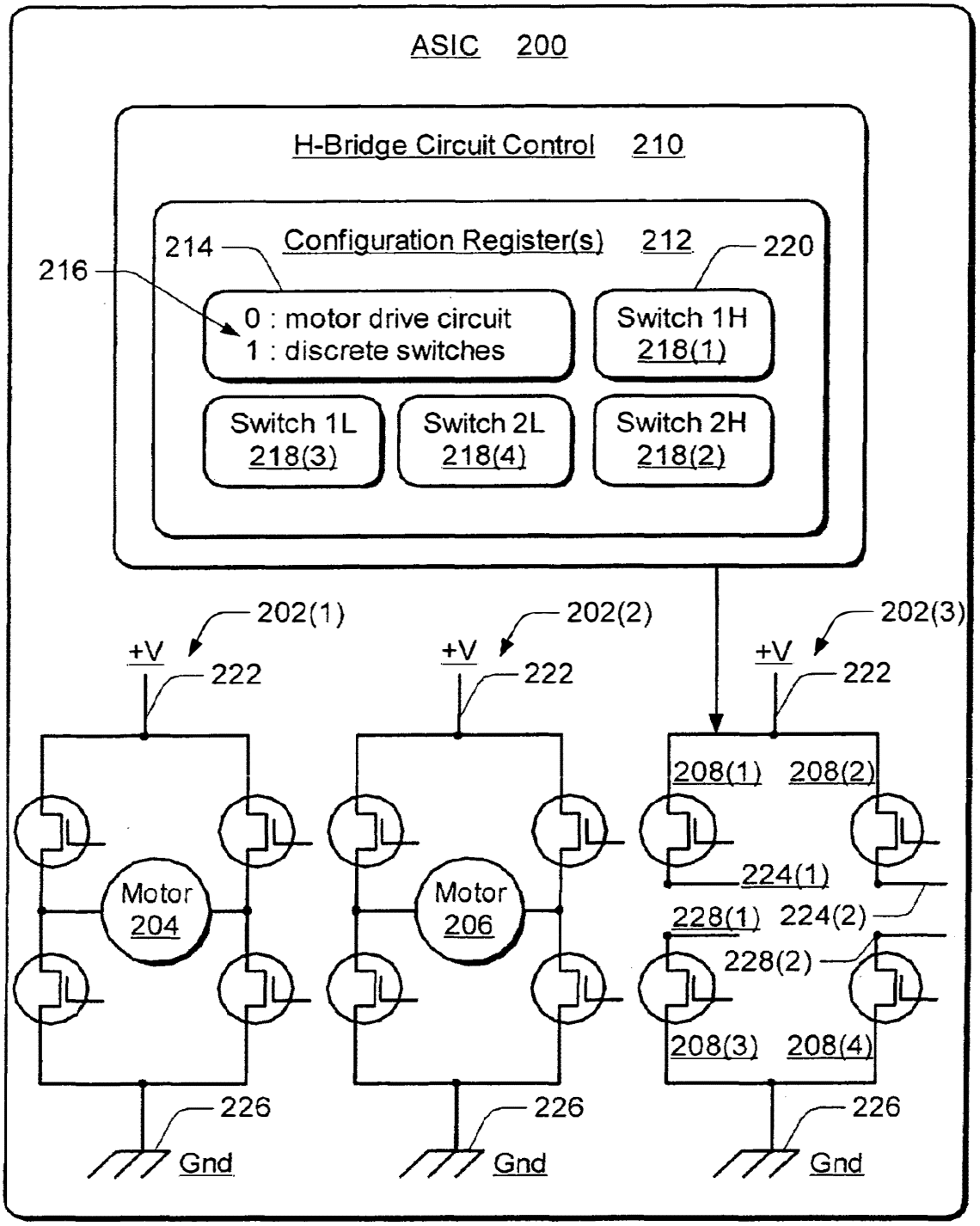

Fig. 2

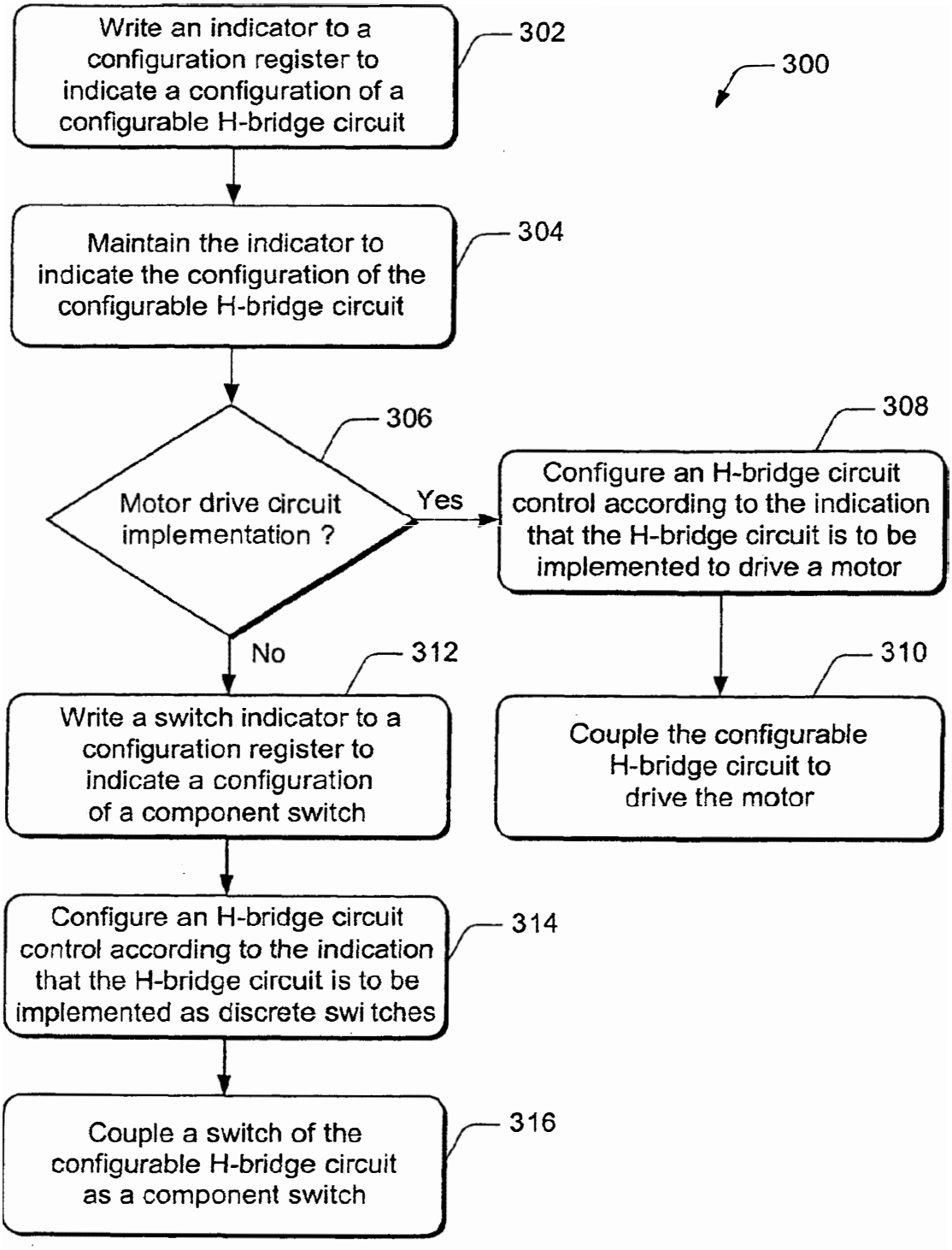

Fig. 3

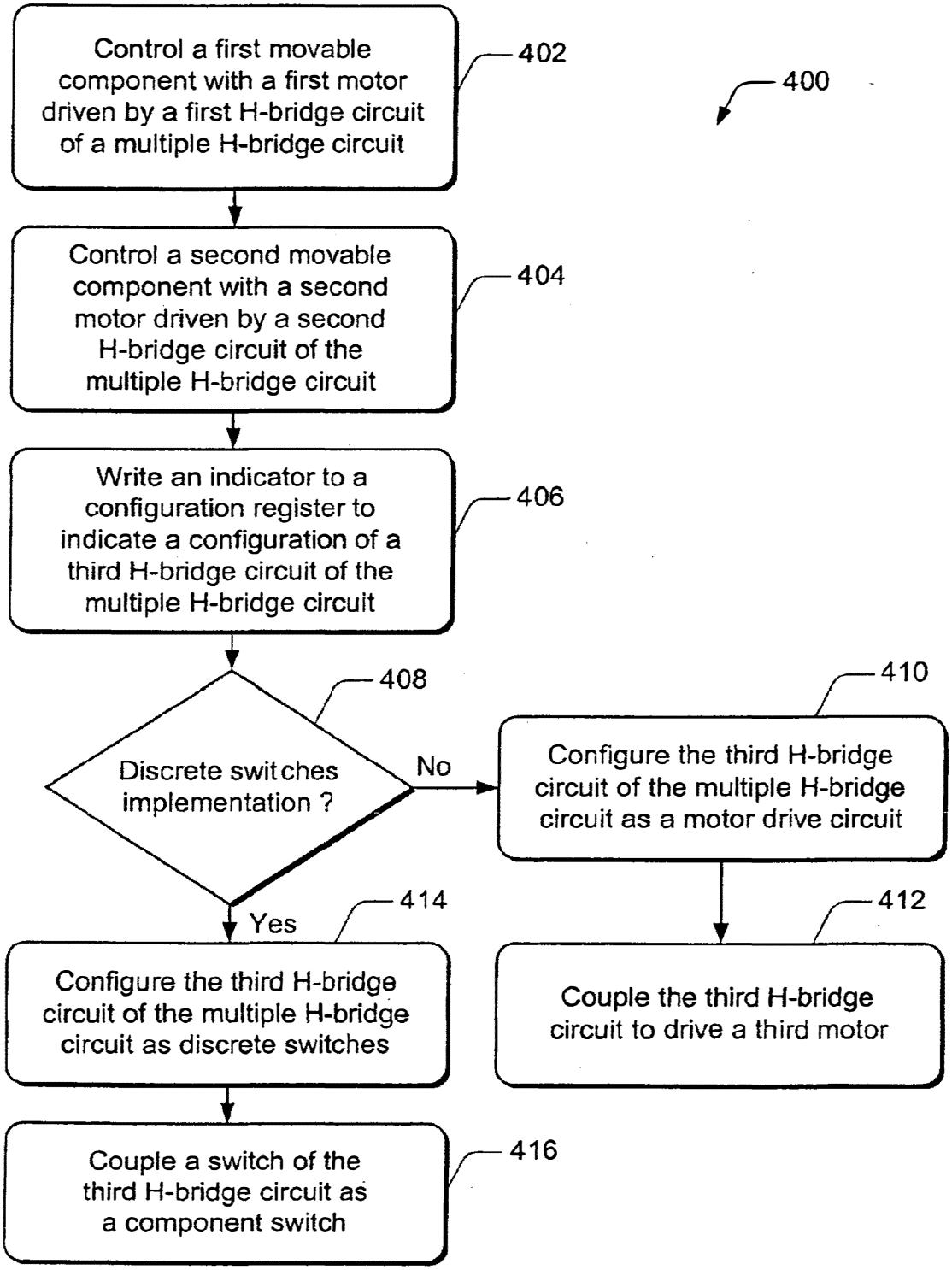

Fig. 4

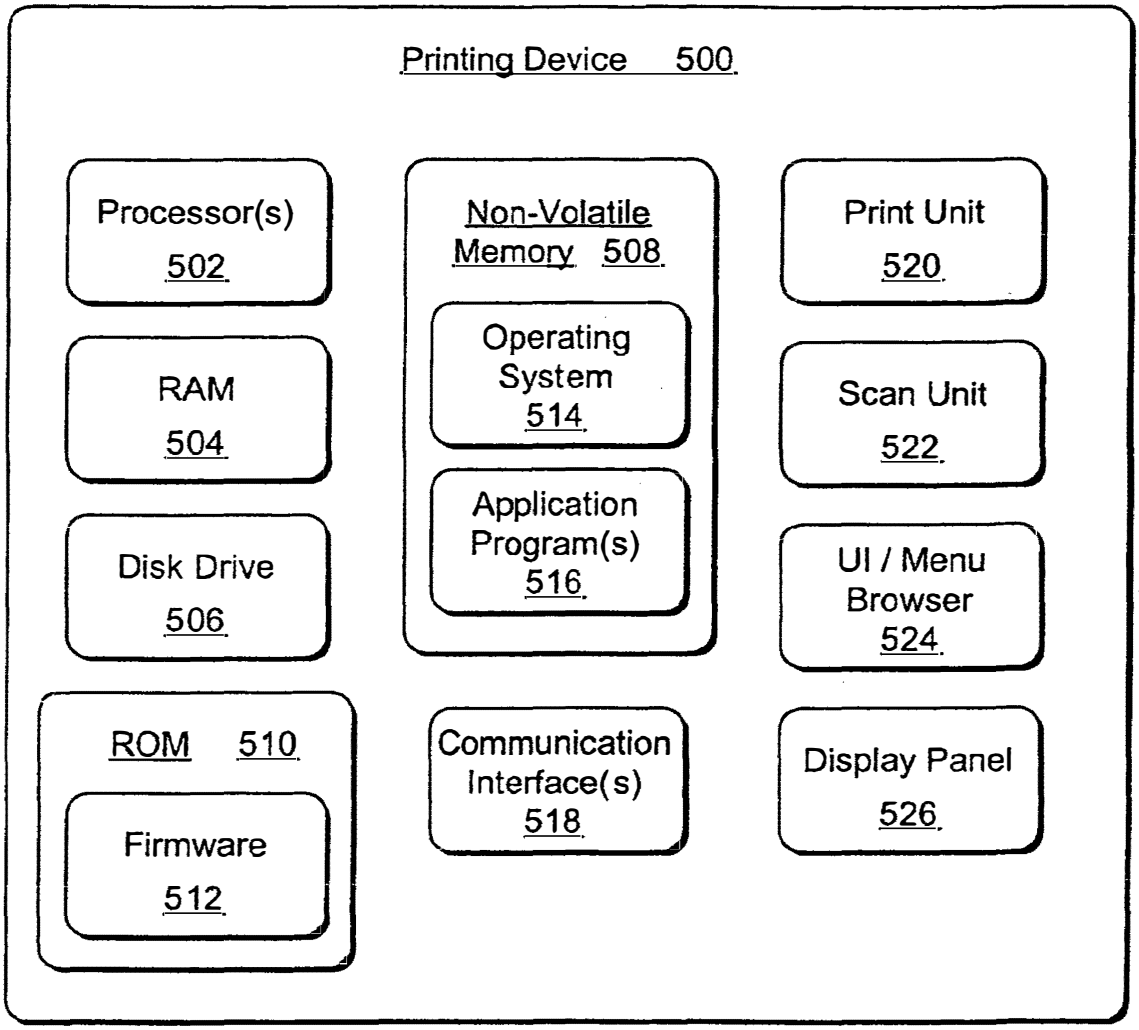

Fig. 5

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 04 25 6356

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	EP 0 833 437 A (HELLA KG HUECK & CO) 1 April 1998 (1998-04-01) * column 2, line 54 - column 6, line 2 *	1-10	H03K17/687 H02P7/00
X	DE 44 40 064 A1 (HELLA KG HUECK & CO, 59557 LIPPSTADT, DE; HELLA KG HUECK & CO) 15 May 1996 (1996-05-15) * column 3, line 45 - column 6, line 65; figures 1-3 *	1-10	
X	EP 0 369 954 A (SGS-THOMSON MICROELECTRONICS S.R.L) 23 May 1990 (1990-05-23) * column 3, line 58 - column 7, line 51; figures 1-5 *	1-10	

TECHNICAL FIELDS SEARCHED (Int.Cl.7)

H03K
H02P

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
The Hague	7 February 2005	Segaert, P

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
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T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
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EPO FORM 1503 03.82 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 04 25 6356

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
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07-02-2005

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EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

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A1

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(54) Multipurpose, internally configurable integrated circuit for driving in a switching mode external inductive loads according to a selectable connection scheme.

(57) A "multipurpose" integrated circuit for driving in a switching mode an externally connected load or loads permits to implement any appropriate supply scheme of the external load or loads through six output terminals thereof and is therefore useful in a large number of applications. The integrated circuit uses six integrated power switching devices provided with respective recirculation diodes and may conveniently use a single externally connected sensing resistor for generating, by means of a customary PWM control loop, a control signal which by means of a logic circuit configurable by programming permits the generation of driving signals function of said control signal for all six integrated power switches in accordance with a configuration of said driving signals which is functionally in conformity with the particular scheme of connection of the load or loads selected among the different bridge type and unipolar-motor type schemes which may be selected by programming. A preferred embodiment contemplates the use of a multiplexer for selecting among bridge type driving signals and unipolar-motor type driving modes and a ROM provided with two input registers for selecting the specific driving scheme and for regulation, respectively.

EP 0 369 954 A1

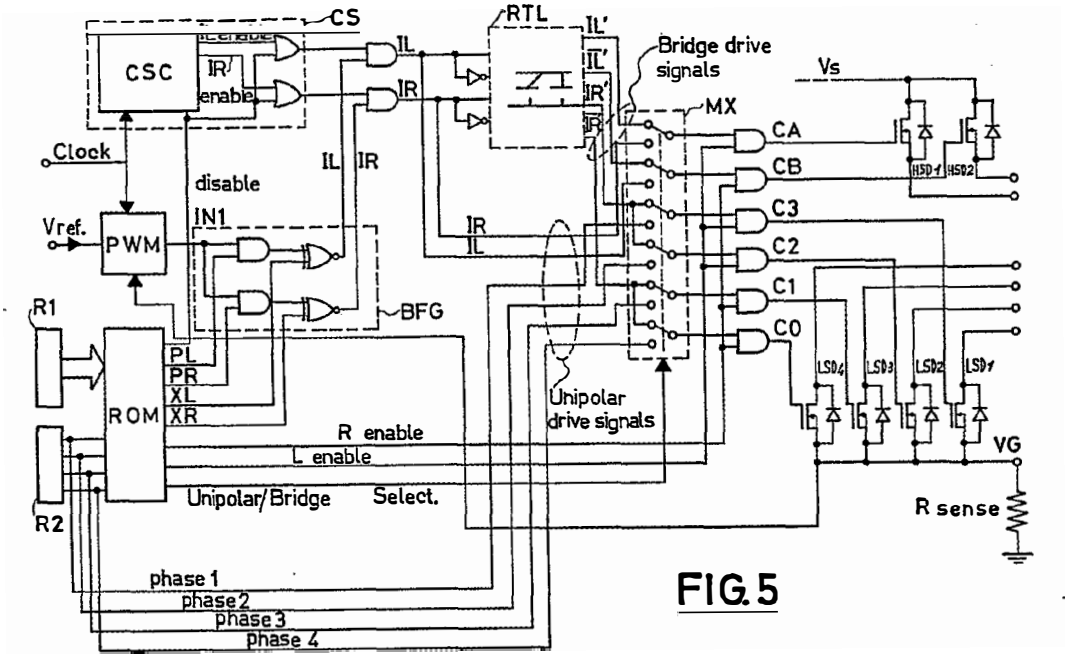


FIG.5

MULTIPURPOSE, INTERNALLY CONFIGURABLE INTEGRATED CIRCUIT FOR DRIVING IN A SWITCHING MODE EXTERNAL INDUCTIVE LOADS ACCORDING TO A SELECTABLE CONNECTION SCHEME

BACKGROUND OF THE INVENTION

1. Field of the invention

The present invention relates to an integrated circuit which may be internally configured by programming, for controlling the switching of a driving current through a single or multiple inductive loads connected across output terminals of the integrated device in accordance with one of several different connection schemes which may be selected for a particular application.

2. Description of the prior art

The controlled driving of stepping motors, transformers, electromagnets and similar actuating means, typically representing inductive loads, is commonly implemented by employing an integrated device combining the output power transistors (typically four power switching transistors connected to a virtual ground node which are referred to as "low-side drivers" and one or more often two power switching transistors connected to the supply rail, known as "high-side driver(s)") and a driving circuit. The latter typically includes a pulse-width-modulation (PWM) control loop, driven by a clock signal, which controls the "duty-cycle" of driving signals fed to the output power switching transistors in function of the detected value of the current flowing through the external load and of a control reference voltage.

Integrated circuits of this kind are well known to a skilled technician and may take different forms, more or less advantageous under certain aspects, but which essentially remain based upon PWM control loops. Among these types of circuits, particularly advantageous is a control circuit based upon a current sharing principle described in the pending European Patent Application Number 88115444.7, filed on September 21, 1988 and claiming a Convention priority date of October 5, 1987, wherein by employing a single current sensing resistor for the current flowing through the external loads, it is possible to adjust independently the current flowing through two external loads connected according to a "dual-half-bridge" scheme or according to a "unipolar motor" connection scheme. The description of such a switching control circuit is here incorporated. On the other hand, the kind of the external inductive load or loads to be driven by the integrated circuit, whether represented by an unipolar motor or by one or more unidirectional motors, solenoids, etc., normally requires a specific design of the integrated switching control circuit compatible with the particular drive configuration or connection scheme of the external load or loads to be driven. In the accompanying Figures 1a, 1b, 1c and 1d, several well known driving schemes for inductive loads (L), according to a bridge, dual-half-bridge, electromagnet, and unipolar motor drive configuration are respectively depicted. In these illustrations six power switching transistors indicated with HSD1, HSD2 (i.e. the two High-Side Drivers), LSD1, LSD2, LSD3 and LSD4 (i.e. the four Low-Side Drivers), respectively, are shown, each being provided with a power diode for the recirculation of the discharge current of the relative external inductive load L. In case of driving an electromagnet, as depicted in Fig. 1c, the integrated circuit may contain also two additional recirculation diodes D1 and D2 as it is well known to a skilled technician. In all the examples shown, a single sensing resistor (Rsense), connected between a virtual ground node and the real ground of the supply circuit, is shown. Obviously the use of a single sensing resistor in the case of the circuit of Fig. 1b, i.e. a dual-half-bridge drive configuration for two external loads L and L', necessarily requires a current sharing kind of switching control circuit when an individual control of the two loads is desired, as described in the above cited application.

According to the prior art, the integrated circuit for controlling the switching must essentially be designed specifically for the contemplated application, e.g. a bridge type application (Fig. 1a), a unipolar motor application (Fig. 1d), and so forth.

Therefore it would be of great utility the availability of an integrated device for controlling the switching of a drive current across external inductive loads (single or multiple loads), which could be internally configured so as to be usable for a driving scheme selectable among a number of possible driving schemes of the externally connected load or loads.

OBJECTIVE AND SUMMARY OF THE INVENTION

The main objective of the present invention is that of providing an integrated circuit for controlling the switching which may be internally configured by means of selection logic means which may be

controlled by the user for making the control circuit functionally suited for a certain driving scheme of an external load or loads which may be implemented by suitably bridging output terminals of the integrated circuit and connecting the external load or loads thereto.

This and other objectives and advantages which will emerge during the following description, are achieved by the switching mode, driving circuit of the invention, which may also conveniently use a single PWM control loop utilizing a single sensing resistor connected between a virtual ground node to which four "low-side drivers" are connected and the real ground of the supply circuit and which is capable of generating at least a control signal, the "duty-cycle" of which is determined by means of a clock signal and a reference voltage. This control signal generated by the PWM control loop is substantially fed to the input of a configurable logic circuit, which may comprise a read-only memory (ROM) and/or a similarly programmable logic array (PLA) and suitable selection registers (programming registers). The configurable logic circuit produces as many drive signals for as many output power switching transistors are used (i.e. for the four "low-side drivers" and for the unique or for the two "high-side drivers") in conformity with a selected driving scheme to be implemented.

According to a preferred embodiment of the invention, the use of relatively slow ROM or PLA, i.e. with a relatively long access time, is made possible without such a speed limit of the programmable logic circuit having a negative effect upon the correct driving in a switching mode of the external load or loads.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1a, 1b, 1c and 1d depict as many driving schemes of one or more external loads which are commonly adopted in the art, as described above;

Figure 2 is a basic block diagram of the integrated driving circuit of the present invention;

Figure 3 is a block diagram of an embodiment of the circuit of the invention suitable to utilize programmable devices having a relatively long access time;

Figure 4 is a circuit diagram of one of the block of the diagram of Fig. 3;

Figure 5 is a more detailed functional block diagram of a circuit of the invention.

DESCRIPTION OF PREFERRED EMBODIMENTS

A basic block diagram of the integrated driving circuit of the invention is depicted in Fig. 2. The two power devices connected to the supply rail Vs, i.e. the two "high-side drivers" HSD1 and HSd2, and the four power devices which are connected to the virtual ground node VG of the output supply circuit, i.e. the four "low-side drivers" LSD1, LSD2, LSD3 and LSD4, are represented as a whole by the block labelled "power drivers", which has six respective output terminals HSD1, HSD2, LSD1 ... LSD4, whereby any one of the supply schemes for single or multiple loads depicted in Figures 1a, ... 1d, may be implemented. In the particular example shown in Fig. 2, it is easily recognized that the implemented supply scheme is the one used for controlling an electromagnet. The load L is connected between the two "high-side drivers" and the four "lowside drivers", which are respectively connected in parallel by means of the indicated external connections.

The integrated device has preferably an external terminal VG for allowing the connection of an external sensing resistance Rsense between such a virtual ground terminal VG and the real ground of the circuit powering the external load L.

Naturally the six power switching devices will have customarily a respective integrated diode for recirculation, as shown in Figures 1a, 1b, ... 1d.

The voltage signal across the sensing resistor Rsense is fed to a PWM block wherein such a signal is detected and compared with a control reference voltage Vref and a pulse-width-modulation control circuit generates at least a control signal IN1, the frequency and "duty-cycle" of which may be adjusted by means of said control reference voltage Vref and the Clock signal. The signal (or the two nonsuperimposing driving signals which are needed in case a dual-half-bridge supply scheme for two distinct loads or a supply scheme for a unipolar motor utilizing a single sensing resistor and a single PWM control loop as described in the above cited pending application are implemented) is not fed directly or through inverters to the respective driving terminals of the six output power switching devices but such a driving signal (or two nonsuperimposing driving signals) is fed to an input of a logic circuit labelled ROM - PLA which may be configured by programming and which generates on at least six output terminals thereof, signals which are replica and inverse signals of such a single signal IN1 (or of two nonsuperimposing signals) which is generated by the PWM control loop. The output signals (CA, CB, C0, C1, C2 and C3) of the configurable logic circuit (ROM - PLA) are respectively fed to the six driving terminals of the output power drivers. The configurable logic circuit (ROM -PLA) is provided with at least a first register R1 for the selection of the driving configuration of the external load, which is connected (obviously in

conformity with such a selected configuration) to the relative output terminals of the integrated circuit, a second register R2 for controlling the driving conditions of the load thus connected and preferably a read-only memory (ROM) capable of storing the data of the two registers and/or a logic circuit array whose configuration may be programmed (PLA) and/or equivalent combinatory logic circuitry and determines a configuration of said six output signals in conformity with the data stored in said two registers R1 and R2.

In view of the fact that especially when using ROM and/or PLA having a relatively long access time, the delays imputable to the access time of the programmable circuits may interfere with a correct driving in a switching mode of the external load or loads, an embodiment as the one depicted in Figures 3 and 4 which is particularly suited when the fabrication technology is such as to determine relatively long access times for ROM and for PLA, may be preferred.

As schematically shown in Fig. 3, the function of selecting the configuration of the six output terminals CA, CB, C0, C1, C2 and C3 of the configurable logic circuit is performed by utilizing six "speed-up" circuits, identified by H1, H2, L1, ... L4, respectively. Each block is formed by an AND gate followed by an EX-OR gate as depicted in Fig. 4. A first signal of a pair of signals coming from the ROM is fed to an input terminal of the AND gate of the speed-up circuits as a "forcing" signal of a respective logic state and the second is fed to an input terminal of the EX-OR gate of the speed-up circuits as a "selection of inversion" signal. According to this preferred embodiment the use of relatively slow programmable arrays for implementing the read-only-memory function of the integrated circuit of the invention is made possible.

A more detailed diagram of the circuit of the invention according to such a particularly preferred embodiment, is depicted in Fig. 5.

In the example shown in Fig. 5, the six integrated power switching devices: HSD1, HSD2, LSD1, LSD2, LSD3 and LSD4, provided with their respective recirculation diodes, are clearly shown. Each power switching device commutes a respective output terminal either to the supply rail Vs or to the virtual ground node VG. In the example shown a single external sensing resistor Rsense is connected between the virtual ground node VG and the ground of the supply circuit of one or more external loads (not shown in this figure) which will be connected to the appropriate output terminals, in accordance with a selected supply scheme. Each power switching device is driven by a signal coming respectively from the outputs terminals CA, CB, C0, C1, C2 and C3 of the programmable logic circuit, as clearly shown.

The voltage signal present across the sensing resistor Rsense, by means of the shown connection, and the control signals Vref and Clock are fed to a PWM control circuit of a substantially customary type. The control signal IN1 produced by the PWM control circuit is fed to the input of a speed-up, "flexibility bridge" circuit BFG, one function of which is that of allowing to control a number of half-bridge circuits, eventually coupled among them in a bridge configuration, thus permitting to control the driving by means of a single control signal IL or IR (assuming that a "low-side driver" is always inverting in respect to the respective "high-side driver" as it is easily understood by a skilled technician), because by considering for example a single left-hand half-bridge (formed by HSD1, LSD1 and LSD2 of the scheme depicted in Fig. 1b) the control signal IL will always be a function of the signal IN1 or of the inverse of the latter; i.e. always "high" or always "low", and therefore the AND gate followed by and EX-OR gate of the BFG circuit will control the function: IL = S (IN1) through the respective left-phase (PL) and left-inversion (XL) signals coming from the ROM. Obviously the same type of control is duplicated by the BFG circuit through the respective PR and XR signals coming from the ROM for generating an IR driving signal for an eventual right-hand half-bridge (formed by HSD2, LSD3 and LSD4 in Fig. 1b). An advantage of such a solution is represented by the small number of components which are necessary for implementing the double half-bridge control as well as by the possibility offered of employing a very slow ROM, because the delay between the signal IN1 generated by the PWM control circuit and the control signals IL and/or IR remains always extremely small, as already observed in relation to the more general schemes of Figures 3 and 4.

As it will be evident to the skilled technician, in case a "full-bridge" supply scheme is utilized, the functions of the "current sharing" CS block are no longer required and the signal "CS disable" coming from the ROM will assume a logic value equivalent to "1" such as to disable the two OR output gates of the CS block. In case a "dual-half-bridge" or a "unipolar motor" supply scheme is selected, the "CS disable" signal will assume a "ø" logic value and the two output signals of the current sharing control circuit "CSC", "IL enable" and "IR enable", are fed to the respective inputs of the two AND gates. The output signals of the two AND gates: IL and IR, essentially correspond to the signals PA and PB of the circuit depicted in Fig. 4 of the cited prior application Serial Number 245,657 of September 16, 1988, so as the "IL enable" and "IR enable" signals correspond sustantially to the two signals Qz and $\overline{Qz}$ of that circuit.

In case a bridge scheme is selected, the two output signals IL and IR of the two AND gates are fed in a replica and in an inverse form, through the shown inverters, to a lag time generating circuit "RTL", i.e. to a circuit capable of determining a certain delay in the transfer of a positive ramp, which circuit has the function of positively excluding simultaneous conduction of a "high-side driver" and of a respective "low-side driver", according to a common technique.

The pair or the pairs of signals, IL' and $\overline{IL'}$ and IR' and $\overline{IR'}$, respectively, are fed through a multiplexer "MX" to the respective driving terminals of the power switching devices, as it will be described further on.

In case a unipolar-motor mode of operation is selected by means of the register R1 (Fig. 1d scheme), the four control phases (phase 1, 2, 3 and 4) are set by means of the register R2 and through the shown connections these signals are fed to the respective inputs of the multiplexer MX to which also the two control signals IR and IL generated as described before by means of the PWM control circuit, the CS current sharing circuit and the BFG circuit are fed. By means of the "unipolar/bridge select" signal coming from the ROM, the multiplexer MX is preset and the six driving signals CA, CB, C3, C2, C1 and C0 for the respective six power switching devices are enabled by means of two enable/disable signals, respectively "R enable" and "L enable" also coming from ROM and which, by means of the six AND gates connected on the six outputs of the multiplexer MX permit to force to an OFF state (disable) the driving signals.

The use of the multiplexer MX is particularly effective for performing a selection among bridge type and unipolar-motor type supply schemes which are radically different from each other and this allows to reduce the number of components which are required for implementing the programmable logic circuitry which is employed in the integrated device of the present invention.

The driving signals relating to the implementation of a bridge type supply scheme or of a solenoid control, are grouped in Fig. 5 by the label "bridge drive signals", while the ensemble of driving signals relating to the implementation of a unipolar-motor supply scheme are labelled "unipolar drive signals" in the diagram of the same Fig. 5.

Notwithstanding the fact that only few preferred embodiments of the invention have been illustrated wherein a ROM is employed, it will be evident to the skilled technician that the ROM may also be substituted by an equivalent logic circuit such as for example a programmable logic array (PLA, PAL, etc.) or by equivalent combinatory logic circuitry. Moreover the invention may be practiced in different embodiments, modified in respect to the embodiments which have been described herein for purely illustrative purposes.

Claims

1. An integrated circuit for driving in a switching mode one or more external loads connected, in accordance with a certain supply scheme, to output terminals of the integrated circuit which essentially comprise at least one or optionally two high-side driver, power switching integrated devices having a common pole connected to a supply rail of the integrated circuit, four low-side driver, power switching integrated devices having a common pole connected to a virtual ground node of the integrated circuit, a second pole of each of said integrated power switching devices being connected respectively to one of an equal number of output terminals of the integrated circuit, an external sensing resistor being connected between said virtual ground node and a real ground node of the supply circuit, each of said integrated power switching devices having a driving terminal to which a driving signal is fed, means for detecting and comparing a signal present across said sensing resistor with a control reference voltage, at least a pulse-with-modulation (PWM) control circuit capable of generating at least a substantially square-wave control signal having a frequency and a duty-cycle respectively controlled by means of a clock signal and said control reference voltage, wherein the integrated circuit includes
at least a logic circuit configurable by programming capable of receiving through at least an input terminal thereof said control signal generated by said PWM control circuit and addressing, through output terminals thereof, toward said driving terminals of said integrated power switching devices, driving signals function of said control signal, according to a configuration of said outputs in conformity with a supply scheme of connection of the external load or loads to said output terminals of the integrated circuit selected among different bridge and unipolar-motor type schemes of connection.

2. The integrated circuit according to claim 1, wherein said PWM control circuit generates two nonsuperimposing, square-wave control signals and said configurable logic circuit receives both said two nonsuperimposing control signals through two input terminals thereof.

3. The integrated circuit according to claim 1, wherein said configurable logic circuit comprises:
a first register for selecting the connection scheme of an external load which is connected, in conformity with said selected scheme, across said output

terminals of the integrated circuit;
a second register for controlling the driving conditions of said externally conneted load;
a read-only memory (ROM) or equivalent logic circuit apt to produce a configuration of output signals for conditioning a combinatory logic circuit in conformity with data stored in said first and in said second registers;
a combinatory logic circuit apt to receive said control signal generated by said PWM control circuit and said conditioning signals produced by said ROM and to produce driving signals, function of said control signal generated by said PWM control circuit, in conformity to said configuration of output signals produced by said ROM;
at least a multiplexer circuit apt to select between bridge type and unipolar-motor type driving mode in function of a conditioning signal generated by said ROM and to reproduce said driving signals generated by said combinatory logic circuit and fed to input terminals of said multiplexer circuit on output terminals thereof which are operatively connected to said driving terminals of said integrated power switching devices through enabling/disabling means controlled by enable/disable signals produced by said ROM.

4. The circuit according to claim 3, wherein said enabling/disabling means of the outputs of said multiplexer include an equal number of logic AND gates cascaded respectively therefrom, each being capable of receiving through a first input terminal one of said driving signals coming from one of said output terminals of said multiplexer circuit and, through a second input terminal, an enable/disable signal coming from said ROM and to produce, while in an enable condition, on an output terminal a driving signal which is fed to the driving terminal of the respective integrated power switching device.

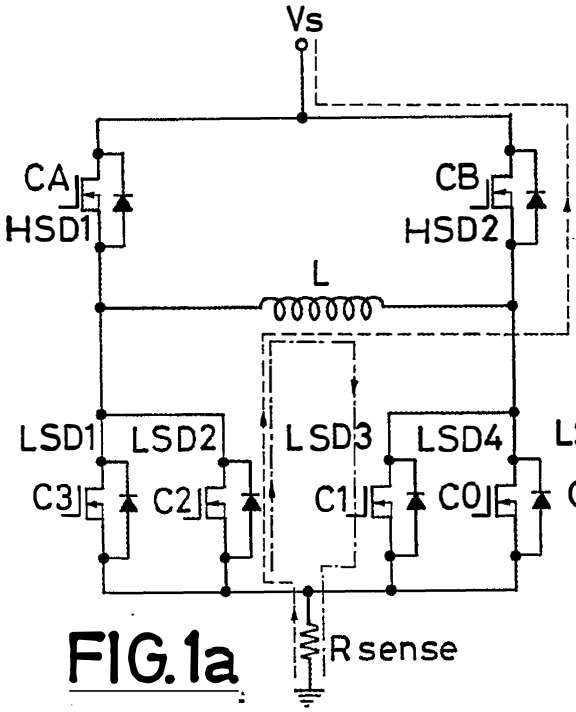


FIG.1a

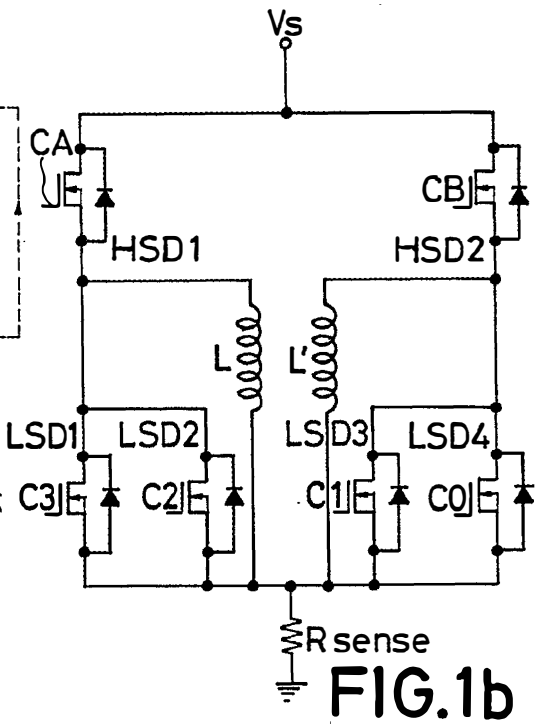


FIG.1b

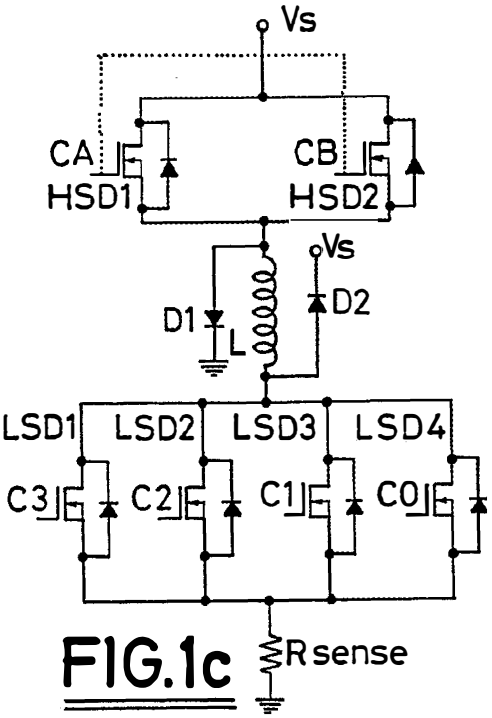


FIG.1c

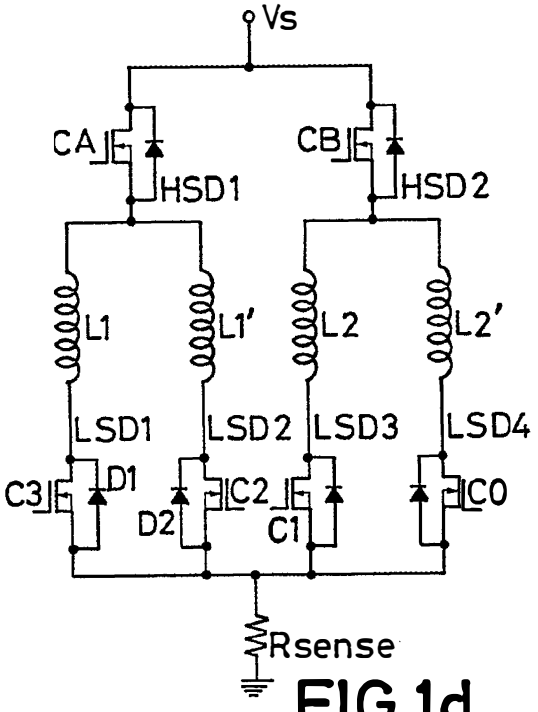


FIG.1d

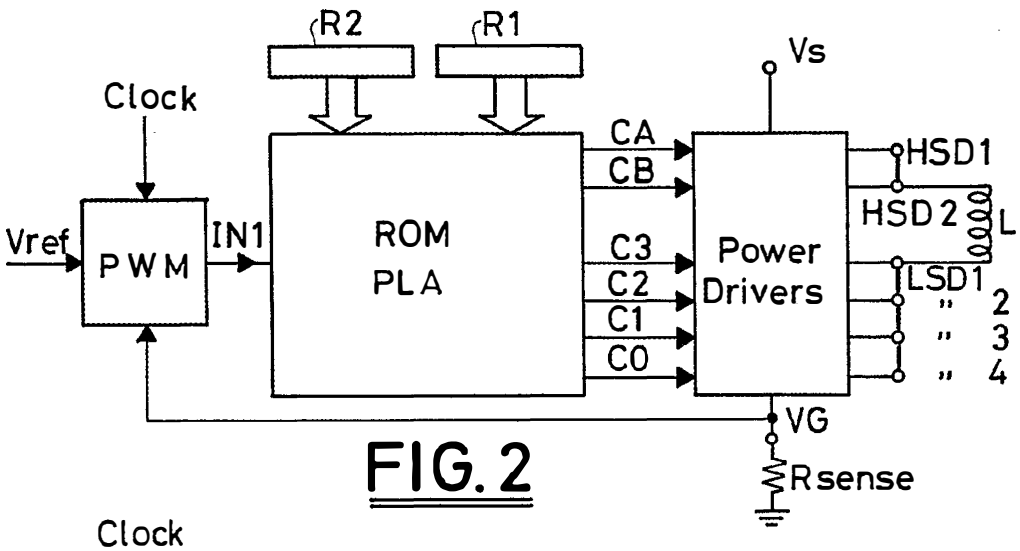


FIG. 2

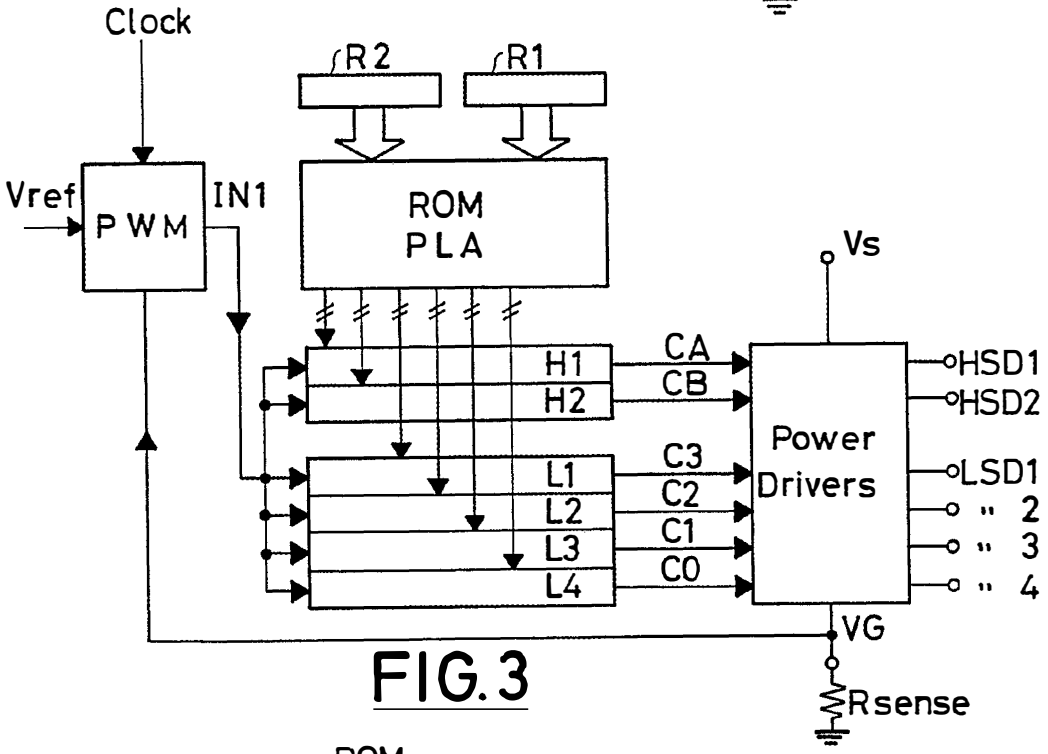


FIG. 3

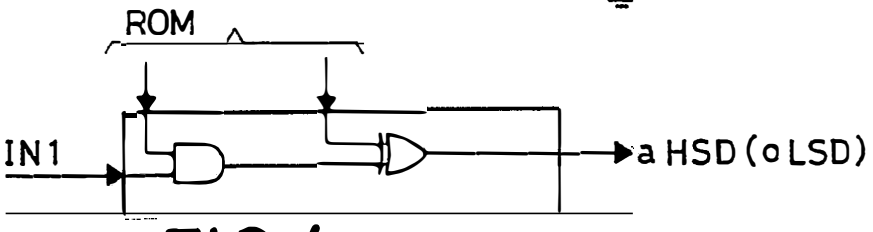


FIG. 4

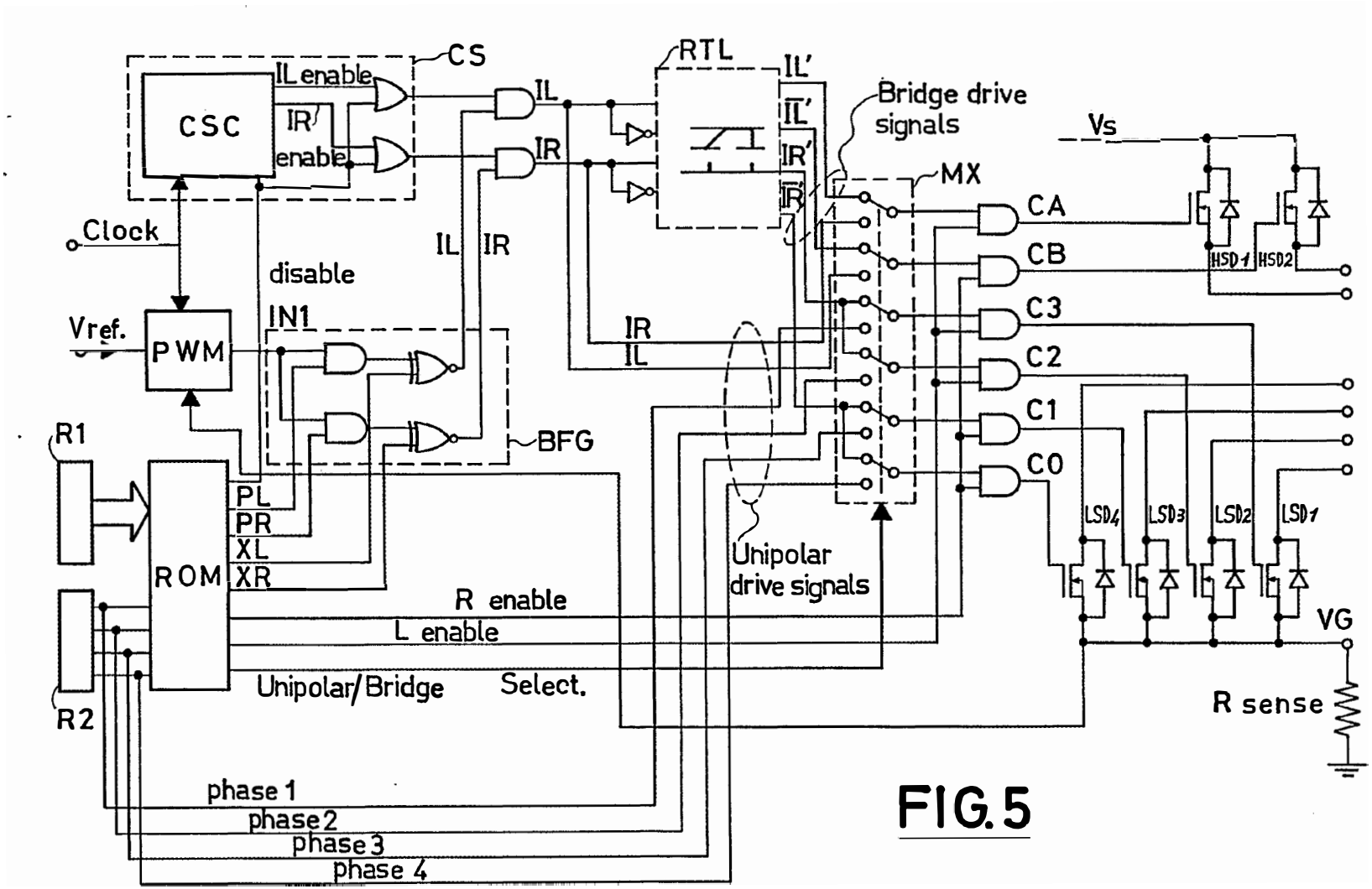


FIG.5

EP 0 369 954 A1

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 89 83 0493

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
Y	EP-A-187224 (IBM) * abstract; figure 1 *	1	H02P7/00
Y	EP-A-198248 (ARNOLD MUELLER GMBH) * abstract; claims 1, 5 *	1	
A		2, 3	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

H02P

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	09 FEBRUARY 1990	BEYER F.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

1

EPO FORM 1503 03.82 (P0401)

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference	**FOR FURTHER ACTION**	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
BCT140220GDE		
International application No.	International filing date *(day/month/year)*	(Earliest) Priority Date *(day/month/year)*
PCT/EP2014/061350	2 June 2014 (02-06-2014)	3 June 2013 (03-06-2013)
Applicant		
ST-ERICSSON SA		

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 3 sheets.

[X] It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**
   a. With regard to the **language,** the international search was carried out on the basis of:
      [X] the international application in the language in which it was filed
      [ ] a translation of the international application into _____, which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))
   b. [ ] This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6*bis*(a)).
   c. [ ] With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.

2. [ ] **Certain claims were found unsearchable** (See Box No. II)

3. [ ] **Unity of invention is lacking** (see Box No III)

4. With regard to the **title,**
   [X] the text is approved as submitted by the applicant
   [ ] the text has been established by this Authority to read as follows:

5. With regard to the **abstract,**
   [X] the text is approved as submitted by the applicant
   [ ] the text has been established, according to Rule 38.2, by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority

6. With regard to the **drawings,**
   a. the figure of the **drawings** to be published with the abstract is Figure No. 2
      [X] as suggested by the applicant
      [ ] as selected by this Authority, because the applicant failed to suggest a figure
      [ ] as selected by this Authority, because this figure better characterizes the invention
   b. [ ] none of the figures is to be published with the abstract

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2014/061350

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03F3/217 H02M3/156 H03K17/693 H02P7/00
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03F H02M H03K H02P

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 1 526 643 A1 (HEWLETT PACKARD DEVELOPMENT CO [US]) 27 April 2005 (2005-04-27) the whole document	1-15
A	EP 0 369 954 A1 (SGS THOMSON MICROELECTRONICS [IT]) 23 May 1990 (1990-05-23) the whole document	1-15

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
30 June 2014	07/07/2014

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Van den Doel, Jules

1

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2014/061350

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 1526643 A1	27-04-2005	EP 1526643 A1	27-04-2005
		JP 2005130694 A	19-05-2005
		US 2005088125 A1	28-04-2005
EP 0369954 A1	23-05-1990	DE 68918232 D1	20-10-1994
		DE 68918232 T2	02-02-1995
		EP 0369954 A1	23-05-1990
		IT 1225630 B	22-11-1990
		JP H02184295 A	18-07-1990
		US 4972130 A	20-11-1990

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:

see form PCT/ISA/220

PCT

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43*bis*.1)

Date of mailing
(day/month/year) see form PCT/ISA/210 (second sheet)

Applicant's or agent's file reference
see form PCT/ISA/220

FOR FURTHER ACTION
See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/EP2014/061350	02.06.2014	03.06.2013

International Patent Classification (IPC) or both national classification and IPC
INV. H03F3/217 H02M3/156 H03K17/693 H02P7/00

Applicant
ST-ERICSSON SA

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☐ Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step and industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☐ Box No. VII Certain defects in the international application
- ☒ Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will usually be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notifed the International Bureau under Rule 66.1*bis*(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

Name and mailing address of the ISA:	Date of completion of this opinion	Authorized Officer
European Patent Office P.B. 5818 Patentlaan 2 NL-2280 HV Rijswijk - Pays Bas Tel. +31 70 340 - 2040 Fax: +31 70 340 - 3016	see form PCT/ISA/210	Van den Doel, Jules Telephone No. +31 70 340-2761

Form PCT/ISA/237 (Cover Sheet) (July 2009)

Box No. I Basis of the opinion

1. With regard to the **language**, this opinion has been established on the basis of:

   ☒ the international application in the language in which it was filed

   ☐ a translation of the international application into , which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1 (b)).

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43bis.1(a))

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of a sequence listing filed or furnished:

   a. (means)

      ☐ on paper

      ☐ in electronic form

   b. (time)

      ☐ in the international application as filed

      ☐ together with the international application in electronic form

      ☐ subsequently to this Authority for the purposes of search

4. ☐ In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

Box No. VIII Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

see separate sheet

Re Item VIII

Certain observations on the international application

The application does not meet the requirements of Article 6 PCT, because the claims are substantially unclear.

It is unclear in claim 1 what is meant with "configurable input/output terminals". It is not clear which technical features distinguish these terminals (T1 - T4) to make them "configurable".

It is furthermore clear from the description that the configurable circuit is an integrated circuit as the problem solved by the invention is to avoid wasting available die space. This feature seems therefore essential to the definition of the invention.

Since independent claim 1 does not contain this feature it does not meet the requirement following from Article 6 PCT, taken in combination with Rule 6.3(b) PCT, that any independent claim must contain all the technical features essential to the definition of the invention.

The application also does not meet the requirements of Article 5 PCT because it cannot be carried out by a skilled person. Nowhere in the description, figures or claims it is disclosed how the various configurations and re-configurations can be implemented and in particular how the transitions between the different operating states can be implemented.

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	RECONFIGURABLE OUTPUT STAGE
First Named Inventor/Applicant Name:	Philippe SIRITO-OLIVIER
Filer:	Steven Maurice Dubois/Andrea Terry
Attorney Docket Number:	0112-301/C03308 US1

Filed as Large Entity

Filing Fees for U.S. National Stage under 35 USC 371

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
National Stage Fee	1631	1	280	280
Natl Stage Search Fee - Report provided	1642	1	480	480
National Stage Exam - all other cases	1633	1	720	720
Pages:				
Claims:				
Miscellaneous-Filing:				
Oath/Decl > 30 Mos From 371 commencement	1617	1	140	140
Petition:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1620**

Electronic Acknowledgement Receipt

EFS ID:	24019872
Application Number:	14889892
International Application Number:	PCT/EP2014/061350
Confirmation Number:	9535
Title of Invention:	RECONFIGURABLE OUTPUT STAGE
First Named Inventor/Applicant Name:	Philippe SIRITO-OLIVIER
Customer Number:	113648
Filer:	Steven Maurice Dubois/Andrea Terry
Filer Authorized By:	Steven Maurice Dubois
Attorney Docket Number:	0112-301/C03308 US1
Receipt Date:	09-NOV-2015
Filing Date:	
Time Stamp:	11:17:38
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$1620
RAM confirmation Number	9308
Deposit Account	505835
Authorized User	DUBOIS, STEVEN M

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal of New Application	C03308-US1_2015-11-09_371_Application_Transmittal_0112-301.pdf	221587 f97c99e75b506f2548a21dc464c32807fa38706a	no	4
Warnings:					
Information:					
2	Application Data Sheet	C03308-US1_2015-11-09_ADS_0112-301.pdf	1819123 9cb5a5c9dc5d4434a5f644bd1b9c913dd3cee0d1	no	7
Warnings:					
Information:					
3		C03308-US1_2015-11-09_Prelminary_Amendment_0112-301.pdf	158678 30d61fff075d87a983a0cee9f231231daaa22823	yes	8

Multipart Description/PDF files in .zip description		
Document Description	**Start**	**End**
Preliminary Amendment	1	1
Claims	2	7
Applicant Arguments/Remarks Made in an Amendment	8	8

Warnings:					
Information:					
4		C03308-US1_2015-11-09_as-filed_Application_0112-301.pdf	1483464 69ed057cfe2c07ece046ca13cf64d7b14023049	yes	28

Multipart Description/PDF files in .zip description		
Document Description	**Start**	**End**
Abstract	1	1
Specification	2	19
Claims	20	24

	Drawings-only black and white line drawings		25	28	
Warnings:					
Information:					
5	Information Disclosure Statement (IDS) Form (SB08)	C03308-US1_2015-11-09_IDS_0112-301.pdf	1035406 6771c31364b2c4f27b6b8dd1d8c512207ad21d30	no	4
Warnings:					
Information:					
A U.S. Patent Number Citation or a U.S. Publication Number Citation is required in the Information Disclosure Statement (IDS) form for autoloading of data into USPTO systems. You may remove the form to add the required data in order to correct the Informational Message if you are citing U.S. References. If you chose not to include U.S. References, the image of the form will be processed and be made available within the Image File Wrapper (IFW) system. However, no data will be extracted from this form. Any additional data such as Foreign Patent Documents or Non Patent Literature will be manually reviewed and keyed into USPTO systems.					
6	Foreign Reference	EP1526643A1.pdf	606060 ce3e3a03eb7ea8b1ec00c9406b11dd43b6d1b02b	no	13
Warnings:					
Information:					
7	Foreign Reference	EP0369954.pdf	1552797 3c0b40d0198cac8c431ef6993c297dbe449d97ec	no	11
Warnings:					
Information:					
8	Non Patent Literature	NPL_ISR.pdf	261796 71094dd30c60695a0ea69f0ab48985bf6a044834	no	3
Warnings:					
Information:					
9	Non Patent Literature	NPL_Written_Opinion.pdf	274713 2317ab9b66adf63b57a4ffd4d01bba92f4cead92	no	3
Warnings:					
Information:					
10	Non Patent Literature	NPL_EESR.pdf	333545 6991cde5677baf875dd33c8702f8b6e6ab96c96a	no	5
Warnings:					
Information:					
11	Fee Worksheet (SB06)	fee-info.pdf	37009 6eb03ebdf868f9b56f0c9dde6b4bc05bcbb5da17	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	7784178		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Europäisches Patentamt
European Patent Office
Office européen des brevets

Bescheinigung	Certificate	Attestation
Die angehefteten Unterlagen stimmen mit der als ursprünglich eingereicht geltenden Fassung der auf dem nächsten Blatt bezeichneten europäischen Patentanmeldung überein.	The attached documents are exact copies of the text in which the European patent application described on the following page is deemed to have been filed.	Les documents joints à la présente attestation sont conformes au texte, considéré comme initialement déposé, de la demande de brevet européen qui est spécifiée à la page suivante.

Patentanmeldung Nr.	**Patent application No.**	**Demande de brevet n°**
	13305740.6 / EP13305740	

The organization code and number of your priority application, to be used for filing abroad under the Paris Convention, is EP13305740.

Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office

Le President de l'Office européen des brevets
p.o.

U. Ingmann

Anmeldung Nr:
Application no.: 13305740.6
Demande no :

Anmeldetag:
Date of filing: 03.06.13
Date de dépôt :

Anmelder / Applicant(s) / Demandeur(s):

ST-Ericsson SA
39 Chemin du Champ-des-Filles
1228 Plan-les-Ouates
Geneva/CH

Bezeichnung der Erfindung / Title of the invention / Titre de l'invention:
(Falls die Bezeichnung der Erfindung nicht angegeben ist, oder falls die Anmeldung in einer Nicht-Amtssprache des EPA eingereicht wurde, siehe Beschreibung bezüglich ursprünglicher Bezeichnung.
If no title is shown, or if the application has been filed in a non-EPO language, please refer to the description for the original title.
Si aucun titre n'est indiqué, ou si la demande a été déposée dans une langue autre qu'une langue officielle de l'OEB, se référer à la description pour le titre original.)

Reconfigurable output stage

In Anspruch genommene Priorität(en) / Priority(Priorities) claimed / Priorité(s) revendiquée(s)
Staat/Tag/Aktenzeichen / State/Date/File no. / Pays/Date/Numéro de dépôt:

Am Anmeldetag benannte Vertragstaaten / Contracting States designated at date of filing / Etats contractants désignées lors du dépôt:

AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR

Description

RECONFIGURABLE OUTPUT STAGE

Technical Field

[0001] The proposed solution relates generally to output stage circuits, and more especially to a reconfigurable output stage.

Background Art

[0002] Recently, designers of portable and other low power electronic devices have devised multimedia features in order for their products to attract more attention from potential customers. Internally to these devices, subsystem circuits such as audio subsystems have an increasingly important role on the realisation of these features and, thus, on user experience.

[0003] A typical audio subsystem, for instance, may combine in a single integrated circuit, various audio configurations for driving multiple output speakers such as a headphone, a hands-free loudspeaker and a receiver speaker, each of these audio configurations potentially having respective output power requirements. For instance, an audio subsystem may use a Class-D amplifier in different audio configurations for driving a circuit such as a hands–free loudspeaker. In fact, depending on the user's need and due to its high power and high efficiency, a Class-D amplifier may provide different levels of loudness. For example, when a medium loudness is required, e.g. 1W, the Class-D amplifier may be powered by the battery of the device. In this configuration the sound loudness would depend on the battery charge state. In another example, when a high loudness is required, e.g. 2W, the Class-D amplifier may be powered by a DC-DC boost converter. In this configuration, the sound loudness could be constant whatever the battery charge state.

[0004] However, with such type of audio subsystems, when only the medium loudness audio configuration is used the DC-DC boost converter is not used. This is inefficient and represents extra subsystems costs due to the unused die area.

Summary

[0005] There is thus a need for an improved subsystem circuit structure which maximises the die area usage and thus reduce the subsystem costs.

Therefore, it is proposed an output stage suitable for use in a subsystem circuit which can be shared between at least two subsystem circuit components. Namely, the proposed output stage may be adapted to work with particular subsystem circuit components. Hence, with the above example of the audio subsystem and contrary to the prior art, only one output stage is needed for both the Class-D amplifier and the DC-DC boost converter within an audio subsystem circuit structure. In fact in the prior art, two output stages are needed, i.e. one output stage for each of the Class-D amplifier and the DC-DC boost converter.

[0006] In a first aspect of the solution described herein, there is proposed an electronic circuit output stage adapted to operate in at least a first operating state and a second operating state, the output stage comprising:

– a first, a second, a third and a fourth configurable input/output terminals; and,

– a first, a second, a third and a fourth switches, each having a first main terminal, a second main terminal and a control terminal, the control terminal being adapted to receive a control signal for controlling the open or closed state of the switch;

wherein,

– the first input/output terminal is connected to the first main terminal of the first switch; – the second input/output terminal is connected to the first main terminal of the second switch;

– the second main terminal of the first switch is connected to the first main terminal of the third switch through a first branch,

– the second main terminal of the second switch is connected to the first main terminal of the fourth switch through a second branch;

– the third input/output terminal is connected to the first branch and the fourth input/output terminal is connected to the second branch;

– the second main terminals of the third and fourth switches are both connected to a common node receiving a reference potential; and,

wherein,

– when the first and second input/output terminals are configured to

operate as input terminals, the third and fourth input/output terminals are configured to operate as output terminals; and,

– when the first and second input/output terminals are configured to operate as output terminals, the third and fourth input/output terminals are configured to operate as input terminals; and,

wherein,

– in the first operating state, the output stage is arranged in a first electrical configuration; and

– in the second operating state wherein the output stage is arranged in a second electrical configuration different from the first configuration

[0007] In a first embodiment of the first aspect, in the first operating state:

– the first and second input/output terminals are configured to operate as input terminals and are configured to be connected to a common node receiving a supply potential; and,

– the third and fourth input/output terminals are configured to be connected to a load element.

[0008] Advantageously, this embodiment may allow creating a class-D configuration.

[0009] In a second embodiment of the first aspect, in the second operating state, the output stage may further comprise an inductor and a decoupling capacitor, wherein:

– the first and second input/output terminals are configured to operate as output terminals and are configured to be connected, in series with a load element and in parallel with the decoupling capacitor;

–the third and fourth input/output terminals are short-circuited ;

– one end of the inductor is configured to be connected to the short circuited third and fourth input/output terminals and another end the inductor is configured to be connected to a node receiving a supply potential.

[0010] Advantageously, this embodiment may allow creating a boost DCDC configuration.

[0011] In a third, alternative embodiment of the first aspect, in the second operating state, the output stage may further comprise an inductor and a

decoupling capacitor, wherein:

– the first and second input/output terminals are configured to operate as input terminals and are configured to be connected to a common node receiving a supply potential;

–the third and fourth input/output terminals are short-circuited;

– one end of the inductor is configured to be connected to the short-circuited third and fourth input/output terminals and another end the inductor is configured to be connected, in series with a load element and in parallel with the decoupling capacitor.

[0012] Advantageously, this embodiment may allow creating a buck DCDC configuration.

[0013] In a fourth possible embodiment of the first aspect, in the second operating state, the output stage may further comprise a first and second inductor and a first and second decoupling capacitor, wherein:

– the first and second input/output terminals are configured to operate as output terminals;

– the first input/output terminal is configured to be connected, in series with a first load element and in parallel with the first decoupling capacitor;

– the second input/output terminal is configured to be connected, in series with a second load element and in parallel with the second decoupling capacitor;

– one end of the first inductor is configured to be connected to the third input/output terminal and another end of the first inductor is configured to be connected to a common node receiving a supply potential;

– one end of the second inductor is configured to be connected to the fourth input/output terminal and another end of the second inductor is configured to be connected to the node receiving a supply potential.

[0014] Advantageously, this embodiment may allow creating a double boost DCDC.

[0015] In a fifth embodiment of the first aspect, in the second operating state, the output stage may further comprise a first and second inductor and a first and second decoupling capacitor, wherein:

– the first and second input/output terminals are configured to operate as

input terminals and are configured to be connected to a common node receiving a supply potential;

– one end of the first inductor is configured to be connected to the third input/output terminal and another end of the first inductor is configured to be connected, in series with a first load element and in parallel with the first decoupling capacitor;

– one end of the second inductor is configured to be connected to the fourth input/output terminal and another end of the second inductor is configured to be connected, in series with a second load element and in parallel with the second decoupling capacitor.

[0016] Advantageously, this embodiment may allow creating a double buck DCDC.

[0017] For instance, in a sixth embodiment of the first aspect, in the second operating state, the output stage may further comprise a first and second inductor and a first and second decoupling capacitor, wherein:

– the first and second input/output terminals are configured to operate as input terminals;

– the third input/output terminal is configured to be connected, in series with a first load element and in parallel with the first decoupling capacitor;

– one end of the first inductor is configured to be connected to the first input/output terminal and another end of the first inductor is configured to be connected to a first node receiving a supply potential;

– one end of the second inductor is configured to be connected to the fourth input/output terminal and another end of the second inductor is configured to be connected, in series with a second load element and in parallel with the second decoupling capacitor.

[0018] Advantageously, this embodiment may allow creating a double DCDC, comprising a buck configuration, and a boost configuration.

[0019] In a second aspect of the solution, there is proposed a control apparatus comprising:

– a control stage configured to control an output stage according to the first embodiment of the first aspect.

[0020] In an embodiment of the second aspect, the control stage is a Class-D control stage.

[0021] In a third aspect of the solution, there is proposed a control apparatus comprising:

– a control stage configured to control an output stage according to any one of the second to sixth embodiments of the first aspect.

[0022] In an embodiment of the third aspect, the control stage is a DC-DC converter control stage.

[0023] In an embodiment of second and/or third aspects, the control stage is adapted to control the output stage by generating control signals for controlling the first, second, third and fourth switches through their respective control terminals.

[0024] In a fourth aspect of the solution, there is proposed a circuit comprising:

– an output stage according to any one of the first to the sixth embodiments of the first aspect;

– a first control apparatus according to the second aspect wherein the control stage of the first control apparatus is connected to the output stage; and,

– a second control apparatus according to the third aspect wherein the control stage of the second control apparatus is connected to the output stage, wherein:

– when the control stage of the first control apparatus is connected to the output stage, the control stage of the second control apparatus is electrically disconnected from the output stage, the output stage being configured to operate in the first operating state; and,

– when the control stage of the second control apparatus is connected to the output stage, the control stage of the first control apparatus is electrically disconnected from the output stage, the output stage being configured to operate in the second operating state.

[0025] In a fifth aspect of the solution, there is proposed a device comprising:

– the circuit of the fourth aspect;

– a battery configured to be connected to the input terminals of the circuit; and,

– a loudspeaker configured to be connected to the output terminals of the circuit.

[0026] In a sixth aspect of the solution, there is proposed the use of an output stage according to any one of the first to the sixth embodiments of the first aspect in conjunction with:

– a first control apparatus according to the second aspect wherein the control stage of the first control apparatus is connected to the output stage; and,

– a second control apparatus according to the third aspect wherein the control stage of the second control apparatus is connected to the output stage, wherein:

– when the control stage of the first control apparatus is connected to the output stage, the control stage of the second control apparatus is electrically disconnected from the output stage, the output stage being configured to operate in the first operating state; and,

– when the control stage of the second control apparatus is connected to the output stage, the control stage of the first control apparatus is electrically disconnected from the output stage, the output stage being configured to operate in the second operating state.

Brief description of drawings

[0027] A more complete understanding of the proposed solution may be obtained from a consideration of the following description in conjunction with the drawings, in which like reference numbers indicate same or similar elements. In the drawings:

[0028] FIG. 1 is a block diagram illustrating an audio subsystem;

[0029] FIG. 2 is a block diagram illustrating an exemplary output stage of the proposed solution;

[0030] FIGs. 3-8 are a block diagrams illustrating embodiments of the proposed solution.

Description of embodiments

[0031] The following detailed description is exemplary in nature and is not intended to limit the scope, applicability, or configuration of the invention in any way. Rather, the following description provides practical illustrations

for implementing exemplary embodiments of the present invention. Examples of constructions, materials, dimensions, and manufacturing processes are provided for selected elements, and all other elements employ that which is known to those of skill in the field of the invention. Those skilled in the art will recognize that many of the examples provided have suitable alternatives that can be utilized.

[0032] FIG. 1 is a block diagram schematically illustrating an audio subsystem 100.

[0033] In FIG. 1, there is shown therein the audio subsystem 100 comprising one audio DAC unit 110 (i.e. Digital to Analog Converter), one gain matrix unit 120, one class-AB amplifiers 130 , two class-AB amplifiers 150, one Class-D amplifier 140, one ear speaker 160, one hands-free speaker 170 and one headphone 180. It is considered herein that there are two class-AB amplifiers 150 that can drive a stereo headphone.

[0034] Referring to FIG. 1, the audio DAC 110 is coupled to the gain matrix 120, which is coupled to the amplifiers 130, 140, 150, which are respectively coupled to the ear speaker 160, the hands-free speaker 170 and the headphone 180.

[0035] The DAC 110 aims at generating at least one audio signal which gain may be modified by the gain matrix 120 prior being amplified by an amplifier 130, 140, 150 and being reproduced by a speaker 160, 170, 180.

[0036] As stated above, the Class-D amplifier 140 may be used in different audio configurations depending on the user's need of loudness. However, different circuit components may be used in different audio configurations thus resulting in a waste of circuit die area when only one or more of the circuit components are in used while the others are not.

[0037] By way of example, let's consider a case where the Class-D amplifier 140 and a DC-DC boost converter are the circuit components used in one or more audio configurations to drive a speaker, 170. It is indicated that other configurations and other components may be used herein. Each of the Class-D amplifier 140 and the DC-DC boost converter is usually organised into two parts:

- a output stage providing the required output; and,

- a control stage for controlling the output stage .

However in the proposed example, when the Class-D is used alone in the audio configuration (e.g. for a medium output loudness), only the control stage and output stage of the Class-D amplifier are used while the control stage and output stage of the DC-DC boost converter are not used. As stated above, this situation results in wastage of the circuit die area.

[0038] In order to solve this problem, it is proposed an electronic circuit output stage adapted to operate in at least a first operating state and a second operating state, such that the output stage may be shared by at least two circuit components such as the Class-D amplifier and the DC-DC boost converter. This way in the example proposed above, the proposed control stage would always be in used in all associated audio configurations.

[0039] FIG. 2 is a block diagram schematically illustrating an exemplary output stage 200 according to the proposed solution.

[0040] In FIG. 2, there is shown therein the output stage 200 comprising:

– a first configurable input/output terminal T_1, a second configurable input/output terminal T_2, a third configurable input/output terminal T_3 and a fourth configurable input/output terminal T_4; and,

– a first switch S_1, a second switch S_2, a third switch S_3 and a fourth switch S_4. The switches S1, S2, S3, S4 may be MOS transistors, NMOS transistors or other transistors of the same or different kind.

[0041] Referring to FIG. 2, the configurable input/output terminal T_1, T_2, T_3, T_4 are configured to operate as input or output terminals such that:

– when the first input/output terminal T1 and second input/output terminal T2 are configured to operate as input terminals, the third input/output terminal T3 and fourth input/output terminal T4 are configured to operate as output terminals; and,

– when the first input/output terminal T1 and second input/output terminal T2 are configured to operate as output terminals, the third input/output terminal T3 and fourth input/output terminal T4 are configured to operate as input terminals.

[0042] Further in FIG. 2, each of the switches S_1, S_2, S_3, S_4 has a first main terminal 1, a second main terminal 2 and a control terminal 3 wherein the

control terminal 3 is adapted to receive a control signal for controlling the open or closed state of the associated switch.

[0043] Structurally, the output stage 200 is organised as follows. The first input/output terminal T1 is connected to the first main terminal 1 of the first switch S1. The second input/output terminal T2 is connected to the first main terminal 1 of the second switch S2. The second main terminal 2 of the first switch S1 is connected to the first main terminal 1 of the third switch S3. The latter connection is forming a first branch 4 of the output stage 200. The second main terminal 2 of the second switch S2 is connected to the first main terminal 1 of the fourth switch s4. The latter connection is forming a second branch 5 of the output stage 200. The third input/output terminal T3 is connected to the first branch 4 of the output stage 200 and the fourth input/output terminal T4 is connected to the second branch 5 of the output stage 200. The second main terminal 2 of the third switch S3 and the second main terminal 2 of fourth switches S4 are both connected to a common node receiving a reference potential VREF of the output stage 200.

[0044] Referring to FIG. 2, when in the first operating state, the output stage is arranged in a first electrical configuration, and when in the second operating state wherein the output stage is arranged in a second electrical configuration different from the first configuration.

[0045] FIG. 3 is a block diagram schematically illustrating a first exemplary embodiment of the proposed solution wherein the output stage 200 of FIG.2 is used, in the first operating state.

[0046] In the example of FIG. 3, the first input/output terminal T1 and second input/output terminal T2 are configured to operate as input terminals and are also configured to be connected to a common node receiving a supply potential 201. The common node receiving a supply potential 201 may be a battery, a DC-DC boost converter or any similar DC power source which needs to be recharged on a periodic basis. Further, in FIG. 3, the third input/output terminal T3 and fourth input/output terminal T4 are configured to be connected to a load element. For example, the load element may be an audio speaker 202. In such case, the third input/output terminal T3 and

fourth input/output terminal T4 may be connected respectively with a first and second end of the audio speaker 202. In another example, the load element may be a motor such as a vibration motor usually used in mobile phone. It is indicated that other components may be used herein. As can be seen, the structure of the output stage 200 in the example of FIG. 3 is an H-bridge circuit structure, thus the output stage 200 may be controlled by an H-bridge control stage 10. Namely, the switches S1, S2, S3, S4 of the output stage 200 may be controlled by the H-bridge control stage 10. In the case of audio subsystems, the H-bridge control stage 10 may be the control stage of a Class-D amplifier. If it is the case, the combination of a Class-D amplifier control stage and the output stage 200 of the FIG. 3 would correspond to the realisation of a Class-D amplifier.

[0047] FIG. 4 is a block diagram schematically illustrating a second exemplary embodiment of the proposed solution wherein the output stage 200 of FIG.2 is used, in the second operating state.

[0048] In the example of FIG. 4, the output stage 200 may further comprise one inductor 204 and one decoupling capacitor 205. Further, in FIG. 4, the first input/output terminal T1 and second input/output terminal T2 are configured to operate as output terminals and are also configured to be connected, in series with a load element 30 and, in parallel with the decoupling capacitor 205. In this configuration, the decoupling capacitor 205 is used for removing on-chip high frequency noise. Also, in FIG. 4, the third input/output terminal T3 and fourth input/output terminal T4 are short-circuited 6. Additionally, in FIG. 4, one end of the inductor 204 is configured to be connected to the short-circuit 6 and another end the inductor 204 is configured to be connected to a common node receiving a supply potential 203 similar to those already presented in FIG. 3. As can be seen, the structure of the output stage 200 in the example of FIG. 4 is not an H-bridge circuit structure since the load element is not on the central branch of the structure. Rather, the structure of the output stage 200 in the example of FIG. 4 may be seen as two branches 4, 5 which are arranged in parallel. Therefore, any control stage 20 that may control such structure may be used. In one embodiment, the control stage 20 may use

the same signal to control two switches S1, S2, S3, S4 which are situated on parallel branches of the output stage 200 of the FIG. 4. In this case, the output stage 200 would be similar to a circuit structure comprising only a single branch. In this case, a DC-DC control stage may be used to control the output stage 200 in the example of FIG. 4. If it is the case, the combination of a DC-DC control stage and the output stage 200 of the FIG. 4 would correspond to the realisation of a DC-DC boost converter configured to, at least, step-up an input voltage.

[0049] FIG. 5 is a block diagram schematically illustrating a third exemplary embodiment of the proposed solution wherein the output stage 200 of FIG.2 is used, in the second operating state.

[0050] In the example of FIG. 5, the output stage 200 may further comprise one inductor 212 and one decoupling capacitor 213 similar to those already presented in FIG 4. Further, in FIG. 5, the first input/output terminal T1 and second input/output terminal T2 are configured to operate as input terminals and are also configured to be connected to a common node receiving a supply potential 203 similar to those already presented in FIG. 3. Also, in FIG. 5, a short circuit 6 is created between the third input/output terminal T3 and fourth input/output terminal T4. Additionally, in FIG. 5, one end of the inductor 212 is configured to be connected to the short circuit 6 and another end the inductor 212 is configured to be connected, in series with a load element 30 and, in parallel with the decoupling capacitor 213. As can be seen, the structure of the output stage 200 in the example of FIG. 4 is not an H-bridge circuit structure since the load element 30 is not directed connected to the central branch of the structure. Rather, the structure of the output stage 200 in the example of FIG. 5 may be seen as having, mutatis mutandis, the same structure presented in FIG. 4. Thus, in one embodiment, the control stage 20 may be a DC-DC control stage which may be used to control the output stage 200 in the example of FIG. 5. If it is the case, the combination of a DC-DC control stage and the output stage 200 of the FIG. 5 would correspond to the realisation of a DC-DC buck converter configured to, at least, step-down an input voltage.

[0051] FIG. 6 is a block diagram schematically illustrating a fourth exemplary embodiment of the proposed solution wherein the output stage 200 of FIG.2 is used, in the second operating state.

[0052] In the example of FIG. 6, the output stage 200 may further comprise one first inductor 207, one second inductor 208, one first decoupling capacitor 209 and one second decoupling capacitor 210. Further, in FIG. 6, the first input/output terminal T1 and second input/output terminal T2 are configured to operate as output terminals. The first input/output terminal T1 is further configured to be connected, in series with a first load element 30 and in parallel with the first decoupling capacitor 209. The second input/output terminal T2 is further configured to be connected, in series with a second load element 40 and in parallel with the second decoupling capacitor 210. Also, one end of the first inductor 207 is configured to be connected to the third input/output terminal T3 and another end of the first inductor 207 is configured to be connected to a common node receiving a supply potential 206 similar to those already presented in FIG. 3. Additionally, one end of the second inductor 208 is configured to be connected to the fourth input/output terminal T4 and another end of the second inductor 208 is configured to be connected to the above-mentioned common node receiving a supply potential 206. As can be seen, the structure of the output stage 200 in the example of FIG. 6 is not an H-bridge circuit structure since the load elements 30, 40 are not directed connected to the central branch of the structure. Rather, the structure of the output stage 200 in the example of FIG. 6 may be seen as having, mutatis mutandis, the same structure presented in FIG. 4. Thus, in one embodiment, the control stage 20 may be a DC-DC control stage which may be used to control the output stage 200 in the example of FIG. 6. If it is the case, the combination of a DC-DC control stage and the output stage 200 of the FIG. 6 would correspond to the realisation of a double DC-DC boost converter configured to, at least, step-up an input voltage. Also, due to the fact that each branch of the structure may be controlled independently by the control stage 20, using a DC-DC control stage enables to generate different voltage on each branch 4,5 of the

output stage that may be used to supply in voltage the load elements 30, 40.

[0053] FIG. 7 is a block diagram schematically illustrating a fifth exemplary embodiment of the proposed solution wherein the output stage 200 of FIG.2 is used, in the second operating state.

[0054] In the example of FIG. 7, the output stage 200 may further comprise one first inductor 215, one second inductor 217, one first decoupling capacitor 216 and one second decoupling capacitor 218. Further, in FIG. 7, the first input/output terminal T1 and second input/output terminal T2 are configured to operate as input terminals and are configured to be connected to a common node receiving a supply potential 214 similar to those already presented in FIG. 3. Also, one end of the first inductor 215 is configured to be connected to the third input/output terminal T3 and another end of the first inductor 215 is configured to be connected, in series with a first load element 30 and in parallel with the first decoupling capacitor 216. Additionally, one end of the second inductor 217 is configured to be connected to the fourth input/output terminal T4 and another end of the second inductor 217 is configured to be connected, in series with a second load element 40 and in parallel with the second decoupling capacitor 218. As can be seen, the structure of the output stage 200 in the example of FIG. 7 is not an H-bridge circuit structure since the load elements 30, 40 are not directed connected to the central branch of the structure. Rather, the structure of the output stage 200 in the example of FIG. 7 may be seen as having, mutatis mutandis, the same structure presented in FIG. 4. Thus, in one embodiment, the control stage 20 may be a DC-DC control stage which may be used to control the output stage 200 in the example of FIG. 7. If it is the case, the combination of a DC-DC control stage and the output stage 200 of the FIG. 7 would correspond to the realisation of a double DC-DC buck converter configured to, at least, step-down an input voltage. Also, due to the fact that each branch of the structure may be controlled independently by the control stage 20, using a DC-DC control stage enables to generate

different voltage on each branch 4,5 of the output stage that may be used to supply in voltage the load elements 30, 40.

[0055] FIG. 8 is a block diagram schematically illustrating a sixth exemplary embodiment of the proposed solution wherein the output stage 200 of FIG.2 is used, in the second operating state. Actually, the example of FIG.8 may correspond to a mix between the circuit structures of the examples of FIGs. 6-7.

[0056] Namely, in the example of FIG. 8, the output stage 200 may further comprise one first inductor 220, one second inductor 223, one first decoupling capacitor 221 and one second decoupling capacitor 224. Further, in FIG. 8, the first input/output terminal T1 and second input/output terminal T2 are configured to operate as input terminals. The third input/output terminal T3 is configured to be connected, in series with a first load element 30 and in parallel with the first decoupling capacitor 221. Also, one end of the first inductor 220 is configured to be connected to the first input/output terminal T1 and another end of the first inductor 220 is configured to be connected to a first node receiving a supply potential 219 similar to those already presented in FIG. 3. Additionally, one end of the second inductor 223 is configured to be connected to the fourth input/output terminal T4 and another end of the second inductor 223 is configured to be connected, in series with a second load element 40 and in parallel with the second decoupling capacitor 224. As can be seen, the structure of the output stage 200 in the example of FIG. 8 is not an H-bridge circuit structure al already explained above. Rather, the structure of the output stage 200 in the example of FIG. 6 may be seen as having, mutatis mutandis, the same structure presented in FIGs. 6-7. Thus, in one embodiment, the control stage 20 may be a DC-DC control stage which may be used to control the output stage 200 in the example of FIG. 6. If it is the case, the combination of a DC-DC control stage and the output stage 200 of the FIG. 6 would correspond to the realisation of a DC-DC buck-boost converter configured to, at least, step-up an input voltage in the first branch 4 of the output stage 200 and step-down an input voltage in the second branch 5 of the output stage 200. This is mainly due to the

fact that each branch of the structure may be controlled independently by the control stage 20, using a DC-DC control stage enables to generate different voltage on each branch 4,5 of the output stage that may be used to supply in voltage the load elements 30, 40.

[0057] In one embodiment, the switches S1, S2, S3, S4 may be controlled trough their respective control terminals based on control signals such a PWM signal which may be generated by a control stage 10, 20.

[0058] Several apparatuses such as control apparatuses may be realized based on the proposed solution. For example, a first control apparatus may comprise a control stage configured to control an output stage according to example of FIG. 3. In another example, a second control apparatus may comprise a control stage configured to control an output stage according to at least one of the examples of FIGs. 4-8.

[0059] Several uses and circuits may also be realized based on the proposed solution. In an example, a first circuit may comprise:

– an output stage according to at least one of the examples of FIGs. 3-8;

– the first control apparatus wherein the control stage of the first control apparatus is connected to the output stage; and,

– the second control apparatus wherein the control stage of the second control apparatus is connected to the output stage;

wherein,

– when the control stage of the first control apparatus is connected to the output stage, the control stage of the second control apparatus is electrically disconnected from the output stage, the output stage being configured to operate in the first operating state; and,

– when the control stage of the second control apparatus is connected to the output stage, the control stage of the first control apparatus is electrically disconnected from the output stage, the output stage being configured to operate in the second operating state.

[0060] In an example, such circuit may be used to drive a stereo hands free speaker. In that case, the first control apparatus may be a class-D controller and the second control apparatus may be a DC-DC controller.

This way, in a first operating state of the output stage, the circuit may be configured to behave as a class-D amplifier according for instance to FIG.3 wherein the load would be the stereo hands free speaker. In this case, the second control apparatus may be deactivated. In a second operating state of the output stage, the circuit may be configured to behave as a DC-DC converter. According to FIG.4, for instance, the circuit may be a DC-DC boost converter where the load 30 would be the stereo hands free speaker. According to FIG.5, for instance, the circuit may be a DC-DC buck converter where the load 30 would be the stereo hands free speaker. According to FIG.6, for instance, the circuit may be a double DC-DC boost converter where the loads 30, 40 may be different terminals of the stereo hands free speaker. According to FIG.7, for instance, the circuit may be a double DC-DC buck converter where the loads 30, 40 may be different terminals of the stereo hands free speaker. Finally, according to FIG.8, for instance, the circuit may be a DC-DC buck-boost converter able to drive different loads 30, 40 for voltage step-up or step-down wherein at least one may be the stereo hands free speaker.

[0061] Several devices, such as portable devices, may also be realized based on the proposed solution. For example, a device may comprise:

– the first circuit;

– a battery configured to be connected to the input terminals of the circuit; and,

– a loudspeaker configured to be connected to the output terminals of the circuit.

[0062] Although the proposed solution is described above in terms of various exemplary embodiments and implementations, it should be understood that the various features, aspects and functionality described in one or more of the individual embodiments are not limited in their applicability to the particular embodiment with which they are described, but instead may be applied, alone or in various combinations, to one or more of the other embodiments of the proposed solution, whether or not such embodiments are described and whether or not such features are presented as being a part of a described embodiment. Thus, the breadth and scope of the

present proposed solution should not be limited by any of the above-described exemplary embodiments. For instance, it is to appreciated that the output and the circuit may be used in other industries different from the audio that has been presented throughout the description. For example, the DC-DC feature of the circuit may be used in motor-based applications.

[0063] Terms and phrases used in this document, and variations thereof, unless otherwise expressly stated, should be construed as open ended as opposed to limiting. As examples of the foregoing: the term "including" should be read as meaning "including, without limitation" or the like; the term "example" is used to provide exemplary instances of the item in discussion, not an exhaustive or limiting list thereof; the terms "a" or "an" should be read as meaning "at least one," "one or more" or the like; and adjectives such as "conventional," "traditional," "normal," "standard," "known" and terms of similar meaning should not be construed as limiting the item described to a given time period or to an item available as of a given time, but instead should be read to encompass conventional, traditional, normal, or standard technologies that may be available or known now or at any time in the future. Likewise, where this document refers to technologies that would be apparent or known to one of ordinary skill in the art, such technologies encompass those apparent or known to the skilled artisan now or at any time in the future.

[0064] The presence of broadening words and phrases such as "one or more, least," "but not limited to" or other like phrases in some instances shall not be read to mean that the narrower case is intended or required in instances where such broadening phrases may be absent. Additionally, the various embodiments set forth herein are described in terms of exemplary block diagrams, flow charts and other illustrations. As will become apparent to one of ordinary skill in the art after reading this document, the illustrated embodiments and their various alternatives may be implemented without confinement to the illustrated examples. These illustrations and their accompanying description should not be construed as mandating a particular architecture or configuration.

Claims

1. An output stage adapted to operate in at least a first operating state and a second operating state, the output stage comprising:

– a first, a second, a third and a fourth configurable input/output terminals (T1, T2, T3, T4); and,

– a first, a second, a third and a fourth switches (S1, S2, S3, S4), each having a first main terminal (1), a second main terminal (2) and a control terminal (3), the control terminal being adapted to receive a control signal for controlling the open or closed state of the switch;

wherein,

– the first input/output terminal is connected to the first main terminal of the first switch;

– the second input/output terminal is connected to the first main terminal of the second switch;

– the second main terminal of the first switch is connected to the first main terminal of the third switch through a first branch,

– the second main terminal of the second switch is connected to the first main terminal of the fourth switch through a second branch;

– the third input/output terminal is connected to the first branch and the fourth input/output terminal is connected to the second branch;

– the second main terminals of the third and fourth switches are both connected to a common node receiving a reference potential; and,

wherein,

– when the first and second input/output terminals are configured to operate as input terminals, the third and fourth input/output terminals are configured to operate as output terminals; and,

– when the first and second input/output terminals are configured to operate as output terminals, the third and fourth input/output terminals are configured to operate as input terminals; and,

wherein,

– in the first operating state, the output stage is arranged in a first electrical configuration; and

– in the second operating state wherein the output stage is arranged in a second electrical configuration different from the first configuration..

2. The output stage of claim 1, wherein, in the first operating state:

– the first and second input/output terminals are configured to operate as input terminals and are configured to be connected to a common node receiving a supply potential; and,

– the third and fourth input/output terminals are configured to be connected to a load element (202).

3. The output stage of claim 1 further comprising an inductor (204) and a decoupling capacitor (205), wherein, in the second operating state:

– the first and second input/output terminals are configured to operate as output terminals and are configured to be connected, in series with a load element (30) and in parallel with the decoupling capacitor;

– the third and fourth input/output terminals are short-circuited;

– one end of the inductor is configured to be connected to the short-circuited third and fourth input/output terminals and another end the inductor is configured to be connected to a common node receiving a supply potential.

4. The output stage of claim 1 further comprising an inductor (212) and a decoupling capacitor (213), wherein, in the second operating state:

– the first and second input/output terminals are configured to operate as input terminals and are configured to be connected to a common node receiving a supply potential;

– the third and fourth input/output terminals are short-circuited;

– one end of the inductor is configured to be connected to the short-circuited third and fourth input/output terminals and another end the inductor is configured to be connected, in series with a load element (30) and in parallel with the decoupling capacitor.

5. The output stage of claim 1 further comprising a first and second inductors (207, 208) and a first and second decoupling capacitors (209, 210), wherein, in the second operating state:

– the first and second input/output terminals are configured to operate as output terminals;

– the first input/output terminal is configured to be connected, in series with a

first load element (30) and in parallel with the first decoupling capacitor;

– the second input/output terminal is configured to be connected, in series with a second load element (40) and in parallel with the second decoupling capacitor;

– one end of the first inductor is configured to be connected to the third input/output terminal and another end of the first inductor is configured to be connected to a common node receiving a supply potential;

– one end of the second inductor is configured to be connected to the fourth input/output terminal and another end of the second inductor is configured to be connected to the common node receiving a supply potential.

6. The output stage of claim 1 further comprising a first and second inductors (215, 217) and a first and second decoupling capacitors (216, 218), wherein, in the second operating state:

– the first and second input/output terminals are configured to operate as input terminals and are configured to be connected to a common node receiving a supply potential;

– one end of the first inductor is configured to be connected to the third input/output terminal and another end of the first inductor is configured to be connected, in series with a first load element (30) and in parallel with the first decoupling capacitor;

– one end of the second inductor is configured to be connected to the fourth input/output terminal and another end of the second inductor is configured to be connected, in series with a second load element (40) and in parallel with the second decoupling capacitor.

7. The output stage of claim 1 further comprising a first and second inductors (220, 223) and a first and second decoupling capacitors (221, 224), wherein, in the second operating state:

– the first and second input/output terminals are configured to operate as input terminals;

– the third input/output terminal is configured to be connected, in series with a first load element (30) and in parallel with the first decoupling capacitor;

– one end of the first inductor is configured to be connected to the first input/output terminal and another end of the first inductor is configured to be

connected to a first node receiving a supply potential;

– one end of the second inductor is configured to be connected to the fourth input/output terminal and another end of the second inductor is configured to be connected, in series with a second load element (40) and in parallel with the second decoupling capacitor.

8. A control apparatus (10) comprising:

   – a control stage configured to control an output stage according to claim 2.

9. The control apparatus of claim 8 wherein the control stage is a Class-D control stage.

10. A control apparatus (20) comprising:

    – a control stage configured to control an output stage according to any one of claims 3 to 7.

11. The control apparatus of claim 10 wherein the control stage is a DC-DC converter control stage.

12. The control apparatus of anyone of claims 8 to 11, wherein the control stage is adapted to control the output stage by generating control signals for controlling the first, second, third and fourth switches through their respective control terminals.

13. A circuit comprising:

    – an output stage according to any one of claims 2 to 7;

    – a first control apparatus according to any one of claims 8 to 9 and 12 wherein the control stage of the first control apparatus is connected to the output stage; and,

    – a second control apparatus according to any one of claims 10 to 11 and 12 wherein the control stage of the second control apparatus is connected to the output stage;

    wherein,

    – when the control stage of the first control apparatus is connected to the output stage, the control stage of the second control apparatus is electrically disconnected from the output stage, the output stage being configured to operate in the first operating state; and,

    – when the control stage of the second control apparatus is connected to the output stage, the control stage of the first control apparatus is electrically

disconnected from the output stage, the output stage being configured to operate in the second operating state.

14. A device comprising:

– the circuit of claim 12;

– a battery configured to be connected to the input terminals of the circuit; and,

– a loudspeaker configured to be connected to the output terminals of the circuit.

15. Use of an output stage according to any one of claims 2 to 7, in conjunction with:

– a first control apparatus according to any one of claims 8 to 9 and 12 wherein the control stage of the first control apparatus is connected to the output stage; and,

– a second control apparatus according to any one of claims 10 to 11 and 12 wherein the control stage of the second control apparatus is connected to the output stage;

wherein,

– when the control stage of the first control apparatus is connected to the output stage, the control stage of the second control apparatus is electrically disconnected from the output stage, the output stage being configured to operate in the first operating state; and,

– when the control stage of the second control apparatus is connected to the output stage, the control stage of the first control apparatus is electrically disconnected from the output stage, the output stage being configured to operate in the second operating state.

Abstract

A circuit comprising:

– an output stage according to the invention;

– a first control apparatus comprising a control stage of the first control apparatus is connected to the output stage; and,

– a second control apparatus comprising a control stage of the second control apparatus is connected to the output stage;

wherein,

– when the control stage of the first control apparatus is connected to the output stage, the control stage of the second control apparatus is electrically disconnected from the output stage, the output stage being configured to operate in a first operating state; and,

– when the control stage of the second control apparatus is connected to the output stage, the control stage of the first control apparatus is electrically disconnected from the output stage, the output stage being configured to operate in a second operating state.

The output stage and the use of the output stage are also claimed.

FIG. 2

Drawings

FIG. 1

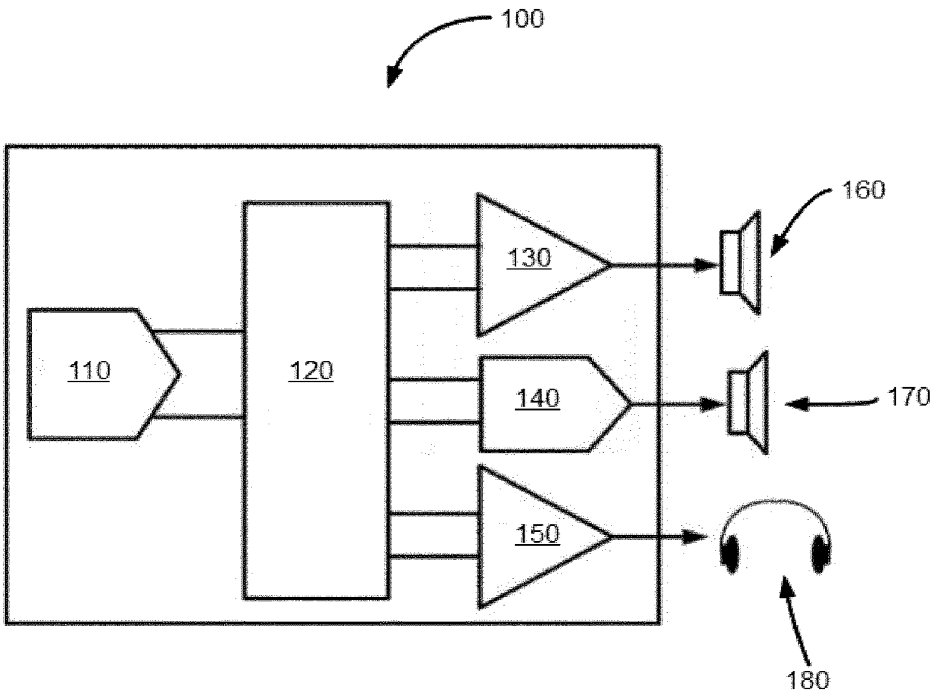


FIG. 2

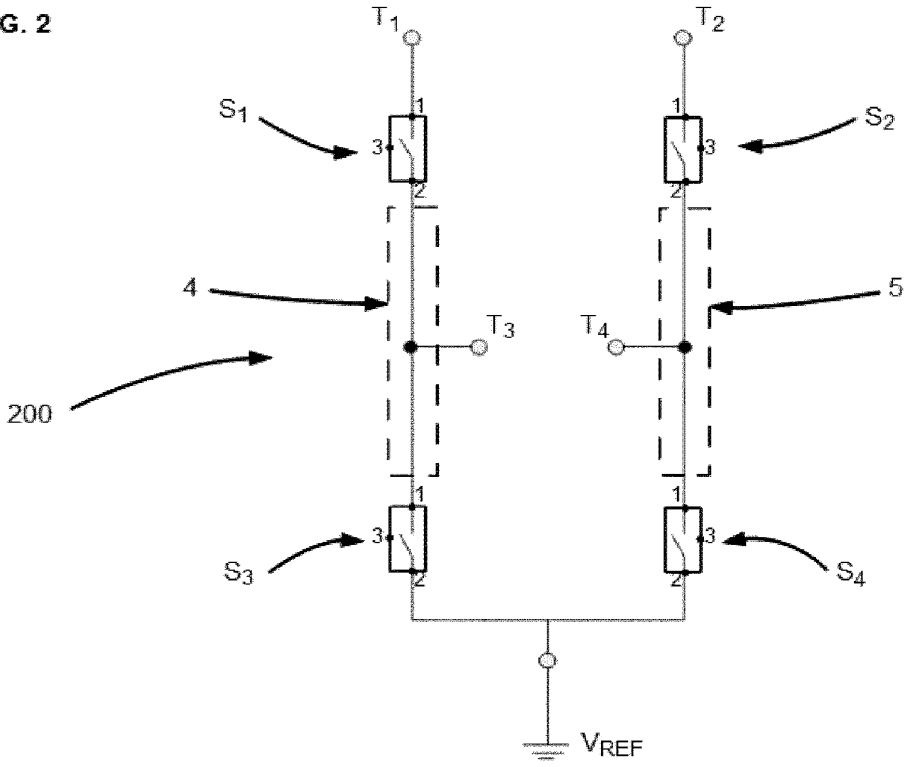
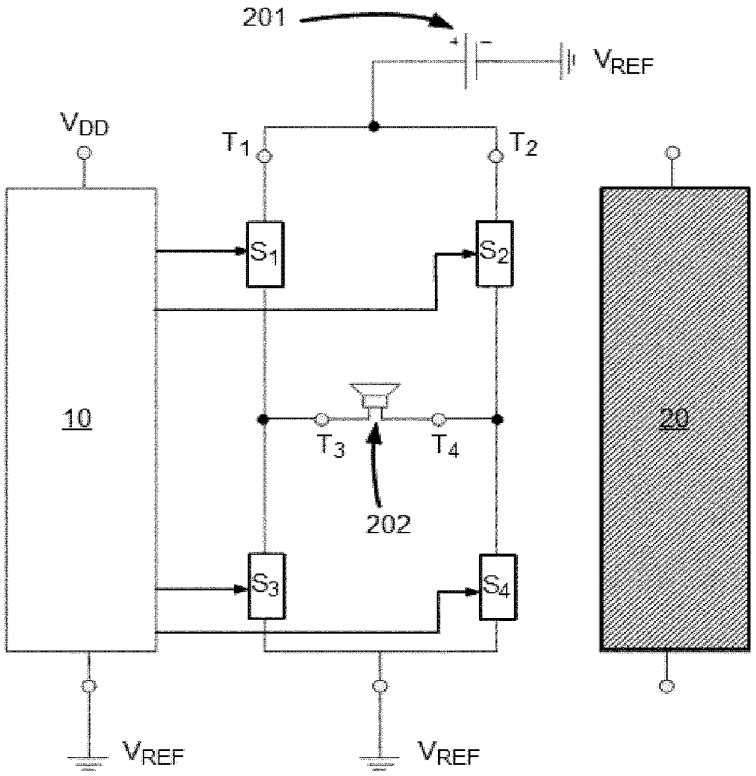


FIG. 3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S2
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T3
T4
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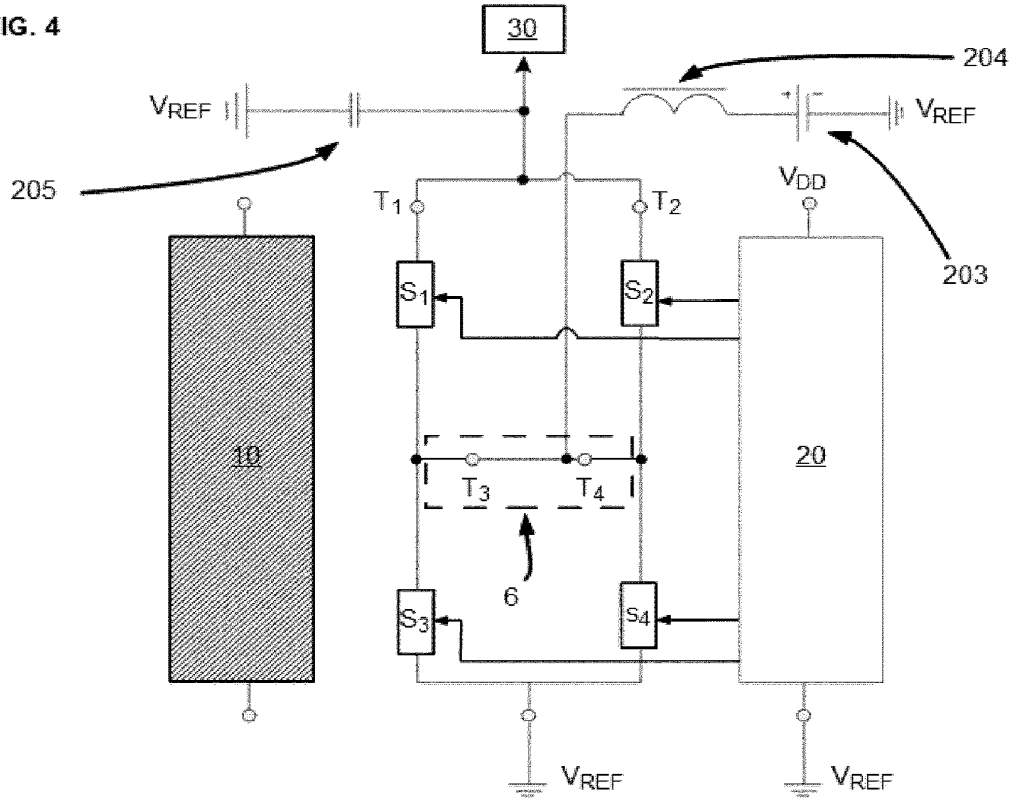
S3
S4
VREF
VREF

FIG. 4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VREF
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S1
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20
T3
T4
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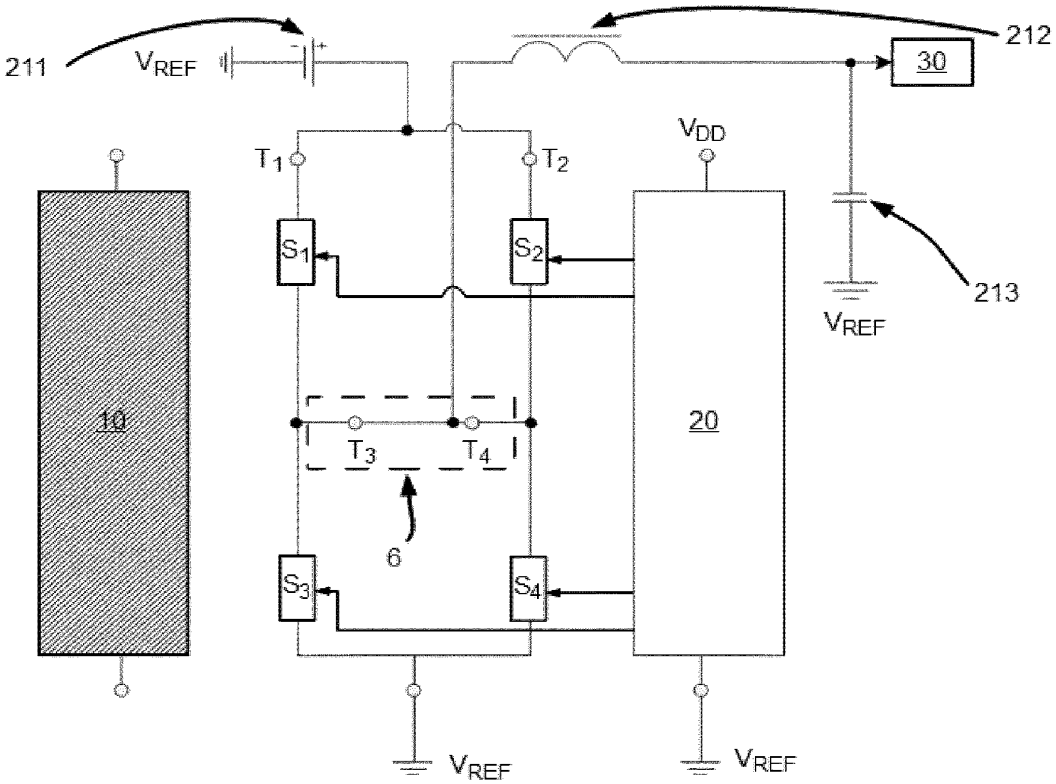
S3
S4
VREF
VREF

FIG. 5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T_4
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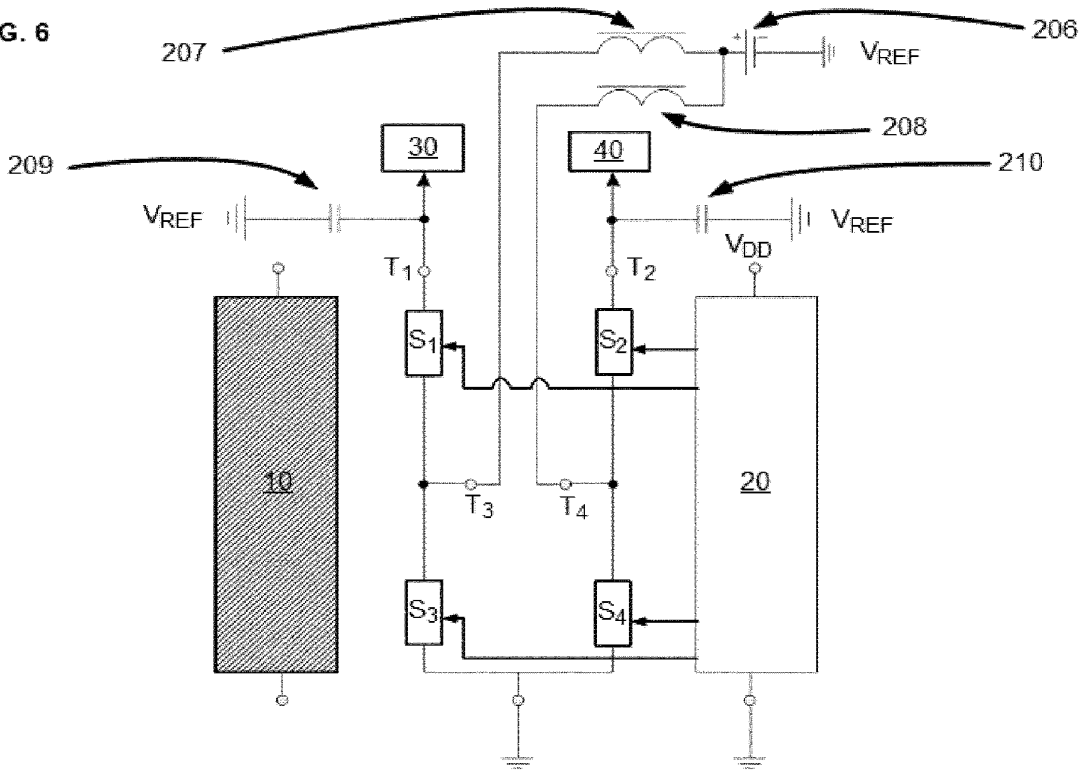
S_4
V_{REF}
V_{REF}

FIG. 6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V_{REF}
V_{DD}
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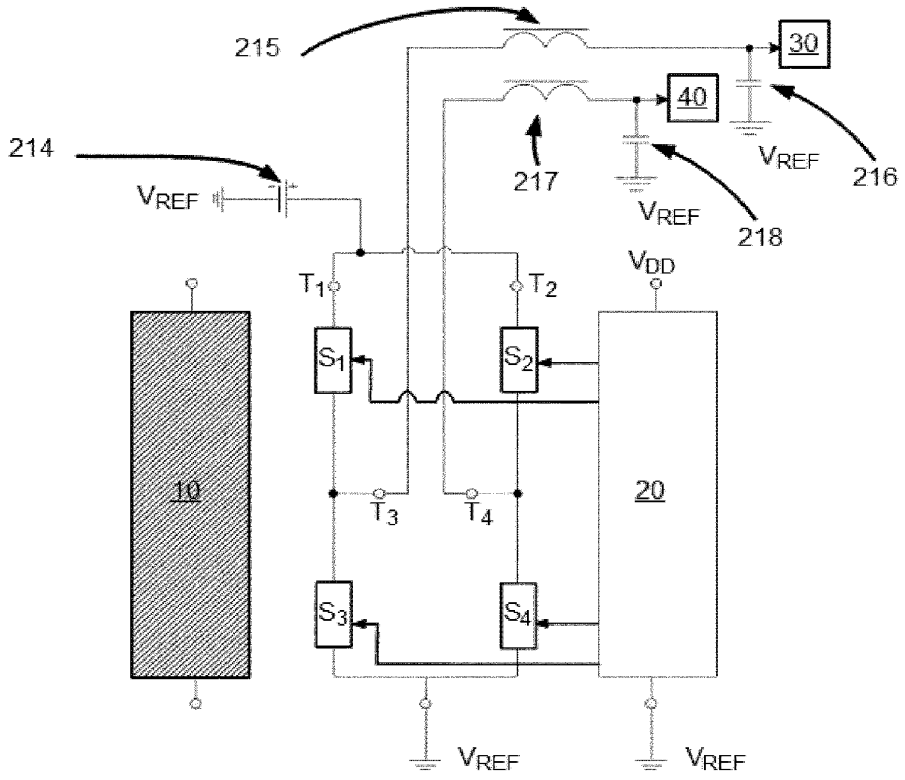
S_3
S_4

FIG. 7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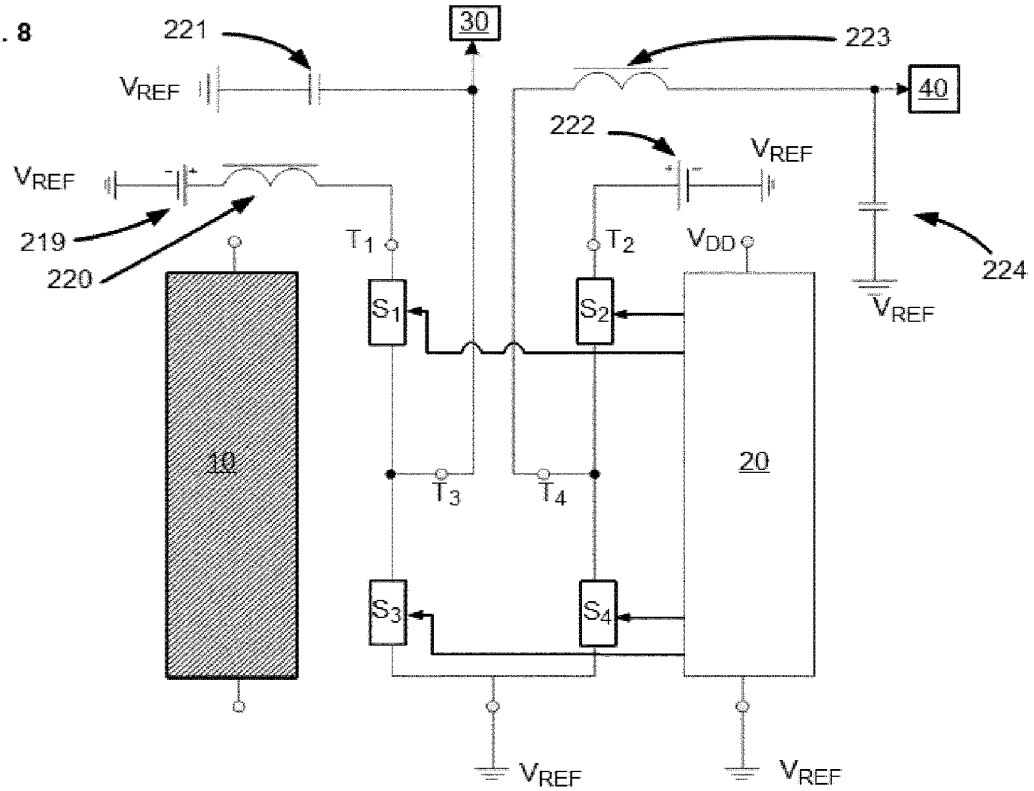
S_4
V_{REF}
V_{REF}

FIG. 8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International filing date:		**02 June 2014 (02.06.2014)**
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0-4-1	Prepared Using	PCT Online Filing Version 3.5.000.235 MT/FOP 20020701/0.20.5.20
0-5	**Petition** The undersigned requests that the present international application be processed according to the Patent Cooperation Treaty	
0-6	**Receiving Office (specified by the applicant)**	European Patent Office (EPO) (RO/EP)
0-7	**Applicant's or agent's file reference**	BCT140220GDE
I	**Title of Invention**	RECONFIGURABLE OUTPUT STAGE
II	**Applicant**	
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IV-1-4	Facsimile No.	00 33 1 42 80 01 59
IV-1-5	e-mail	info@plass.com
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V-1	**The filing of this request constitutes under Rule 4.9(a), the designation of all Contracting States bound by the PCT on the international filing date, for the grant of every kind of protection available and, where applicable, for the grant of both regional and national patents.**	
VI-1	**Priority claim of earlier regional application**	
VI-1-1	Filing date	03 June 2013 (03.06.2013)
VI-1-2	Number	13305740.6
VI-1-3	Regional Office	EP
VI-2	**Priority document request**	
	The receiving Office is requested to prepare and transmit to the International Bureau a certified copy of the earlier application(s) identified above as item(s):	VI-1

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VII-1	**International Searching Authority Chosen**	European Patent Office (EPO) (ISA/EP)	
VII-2	**Request to use results of earlier search; reference to that search**		
VII-2-1	Filing date	06 June 2013 (06.06.2013)	
VII-2-2	Application Number	EP13305740	
VII-2-3	Country (or regional Office)	EP	
VIII	**Declarations**	Number of declarations	
VIII-1	Declaration as to the identity of the inventor	–	
VIII-2	Declaration as to the applicant's entitlement, as at the international filing date, to apply for and be granted a patent	–	
VIII-3	Declaration as to the applicant's entitlement, as at the international filing date, to claim the priority of the earlier application	–	
VIII-4	Declaration of inventorship (only for the purposes of the designation of the United States of America)	–	
VIII-5	Declaration as to non-prejudicial disclosures or exceptions to lack of novelty	–	
IX	**Check list**	Number of sheets	Electronic file(s) attached
IX-1	Request (including declaration sheets)	4	✓
IX-2	Description	18	✓
IX-3	Claims	5	✓
IX-4	Abstract	1	✓
IX-5	Drawings	4	✓
IX-7	TOTAL	32	
	Accompanying Items	Paper document(s) attached	Electronic file(s) attached
IX-8	Fee calculation sheet	–	✓
IX-18	PCT-SAFE physical media	–	–
IX-20	**Figure of the drawings which should accompany the abstract**	2	
IX-21	**Language of filing of the international application**	English	

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X-1-2	Name of signatory	FR, Cabinet Plasseraud, J.-L. Hartmann 28695
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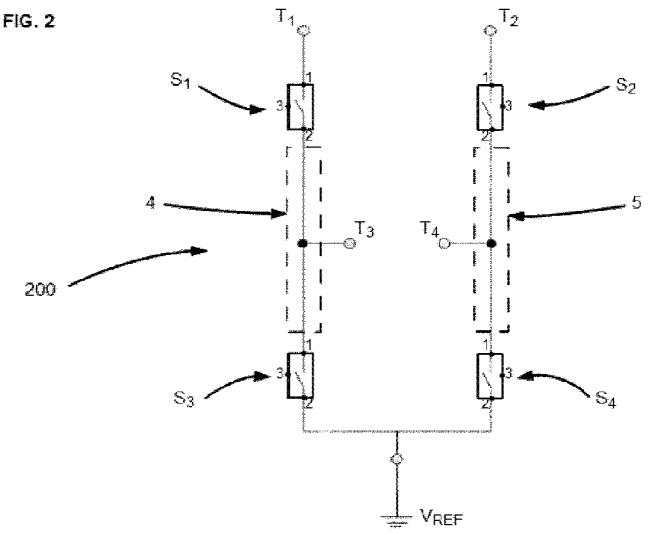
(54) **Title**: RECONFIGURABLE OUTPUT STAGE

FIG. 2



(57) **Abstract**: A circuit comprising: – an output stage according to the invention; – a first control apparatus comprising a control stage of the first control apparatus is connected to the output stage; and, – a second control apparatus comprising a control stage of the second control apparatus is connected to the output stage; wherein, – when the control stage of the first control apparatus is connected to the output stage, the control stage of the second control apparatus is electrically disconnected from the output stage, the output stage being configured to operate in a first operating state; and, – when the control stage of the second control apparatus is connected to the output stage, the control stage of the first control apparatus is electrically disconnected from the output stage, the output stage being configured to operate in a second operating state. The output stage and the use of the output stage are also claimed.

WO 2014/195258 A1

Description

RECONFIGURABLE OUTPUT STAGE

Technical Field

[0001] The proposed solution relates generally to output stage circuits, and more especially to a reconfigurable output stage.

Background Art

[0002] Recently, designers of portable and other low power electronic devices have devised multimedia features in order for their products to attract more attention from potential customers. Internally to these devices, subsystem circuits such as audio subsystems have an increasingly important role on the realisation of these features and, thus, on user experience.

[0003] A typical audio subsystem, for instance, may combine in a single integrated circuit, various audio configurations for driving multiple output speakers such as a headphone, a hands-free loudspeaker and a receiver speaker, each of these audio configurations potentially having respective output power requirements. For instance, an audio subsystem may use a Class-D amplifier in different audio configurations for driving a circuit such as a hands–free loudspeaker. In fact, depending on the user's need and due to its high power and high efficiency, a Class-D amplifier may provide different levels of loudness. For example, when a medium loudness is required, e.g. 1W, the Class-D amplifier may be powered by the battery of the device. In this configuration the sound loudness would depend on the battery charge state. In another example, when a high loudness is required, e.g. 2W, the Class-D amplifier may be powered by a DC-DC boost converter. In this configuration, the sound loudness could be constant whatever the battery charge state.

[0004] However, with such type of audio subsystems, when only the medium loudness audio configuration is used the DC-DC boost converter is not used. This is inefficient and represents extra subsystems costs due to the unused die area.

Summary

[0005] There is thus a need for an improved subsystem circuit structure which maximises the die area usage and thus reduce the subsystem costs.

Therefore, it is proposed an output stage suitable for use in a subsystem circuit which can be shared between at least two subsystem circuit components. Namely, the proposed output stage may be adapted to work with particular subsystem circuit components. Hence, with the above example of the audio subsystem and contrary to the prior art, only one output stage is needed for both the Class-D amplifier and the DC-DC boost converter within an audio subsystem circuit structure. In fact in the prior art, two output stages are needed, i.e. one output stage for each of the Class-D amplifier and the DC-DC boost converter.

[0006] In a first aspect of the solution described herein, there is proposed an electronic circuit output stage adapted to operate in at least a first operating state and a second operating state, the output stage comprising:

– a first, a second, a third and a fourth configurable input/output terminals; and,

– a first, a second, a third and a fourth switches, each having a first main terminal, a second main terminal and a control terminal, the control terminal being adapted to receive a control signal for controlling the open or closed state of the switch;

wherein,

– the first input/output terminal is connected to the first main terminal of the first switch; – the second input/output terminal is connected to the first main terminal of the second switch;

– the second main terminal of the first switch is connected to the first main terminal of the third switch through a first branch,

– the second main terminal of the second switch is connected to the first main terminal of the fourth switch through a second branch;

– the third input/output terminal is connected to the first branch and the fourth input/output terminal is connected to the second branch;

– the second main terminals of the third and fourth switches are both connected to a common node receiving a reference potential; and,

wherein,

– when the first and second input/output terminals are configured to

operate as input terminals, the third and fourth input/output terminals are configured to operate as output terminals; and,

– when the first and second input/output terminals are configured to operate as output terminals, the third and fourth input/output terminals are configured to operate as input terminals; and,

wherein,

– in the first operating state, the output stage is arranged in a first electrical configuration; and

– in the second operating state wherein the output stage is arranged in a second electrical configuration different from the first configuration

[0007] In a first embodiment of the first aspect, in the first operating state:

– the first and second input/output terminals are configured to operate as input terminals and are configured to be connected to a common node receiving a supply potential; and,

– the third and fourth input/output terminals are configured to be connected to a load element.

[0008] Advantageously, this embodiment may allow creating a class-D configuration.

[0009] In a second embodiment of the first aspect, in the second operating state, the output stage may further comprise an inductor and a decoupling capacitor, wherein:

– the first and second input/output terminals are configured to operate as output terminals and are configured to be connected, in series with a load element and in parallel with the decoupling capacitor;

–the third and fourth input/output terminals are short-circuited ;

– one end of the inductor is configured to be connected to the short circuited third and fourth input/output terminals and another end the inductor is configured to be connected to a node receiving a supply potential.

[0010] Advantageously, this embodiment may allow creating a boost DCDC configuration.

[0011] In a third, alternative embodiment of the first aspect, in the second operating state, the output stage may further comprise an inductor and a

decoupling capacitor, wherein:

– the first and second input/output terminals are configured to operate as input terminals and are configured to be connected to a common node receiving a supply potential;

–the third and fourth input/output terminals are short-circuited;

– one end of the inductor is configured to be connected to the short-circuited third and fourth input/output terminals and another end the inductor is configured to be connected, in series with a load element and in parallel with the decoupling capacitor.

[0012] Advantageously, this embodiment may allow creating a buck DCDC configuration.

[0013] In a fourth possible embodiment of the first aspect, in the second operating state, the output stage may further comprise a first and second inductor and a first and second decoupling capacitor, wherein:

– the first and second input/output terminals are configured to operate as output terminals;

– the first input/output terminal is configured to be connected, in series with a first load element and in parallel with the first decoupling capacitor;

– the second input/output terminal is configured to be connected, in series with a second load element and in parallel with the second decoupling capacitor;

– one end of the first inductor is configured to be connected to the third input/output terminal and another end of the first inductor is configured to be connected to a common node receiving a supply potential;

– one end of the second inductor is configured to be connected to the fourth input/output terminal and another end of the second inductor is configured to be connected to the node receiving a supply potential.

[0014] Advantageously, this embodiment may allow creating a double boost DCDC.

[0015] In a fifth embodiment of the first aspect, in the second operating state, the output stage may further comprise a first and second inductor and a first and second decoupling capacitor, wherein:

– the first and second input/output terminals are configured to operate as

input terminals and are configured to be connected to a common node receiving a supply potential;

– one end of the first inductor is configured to be connected to the third input/output terminal and another end of the first inductor is configured to be connected, in series with a first load element and in parallel with the first decoupling capacitor;

– one end of the second inductor is configured to be connected to the fourth input/output terminal and another end of the second inductor is configured to be connected, in series with a second load element and in parallel with the second decoupling capacitor.

[0016] Advantageously, this embodiment may allow creating a double buck DCDC.

[0017] For instance, in a sixth embodiment of the first aspect, in the second operating state, the output stage may further comprise a first and second inductor and a first and second decoupling capacitor, wherein:

– the first and second input/output terminals are configured to operate as input terminals;

– the third input/output terminal is configured to be connected, in series with a first load element and in parallel with the first decoupling capacitor;

– one end of the first inductor is configured to be connected to the first input/output terminal and another end of the first inductor is configured to be connected to a first node receiving a supply potential;

– one end of the second inductor is configured to be connected to the fourth input/output terminal and another end of the second inductor is configured to be connected, in series with a second load element and in parallel with the second decoupling capacitor.

[0018] Advantageously, this embodiment may allow creating a double DCDC, comprising a buck configuration, and a boost configuration.

[0019] In a second aspect of the solution, there is proposed a control apparatus comprising:

– a control stage configured to control an output stage according to the first embodiment of the first aspect.

[0020] In an embodiment of the second aspect, the control stage is a Class-D control stage.

[0021] In a third aspect of the solution, there is proposed a control apparatus comprising:

– a control stage configured to control an output stage according to any one of the second to sixth embodiments of the first aspect.

[0022] In an embodiment of the third aspect, the control stage is a DC-DC converter control stage.

[0023] In an embodiment of second and/or third aspects, the control stage is adapted to control the output stage by generating control signals for controlling the first, second, third and fourth switches through their respective control terminals.

[0024] In a fourth aspect of the solution, there is proposed a circuit comprising:

– an output stage according to any one of the first to the sixth embodiments of the first aspect;

– a first control apparatus according to the second aspect wherein the control stage of the first control apparatus is connected to the output stage; and,

– a second control apparatus according to the third aspect wherein the control stage of the second control apparatus is connected to the output stage, wherein:

– when the control stage of the first control apparatus is connected to the output stage, the control stage of the second control apparatus is electrically disconnected from the output stage, the output stage being configured to operate in the first operating state; and,

– when the control stage of the second control apparatus is connected to the output stage, the control stage of the first control apparatus is electrically disconnected from the output stage, the output stage being configured to operate in the second operating state.

[0025] In a fifth aspect of the solution, there is proposed a device comprising:

– the circuit of the fourth aspect;

– a battery configured to be connected to the input terminals of the circuit; and,

– a loudspeaker configured to be connected to the output terminals of the circuit.

[0026] In a sixth aspect of the solution, there is proposed the use of an output stage according to any one of the first to the sixth embodiments of the first aspect in conjunction with:

– a first control apparatus according to the second aspect wherein the control stage of the first control apparatus is connected to the output stage; and,

– a second control apparatus according to the third aspect wherein the control stage of the second control apparatus is connected to the output stage, wherein:

– when the control stage of the first control apparatus is connected to the output stage, the control stage of the second control apparatus is electrically disconnected from the output stage, the output stage being configured to operate in the first operating state; and,

– when the control stage of the second control apparatus is connected to the output stage, the control stage of the first control apparatus is electrically disconnected from the output stage, the output stage being configured to operate in the second operating state.

Brief description of drawings

[0027] A more complete understanding of the proposed solution may be obtained from a consideration of the following description in conjunction with the drawings, in which like reference numbers indicate same or similar elements. In the drawings:

[0028] FIG. 1 is a block diagram illustrating an audio subsystem;

[0029] FIG. 2 is a block diagram illustrating an exemplary output stage of the proposed solution;

[0030] FIGs. 3-8 are a block diagrams illustrating embodiments of the proposed solution.

Description of embodiments

[0031] The following detailed description is exemplary in nature and is not intended to limit the scope, applicability, or configuration of the invention in any way. Rather, the following description provides practical illustrations

for implementing exemplary embodiments of the present invention. Examples of constructions, materials, dimensions, and manufacturing processes are provided for selected elements, and all other elements employ that which is known to those of skill in the field of the invention. Those skilled in the art will recognize that many of the examples provided have suitable alternatives that can be utilized.

[0032] FIG. 1 is a block diagram schematically illustrating an audio subsystem 100.

[0033] In FIG. 1, there is shown therein the audio subsystem 100 comprising one audio DAC unit 110 (i.e. Digital to Analog Converter), one gain matrix unit 120, one class-AB amplifiers 130 , two class-AB amplifiers 150, one Class-D amplifier 140, one ear speaker 160, one hands-free speaker 170 and one headphone 180. It is considered herein that there are two class-AB amplifiers 150 that can drive a stereo headphone.

[0034] Referring to FIG. 1, the audio DAC 110 is coupled to the gain matrix 120, which is coupled to the amplifiers 130, 140, 150, which are respectively coupled to the ear speaker 160, the hands-free speaker 170 and the headphone 180.

[0035] The DAC 110 aims at generating at least one audio signal which gain may be modified by the gain matrix 120 prior being amplified by an amplifier 130, 140, 150 and being reproduced by a speaker 160, 170, 180.

[0036] As stated above, the Class-D amplifier 140 may be used in different audio configurations depending on the user's need of loudness. However, different circuit components may be used in different audio configurations thus resulting in a waste of circuit die area when only one or more of the circuit components are in used while the others are not.

[0037] By way of example, let's consider a case where the Class-D amplifier 140 and a DC-DC boost converter are the circuit components used in one or more audio configurations to drive a speaker, 170. It is indicated that other configurations and other components may be used herein. Each of the Class-D amplifier 140 and the DC-DC boost converter is usually organised into two parts:

- a output stage providing the required output; and,

- a control stage for controlling the output stage .

However in the proposed example, when the Class-D is used alone in the audio configuration (e.g. for a medium output loudness), only the control stage and output stage of the Class-D amplifier are used while the control stage and output stage of the DC-DC boost converter are not used. As stated above, this situation results in wastage of the circuit die area.

[0038] In order to solve this problem, it is proposed an electronic circuit output stage adapted to operate in at least a first operating state and a second operating state, such that the output stage may be shared by at least two circuit components such as the Class-D amplifier and the DC-DC boost converter. This way in the example proposed above, the proposed control stage would always be in used in all associated audio configurations.

[0039] FIG. 2 is a block diagram schematically illustrating an exemplary output stage 200 according to the proposed solution.

[0040] In FIG. 2, there is shown therein the output stage 200 comprising:

– a first configurable input/output terminal T_1, a second configurable input/output terminal T_2, a third configurable input/output terminal T_3 and a fourth configurable input/output terminal T_4; and,

– a first switch S_1, a second switch S_2, a third switch S_3 and a fourth switch S_4. The switches S1, S2, S3, S4 may be MOS transistors, NMOS transistors or other transistors of the same or different kind.

[0041] Referring to FIG. 2, the configurable input/output terminal T_1, T_2, T_3, T_4 are configured to operate as input or output terminals such that:

– when the first input/output terminal T1 and second input/output terminal T2 are configured to operate as input terminals, the third input/output terminal T3 and fourth input/output terminal T4 are configured to operate as output terminals; and,

– when the first input/output terminal T1 and second input/output terminal T2 are configured to operate as output terminals, the third input/output terminal T3 and fourth input/output terminal T4 are configured to operate as input terminals.

[0042] Further in FIG. 2, each of the switches S_1, S_2, S_3, S_4 has a first main terminal 1, a second main terminal 2 and a control terminal 3 wherein the

control terminal 3 is adapted to receive a control signal for controlling the open or closed state of the associated switch.

[0043] Structurally, the output stage 200 is organised as follows. The first input/output terminal T1 is connected to the first main terminal 1 of the first switch S1. The second input/output terminal T2 is connected to the first main terminal 1 of the second switch S2. The second main terminal 2 of the first switch S1 is connected to the first main terminal 1 of the third switch S3. The latter connection is forming a first branch 4 of the output stage 200. The second main terminal 2 of the second switch S2 is connected to the first main terminal 1 of the fourth switch s4. The latter connection is forming a second branch 5 of the output stage 200. The third input/output terminal T3 is connected to the first branch 4 of the output stage 200 and the fourth input/output terminal T4 is connected to the second branch 5 of the output stage 200. The second main terminal 2 of the third switch S3 and the second main terminal 2 of fourth switches S4 are both connected to a common node receiving a reference potential VREF of the output stage 200.

[0044] Referring to FIG. 2, when in the first operating state, the output stage is arranged in a first electrical configuration, and when in the second operating state wherein the output stage is arranged in a second electrical configuration different from the first configuration.

[0045] FIG. 3 is a block diagram schematically illustrating a first exemplary embodiment of the proposed solution wherein the output stage 200 of FIG.2 is used, in the first operating state.

[0046] In the example of FIG. 3, the first input/output terminal T1 and second input/output terminal T2 are configured to operate as input terminals and are also configured to be connected to a common node receiving a supply potential 201. The common node receiving a supply potential 201 may be a battery, a DC-DC boost converter or any similar DC power source which needs to be recharged on a periodic basis. Further, in FIG. 3, the third input/output terminal T3 and fourth input/output terminal T4 are configured to be connected to a load element. For example, the load element may be an audio speaker 202. In such case, the third input/output terminal T3 and

fourth input/output terminal T4 may be connected respectively with a first and second end of the audio speaker 202. In another example, the load element may be a motor such as a vibration motor usually used in mobile phone. It is indicated that other components may be used herein. As can be seen, the structure of the output stage 200 in the example of FIG. 3 is an H-bridge circuit structure, thus the output stage 200 may be controlled by an H-bridge control stage 10. Namely, the switches S1, S2, S3, S4 of the output stage 200 may be controlled by the H-bridge control stage 10. In the case of audio subsystems, the H-bridge control stage 10 may be the control stage of a Class-D amplifier. If it is the case, the combination of a Class-D amplifier control stage and the output stage 200 of the FIG. 3 would correspond to the realisation of a Class-D amplifier.

[0047] FIG. 4 is a block diagram schematically illustrating a second exemplary embodiment of the proposed solution wherein the output stage 200 of FIG.2 is used, in the second operating state.

[0048] In the example of FIG. 4, the output stage 200 may further comprise one inductor 204 and one decoupling capacitor 205. Further, in FIG. 4, the first input/output terminal T1 and second input/output terminal T2 are configured to operate as output terminals and are also configured to be connected, in series with a load element 30 and, in parallel with the decoupling capacitor 205. In this configuration, the decoupling capacitor 205 is used for removing on-chip high frequency noise. Also, in FIG. 4, the third input/output terminal T3 and fourth input/output terminal T4 are short-circuited 6. Additionally, in FIG. 4, one end of the inductor 204 is configured to be connected to the short-circuit 6 and another end the inductor 204 is configured to be connected to a common node receiving a supply potential 203 similar to those already presented in FIG. 3. As can be seen, the structure of the output stage 200 in the example of FIG. 4 is not an H-bridge circuit structure since the load element is not on the central branch of the structure. Rather, the structure of the output stage 200 in the example of FIG. 4 may be seen as two branches 4, 5 which are arranged in parallel. Therefore, any control stage 20 that may control such structure may be used. In one embodiment, the control stage 20 may use

the same signal to control two switches S1, S2, S3, S4 which are situated on parallel branches of the output stage 200 of the FIG. 4. In this case, the output stage 200 would be similar to a circuit structure comprising only a single branch. In this case, a DC-DC control stage may be used to control the output stage 200 in the example of FIG. 4. If it is the case, the combination of a DC-DC control stage and the output stage 200 of the FIG. 4 would correspond to the realisation of a DC-DC boost converter configured to, at least, step-up an input voltage.

[0049] FIG. 5 is a block diagram schematically illustrating a third exemplary embodiment of the proposed solution wherein the output stage 200 of FIG.2 is used, in the second operating state.

[0050] In the example of FIG. 5, the output stage 200 may further comprise one inductor 212 and one decoupling capacitor 213 similar to those already presented in FIG 4. Further, in FIG. 5, the first input/output terminal T1 and second input/output terminal T2 are configured to operate as input terminals and are also configured to be connected to a common node receiving a supply potential 203 similar to those already presented in FIG. 3. Also, in FIG. 5, a short circuit 6 is created between the third input/output terminal T3 and fourth input/output terminal T4. Additionally, in FIG. 5, one end of the inductor 212 is configured to be connected to the short circuit 6 and another end the inductor 212 is configured to be connected, in series with a load element 30 and, in parallel with the decoupling capacitor 213. As can be seen, the structure of the output stage 200 in the example of FIG. 4 is not an H-bridge circuit structure since the load element 30 is not directed connected to the central branch of the structure. Rather, the structure of the output stage 200 in the example of FIG. 5 may be seen as having, mutatis mutandis, the same structure presented in FIG. 4. Thus, in one embodiment, the control stage 20 may be a DC-DC control stage which may be used to control the output stage 200 in the example of FIG. 5. If it is the case, the combination of a DC-DC control stage and the output stage 200 of the FIG. 5 would correspond to the realisation of a DC-DC buck converter configured to, at least, step-down an input voltage.

[0051] FIG. 6 is a block diagram schematically illustrating a fourth exemplary embodiment of the proposed solution wherein the output stage 200 of FIG.2 is used, in the second operating state.

[0052] In the example of FIG. 6, the output stage 200 may further comprise one first inductor 207, one second inductor 208, one first decoupling capacitor 209 and one second decoupling capacitor 210. Further, in FIG. 6, the first input/output terminal T1 and second input/output terminal T2 are configured to operate as output terminals. The first input/output terminal T1 is further configured to be connected, in series with a first load element 30 and in parallel with the first decoupling capacitor 209. The second input/output terminal T2 is further configured to be connected, in series with a second load element 40 and in parallel with the second decoupling capacitor 210. Also, one end of the first inductor 207 is configured to be connected to the third input/output terminal T3 and another end of the first inductor 207 is configured to be connected to a common node receiving a supply potential 206 similar to those already presented in FIG. 3. Additionally, one end of the second inductor 208 is configured to be connected to the fourth input/output terminal T4 and another end of the second inductor 208 is configured to be connected to the above-mentioned common node receiving a supply potential 206. As can be seen, the structure of the output stage 200 in the example of FIG. 6 is not an H-bridge circuit structure since the load elements 30, 40 are not directed connected to the central branch of the structure. Rather, the structure of the output stage 200 in the example of FIG. 6 may be seen as having, mutatis mutandis, the same structure presented in FIG. 4. Thus, in one embodiment, the control stage 20 may be a DC-DC control stage which may be used to control the output stage 200 in the example of FIG. 6. If it is the case, the combination of a DC-DC control stage and the output stage 200 of the FIG. 6 would correspond to the realisation of a double DC-DC boost converter configured to, at least, step-up an input voltage. Also, due to the fact that each branch of the structure may be controlled independently by the control stage 20, using a DC-DC control stage enables to generate different voltage on each branch 4,5 of the

output stage that may be used to supply in voltage the load elements 30, 40.

[0053] FIG. 7 is a block diagram schematically illustrating a fifth exemplary embodiment of the proposed solution wherein the output stage 200 of FIG.2 is used, in the second operating state.

[0054] In the example of FIG. 7, the output stage 200 may further comprise one first inductor 215, one second inductor 217, one first decoupling capacitor 216 and one second decoupling capacitor 218. Further, in FIG. 7, the first input/output terminal T1 and second input/output terminal T2 are configured to operate as input terminals and are configured to be connected to a common node receiving a supply potential 214 similar to those already presented in FIG. 3. Also, one end of the first inductor 215 is configured to be connected to the third input/output terminal T3 and another end of the first inductor 215 is configured to be connected, in series with a first load element 30 and in parallel with the first decoupling capacitor 216. Additionally, one end of the second inductor 217 is configured to be connected to the fourth input/output terminal T4 and another end of the second inductor 217 is configured to be connected, in series with a second load element 40 and in parallel with the second decoupling capacitor 218. As can be seen, the structure of the output stage 200 in the example of FIG. 7 is not an H-bridge circuit structure since the load elements 30, 40 are not directed connected to the central branch of the structure. Rather, the structure of the output stage 200 in the example of FIG. 7 may be seen as having, mutatis mutandis, the same structure presented in FIG. 4. Thus, in one embodiment, the control stage 20 may be a DC-DC control stage which may be used to control the output stage 200 in the example of FIG. 7. If it is the case, the combination of a DC-DC control stage and the output stage 200 of the FIG. 7 would correspond to the realisation of a double DC-DC buck converter configured to, at least, step-down an input voltage. Also, due to the fact that each branch of the structure may be controlled independently by the control stage 20, using a DC-DC control stage enables to generate

different voltage on each branch 4,5 of the output stage that may be used to supply in voltage the load elements 30, 40.

[0055] FIG. 8 is a block diagram schematically illustrating a sixth exemplary embodiment of the proposed solution wherein the output stage 200 of FIG.2 is used, in the second operating state. Actually, the example of FIG.8 may correspond to a mix between the circuit structures of the examples of FIGs. 6-7.

[0056] Namely, in the example of FIG. 8, the output stage 200 may further comprise one first inductor 220, one second inductor 223, one first decoupling capacitor 221 and one second decoupling capacitor 224. Further, in FIG. 8, the first input/output terminal T1 and second input/output terminal T2 are configured to operate as input terminals. The third input/output terminal T3 is configured to be connected, in series with a first load element 30 and in parallel with the first decoupling capacitor 221. Also, one end of the first inductor 220 is configured to be connected to the first input/output terminal T1 and another end of the first inductor 220 is configured to be connected to a first node receiving a supply potential 219 similar to those already presented in FIG. 3. Additionally, one end of the second inductor 223 is configured to be connected to the fourth input/output terminal T4 and another end of the second inductor 223 is configured to be connected, in series with a second load element 40 and in parallel with the second decoupling capacitor 224. As can be seen, the structure of the output stage 200 in the example of FIG. 8 is not an H-bridge circuit structure al already explained above. Rather, the structure of the output stage 200 in the example of FIG. 6 may be seen as having, mutatis mutandis, the same structure presented in FIGs. 6-7. Thus, in one embodiment, the control stage 20 may be a DC-DC control stage which may be used to control the output stage 200 in the example of FIG. 6. If it is the case, the combination of a DC-DC control stage and the output stage 200 of the FIG. 6 would correspond to the realisation of a DC-DC buck-boost converter configured to, at least, step-up an input voltage in the first branch 4 of the output stage 200 and step-down an input voltage in the second branch 5 of the output stage 200. This is mainly due to the

fact that each branch of the structure may be controlled independently by the control stage 20, using a DC-DC control stage enables to generate different voltage on each branch 4,5 of the output stage that may be used to supply in voltage the load elements 30, 40.

[0057] In one embodiment, the switches S1, S2, S3, S4 may be controlled trough their respective control terminals based on control signals such a PWM signal which may be generated by a control stage 10, 20.

[0058] Several apparatuses such as control apparatuses may be realized based on the proposed solution. For example, a first control apparatus may comprise a control stage configured to control an output stage according to example of FIG. 3. In another example, a second control apparatus may comprise a control stage configured to control an output stage according to at least one of the examples of FIGs. 4-8.

[0059] Several uses and circuits may also be realized based on the proposed solution. In an example, a first circuit may comprise:

– an output stage according to at least one of the examples of FIGs. 3-8;

– the first control apparatus wherein the control stage of the first control apparatus is connected to the output stage; and,

– the second control apparatus wherein the control stage of the second control apparatus is connected to the output stage;

wherein,

– when the control stage of the first control apparatus is connected to the output stage, the control stage of the second control apparatus is electrically disconnected from the output stage, the output stage being configured to operate in the first operating state; and,

– when the control stage of the second control apparatus is connected to the output stage, the control stage of the first control apparatus is electrically disconnected from the output stage, the output stage being configured to operate in the second operating state.

[0060] In an example, such circuit may be used to drive a stereo hands free speaker. In that case, the first control apparatus may be a class-D controller and the second control apparatus may be a DC-DC controller.

This way, in a first operating state of the output stage, the circuit may be configured to behave as a class-D amplifier according for instance to FIG.3 wherein the load would be the stereo hands free speaker. In this case, the second control apparatus may be deactivated. In a second operating state of the output stage, the circuit may be configured to behave as a DC-DC converter. According to FIG.4, for instance, the circuit may be a DC-DC boost converter where the load 30 would be the stereo hands free speaker. According to FIG.5, for instance, the circuit may be a DC-DC buck converter where the load 30 would be the stereo hands free speaker. According to FIG.6, for instance, the circuit may be a double DC-DC boost converter where the loads 30, 40 may be different terminals of the stereo hands free speaker. According to FIG.7, for instance, the circuit may be a double DC-DC buck converter where the loads 30, 40 may be different terminals of the stereo hands free speaker. Finally, according to FIG.8, for instance, the circuit may be a DC-DC buck-boost converter able to drive different loads 30, 40 for voltage step-up or step-down wherein at least one may be the stereo hands free speaker.

[0061] Several devices, such as portable devices, may also be realized based on the proposed solution. For example, a device may comprise:

– the first circuit;

– a battery configured to be connected to the input terminals of the circuit; and,

– a loudspeaker configured to be connected to the output terminals of the circuit.

[0062] Although the proposed solution is described above in terms of various exemplary embodiments and implementations, it should be understood that the various features, aspects and functionality described in one or more of the individual embodiments are not limited in their applicability to the particular embodiment with which they are described, but instead may be applied, alone or in various combinations, to one or more of the other embodiments of the proposed solution, whether or not such embodiments are described and whether or not such features are presented as being a part of a described embodiment. Thus, the breadth and scope of the

present proposed solution should not be limited by any of the above-described exemplary embodiments. For instance, it is to appreciated that the output and the circuit may be used in other industries different from the audio that has been presented throughout the description. For example, the DC-DC feature of the circuit may be used in motor-based applications.

[0063] Terms and phrases used in this document, and variations thereof, unless otherwise expressly stated, should be construed as open ended as opposed to limiting. As examples of the foregoing: the term "including" should be read as meaning "including, without limitation" or the like; the term "example" is used to provide exemplary instances of the item in discussion, not an exhaustive or limiting list thereof; the terms "a" or "an" should be read as meaning "at least one," "one or more" or the like; and adjectives such as "conventional," "traditional," "normal," "standard," "known" and terms of similar meaning should not be construed as limiting the item described to a given time period or to an item available as of a given time, but instead should be read to encompass conventional, traditional, normal, or standard technologies that may be available or known now or at any time in the future. Likewise, where this document refers to technologies that would be apparent or known to one of ordinary skill in the art, such technologies encompass those apparent or known to the skilled artisan now or at any time in the future.

[0064] The presence of broadening words and phrases such as "one or more, least," "but not limited to" or other like phrases in some instances shall not be read to mean that the narrower case is intended or required in instances where such broadening phrases may be absent. Additionally, the various embodiments set forth herein are described in terms of exemplary block diagrams, flow charts and other illustrations. As will become apparent to one of ordinary skill in the art after reading this document, the illustrated embodiments and their various alternatives may be implemented without confinement to the illustrated examples. These illustrations and their accompanying description should not be construed as mandating a particular architecture or configuration.

Claims

1. An output stage adapted to operate in at least a first operating state and a second operating state, the output stage comprising:

– a first, a second, a third and a fourth configurable input/output terminals (T1, T2, T3, T4); and,

– a first, a second, a third and a fourth switches (S1, S2, S3, S4), each having a first main terminal (1), a second main terminal (2) and a control terminal (3), the control terminal being adapted to receive a control signal for controlling the open or closed state of the switch;

wherein,

– the first input/output terminal is connected to the first main terminal of the first switch;

– the second input/output terminal is connected to the first main terminal of the second switch;

– the second main terminal of the first switch is connected to the first main terminal of the third switch through a first branch,

– the second main terminal of the second switch is connected to the first main terminal of the fourth switch through a second branch;

– the third input/output terminal is connected to the first branch and the fourth input/output terminal is connected to the second branch;

– the second main terminals of the third and fourth switches are both connected to a common node receiving a reference potential; and,

wherein,

– when the first and second input/output terminals are configured to operate as input terminals, the third and fourth input/output terminals are configured to operate as output terminals; and,

– when the first and second input/output terminals are configured to operate as output terminals, the third and fourth input/output terminals are configured to operate as input terminals; and,

wherein,

– in the first operating state, the output stage is arranged in a first electrical configuration; and

– in the second operating state wherein the output stage is arranged in a second electrical configuration different from the first configuration..

2. The output stage of claim 1, wherein, in the first operating state:
– the first and second input/output terminals are configured to operate as input terminals and are configured to be connected to a common node receiving a supply potential; and,
– the third and fourth input/output terminals are configured to be connected to a load element (202).
3. The output stage of claim 1 further comprising an inductor (204) and a decoupling capacitor (205), wherein, in the second operating state:
– the first and second input/output terminals are configured to operate as output terminals and are configured to be connected, in series with a load element (30) and in parallel with the decoupling capacitor;
– the third and fourth input/output terminals are short-circuited;
– one end of the inductor is configured to be connected to the short-circuited third and fourth input/output terminals and another end the inductor is configured to be connected to a common node receiving a supply potential.
4. The output stage of claim 1 further comprising an inductor (212) and a decoupling capacitor (213), wherein, in the second operating state:
– the first and second input/output terminals are configured to operate as input terminals and are configured to be connected to a common node receiving a supply potential;
– the third and fourth input/output terminals are short-circuited;
– one end of the inductor is configured to be connected to the short-circuited third and fourth input/output terminals and another end the inductor is configured to be connected, in series with a load element (30) and in parallel with the decoupling capacitor.
5. The output stage of claim 1 further comprising a first and second inductors (207, 208) and a first and second decoupling capacitors (209, 210), wherein, in the second operating state:
– the first and second input/output terminals are configured to operate as output terminals;
– the first input/output terminal is configured to be connected, in series with a

first load element (30) and in parallel with the first decoupling capacitor;

– the second input/output terminal is configured to be connected, in series with a second load element (40) and in parallel with the second decoupling capacitor;

– one end of the first inductor is configured to be connected to the third input/output terminal and another end of the first inductor is configured to be connected to a common node receiving a supply potential;

– one end of the second inductor is configured to be connected to the fourth input/output terminal and another end of the second inductor is configured to be connected to the common node receiving a supply potential.

6. The output stage of claim 1 further comprising a first and second inductors (215, 217) and a first and second decoupling capacitors (216, 218), wherein, in the second operating state:

– the first and second input/output terminals are configured to operate as input terminals and are configured to be connected to a common node receiving a supply potential;

– one end of the first inductor is configured to be connected to the third input/output terminal and another end of the first inductor is configured to be connected, in series with a first load element (30) and in parallel with the first decoupling capacitor;

– one end of the second inductor is configured to be connected to the fourth input/output terminal and another end of the second inductor is configured to be connected, in series with a second load element (40) and in parallel with the second decoupling capacitor.

7. The output stage of claim 1 further comprising a first and second inductors (220, 223) and a first and second decoupling capacitors (221, 224), wherein, in the second operating state:

– the first and second input/output terminals are configured to operate as input terminals;

– the third input/output terminal is configured to be connected, in series with a first load element (30) and in parallel with the first decoupling capacitor;

– one end of the first inductor is configured to be connected to the first input/output terminal and another end of the first inductor is configured to be

connected to a first node receiving a supply potential;

– one end of the second inductor is configured to be connected to the fourth input/output terminal and another end of the second inductor is configured to be connected, in series with a second load element (40) and in parallel with the second decoupling capacitor.

8. A control apparatus (10) comprising:

– a control stage configured to control an output stage according to claim 2.

9. The control apparatus of claim 8 wherein the control stage is a Class-D control stage.

10. A control apparatus (20) comprising:

– a control stage configured to control an output stage according to any one of claims 3 to 7.

11. The control apparatus of claim 10 wherein the control stage is a DC-DC converter control stage.

12. The control apparatus of anyone of claims 8 to 11, wherein the control stage is adapted to control the output stage by generating control signals for controlling the first, second, third and fourth switches through their respective control terminals.

13. A circuit comprising:

– an output stage according to any one of claims 2 to 7;

– a first control apparatus according to any one of claims 8 to 9 and 12 wherein the control stage of the first control apparatus is connected to the output stage; and,

– a second control apparatus according to any one of claims 10 to 11 and 12 wherein the control stage of the second control apparatus is connected to the output stage;

wherein,

– when the control stage of the first control apparatus is connected to the output stage, the control stage of the second control apparatus is electrically disconnected from the output stage, the output stage being configured to operate in the first operating state; and,

– when the control stage of the second control apparatus is connected to the output stage, the control stage of the first control apparatus is electrically

disconnected from the output stage, the output stage being configured to operate in the second operating state.

14. A device comprising:

– the circuit of claim 12;

– a battery configured to be connected to the input terminals of the circuit; and,

– a loudspeaker configured to be connected to the output terminals of the circuit.

15. Use of an output stage according to any one of claims 2 to 7, in conjunction with:

– a first control apparatus according to any one of claims 8 to 9 and 12 wherein the control stage of the first control apparatus is connected to the output stage; and,

– a second control apparatus according to any one of claims 10 to 11 and 12 wherein the control stage of the second control apparatus is connected to the output stage;

wherein,

– when the control stage of the first control apparatus is connected to the output stage, the control stage of the second control apparatus is electrically disconnected from the output stage, the output stage being configured to operate in the first operating state; and,

– when the control stage of the second control apparatus is connected to the output stage, the control stage of the first control apparatus is electrically disconnected from the output stage, the output stage being configured to operate in the second operating state.

Drawings

FIG. 1

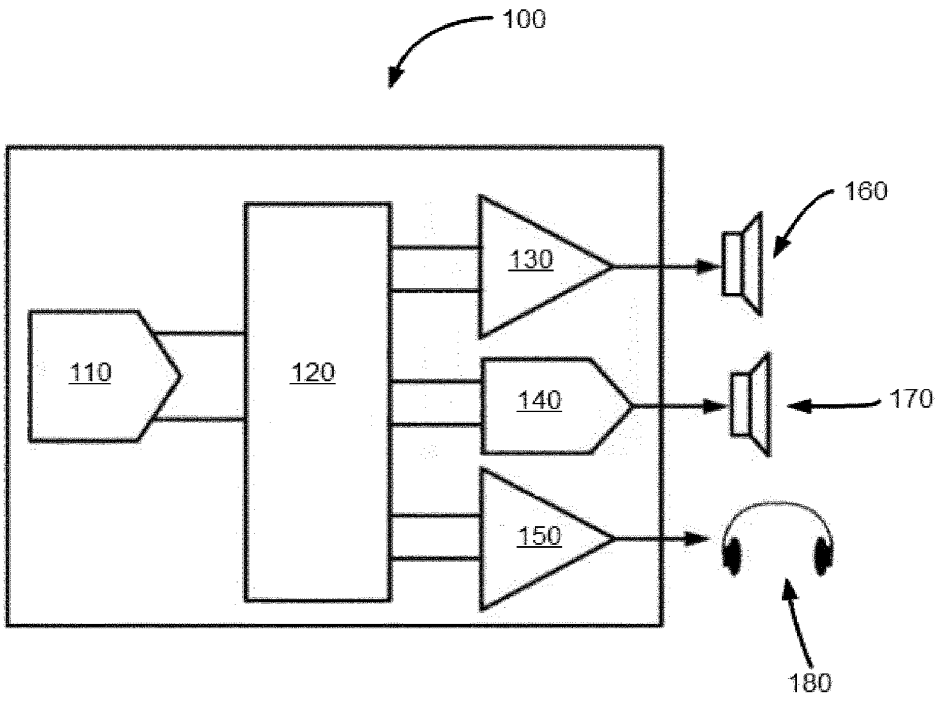


FIG. 2

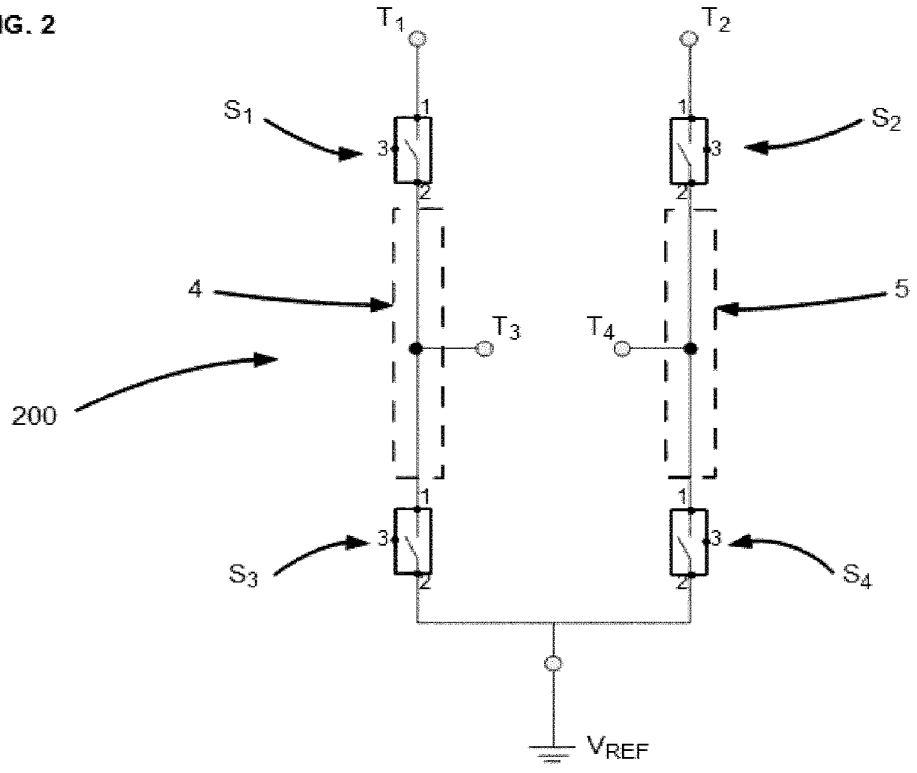
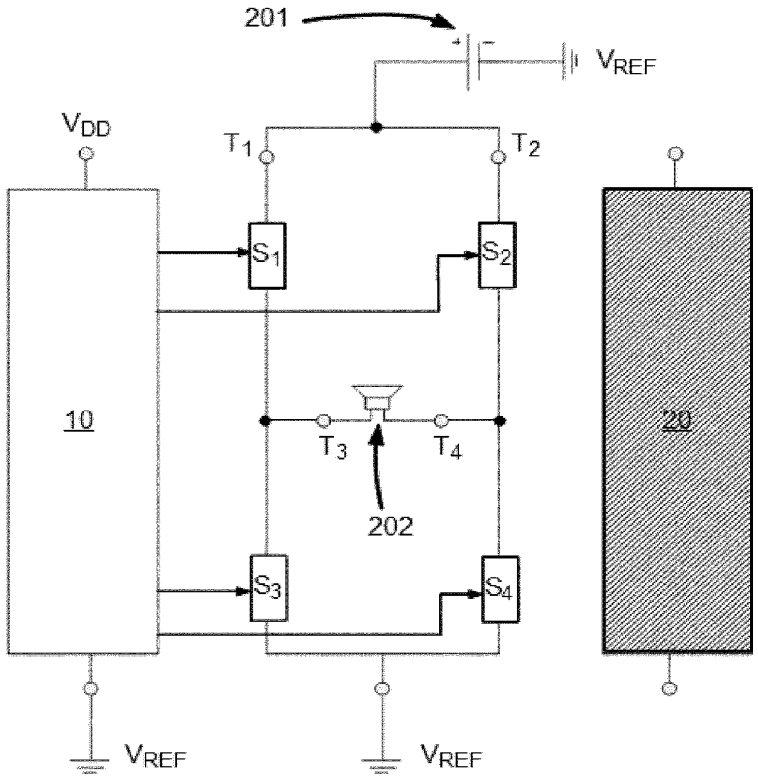


FIG. 3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T4
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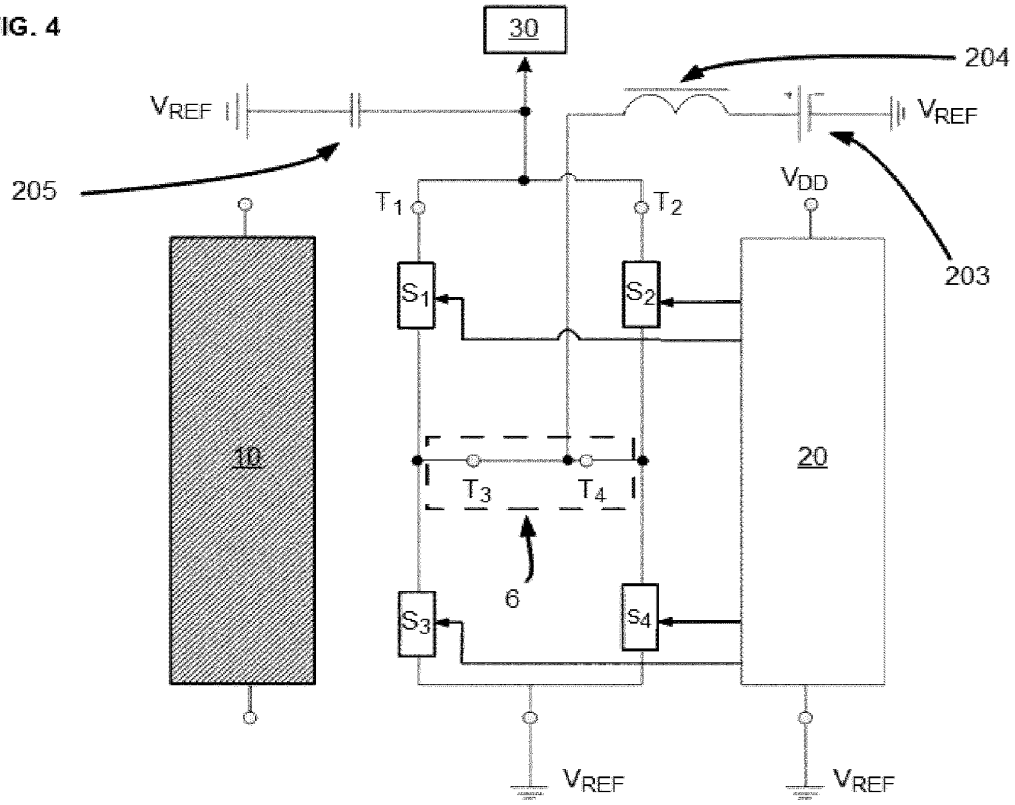
VREF
VREF

FIG. 4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VREF
VREF

FIG. 5

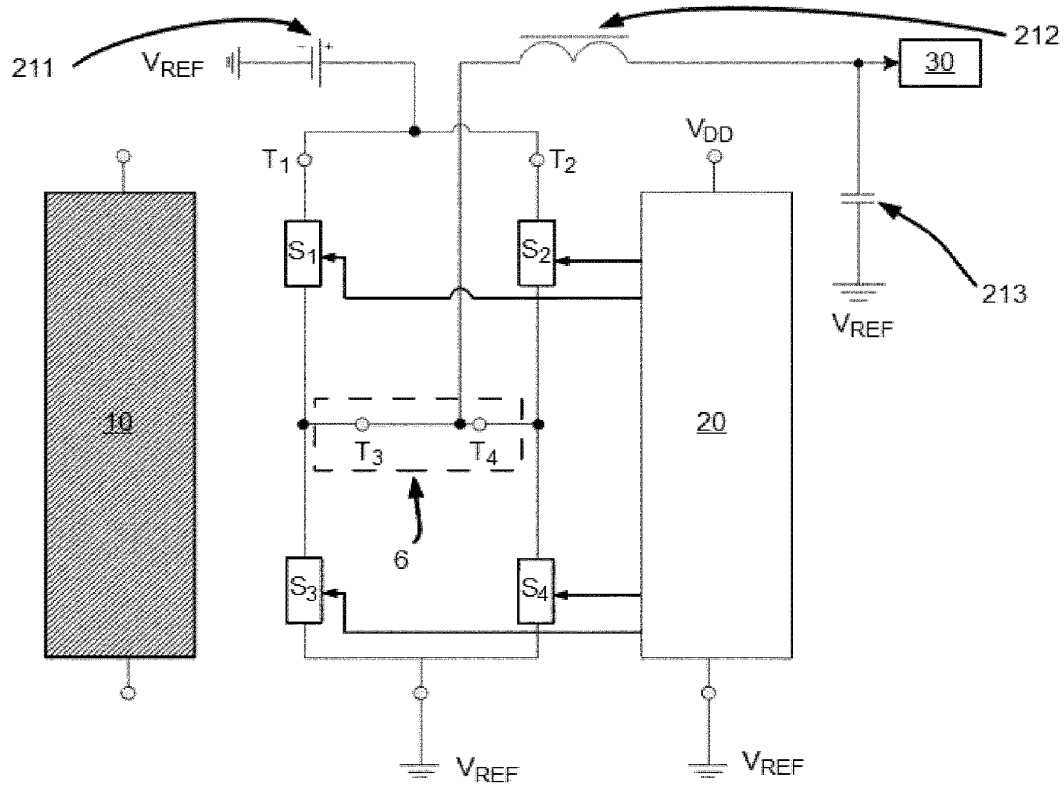
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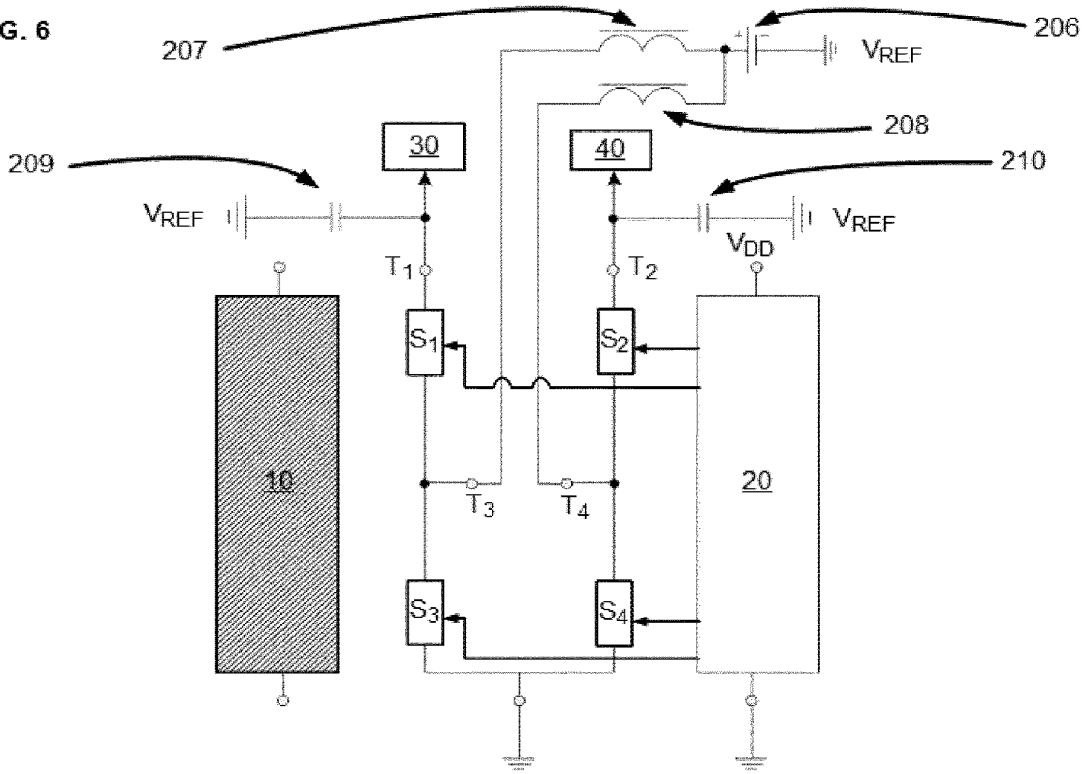
FIG. 6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S_4

FIG. 7

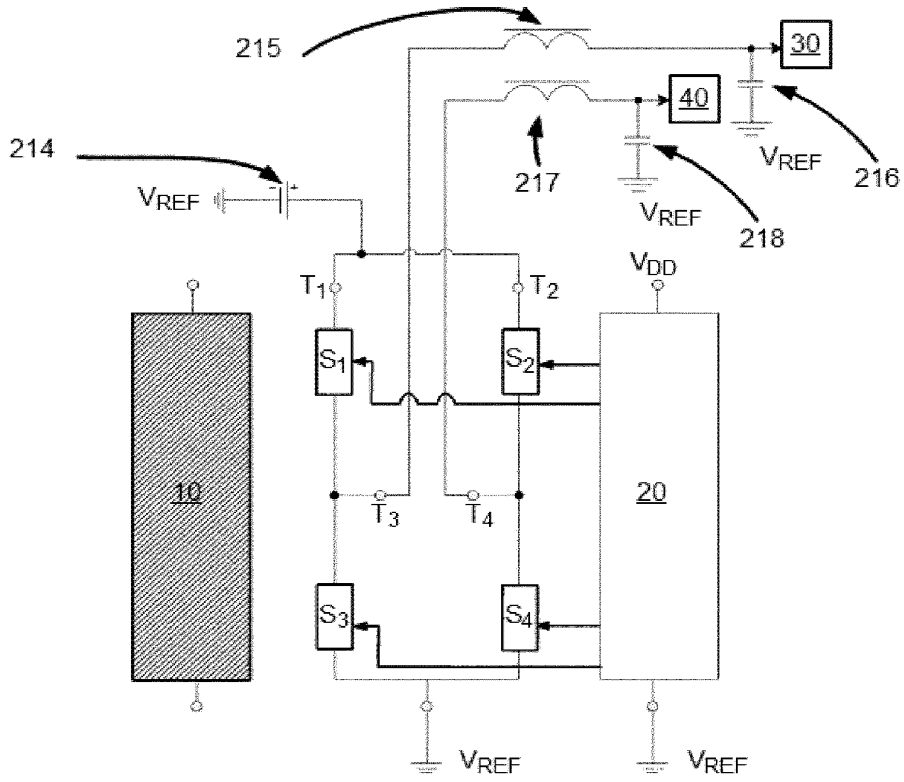
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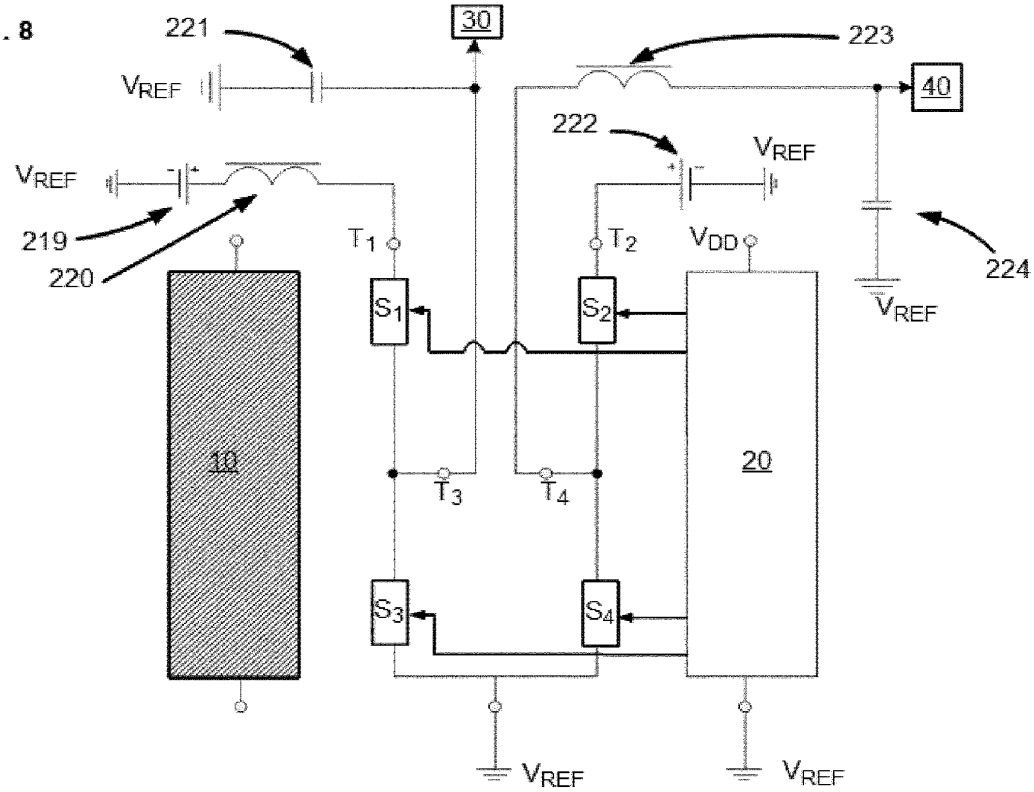
FIG. 8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V_{REF}
V_{REF}

Docket No.: 0112-301/C03308 US1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Philippe SIRITO-OLIVIER *et al*.

Confirmation No.: 9535

Application No.: 14/889,892

Art Unit: *To Be Assigned*

Filed: November 9, 2015

Examiner: *To Be Assigned*

For: RECONFIGURABLE OUTPUT STAGE

SUBMISSION OF DECLARATION

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Applicant respectfully submits the signed Declarations from the inventors.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Steven M. duBois at the telephone number listed below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 50-5835 for any additional fees required under 37.C.F.R. §§1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,
PATENT PORTFOLIO BUILDERS, PLLC

By: /stevenmdubois/
Steven M. duBois
Registration No. 35,023

Date: November 20, 2015

Customer No. 113648

Patent Portfolio Builders, PLLC
P.O. Box 7999
Fredericksburg, VA 22404
(540) 361-1863, Ext. 125

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention:	RECONFIGURABLE OUTPUT STAGE

As the below named inventor, I hereby declare that:

This declaration is directed to:

☐ The application attached hereto. If the application is not attached hereto, the application is identified by the Attorney docket number and title as set forth above.

☑ United States application or PCT international application number 14/889,892 filed on November 9, 2015.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I have reviewed and understand the contents of the above-identified application, including the claims.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations § 1.56.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

LEGAL NAME OF INVENTOR

Inventor: Philippe SIRITO-OLIVIER Date: Nov. 16th 2015

Signature: Philippe Sirito-Olivier

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention:	RECONFIGURABLE OUTPUT STAGE

As the below named inventor, I hereby declare that:

This declaration is directed to:

☐ The application attached hereto. If the application is not attached hereto, the application is identified by the Attorney docket number and title as set forth above.

☑ United States application or PCT international application number 14/889,892 filed on November 9, 2015.

The above-identified application was made or authorized to be made by me.

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I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

LEGAL NAME OF INVENTOR

Inventor: Patrizia MILAZZO Date: 17-11-2015

Signature: Patrizia Milazzo

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention:	RECONFIGURABLE OUTPUT STAGE

As the below named inventor, I hereby declare that:

This declaration is directed to:

☐ The application attached hereto. If the application is not attached hereto, the application is identified by the Attorney docket number and title as set forth above.

☑ United States application or PCT international application number 14/889,892 filed on November 9, 2015.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

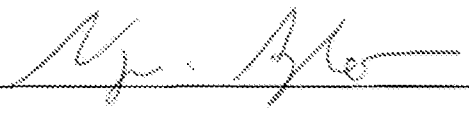
I have reviewed and understand the contents of the above-identified application, including the claims.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations § 1.56.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

LEGAL NAME OF INVENTOR

Inventor: Angelo NAGARI Date: November 12th 2015

Signature: 

Electronic Acknowledgement Receipt

EFS ID:	24144046
Application Number:	14889892
International Application Number:	
Confirmation Number:	9535
Title of Invention:	Reconfigurable Output Stage
First Named Inventor/Applicant Name:	Philippe SIRITO-OLIVIER
Customer Number:	113648
Filer:	Steven Maurice Dubois/Andrea Terry
Filer Authorized By:	Steven Maurice Dubois
Attorney Docket Number:	0112-301/C03308 US1
Receipt Date:	20-NOV-2015
Filing Date:	
Time Stamp:	12:04:34
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	C03308-US1_2015-11-20_Declaration_Submission_0112-301.pdf	77714 e089f36e41548c775c79b28d3b3eee363b32c9c8	no	1

Warnings:	
Information:	

2	Oath or Declaration filed	C03308-US1_2015-11-20_signed_Declaration_0112-301.pdf	1983282 6cca0cae660686046cd1281b0738be63526122d0	no	3

Warnings:	
Information:	
Total Files Size (in bytes):	2060996

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 14/889,892

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	480
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720
TOTAL CLAIMS (37 CFR 1.16(i))	15 minus 20 =	*			OR	x 80 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1 minus 3 =	*				x 420 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1480

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

U.S. APPLICATION NUMBER NO.	FIRST NAMED INVENTOR	ATTY. DOCKET NO.
14/889,892	Philippe SIRITO-OLIVIER	0112-301/C03308 US1

113648
Patent Portfolio Builders, PLLC
P.O. Box 7999
Fredericksburg, VA 22404-7999

INTERNATIONAL APPLICATION NO.	
PCT/EP2014/061350	
I.A. FILING DATE	PRIORITY DATE
06/02/2014	06/03/2013

CONFIRMATION NO. 9535
371 ACCEPTANCE LETTER

OC000000079981594

Date Mailed: 01/22/2016

NOTICE OF ACCEPTANCE OF APPLICATION UNDER 35 U.S.C 371 AND 37 CFR 1.495

The applicant is hereby advised that the United States Patent and Trademark Office, in its capacity as a Designated / Elected Office (37 CFR 1.495), has ACCEPTED the above identified international application for national patentability examination in the United States Patent and Trademark Office.

The United States Application Number assigned to the application is shown above. A Filing Receipt will be issued for the present application in due course. **THE DATE APPEARING ON THE FILING RECEIPT AS THE "FILING DATE or 371(c) DATE" IS THE DATE ON WHICH THE LAST OF THE 35 U.S.C. 371 (c)(1) and (c)(2) REQUIREMENTS HAS BEEN RECEIVED IN THE OFFICE. THIS DATE IS SHOWN BELOW.** The filing date of the above identified application is the international filing date of the international application (Article 11(3) and 35 U.S.C. 363)

11/09/2015
DATE OF RECEIPT OF 35 U.S.C.
371(c)(1) and (c)(2) REQUIREMENTS

The following items have been received:

- Copy of the International Application filed on 11/09/2015
- Copy of the International Search Report filed on 11/09/2015
- Preliminary Amendments filed on 11/09/2015
- Information Disclosure Statements filed on 11/09/2015
- Inventor's Oath or Declaration filed on 11/20/2015
- Request for Immediate Examination filed on 11/09/2015
- U.S. Basic National Fees filed on 11/09/2015
- Priority Documents filed on 11/09/2015
- Authorization to Permit Access filed on 11/09/2015
- Application Data Sheet (37 CFR 1.76) filed on 11/09/2015

Applicant is reminded that any communications to the United States Patent and Trademark Office must be mailed to the address given in the heading and include the U.S. application no. shown above (37 CFR 1.5)

SHAKEEL AHMED

Telephone: (703) 756-1423

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
14/889,892	11/09/2015		1620	0112-301/C03308 US1	15	1

CONFIRMATION NO. 9535

FILING RECEIPT

113648
Patent Portfolio Builders, PLLC
P.O. Box 7999
Fredericksburg, VA 22404-7999

OC000000079981593

Date Mailed: 01/22/2016

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Philippe SIRITO-OLIVIER, Saint Egreve, FRANCE;
Patrizia MILAZZO, S. Agata Li Battiati, ITALY;
Angelo NAGARI, Grenoble, FRANCE;

Applicant(s)

ST-Ericsson SA, Plan-Les-Quates, SWITZERLAND;

Power of Attorney: None

Domestic Priority data as claimed by applicant

This application is a 371 of PCT/EP2014/061350 06/02/2014

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.)
EUROPEAN PATENT OFFICE (EPO) 13305740.6 06/03/2013

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: No

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 01/18/2016

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 14/889,892**

Projected Publication Date: 04/28/2016

Non-Publication Request: No

Early Publication Request: No
Title

Reconfigurable Output Stage

Preliminary Class

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

MULTIPLE DEPENDENT CLAIM FEE CALCULATION SHEET

Substitute for Form PTO-1360
(For use with Form PTO/SB/06)

Application Number	Filing Date
14889892	

Applicant(s) Philippe SIRITO-OLIVIER

* May be used for additional claims or amendments

CLAIMS	AS FILED		AFTER FIRST AMENDMENT		AFTER SECOND AMENDMENT	
	Indep	Depend	Indep	Depend	Indep	Depend
1	1		1			
2		1		1		
3		1		1		
4		1		1		
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Total Indep	1		1		0	
Total Depend	22	↵	14	↵	0	↵
Total Claims	23		15		0	

	*		*		*	
	Indep	Depend	Indep	Depend	Indep	Depend
51						
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/889,892	11/09/2015	Philippe SIRITO-OLIVIER	0112-301/C03308 US1

CONFIRMATION NO. 9535

113648
Patent Portfolio Builders, PLLC
P.O. Box 7999
Fredericksburg, VA 22404-7999

PUBLICATION NOTICE

OC00000082528716

Title: Reconfigurable Output Stage

Publication No.US-2016-0118892-A1
Publication Date:04/28/2016

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently http://pair.uspto.gov/. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

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Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

Attorney's Docket No. 0112-301/C03308 US1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	)	
	)	Group Art Unit: 2654
Philippe SIRITO-OLIVIER *et al.*	)	
	)	Examiner: Chin, Vivian C.
Application No.: 14/889,892	)	
	)	Confirmation No.: 9535
Filed: November 9, 2015	)	
	)	
For: RECONFIGURABLE OUTPUT STAGE	)	

SUPPLEMENTAL PRELIMINARY AMENDMENT

Commissioner for Patents
Alexandria, VA 22313-1450

Sir:

Prior to examination of the above-identified application, please enter the following amendments:

IN THE ABSTRACT:

Please replace the abstract as follows:

An output stage configuration with four configurable input/output terminals and four switches is specified. Each switch has a first main terminal, a second main terminal and a control terminal, which receives a control signal for controlling the open or closed state of the switch. The output stage is included in a circuit together with a first control apparatus and a second control apparatus. When a control stage of the first control apparatus is connected to the output stage, a control stage of the second control apparatus is electrically disconnected from the output stage, and the output stage operates in a first operating state. When the control stage of the second control apparatus is connected to the output stage, the control stage of the first control apparatus is electrically disconnected from the output stage, the output stage then operating in a second operating state.

IN THE CLAIMS:

The text of all pending claims is set forth below. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered). The following listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) An output stage adapted to operate in at least a first operating state and a second operating state, the output stage comprising:

[[–]]a first, a second, a third and a fourth configurable input/output terminals; and,

[[–]]a first, a second, a third and a fourth switches, each having a first main terminal, a second main terminal and a control terminal, the control terminal being adapted to receive a control signal for controlling the open or closed state of the switch~~;~~,

wherein,

[[–]]the first input/output terminal is connected to the first main terminal of the first switch;

[[–]]the second input/output terminal is connected to the first main terminal of the second switch;

[[–]]the second main terminal of the first switch is connected to the first main terminal of the third switch through a first branch,

[[–]]the second main terminal of the second switch is connected to the first main terminal of the fourth switch through a second branch;

[[–]]the third input/output terminal is connected to the first branch and the fourth input/output terminal is connected to the second branch;

[[–]]the second main terminals of the third and fourth switches are both connected to a common node receiving a reference potential; and,

wherein,

[[–]]when the first and second input/output terminals are configured to operate as input terminals, the third and fourth input/output terminals are configured to operate as

output terminals; and,

[[–]]when the first and second input/output terminals are configured to operate as output terminals, the third and fourth input/output terminals are configured to operate as input terminals; and,

wherein,

[[–]]in the first operating state, the output stage is arranged in a first electrical configuration; and

[[–]]in the second operating state wherein the output stage is arranged in a second electrical configuration different from the first configuration.

2. (Currently Amended) The output stage of claim 1, wherein, in the first operating state:

[[–]]the first and second input/output terminals are configured to operate as input terminals and are configured to be connected to a common node receiving a supply potential; and,

[[–]]the third and fourth input/output terminals are configured to be connected to a load element.

3. (Currently Amended) The output stage of claim 1 further comprising an inductor and a decoupling capacitor, wherein, in the second operating state:

[[–]]the first and second input/output terminals are configured to operate as output terminals and are configured to be connected, in series with a load element and in parallel with the decoupling capacitor;

[[–]]the third and fourth input/output terminals are short-circuited;

[[–]]one end of the inductor is configured to be connected to the short-circuited third and fourth input/output terminals, and another end the inductor is configured to be connected to a common node receiving a supply potential.

4. (Currently Amended) The output stage of claim 1 further comprising an inductor and a decoupling capacitor, wherein, in the second operating state:

[[–]]the first and second input/output terminals are configured to operate as input terminals and are configured to be connected to a common node receiving a supply potential;

[[–]]the third and fourth input/output terminals are short-circuited;

[[–]]one end of the inductor is configured to be connected to the short-circuited third and fourth input/output terminals, and another end the inductor is configured to be connected, in series with a load element and in parallel with the decoupling capacitor.

5. (Currently Amended) The output stage of claim 1 further comprising a first and second inductors and a first and second decoupling capacitors, wherein, in the second operating state:

[[–]]the first and second input/output terminals are configured to operate as output terminals;

[[–]]the first input/output terminal is configured to be connected, in series with a first load element and in parallel with the first decoupling capacitor;

[[–]]the second input/output terminal is configured to be connected, in series with a second load element and in parallel with the second decoupling capacitor;

[[–]]one end of the first inductor is configured to be connected to the third input/output terminal, and another end of the first inductor is configured to be connected to a common node receiving a supply potential; and

[[–]]one end of the second inductor is configured to be connected to the fourth input/output terminal, and another end of the second inductor is configured to be connected to the common node receiving a supply potential.

6. (Currently Amended) The output stage of claim 1 further comprising a first and second inductors, and a first and second decoupling capacitors ~~(216, 218)~~, wherein, in the second operating state:

[[–]]the first and second input/output terminals are configured to operate as input terminals and are configured to be connected to a common node receiving a supply potential;

[[–]]one end of the first inductor is configured to be connected to the third input/output terminal, and another end of the first inductor is configured to be connected, in series with a first load element and in parallel with the first decoupling capacitor; and

[[–]]one end of the second inductor is configured to be connected to the fourth input/output terminal, and another end of the second inductor is configured to be connected, in series with a second load element and in parallel with the second decoupling capacitor.

7. (Currently Amended) The output stage of claim 1 further comprising a first and second inductors and a first and second decoupling capacitors, wherein, in the second operating state:

[[–]]the first and second input/output terminals are configured to operate as input terminals;

[[–]]the third input/output terminal is configured to be connected, in series with a first load element and in parallel with the first decoupling capacitor;

[[–]]one end of the first inductor is configured to be connected to the first input/output terminal, and another end of the first inductor is configured to be connected to a first node receiving a supply potential; and

[[–]]one end of the second inductor is configured to be connected to the fourth input/output terminal, and another end of the second inductor is configured to be connected, in series with a second load element and in parallel with the second decoupling capacitor.

8. (Currently Amended) A control apparatus comprising:

[[–]]a control stage configured to control an output stage according to claim 2.

9. (Original) The control apparatus of claim 8 wherein the control stage is a Class-D control stage.

10. (Currently Amended) A control apparatus comprising:

[[–]]a control stage configured to control an output stage according to claim 3.

11. (Original) The control apparatus of claim 10 wherein the control stage is a DC-DC converter control stage.

12. (Currently Amended) The control apparatus of claim 8, wherein the control stage is adapted to control the output stage by generating control signals for controlling the first, second, third and fourth switches through their respective control terminals.

13. (Currently Amended) A circuit comprising:

[[–]]an output stage according to claim 2;

[[–]]a first control apparatus wherein the control stage of the first control apparatus is connected to the output stage; and,

[[–]]a second control apparatus wherein the control stage of the second control apparatus is connected to the output stage;

wherein,

[[–]]when the control stage of the first control apparatus is connected to the output stage, the control stage of the second control apparatus is electrically disconnected from the output stage, the output stage being configured to operate in the first operating state; and,

[[–]]when the control stage of the second control apparatus is connected to the output stage, the control stage of the first control apparatus is electrically disconnected from the output stage, the output stage being configured to operate in the second operating state.

14. (Currently Amended) A device comprising:

[[–]]the circuit of claim 12;

[[–]]a battery configured to be connected to the input terminals of the circuit; and,

[[–]] a loudspeaker configured to be connected to the output terminals of the circuit.

15. (Currently Amended) An apparatus comprising: ~~Use of~~ an output stage according to claim 2 connected to ~~, in conjunction with:~~

[[–]]a first control apparatus, ~~wherein the~~ a control stage of the first control apparatus ~~is~~ being connected to the output stage; or to ~~and,~~

[[–]]a second control apparatus, ~~wherein the~~ a control stage of the second control apparatus being ~~is~~ connected to the output stage;

wherein,

[[–]]when the control stage of the first control apparatus is connected to the output stage, the control stage of the second control apparatus is electrically disconnected from the output stage, the output stage being configured to operate in the first operating state; and,

[[–]]when the control stage of the second control apparatus is connected to the output stage, the control stage of the first control apparatus is electrically disconnected from the output stage, the output stage being configured to operate in the second operating state.

REMARKS

In this supplemental preliminary amendment, the claims have been amended to place them in better form according to the U.S. patent claim practice. A new abstract is provided to meet the requirements of 37 C.F.R. 1.72. No new matter has been added. Prompt examination on the merits is respectfully requested.

Respectfully submitted,

PATENT PORTFOLIO BUILDERS PLLC

By: */Luminita TODOR/*
Luminita A. Todor, Ph.D
Registration No. 57,639

Date: July 14, 2016
Customer No. 113648
Patent Portfolio Builders PLLC
P.O. Box 7999
Fredericksburg, VA 22404
(540) 361-1863, Ext. 126

Electronic Acknowledgement Receipt

EFS ID:	26348168
Application Number:	14889892
International Application Number:	
Confirmation Number:	9535
Title of Invention:	Reconfigurable Output Stage
First Named Inventor/Applicant Name:	Philippe SIRITO-OLIVIER
Customer Number:	113648
Filer:	Luminita Anca Todor/Erin Rathgeber
Filer Authorized By:	Luminita Anca Todor
Attorney Docket Number:	0112-301/C03308 US1
Receipt Date:	14-JUL-2016
Filing Date:	09-NOV-2015
Time Stamp:	12:20:44
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		C03308-US1_2016-07-14_Supp_Preliminary_Amendment_0112-301.pdf	84529 1528d686bf77c0b2701f24fa10ab63f0dec4a08d	yes	9

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Preliminary Amendment	1	1
	Abstract	2	2
	Claims	3	8
	Applicant Arguments/Remarks Made in an Amendment	9	9
Warnings:			
Information:			
	Total Files Size (in bytes):	84529	

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

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PTO/SB/06 (09-11)
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 14/889,892	Filing Date 11/09/2015	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT **07/14/2016**

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 15	Minus	** 20	= 0	X $80 =	0
Independent (37 CFR 1.16(h))	* 1	Minus	***3	= 0	X $420 =	0
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	0

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
THERESA LINDSAY

PTO/AIA/80 (07-12)
Approved for use through 11/30/2014. OMB 0651-0035
U.S. Patent and Trademark Office; U.S DEPARTMENT OF COMMERCE

POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(c).

I hereby appoint:

☐ Practitioners associated with Customer Number:

OR

☒ Practitioner(s) named below (If more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number
Shreen K. Danamraj	41,696
Betty Formby	36,536
Kenneth A. McClure	62,886
Thomas L. Crisman	24,846
Spencer R. Guy	71,035

Name	Registration Number
Lewis W. Schiel Jr.	69,883

As attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignments documents attached to this form in accordance with 37 CFR 3.73(c).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(c) to:

☒ The address associated with Customer Number: 28240

OR

☐	Firm or Individual Name		
	Address		
	City	State	Zip
	Country		
	Telephone	Email	

Assignee Name and Address: Optis Circuit Technology, LLC
P.O. Box 250649
Plano, TX 75025

A copy of this form, together with a statement under 37 CFR 3.73(c) (Form PTO/AIA/96 or equivalent) is required to be Filed in each application in which this form is used. The statement under 37 CFR 3.73(c) may be completed by one of The practitioners appointed in this form, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature		Date	December 15, 2016
Name	James W. Ribman	Telephone	214-744-5000
Title	President		

PTO/AIA/96 (08-12)
Approved for use through 01/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: Philippe SIRITO-OLIVIER; Patrizia MILAZZO; Angelo NAGARI

Application No./Patent No.: 14/889,892 Filed/Issue Date: November 9, 2015

Titled: Reconfigurable Output Stage

OPTIS CIRCUIT TECHNOLOGY, LLC, a LIMITED LIABILITY COMPANY

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☑ The assignee of the entire right, title, and interest.

2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):

☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

B. ☑ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: Philippe SIRITO-OLIVIER; Patrizia MILAZZO; Angelo NAGARI To: ST-ERICSSON SA

The document was recorded in the United States Patent and Trademark Office at

Reel 036991, Frame 0781, or for which a copy thereof is attached.

2. From: ST-ERICSSON SA To: ST-ERICSSON, EN LIQUIDATION

The document was recorded in the United States Patent and Trademark Office at

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Approved for use through 01/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

STATEMENT UNDER 37 CFR 3.73(c)

3. From: ST-ERICSSON SA, EN LIQUIDATION To: OPTIS CIRCUIT TECHNOLOGY, LLC

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☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☑ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

Signature	January 12, 2017 Date
Shreen K. Danamraj Printed or Typed Name	41,696 Title or Registration Number

Electronic Acknowledgement Receipt

EFS ID:	28049043
Application Number:	14889892
International Application Number:	
Confirmation Number:	9535
Title of Invention:	Reconfigurable Output Stage
First Named Inventor/Applicant Name:	Philippe SIRITO-OLIVIER
Customer Number:	113648
Filer:	Shreen K. Danamraj/Sarah Parker
Filer Authorized By:	Shreen K. Danamraj
Attorney Docket Number:	0112-301/C03308 US1
Receipt Date:	12-JAN-2017
Filing Date:	09-NOV-2015
Time Stamp:	15:51:36
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	QE1541US1_Transmittal_Letter.pdf	106246 cab0f3282a8f2252eb2045fcaec53542962ad534	no	1

Warnings:

Information:					
2	Application Data Sheet	QE1541US1_Corrected_ADS.pdf	1207269 9abf564bd86a00a72ac4ee32498010494b14e0f6	no	6
Warnings:					
Information:					
This is not an USPTO supplied ADS fillable form					
3	Power of Attorney	QE1541US1_PTO-AIA-80-General_Power_of_Attorney.pdf	95729 b0c9188c4b544794f39466278abe5813bf5a0797	no	1
Warnings:					
The page size in the PDF is too large. The pages should be 8.5 x 11 or A4. If this PDF is submitted, the pages will be resized upon entry into the Image File Wrapper and may affect subsequent processing					
Information:					
4	Assignee showing of ownership per 37 CFR 3.73	QE1541US1_Statement_Under_Rule_373.pdf	354764 7d34fbedc5d80f03f702b93fab9c32be2ae4c4ac	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	1764008	

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

THE DANAMRAJ LAW GROUP, P.C.

ATTORNEYS AND COUNSELORS
INTELLECTUAL PROPERTY LAW AND RELATED MATTERS

THE TURLEY LAW CENTER, SUITE 810
6440 NORTH CENTRAL EXPRESSWAY
DALLAS, TEXAS 75206

SHREEN K. DANAMRAJ
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(214) 750-5666 (tel)
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shreen@danamraj.com

January 12, 2017

Electronic Filing:

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313 -1450

Re: Application No.: 14/889,892
Reconfigurable Output Stage
Confirmation No.: 9535
Our File: 2000-1043US1

Dear Sir:

Enclosed for filing please find the following item(s) relating to the above-identified application:

(1) Corrected ADS;

(2) Executed Power of Attorney; and

(3) Statement Under 37 CFR 3.73(c).

Charge Statement
No/additional fees are believed to be due for the filing of the attached paper(s). However, if any (additional) fees are due, or any overpayments have been made, please charge, or credit, Deposit Account 03-1130.

If you have any questions or comments concerning this matter, please call the undersigned at your earliest convenience. Otherwise, please accept the enclosed.

Issuance of an updated Filing Receipt and a Notice of Acceptance of the Power of Attorney is awaited.

Sincerely,

Shreen K. Danamraj
Reg. No. 41,696

Enclosures

PTO/AIA/14 (07-14)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	~~0112-301/C03308-US1~~ 2000-1043US1
	Application Number	14/889,892
Title of Invention	Reconfigurable Output Stage	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Philippe		SIRITO-OLIVIER	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Saint Egreve	Country of Residence i	FR

Mailing Address of Inventor:

Address 1	2bis rue de Bellevue Parc symphonie 13		
Address 2			
City	Saint Egreve	State/Province	
Postal Code	F-38120	Country i	FR

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Patrizia		MILAZZO	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	S. Agata Li Battiati	Country of Residence i	IT

Mailing Address of Inventor:

Address 1	Via J.F. Kennedy 23		
Address 2			
City	S. Agata Li Battiati	State/Province	
Postal Code	I-95030	Country i	IT

Inventor 3 Remove

Legal Name

PTO/AIA/14 (07-14)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	~~0112-301/C03308-US1~~ 2000-1043US1
	Application Number	14/889,892
Title of Invention	Reconfigurable Output Stage	

Prefix	Given Name	Middle Name	Family Name	Suffix
	Angelo		NAGARI	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Grenoble	Country of Residence [i]	FR

Mailing Address of Inventor:

Address 1	12 Rue de la Poste		
Address 2			
City	Grenoble	**State/Province**	
Postal Code	F-38000	**Country** [i]	FR

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	~~113648~~ 28240		
Email Address		Add Email	Remove Email

Application Information:

Title of the Invention	Reconfigurable Output Stage		
Attorney Docket Number	~~0112-301/C03308-US1~~ 2000-1043US1	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	4	**Suggested Figure for Publication (if any)**	2

Filing By Reference :

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country [i]

PTO/AIA/14 (07-14)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	~~0112-301/C03308-US1~~ 2000-1043US1
	Application Number	14/889,892
Title of Invention	Reconfigurable Output Stage	

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	◉ ~~Customer Number~~	ⓧ US Patent Practitioner	◯ Limited Recognition (37 CFR 11.9)
Customer Number	~~113648~~ Shreen K. Danamraj 41,696; Betty Formby 36,536; Kenneth A. McClure 62,886; Thomas L. Crisman 24,846; Spencer R. Guy 71,035; Lewis W. Schiel Jr. 69,883		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the application number blank.

Prior Application Status			Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	a 371 of international	PCT/EP2014/061350	2014-06-02

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX) the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

			Remove
Application Number	Country	Filing Date (YYYY-MM-DD)	Access Code (if applicable)
13305740.6	EP	2013-06-03	

PTO/AIA/14 (07-14)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	~~0112-301/C03308-US1~~ 2000-1043US1
	Application Number	14/889,892
Title of Invention	Reconfigurable Output Stage	

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Authorization to Permit Access:

☒ Authorization to Permit Access to the Instant Application by the Participating Offices

If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application.

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date o f filing this Authorization.

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

PTO/AIA/14 (07-14)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	~~0112-301/C03308-US1~~ 2000-1043US1
	Application Number	14/889,892
Title of Invention	Reconfigurable Output Stage	

Applicant 1 Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

(•) Assignee	( ) Legal Representative under 35 U.S.C. 117	( ) Joint Inventor
( ) Person to whom the inventor is obligated to assign.	( ) Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor :

If the Applicant is an Organization check here. [X]

Organization Name	~~ST-Ericsson SA~~ Optis Circuit Technology, LLC		
Mailing Address Information For Applicant:			
Address 1	~~39 Chemin du Champ-des-Filles~~ P.O. Box 250649		
Address 2			
City	~~Plan-Les-Ouates~~ Plano	**State/Province**	TX
Country i ~~CH~~ US		Postal Code	~~CH-1228~~ 75025
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not subsitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication . An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

Remove

If the Assignee or Non-Applicant Assignee is an Organization check here. [ ]

PTO/AIA/14 (07-14)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	~~0112-301/C03308 US1~~ 2000-1043US1
	Application Number	14/889,892
Title of Invention	Reconfigurable Output Stage	

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. Add

Signature:

Remove

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Signature	~~/stevenmdubois/-~~			Date (YYYY-MM-DD)	~~2015-11-09~~ 2017-01-12
First Name	~~Steven~~ Shreen	Last Name	~~duBois~~ Danamraj	Registration Number	~~35023~~ 41,696

Additional Signature may be generated within this form by selecting the Add button. Add

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/889,892	11/09/2015	Philippe SIRITO-OLIVIER	2000-1043US1

CONFIRMATION NO. 9535

POA ACCEPTANCE LETTER

28240
THE DANAMRAJ LAW GROUP, P.C.
TURLEY LAW CENTER, SUITE 810
6440 N. CENTRAL EXPRESSWAY
DALLAS, TX 75206

OC000000088526567

Date Mailed: 01/19/2017

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 01/12/2017.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/cnguyen/

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
14/889,892	11/09/2015	2651	1620	2000-1043US1	15	1

CONFIRMATION NO. 9535

CORRECTED FILING RECEIPT

28240
THE DANAMRAJ LAW GROUP, P.C.
TURLEY LAW CENTER, SUITE 810
6440 N. CENTRAL EXPRESSWAY
DALLAS, TX 75206

OC000000088526683

Date Mailed: 01/19/2017

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Philippe SIRITO-OLIVIER, Saint Egreve, FRANCE;
Patrizia MILAZZO, S. Agata Li Battiati, ITALY;
Angelo NAGARI, Grenoble, FRANCE;

Applicant(s)

Optis Circuit Technology, LLC, Plano, TX;

Power of Attorney:

Thomas Crisman--24846
Betty Formby--36536
Shreen Danamraj--41696
Kenneth McClure--62886
Lewis Schiel Jr.--69883
Spencer Guy--71035

Domestic Priority data as claimed by applicant

This application is a 371 of PCT/EP2014/061350 06/02/2014

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.)
EUROPEAN PATENT OFFICE (EPO) 13305740.6 06/03/2013

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: No

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 01/18/2016

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 14/889,892**

Projected Publication Date: Not Applicable

Non-Publication Request: No

Early Publication Request: No

Title

Reconfigurable Output Stage

Preliminary Class

381

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific

countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop

technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

28240 7590 03/06/2017

THE DANAMRAJ LAW GROUP, P.C.
TURLEY LAW CENTER, SUITE 810
6440 N. CENTRAL EXPRESSWAY
DALLAS, TX 75206

EXAMINER
MONIKANG, GEORGE C

ART UNIT	PAPER NUMBER
2651	

DATE MAILED: 03/06/2017

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/889,892	11/09/2015	Philippe SIRITO-OLIVIER	2000-1043US1	9535

TITLE OF INVENTION: Reconfigurable Output Stage

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	06/06/2017

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

28240 7590 03/06/2017
THE DANAMRAJ LAW GROUP, P.C.
TURLEY LAW CENTER, SUITE 810
6440 N. CENTRAL EXPRESSWAY
DALLAS, TX 75206

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/889,892	11/09/2015	Philippe SIRITO-OLIVIER	2000-1043US1	9535

TITLE OF INVENTION: Reconfigurable Output Stage

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	06/06/2017

EXAMINER	ART UNIT	CLASS-SUBCLASS
MONIKANG, GEORGE C	2651	381-120000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ Applicant certifying micro entity status. See 37 CFR 1.29 — NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ❑ Applicant asserting small entity status. See 37 CFR 1.27 — NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ❑ Applicant changing to regular undiscounted fee status. — NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/889,892	11/09/2015	Philippe SIRITO-OLIVIER	2000-1043US1	9535

28240 7590 03/06/2017

THE DANAMRAJ LAW GROUP, P.C.
TURLEY LAW CENTER, SUITE 810
6440 N. CENTRAL EXPRESSWAY
DALLAS, TX 75206

EXAMINER	
MONIKANG, GEORGE C	

ART UNIT	PAPER NUMBER
2651	

DATE MAILED: 03/06/2017

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 14/889,892	Applicant(s) SIRITO-OLIVIER ET AL.	
	Examiner GEORGE MONIKANG	Art Unit 2651	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *7/14/2016*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-15*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☒ All b) ☐ Some *c) ☐ None of the:
   1. ☒ Certified copies of the priority documents have been received.
   2. ☒ Certified copies of the priority documents have been received in Application No. *14/889,892* .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

DETAILED ACTION

Allowable Subject Matter

1. Claims 1-15 are allowed.

2. The following are examiner's statement of reasons for allowable subject matter:

3. Referring to claim 1, the Billey et al reference (EP 1526643 A1) discloses an output stage adapted to operate in at least a first operating state and a second operating state. The Billey et al reference taken alone or in combination with another, do not disclose, teach or fairly suggest the output stage as a whole comprising: a first, a second, a third and a fourth configurable input/output terminals; and, a first, a second, a third and a fourth switches, each having a first main terminal, a second main terminal and a control terminal, the control terminal being adapted to receive a control signal for controlling the open or closed state of the switch; wherein, the first input/output terminal is connected to the first main terminal of the first switch; the second input/output terminal is connected to the first main terminal of the second switch; the second main terminal of the first switch is connected to the first main terminal of the third switch through a first branch, the second main terminal of the second switch is connected to the first main terminal of the fourth switch through a second branch; the third input/output terminal is connected to the first branch and the fourth input/output terminal is connected to the second branch; the second main terminals of the third and fourth switches are both connected to a common node receiving a reference potential; and,

wherein, when the first and second input/output terminals are configured to operate as input terminals, the third and fourth input/output terminals are configured to operate as output terminals; and, when the first and second input/output terminals are configured to operate as output terminals, the third and fourth input/output terminals are configured to operate as input terminals; and, wherein, in the first operating state, the output stage is arranged in a first electrical configuration; and in the second operating state wherein the output stage is arranged in a second electrical configuration different from the first configuration as recited in claim 1. Specifically, Billey et al fails to disclose wherein, when the first and second input/output terminals are configured to operate as input terminals, the third and fourth input/output terminals are configured to operate as output terminals; and, when the first and second input/output terminals are configured to operate as output terminals, the third and fourth input/output terminals are configured to operate as input terminals.

4. Claims 8, 10, 13-15 are allowed for the same reason as claim 1.

5. Claims 2-7 depend on claim 1. Claims 9 & 12 depend on claim 8. Claim 11 depends on claim 10.

6.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled “Comments on Statement of Reasons for Allowance.”

Contact

Any inquiry concerning this communication or earlier communications from the examiner should be directed to GEORGE MONIKANG whose telephone number is (571)270-1190. The examiner can normally be reached on 9:00-5:00 EST Monday-Friday, Alt Friday off.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Duc Nguyen can be reached on 571-272-7503. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/GEORGE MONIKANG/

Primary Examiner, Art Unit 2651 2/17/17

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14889892	SIRITO-OLIVIER ET AL.
	Examiner	**Art Unit**
	GEORGE MONIKANG	2651

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	02/17/2017								
1	1	=								
2	2	=								
3	3	=								
4	4	=								
5	5	=								
6	6	=								
7	7	=								
8	8	=								
9	9	=								
11	10	=								
12	11	=								
10	12	=								
13	13	=								
14	14	=								
15	15	=								

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
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	GEORGE MONIKANG	2651

CPC						
Symbol					**Type**	**Version**
H02M		3	/	158	F	2013-01-01
H03F		3	/	2173	I	2013-01-01
H03F		3	/	2175	I	2013-01-01
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CPC Combination Sets							
Symbol					**Type**	**Set**	**Ranking**	**Version**
			/					
			/					

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	15	
/GEORGE MONIKANG/ Primary Examiner.Art Unit 2651	2/17/2017	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	fig. 2

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14889892	SIRITO-OLIVIER ET AL.
	Examiner	**Art Unit**
	GEORGE MONIKANG	2651

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION												
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED							
381	85	H	0	4	R	27 / 00 (2006.01.01)								
CROSS REFERENCE(S)		H	0	4	R	3 / 12 (2006.01.01)								
		H	0	4	R	5 / 04 (2006.01.01)								

CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
381	80	81	84	28	

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	15	
/GEORGE MONIKANG/ Primary Examiner.Art Unit 2651	2/17/2017	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	fig. 2

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
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	Examiner	**Art Unit**
	GEORGE MONIKANG	2651

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
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5	5														
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13	13														
14	14														
15	15														

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	15	
/GEORGE MONIKANG/ Primary Examiner.Art Unit 2651	2/17/2017	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	fig. 2

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	323	(switch$3 with output with configuration) and 381/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2017/02/17 11:28
L2	87	1 AND ((H04R5/04 OR H04R1/1041 OR H04R2420/03 OR H04R2420/01 OR G10K11/1786 OR H03F3/217 OR H03F3/2173 OR H03F2200/249 OR H03F2200/414 OR H03F3/2178 OR H03F2203/7231).CPC.)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2017/02/17 11:36
L3	21	(switch same input same output same terminal$1 same branch same potential same reference same branch).clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2017/02/17 12:07
L4	2	(switch same input same output same terminal$1 same branch same potential same reference same main).clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2017/02/17 12:07
L5	1	(switch same input same output same terminal$1 same branch same potential same reference same main same first same second same third same fourth).clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2017/02/17 12:07
S1	1	"14889892"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2017/02/16 08:45
S2	11	"1526643"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2017/02/16 09:12
S3	56	"369954"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2017/02/16 09:15
S5	0	sirito-olivier-philippe$,in.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2017/02/16 13:30
S6	51	sirito-olivier-philippe$.in.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2017/02/16 13:31
S7	48	milazzo-patrizia$.in.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2017/02/16 13:39
S8	48	nagari-angelo$.in.	US-PGPUB; USPAT; EPO; JPO;	OR	OFF	2017/02/16 13:43

			DERWENT			
S9	5	"20100048256"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2017/02/16 13:50
S10	3	"20130051601"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2017/02/16 13:50
S11	2	"20060116111"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2017/02/16 13:50
S12	3	"20090226013"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2017/02/16 14:06
S13	2	(switch$3 with input with output with exchange) and 381/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2017/02/16 21:39
S14	3750	(switch$3 with input with output) and 381/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2017/02/16 21:46
S15	0	(switch$3 with input with output with when) and 381/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2017/02/16 21:46
S16	400	(switch$3 with input with output with configur$5) and 381/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2017/02/16 21:46

2/ 17/ 2017 12:36:23 PM
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PTO/SB/08a (03-15)
Approved for use through 07/31/2016. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	14/889,892
Filing Date	2015-11-09
First Named Inventor	Philippe SIRITO-OLIVIER
Art Unit	TBD
Examiner Name	TBD
Attorney Docket Number	0112-301/C03308 US1

U.S.PATENTS Remove

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
/G.C.M/	1	1 526 643	EP	A1	2005-04-27	Hewlett-Packard Development Company, L.P.		☐
/G.C.M/	2	0 369 954	EP	A1	1990-05-23	SGS-Thomson Microelectronics s.r.l.		☐

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Application Number	14/889,892
Filing Date	2015-11-09
First Named Inventor	Philippe SIRITO-OLIVIER
Art Unit	TBD
Examiner Name	TBD
Attorney Docket Number	0112-301/C03308 US1

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
/G.C.M/	1	International Search Report issued in corresponding International application no. PCT/EP2014/061350, date of completion of the International search June 30, 2014.	☐
/G.C.M/	2	Written Opinion of the International Searching Authority issued in corresponding International application no. PCT/EP2014/061350, date of mailing July 7, 2014.	☐
/G.C.M/	3	Extended European Search Report issued in corresponding European patent application no. EP 13 30 5740, date of completion of the report September 6, 2013.	☐

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Examiner Signature	/GEORGE C MONIKANG/	Date Considered	02/16/2017

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[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14/889,892
	Filing Date	2015-11-09
	First Named Inventor	Philippe SIRITO-OLIVIER
	Art Unit	TBD
	Examiner Name	TBD
	Attorney Docket Number	0112-301/C03308 US1

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/stevenmdubois/	Date (YYYY-MM-DD)	2015-11-09
Name/Print	Steven M. duBois	Registration Number	35,023

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14889892	SIRITO-OLIVIER ET AL.
	Examiner	**Art Unit**
	GEORGE MONIKANG	2651

CPC- SEARCHED		
Symbol	**Date**	**Examiner**
H04R5/04; H04R1/1041; H04R2420/03; H04R2420/01; G10K11/1786; H03F3/217; H03F3/2173	2/17/2017	GM
H03F2200/249; H03F2200/414; H03F3/2178; H03F2203/7231	2/17/2017	GM

CPC COMBINATION SETS - SEARCHED		
Symbol	**Date**	**Examiner**

US CLASSIFICATION SEARCHED			
Class	**Subclass**	**Date**	**Examiner**
381	28, 80-81, 84-85	2/17/2017	GM

SEARCH NOTES		
Search Notes	**Date**	**Examiner**
No double patenting issues. Inventor search completed in EAST.	2/17/2017	GM

INTERFERENCE SEARCH			
US Class/ CPC Symbol	**US Subclass / CPC Group**	**Date**	**Examiner**
	Interference search completed in EAST.	2/17/2017	GM
	Same class/subclass as above.	2/17/2017	GM

2/17/2017	/GEORGE MONIKANG/ Primary Examiner.Art Unit 2651

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BIB DATA SHEET

CONFIRMATION NO. 9535

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
14/889,892	11/09/2015 RULE	381	2651	2000-1043US1

APPLICANTS

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INVENTORS

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Patrizia MILAZZO, S. Agata Li Battiati, ITALY;
Angelo NAGARI, Grenoble, FRANCE;

**** CONTINUING DATA ***************************

This application is a 371 of PCT/EP2014/061350 06/02/2014

**** FOREIGN APPLICATIONS ***************************

EUROPEAN PATENT OFFICE (EPO) 13305740.6 06/03/2013

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

01/18/2016

Foreign Priority claimed	35 USC 119(a-d) conditions met	Verified and Acknowledged		STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
☑ Yes ☐ No	☑ Yes ☐ No	/GEORGE C MONIKANG/ Examiner's Signature	☑ Met after Allowance G.M. Initials	FRANCE	4	15	1

ADDRESS

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DALLAS, TX 75206
UNITED STATES

TITLE

Reconfigurable Output Stage

FILING FEE RECEIVED		
1620	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s):	SIRITO-OLIVIER et al.	§ Group Art Unit:	2651
Application No:	14/889,892	§ Examiner:	George C. Monikang
Filed:	November 9, 2015	§ Confirmation No:	9535

Attorney Docket No: 2000-1043US1
Customer No.: 28240

For: **RECONFIGURABLE OUTPUT STAGE**

Mail Stop Issue Fee
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Date: May 10, 2017

Name: Meredith Burmaster

Signature: /Meredith Burmaster/

Dear Examiner:

AMENDMENT UNDER 37 C.F.R. § 1.312

Applicant submits this amendment under 37 C.F.R. § 1.312 prior to payment of the Issue Fee in respect of the above-captioned patent Application. Entry of the amendments is respectfully requested.

1. **Listing of Claims begins on page 2 of this paper.**

2. **Remarks begin on page 20 of this paper.**

LISTING OF THE CLAIMS PER 37 C.F.R. § 1.121

1. (Previously Presented) An output stage adapted to operate in at least a first operating state and a second operating state, the output stage comprising:

a first, a second, a third and a fourth configurable input/output terminals; and,

a first, a second, a third and a fourth switches, each having a first main terminal, a second main terminal and a control terminal, the control terminal being adapted to receive a control signal for controlling the open or closed state of the switch,

wherein,

the first input/output terminal is connected to the first main terminal of the first switch;

the second input/output terminal is connected to the first main terminal of the second switch;

the second main terminal of the first switch is connected to the first main terminal of the third switch through a first branch,

the second main terminal of the second switch is connected to the first main terminal of the fourth switch through a second branch;

the third input/output terminal is connected to the first branch and the fourth input/output terminal is connected to the second branch;

the second main terminals of the third and fourth switches are both connected to a common node receiving a reference potential; and,

wherein,

when the first and second input/output terminals are configured to operate as input terminals, the third and fourth input/output terminal are configured to operate as output terminals; and,

when the first and second input/output terminals are configured to operate as output terminals, the third and fourth input/output terminals are configured to operate as input terminals; and,

wherein,

in the first operating state, the output stage is arranged in a first electrical configuration; and

in the second operating state wherein the output stage is arranged in a second electrical configuration different from the first configuration.

2. (Previously Presented) The output stage of claim 1, wherein, in the first operating state:

the first and second input/output terminals are configured to operate as input terminals and are configured to be connected to a common node receiving a supply potential; and

the third and fourth input/output terminals are configured to be connected to a load element.

3. (Currently Amended) The output stage of claim 1 further comprising an inductor and a decoupling capacitor, wherein, in the second operating state:

the first and second input/output terminals are configured to operate as output terminals and are configured to be connected, in series with a load element and in parallel with the decoupling capacitor;

the third and fourth input/output terminals are short-circuited; and

one end of the inductor is configured to be connected to the short-circuited third and fourth input/output terminals, and another end of the inductor is configured to be connected to a common node receiving a supply potential.

4. (Currently Amended) The output stage of claim 1 further comprising an inductor and a decoupling capacitor, wherein, in the second operating state:

the first and second input/output terminals are configured to operate as input terminals and are configured to be connected to a common node receiving a supply potential;

the third and fourth input/output terminals are short-circuited; and

one end of the inductor is configured to be connected to the short-circuited third and fourth input/output terminals, and another end of the inductor is configured to be connected, in series with a load element and in parallel with the decoupling capacitor.

5. (Previously Presented) The output stage of claim 1 further comprising a first and second inductors and a first and second decoupling capacitors, wherein, in the second operating state:

the first and second input/output terminals are configured to operate as output terminals;

the first input/output terminal is configured to be connected, in series with a first load element and in parallel with the first decoupling capacitor;

the second input/output terminal is configured to be connected, in series with a second load element and in parallel with the second decoupling capacitor;

one end of the first inductor is configured to be connected to the third input/output terminal, and another end of the first inductor is configured to be connected to a common node receiving a supply potential; and

one end of the second inductor is configured to be connected to the fourth input/output terminal, and another end of the second inductor is configured to be connected to the common node receiving a supply potential;

6. (Previously Presented) The output stage of claim 1 further comprising a first and second inductors, and a first and second decoupling capacitors, wherein, in the second operating state:

the first and second input/output terminals are configured to operate as input terminals and are configured to be connected to a common node receiving a supply potential;

one end of the first inductor is configured to be connected to the third input/output terminal, and another end of the first inductor is configured to be connected, in series with a first load element and in parallel with the first decoupling capacitor; and

one end of the second inductor is configured to be connected the fourth input/output terminal, and another end of the second inductor is configured to be

connected, in series with a second load element and in parallel with the second decoupling capacitor.

7. (Previously Presented) The output stage of claim 1 further comprising a first and second inductors and a first and second decoupling capacitors, wherein, in the second operating state:

the first and second input/output terminals are configured to operate as input terminals;

the third input/output terminal is configured to be connected, in series with a first load element and in parallel with the first decoupling capacitor;

one end of the first inductor is configured to be connected to the first input/output terminal, and another end of the first inductor is configured to be connected to a first node receiving a supply potential; and

one end of the second inductor is configured to be connected to the fourth input/output terminal, and another end of the second inductor is configured to be connected, in series with a second load element and in parallel with the second decoupling capacitor.

8. (Currently Amended) A control apparatus comprising:

a control stage configured to control an output stage adapted to operate in at least a first operating state and a second operating state, the output stage including: ~~according to claim 2.~~

a first, a second, a third and a fourth configurable input/output terminals; and,

a first, a second, a third and a fourth switches, each having a first main terminal, a second main terminal and a control terminal, the control terminal being adapted to receive a control signal for controlling the open or closed state of the switch,

wherein,

the first input/output terminal is connected to the first main terminal of the first switch;

the second input/output terminal is connected to the first main terminal of the second switch;

the second main terminal of the first switch is connected to the first main terminal of the third switch through a first branch,

the second main terminal of the second switch is connected to the first main terminal of the fourth switch through a second branch;

the third input/output terminal is connected to the first branch and the fourth input/output terminal is connected to the second branch;

the second main terminals of the third and fourth switches are both connected to a common node receiving a reference potential; and,

wherein,

when the first and second input/output terminals are configured to operate as input terminals, the third and fourth input/output terminal are configured to operate as output terminals; and,

when the first and second input/output terminals are configured to operate as output terminals, the third and fourth input/output terminals are configured to operate as input terminals; and,

wherein,

in the first operating state, the output stage is arranged in a first electrical configuration; and

in the second operating state wherein the output stage is arranged in a second electrical configuration different from the first configuration,

and

further wherein, in the first operating state,

the first and second input/output terminals are configured to operate as input terminals and are configured to be connected to a common node receiving a supply potential; and

the third and fourth input/output terminals are configured to be connected to a load element.

9. (Original) The control apparatus of claim 8 wherein the control stage is a Class-D control stage.

10. (Currently Amended) A control apparatus comprising:

a control stage configured to control an output stage adapted to operate in at least a first operating state and a second operating state, the output stage including: ~~according to claim 3.~~

a first, a second, a third and a fourth configurable input/output terminals; and,

a first, a second, a third and a fourth switches, each having a first main terminal, a second main terminal and a control terminal, the control terminal being adapted to receive a control signal for controlling the open or closed state of the switch,

wherein,

the first input/output terminal is connected to the first main terminal of the first switch;

the second input/output terminal is connected to the first main terminal of the second switch;

the second main terminal of the first switch is connected to the first main terminal of the third switch through a first branch,

the second main terminal of the second switch is connected to the first main terminal of the fourth switch through a second branch;

the third input/output terminal is connected to the first branch and the fourth input/output terminal is connected to the second branch;

the second main terminals of the third and fourth switches are both connected to a common node receiving a reference potential; and,

wherein,

when the first and second input/output terminals are configured to operate as input terminals, the third and fourth input/output terminal are configured to operate as output terminals; and,

when the first and second input/output terminals are configured to operate as output terminals, the third and fourth input/output terminals are configured to operate as input terminals; and,

wherein,

in the first operating state, the output stage is arranged in a first electrical configuration; and

in the second operating state wherein the output stage is arranged in a second electrical configuration different from the first configuration, and,

the output stage further comprising an inductor and a decoupling capacitor,

and wherein, in the second operating state:

the first and second input/output terminals are configured to operate as output terminals and are configured to be connected, in series with a load element and in parallel with the decoupling capacitor;

the third and fourth input/output terminals are short-circuited; and

one end of the inductor is configured to be connected to the short-circuited third and fourth input/output terminals, and another end of the inductor is configured to be connected to a common node receiving a supply potential.

11. (Original) The control apparatus of claim 10 wherein the control stage is a DC-DC converter stage.

12. (Previously Presented) The control apparatus of claim 8, wherein the control stage is adapted to control the output stage by generating control signals for controlling the first, second, third and fourth switches through their respective control terminals.

13. (Currently Amended) A circuit comprising:

an output stage adapted to operate in at least a first operating state and a second operating state, the output stage including: ~~according to claim 2;~~

a first, a second, a third and a fourth configurable input/output terminals; and,

a first, a second, a third and a fourth switches, each having a first main terminal, a second main terminal and a control terminal, the control terminal being adapted to receive a control signal for controlling the open or closed state of the switch,

wherein,

the first input/output terminal is connected to the first main terminal of the first switch;

the second input/output terminal is connected to the first main terminal of the second switch;

the second main terminal of the first switch is connected to the first main terminal of the third switch through a first branch,

the second main terminal of the second switch is connected to the first main terminal of the fourth switch through a second branch;

the third input/output terminal is connected to the first branch and the fourth input/output terminal is connected to the second branch;

the second main terminals of the third and fourth switches are both connected to a common node receiving a reference potential; and,

wherein,

when the first and second input/output terminals are configured to operate as input terminals, the third and fourth input/output terminal are configured to operate as output terminals; and,

when the first and second input/output terminals are configured to operate as output terminals, the third and fourth input/output terminals are configured to operate as input terminals; and,

wherein,

in the first operating state, the output stage is arranged in a first electrical configuration; and

in the second operating state wherein the output stage is arranged in a second electrical configuration different from the first configuration,

and,

further wherein, in the first operating state,

the first and second input/output terminals are configured to operate as input terminals and are configured to be connected to a common node receiving a supply potential; and

the third and fourth input/output terminals are configured to be connected to a load element;

a first control apparatus wherein [[the]] a control stage of the first control apparatus is connected to the output stage; and,

a second control apparatus wherein [[the]] a control stage of the second control apparatus is connected to the output stage;

wherein,

when the control stage of the first control apparatus is connected to the output stage, the control stage of the second control apparatus is electrically disconnected from the output stage, the output stage being configured to operate in the first operating state; and,

when the control stage of the second control apparatus is connected to the output stage, the control stage of the first control apparatus is electrically disconnected from the output stage, the output stage being configured to operate in the second operating state.

14. (Currently Amended) A device comprising:

a [[the]] circuit ~~of claim 12;~~ comprising a control apparatus that includes a control stage configured to control an output stage adapted to operate in at least a first operating state and a second operating state, the output stage including:

a first, a second, a third and a fourth configurable input/output terminals; and,

a first, a second, a third and a fourth switches, each having a first main terminal, a second main terminal and a control terminal, the control terminal being adapted to receive a control signal for controlling the open or closed state of the switch,

wherein,

the first input/output terminal is connected to the first main terminal of the first switch;

the second input/output terminal is connected to the first main terminal of the second switch;

the second main terminal of the first switch is connected to the first main terminal of the third switch through a first branch,

the second main terminal of the second switch is connected to the first main terminal of the fourth switch through a second branch;

the third input/output terminal is connected to the first branch and the fourth input/output terminal is connected to the second branch;

the second main terminals of the third and fourth switches are both connected to a common node receiving a reference potential; and,

wherein,

when the first and second input/output terminals are configured to operate as input terminals, the third and fourth input/output terminal are configured to operate as output terminals; and,

when the first and second input/output terminals are configured to operate as output terminals, the third and fourth input/output terminals are configured to operate as input terminals; and,

wherein,

in the first operating state, the output stage is arranged in a first electrical configuration; and

in the second operating state wherein the output stage is arranged in a second electrical configuration different from the first configuration,

and,

further wherein, in the first operating state,

the first and second input/output terminals are configured to operate as input terminals and are configured to be connected to a common node receiving a supply potential; and

the third and fourth input/output terminals are configured to be connected to a load element, and

wherein the control stage is adapted to control the output stage by generating control signals for controlling the first, second, third and fourth switches through their respective control terminals;

a battery configured to be connected to the input terminals of the circuit; and[[,]]

a loudspeaker configured to be connected to the output terminals of the circuit.

15. (Currently Amended) An apparatus comprising:

an output stage adapted to operate in at least a first operating state and a second operating state, the output stage including: ~~according to claim 2 connected to,~~

a first, a second, a third and a fourth configurable input/output terminals; and,

a first, a second, a third and a fourth switches, each having a first main terminal, a second main terminal and a control terminal, the control terminal being adapted to receive a control signal for controlling the open or closed state of the switch,

wherein,

the first input/output terminal is connected to the first main terminal of the first switch;

the second input/output terminal is connected to the first main terminal of the second switch;

the second main terminal of the first switch is connected to the first main terminal of the third switch through a first branch,

the second main terminal of the second switch is connected to the first main terminal of the fourth switch through a second branch;

the third input/output terminal is connected to the first branch and the fourth input/output terminal is connected to the second branch;

the second main terminals of the third and fourth switches are both connected to a common node receiving a reference potential; and,

wherein,

when the first and second input/output terminals are configured to operate as input terminals, the third and fourth input/output terminal are configured to operate as output terminals; and,

when the first and second input/output terminals are configured to operate as output terminals, the third and fourth input/output terminals are configured to operate as input terminals; and,

wherein,

in the first operating state, the output stage is arranged in a first electrical configuration; and

in the second operating state wherein the output stage is arranged in a second electrical configuration different from the first configuration,

and

further wherein, in the first operating state,

the first and second input/output terminals are configured to operate as input terminals and are configured to be connected to a common node receiving a supply potential; and

the third and fourth input/output terminals are configured to be connected to a load element, and

the output stage connected to:

a first control apparatus, a control stage of the first control apparatus being connected to the output stage; or to

a second control apparatus, a control stage of the second control apparatus being connected to the output stage;

wherein,

when the control stage of the first control apparatus is connected to the output stage, the control stage of the second control apparatus is electrically disconnected from the output stage, the output stage being configured to operate in the first operating state; and,

when the control stage of the second control apparatus is connected to the output stage, the control stage of the first control apparatus is electrically disconnected from the output stage, the output stage being configured to operate in the second operating state.

REMARKS

Claims 1-15 are currently pending, of which claims 1, 8, 10, 13-15 are in independent form.

Claims 3, 4, 8, 10 and 13-15 are proposed to be amended as set forth above to address minor formalities as well as to remove claim dependency with respect to certain claims. In particular, claim 8 has been rewritten in independent form to explicitly recite the features of claims 1 and 2 referenced in the previous version. Likewise, claim 10 has been rewritten in independent form to explicitly recite the features of claims 1 and 3; claim 13 has been rewritten in independent form to explicitly recite the features of claims 1 and 2; claim 14 has been rewritten in independent form to explicitly recite the features of claims 1, 2 and 12; and claim 15 has been rewritten in independent form to explicitly recite the features of claims 1 and 2.

No new matter has been introduced hereby.

Applicant respectfully submits that the proposed amendments set forth in the instant paper require no substantial amount of additional work on the part of the Patent Office as the scope of pending claims has not changed and no additional search or examination is warranted.

Entry of the amendments is therefore respectfully requested.

Fee Statement

Compared to the highest number previously paid for, the total number of claims has not changed whereas the number of independent claims has increased by three. Applicable fees are therefore being paid via EFS-Web. Applicant believes no additional fees are due for the filing of this Rule 312 amendment. If any fees are due, however, please charge our deposit account (Deposit Account No. 03-1130).

SUMMARY AND CONCLUSION

Applicant respectfully requests entry of the foregoing amendments prior to issuance of the present application.

Applicant requests a telephonic interview if the Examiner has any questions or requires any additional information with respect to the instant paper.

Respectfully submitted,

Dated: May 10th, 2017

Shreen K. Danamraj
Registration No. 41,696

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Fax (214) 363-8177

Electronic Patent Application Fee Transmittal

Application Number:	14889892
Filing Date:	09-Nov-2015
Title of Invention:	Reconfigurable Output Stage
First Named Inventor/Applicant Name:	Philippe SIRITO-OLIVIER
Filer:	Shreen K. Danamraj/Meredith Burmaster
Attorney Docket Number:	2000-1043US1

Filed as Large Entity

Filing Fees for U.S. National Stage under 35 USC 371

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
INDEPENDENT CLAIMS IN EXCESS OF 3	1614	3	420	1260
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**1260**

Electronic Acknowledgement Receipt

EFS ID:	29174412
Application Number:	14889892
International Application Number:	
Confirmation Number:	9535
Title of Invention:	Reconfigurable Output Stage
First Named Inventor/Applicant Name:	Philippe SIRITO-OLIVIER
Customer Number:	28240
Filer:	Shreen K. Danamraj/Meredith Burmaster
Filer Authorized By:	Shreen K. Danamraj
Attorney Docket Number:	2000-1043US1
Receipt Date:	10-MAY-2017
Filing Date:	09-NOV-2015
Time Stamp:	16:32:55
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$1260
RAM confirmation Number	051117INTEFSW16360900
Deposit Account	031130
Authorized User	Shreen Danamraj

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	QE1541US1_Transmittal_Letter.pdf	101953 dd8a2d217bc52c4d66b8faddc1af0b1e7f1bb160	no	1
Warnings:					
Information:					
2	Amendment after Notice of Allowance (Rule 312)	QE1541US1_Rule_312_Post-Allowance_Amendment.pdf	2547225 d183371d353721377ddcf1d355028e16c57cfc76	no	22
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	31007 4f9adadbf49d3c3ae9b8afb62c7355e516a673eb	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	2680185		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

THE DANAMRAJ LAW GROUP, P.C.

ATTORNEYS AND COUNSELORS
INTELLECTUAL PROPERTY LAW AND RELATED MATTERS

THE TURLEY LAW CENTER, SUITE 810
6440 NORTH CENTRAL EXPRESSWAY
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SHREEN K. DANAMRAJ
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(214) 750-5666 (tel)
(214) 363-8177 (fax)
shreen@danamraj.com

May 10, 2017

Electronic Filing:

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313 -1450

Re: Application No.: 14/889,892
Reconfigurable Output Stage
Confirmation No.: 9535
Our File: 2000-1043US1

Dear Sir:

Enclosed for filing please find the following item(s) relating to the above-identified application:

(1) Amendment Under 37 C.F.R. § 1.312.

Charge Statement
No/additional fees are believed to be due for the filing of the attached paper(s). However, if any (additional) fees are due, or any overpayments have been made, please charge, or credit, Deposit Account 03-1130.

If you have any questions or comments concerning this matter, please call the undersigned at your earliest convenience. Otherwise, please accept the enclosed.

Sincerely,

Shreen K. Danamraj
Reg. No. 41,696

Enclosures

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/889,892	11/09/2015	Philippe SIRITO-OLIVIER	2000-1043US1	9535

28240 7590 05/30/2017

THE DANAMRAJ LAW GROUP, P.C.
TURLEY LAW CENTER, SUITE 810
6440 N. CENTRAL EXPRESSWAY
DALLAS, TX 75206

EXAMINER
MONIKANG, GEORGE C

ART UNIT	PAPER NUMBER
2651	

NOTIFICATION DATE	DELIVERY MODE
05/30/2017	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

SHREEN@DANAMRAJ.COM
Betty@DANAMRAJ.COM
dlg-admin@DANAMRAJ.COM

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

DETAILED ACTION

Allowable Subject Matter

1. Claims 1-15 are allowed.

2. The following are examiner's statement of reasons for allowable subject matter:

3. Referring to claim 1, the Billey et al reference (EP 1526643 A1) discloses an output stage adapted to operate in at least a first operating state and a second operating state. The Billey et al reference taken alone or in combination with another, do not disclose, teach or fairly suggest the output stage as a whole comprising: a first, a second, a third and a fourth configurable input/output terminals; and, a first, a second, a third and a fourth switches, each having a first main terminal, a second main terminal and a control terminal, the control terminal being adapted to receive a control signal for controlling the open or closed state of the switch; wherein, the first input/output terminal is connected to the first main terminal of the first switch; the second input/output terminal is connected to the first main terminal of the second switch; the second main terminal of the first switch is connected to the first main terminal of the third switch through a first branch, the second main terminal of the second switch is connected to the first main terminal of the fourth switch through a second branch; the third input/output terminal is connected to the first branch and the fourth input/output terminal is connected to the second branch; the second main terminals of the third and fourth switches are both connected to a common node receiving a reference potential; and,

wherein, when the first and second input/output terminals are configured to operate as input terminals, the third and fourth input/output terminals are configured to operate as output terminals; and, when the first and second input/output terminals are configured to operate as output terminals, the third and fourth input/output terminals are configured to operate as input terminals; and, wherein, in the first operating state, the output stage is arranged in a first electrical configuration; and in the second operating state wherein the output stage is arranged in a second electrical configuration different from the first configuration as recited in claim 1. Specifically, Billey et al fails to disclose wherein, when the first and second input/output terminals are configured to operate as input terminals, the third and fourth input/output terminals are configured to operate as output terminals; and, when the first and second input/output terminals are configured to operate as output terminals, the third and fourth input/output terminals are configured to operate as input terminals.

4. Claims 8, 10, 13-15 are allowed for the same reason as claim 1.

5. Claims 2-7 depend on claim 1. Claims 9 & 12 depend on claim 8. Claim 11 depends on claim 10.

6.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled “Comments on Statement of Reasons for Allowance.”

Response to Rule 312 Communication	Application No.	Applicant(s)
	14/889,892	SIRITO-OLIVIER ET AL.
	Examiner	Art Unit
	GEORGE MONIKANG	2651

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address –

1. ☒ The amendment filed on *10 May 2017* under 37 CFR 1.312 has been considered, and has been:

a) ☐ entered.

b) ☒ entered as directed to matters of form not affecting the scope of the invention.

c) ☐ disapproved because the amendment was filed after the payment of the issue fee.
Any amendment filed after the date the issue fee is paid must be accompanied by a petition under 37 CFR 1.313(c)(1) and the required fee to withdraw the application from issue.

d) ☐ disapproved. See explanation below.

e) ☐ entered in part. See explanation below.

/GEORGE MONIKANG/
Primary Examiner, Art Unit 2651

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

28240 7590 03/06/2017
THE DANAMRAJ LAW GROUP, P.C.
TURLEY LAW CENTER, SUITE 810
6440 N. CENTRAL EXPRESSWAY
DALLAS, TX 75206

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited [illegible] transmitted to the USPTO (571) 273-2885, on the date indicated below. via EFS Web

Meredith Burmaster	(Depositor's name)
Meredith Burmaster	(Signature)
June 1, 2017	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/889,892	11/09/2015	Philippe SIRITO-OLIVIER	2000-1043US1	9535

TITLE OF INVENTION: Reconfigurable Output Stage

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	06/06/2017

EXAMINER	ART UNIT	CLASS-SUBCLASS
MONIKANG, GEORGE C	2651	381-120000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 The Danamraj Law Group , P.C.
2 Thomas L. Crisman
3 Kenneth A. McClure

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: OPTIS CIRCUIT TECHNOLOGY, LLC

(B) RESIDENCE: (CITY and STATE OR COUNTRY): PLANO, TX

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
☒ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
☐ A check is enclosed.
☒ Payment by credit card. [illegible] is attached.
☒ The director is hereby authorized to charge [illegible], any deficiency, or credits any overpayment, to Deposit Account Number 03-1130 [illegible]

5. **Change in Entity Status** (from status indicated above)
☐ Applicant certifying micro entity status. See 37 CFR 1.29
NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
☐ Applicant asserting small entity status. See 37 CFR 1.27
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
☐ Applicant changing to regular undiscounted fee status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date June 1, 2017

Typed or printed name Shreen K. Danamraj Registration No. 41,696

Electronic Patent Application Fee Transmittal

Application Number:	14889892
Filing Date:	09-Nov-2015
Title of Invention:	Reconfigurable Output Stage
First Named Inventor/Applicant Name:	Philippe SIRITO-OLIVIER
Filer:	Shreen K. Danamraj/Meredith Burmaster
Attorney Docket Number:	2000-1043US1

Filed as Large Entity

Filing Fees for U.S. National Stage under 35 USC 371

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	960	960

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**960**

Electronic Acknowledgement Receipt

EFS ID:	29372336
Application Number:	14889892
International Application Number:	
Confirmation Number:	9535
Title of Invention:	Reconfigurable Output Stage
First Named Inventor/Applicant Name:	Philippe SIRITO-OLIVIER
Customer Number:	28240
Filer:	Shreen K. Danamraj/Meredith Burmaster
Filer Authorized By:	Shreen K. Danamraj
Attorney Docket Number:	2000-1043US1
Receipt Date:	01-JUN-2017
Filing Date:	09-NOV-2015
Time Stamp:	16:42:16
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$960
RAM confirmation Number	060217INTEFSW16451400
Deposit Account	031130
Authorized User	Shreen Danamraj

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	QE1541US1_Part_B_Transmittal.pdf	263031 25bf95aee8c65a4892f8cedca73376662537b6f2	no	1
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30956 cb14406989c507688a1f942e542bf971ff4b5165	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	293987		

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New Applications Under 35 U.S.C. 111

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New International Application Filed with the USPTO as a Receiving Office

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/889,892	07/11/2017	9705400	2000-1043US1	9535

28240 7590 06/21/2017

THE DANAMRAJ LAW GROUP, P.C.
TURLEY LAW CENTER, SUITE 810
6440 N. CENTRAL EXPRESSWAY
DALLAS, TX 75206

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 24 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Philippe SIRITO-OLIVIER, Saint Egreve, FRANCE;
Optis Circuit Technology, LLC, Plano, TX;
Patrizia MILAZZO, S. Agata Li Battiati, ITALY;
Angelo NAGARI, Grenoble, FRANCE;