Application Note
APT0201 Rev. B
July 1, 2002

IGBT Tutorial

Jonathan Dodge, P.E.
Senior Applications Engineer

John Hess
Vice President, Marketing

Advanced Power Technology
405 S.W. Columbia Street
Bend, OR 97702

Introduction

With the combination of an easily driven MOS gate and low conduction loss, IGBTs quickly displaced power bipolar transistors as the device of choice for high current and high voltage applications. The balance in tradeoffs between switching speed, conduction loss, and ruggedness is now being ever finely tuned so that IGBTs are encroaching upon the high frequency, high efficiency domain of power MOSFETs. In fact, the industry trend is for IGBTs to replace power MOSFETs except in very low current applications. To help understand the tradeoffs and to help circuit designers with IGBT device selection and application, this application note provides a relatively painless overview of IGBT technology and a walkthrough of Advanced Power Technology IGBT datasheet information.

How to Select an IGBT

This section is intentionally placed before the technical discourse. Answers to the following set of burning questions will help determine which IGBT is appropriate for a particular application. The differences between Non Punch-Through (NPT) and Punch-Through (PT) devices as well as terms and graphs will be explained later.

1. What is the operating voltage? The highest voltage the IGBT has to block should be no more than 80% of the V_{CES} rating.
2. Is it hard or soft switched? A PT device is better suited for soft switching due to reduced tail current, however a NPT device will also work.
3. What is the current that will flow through the device? The first two numbers in the part number give a rough indication of the usable current. For hard switching applications, the usable frequency versus current graph is helpful in determining whether a device will fit the application. Differences between datasheet test conditions and the application should be taken into account, and an example of how to do this will be given later. For soft switching applications, the I_{C2} rating could be used as a starting point.
4. What is the desired switching speed? If the answer is "the higher, the better", then a PT device is the best choice. Again, the usable frequency versus current graph can help answer this question for hard switching applications.
5. Is short circuit withstand capability required? For applications such as motor drives, the answer is yes, and the switching frequency also tends to be relatively low. An NPT device would be required. Switch mode power supplies often don't require short circuit capability.

IGBT Overview

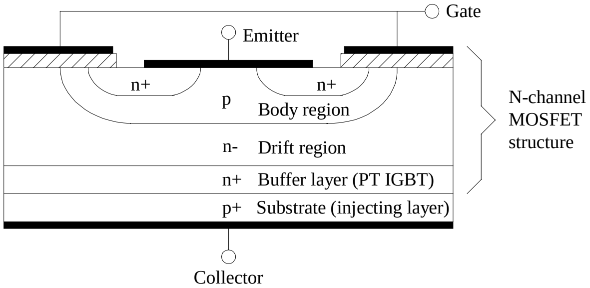

Figure 1 N-Channel IGBT Cross Section

An N-channel IGBT is basically an N-channel power MOSFET constructed on a p-type substrate, as illustrated by the generic IGBT cross section in Figure 1. (PT IGBTs have an additional n+ layer as well as will be explained.) Consequently, operation of an IGBT is very similar to a power MOSFET. A positive voltage applied from the emitter to gate terminals causes electrons to be drawn toward the gate terminal in the body region. If the gate-emitter voltage is at or above what is called the threshold voltage, enough electrons are drawn toward the gate to form a conductive channel across the body region, allowing current to flow from the collector to the emitter. (To be precise, it allows electrons to flow from the emitter to the collector.) This flow of electrons draws positive ions, or holes, from the p-type substrate into the drift region toward the emitter. This leads to a couple of simplified equivalent circuits for an IGBT as shown in Figure 2.

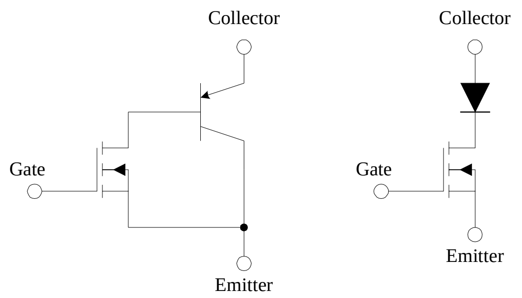

Figure 2 IGBT Simplified Equivalent Circuits

The first circuit shows an N-channel power MOSFET driving a wide base PNP bipolar transistor in a Darlington configuration. The second circuit simply shows a diode in series with the drain of an N-channel power MOSFET. At first glance, it would seem that the on state voltage across the IGBT would be one diode drop higher than for the N-channel power MOSFET by itself. It is true in fact that the on state voltage across an IGBT is always at least one diode drop. However, compared to a power MOSFET of the same die size and operating at the same temperature and current, an IGBT can have significantly lower on state voltage. The reason for this is that a MOSFET is a majority carrier device only. In other words, in an N-channel MOSFET only electrons flow. As mentioned before, the p-type substrate in an N-channel IGBT injects holes into the drift region. Therefore, current flow in an IGBT is composed of both electrons and holes. This injection of holes (minority carriers) significantly reduces the effective resistance to current flow in the drift region. Stated otherwise, hole injection significantly increases the conductivity, or the conductivity is modulated. The resulting reduction in on state voltage is the main advantage of IGBTs over power MOSFETs.

Nothing comes for free of course, and the price for lower on state voltage is slower switching speed, especially at turn-off. The reason for this is that during turn-off the electron flow can be stopped rather abruptly, just as in a power MOSFET, by reducing the gate-emitter voltage below the threshold voltage. However, holes are left in the drift region, and there is no way to remove them except by voltage gradient and recombination. The IGBT exhibits a tail current during turn-off until all the holes are swept out or recombined. The rate of recombination can be controlled, which is the purpose of the n+ buffer layer shown in Figure 1. This buffer layer quickly absorbs trapped holes during turn-off. Not all IGBTs incorporate an n+ buffer layer; those that do are called punch-through (PT), those that do not are called non punch-through (NPT). PT IGBTs are sometimes referred to as asymmetrical, and NPT as symmetrical.

The other price for lower on state voltage is the possibility of latchup if the IGBT is operated well outside the datasheet ratings. Latchup is a failure mode where the IGBT can no longer be turned off by the gate. Latchup can be induced in any IGBT through misuse. Thus the latchup failure mechanism in IGBTs warrants some explanation.

The basic structure of an IGBT resembles a thyristor, namely a series of PNPN junctions. This can be explained by analyzing a more detailed equivalent circuit model for an IGBT shown in Figure 3.

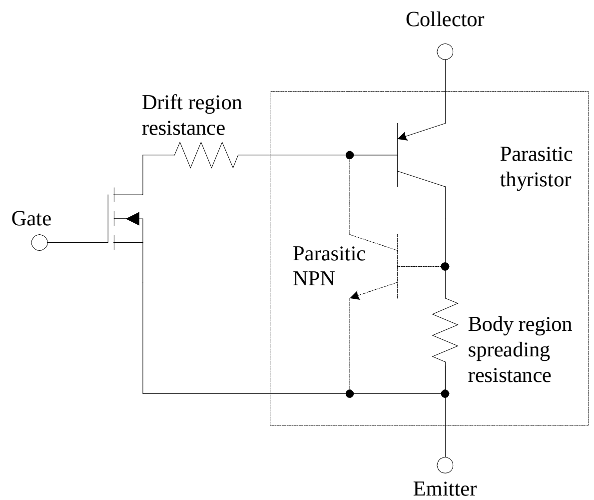

Figure 3 IGBT Model Showing Parasitic Thyristor

A parasitic NPN bipolar transistor exists within all N-channel power MOSFETS and consequently all N-channel IGBTs. The base of this transistor is the body region, which is shorted to the emitter to prevent it from turning on. Note however that the body region has some resistance, called body region spreading resistance, as shown in Figure 3. The P-type substrate and drift and body regions form the PNP portion of the IGBT. The PNPN structure forms a parasitic thyristor. If the parasitic NPN transistor ever turns on and the sum of the gains of the NPN and PNP transistors are greater than one, latchup occurs. Latchup is avoided through design of the IGBT by optimizing the doping levels and geometries of the various regions shown in Figure 1.

The gains of the PNP and NPN transistors are set so that their sum is less than one. As temperature increases, the PNP and NPN gains increase, as well as the body region spreading resistance. Very high collector current can cause sufficient voltage drop across the body region to turn on the parasitic NPN transistor, and excessive localized heating of the die increases the parasitic transistor gains so their sum exceeds one. If this happens, the parasitic thyristor latches on, and the IGBT cannot be turned off by the gate and may be destroyed due to over-current heating. This is static latchup. High dv/dt during turn-off combined with excessive collector current can also effectively increase gains and turn on the parasitic NPN transistor. This is dynamic latchup, which is actually what limits the safe operating area since it can happen at a much lower collector current than static latchup, and it depends on the turn-off dv/dt. By staying within the maximum current and safe operating area ratings, static and dynamic latchup are avoided regardless of turn-off dv/dt. Note that turn-on and turn-off dv/dt, overshoot, and ringing can be set by an external gate resistor (as well as by stray inductance in the circuit layout).

PT versus NPT Technology

Conduction Loss

For a given switching speed, NPT technology generally has a higher $V_{CE(on)}$ than PT technology. This difference is magnified further by fact that $V_{CE(on)}$ increases with temperature for NPT (positive temperature coefficient), whereas $V_{CE(on)}$ decreases with temperature for PT (negative temperature coefficient). However, for any IGBT, whether PT or NPT, switching loss is traded off against $V_{CE(on)}$. Higher speed IGBTs have a higher $V_{CE(on)}$; lower speed IGBTs have a lower $V_{CE(on)}$. In fact, it is possible that a very fast PT device can have a higher $V_{CE(on)}$ than a NPT device of slower switching speed.

Switching Loss

For a given $V_{CE(on)}$, PT IGBTs have a higher speed switching capability with lower total switching energy. This is due to higher gain and minority carrier lifetime reduction, which quenches the tail current.

Ruggedness

NPT IGBTs are typically short circuit rated while PT devices often are not, and NPT IGBTs can absorb more avalanche energy than PT IGBTs. NPT technology is more rugged due to the wider base and lower gain of the PNP bipolar transistor. This is the main advantage gained by trading off switching speed with NPT technology. It is difficult to make a PT IGBT with greater than 600 Volt V_{CES} whereas it is easily done with NPT technology. Advanced Power Technology does offer a series of very fast 1200 Volt PT IGBTs, the Power MOS 7® IGBT series.

Temperature Effects

For both PT and NPT IGBTs, turn-on switching speed and loss are practically unaffected by temperature. Reverse recovery current in a diode however increases with temperature, so temperature effects of an external diode in the power circuit affect IGBT turn-on loss.

For NPT IGBTs, turn-off speed and switching loss remain relatively constant over the operating temperature range. For PT IGBTs, turn-off speed degrades and switching loss consequently increases with temperature. However, switching loss is low to begin with due to tail current quenching.

As mentioned previously, NPT IGBTs typically have a positive temperature coefficient, which makes them well suited for paralleling. A positive temperature coefficient is desirable for paralleling devices because a hot device will conduct less current than a cooler device, so all the parallel devices tend to naturally share current. It is a misconception however that PT IGBTs cannot be paralleled because of their negative temperature coefficient. PT IGBTs can be paralleled because of the following:

- Their temperature coefficients tend to be almost zero and are sometimes positive at higher current.
- Heat sharing through the heat sink tends to force devices to share current because a hot device will heat its neighbors, thus lowering their on voltage.
- Parameters that affect the temperature coefficient tend to be well matched between devices.

IGBTs from Advanced Power Technology

Advanced Power Technology offers three series of IGBTs to cover a broad range of applications:

- Power MOS 7® Series – 600V and 1200V PT technology IGBTs designated by 'GP' in the part number, one of the fastest IGBTs on the market, designed for operation at high frequencies and/or for tail current sensitive applications such as soft switching.
- Thunderbolt® Series – 600V only NPT technology IGBTs designated by 'GT' in the part number, fast IGBTs capable of 150kHz in hard switching applications, short circuit rated rugged devices suitable for switch-mode power supplies as well as motor drives.
- Fast Series – 600V and 1200V NPT technology IGBTs designated by 'GF' in the part number, short circuit rated rugged devices with low on voltage suitable for hard switching operation below 100kHz such as in motor drives.

Power MOS 7® IGBTs from APT are unique in that they are designed to switch extremely fast, and they incorporate a proprietary metal gate and open cell structure. The result is extremely low internal equivalent gate resistance (EGR), typically a fraction of an Ohm; one to two orders of magnitude lower than for poly-silicon gate devices. Low EGR enables faster switching and consequently lower switching loss. The metal gate and open cell structure also result in extremely uniform and fast excitation of the gate, minimizing hot spots during switching transients and improving reliability. An open cell structure is also more tolerant of defects induced during the manufacturing process.

Datasheet Walkthrough

The intent of datasheets provided by APT is to include relevant information that is useful and convenient for the power circuit designer, both for selection of the appropriate device as well as predicting its performance in an application. Graphs are provided to enable the designer to extrapolate from one set of operating conditions to another. It should be noted though that test results are very strongly circuit dependent, especially on stray emitter inductance but also on stray collector inductance and gate drive circuit design and layout. Different test circuits yield different results.

The following walkthrough provides definition of terms in APT datasheets as well as further details on IGBT characteristics.

Heading

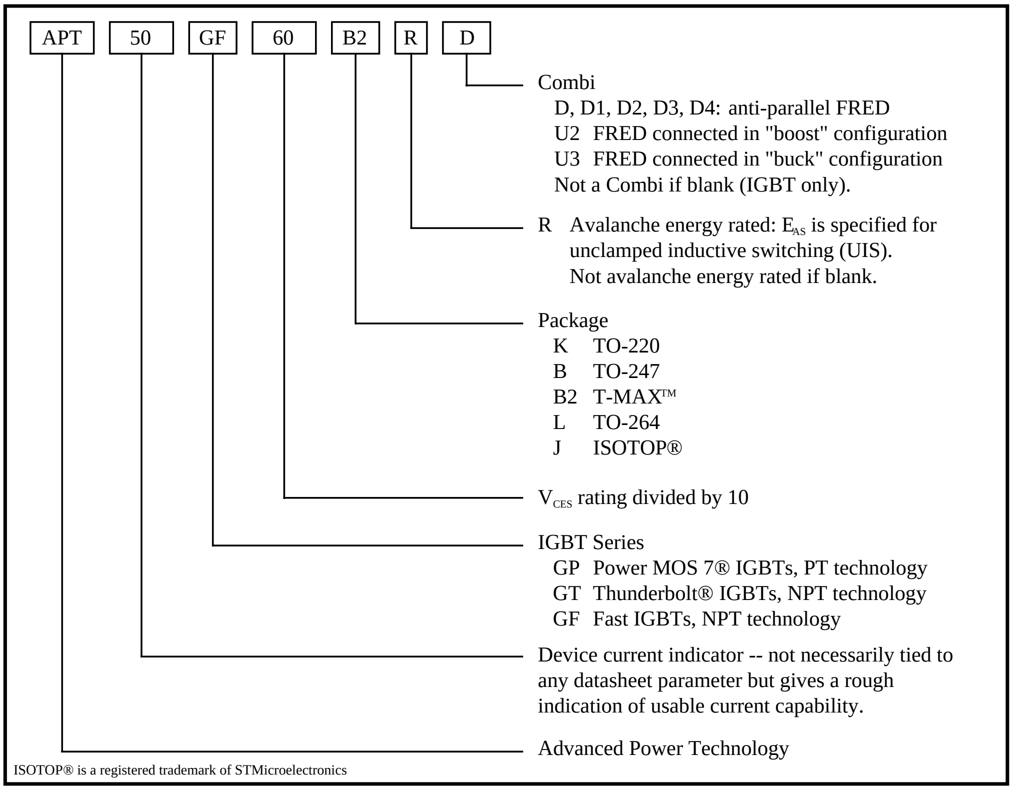

Figure 4 APT Part Numbering for IGBTs

Maximum Ratings

V_{CES} – Collector-Emitter Voltage

This is a rating of the maximum voltage between the collector and emitter terminals with the gate shorted to the emitter. This is a maximum rating, and depending on temperature, the maximum permissible collector-emitter voltage could actually be less than the V_{CES} rating. See the description of BV_{CES} in Static Electrical Characteristics.

V_{GE} – Gate-Emitter Voltage

V_{GE} is a rating of the maximum continuous voltage between the gate and emitter terminals. The purposes of this rating are to prevent breakdown of the gate oxide and to limit short circuit current. The actual gate oxide breakdown voltage is significantly higher than this, but staying within this rating at all times ensures application reliability.

V_{GEM} – Gate Emitter Voltage Transient

V_{GEM} is the maximum pulsed voltage between the gate and emitter terminals. The purpose of this rating is to prevent breakdown of the gate oxide.

Transients on the gate can be induced not only by the applied gate drive signal but often more significantly by stray inductance in the gate drive circuit as well as feedback through the gate-collector capacitance. If there is more ringing on the gate than V_{GEM}, stray circuit inductances probably need to be reduced, and/or the gate resistance should be increased to slow down the switching speed. In addition to the power circuit layout, gate drive circuit layout is critical in minimizing the effective gate drive loop area and resulting stray inductances. See Figure 9.

If a clamping zener is used, it is recommended to connect it between the gate driver and the gate resistor rather than directly to the gate terminal. Negative gate drive is not necessary but may be used to achieve the utmost in switching speed while avoiding dv/dt induced turn-on. See application note APT9302 for more information on gate drive design.

I_{C1}, I_{C2} – Continuous Collector Current

I_{C1} and I_{C2} are ratings of the maximum continuous DC current with the die at its maximum rated junction temperature. They are based on the junction to case thermal resistance rating $R_{\theta JC}$ and the case temperature as follows:

$$P_D = \frac{T_{J(max)} - T_C}{R_{\theta JC}} = V_{CE(on)} \cdot I_C \qquad (1)$$

This equation simply says that the maximum heat that can be dissipated, $\frac{T_{J(max)} - T_C}{R_{\theta JC}}$, equals the maximum allowable heat generated by conduction loss, $V_{CE(on)} \cdot I_C$. There are no switching losses involved in I_{C1} and I_{C2}. Solving for I_C:

$$I_C = \frac{T_{J(max)} - T_C}{R_{\theta JC} \cdot V_{CE(on)}} \qquad (2)$$

Of course $V_{CE(on)}$ depends upon I_C (as well as junction temperature). Except at relatively low current, the relationship between I_C and $V_{CE(on)}$ is fairly linear, as shown in Figure 5. Thus a linear approximation can be used to relate I_C to $V_{CE(on)}$.

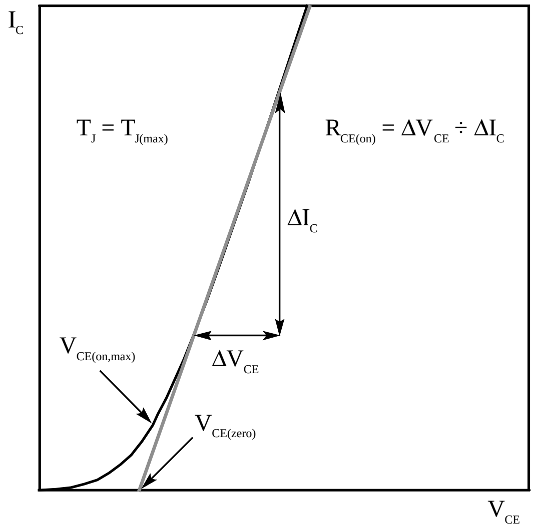

Figure 5 Linear Approximation of I_C versus $V_{CE(on)}$

The curve of $V_{CE(on)}$ is with the die at elevated temperature. (To calculate datasheet values, APT uses the maximum $V_{CE(on)}$, which is higher than the typical $V_{CE(on)}$ to account for normal variations between parts.) The equation relating $V_{CE(on)}$ to I_C is:

$$V_{CE(on)} = I_C \cdot R_{CE(on)} + V_{CE(zero)} \qquad (3)$$

This equation is substituted into (2) for $V_{CE(on)}$ to solve for I_C:

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