

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APPLIED MATERIALS, INC.,
Petitioner,

v.

OCEAN SEMICONDUCTOR LLC,
Patent Owner.

IPR2021-01342
Patent 6,968,248 B1

Before MIRIAM L. QUINN, JOHN D. HAMANN, and DAVID COTTA,
Administrative Patent Judges.

QUINN, *Administrative Patent Judge.*

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314, 37 C.F.R. § 42.4

I. INTRODUCTION

Applied Materials, Inc. (“Petitioner”) filed a Petition (Paper 1, “Petition” or “Pet.”) requesting an *inter partes* review of claims 1–22 (“the challenged claims”) of U.S. Patent No. 6,968,248 B1 (Ex. 1001, “the ’248 patent”) pursuant to 35 U.S.C. §§ 311–319. Ocean Semiconductor LLC (“Patent Owner”) filed a Preliminary Response. Paper 10 (“Preliminary Response” or “Prelim. Resp.”). With our authorization, Petitioner filed a Reply to Patent Owner’s Preliminary Response (Paper 13, “Reply”), and Patent Owner filed a Sur-Reply in Support of Patent Owner’s Preliminary Response (Paper 14, “Sur-reply”).

The standard for institution is set forth in 35 U.S.C. § 314, which provides that an *inter partes* review may not be instituted unless the information presented in the Petition and the Preliminary Response shows that “there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314 (2018); *see also* 37 C.F.R. § 42.4(a) (“The Board institutes the trial on behalf of the Director.”). Upon consideration of the parties’ contentions and the evidence of record, we conclude that Petitioner has established a reasonable likelihood of prevailing in demonstrating the unpatentability of at least one challenged claim of the ’248 patent. Accordingly, we grant Petitioner’s request and institute an *inter partes* review of the challenged claims.

A. Related Matters

The parties indicate that the ’248 patent has been asserted in the following proceedings: *Ocean Semiconductor LLC v. Analog Devices*, No. 1:20-cv-12310 (D. Mass.); *Ocean Semiconductor LLC v. Infineon*, No. 1:20-cv-12311 (D. Mass.); *Ocean Semiconductor LLC v. Huawei*, No. 4:20-cv-

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911 (E.D. Tex.); *Ocean Semiconductor LLC v. MediaTek*, No. 6:20-cv-1210 (W.D. Tex.); *Ocean Semiconductor LLC V. NVIDIA*, No. 6:20-cv-1211 (W.D. Tex.); *Ocean Semiconductor LLC v. NXP*, No. 6:20-cv-1212 (W.D. Tex.); *Ocean Semiconductor LLC v. Renesas*, No. 6:20-cv-1213 (W.D. Tex.); *Ocean Semiconductor LLC v. Silicon Labs*, No. 6:20-cv-1214 (W.D. Tex.); *Ocean Semiconductor LLC v. ST Micro*, No. 6:20-cv-1215 (W.D. Tex.); and *Ocean Semiconductor LLC v. Western Digital*, No. 6:20-cv-1216 (W.D. Tex.). Pet. 1–2; Paper 5, 2.

B. The '248 Patent

The '248 patent relates to “scheduling in an automated manufacturing environment.” Ex. 1001, 1:20–21. The '248 patent describes the manufacture of integrated circuits for modern semiconductor devices containing numerous structures or features, typically the size of a few micrometers. *Id.* at 1:38–41. The '248 patent further describes that the fabrication of integrated circuits generally involves processing a number of wafers through a series of fabrication tools, where layers of material are added to, removed from, and/or treated on a semiconducting substrate. *Id.* at 1:41–45. According to the '248 patent, controlling a semiconductor factory (“fab”) that fabricates such integrated circuits is a challenging task, where the fab is a complex environment where numerous parts (typically 40,000 wafers or more) and numerous part types (typically 100 part types or more) are simultaneously being manufactured. *Id.* at 1:65–2:3. As each wafer moves through the fab, it may undergo more than 300 processing steps, many of which use the same machines, where a large factory may contain approximately 500 computer-controlled machines to perform this wafer processing. *Id.* at 2:3–8. As described in the '248 patent, routing, scheduling, and tracking material through the fab is a difficult and

complicated task, even with the assistance of a computerized factory control system. *Id.* at 2:8–11.

Figure 3 illustrates an implementation of reactive scheduling of activities of a process flow for a semiconductor fabrication facility and is reproduced below.

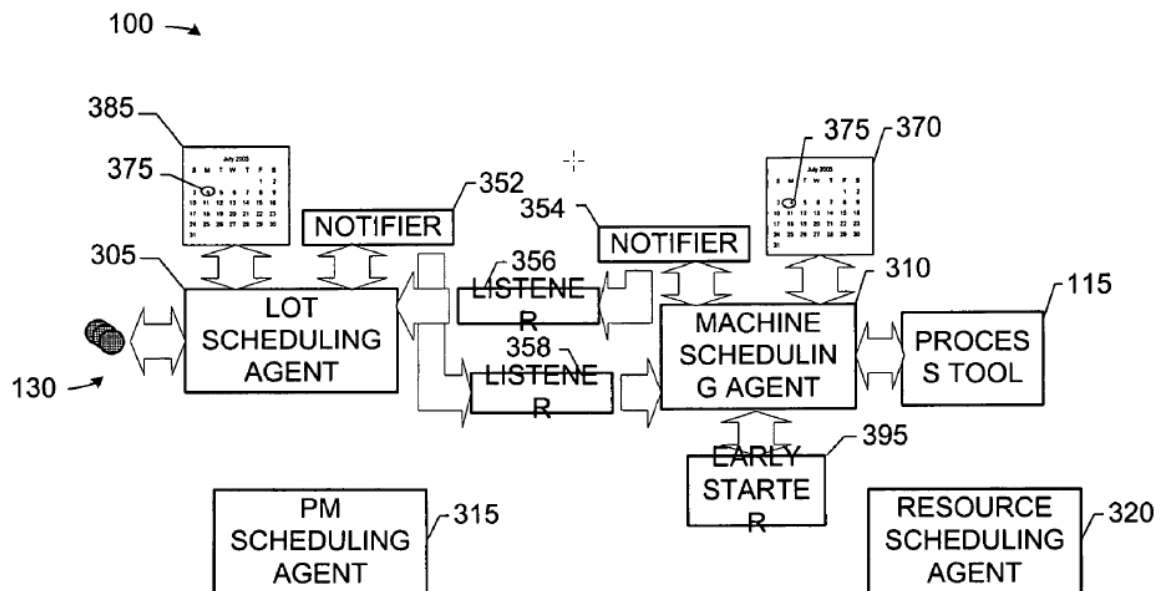


FIG. 3

Figure 3 shows a portion of process flow 100 from a semiconductor fabrication facility, and the manner in which it schedules appointments for the consumption of resources. *Id.* at 4:28–32. Process flow 100 includes stations 105, each station 105 including computing device 110 communicating with process tool 115. *Id.* at 5:17–19. Process tools 115 are processing lots 130 of wafers 135 that will eventually become integrated circuit devices, where process tool 115 may be a fabrication tool used to fabricate some portion of wafers 135. *Id.* at 5:24–26, 6:43–45.

Each computing device 110 includes software agent 265, where software agents 265, collectively, are responsible for efficiently scheduling

and controlling lots 130 of wafers 135 through the fabrication process. *Id.* at 6:24–26, 47–50. Collectively, software agents 265 reactively and proactively schedule activities for each lot 130 for operations on a specific qualified process tool 115. *Id.* at 6:63–7:3. More specifically, the software agents (or scheduling agents) 265 include: Lot Scheduling Agent (“LSA”) 305 that schedules activities on behalf of lots 130 of wafers 135; Machine Scheduling Agent (“MSA”) 310 that schedules activities on behalf of process tools 115; PM Scheduling Agent (“PMSA”) 315 that schedules activities on behalf of preventative maintenance (“PMs”) and equipment qualification (“Quals”) (not shown in Figure 3); and Resource Scheduling Agent (“RSA”) that schedules activities on behalf of resources (not shown in Figure 3). *Id.* at 7:20–30. Some of these activities are scheduled reactively (i.e., in response to events occurring in process flow 100). *Id.* at 7:36–37. For example, the ’248 patent describes the process as detecting an occurrence of a predetermined event in the process flow 100; notifying a subscribing software scheduling agent (e.g., LSA 305, MSA 310, PMAS 315, or RSA 320) of the occurrence; and reactively scheduling an action responsive to the detection of the predetermined event. *Id.* at 7:38–46.

C. Illustrative Claims

Of the challenged claims, claims 1 and 14 are independent. Each of challenged claims 2–13 and 15–22 depends from claim 1 or 14.

Claim 1 is illustrative:

1. A method for scheduling in an automated manufacturing environment, comprising:
 - automatically detecting an occurrence of a predetermined event in an integrated, automated process flow;
 - automatically notifying a software scheduling agent of the occurrence; and

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