Input Harmonics control using non-linear capacitor in GaAs FET Power Amplifier

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Abstract

We address the effect of gate signal distortion arising from capacitance non-linearity on the power added efficiencies of power amplifiers based on FET. A novel method which can compensate the non-linearity of gate capacitance is proposed. The key idea is that a reversed diode is connected to the gate, where the gate and source part of a FET is simply modeled as a diode. We demonstrated this scheme with the load-pull and source-pull measurement of the circuit. 7 % increase of power added efficiency is achieved.

Introduction

RF field effect transistors usually have the gate capacitance characteristic showing severe non-linearity around threshold voltage(V_{th}) as shown in Fig. 1. A hard turn-off of capacitance value around V_{th} is due to sudden retreat of channel carriers from the gate shadow region at the moment a transistor turns off. Below V_{th} the gate metalization sees only the parasitic capacitance in the gate fringing depletion region, the C_0. This is expected to be more severe in low-high doped MESFET and HEMTs, which are widely used in RF power amplifier. This becomes the main reason of signal distortion at the input gate when the bias is set to around V_{th} as in the class B, AB or F amplifiers. Fig 2 is the typical distorted waveform of gate signal and drain current. This simulation is done with modified Materka model fitting HEMT characteristics[1]. A spike is formed below the bias voltage. This spike is because small capacitance C_0 stores the energy rating during the half cycle. Note that in one cycle of distorted signal, the duration while the $v_g(t)$ is above V_{gb} exceeds that of $v_g(t) < V_{gb}$. The resulting excessive turn-on time results in excessive power dissipation and thus decrease of power added efficiency, which is critical measure of per-

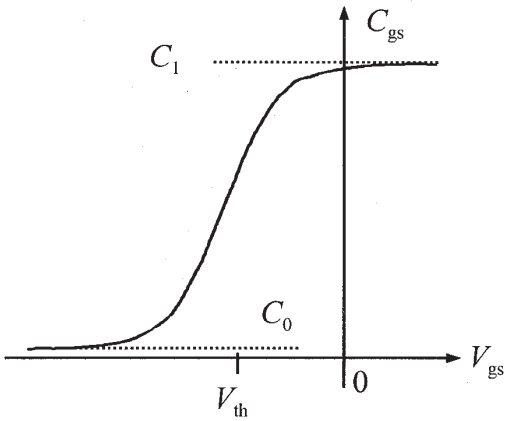

Fig 1 Typical gate capacitance characteristic of MESFET and HEMT

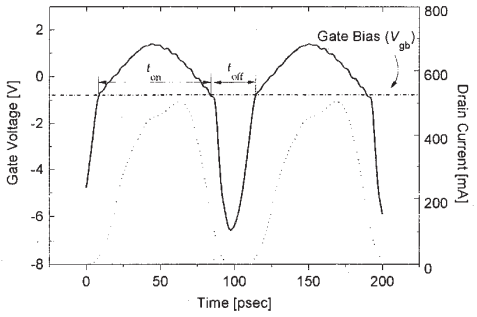

Fig. 2 Distorted signal in the gate(solid line) and waveform of drain current(dot line) in a power amplifier. Note that turn-on angle is far greater than turn-off angle and also note that the peak of negative spike is formed when the drain voltage is highest in usual power amplifier operating cycle.

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formance in mobile communication applications. Moreover, when the $v_g(t)$ is the negative peak of the spike the drain voltage is expected to be the highest. This might induce the gate-drain breakdown. From all the reasons, the input capacitance non-linearity is undesirable for power amplifiers. In the view of frequency domain this asymmetric distortion at gate can be recognized as increase of second harmonic component($2f_0$). Some circuit designers suppress the $2f_0$ by LC series network connected between gate and ground whose resonance frequency is set to $2f_0$[2]. However, it has narrow band characteristic and is dependent on the operating frequency. Shunt capacitor circuit proposed by P.M. White[3] does not depend on the operating frequency and have broadband characteristic. Although this is a very simple, this addition result in difficulty of input matching due to the increase of capacitance both below and above threshold voltage. In this paper, we employ a non-linear circuit composed of one bias capacitor and one diode to control the turn on angle of power transistor. An efficiency increase is demonstrated by load-pull and source-pull measurement.

The New Approach

The excessive turn-on angle at onset of power saturation will be avoided if we compensate gate capacitance nonlinearity. In this work, the compensation is carried out by just adding the reversed diode between the gate and constant voltage V_{diode} as shown in Fig. 3. The diode realized by another transistor whose anode is formed by wiring source and drain act as compensating non-linear capacitor. For the maximum flatness of capacitance profile, the cathode area is selected to be the same as gate metalization area and V_{diode} is set to 2 $V_{th.}$ Because the diode junction is connected in the opposite direction with the diode in the gate, the gate sees constant capacitance even below the threshold voltage. The compensated gate capacitance characteristic is depicted in Fig 4. Since the increase of capacitance value above

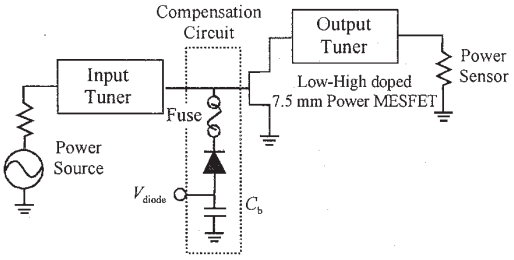


Fig. 3. Circuit compensating gate capacitance non-linearity and setup for load-pull and source-pull

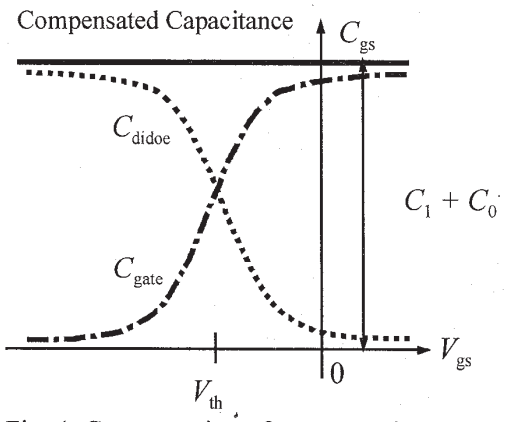


Fig. 4. Compensation of gate capacitance non-linearity using diode capacitance non-linearity. Total capacitance at gate $= C_{gs} + C_{diode}$

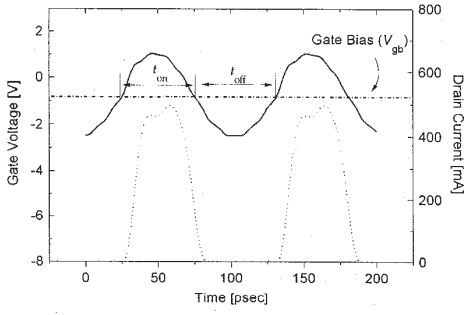
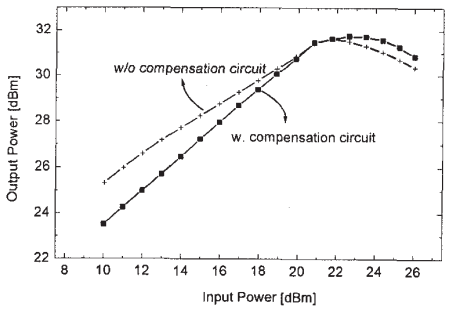


Fig. 5 Voltage wave form at gate(solid line) and drain current waveform (dot line) of the FET whose gate capacitance non-linearity is compensated. Note that turn-on angle is increased and that negative spike is not formed.

V_{th} is very small amount, the C_0, the compensation circuit hardly affect the ease of input matching. Actually, the cathode area and V_{diode} still want optimizing in the design process. The simulated voltage waveform at gate in Fig. 4 does not show a asymmetric distortion and large negative spike. This enhances power added efficiency at the point output power saturates.

Experiments and Results

As a demonstration we established the setup of Fig 3 composed of chip power MESFET , chip diode, chip capacitor on hybrid. To minimize the parasitic inductance effect they are put together as close as possible and they are connected with bonding wires. Load-pull and source-pull measurements are done at the frequency of 840 MHz. After finding the optimum load and source impedance for maximum output power with the proposed compensation circuit, power saturation characteristics are measured. The results are compared with that



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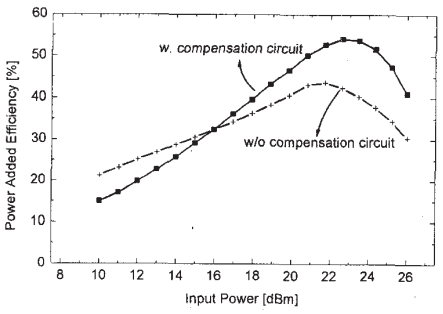

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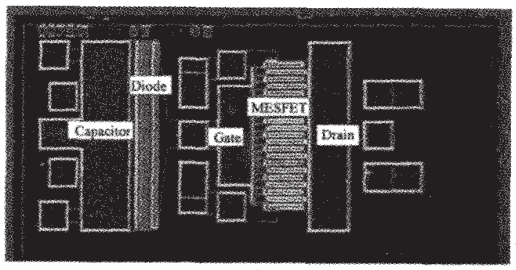
Fig 6. Performance comparison of a power MESFET with and without the compensation circuit. a) Output power b) Power added efficiency



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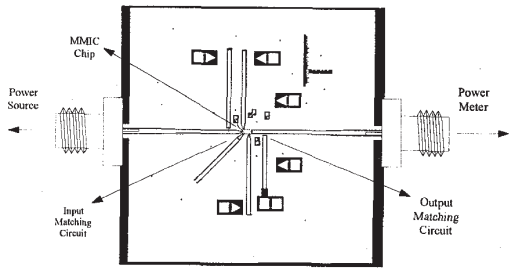

b)

Fig7. Fabricated power amplifier on PCB. a) The photograph of MMIC part. Shown area is 2mm × 1mm. b) The draft of power amplifier.

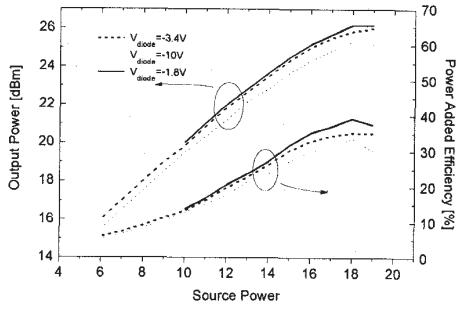

Fig 8 Output power and PAE vs. source power setting for various diode bias voltage. of fabricated power amplifier.

of bare FET. These two measurements are done by breaking the fuse between the gate and the anode of the diode. Measured output power at onset of saturation(at Pin = 21 dBm) are actually same for two cases, however, the power added efficiency(PAE) is 7 % higher for the case with compensation circuit.

We can change diode bias V_{diode} for the purpose of tuning input matching circuit. As a demonstration, we made single stage power amplifier on printed circuit board with 0.5μ × 20 × 150μ ion implant power MESFET where the capacitor and diode are integrated. Fig 7 a) is the picture of power MESFET in which the compensation network is integrated. Fig 7 b) is the draft of PCB circuit. First we roughly designed input matching circuit and then measured P_{in}-P_{out} characteristic for various diode bias at 2.4 GHz. In Fig 8, we see an output performance better than others at the diode bias of -1.8V. This implies post-fabrication tuning is possible in even MMIC process not by mechanical method but by electrical method.

Discussion

The input signal distortion comes from the voltage dependent input impedance around bias point. This distortion is amplified, mixed with other non-linearities, and appeared at output in a more complicated manner. The harmonics and third order terms are produced due to this impedance non-uniformity and affect on linearity as well as PAE of amplifiers. Therefore, the impedance flattening scheme proposed here are expected to enhance linearity as well as PAE. Also this can be applicable to HBT. In HBT, while there coexists real part and imaginary part of admittance in active region, only imaginary part exists in cut-off region.

Conclusions

We addressed effect of gate signal distortion arising from capacitance non-linearity on the power added efficiency of RF FET power amplifier. This distortion deteriorates the efficiency, bringing excessive turn-on time at the onset of output power saturation and lowering the limit of drain voltage sweep. We proposed a new approach to increase power added efficiency by compensating gate capacitance non-linearity. It is demonstrated with load-pull and source-pull measurement of both the power GaAs MESFET with compensation circuit and bare device. The device with compensation circuit showed the 7 % higher power added efficiency at the onset of output power saturation. We expect that more enhancement in PAE will be expected in the case of HFET where the capacitance non-linearity is more severe than MESFET.

References

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