V_t Compensated voltage-data a-Si TFT AMOLED pixel circuits

James L. Sanford
Frank R. Libsch

Abstract — Active-matrix organic light-emitting-diode (AMOLED) displays are now entering the marketplace. The use of a thin-film-transistor (TFT) active matrix allows OLED displays to be larger in size, higher in resolutions and lower in power dissipation than is possible using a conventional passive matrix. A number of TFT active-matrix pixel circuits have been developed for luminance control, while correcting for initial and electrically stressed TFT parameter variations. Previous circuits and driving methods are reviewed. A new driving method is presented in which the threshold-voltage (V_t) compensation performance, along with various circuit improvements for amorphous-silicon (a-Si) TFT pixel circuits using voltage data, are discussed. This new driving method along with various circuit improvements is demonstrated in a state-of-the-art 20-in. a-Si TFT AMOLED HDTV.

Keywords — *Active matrix, amorphous silicon (a-Si), organic light-emitting diode (OLED), light-emitting diode (LED), thin-film transistor (TFT), threshold voltage, threshold-voltage compensation.*

1 Introduction

Due to their high brightness and efficiency, the development of organic light-emitting diodes (OLEDs) has lead to considerable interest for use in displays.[1] OLED display products were first commercialized incorporating passive-matrix addressing in 1999 for use in automotive stereo displays.[2,3] Passive-matrix OLED displays are now being used in mobile telephones and even electric shavers. While conventional passive-matrix addressing simplifies the display fabrication, the number of rows is limited to a few hundred.[4,5] Since the OLED is on only when being addressed, high peak currents are required to obtain average brightness levels. Row line resistance, column line resistance, and various OLED electrical characteristics restrict display luminance, size, format, and efficiency. Some improvements are possible by tiling multiple passive-matrix displays or by fabricating a monolithic array of passive-matrix sub-arrays with associated drive electronics on the substrate backside.[6] For very-high-information-content displays, the cost of these approaches is likely to be prohibitive.

Thin-film-transistor (TFT) active-matrix backplanes can virtually eliminate the limitations of display content, size, format, luminance, and efficiency. Kodak has incorporated a small AMOLED display in their commercially available EasyShare LS633 digital camera.[7] Large-area high-resolution AMOLED TFT displays are being demonstrated with active-matrix TFT backplanes.[8–10] The largest AMOLED display demonstrated to date, for example, uses a-Si TFT backplanes to achieve 20-in. diagonal HDTV formats with peak brightness (>500 cd/m^2), with an efficiency >20 cd/A NTSC white.[10] TFT active-matrix backplanes were initially developed for making large-sized and high-resolution liquid-crystal displays (LCDs). The pixel circuit simply consists of a TFT connected to a storage capacitor and the pixel LC electrode. The impedance of the liquid-crystal materials used is that of a capacitor whose value varies as a function of applied voltage as the refractive index changes. TFT performance is sufficient to stabilize the storage-capacitor voltage and LC voltage within a row time. The percentage of time that the pixel TFT is on and conducts is very low (~0.1–1%). Applied data and LC voltages alternate polarity from frame to frame to avoid image sticking due to ion plating in the LC. The alternating data voltages and low duty factor on times tend to stabilize transistor characteristics such as threshold voltage for long operating lifetimes in AMLCDs.

Driving OLEDs uniformly with TFTs is more challenging than driving liquid crystal. The main reasons are (1) OLED current-dependent luminance, (2) high OLED capacitance, (3) large TFT dimensions with high gate-to-drain capacitance (C_{gd}) and gate-to-source capacitance (C_{gs}), and (4) threshold voltage and mobility variations. The drive TFT should provide a continuous current over a large portion of the frame time to efficiently drive the OLED to desired luminance levels. The pixel area limits the number of TFTs and their widths, which is directly proportional to TFT transconductance. As a result, the OLED driving TFT transconductance can be limited. The mobility (μ) of low-temperature polysilicon (LTPS) can be one to two orders of magnitude higher than that of amorphous-silicon (a-Si). As a consequence, LTPS TFT widths can be smaller, with possibilities of allowing for more TFTs in the pixel area for additional error correction. In addition, the LTPS TFT terminal voltages may be lower, yielding better power-efficient operation. As a result of high gate capacitances, TFT on/off switching can create large voltage offsets. Thus, offset correction is required. The OLED capacitance is so large that the OLED current and voltage cannot be driven into equi-

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The authors are with the IBM T. J. Watson Research Center, M/S 25-137, 1101 Kitchawan Road, Route 134, P.O. Box 218, Yorktown Height, NY 10598; telephone 914/945-1568, fax -2141, e-mail: sanfordj@us.ibm.com

librium within a typical row time (10–30 μsec). This can result in luminance that depends upon the previous state. Pixel-to-pixel variations in V_t and μ add to unwanted luminance variations. With LTPS, initial V_t and mobility variations exist due to grain size and boundary variations.[11] Time-related electrical stress variations in both V_t and mobility usually occur.[12,13] In contrast, in most a-Si processes, the initial V_t and μ are uniform within a backplane.[10,14] While time-related electrical stress may produce large V_t variations, there is typically little change in mobility.[15] Optimized AC terminal voltages help to minimize time-related electrical stress variations.[16]

Various techniques have been employed to minimize the impact of TFT variations with the use of simple pixel circuits. For example, restricting the use of an AMOLED display to video can assure that all pixels experience the same electrical stress. Another method is to operate the OLED driving TFT in a highly nonlinear manner such as an on-off switch.[17,18] In one method, to obtain gray-level images, the bits are sequentially written with binary-weighted timing to the array. This requires a custom-designed frame buffer. In another method, the binary data bits are decoded to drive separate subpixel OLEDs.

A lower cost solution is to send analog data to the pixel circuit and to have the driving method compensate for the V_t and μ variations in the OLED driving TFT. The need for V_t compensation and previous V_t compensation methods are discussed. A distinction is made regarding current or voltage data and the logical use of such data for a-Si and LTPS backplanes. Due to its inherent lower manufacturing cost, a-Si backplanes for driving OLEDs is of interest. Emphasis on lower cost also creates a need for simpler voltage-data circuits along with simpler driving methods. New pixel circuits and driving methods with performance results are presented.[19,20] Further improvements and display system integration methods are discussed.

2 Prior art

2.1 Simple pixel circuits: The need for V_t compensation

The purpose of an ideal AMOLED pixel circuit is to convert the data signal into a predetermined non-varying current for the OLED. Almost all pixel circuits using only conventional active-matrix-addressing schemes are V_t dependent. To illustrate this point, two relatively simple pixel circuits, a voltage follower and a current source, are shown in Fig. 1. In Fig. 1(a), data in the form of voltage is written onto the data storage capacitor, C, by T1 when the gate line signal is switched high. Transistor T3 operates as a voltage source follower to provide OLED current. Operating in the saturation regime, T3 drain-to-source current, I, is proportional to $(V_{data} - V_{OLED} - V_t)^2$ for $V_{data} < V_{dd} + V_t$, where V_t is the T3 threshold voltage. It is desirable for the OLED driving transistor to operate in saturation so as to minimize current dependence on drain-to-source voltage. In addition to current dependence on V_t, the current also depends on the OLED voltage. The OLED voltage may vary from pixel to pixel and increase slowly with usage, ~0.1–1 mV/hour, providing additional sources of non-uniformity.

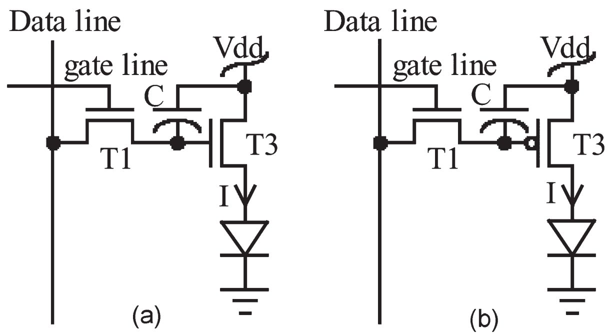

FIGURE 1 — Simple AMOLED pixel circuits; (a) voltage follower, (b) current source.

The current dependence on OLED voltage is eliminated by using the circuit shown in Fig. 1(b). T3 is a PFET device connected in a common source arrangement, allowing T3 to operate as a current source. The current is proportional to $(V_{dd} - V_{data} - V_t)^2$ for $V_{dd} + V_t > V_{data} > V_{OLED} - V_t$. As such, the drive current is independent of the OLED voltage.

There are some other operating issues with the circuits in Fig. 1. First, turning T1 off will increase the voltage across C because of T1's gate-to-source capacitance. This is a systematic effect that can be compensated for by modifying the applied data voltages. Second, as the OLED luminance is changed from one frame to the next, the OLED voltage will change, which modifies the voltage across C due to T3's C_{gs} coupling in Fig. 1(a) and T3's C_{gd} coupling in Fig. 1(b). Several addressing frames using the same data level may be needed for stabilizing the luminance. Thus, a need exists for incorporating V_t compensation.

2.2 Voltage-data V_t compensation

The first V_t-compensation AMOLED pixel circuit used voltage data (V_{data}) and four TFTs with two additional row line-control signals.[21] The circuit is shown in Fig. 2. Seven sequential operations are performed to address each row. First, with a low SW input signal and a high AZ input signal, the gate line voltage is switched with V_{dd} on the data line. Second, the AZ signal is set low, turning T2 on. A voltage across both capacitors is developed that forces T3 to conduct. Third, the SW input signal is pulsed high, turning T4 off and isolating the circuit from the OLED. With T2 on, a voltage that is proportional to the threshold voltage of T3, due to T3 conduction, is developed across both capacitors. Fourth, the AZ input voltage is switched high, turning T2 off. Fifth, the data voltage for luminance is then presented on the data line. A part of the data voltage is coupled onto the capacitor C by capacitor C_c. Sixth, the gate line signal is set high. Sev-

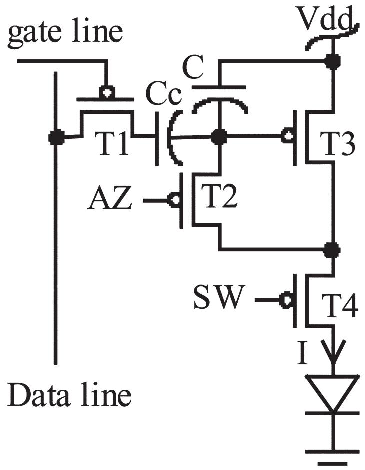

FIGURE 2 — Data voltage pixel with threshold compensation.

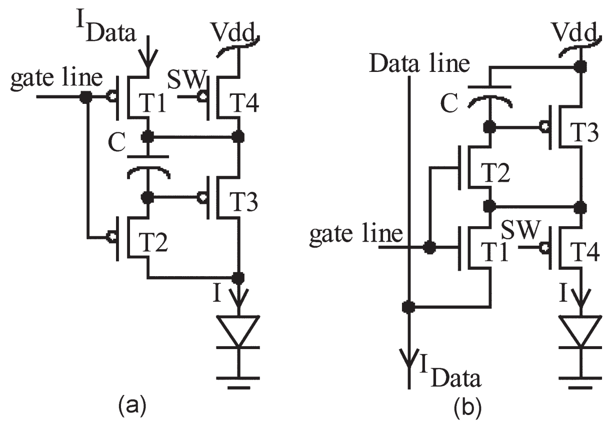

FIGURE 3 — poly-Si current data pixel circuits.

enth, the SW input signal is pulsed low turning T4 on and allowing current to flow into the OLED. The OLED current is, to a first order, proportional to the square of the data voltage coupled onto capacitor C.

The circuit in Fig. 2 is fairly complex. It uses four transistors and two storage capacitors. In addition, two other signals and drivers, SW and AZ inputs, are needed for each row. Simulations have shown that there is not sufficient time to accurately set the threshold voltage and write data within a typical row time. To account for high OLED capacitance, a two-row timing scheme was developed for a prototype QVGA display.[22] With this driving method, it is unlikely the circuit in Fig. 2 can be made to work for a higher-resolution display having shorter row times. Accurately setting the threshold voltage on the storage capacitor is a time-consuming operation.

2.3 Current data V_t compensation

Another threshold-voltage compensation approach uses data in the form of current or current data (I_{data}).[17] Data line current is used to directly set the current flowing through the OLED driving transistor. Both the circuit and driving method are simpler than the circuit shown in Fig. 2. Figure 3 shows two circuit implementations. The circuits consist of four transistors, one capacitor and only one additional input. The driving method consists of four sequential steps. First, the SW signal is switched high turning off T4 to isolate the pixel circuit from V_{DD} in Fig. 3(a) or from the OLED in Fig. 3(b). Second, in Fig. 3(a), a data current is put onto the data line while the gate line is pulled low, turning on T1 and T2, allowing the data current to flow into the pixel circuit. In Fig. 3(b), a data current is pulled out of the data line while the gate line voltage is set high turning T1 and T2 on. In both cases, the data current flows through both T2 and T3 until the current through T3 matches the data current. Third, the gate line voltage is switched high in Fig. 3(a) and is switched low in Fig. 3(b). Fourth, the SW input signal is pulled, connecting the pixel circuit to V_{dd} in Fig. 3(a) and to the OLED in Fig. 3(b).

Ignoring the capacitor-voltage errors arising from switching of the row and SW inputs, the I_{data} method does account for any changes in V_t and μ in the OLED driving transistor T3. However, for dark-gray data levels, the low data current is not able to charge or discharge the data line for pixel circuit to reach equilibrium within a row time. There are some solutions to this issue. One solution is to incorporate high data currents with a current mirror that provides a reduction in the ratio data current to the OLED current.[9] However, this arrangement does not directly set the current of the OLED driving transistor. The current through the OLED driving TFT can be different than the current mirror ratio of the data current because of variations in fabrication and differences in electrical stress. Another solution is to modulate the SW input signal in Fig. 3 at a low duty factor to compensate for the use of high data currents. A third solution is to drive the SW input in Fig. 3 with time binary-weighted digital data.[24] A reference current is used in the place of current data.

Recently, threshold-voltage compensation circuits using I_{data} for an a-Si TFT active matrix are being considered.[25] Figure 4 shows an a-Si pixel circuit using only NFETs. The circuit operation is essentially the same as the circuits shown in Fig. 3. Since the drain and source currents are identical, it is only a matter of perspective to use NFETs to form current sources. The SW input signal can be eliminated by connecting the input to V_{dd}. This allows T4 to function like a diode and still provide some power-supply isolation when writing.

While a-Si is able to produce steady-state currents suitable for reasonable brightness levels, the terminal voltages are fairly large. Due to the high terminal voltages resulting from low μ the two transistors in series between the power supply and the OLED significantly add to the power dissipation. As a result, the circuit in Fig. 4 may not be suitable for large-sized displays having high luminance. Fur-

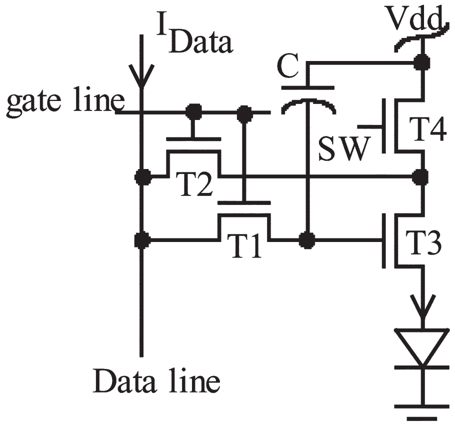

FIGURE 4 — An a-Si current data pixel circuit.

thermore, unlike poly-Si where the current data drivers may be designed into the display panel, a-Si backplanes must incorporate crystalline-silicon data drivers. Commercial I_{data} drivers are not available. An I_{data} driver for various display sizes, formats, pixel designs, and brightness levels are more complex and costly than V_{data} drivers to design and build.

3 A new voltage-data V_t compensation method for a-Si

It is generally accepted that the backplane fabrication using a-Si is lower in cost than that for poly-Si. Since, a-Si mobility does not vary within a backplane or with electrical stress over time, it seems appropriate to use the V_{data} compensation method with a-Si. In contrast, it seems appropriate to use I_{data} with poly-Si since mobility varies across the backplane. V_{data} allows the use of low-cost commercial LCD data drivers and eliminates the cost associated with crystalline-silicon I_{data} drivers.

In the design of an AMOLED pixel circuit, there are many design tradeoffs such as cost, display lifetime, the number and size of the pixel circuit components, data voltage range, and power dissipation. As seen with the V_{data} pixel circuit shown in Fig. 2, additional row control signals

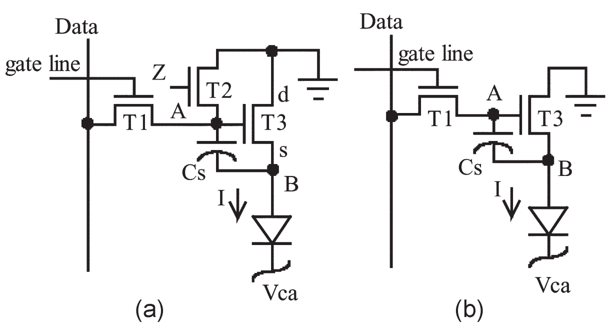

FIGURE 5 — (a) Initial pixel circuit; (b) a simpler circuit.

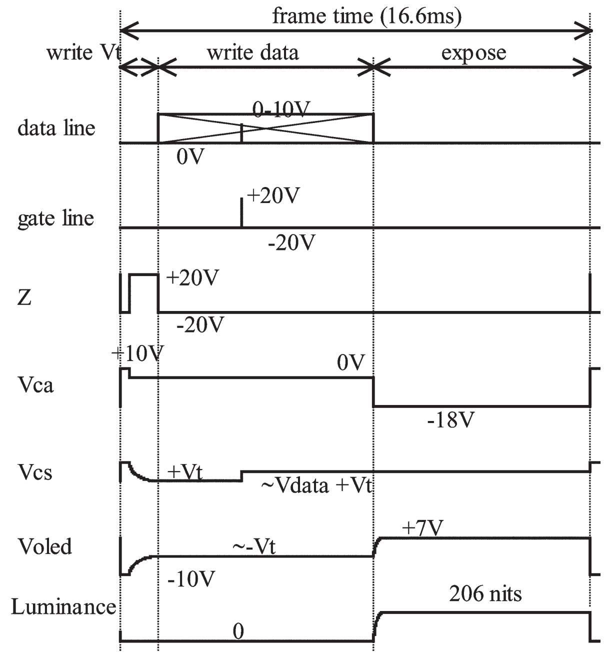

FIGURE 6 — Signal timing for Fig. 5(a).

are needed. For a-Si backplanes, this requires a custom-designed crystalline-silicon row driver, which would be more expensive than commercial LCD row drivers. The on time or duty factor of the OLED current driving TFT needs to be a large part of the frame in order to produce sufficient luminance. Too much variation in V_t will produce objectionable luminance variation. The large duty cycle severely stresses the OLED driving TFT. By increasing the width of the OLED driving TFT, the terminal voltages can be reduced. On the other hand, the TFT width cannot be too large or else the TFT will not fit within the pixel area or leave room for the other pixel circuit components. It may also be necessary for the TFT terminal voltage polarities to be alternated to further reduce the electrical stress in order to meet the display lifetime requirements. The size of the data storage capacitor also impacts the time required to establish the threshold voltage, the time to write data, the amount of pixel area, the voltage offsets, and V_t errors due to switching signals. In addition, the range of data voltages (just off to maximum luminance) should be large relative to V_t to minimize the impact of V_t compensation errors. For operation in the saturation regime, the OLED driving TFT drain-to-source voltage needs to be equal to or greater than the data voltage range. A larger data voltage range results in higher power dissipation. The different design tradeoffs depend largely upon the application.

Simpler V_{data} V_t compensation pixel circuits are possible by using multilevel cathode voltages, use of the OLED capacitance, elimination of write data conduction, and

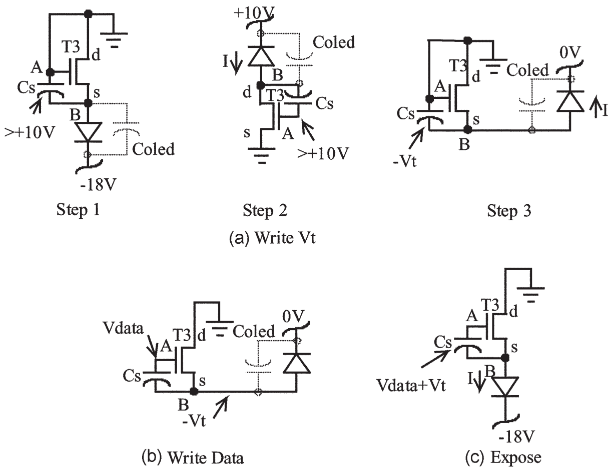

FIGURE 7 — Figure 5 equivalent circuits for the different circuit operation.

device merging. An initial pixel circuit and signal timing incorporating a multilevel cathode voltage is shown in Figs. 5(a) and 6, respectively. The equivalent circuit for each step is shown in Fig. 7. The frame time is segmented into a write V_t period, a write data period, and an expose period. This allows the write V_t step to be longer than a row time. At the beginning of the write V_t period (step 1), the Z input signal is momentarily pulled high to assure that a voltage greater than T3's V_t (~10 V) is established on the storage capacitor C_s. The cathode voltage (V_{ca}) is then switched from –18 V to +10 V with a low Z input (step 2). This reverse biases the

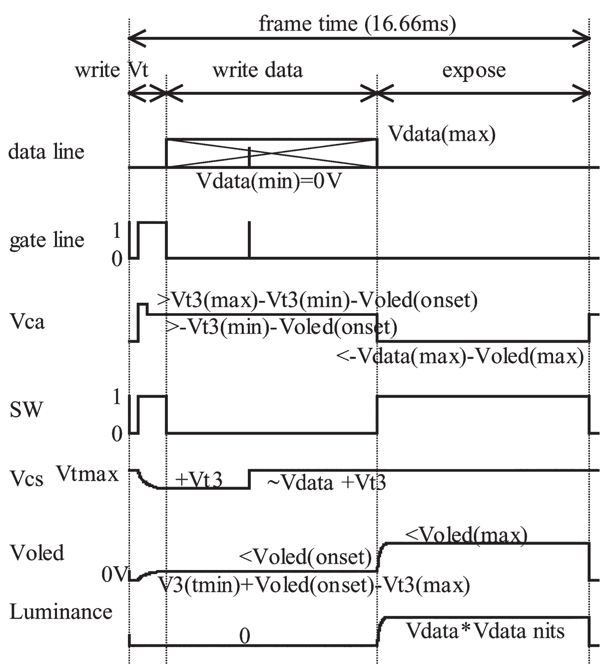

FIGURE 8 — Signal timing for Figs. 5(b), 9, and 13.

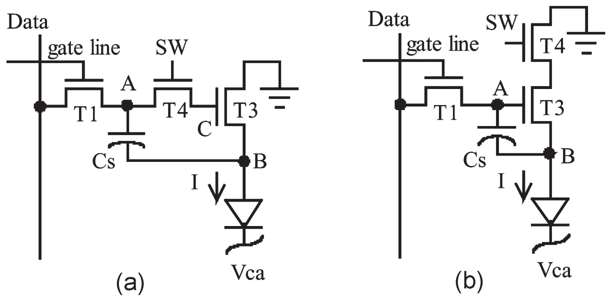

FIGURE 9 — Circuits that inhibits write period conduction in T3.

OLED *via* the reverse (source-to-drain) conduction of T3. In addition, the gate-to-drain voltage and drain-to-source voltage is reversed for removing residual charge induced from normal operation. The duration and voltages in this step can be adjusted to minimize the electrical stress due to T3 driving the OLED. The V_{ca} is then set to 0 V with a high Z input signal (step 3). The T3's drain-to-source conduction then establishes a voltage that is approximately equal to T3's V_t across C_s and the OLED cathode-to-anode terminals. Since the settling time is non-linear, the duration and accuracy are best determined with circuit simulations. During the write data period, the Z input is low while data is written onto node A. Since the OLED capacitance is much greater than C_s and T3's C_{gs}, node B is maintained at $-V_t$ during the write data period. The resulting voltage on C_s is $V_{data} + V_t$. During the expose period, the V_{ca} is set to –18 V assuring that T3 operates in saturation. The current through T3 and the OLED is proportional to $(V_{data} + V_t - V_t)^2$ or just $V_{data}{}^2$. SW and V_{ca} are connected to all of the pixels in the display.

The circuit in Fig. 5(b) functions in a similar manner, but without T2. The gate-line signal timing has been modified and is shown in Fig. 8. The gate-signal timing during the write V_t period along with the 0-V data line voltage performs the same function that T2 and SW input did for the circuit in Fig. 5(a). The required operating signal voltage amplitudes are shown as a function of circuit properties. This notation allows for signal and power dissipation optimi-

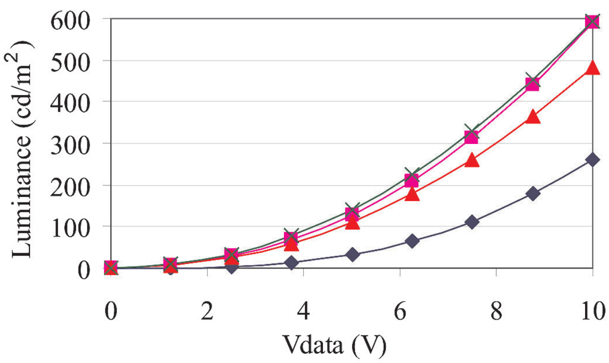

FIGURE 10 — Luminance for standard voltage follower circuit (diamonds); Fig. 5(b) (squares), Fig. 9(a) (triangles), and Fig. 9(b) (×).

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