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(54) DISPLAY DRIVER CIRCUIT, CURRENT SAMPLE/HOLD CIRCUIT AND DISPLAY DRIVING METHOD USING THE DISPLAY DRIVER CIRCUIT

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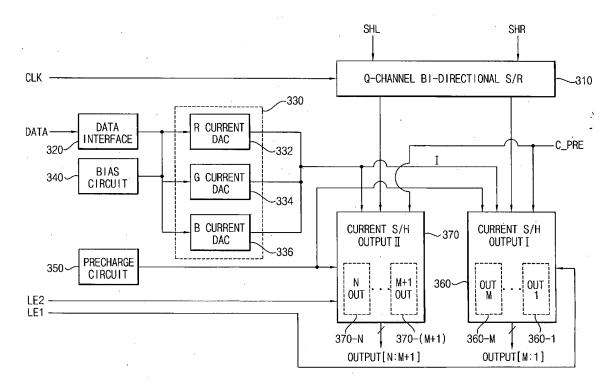
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ABSTRACT (57)

A display driver circuit may include, a shift register configured to shift a first clock signal to generate at least one second clock signal, a digital-to-analog conversion unit configured to convert digital gray-scale data to an analog gray-scale signal, a first sample/hold output circuit configured to sample/hold the analog gray-scale signal in response to the at least one second clock signal, and configured to provide the sampled/hold analog gray-scale signal to a plurality of first channels in response to a first latch enable signal, and a second sample/hold output circuit configured to sample/hold the analog gray-scale signal in response to the second clock signal, and configured to provide the sample/ hold analog gray-scale signal to a plurality of second channels in response to a second latch enable signal.





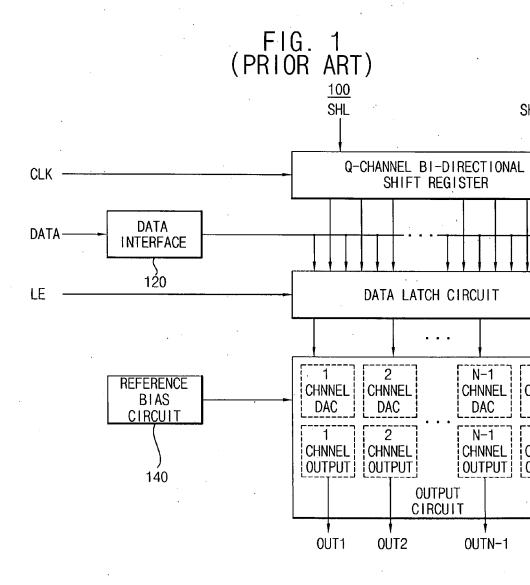
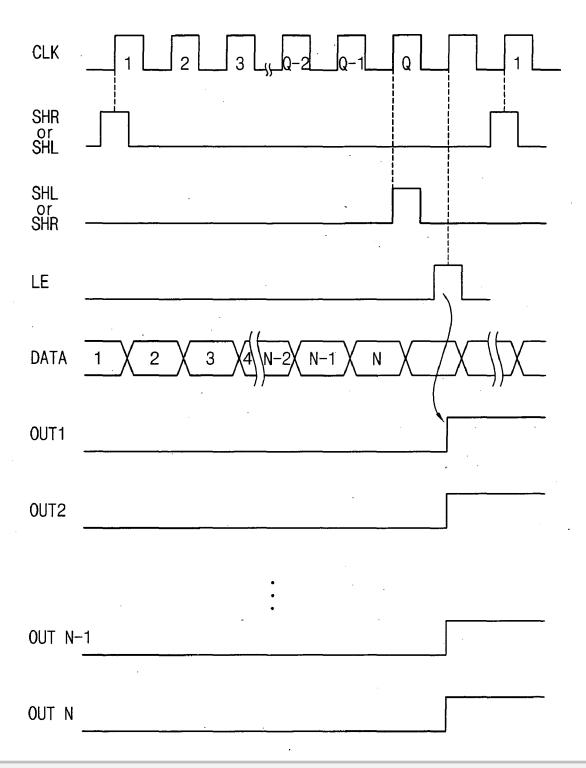


FIG. 2 (PRIOR ART)





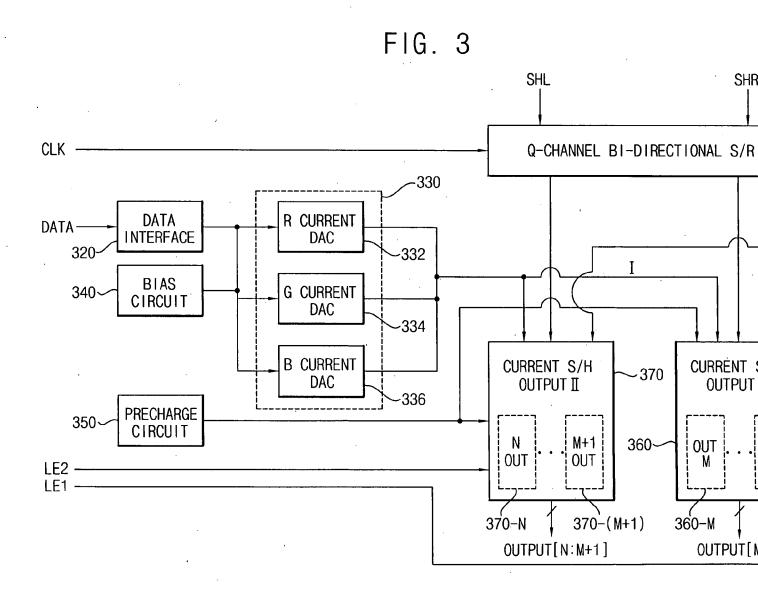
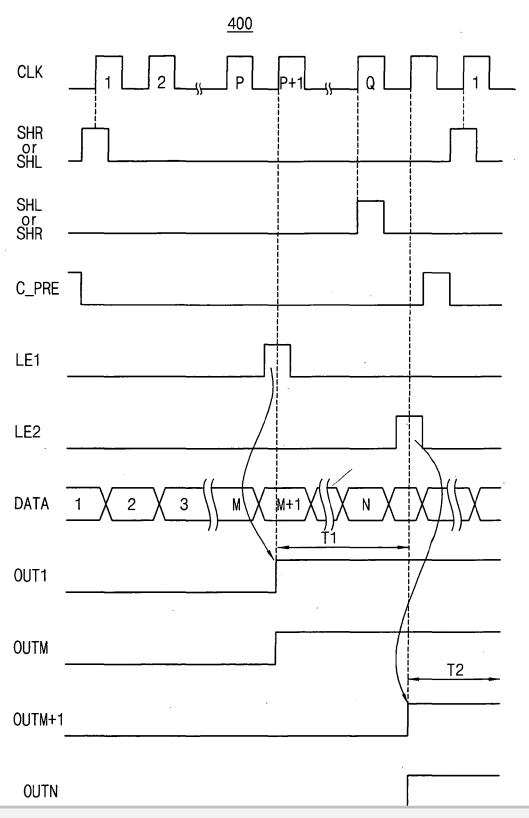


FIG. 4



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