AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Western District of Texas on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
6:21-cv-00579-ADA	6/7/2021	Western District of Texas

PLAINTIFF	DEFENDANT
SCRAMOGE TECHNOLOGY LIMITED	APPLE INC.

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	10,622,842	4/14/2020	Scramoge Technology Limited
2	9,806,565	10/31/2017	Scramoge Technology Limited
3	10,804,740	10/13/2020	Scramoge Technology Limited
4	9,843,215	12/12/2017	Scramoge Technology Limited
5	10,424,941	9/24/2019	Scramoge Technology Limited

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY
6/18/2021	☑ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	9,997,962	6/12/2018	Scramoge Technology Limited
2			
3			
4			
5			

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

AO 120 (Rev. 08/10)

TO:	Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK

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6:21-cv-00579	6/7/2021	Western District of Texas

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SCRAMOGE TECHNOLOGY LIMITED	APPLE INC.

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DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
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Print Save As... Reset

AO 120 (Rev. 08/10)

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Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

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6:21-cv-00579	6/7/2021	Western District of Texas

PLAINTIFF	DEFENDANT
SCRAMOGE TECHNOLOGY LIMITED	APPLE INC.

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PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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3		
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DECISION/JUDGEMENT

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Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/182,258	11/06/2018	Ki Min LEE	0106.001POA1

CONFIRMATION NO. 1026

151145
Shami Messinger PLLC
1000 Wisconsin Ave. NW
Suite 200
Washington, DC 20007

POA ACCEPTANCE LETTER

OC000000124937575

Date Mailed: 04/16/2021

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 04/14/2021.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/tmwilliams/

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/182,258	11/06/2018	Ki Min LEE	SUN.LGI.417D3

CONFIRMATION NO. 1026

POWER OF ATTORNEY NOTICE

23557
SALIWANCHIK, LLOYD & EISENSCHENK
A PROFESSIONAL ASSOCIATION
P.O. BOX 142950
GAINESVILLE, FL 32614

OC000000124937481

Date Mailed: 04/16/2021

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 04/14/2021.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/tmwilliams/

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/83B (07-13)
Approved for use through 01/31/2018. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number

POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date

(Note. The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☑ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above: 151145

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☑ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

Scramoge Technology Limited

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☑ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature	[signature]	Date (Optional)	FEB 19 2021
Name	Carlos Olaso		
Title	Director		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☐ Total of forms are submitted

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82A (07-13)
Approved for use through 01/31/2018. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5, unless the application number and filing date are identified in the Power of Attorney by Applicant form. If neither form PTO/AIA/82A nor form PTO/AIA82B identifies the application to which the Power of Attorney is directed, the Power of Attorney will not be recognized in the application.

Application Number	16/182,258
Filing Date	11-06-2018
First Named Inventor	Ki Min LEE
Title	WIRELESS POWER RECEIVER AND CONTROL METHOD THEREOF
Art Unit	2836
Examiner Name	KESSIE, DANIEL
Attorney Docket Number	0106.001POA1

SIGNATURE of Applicant or Patent Practitioner

Signature	/Khaled Shami/	Date (Optional)	
Name	Khaled Shami	Registration Number	38,745
Title (if Applicant is a juristic entity)			
Applicant Name (if Applicant is a juristic entity)			

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.

☐ *Total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/123 (08-12)
Approved for use through 03/31/2021. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

CHANGE OF CORRESPONDENCE ADDRESS
Patent

Address to:
Mail Stop Post Issue
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Patent Number	10,622,842
Issue Date	04-14-2020
Application Number	16/182,258
Filing Date	11-06-2018
First Named Inventor	Ki Min LEE
Attorney Docket Number	0106.001POA1

Please change the Correspondence Address for the above-identified patent to:

☑ The address associated with Customer Number: 151145

OR

☐ **Firm *or* Individual Name**

Address

City | **State** | **ZIP**

Country

Telephone | **Email**

This form cannot be used to change the data associated with a Customer Number. To change the data associated with an existing Customer Number use "Request for Customer Number Data Change" (PTO/SB/124).

This form will not affect any "fee address" provided for the above-identified patent. To change a "fee address" use the "Fee Address Indication Form" (PTO/SB/47).

I am the:

☐ Patentee.

☐ If the Patentee was not the applicant for patent (37 CFR 1.42), then a Statement under 37 CFR 3.73(c) (Form PTO/AIA/96 or equivalent) is enclosed or was filed on _____. See 37 CFR 3.71.

☑ Attorney or agent of record. Registration Number 38,745.

☐ Patent practitioner acting in a representative capacity whose correspondence address is the correspondence address of record. Notice has been given to the patentee or owner. Registration Number 38,745.

Signature /Khaled Shami/

Typed or Printed Name KHALED SHAMI

Date April 13, 2021 | Telephone 202-516-6901

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of _____ forms are submitted.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/AIA/96 (08-12)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: SCRAMOGE TECHNOLOGY LIMITED

Application No./Patent No.: 10,622,842 Filed/Issue Date: 04-14-2020

Titled: WIRELESS POWER RECEIVER AND CONTROL METHOD THEREOF

SCRAMOGE TECHNOLOGY LIMITED, a Corporation

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☑ The assignee of the entire right, title, and interest.

2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):

   ☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

   ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

B. ☑ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: LEE, KI MIN, LEE, JUNG OH To: LG INNOTEK CO., LTD.

   The document was recorded in the United States Patent and Trademark Office at

   Reel 029174, Frame 0295, or for which a copy thereof is attached.

2. From: LG INNOTEK CO., LTD. To: SCRAMOGE TECHNOLOGY LIMITED

   The document was recorded in the United States Patent and Trademark Office at

   Reel 055335, Frame 0652, or for which a copy thereof is attached.

PTO/AIA/96 (08-12)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☐ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Khaled Shami/	April 13, 2021
Signature	Date
Khaled Shami	38,745
Printed or Typed Name	Title or Registration Number

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	42438638
Application Number:	16182258
International Application Number:	
Confirmation Number:	1026
Title of Invention:	WIRELESS POWER RECEIVER AND CONTROL METHOD THEREOF
First Named Inventor/Applicant Name:	Ki Min LEE
Customer Number:	23557
Filer:	Khaled Shami/Susanh Perez
Filer Authorized By:	Khaled Shami
Attorney Docket Number:	SUN.LGI.417D3
Receipt Date:	14-APR-2021
Filing Date:	06-NOV-2018
Time Stamp:	10:03:17
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	01060000000_POASigned.pdf	1055768 a163da1e2fda2ffb59b2385b929b44750ed33a63	no	1

Warnings:

Information:					
2	Transmittal Letter	Pat_10622842_POA_Transmittal.pdf	229381 66e744df52156ccdcf174d0d71b8aaa02f63cd8a	no	1
Warnings:					
Information:					
3	Change of Address	Pat_10622842_aia0123.pdf	257488 3973e3a672466f9fa64cb8269ba08e42817b1375	no	2
Warnings:					
Information:					
4	Assignee showing of ownership per 37 CFR 3.73	Pat_10622842_373_aia0096.pdf	160126 18ac82ce9a9689620754aadcd520c9e198e5ea0e	no	3
Warnings:					
Information:					
		Total Files Size (in bytes):	1702763		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 16/182,258	Filing Date 11/06/2018	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $100 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $460 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	08/24/2020	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 18	Minus	** 27	= 0		x $100 =	0
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0		x $460 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/JACQUELYN L WILLIAMS/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/182,258	04/14/2020	10622842	SUN.LGI.417D3	1026

23557 7590 03/25/2020

SALIWANCHIK, LLOYD & EISENSCHENK
A PROFESSIONAL ASSOCIATION
P.O. BOX 142950
GAINESVILLE, FL 32614

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

LG INNOTEK CO., LTD., Seoul, KOREA, REPUBLIC OF;
Ki Min LEE, Seoul, KOREA, REPUBLIC OF;
Jung Oh LEE, Seoul, KOREA, REPUBLIC OF;

In the Specification

Please replace Figures 9 and 10 with the corrected drawing sheets attached hereto.

Please amend paragraph [0083] as follows:

[0083] First, referring to FIG. 9, after the short-range communication antenna 340 has been disposed on in the printed circuit board 301, the shielding unit 380 may be attached to one side of the printed circuit board 301 with an adhesive. The printed circuit board 301 comprises a plurality of layers wherein each layer of the plurality of layers is spaced apart from adjacent layers. The shielding unit 380 is disposed under the short-range communication antenna 340 or the receiving coil 310 (not shown in the Fig. 9). Referring still to FIG. 9, in a first region 411, at least one of the layers can overlap 405 the wireless power receiving coil in a vertical direction 400 perpendicular to an upper surface 385 of the shielding unit 380; and in a second region 412,413, at least one of the layers does not overlap the wireless power receiving coil in the vertical direction 400. Also, a first gap d1 or a first distance d1, measured in the vertical direction 400, between layers in the first region 411 can be greater than a second gap d2 or a second distance d2, measured in the vertical direction, between layers in the second region 412,413.

Change(s) applied to document, /R.K.C./ 1/29/2020

Please amend paragraph [~~0083~~] 0084 as follows:

[0084] Referring to FIG. 10, the printed circuit board 301 comprises a plurality of layers wherein each layer of the plurality of layers is spaced apart from adjacent layers, the short-range communication antenna 340 or the receiving coil 310 (not shown in the Fig. 10) is disposed in the printed circuit board 301. Moreover, the shielding unit 380 is disposed in the printed circuit board 301. The shielding unit 380 is disposed under the receiving coil 310 or the short-range communication antenna 340. The receiving coil 310 (not shown in the Fig. 10), the short-range communication antenna 340, and the shielding unit 380 are disposed between the plurality of layers of the printed circuit board 301. While the procedure of disposing the short-range communication antenna 340 or receiving coil(310)(not shown in the Fig. 10) in the printed circuit board 301 is being performed, the shielding unit 380 may be inserted into the printed circuit board 301. That is, unlike

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

23557 7590 12/11/2019
SALIWANCHIK, LLOYD & EISENSCHENK
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GAINESVILLE, FL 32614

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/182,258	11/06/2018	Ki Min LEE	SUN.LGI.417D3	1026

TITLE OF INVENTION: WIRELESS POWER RECEIVER AND CONTROL METHOD THEREOF

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0.00	$0.00	$1000	03/11/2020

EXAMINER	ART UNIT	CLASS-SUBCLASS
KESSIE, DANIEL	2836	307-104000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Saliwanchik, Lloyd & Eisenschenk
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: LG INNOTEK CO., LTD.

(B) RESIDENCE: (CITY and STATE OR COUNTRY): SEOUL, KOREA

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☒ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

☒ Electronic Payment via EFS-Web ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. 190065

5. **Change in Entity Status** (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date 10 MAR. 2020

Typed or printed name Jeff Lloyd Registration No. 35,589

PTOL-85 Part B (08-18) Approved for use through 01/31/2020 OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Electronic Patent Application Fee Transmittal

Application Number:	16182258
Filing Date:	06-Nov-2018
Title of Invention:	WIRELESS POWER RECEIVER AND CONTROL METHOD THEREOF
First Named Inventor/Applicant Name:	Ki Min LEE
Filer:	Jeff Lloyd/Larann Arzie
Attorney Docket Number:	SUN.LGI.417D3

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	1000	1000

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**1000**

Electronic Acknowledgement Receipt

EFS ID:	38823123
Application Number:	16182258
International Application Number:	
Confirmation Number:	1026
Title of Invention:	WIRELESS POWER RECEIVER AND CONTROL METHOD THEREOF
First Named Inventor/Applicant Name:	Ki Min LEE
Customer Number:	23557
Filer:	Jeff Lloyd/Larann Arzie
Filer Authorized By:	Jeff Lloyd
Attorney Docket Number:	SUN.LGI.417D3
Receipt Date:	10-MAR-2020
Filing Date:	06-NOV-2018
Time Stamp:	15:38:53
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$1000
RAM confirmation Number	E202030F39417317
Deposit Account	190065
Authorized User	Larann Arzie
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	SUN-LGI-417D3-IFP-AF.pdf	185854 ad4ccffbfcc9b5f11aea07604e7ad9964a802988	no	1
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30282 79b1037aa13e59766c571e37ed864c5ee17798f1	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	216136		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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NOTICE OF ALLOWANCE AND FEE(S) DUE

23557 7590 12/11/2019

SALIWANCHIK, LLOYD & EISENSCHENK
A PROFESSIONAL ASSOCIATION
P.O. BOX 142950
GAINESVILLE, FL 32614

EXAMINER
KESSIE, DANIEL

ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 12/11/2019

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/182,258	11/06/2018	Ki Min LEE	SUN.LGI.417D3	1026

TITLE OF INVENTION: WIRELESS POWER RECEIVER AND CONTROL METHOD THEREOF

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0.00	$0.00	$1000	03/11/2020

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

23557 7590 12/11/2019

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A PROFESSIONAL ASSOCIATION
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GAINESVILLE, FL 32614

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/182,258	11/06/2018	Ki Min LEE	SUN.LGI.417D3	1026

TITLE OF INVENTION: WIRELESS POWER RECEIVER AND CONTROL METHOD THEREOF

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0.00	$0.00	$1000	03/11/2020

EXAMINER	ART UNIT	CLASS-SUBCLASS
KESSIE, DANIEL	2836	307-104000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1_____
2_____
3_____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑Issue Fee ❑Publication Fee (if required) ❑Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/182,258	11/06/2018	Ki Min LEE	SUN.LGI.417D3	1026

23557 7590 12/11/2019

SALIWANCHIK, LLOYD & EISENSCHENK
A PROFESSIONAL ASSOCIATION
P.O. BOX 142950
GAINESVILLE, FL 32614

EXAMINER	
KESSIE, DANIEL	
ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 12/11/2019

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 02/11)

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 16/182,258	Applicant(s) LEE et al.	
	Examiner DANIEL KESSIE	Art Unit 2836	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to See Continuation Sheet.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 1-2 and 21-38 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information , please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☑ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☑ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/DANIEL KESSIE/
Primary Examiner, Art Unit 2836

Continuation of 1. This communication is responsive to: 02/25/2019

DETAILED ACTION

Notice of Pre-AIA or AIA Status

1. The present application is being examined under the pre-AIA first to invent provisions.

Allowable Subject Matter

2. Claims 1, 2 and 21-38 are allowed.

3. The following is an examiner's statement of reasons for allowance: The combination of references does not disclose a first region in which at least one of the first layer and the second layer overlaps the wireless power receiving coil in a vertical direction perpendicular to an upper surface of the shielding unit: and a second region in which at least one of the first layer and the second laver does not overlap the wireless power receiving coil in the vertical direction, wherein a first distance, measured in the vertical direction, between the first laver and the second layer in the first region is greater than a second distance measured in the vertical direction, between the first layer and the second layer in the second region.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to DANIEL KESSIE whose telephone number is (571)272-4449. The examiner can normally be reached on Monday-Friday 8am-5pmEst.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/DANIEL KESSIE/
11/29/2019
Primary Examiner, Art Unit 2836

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/182,258	LEE et al.
	Examiner	Art Unit
	DANIEL KESSIE	2836

CPC - Searched*		
Symbol	Date	Examiner
H02J50/10,12,70	07/08/2019	FMF

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
EAST.	07/08/2019	FMF
inventor search	11/29/2019	DK
assignee search	11/29/2019	DK
CPC search	11/29/2019	DK

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
	See interference search printout.	07/08/2019	FMF

/DANIEL KESSIE/ Primary Examiner, Art Unit 2836	

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/182,258	LEE et al.
	Examiner	Art Unit
	DANIEL KESSIE	2836

CPC						
Symbol					Type	Version
H02J	/	50	/	12	F	2016-02-01
G06K	/	19	/	0708	I	2013-01-01
G06K	/	19	/	0715	I	2013-01-01
G06K	/	19	/	07783	I	2013-01-01
H01Q	/	1	/	2225	I	2013-01-01
H04B	/	5	/	0031	I	2013-01-01
H04B	/	5	/	0037	I	2013-01-01
H04B	/	5	/	0087	I	2013-01-01
H01Q	/	1	/	526	I	2013-01-01
H02J	/	50	/	70	I	2016-02-01
H01Q	/	7	/	00	I	2013-01-01
H02J	/	50	/	80	I	2016-02-01
H02J	/	7	/	025	I	2013-01-01
H02J	/	7	/	045	I	2013-01-01
H02J	/	50	/	10	A	2016-02-01

CPC Combination Sets							
Symbol					Type	Set	Ranking	Version
	/		/					

NONE (Assistant Examiner)	(Date)	Total Claims Allowed: 20	
/DANIEL KESSIE/ Primary Examiner, Art Unit 2836 (Primary Examiner)	29 November 2019 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 9

U.S. Patent and Trademark Office — Part of Paper No.: 20191129

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/182,258	LEE et al.
	Examiner	Art Unit
	DANIEL KESSIE	2836

INTERNATIONAL CLASSIFICATION				
CLAIMED				
H02J	/	50	/	12

NON-CLAIMED				
	/		/	

US ORIGINAL CLASSIFICATION	
CLASS	SUBCLASS

CROSS REFERENCES(S)						
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					

NONE (Assistant Examiner)	(Date)	Total Claims Allowed: 20	
/DANIEL KESSIE/ Primary Examiner, Art Unit 2836 (Primary Examiner)	29 November 2019 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 9

U.S. Patent and Trademark Office — Part of Paper No.: 20191129

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/182,258	LEE et al.
	Examiner	**Art Unit**
	DANIEL KESSIE	2836

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	10	28	19	37										
2	2	11	29	20	38										
3	21	12	30												
4	22	13	31												
5	23	14	32												
6	24	15	33												
7	25	16	34												
8	26	17	35												
9	27	18	36												

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 20	
/DANIEL KESSIE/ Primary Examiner, Art Unit 2836 (Primary Examiner)	29 November 2019 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 9

U.S. Patent and Trademark Office Part of Paper No.: 20191129

PTO/SB/08A (08-03)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

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Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	16/182,258
Filing Date	November 6, 2018
First Named Inventor	Ki Min LEE
Art Unit	2836
Examiner Name	~~Fleming, Fritz M.~~ Daniel Kessie
Attorney Docket Number	SUN.LGI.417D3

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. [1]	Document Number Number - Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	U1	2004/0085247-A1	05-06-2004	Mickle et al.	ALL
	U2	2007/0069961-A1	03-29-2007	Akiho et al.	ALL

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. [1]	Foreign Patent Document Country Code [3] - Number [4] - Kind Code [5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
	F1	JP-2006-319223-A (with English Abstract)	11-24-2006	MURATA MFG CO LTD	ALL	

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. [1]	Include name of the author (in CAPITAL LETTERS), title of the article, (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	R1	European Search Report dated June 25, 2019 in European Application No. 19159579.2.	

Examiner Signature	/DANIEL KESSIE/	Date Considered	11/29/2019

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] Applicant's unique citation designation number (optional). [2] Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /D.K/

J:\SUN\LGI\417D3\IDS-Refs\PTO-SB-08(3).doc/whs

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	0	(("2004085247") or ("2007069961")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/11/29 11:07
L2	2	(("20040085247") or ("20070069961")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/11/29 11:07
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L4	22	("2004/0085247").URPN.	USPAT	OR	ON	2019/11/29 11:46
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L10	109	("20020018911" | "20020022284" | "20020025391" | "20020053320" | "20020056839" | "20020068392" | "20020130042" | "20020170897" | "20020195644" | "20030059987" | "20030112576" | "20030175427" | "20040002176" | "20040013982" | "20040026689" | "20040084670" | "20040211329" | "3512052" | "3769096" | "3955098" | "3999122" | "4183006" | "4302648" | "4340657" | "4442019" | "4865197" | "4926052" | "4937119" | "4951028" | "5140302" | "5173835" | "5206525" | "5259926" | "5321240" | "5347144" | "5350237" | "5364735" |	US-PGPUB; USPAT; USOCR	OR	ON	2019/11/29 12:06

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L12	430	11 and coil same layer with overlap$4	US-PGPUB; USPAT	OR	ON	2019/11/29 12:11

EAST Search History (Interference)

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11/29/2019 12:37:08 PM

PTO/SB/08A (08-03)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	16/182,258
Filing Date	November 6, 2018
First Named Inventor	Ki Min LEE
Art Unit	2836
Examiner Name	~~Fleming, Fritz M.~~ Daniel Kessie
Attorney Docket Number	SUN.LGI.417D3

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. [1]	Document Number Number - Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. [1]	Foreign Patent Document Country Code [3] - Number [4] - Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
	F1	KR-10-2011-0103395-A (with English Abstract)	09-20-2011	QUALCOMM INC	ALL	

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. [1]	Include name of the author (in CAPITAL LETTERS), title of the article, (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	R1	Office Action September 10, 2019 in Korea Patent Application No. 10-2019-0080545.	

Examiner Signature	/DANIEL KESSIE/	Date Considered	11/29/2019

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] Applicant's unique citation designation number (optional). [2] Applicant is to place a check mark here if English language Translation is attached.

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /D.K/

J:\SUN\LGI\417D3\IDS-Refs\PTO-SB-08(4).doc/whs

PTO/SB/08A (08-03)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
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Art Unit	2836
Examiner Name	Fleming, Fritz M.
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Examiner Initials*	Cite No. [1]	Document Number Number - Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. [1]	Foreign Patent Document Country Code [3] - Number [4] - Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
	F1	KR-10-2011-0103395-A (with English Abstract)	09-20-2011	QUALCOMM INC	ALL	

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. [1]	Include name of the author (in CAPITAL LETTERS), title of the article, (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	R1	Office Action September 10, 2019 in Korea Patent Application No. 10-2019-0080545.	

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] Applicant's unique citation designation number (optional). [2] Applicant is to place a check mark here if English language Translation is attached.

I hereby certify that this correspondence is being electronically filed in the United States Patent and Trademark Office on November 19, 2019.

Jeff Lloyd, Patent Attorney, Reg. No. 35,589

SUPPLEMENTAL INFORMATION
DISCLOSURE STATEMENT
UNDER 37 C.F.R §§ 1.97 AND 1.98
Examining Group 2836
Patent Application
Docket No. SUN.LGI.417D3
Serial No. 16/182,258

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Examiner	:	Fleming, Fritz M.
Art Unit	:	2836
Applicants	:	Ki Min Lee, Jung Oh Lee
Serial No.	:	16/182,258
Filed	:	November 6, 2018
Conf. No.	:	1026
For	:	WIRELESS POWER RECEIVER AND CONTROL METHOD THEREOF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT
UNDER 37 C.F.R. §§ 1.97 AND 1.98

Sir:

In accordance with 37 C.F.R. § 1.56, the references listed on the attached form PTO/SB/08 are being brought to the attention of the Examiner for consideration in connection with the examination of the patent application identified above. Copies of the cited references are attached.

The undersigned hereby certifies that each item of information contained in this Supplemental Information Disclosure Statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. Applicants are attaching a copy of the Korean Office Action.

J:\SUN\LGI\417D3\IDS-Refs\SIDS3.DOC/whs

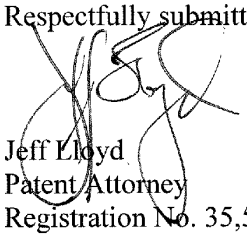
This Information Disclosure Statement is being submitted subsequent to the mailing of an Ex Parte Quayle Action but before the mailing of a Notice of Allowance. The fee of $240.00 was paid at the time this statement was filed.

It is respectfully requested that the Examiner indicate consideration of the cited references by returning a copy of the attached form PTO/SB/08 with initials or other appropriate marks.

Applicants respectfully assert that the substantive provisions of 37 C.F.R. §§ 1.56, 1.97, and 1.98 are met by the foregoing statements.

The Commissioner is hereby authorized to charge any fees under 37 C.F.R. §§ 1.16 or 1.17 as required by this paper to Deposit Account 19-0065.

Respectfully submitted,



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JL/whs

Attachments: Form PTO/SB/08; copies of references cited.

J:\SUN\LGI\417D3\IDS-Refs\SIDS3.DOC/whs

Espacenet

Bibliographic data: KR20110103395 (A) — 2011-09-20

RETROFITTING WIRELESS POWER AND NEAR-FIELD COMMUNICATION IN ELECTRONIC DEVICES

Inventor(s): KIRBY MILES A [GB]; GROB MATTHEW S [US]; OZAKI ERNEST T [US]; TONCICH STANLEY S [US]; COOK NIGEL P [GB]; KINSEY STANLEY [US]; HILLAN JOHN [GB]; FRANKLAND STEVE [GB] ± (KIRBY MILES A, ; GROB MATTHEW S, ; OZAKI ERNEST T, ; TONCICH STANLEY S, ; COOK NIGEL P, ; KINSEY STANLEY, ; HILLAN JOHN, ; FRANKLAND STEVE)

Applicant(s): QUALCOMM INC [US] ± (QUALCOMM INCORPORATED)

Classification: **- international:** ***H01M10/46; H02J17/00; H02J7/00***
- cooperative: **H01F27/365 (KR); H01M10/46 (KR); H02J50/12 (KR); H02J50/70 (KR); H02J7/0045 (KR); H02J7/022 (KR); H02J7/025 (KR); H04B5/0031 (KR)**

Application number: KR20117014027 20091217 Global Dossier

Priority number(s): US20090150257P 20090205 ; US20090610831 20091102 ; US20090163387P 20090325

Also published as: CN102301558 (A) JP2012517206 (A) JP2014241717 (A) JP5628191 (B2) KR20140117690 (A) TW201112567 (A) less

Abstract not available for KR20110103395 (A)
Abstract of corresponding document: TW201112567 (A)

Exemplary embodiments are directed to retrofitting existing electronic devices for wireless power transfer and near-field communication. Retrofitting circuitry includes an antenna for receiving a signal from an external source, and conversion circuitry for converting the signal to be used by an electronic device. The antenna and conversion circuitry are configured to retrofit to the electronic device, where the electronic device did not originally include the antenna or conversion circuitry. The antenna and conversion circuitry may be configured to receive and convert the signal to generate wireless power for the electronic device. The antenna and the conversion circuitry may also be configured to enable the electronic device to send and receive near-field communication data.

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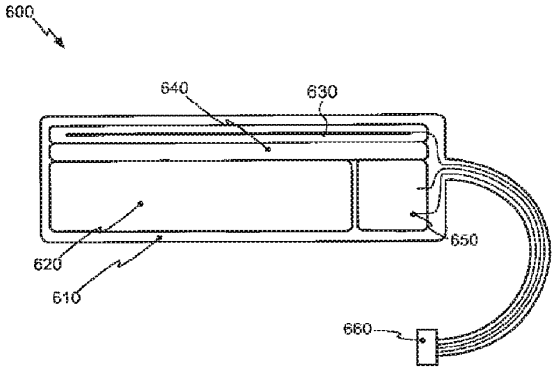
전체 청구항 수 : 총 28 항

(54) 발명의 명칭 전자 디바이스의 무선 전력공급 및 근거리장 통신 개장

(57) 요 약

예시적인 실시예들은 무선 전력 전달 및 근거리장 통신을 위한 기존 전자 디바이스들의 개장에 관한 것이다. 개장 회로는 외부 소스로부터 신호를 수신하기 위한 안테나, 및 전자 디바이스에 의해 사용되도록 이 신호를 변환하는 변환 회로를 포함한다. 안테나와 변환 회로는 전자 디바이스에 개장되도록 구성되어 있는데, 즉 전자 디바이스는 원래에는 안테나 또는 변환 회로를 포함하지 않았다. 안테나 및 변환 회로는 신호를 수신 및 변환하여 전자 디바이스를 위한 무선 전력을 생성하도록 구성될 수 있다. 안테나 및 변환 회로는 또한 전자 디바이스가 근거리장 통신 데이터를 전송 및 수신할 수 있게 하도록 구성될 수 있다.

대 표 도 - 도6a



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61/150,257 2009년02월05일 미국(US)

61/163,367 2009년03월25일 미국(US)

특허청구의 범위

청구항 1

전자 디바이스를 위한 전력 회로로서,

송신 안테나에 의해 생성되는 근거리장 방사의 커플링 모드 구역으로부터 신호를 수신하기 위한 안테나; 및

상기 신호를 전자 디바이스에 의해 사용될 DC 전력으로 변환하기 위한 변환 회로를 포함하며,

상기 안테나 및 상기 변환 회로는 상기 전자 디바이스의 배터리 격납부 (compartment) 의 기존 연결 및 기존 폼 팩터 (form factor) 를 사용하여 상기 전자 디바이스에 전기적으로 및 기계적으로 결합하도록 구성되는, 전력 회로.

청구항 2

제 1 항에 있어서,

상기 변환 회로에 동작 가능하도록 결합되고 상기 변환 회로로부터의 상기 DC 전력으로 충전되도록 구성된 배터리를 더 포함하는, 전력 회로.

청구항 3

제 1 항에 있어서,

상기 안테나 및 상기 변환 회로는 근거리장 통신 데이터를 전송 및 수신하도록 더 구성되는, 전력 회로.

청구항 4

제 1 항에 있어서,

상기 전자 디바이스의 상응하는 하우징부를 대체하도록 구성된 대체 하우징부를 더 포함하며,

상기 안테나 및 상기 변환 회로는 상기 대체 하우징부와 통합형으로 형성되고,

상기 변환 회로는 상기 전자 디바이스의 기존 배터리에 전기적으로 결합되는, 전력 회로.

청구항 5

제 1 항에 있어서,

상기 안테나 및 상기 변환 회로는 상기 전자 디바이스의 기존 하우징부에 부착하고 상기 전자 디바이스의 기존 배터리에 동작 가능하게 결합하도록 구성되는, 전력 회로.

청구항 6

제 1 항에 있어서,

상기 전자 디바이스에 전력을 공급하기 위해 전하를 저장하는 재충전가능 저장 전지들을 더 포함하며,

상기 재충전가능 저장 전지들은 상기 DC 전력으로 충전되도록 구성되고,

상기 저장 전지들은 상기 안테나 및 상기 변환 회로와 공통 어셈블리에 수용되고, 상기 공통 어셈블리는 상기 전자 디바이스에 부착되도록 구성되는, 전력 회로.

청구항 7

제 6 항에 있어서,

상기 공통 어셈블리 내에 상기 재충전가능 저장 전지들과 상기 안테나 사이에 위치하는 차폐기를 더 포함하며,

상기 차폐기는 상기 안테나를 상기 재충전가능 저장 전지들로부터 전자기적으로 격리시키도록 구성되는, 전력 회로.

청구항 8

제 7 항에 있어서,

상기 차폐기는 페라이트 (ferrite) 재료를 포함하는, 전력 회로.

청구항 9

제 6 항에 있어서,

상기 공통 어셈블리는 상기 전자 디바이스의 기존 배터리를 대체하도록 구성되는, 전력 회로.

청구항 10

제 9 항에 있어서,

상기 공통 어셈블리는 상기 기존 배터리와 실질적으로 동일한 폼 팩터 및 실질적으로 동일한 전기 접점 위치를 가지는, 전력 회로.

청구항 11

제 9 항에 있어서,

상기 공통 어셈블리의 형상은 맞춤식 배터리, AA, AAA, C 셀, D 셀, 및 9-Volt 셀 중 적어도 하나에 따라 구성된 배터리 격납부 내에 맞도록 구성되는, 전력 회로.

청구항 12

제 9 항에 있어서,

상기 재충전가능 저장 전지들은 리튬 이온, 니켈 카드뮴, 및 니켈 금속수소화물 중 적어도 하나의 화학 조성을 포함하는, 전력 회로.

청구항 13

제 1 항에 있어서,

상기 전자 디바이스는 셀폰, 오디오 플레이어, 비디오 플레이어, PDA (personal digital assistant), 컴퓨터, 카메라, 완구, 도구, 리모콘 (remote control), 및 컴퓨터 마우스 중 적어도 하나로서 구성되는, 전력 회로.

청구항 14

제 1 항에 있어서,

상기 안테나 및 상기 변환 회로는 공통 어셈블리에 수용되고, 상기 공통 어셈블리는 상기 전자 디바이스에 외부적으로 부착하여 상기 변환 회로를 상기 기존 연결에 전기적으로 연결하도록 구성되는, 전력 회로.

청구항 15

전자 디바이스를 개장하는 방법으로서,

원래에는 안테나 및 변환 회로를 구비하지 않은 전자 디바이스와 기계적으로 및 전기적으로 결합하도록 상기 안테나 및 상기 변환 회로를 연결하는 단계;

송신 안테나에 의해 생성되는 근거리장 방사의 커플링 모드 구역으로부터 신호를 수신하는 단계; 및

상기 신호를 상기 전자 디바이스에 의해 사용될 DC 전력으로 변환하는 단계를 포함하는, 전자 디바이스 개장 방법.

청구항 16

제 15 항에 있어서,

상기 전자 디바이스에 의해 사용되는 상기 신호를 수신하는 단계 및 변환하는 단계는 상기 전자 디바이스로의 근거리장 통신 송신들을 수신하는 단계 및 변환하는 단계를 더 포함하는, 전자 디바이스 개장 방법.

청구항 17

제 15 항에 있어서,

상기 안테나의 무선 전력 커플링 중 전하를 저장하기 위해 상기 변환 회로에 재충전가능 저장 전지들을 연결하는 단계; 및

상기 전자 디바이스의 기존 배터리를 대체하도록 상기 재충전가능 저장 전지들, 상기 변환 회로, 및 상기 안테나를 공통 어셈블리에 수용하는 단계를 더 포함하는, 전자 디바이스 개장 방법.

청구항 18

제 15 항에 있어서,

상기 전자 디바이스에 맞도록 상기 안테나 및 상기 변환 회로를 연결하는 단계는 상기 전자 디바이스 내에 맞추어지도록 상기 안테나 및 상기 변환 회로를 공통 어셈블리에 수용하는 단계를 포함하는, 전자 디바이스 개장 방법.

청구항 19

제 18 항에 있어서,

상기 전자 디바이스에 맞도록 상기 안테나 및 상기 변환 회로를 공통 어셈블리에 수용하는 단계는 상기 안테나 및 상기 변환 회로를 상기 전자 디바이스의 상응하는 하우징부를 대체하도록 구성된 대체 하우징부와 통합형으로 형성하는 단계를 포함하는, 전자 디바이스 개장 방법.

청구항 20

원래에는 안테나 및 변환 회로를 구비하지 않은 전자 디바이스와 기계적으로 및 전기적으로 결합하도록 상기 안테나 및 상기 변환 회로를 연결하는 수단;

송신 안테나에 의해 생성되는 근거리장 방사의 커플링 모드 구역으로부터 신호를 수신하는 수단; 및

상기 신호를 상기 전자 디바이스에 의해 사용될 DC 전력으로 변환하는 수단을 포함하는, 무선 전력 수신기.

청구항 21

제 20 항에 있어서,

상기 신호를 상기 전자 디바이스를 위한 근거리장 통신 송신들로 변환하는 수단을 더 포함하는, 무선 전력 수신기.

청구항 22

제 20 항에 있어서,

상기 안테나의 무선 전력 커플링 중 전하를 저장하기 위해 상기 변환 회로에 재충전가능 저장 전지들을 연결하는 수단; 및

상기 전자 디바이스의 기존 배터리를 대체하도록 상기 재충전가능 저장 전지들, 상기 변환 회로, 및 상기 안테나를 공통 어셈블리에 수용하는 수단을 더 포함하는, 무선 전력 수신기.

청구항 23

제 20 항에 있어서,

상기 전자 디바이스에 맞도록 상기 안테나 및 상기 변환 회로를 연결하는 수단은 상기 전자 디바이스 내에 맞추어지도록 상기 안테나 및 상기 변환 회로를 공통 어셈블리에 수용하는 수단을 포함하는, 무선 전력 수신기.

청구항 24

제 23 항에 있어서,

상기 전자 디바이스에 맞도록 상기 안테나 및 상기 변환 회로를 공통 어셈블리에 수용하는 수단은 상기 안테나

및 상기 변환 회로를 상기 전자 디바이스의 상응하는 하우징부를 대체하도록 구성된 대체 하우징부와 통합형으로 형성하는 수단을 포함하는, 무선 전력 수신기.

청구항 25

전자 디바이스로서,

원래에는 상기 전자 디바이스의 일부가 아니었던 기능성을 부가하기 위한 개장 회로를 포함하며,

상기 개장 회로는:

외부 소스에 의해 생성되는 근거리장 방사의 커플링 모드 구역으로부터 신호를 수신하기 위한 안테나; 및

상기 신호를 전자 디바이스에 의해 사용되도록 변환하기 위한 변환 회로를 포함하며,

상기 안테나 및 상기 변환 회로는 원래에는 무선 전력 수신 기능이 구비되지 않았던 상기 전자 디바이스를 개장하도록 구성되는, 전자 디바이스.

청구항 26

제 25 항에 있어서,

상기 외부 소스는 무선 전력 송신기를 포함하는, 전자 디바이스.

청구항 27

제 26 항에 있어서,

상기 변환 회로 및 상기 전자 디바이스에 동작 가능하게 결합되는 개장 재충전가능 배터리를 더 포함하며, 상기 개장 재충전가능 배터리는 상기 변환 회로에 의해 충전되고 상기 전자 디바이스에 DC 전력을 제공하도록 구성되는, 전자 디바이스.

청구항 28

제 25 항에 있어서,

상기 안테나 및 상기 변환 회로는 상기 전자 디바이스가 근거리장 통신 데이터를 전송 및 수신 가능하도록 구성되는, 전자 디바이스.

명 세 서

기 술 분 야

[0001] 35 U.S.C. §119 하의 우선권 주장

[0002] 본 출원은 35 U.S.C. §119(e) 하에:

[0003] 2009년 2월 5일에 출원되고 본 출원의 양수인에게 양도된 것으로서 발명의 명칭이 "무선 전력 배터리 팩(WIRELESS POWER BATTERY PACK)"인 미국특허 가출원 제 61/150,257 호에 대해 우선권을 주장하며, 이 출원 전부는 본 명세서에 참조로서 통합되고;

[0004] 2009년 3월 25일에 출원되고 본 출원의 양수인에게 양도된 것으로서 발명의 명칭이 "내장 무선 전력 안테나를 구비한 배터리 어셈블리 (BATTERY ASSEMBLY WITH BUILT IN WIRELESS POWER ANTENNA)"인 미국특허 가출원 제 61/163,387 호에 대해 우선권을 주장하며, 이 출원 전부는 본 명세서에 참조로서 통합되고;

[0005] 2008년 11월 20일에 출원되고 본 출원의 양수인에게 양도된 것으로서 발명의 명칭이 "무선 전력 배터리 대체물(WIRELESS POWER BATTERY REPLACEMENT)"인 미국특허 가출원 제 61/116,608 호에 대해 우선권을 주장하며, 이 출원 전부는 본 명세서에 참조로서 통합된다.

[0006] 본 발명은 일반적으로 무선 충전에 관한 것으로, 보다 상세하게는 무선 전력 충전기들에 관련된 디바이스들, 시스템들, 및 방법들에 관한 것이다.

배 경 기 술

[0007] 통상적으로, 무선 통신 디바이스 (예컨대, 셀폰) 와 같이 배터리로 전력이 공급되는 각 디바이스는 자체의 충전기와, 일반적으로 AC 전력 콘센트인 전원을 요구한다. 이는 각각 별도로 충전기를 요구하는 다수의 디바이스들을 충전할 필요가 있을 때 거추장스러워질 수 있다.

[0008] 송신기와 충전될 전자 디바이스에 결합된 수신기 사이에 공중 (over-the-air) 혹은 무선 전력 송신을 사용하는 접근법들이 개발되고 있다. 이러한 접근법들은 일반적으로 두 부류에 속한다. 하나는 송신 안테나와 충전될 디바이스 상의 수신 안테나 사이 평면파 방사 (plane wave radiation) (혹은 원거리장 방사) 의 커플링에 기초한다. 수신 안테나는 방사된 전력을 수집하며 배터리를 충전하기 위해 방사된 전력을 정류한다. 커플링 효율을 향상시키기 위해 안테나들은 일반적으로 공진길이를 가진다. 이 접근법의 저너는 결점은, 안테나들 사이의 거리에 따라 전력 커플링이 신속히 떨어져서 합리적인 거리들 (예컨대, 1 내지 2 미터 미만) 사이의 충전이 어려워진다는 사실이다. 이에 더해, 송신 시스템이 평면파들을 방사하기 때문에, 필터링을 통해 올바로 제어되지 않으면 의도되지 않은 방사가 다른 시스템들에 간섭할 수 있다.

[0009] 무선 에너지 송신 거법들에 대한 다른 접근법들은, 예를 들어 "충전" 디바이스, 매트 (mat), 또는 표면에 내장된 송신 안테나와 충전될 호스트 전자 디바이스에 내장된 수신 안테나 (및 정류 회로) 사이의 유도 커플링에 기초한다. 이 접근법은 송신 및 수신 안테나들 사이의 간격이 매우 근접해야 한다는 (예컨대, 미터의 천분의 일 단위로) 단점을 가진다. 이 접근법은 동일한 영역 내 복수의 디바이스들을 동시에 충전할 수 있는 능력이 있지만, 이 영역은 통상적으로 매우 작으며 사용자가 디바이스들을 특정한 영역에 정확히 위치시키는 것이 요구된다.

[0010] 동시 충전에 따른 편의 증대에 더하여, 무선 충전과 관련하여 환경적 및 비용적 문제들도 고려될 수 있다. 현재, AA, AAA, D, C 셀, 9-Volt 등의 종류의 표준 크기 배터리들에 의해 전력이 공급되는 다수의 전자 디바이스들이 사용되고 있다. 이러한 배터리들은 1차 전지들 또는 재충전 가능한 2차 전지들일 수 있다. 1차 전지들은 폐기용으로서 환경 문제들을 야기한다. 재충전 가능한 2차 전지들은 환경적 우려에 응대함에 있어 도움이 될 수 있지만, 2차 전지들은 여전히 충전될 디바이스로부터 제거되는 것이 요구될 수 있는데, 이는 배터리들을 위한 제한된 공간, 통상적으로 4개의 공간만을 가지는 충전기에 재충전 가능한 2차 전지들을 배치하는 것을 포함할 수 있다. 무선 전력 충전의 장점들을 볼 때, 무선 충전장 (charging field) 에서 배터리들을 재충전시키거나 동작시키기 위해, 1차 또는 2차 전지들로부터 전력을 공급 받는 기존 디바이스들을 무선으로 전력을 공급하는 것이 가능한 디바이스가 되도록 변환 (즉, 개장) 시킬 필요가 있을 수 있다.

도면의 간단한 설명

[0011] 도 1 은 무선 전력 전달 시스템을 단순화하여 도시하는 블록도이다.

도 2 는 무선 전력 전달 시스템을 단순화하여 도시하는 개략도이다.

도 3a 는 본 발명의 예시적 실시예들에서 사용하기 위한 루프 안테나의 개략도이다.

도 3b 는 본 발명의 예시적 실시예들에서 사용되는 차등적 안테나의 대안적인 실시예의 도면이다.

도 4 는 본 발명의 예시적인 실시예에 따른 개장 회로를 가진 전자 디바이스의 도면이다.

도 5 는 본 발명의 예시적인 실시예에 따른 무선 전력공급을 위한 개장 회로를 가진 전자 디바이스의 도면이다.

도 6a 는 본 발명의 예시적인 실시예에 따른 통합형 저장 디바이스의 단면도이다.

도 6b 는 본 발명의 다른 예시적인 실시예에 따른 통합형 저장 디바이스의 단면도이다.

도 6c 는 본 발명의 예시적인 실시예에 따른 통합형 저장 디바이스의 사시도이다.

도 7 은 본 발명의 또 다른 예시적인 실시예에 따른 통합형 저장 디바이스의 도면이다.

발명을 실시하기 위한 구체적인 내용

[0012] 본 명세서에서 "예시적" 이라는 단어는 "예, 사례, 보기로서" 를 의미하는 것으로 사용된다. 본 명세서에 "예시적" 인 것으로 설명되는 어떠한 실시예는 다른 실시예들에 비해 반드시 바람직하거나 유리한 것으로 해석되어서는 아니 된다.

[0013] 첨부된 도면들과 연결하여 제시되는 이하의 상세한 설명은 본 발명의 예시적인 실시예들의 설명으로 의도된 것

이며, 본 발명을 그 실시예들로만 실시할 수 있다는 의미로 의도된 것이 아니다. 본 상세한 설명에 걸쳐 사용되는 "예시적" 이라는 단어는 "예, 사례, 보기로서" 를 의미하며 다른 실시예들에 비해 반드시 바람직하거나 유리한 것으로 해석되어서는 아니 될 것이다. 상세한 설명은 본 발명의 예시적 실시예들의 철저한 이해를 제공하는 목적으로 구체적인 세부점들을 포함한다. 해당 기술분야의 기술자라면 이러한 구체적인 세부점들 없이도 본 발명의 예시적인 실시예들이 실시될 수 있음을 인식할 것이다. 일부 사례들에서는, 본 명세서에 제시되는 예시적 실시예들의 신규성을 모호하게 하는 것을 피하기 위하여, 공지된 구조들 및 디바이스들이 블록도 형태로 도시된다.

[0014] 본 명세서에서 사용되는 단어들 "무선 전력" 은 전기장, 자기장, 전자기장, 또는 그 외 물리적 전자기 도체들의 사용 없이 송신기에서 수신기로 송신되는 것과 연관되는 어떠한 형태의 에너지를 의미하는 것으로 사용된다.

[0015] 도 1 은 본 발명의 다양한 예시적 실시예들에 따른 무선 송신 또는 충전 시스템 (100) 을 도시한다. 송신기 (104) 에는 에너지 전달을 제공하기 위한 방사장 (radiated field) (106) 을 생성하도록 입력 전력 (102) 이 제공된다. 수신기 (108) 는 방사장 (106) 에 커플링하고, 출력 전력 (110) 에 커플링된 디바이스 (미도시) 에 의한 저장 혹은 소비를 위해 출력 전력 (110) 을 생성한다. 송신기 (104) 및 수신기 (108) 양자는 거리 (112) 에 의해 이격되어 있다. 예시적인 일 실시예에서, 송신기 (104) 및 수신기 (108) 는 상호 공진 관계에 따라 구성되며, 수신기 (106) 의 공진 주파수와 송신기 (104) 의 공진 주파수가 정확히 매칭되면, 수신기 (108) 가 방사장 (106) 의 "근거리장 (near-field)" 에 위치할 때 송신기 (104) 와 수신기 (108) 사이의 송신 손실들이 최소화된다.

[0016] 송신기 (104) 는 에너지 송신의 수단을 제공하는 송신 안테나 (114) 를 더 포함하고, 수신기 (108) 는 에너지 수신의 수단을 제공하는 수신 안테나 (118) 를 더 포함한다. 송신 및 수신 안테나들은 이들에 연관될 어플리케이션들 및 디바이스들에 따라 크기가 정해진다. 전술한 바와 같이, 효율적인 에너지 전달은, 에너지의 대부분을 전자기파로서 원거리장으로 전파시키는 것보다는, 에너지의 큰 부분을 송신하는 안테나의 근거리장 내에서 수신하는 안테나에 커플링시킴으로써 발생한다. 근거리장에 있을 때, 송신 안테나 (114) 와 수신 안테나 (118) 사이에 커플링 모드가 개설될 수 있다. 근거리장 커플링이 발생할 수 있는 안테나들 (114 및 118) 주위의 영역은 본 명세서에서 커플링 모드 구역으로 지칭된다.

[0017] 도 2 는 무선 전력 전달 시스템을 단순화하여 도시하는 개략도이다. 송신기 (104) 는 발진기 (122), 전력 증폭기 (124), 및 필터 및 매칭 회로 (126) 를 포함한다. 발진기는 원하는 주파수의 발진기 신호를 생성하도록 구성되어 있는데, 이는 조절 신호 (123) 에 응대하여 조절될 수 있다. 발진기 신호는 제어 신호 (125) 에 응대하는 증폭량으로 전력 증폭기 (124) 에 의해 증폭될 수 있다. 고조파 또는 기타 원하지 않는 주파수들을 필터링하고 송신기 (104) 의 임피던스를 송신 안테나 (114) 에 매칭시키도록 필터 및 매칭 회로 (126) 가 포함될 수 있다.

[0018] 수신기 (108) 는 매칭 회로 (132) 및 정류 및 스위칭 회로 (134) 를 포함하여, 도 2 에 도시된 것과 같은 배터리 (136) 를 충전하거나 수신기 (미도시) 에 결합된 디바이스에 전력을 공급하도록 DC 전력 출력을 생성할 수 있다. 수신기 (108) 의 임피던스를 수신 안테나 (118) 에 매칭시키도록 매칭 회로 (132) 가 포함될 수 있다. 본 명세서에서 "배터리" 라는 용어는 충전 전지들 자체에 더해 초과전압 보호 회로들과 같은 부가 물체들을 포함할 수 있다.

[0019] 도 3a 에 도시된 바와 같이, 예시적 실시예들에서 사용되는 안테나들은 "루프" 안테나 (150) 로서 구성될 수 있는데, 본 명세서에서 이는 "자기" 안테나로 지칭될 수도 있다. 루프 안테나들은 에어 코어 (air core) 를 포함하거나 강자성 코어와 같은 물리적 코어를 포함하도록 구성될 수 있다. 에어 코어 루프 안테나들은 이종의 (extraneous) 물리적 디바이스들이 코어 근처에 배치되는 것에 대해 더 포용력일 수 있다. 더 나아가, 에어 코어 루프 안테나는 코어 영역 내에 다른 구성요소들의 배치를 허용한다. 또한, 에어 코어 루프는 송신 안테나 (114) (도 2) 의 커플 모드 구역이 보다 강할 수 있는 송신 안테나 (114) (도 2) 의 평면 내에 수신 안테나 (118) (도 2) 의 배치를 보다 용이하게 할 수 있다.

[0020] 전술한 바와 같이, 송신기 (104) 와 수신기 (108) 사이에 공진이 매칭 혹은 거의 매칭되었을 때 송신기 (104) 와 수신기 (108) 사이에 효율적인 에너지 전달이 발생한다. 그러나 송신기 (104) 와 수신기 (108) 사이에 공진이 매칭되지 않은 때에도, 에너지는 더 낮은 효율로 전달될 수 있다. 에너지의 전달은, 송신하는 안테나로부터 자유 공간으로 에너지를 전파시키는 것보다는, 송신하는 안테나의 근거리장으로부터 근거리장이 성립된 근방에 소재하는 수신하는 안테나로 에너지를 커플링함으로써 발생한다.

[0021] 루프 혹은 자기 안테나들의 공진 주파수는 인덕턴스 및 캐패시턴스에 기초한다. 루프 안테나에서의 인덕턴스는 일반적으로 루프에 의해 발생된 인덕턴스이고, 캐패시턴스는 일반적으로 루프 안테나의 인덕턴스에 더해져 원하는 공진 주파수의 공진 구조가 만들어진다. 비한정적인 예로서, 캐패시터 (152) 및 캐패시터 (154)를 안테나에 추가하여 공진 신호 (156) 를 생성하는 공진 회로를 만들 수 있다. 따라서 큰 직경의 루프 안테나들에서는, 루프의 직경 또는 인덕턴스가 증가함에 따라 공진을 유도하는 데 필요한 캐패시턴스의 크기는 감소한다. 더 나아가, 루프 혹은 자기 안테나의 직경이 증가함에 따라, 근거리장의 효율적인 에너지 전달 영역은 증가한다. 물론, 다른 공진 회로들도 가능하다. 또 하나의 비한정적인 예로서, 캐패시터가 루프 안테나의 두 터미널들 사이에 병렬로 배치될 수 있다. 또한, 해당 기술분야에서 통상의 지식을 가진 자라면 송신 안테나들에서 공진 신호 (156) 가 루프 안테나 (150) 로의 입력일 수 있음을 인식할 것이다.

[0022] 도 3b 는 본 발명의 예시적 실시예들에서 사용되는 차등적 안테나 (250) 의 대안적인 실시예를 도시한다. 안테나 (250) 는 차등적 코일 안테나로 구성될 수 있다. 차등적 안테나 구성에서는, 안테나 (250) 의 중심이 접지에 연결된다. 안테나 (250) 는, 도 3a 에서처럼 일단이 접지에 연결되는 것 대신, 양단이 수신기/송신기 유닛 (미도시) 에 연결된다. 안테나 (250) 에는 차등적 공진 신호를 생성하는 공진 회로를 만들도록 캐패시터들 (252, 253, 254) 이 추가될 수 있다. 차등적 안테나 구성은 통신이 양방향성이고 코일로의 송신이 요구되는 상황들에서 유용할 수 있다. 이러한 상황 한 가지로는 근거리장 통신 (NFC) 시스템들의 경우를 들 수 있다.

[0023] 본 발명의 예시적 실시예들은 서로의 근거리장들에 있는 두 안테나들 사이에 전력을 커플링하는 것을 포함한다. 전술한 바와 같이, 근거리장은 전자기장들이 존재하지만 안테나로부터 멀어지게 전파 또는 방사될 수 없는 안테나 주위의 영역이다. 근거리장은 통상적으로 안테나의 물리적 부피 근처의 부피로 한정된다. 본 발명의 예시적 실시예들에서, 단회전 및 다회전 루프 안테나들과 같은 자기형 안테나들이 송신 (Tx) 및 수신 (Rx) 안테나 시스템들 모두에서 사용되는데, 자기형 안테나들에서의 근거리 자기장 진폭들이 전기형 안테나 (예컨대, 소형 다이폴) 의 근거리 전기장에 비해 높은 경향이 있어 두 시스템들 사이에 잠재적으로 더 높은 커플링을 허용하기 때문이다. 그러나 "전기" 안테나들 (예컨대, 다이폴들 및 모노폴들) 또는 자기 및 전기 안테나들의 조합도 본 발명의 범위 내에 속하는 것으로 사료된다.

[0024] Tx 안테나는 전술한 원거리장 및 유도성 접근법들이 허용하는 것에 비해 현저히 더 큰 거리들에서 소형 Rx 안테나에 대해 우수한 커플링 (예컨대, > -4 dB) 을 획득하기에 충분히 낮은 주파수로, 그리고 충분히 큰 안테나 크기로 동작될 수 있다. Tx 안테나의 크기가 올바르게 결정되면, 구동되는 Tx 루프 안테나의 커플링 모드 구역 (즉, 근거리장) 내에 호스트 디바이스 상의 Rx 안테나가 배치될 때 높은 커플링 수준들 (예컨대, -1 내지 -4 dB) 을 획득할 수 있다.

[0025] 미래에는 전자 디바이스들이 무선 전력공급 및/또는 NFC 내장된 채 제조될 수 있다. 그러나 현재에는 무선 전력공급 기능이 없고 NFC 기능이 없는, 일반 폐기용 또는 재충전가능 배터리들을 사용하는 전자 디바이스들이 다수 사용되고 있다. 본 발명의 실시예들은 원래에는 무선 전력공급 기술 또는 NFC 가 내장되지 않았던 전자 디바이스들을 개장하는 실시예들을 포함하는데, 사용자들에게는 아직도 이러한 구식 전자 디바이스들이 존재한다. 이러한 실시예들에는 맞춤식 배터리 팩, 맞춤식 대체 하우징, 표준 배터리 팩의 개장 등이 포함된다.

[0026] 본 명세서에서 사용되는 "개장" 이라 함은, 기존 배터리 및 배터리 캐비티를 가지고 기존 배터리를 전자 디바이스 내에 저니기 위한 폼 팩터를 가지는 기존 전자 디바이스를, 기존 배터리를 충전하거나 기존 배터리 대체용으로서 전자 디바이스들 내에 설치된 새로운 배터리를 충전하기 위한 추가적인 기능성을 포함하도록 수정하는 것을 의미한다.

[0027] 도 4 는 본 발명의 예시적인 실시예에 따른 개장 회로를 가진 전자 디바이스 (400) 를 도시한다. 전자 디바이스 (400) 는 무선 전력 수신 안테나 (420) 및 변환 회로 (430) 를 가지는 백 하우징 (410) 을 포함할 수 있다. 전자 디바이스 (400) 는 전자 디바이스 (400) 를 위한 내부 전자 회로 (미도시) 를 포함하는 프론트 하우징 (440) 과 배터리 (450) 를 포함할 수 있다. 도 4 에 도시된 바와 같이, 백 하우징 (410) 은 프론트 하우징 (440) 으로부터 제거될 수 있다. 프론트 하우징 (440) 으로부터 백 하우징 (410) 이 제거 및 분리되면, 배터리 (450), 안테나 (420), 및 변환 회로 (430) 는 노출될 수 있다. 안테나 (420) 는 백 하우징 (410) 에 배치되거나 통합형으로 형성될 수 있다. 안테나 (420) 및 변환 회로 (430) 는 프론트 하우징 (440) 과는 별도로 백 하우징 (410) 과 함께 제조될 수 있다. 이에 따라, 백 하우징 (410) 은 기존 전자 디바이스들에 맞도록, 그러고 원래에는 무선 전력공급 기능이 없었던 전자 디바이스들의 상응하는 원래의 하우

정부들을 대체하도록 구성될 수 있다.

[0028] 안테나 (420) 및 변환 회로 (430) 는 외부 디바이스로부터 신호를 수신 및 변환하도록, 그리고 원래에는 안테나 (420) 또는 변환 회로 (430) 를 포함하지 않았던 전자 디바이스를 개장하도록 구성될 수 있다. 외부 소스는 무선 전력 송신기일 수 있으며, 안테나 (420) 및 변환 회로 (430) 는 신호를 수신 및 변환하여 전자 디바이스 (400) 를 위한 무선 전력을 생성하도록 더 구성될 수 있다. 이에 따라, 변환 회로 (430) 는 매칭 회로 (132) 및 정류 회로 (134) (도 2) 와 같은 무선 전력 수신 회로를 포함할 수 있다. 안테나 (420) 및 변환 회로 (430) 는 전자 디바이스가 NFC 데이터를 전송 및 수신할 수 있게 하도록 구성될 수도 있다.

[0029] NFC 를 위한 예시적 통신 메커니즘들 및 프로토콜들의 세부점들은 2008년 10월 10일에 출원되고 발명의 명칭이 "무선 전력 환경에서의 충전 신호 (SIGNALING CHARGING IN WIRELESS POWER ENVIRONMENT)" 인 미국 특허 출원 제 12/249,866 호에서 볼 수 있으며, 이 출원 전부는 본 명세서에 참조로서 통합된다.

[0030] 안테나 (420) 주위의 자기장 생성을 가능하게 하고 그 성능을 향상시키기 위해, 안테나 (420) 는 (다른 안테나들 또는 접지면들과 같은) 금속 장애물들 주위로 클리어런스 (clearance) 을 가지도록 라우팅 (routed) 될 수 있다. 일 실시예에서는, 변환 회로 (430) 가 ASIC 와 같은 별개의 (discrete) 구성요소로 구성될 수 있다.

동작 중에, 전자 디바이스 (400) 는 송신 안테나 (미도시) 의 범위 내에 배치될 수 있고, 배터리 (450) 가 전자 디바이스 (400) 로부터 제거되거나 전자 디바이스 (400) 가 AC 콘센트에 연결될 필요 없이 배터리 (450) 가 충전될 수 있다.

[0031] 동작시, 백 하우징 (410) 은 변환 회로 (430) 와 배터리 (450) 사이에 전기적 연결이 이루어지는 방식으로 프론트 하우징 (440) 에 연결되도록 구성될 수 있다. 변환 회로 (430) 와 배터리 (450) 사이의 전기적 연결은 변환 회로 (430) 의 접점들이 배터리 (450) 의 접점들과 접촉하여 전기 연결을 구축함으로써 이루어질 수 있다. (도 5 에 도시된 것과 같은) 대안적인 예시적 실시예는 변환 회로 (430) 로부터 연장하여 배터리 (450) 의 접점들과 전기적 접속을 구축하는 (케이블과 같은) 커넥터를 포함할 수 있다. 배터리 (450) 는 원래 전자 디바이스 (400) 를 동작시키도록 의도된 배터리일 수 있으나, 배터리 (450) 는 전자 디바이스 (400) 의 기존 배터리를 위한 폼 팩터에 맞고, 변환 회로 (430) 에 연결되고, 필요한 경우 안테나 (420) 및 변환 회로 (430) 를 위한 공간을 허용하도록 맞춤식으로 만들어질 수 있다.

[0032] 다른 예시적 실시예에서, 안테나 (420) 및 변환 회로 (430) 는, 예를 들면 키트 (kit) 의 형태로서, 백 하우징 (410) 과는 별도로 제조될 수 있다. 이러한 키트는 곧이어 원래에는 무선 전력 충전 또는 NFC 능력들이 없이 만들어진 전자 디바이스 (400) 내로 개장될 수 있다. 안테나 (420) 및 변환 회로 (430) 를 포함하는 키트는 전자 디바이스 (400) 에, 예를 들면 원래의 백 하우징 (410) 에, 부착되거나 포함되도록 구성될 수 있다.

이러한 부착 행위들은 사용자, 전자 디바이스 (400) 의 제공자, 또는 관련된 다른 주체에 의해 수행될 수 있다.

[0033] 배터리들이 재충전가능한지 결정하기 위해, 충전 디바이스 (즉, 개장된 안테나 (420) 및 변환 회로 (430)) 는 무선 충전 NFC 또는 기타 단거리 통신들 (예컨대, 지그비, 블루투스 등) 을 통해 전자 디바이스 (400) 와 통신하여 저장 전지들이 재충전을 위해 적합한지 (즉, 1차 전지들이 아닌지) 결정할 수 있다. 충전 디바이스는 또한 적절한 충전 프로토콜을 적용하기 위해 전자 디바이스 (400) 와 통신하여 배터리 기술 (예컨대, 니켈 카드뮴, 니켈 금속수소화물, 리튬 이온 등) 을 결정할 수도 있다.

[0034] 예시의 목적으로, 전자 디바이스 (400) 는 도 4 에 도시된 것과 같은 셀폰일 수 있다. 그러나 해당 기술분야에서 통상의 지식을 가진 자라면 본 발명의 예시적 실시예들이 이러한 전자 디바이스들로 한정되는 것은 아님을 인식할 것이다. 그 외의 전자 디바이스들에는 PDA (personal digital assistants), 오디오/비디오 디바이스, 카메라, 배터리에 의해 전력 공급되는 전동도구, 리모콘 (remote controls), 컴퓨터 마우스, 랩탑 컴퓨터, 및 기타 배터리에 의해 전력 공급되는 전자 디바이스들이 포함된다.

[0035] 도 5 는 본 발명의 예시적인 실시예에 따른 무선 전력공급을 위한 개장 회로를 가진 전자 디바이스 (500) 를 도시한다. 전자 디바이스 (500) 는 무선 전력 수신 안테나 (520) 및 무선 전력 수신 회로 (530) 를 가지는 백 하우징 (510) 을 포함할 수 있다. 전자 디바이스 (500) 는 전자 디바이스 (500) 의 동작을 위한 내부 전자 회로 (미도시) 를 포함하는 프론트 하우징 (540), 배터리 (미도시), 및 차폐기 (550) 를 포함할 수 있다.

도 5 에 도시된 바와 같이, 차폐기 (550) 는 배터리를 덮는다. 차폐기 (550) 는 배터리를 감쌀 수 있는 금속 캐이싱으로부터 안테나를 격리시키도록 구성될 수 있는데, 이에 대해서는 이후에 보다 상세히 설명될 것이다.

[0036] 도 5 에 도시된 바와 같이, 백 하우징 (510) 은 프론트 하우징 (540) 으로부터 제거될 수 있다. 프론트 하우징 (540) 으로부터 백 하우징 (510) 이 제거 및 분리되면, 차폐기 (550), 무선 전력 수신 안테나 (520), 및 무선 전력 수신 회로 (530) 는 노출될 수 있다. 무선 전력 수신 안테나 (520) 는 백 하우징 (510) 에 배치되거나 통합형으로 형성될 수 있다. 무선 전력 수신 안테나 (520) 및 무선 전력 수신 회로 (530)는 프론트 하우징 (540) 과는 별도로 백 하우징 (510) 과 함께 제조될 수 있다. 이에 따라, 백 하우징 (510) 은 기존 전자 디바이스들에 맞도록, 그리고 원래에는 무선 전력공급 기능이 없었던 전자 디바이스들의 상응하는 원래의 백 하우징들을 대체하도록 구성될 수 있다.

[0037] 동작시, 백 하우징 (510) 은 무선 전력 수신 회로 (520) 와 배터리 사이에 전기적 연결이 이루어지는 방식으로 프론트 하우징 (540) 에 연결되도록 구성될 수 있다. 무선 전력 수신 회로 (520) 와 배터리 사이의 전기적 연결은 무선 전력 수신 회로 (520) 의 접점들이 배터리의 접점들과 전기적으로 접속하여 전기 연결을 구축함으로써 이루어질 수 있다. 대안적으로는, 도 5 에 도시된 바와 같이 전자 디바이스 (500) 가, 무선 전력 충전 중에 배터리를 충전하기 위하여, 무선 전력 수신 회로 (520) 로부터 연장하고 차폐 (550) 를 통과하여 배터리의 접점들과 전기적 연결을 구축하는 (케이블과 같은) 커넥터 (560) 를 포함할 수 있다.

[0038] 도 6a 는 본 발명의 예시적인 실시예에 따른 통합형 저장 디바이스 (600) 의 단면도이다. 통합형 저장 디바이스 (600) 는 공통 하우징 봉입체 (610) 내에 저장 전지들 (620), 안테나 (630), 차폐기 (640), 및 기타 회로 (650) 를 포함한다.

[0039] 공통 하우징 봉입체 (610) 는 전자 디바이스에 사용되는 일반 배터리와 동일한 폼 팩터로 형상 및 치수가 정하여질 수 있다. 그러면 통합형 저장 디바이스 (600) 는 원래의 배터리를 대신하여 전자 디바이스 내에 삽입되어 송신 안테나 (따로서) 로부터 무선 전력으로 충전될 수 있는 배터리 (즉, 저장 전지들 (620)) 를 전자 디바이스에 제공할 수 있다. 통합형 저장 디바이스는 전술한 바와 같이 NFC 능력들을 포함할 수도 있다.

[0040] 커넥터 (660) 는 전자 디바이스에 전력을 제공하기 위해 전자 디바이스의 원래 배터리와 유사한 방식으로 전자 디바이스와 전기적 접속들을 만들도록 구성될 수 있다. 커넥터 (660) 는 도 6a 내지 도 6c 에 도시된 것과 같은 케이블일 수 있으며, 또는 대안적으로 보통의 배터리가 전자 디바이스에 전력을 공급하기 위해 접속할 접점들과 전기적 연결을 구축하는 일 세트의 접점들일 수 있다.

[0041] 안테나 (630) 는, 코일 안테나와 같이, 무선 전력 및 NFC 을 수신하도록 구성될 수 있다. 달리 표현하자면, 안테나는 무선 전력 송신들 또는 NFC 송신들을 또는 그 둘의 조합을 수신하도록 구성될 수 있다. 둘 모두를 수신하도록 구성된 경우, 안테나 (630) 는 무선 전력공급 시스템 및 전자 디바이스의 원래 전자계 양자에 의해 공유될 수 있는데, 이는 현재 그러한 능력들을 가지고 있지 않은 기존 전자 디바이스들에서 무선 전력공급 및 NFC 를 통합시키는 경제적인 방법일 수 있다.

[0042] 저장 전지들 (620) 은 임의의 종류의 배터리 저장 전지들로 구성될 수 있는데, 예를 들어 리튬 이온 배터리일 수 있다. 통합형 저장 디바이스 (620) 의 공통 하우징 봉입체 (610) 는 추가 회로를 가지면서도 전자 디바이스의 기존 배터리를 대체하도록 구성될 수 있으므로, 저장 전지들 (620) 의 물리적 영역은 전자 디바이스 내에서 통합형 저장 디바이스 (600) 대체할 기존 배터리 내의 상응하는 저장 전지들보다 물리적으로 작을 수 있다. 그러나 저장 전지들 (620) 은 이전 배터리의 저장 전지들에 비해 전기적으로 동일하거나 더 클 수 있다.

[0043] 차폐기 (640) 는 저장 전지들 (620) 과 안테나 (630) 사이에 위치하는, 자기장을 형성하는 보호 재료일 수 있다. 차폐기 (640) 는 저장 전지들 (620) 을 감쌀 수 있는 금속 케이싱으로부터 안테나를 격리시키도록 구성될 수 있다. 달리 표현하자면, 차폐기 (640) 는 자기장을 국부화시켜 저장 전지들 (620) 이 안테나 (630) 의 성능에 미칠 수 있는 방해성 효과들을 감소시키는 효과를 가질 수 있다. 차폐기는, 예컨대 일본 도쿄의 TDK 사에서 입수가능한 FLEXIELD 와 같은, 페라이트 (ferrite) 재료로 만들어질 수 있다.

[0044] 기타 회로 (650) 는 무선 전력공급 기능을 가지도록, 또는 NFC 기능을 가지도록, 또는 무선 전력공급 기능 및 NFC 기능을 모두 가지도록 전자 디바이스를 변환하는 능력을 통합형 저장 디바이스 (600) 에 제공할 수 있다. 이러한 회로의 예로는 도 2 에 관하여 전술한 매칭 회로 및 정류 회로가 포함된다. 기타 회로 (650) 는 또한, 초과 보호 회로가 저장 전지들 (620) 에 내장되어 있지 않다면, 초과전압 보호 회로를 포함할 수도 있다.

[0045] 이에 더해, 통합형 저장 디바이스 (600) 는 표시기 (예컨대, 시각적 또는 청각적) 를 포함할 수 있으며, 이는 연관 전자 디바이스가 무선 전력 송신 충전장의 범위 내에 있을 때 활성화 (예컨대, 발광다이오드로부터 광이

깜빡이거나 어떠한 청각적 표시를 통해) 될 수 있다. 통합형 저장 디바이스 (600) 는 또한, 자기장에 대한 추가적 로버스트성을 위해, 구성요소들을 감싸는 자기적으로 투명한 포장 재료를 포함할 수도 있다.

[0046] 동작시, 통합형 저장 디바이스 (600) 는 무선 전력 충전기의 송신기에 의해 생성되는 방사장 내에 있을 때 무선 전력을 수신하도록 구성될 수 있다. 무선 전력은 배터리와 같은 저장 전지들 (620) 내에 저장될 수 있다. 그러면 저장 전지들 (620) 로부터의 저장된 전하는 연관 전자 디바이스에 전력을 공급하는 데 사용될 수 있다. 대안적으로, 통합형 무선 저장 디바이스 (600) 에 의해 수신되는 전력은, 저장 전지들 (620) 에 저장되는 대신, 전자 디바이스에 직접 전력을 공급할 수 있다. 달리 표현하자면, 일 사용행태는 전자 디바이스에 전력을 공급하기 위한 저장 전지들 (620) 을 충전하는 것일 수 있고, 다른 사용행태는 전자 디바이스가 송신 안테나의 방사장 범위 내에 있는 경우 전자 디바이스에 직접 전력을 공급하는 것일 수 있다. 전술한 바와 같이, 무선 충전에는 송신하는 안테나가 충전될 전자 디바이스 내의 수신 안테나에 전력을 공급하고, 이어서 수신된 전력을 DC 전력으로 변환하는 정류 회로를 급전하는 것이 포함된다. DC 전력은 전자 디바이스의 배터리를 충전하거나 동시 동작을을 위한 전력을 제공할 수 있다. 일반적으로는, 통합형 저장 디바이스 (600) 가 수신 안테나 (630), 저장 전지들 (620) (예컨대, 배터리), 및 기타 회로 (650) (예컨대, 정류 회로와 또한 충전하는 송신 안테나에 신호를 보내기 위한 회로들) 를 전자 디바이스의 기존 배터리 팩을 대체하는 공통의 하우징 봉입체 (610) 내로 조합시킬 수 있다.

[0047] 대안적으로, 혹은 부가적으로, 통합형 저장 디바이스 (600) 는 전자 디바이스가 안테나 (630) 를 통해 NFC 를 전송 및 수신할 수 있게 하도록 구성될 수 있다. 기존 배터리 팩을 대체하도록 통합형 저장 디바이스 (600) 를 사용함으로써, 전자 디바이스는 소프트웨어 수정을 요구하지 않을 수 있다. 통합형 저장 디바이스 (600) 의 사용은 유리할 수 있는데, 다수의 전자 디바이스들은 전자 디바이스가 특정 전자 디바이스에 대한 맞춤식 AC 어댑터에 의해서만 충전될 수 있게 하는 맞춤식 소프트웨어를 가지기 때문이다. 기존 배터리 터미널에서 직접 충전하는 것은 이러한 소프트웨어 호환성 문제들을 완화시킬 수 있는데, 전자 디바이스 내의 소프트웨어에게는 전력이 일반 배터리에 의해 제공되는 것처럼 보일 것이기 때문이다. 이에 더해, 통합형 저장 디바이스 (600) 가 전자 디바이스의 기존 배터리의 크기 및 형상에 부합하도록 구성될 수 있기 때문에, 전자 디바이스 원래의 산업적 디자인이 유지될 수 있다. 이에 더해, 통합형 저장 디바이스 (600) 는 사용자가 기존 배터리 팩을 통합형 저장 디바이스 (600) 로 대체함으로써 현재의 전자 디바이스를 간단한 방법으로 업그레이드하게 할 수 있다.

[0048] 공통 하우징 봉입체 (610) 를 가진 통합형 저장 디바이스 (600) 는 상이한 통합형 저장 디바이스들 (600) 에 걸쳐 보다 일정한 공진을 유지하는 것을 가능하게 할 수 있다. 안테나 (630), 차폐기 (640), 및 저장 전지들 (620) 의 상대적 위치들 및 간격은 안테나 (630) 의 올바른 튜닝에 현저히 기여할 수 있다. 구성요소들 (예컨대, 저장 전지들 (620), 안테나 (630), 차폐기 (640) 등) 이 느슨하게 (loose) 있으면, 이러한 구성요소들 사이의 다양한 간격은 상이한 공진 주파수들이 얻어질 수 있다. 달리 표현하자면, 통합형 저장 디바이스 (600) 를 제공하면 무선 전력공급 또는 NFC 통신의 성능이 보다 신뢰성 있고 반복 가능하게 될 수 있다.

[0049] 도 6b 는 본 발명의 다른 예시적인 실시예에 따른 통합형 저장 디바이스 (600) 의 단면도이다. 통합형 저장 디바이스 (600) 는 커넥터 (660) 를 가진 공통 하우징 봉입체 (610) 내에 저장 전지들 (620), 안테나 (630), 차폐기 (640), 및 기타 회로 (650) 를 포함하며, 각각은 도 6a 에서와 같이 구성되어 있다. 통합형 저장 디바이스 (600) 는 추가적으로 수신 회로 (670) 를 포함하는데, 이는 기타 회로 (650) 와는 상이한 모듈 내에 있을 수 있다. 수신 회로 (670) 는 무선 전력공급 및/또는 NFC 변환과 관련된 회로를 포함할 수 있다. 이러한 회로의 예들에는 안테나 (630) 에 의해 수신된 전력을 DC 전력으로 변환하는 정류기, 필터, 및 조정기가 포함될 수 있다.

[0050] 도 6c 는 본 발명의 예시적인 실시예에 따른 통합형 저장 디바이스 (600) 의 사시도이다. 통합형 저장 디바이스 (600) 는 커넥터 (660) 를 가진 공통 하우징 봉입체 (610) 내에 저장 전지들 (620), 안테나 (630), 차폐기 (640), 및 기타 회로 (650) 를 포함하며, 각각은 도 6a 에서와 같이 구성되어 있다. 무선 전력 변환, NFC, 또는 그 조합을 위한 회로는 기타 회로 (650) 에 포함되거나, 도 6b 에 도시된 것과 같은 다른 모듈 (670) 내에 포함될 수 있다. 대안적으로는, NFC 및/또는 무선 전력 변환을 위한 회로가 통합형 저장 디바이스 (600) 의 외부에 수용될 수 있는데, 이와 같이 하는 데에는 통합형 저장 디바이스 (600) 외부에 안테나 (630) 연결들이 존재하는 것이 요구될 수 있다.

[0051] 도 7 은 본 발명의 또 다른 예시적인 실시예에 따른 통합형 저장 디바이스 (700) 를 도시한다. 통합형 저장 디바이스 (700) 는 기존 배터리의 형상 및 크기 (즉, 동일한 폼 팩터에 맞도록) 로 구성되고, 기존 배터리와 동일한 전극 연결들을 가져도록 구성될 수 있다. 예를 들어, 전자 디바이스가 AA 배터리들 (701 및

702) 과 같은 폐기용 배터리들에 의해 전력을 공급받을 수 있다. 이러한 배터리 종류들은 흔히 손전등 또는 완구와 같은 휴대용 전자 물체의 배터리 격납부에 사용될 수 있다. 본 예시적 실시예에서, 개장 배터리들 (701 및 702) 은 코일 안테나 (705) 를 포함하는데, 이는 배터리들 (701, 702) 의 외주면들 중 하나 혹은 둘 모두의 가장자리 주위로 배치될 수 있다. 이에 더해, 개장 배터리들 (701 및 702) 의 일부는 정류기, 필터, 조정기, 및 디바이스가 무선 전력, NFC, 또는 그 조합을 수신할 수 있게 하는 데 필요한 기타 회로를 포함하는 전자 회로 (710) 로 형성될 수 있다. 연관 전자 디바이스들, 또는 개장 배터리들 (701, 702) 을 별도로 송신 안테나의 커플링 모드 구역에 배치함으로써, 배터리 (702) 의 나머지 부분의 저장 전지들 (일반적으로 712, 714, 716 로 표시됨) 은 무선으로 충전될 수 있다.

[0052] 그러므로 통합형 저장 디바이스 (700) 는 공통 하우징 내에 양 저장 전지들 (712, 714, 716), 코일 안테나 (705), 및 연관 전자 회로 (710) 을 포함한다. 통합형 저장 디바이스 (700) 는, 새 무선충전 배터리 어셈블리에 의한 대체 배터리의 무선 충전을 가능하게 함으로써, 전자 디바이스가 무선 전력 수신에 따라 동작하도록 또는 NFC 기능이 가능해지도록 전자 디바이스를 개장하는 데 사용될 수 있다. 배터리 내의 저장 전지들이 사용하는 물리적 공간은 감소될 수 있는데, 배터리의 일부 영역이 추가적 전자 회로들을 위해 예비될 수 있기 때문이다. 그러나 배터리의 전기적 성능은 대체되는 기존 배터리들과 실질적으로 유사할 수 있다. 도 7 에는 AA 배터리들이 도시되었지만, 이러한 예시적 배터리 형상들 및 크기들은 한정적인 것으로 여겨져서는 아니 된다. 통합형 저장 디바이스들은, 예를 들면, AA, AAA, C 셀, D 셀, 9-Volt, 리튬 이온, 니켈 카드뮴, 및 니켈 금속 수소화물 배터리들처럼, 어떠한 종류의 배터리로든 그 형상 또는 크기가 정해지도록 구성될 수 있다.

[0053] 다른 예시적 실시예에서는, 어떠한 기존 전자 디바이스들의 하우징들이 너무 두껍거나 너무 많은 내부적 치폐를 제공할 수 있고, 이는 무선 충전장이 기존 전자 디바이스의 하우징을 투과하지 못하게 할 수 있다. 이러한 다른 예시적 실시예에서는, 도 4 내지 도 7 에서와 같은 무선 전력공급 기능을 가진 배터리들이 전자 디바이스로부터 제거되어 무선 전력장 내에, 예를 들면 충전 패드 상에, 배치될 수 있다. 이러한 배터리를 제거하는 것은 차폐된 영역으로부터 배터리를 제거하여 무선 커플링이 발생하는 것을 가능하게 할 수 있다. 무선 전력 수신을 통해 충전이 되면, 무선 전력공급 기능을 가진 배터리들이 전자 디바이스 내에 다시 배치될 수 있다.

[0054] 다른 예시적 실시예에서, 무선 전력 변환 하드웨어가 전자 디바이스에 외부적으로, 예컨대 전자 디바이스로의 DC 입력단에서, 연결되는 디바이스로 구성될 수 있다.

[0055] 본 명세서에서 설명된 접근법은 CDMA, WCDMA, OFDM, 802.11, GPS, 블루투스, LGE 등과 같은 다양한 통신 규격들에 적용 가능하다. 해당 기술분야에서 통상의 지식을 가진 자라면 다양한 기술들 및 기법들을 어떠한 것이든 사용하여 정보 및 신호들이 표현될 수 있음을 인식할 것이다. 예를 들어, 본 상세한 설명에 걸쳐 언급된 데이터, 지시어, 명령, 정보, 신호, 비트, 기호, 및 칩은 전압, 전류, 전자기파, 자기장 혹은 자기입자, 광학장 혹은 광입자, 또는 이들의 어떠한 조합으로 표현될 수 있다.

[0056] 해당 기술분야에서 통상의 지식을 가진 자라면 본 명세서에 개시된 예시적 실시예들과 연계하여 설명된 다양한 예시적 논리 블록, 모듈, 회로, 및 알고리즘 단계들이 전자 하드웨어, 컴퓨터 소프트웨어, 또는 그 조합으로 구현될 수 있음을 이해할 것이다. 하드웨어 및 소프트웨어의 상호교환성을 명확히 나타내기 위하여, 다양한 예시적 구성요소, 블록, 모듈, 회로, 및 단계는 상기에서 그 기능성 측면으로 일반적으로 설명되었다. 이러한 기능성이 하드웨어로 또는 소프트웨어로 구현될 것인지 여부는 전체 시스템에 부여된 특정 어플리케이션 및 디자인 제약들에 의존한다. 숙련된 기술자들은 설명된 기능성을 특정 어플리케이션 각각에 대해 다양한 방법들로 구현할 수 있으나, 이러한 구현형태 션택들이 본 발명의 예시적 실시예들의 범위에서 벗어나는 것으로 해석되어서는 아니 된다.

[0057] 본 명세서에 개시된 예시적 실시예들과 연계하여 설명된 다양한 예시적 논리 블록, 모듈, 및 회로는 본 명세서에 설명된 기능들을 수행하도록 설계된 범용 프로세서, 디지털 신호 프로세서 (DSP), 어플리케이션 전용 집적 회로 (ASIC), 필드 프로그래머블 게이트 어레이 (FPGA), 또는 기타 프로그래머블 로직 디바이스, 이산 게이트 또는 트랜지스터 로직, 이산 하드웨어 컴포넌트, 또는 이들의 어떠한 조합으로 구현 또는 수행될 수 있다. 범용 프로세서는 마이크로프로세서일 수 있으나, 대안적으로는, 프로세서가 임의의 종래 프로세서, 제어기, 마이크로컨트롤러, 또는 상태 기계일 수 있다. 프로세서는 또한 컴퓨팅 디바이스들의 조합으로서 구현될 수 있는데, 예를 들면, DSP 및 마이크로프로세서의 조합, 복수의 마이크로프로세서, DSP 코어와 연동하는 하나 이상의 마이크로프로세서, 또는 이와 같은 임의의 다른 구성으로서 구현될 수 있다.

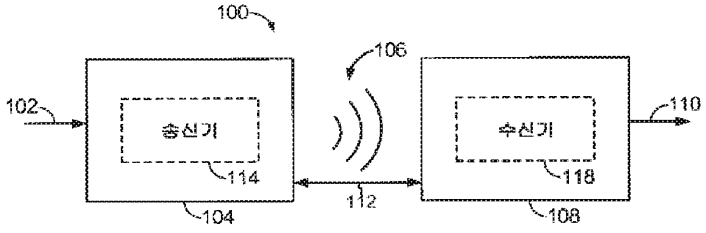
[0058] 본 명세서에 개시된 예시적 실시예들과 연계하여 설명된 방법 또는 알고리즘의 단계들은 직접적으로 하드웨어로, 또는 프로세서에 의해 실행되는 소프트웨어 모듈로, 또는 이 둘의 조합으로 구체화될 수 있다. 소프트웨어 모듈은 랜덤 액세스 메모리 (RAM), 플래시 메모리, 리드 온리 메모리 (ROM), 전기적 프로그래머블 ROM (EPROM), 전기적 소거가능 프로그래머블 ROM (EEPROM), 레지스터, 하드 디스크, 제거가능 디스크, CD-ROM, 또는 해당 기술분야에 공지된 기타 형태의 저장 매체 내에 존재할 수 있다. 예시적인 저장 매체는, 프로세서가 저장 매체로부터 정보를 판독하고 저장 매체에 정보를 기록할 수 있도록, 프로세서에 결합된다. 대안적으로는, 저장 매체가 프로세서에 통합될 수 있다. 프로세서 및 저장 매체는 ASIC 내에 존재할 수 있다. ASIC 는 사용자 터미널 내에 존재할 수 있다. 대안적으로는, 프로세서 및 저장 매체가 사용자 터미널 내에 별개의 구성요소들로 존재할 수 있다.

[0059] 하나 이상의 예시적 실시예들에서, 설명된 기능들은 하드웨어, 소프트웨어, 펌웨어, 또는 이들의 조합으로 구현될 수 있다. 소프트웨어로 구현되는 경우, 기능들은 컴퓨터 판독가능 매체 상의 하나 이상의 지시어 또는 코드 상에 저장되거나 이를 통해 송신될 수 있다. 컴퓨터 판독가능 매체는 한 장소에서 다른 장소로 컴퓨터 프로그램의 전달을 용이하게 하는 임의의 매체를 포함하는 컴퓨터 저장 매체 및 통신 매체를 포함한다. 저장 매체로는 컴퓨터에 의해 액세스 될 수 있는 이용 가능한 매체 어떠한 것이든 가능하다. 한정이 아닌 예로서, 이러한 컴퓨터 판독가능 매체는, 컴퓨터에 의해 액세스 될 수 있고 지시어들 또는 데이터 구조들 형태로 원하는 프로그램 코드를 수용 또는 저장하는 데 이용될 수 있는 RAM, ROM, EEPROM, CD-ROM 또는 기타 광 디스크 저장, 자기 디스크 저장, 또는 다른 자기 저장 디바이스, 또는 기타 매체를 포함할 수 있다. 또한, 어떠한 연결을 컴퓨터 판독가능 매체로 칭하는 것은 올바르다. 예를 들어, 동축 케이블, 광섬유 케이블, 연선 (twisted pair), DSL, 또는 적외선, 라디오, 및 마이크로파와 같은 무선 기술을 이용하여 웹사이트, 서버, 또는 기타 원격 소스로부터 소프트웨어가 송신된다면, 이러한 동축 케이블, 광섬유 케이블, 연선, DSL, 또는 적외선, 무선, 및 마이크로파와 같은 무선 기술은 매체의 정의 내에 포함된다. 본 명세서에서 사용되는 디스크 (disk) 및 디스크 (disc) 에는 컴팩트 디스크 (CD), 레이저 디스크, 광학 디스크, 디지털 다기능 디스크 (DVD), 플로피 디스크, 및 블루레이 디스크가 포함되는데, 여기서 디스크 (disk) 는 통상적으로 데이터를 자기적으로 재생하는 것이고, 디스크 (disc) 는 레이저를 이용하여 데이터를 광학적으로 재생하는 것이다. 상기의 조합들 또한 컴퓨터 판독가능 매체의 범위 내에 포함될 것이다.

[0060] 개시된 예시적 실시예들의 상기 설명은 해당 기술분야의 기술자로 하여금 본 발명을 제조 또는 사용할 수 있도록 제공되었다. 해당 분야의 기술자에게는 이러한 실시예들에 대한 다양한 수정예가 자명할 것이며, 여기에 정의된 일반적인 원리들은 본 발명의 기술적 사상 또는 범위로부터 벗어나지 않고도 다른 실시예들에 적용될 수 있다. 따라서 본 발명은 여기에 나타난 실시예들로 한정될 것이 아니라, 개시된 원리들 및 새로운 특징들과 부합하는 최광의의 범위에 따를 것이다.

도면

도면1



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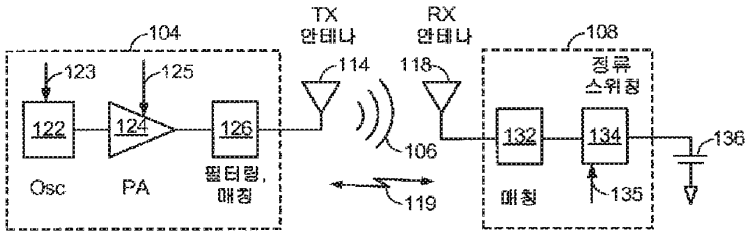
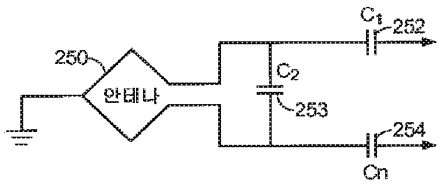
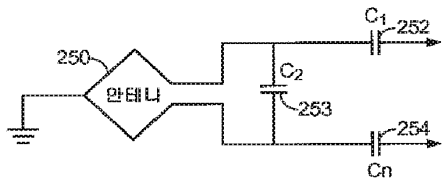


도면3a



도면3b



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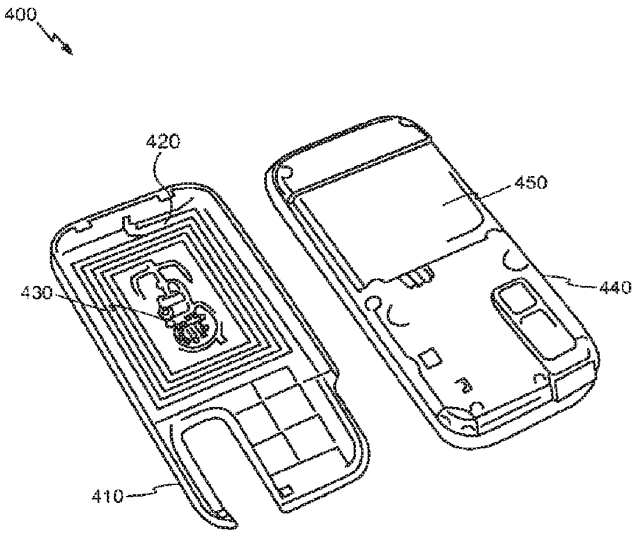
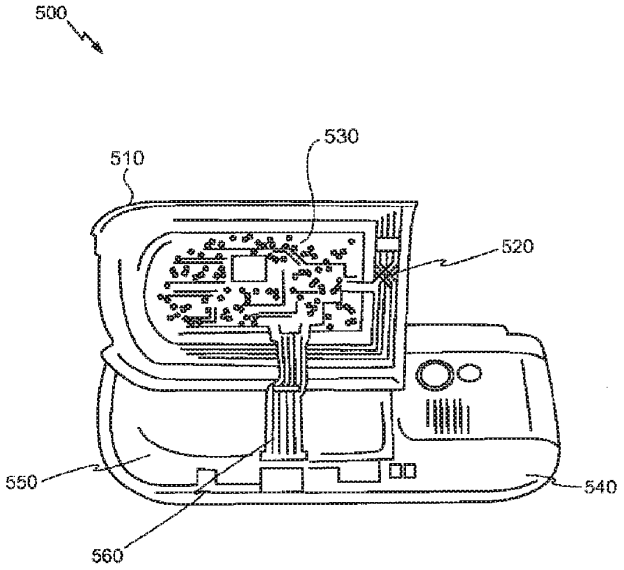
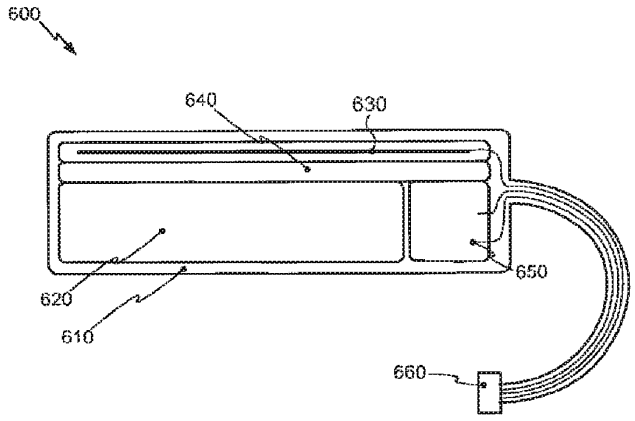


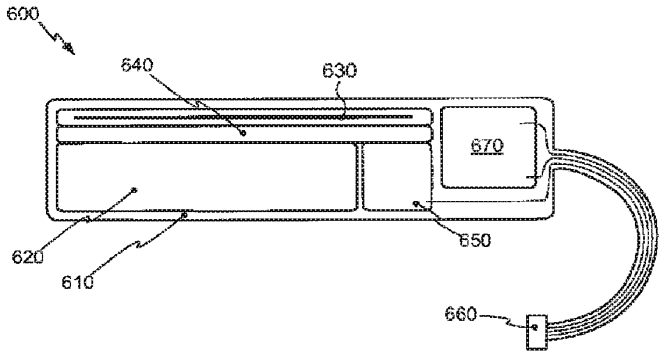
도면5



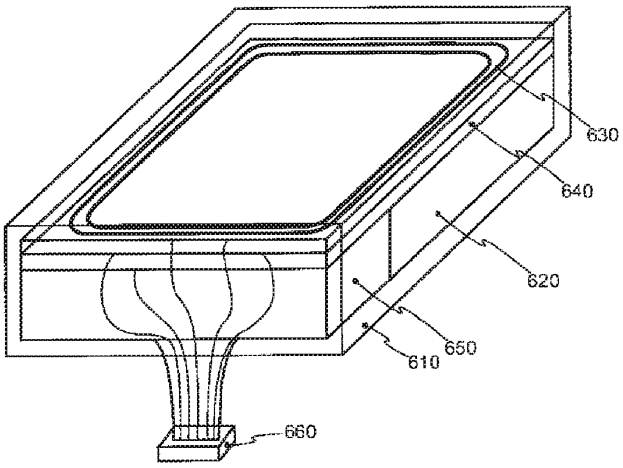
도면6a



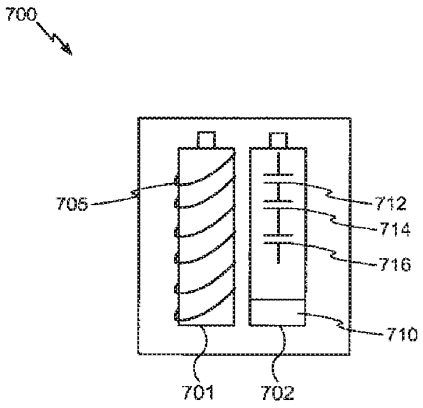
도면6b



도면6c



도면7



Electronic Patent Application Fee Transmittal

Application Number:	16182258
Filing Date:	06-Nov-2018
Title of Invention:	Wireless Power Receiver and Control Method Thereof
First Named Inventor/Applicant Name:	Ki Min LEE
Filer:	Jeff Lloyd/Larann Arzie
Attorney Docket Number:	SUN.LGI.417D3

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
SUBMISSION- INFORMATION DISCLOSURE STMT	1806	1	240	240
		Total in USD ($)		**240**

Electronic Acknowledgement Receipt	
EFS ID:	37793103
Application Number:	16182258
International Application Number:	
Confirmation Number:	1026
Title of Invention:	Wireless Power Receiver and Control Method Thereof
First Named Inventor/Applicant Name:	Ki Min LEE
Customer Number:	23557
Filer:	Jeff Lloyd/Larann Arzie
Filer Authorized By:	Jeff Lloyd
Attorney Docket Number:	SUN.LGI.417D3
Receipt Date:	19-NOV-2019
Filing Date:	06-NOV-2018
Time Stamp:	13:36:18
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$240
RAM confirmation Number	E2019AID37163941
Deposit Account	190065
Authorized User	Larann Arzie
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		SUN-LGI-417D3-SIDS3-AF.pdf	198119 593fb73e86081c033e0afff3fca5ed8d571553f3	yes	3
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Information Disclosure Statement (IDS) Form (SB08)		3	3	
	Transmittal Letter		1	2	
Warnings:					
Information:					
2	Foreign Reference	F1.pdf	629077 1e691eef2d6c2fe5a9d20e80dbc6828aa15dd3ea	no	19
Warnings:					
Information:					
3	Other Reference-Patent/App/Search documents	R1.pdf	93942 96e95871a9bc9169e98a2163227e508235563a84	no	7
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4	Fee Worksheet (SB06)	fee-info.pdf	30621 49d19785b7fca5c91021b23911f8c76129b603d6	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	951759		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

DocCode – SCORE

SCORE Placeholder Sheet for IFW Content

Application Number: 16182258 Document Date: 10/03/2019

The presence of this form in the IFW record indicates that the following document type was received in electronic format on the date identified above. This content is stored in the SCORE database.

Since this was an electronic submission, there is no physical artifact folder, no artifact folder is recorded in PALM, and no paper documents or physical media exist. The TIFF images in the IFW record were created from the original documents that are stored in SCORE.

- Drawing

At the time of document entry (noted above):

- USPTO employees may access SCORE content via DAV or via the SCORE web page.
- External customers may access SCORE content via PAIR using the Supplemental Content tab.

Form Revision Date: March 1, 2019

I hereby certify that this correspondence is being electronically transmitted via EFS to the United States Patent and Trademark Office on the date shown below:

30 OCTOBER 2019

Jeff Lloyd, Patent Attorney, Reg. No. 35,589

AMENDMENT AFTER
EX PARTE QUAYLE ACTION
Examining Group 2836
Patent Application
Docket No. SUN.LGI.417D3
Serial No. 16/182,258

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Examiner	:	Fritz M. Fleming
Art Unit	:	2836
Applicants	:	Ki Min Lee, Jung Oh Lee
Serial No.	:	16/182,258
Filed	:	November 6, 2018
Confirm. No.	:	1026
For	:	Wireless Power Receiver and Control Method Thereof

Mail Stop **Amendment**
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT AFTER *EX PARTE QUAYLE* ACTION

Sir:

Applicants request that the period for response be extended one month, through and including October 11, 2019, the fee for which was paid at the time this Amendment was filed.

As indicated in the Office Action dated July 11, 2019, the above-referenced application is in condition for allowance except for formal matters, and prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*. Please amend the subject application as follows:

J:\SUN\LGI\417D3\Amd-Resp\Response1.doc/ps/lcf

In the Specification

Please replace Figures 9 and 10 with the corrected drawing sheets attached hereto.

Please amend paragraph [0083] as follows:

[0083] First, referring to FIG. 9, after the short-range communication antenna 340 has been disposed on in the printed circuit board 301, the shielding unit 380 may be attached to one side of the printed circuit board 301 with an adhesive. The printed circuit board 301 comprises a plurality of layers wherein each layer of the plurality of layers is spaced apart from adjacent layers. The shielding unit 380 is disposed under the short-range communication antenna 340 or the receiving coil 310 (not shown in the Fig. 9). Referring still to FIG. 9, in a first region 411, at least one of the layers can overlap 405 the wireless power receiving coil in a vertical direction 400 perpendicular to an upper surface 385 of the shielding unit 380; and in a second region 412,413, at least one of the layers does not overlap the wireless power receiving coil in the vertical direction 400. Also, a first gap d1 or a first distance d1, measured in the vertical direction 400, between layers in the first region 411 can be greater than a second gap d2 or a second distance d2, measured in the vertical direction, between layers in the second region 412,413.

Please amend paragraph [0083] as follows:

[0084] Referring to FIG. 10, the printed circuit board 301 comprises a plurality of layers wherein each layer of the plurality of layers is spaced apart from adjacent layers, the short-range communication antenna 340 or the receiving coil 310 (not shown in the Fig. 10) is disposed in the printed circuit board 301. Moreover, the shielding unit 380 is disposed in the printed circuit board 301. The shielding unit 380 is disposed under the receiving coil 310 or the short-range communication antenna 340. The receiving coil 310 (not shown in the Fig. 10), the short-range communication antenna 340, and the shielding unit 380 are disposed between the plurality of layers of the printed circuit board 301. While the procedure of disposing the short-range communication antenna 340 or receiving coil(310)(not shown in the Fig. 10) in the printed circuit board 301 is being performed, the shielding unit 380 may be inserted into the printed circuit board 301. That is, unlike

FIG. 9, since the shielding unit 380 is disposed in the printed circuit board 301, the procedure of disposing the shielding unit 380 may be included in the procedure of disposing the short-range communication antenna 340 without performing the procedure of disposing the shielding unit 380 at one side of the printed circuit board 301. That is, as described above, according to the embodiment shown in FIG. 8, when the shielding unit 380 is inserted into the printed circuit board 301, the entire thickness of the wireless power receiver 300 may be reduced corresponding to the thickness of the adhesive 303. Thus, a separate procedure of attaching the shielding unit 380 is not necessary, so the manufacturing process may be simplified. Referring still to FIG. 10, in a first region 411, at least one of the layers can overlap 405 the wireless power receiving coil in a vertical direction 400 perpendicular to an upper surface 385 of the shielding unit 380; and in a second region 412,413, at least one of the layers does not overlap the wireless power receiving coil in the vertical direction 400. Also, a first gap d1 or a first distance d1, measured in the vertical direction 400, between layers in the first region 411 can be greater than a second gap d2 or a second distance d2, measured in the vertical direction, between layers in the second region 412,413.

Remarks

Claims 1, 2, and 21-38 are allowed. Applicants thank the Examiner for the indication of allowed claims. By this Amendment, the specification and Figures 9 and 10 are amended to clarify features shown in original Figures 9 and 10. No new matter has been introduced.

Objection to the specification

The specification has been objected to as failing to provide proper antecedent basis for the claimed subject matter. The specification has been amended to explicitly discuss features shown in the original figures. In view of the amendments to the specification presented herein, Applicants respectfully request reconsideration and withdrawal of this objection.

Objection to the drawings under 37 C.F.R. §1.83(a)

The drawings have been objected to under 37 C.F.R. §1.83(a). Figures 9 and 10 have been amended to include reference numerals for features shown in original Figures 9 and 10. In view of the replacement Figures 9 and 10 submitted herewith, Applicants respectfully request withdrawal of this objection.

In view of the foregoing remarks and amendments, Applicants believe that the claims as currently pending are in condition for allowance, and such action is respectfully requested.

Applicants invite the Examiner to call the undersigned if clarification is needed on any of this response, or if the Examiner believes a telephonic interview would expedite the prosecution of the subject application to completion.

The Commissioner is hereby authorized to charge any fees under 37 C.F.R. §§ 1.16 or 1.17 as required by this paper to Deposit Account 19-0065.

Respectfully submitted,

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JL/ps/lcf

Attachments: Replacement Figures 9 and 10

J:\SUN\LGI\417D3\Amd-Resp\Response1.doc/ps/lcf

FIG. 9

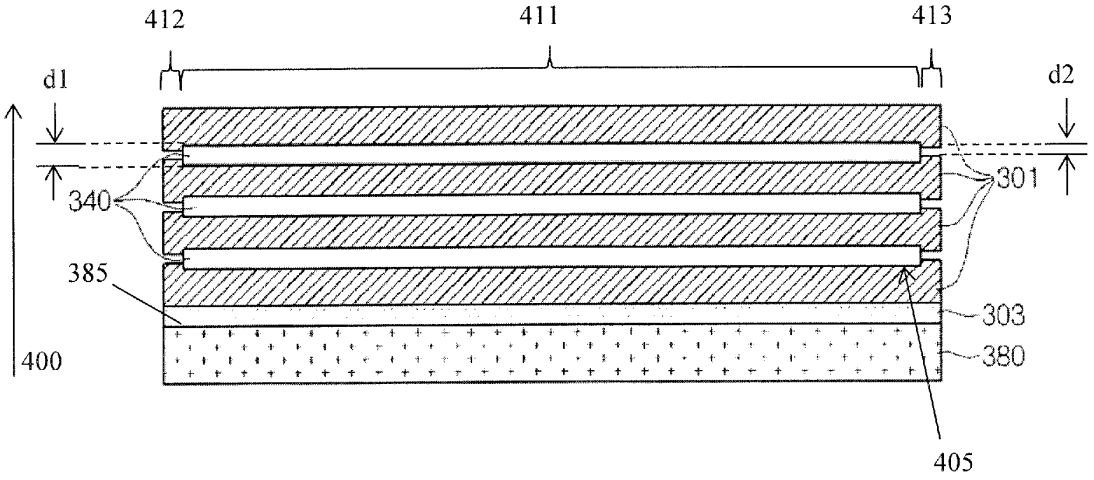
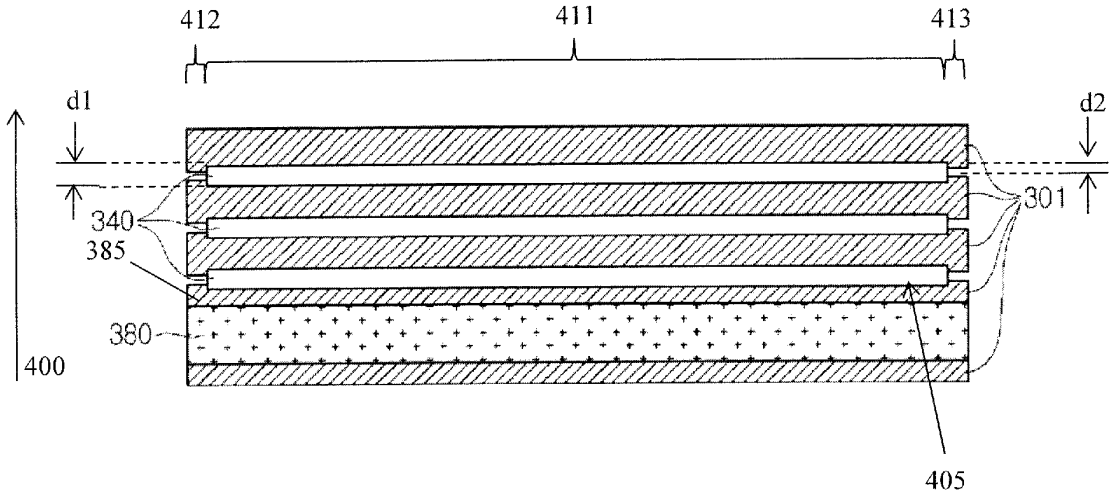


FIG. 10



Electronic Patent Application Fee Transmittal

Application Number:	16182258
Filing Date:	06-Nov-2018
Title of Invention:	Wireless Power Receiver and Control Method Thereof
First Named Inventor/Applicant Name:	Ki Min LEE
Filer:	Jeff Lloyd/Larann Arzie
Attorney Docket Number:	SUN.LGI.417D3

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension - 1 month with $0 paid	1251	1	200	200
Miscellaneous:				
		Total in USD ($)		**200**

Electronic Acknowledgement Receipt	
EFS ID:	37360612
Application Number:	16182258
International Application Number:	
Confirmation Number:	1026
Title of Invention:	Wireless Power Receiver and Control Method Thereof
First Named Inventor/Applicant Name:	Ki Min LEE
Customer Number:	23557
Filer:	Jeff Lloyd/Larann Arzie
Filer Authorized By:	Jeff Lloyd
Attorney Docket Number:	SUN.LGI.417D3
Receipt Date:	03-OCT-2019
Filing Date:	06-NOV-2018
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Payment information:

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Payment Type	CARD
Payment was successfully received in RAM	$200
RAM confirmation Number	E201903G25004097
Deposit Account	190065
Authorized User	Larann Arzie
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		SUN-LGI-417D3-Response1-AF.pdf	373711 49bfea9ad7d595dd5d2f5ba4f48143a9d7d97126	yes	7

Multipart Description/PDF files in .zip description

Document Description	Start	End
Response after Ex Parte Quayle Action	1	1
Specification	2	3
Applicant Arguments/Remarks Made in an Amendment	4	5
Drawings-other than black and white line drawings	6	7

Warnings:

Information:

2	Fee Worksheet (SB06)	fee-info.pdf	30822 0659923e100bf463bc1f8f4bda132a1b84dad6ea	no	2

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National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	16/182,258
Filing Date	November 6, 2018
First Named Inventor	Ki Min LEE
Art Unit	2836
Examiner Name	Fleming, Fritz M.
Attorney Docket Number	SUN.LGI.417D3

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. [1]	Document Number Number - Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	U1	2004/0085247-A1	05-06-2004	Mickle et al.	ALL
	U2	2007/0069961-A1	03-29-2007	Akiho et al.	ALL

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. [1]	Foreign Patent Document Country Code [3] - Number [4] - Kind Code [5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
	F1	JP-2006-319223-A (with English Abstract)	11-24-2006	MURATA MFG CO LTD	ALL	

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. [1]	Include name of the author (in CAPITAL LETTERS), title of the article, (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	R1	European Search Report dated June 25, 2019 in European Application No. 19159579.2.	

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] Applicant's unique citation designation number (optional). [2] Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

Bibliographic data: JP2006319223 (A) — 2006-11-24

LAMINATED COIL

Inventor(s): MAEDA HIDEKAZU; YAMAGUCHI KOICHI; HAMANO MORIHIRO ± (MAEDA HIDEKAZU, ; YAMAGUCHI KOICHI, ; HAMANO MORIHIRO)

Applicant(s): MURATA MANUFACTURING CO ± (MURATA MFG CO LTD)

Classification: **- international:** ***H01F17/00***
- cooperative:

Application number: JP20050141970 20050513 Global Dossier

Priority number (s): JP20050141970 20050513

Abstract of JP2006319223 (A)

PROBLEM TO BE SOLVED: To provide a laminated coil that improves the directivity and use efficiency of flux arising from a coil. ;SOLUTION: This laminated coil is fabricated by incorporating a coil 15 made by spirally winding multiple coil conductors 16 into a laminated body 11 of ceramics, and forming an external electrode at both ends of the laminated body 11. A laminated body area with coil conductors 16 formed is made of a nonmagnetic material layer 12, an inner area with coil conductors 16 formed is made of a first magnetic material layer 13, and a second magnetic material layer 14 is made at the lower side of the nonmagnetic material layer 12 and the first magnetic material layer 13. ;COPYRIGHT: (C)2007,JPO&INPIT

(19)日本国特許庁(JP)　(12)公開特許公報(A)　(11)特許出願公開番号
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	H01F 17/00	D	

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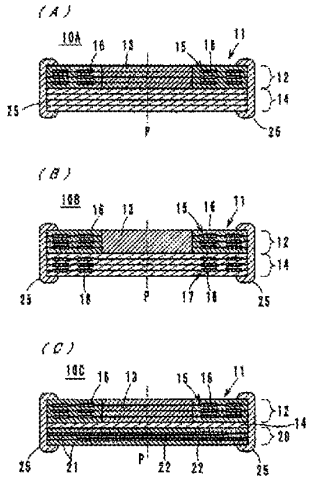
Ｆターム(参考)　5E070 AA01　AB01　BA12　CB02　CB13
EA01

(54)【発明の名称】積層コイル

(57)【要約】
【課題】　コイルから発生する磁界の指向性及び磁束の利用効率の向上を図ることのできる積層コイルを提供する。
【解決手段】　セラミック層からなる積層体１１に、複数のコイル導体１６を螺旋状に接続してなるコイル１５を内蔵し、積層体１１の両端部に外部電極を形成した積層コイル。コイル導体１６が形成されている積層体領域は非磁性体層１２からなり、コイル導体１６が形成されている領域の内側領域は第１磁性体層１３からなり、非磁性体層１２及び第１磁性体層１３の下側には第２磁性体層１４が積層されている。
【選択図】　図１



【特許請求の範囲】
【請求項1】
複数のセラミック層からなる積層体に、複数のコイル導体を螺旋状に接続してなるコイルを内蔵し、積層体の両端部に該コイルのコイル軸と直交する方向に対向する外部電極を形成した積層コイルにおいて、
前記コイル導体が形成されている積層体領域は非磁性体層からなり、
前記コイル導体が形成されている積層体領域の内側領域は第１磁性体層からなり、
前記非磁性体層及び前記第１磁性体層に対して積層方向に隣接した第２磁性体層を備えていること、
を特徴とする積層コイル。
【請求項2】
前記コイルは複数のコイル導体をスパイラル状に接続してなることを特徴とする請求項１に記載の積層コイル。
【請求項3】
前記第２磁性体層の複素比透磁率の虚数部が前記第１磁性体層の複素比透磁率の虚数部よりも小さいことを特徴とする請求項１又は請求項２に記載の積層コイル。
【請求項4】
前記第２磁性体層にもコイルが形成されていることを特徴とする請求項１ないし請求項３のいずれかに記載の積層コイル。
【請求項5】
前記第２磁性体層に対して前記第１磁性体層とは反対側に隣接した容量部を備えたことを特徴とする請求項１ないし請求項４のいずれかに記載の積層コイル。

【発明の詳細な説明】
【技術分野】
【0001】
本発明は、積層コイル、特に、セラミック積層体にコイルを内蔵した積層コイルに関する。
【背景技術】
【0002】
従来から、この種の積層コイルとしては種々のものが提供されており、例えば、特許文献１には、図１０に示すように、複数の非磁性体シート２上に形成した複数のコイル導体６を電気的に接続して螺旋状のコイル５を構成し、該コイル５の内側（巻芯部）に磁性体シート３を設けた積層コイル１が開示されている。なお、符号７，７は外部電極を示し、それぞれコイル５の端部に電気的に接続されている。
【0003】
この積層コイル１においては、コイル５の巻芯部に磁性体層が形成されているため、図１１に模式的に示すように、磁界がコイル軸上に指向することになるが、磁界は積層コイルの上下方向に分散する。そのため、この積層コイルをチップコイルアンテナとして、上方に発生する磁束のみを利用する場合、下方に発生する磁束は漏れ磁束となってしまい、磁束の利用効率が低下するという問題点を有していた。
【特許文献1】特公平２－６４４５号公報
【発明の開示】
【発明が解決しようとする課題】
【0004】
そこで、本発明の目的は、コイルから発生する磁界の指向性及び磁束の利用効率の向上を図ることのできる積層コイルを提供することにある。
【課題を解決するための手段】
【0005】
前記目的を達成するため、本発明に係る積層コイルは、複数のセラミック層からなる積

層体に、複数のコイル導体を螺旋状に接続してなるコイルを内蔵し、積層体の両端部に該コイルのコイル軸と直交する方向に対向する外部電極を形成した積層コイルにおいて、コイル導体が形成されている積層体領域は非磁性体層からなり、コイル導体が形成されている積層体領域の内側領域は第１磁性体層からなり、非磁性体層及び第１磁性体層に対して積層方向に隣接した第２磁性体層を備えていることを特徴とする。

【0006】

本発明に係る積層コイルにおいては、コイルの内側（巻芯部）には第１磁性体層が存在するため、磁界がコイル軸上に指向することとなり、かつ、第２磁性体層によって磁束の漏れが防止され、磁束は第２磁性体層とは反対側により多く集中することになる。

【0007】

本発明に係る積層コイルにおいて、コイルは複数のコイル導体をスパイラル状に接続してなることが好ましい。磁界密度を高めて磁束をより多く発生させることができる。また、第２磁性体層の複素比透磁率の虚数部が第１磁性体層の複素比透磁率の虚数部よりも小さいことが好ましく、損失を小さくすることができる。

【0008】

さらに、第２磁性体層にもコイルが形成されていてもよい。コイルから生じる磁界密度をより高くすることができる。また、第２磁性体層に対して第１磁性体層とは反対側に隣接した容量部を備えていてもよい。ＬＣ共振器を構成でき、かつ、容量部に磁界の影響が及ぶことを抑えることができる。

【発明の効果】

【0009】

本発明によれば、コイルの内側（巻芯部）に第１磁性体層を設けたため、コイルから発生する磁界がコイル軸上に指向することとなり、かつ、第２磁性体層によって磁束の漏れが防止され、磁束は第２磁性体層とは反対側により多く集中し、漏れ磁束を少なくして磁束を有効に利用することができる。

【発明を実施するための最良の形態】

【0010】

以下、本発明に係る積層コイルの実施例を添付図面を参照して説明する。

【0011】

（実施例１，２，３、図１及び図２参照）

本発明に係る積層コイルの実施例１を図１（Ａ）に示し、実施例２を図１（Ｂ）に示し、実施例３を図１（Ｃ）に示す。

【0012】

図１（Ａ）に示す実施例１（積層コイル１０Ａ）は、スパイラル状のコイル導体１６の両端部を図示しないビアホール導体にて螺旋状に接続してなるコイル１５を内蔵した非磁性体層１２と、該コイル１５の内側（巻芯部）に設けた第１磁性体層１３と、非磁性体層１２及び第１磁性体層１３の下部に積層した第２磁性体層１４とで積層体１１を構成したものである。

【0013】

積層体１１の両端部にはコイル１５のコイル軸Ｐと直交する方向に対向する外部電極２５，２５が形成され、この外部電極２５，２５はそれぞれコイル１５の端部と電気的に接続されている。

【0014】

図１（Ｂ）に示す実施例２（積層コイル１０Ｂ）は、スパイラル状のコイル導体１６の両端部を図示しないビアホール導体にて螺旋状に接続してなるコイル１５を内蔵した非磁性体層１２と、該コイル１５の内側（巻芯部）に設けた第１磁性体層１３と、非磁性体層１２及び第１磁性体層１３の下部に積層した第２磁性体層１４とで積層体１１を構成したものである。

【0015】

さらに、第２磁性体層１４にもコイル１７が形成されている。コイル１７は、前記コイ

ル１５と同様に、コイル導体１８の両端部を図示しないビアホール導体にてコイル１５と同軸上で螺旋状に接続してなるもので、コイル１５とは直列に接続されている。また、積層体１１の両端部にはコイル１５，１７のコイル軸Ｐと直交する方向に対向する外部電極２５，２５が形成され、この外部電極２５，２５はそれぞれコイル１５，１７の端部と電気的に接続されている。

【0016】

図１（Ｃ）に示す実施例３（積層コイル１０Ｃ）は、スパイラル状のコイル導体１６の両端部を図示しないビアホール導体にて螺旋状に接続してなるコイル１５を内蔵した非磁性体層１２と、該コイル１５の内側（巻芯部）に設けた第１磁性体層１３と、非磁性体層１２及び第１磁性体層１３の下部に積層した第２磁性体層１４と、第２磁性体層１４の下側に積層した容量部２０とで積層体１１を構成したものである。

【0017】

容量部２０は、コンデンサ電極２２，２２を形成した非磁性体（誘電体）シート２１を積層したものである。また、積層体１１の両端部にはコイル１５のコイル軸Ｐと直交する方向に対向する外部電極２５，２５が形成され、この外部電極２５，２５はそれぞれコイル１５の端部及びコンデンサ電極２２，２２の端部と電気的に接続されている。

【0018】

図２に前記積層コイル１０（１０Ａ，１０Ｂ，１０Ｃ）の外観を示し、第１磁性体層１３は平面視で矩形形状（図２（Ａ）参照）であってもよく、あるいは、円形状（図２（Ｂ）参照）であってもよい。また、楕円など他の形状であってもよい。

【0019】

（実施例１の製造方法、図３及び図４参照）

ここで、実施例１である積層コイル１０Ａの製造方法について説明する。図３（Ａ）に示すように、まず、フェライト製非磁性体シート１２ａの中央部分にフェライト製磁性体シート１３ａを埋め込んだ複数枚のシートを用意する。このシート上にコイル導体１６を導体ペーストにて所定のパターンにスクリーン印刷し、かつ、コイル導体１６の端部に必要に応じて層間接続用のビアホール導体（図示せず）を形成する。なお、実施例１では図３（Ａ）に示すように、コイル導体１６をスパイラル状にシート１２ａ上に印刷している。

【0020】

前記シートは、図４（Ａ）に示すように、キャリアテープ３０で裏打ちされた非磁性体シート１２ａに形成された矩形の開口部１２ａ’に、磁性体シート１３ａを埋め込む（図４（Ｂ）参照）。その後、非磁性体シート１２ａ上にコイル導体１６をスクリーン印刷する（図４（Ｃ）参照）。

【0021】

前記シートを積層／圧着し、さらに、その下側に所定枚数のフェライト製磁性体シート１４ａを積層／圧着し、所定サイズにカットした後、脱脂／焼成して積層体１１とする（図３（Ｂ）参照）。この積層体１１の両端部に導体ペーストを塗布・焼き付けし、コイル導体１６の引出し部１６ａ，１６ａと電気的に接続した外部電極２５，２５を形成する（図３（Ｃ）参照）。焼き付けられた外部電極２５，２５上にはさらにはんだとの親和性を良好にするめっきが施される。なお、圧着工程は各シートを積層した後に１回だけ行うようにしてもよい。

【0022】

ところで、前記非磁性体シート１２ａは以下のようにして製作される。酸化第二鉄（Fe_2O_3）、酸化亜鉛（ＺｎＯ）及び酸化銅（ＣｕＯ）を所定の比率で秤量したそれぞれの材料を原材料としてボールミルに投入し、湿式調合を行う。得られた混合物を乾燥してから粉砕し、得られた粉末を７５０℃で１時間仮焼する。得られた仮焼粉末をボールミルにて湿式粉砕した後、乾燥してから解砕し、非磁性体セラミック粉末を得る。

【0023】

この非磁性体セラミック粉末に対して結合剤と可塑剤、湿潤材、分散剤とを加えてボー

ルミルで混合した後、減圧により脱泡する。得られたセラミックスラリーをドクターブレードを用いてシート状に成形して乾燥させ、所望の膜厚の非磁性体セラミックグリーンシートを製作する。

【0024】

また、磁性体シート１３ａ（以下に説明する磁性体シート１４ａも同じ）は以下のようにして製作される。酸化第二鉄（Fe_2O_3）、酸化亜鉛（ＺｎＯ）、酸化ニッケル（ＮｉＯ）及び酸化銅（ＣｕＯ）を所定の比率で秤量したそれぞれの材料を原材料としてボールミルに投入し、湿式調合を行う。得られた混合物を乾燥してから粉砕し、得られた粉末を７５０℃で１時間仮焼する。得られた仮焼粉末をボールミルにて湿式粉砕した後、乾燥してから解砕し、磁性体セラミック粉末を得る。

【0025】

この磁性体セラミック粉末に対して結合剤と可塑剤、湿潤材、分散剤とを加えてボールミルで混合した後、減圧により脱泡する。得られたセラミックスラリーをドクターブレードを用いてシート状に成形して乾燥させ、所望の膜厚の磁性体セラミックグリーンシートを製作する。

【0026】

（実施例２の製造方法、図５及び図６参照）

次に、実施例２である積層コイル１０Ｂの製造方法について説明する。図５（Ａ）に示すように、まず、フェライト製非磁性体シート１２ａ上にコイル導体１６を導体ペーストにて所定のパターンにスクリーン印刷し、かつ、コイル導体１６の端部に必要に応じて層間接続用のビアホール導体（図示せず）を形成する。さらに、シート１２ａの中央部分に矩形の開口部１２ａ’を形成する。なお、実施例２では図５（Ａ）に示すように、コイル導体１６をスパイラル状にシート１２ａ上に印刷している。

【0027】

前記非磁性体シート１２ａは、図６（Ａ）に示すように、キャリアテープ３０で裏打ちされた状態でコイル導体１６をスクリーン印刷した後、キャリアテープ３０とともに開口部１２ａ’を矩形状に打ち抜き形成する（図６（Ｂ）参照）。

【0028】

前記非磁性体シート１２ａを積層／圧着し、さらに、その下側に所定枚数のフェライト製磁性体シート１４ａを積層／圧着し、所定サイズにカットする（図５（Ｂ）参照）。なお、圧着工程は各シートを積層した後に１回だけ行うようにしてもよい。また、磁性体シート１４ａを積層する工程は、図６（Ｃ）に示すように、キャリアテープ３０で裏打ちされたシート１４ａを１枚ずつ積層体上に重ね合わせていく。なお、この工程は前記実施例１でも同様である。

【0029】

その後、開口部１２ａ’に磁性体材料を充填して磁性体層１３を形成し、脱脂／焼成して積層体１１とする（図５（Ｃ）参照）。なお、実施例２では、磁性体材料として磁性体セラミック粉末を用いた。具体的には、磁性体セラミック粉末を金型に入れて圧着した磁性体ユニットを開口部１２ａ’に埋め込む。この積層体１１の両端部に導体ペーストを塗布・焼き付けし、コイル導体１６の引出し部１６ａ，１６ａと電気的に接続した外部電極２５，２５を形成する（図５（Ｄ）参照）。焼き付けられた外部電極２５、２５上にはさらにはんだとの親和性を良好にするめっきが施される。

【0030】

（実施例３の製造方法、図７参照）

実施例３である積層コイル１０Ｃの製造方法は、図７に示すように、基本的には前記実施例１と同様である。即ち、フェライト製非磁性体シート１２ａの中央部分にフェライト製磁性体シート１３ａを埋め込んだ複数枚のシートを用意し、このシート上にコイル導体１６を導体ペーストにて所定のパターンにスクリーン印刷し、かつ、コイル導体１６の端部に必要に応じて層間接続用のビアホール導体（図示せず）を形成する。この工程は図４にて説明したとおりである。

【0031】
前記シートを積層／圧着し、さらに、その下側に所定枚数のフェライト製磁性体シート１４ａを積層／圧着する。さらに、コンデンサ電極２２を形成したセラミック製非磁性体（誘電体）シート２１を積層／圧着して容量部２０とし、所定サイズにカットした後、脱脂／焼成して積層体１１とする。この積層体１１の両端部に導体ペーストを塗布・焼き付けし、コイル導体１６の引出し部１６ａ，１６ａ及びコンデンサ電極２２の端部２２ａと電気的に接続した外部電極２５，２５を形成する。焼き付けられた外部電極２５，２５上にはさらにはんだとの親和性を良好にするめっきが施される。なお、圧着工程は各シートを積層した後に１回だけ行うようにしてもよい。
【0032】
（各実施例の作用、効果）
前記実施例１～３の積層コイル１０Ａ，１０Ｂ，１０Ｃにおいては、コイル１５の内側（巻芯部）には第１磁性体層１３が存在するため、磁界がコイル軸Ｐ上に指向することとなり、かつ、第２磁性体層１４によって磁束の漏れが防止され、磁束は第２磁性体層１４とは反対側により多く集中することになる。
【0033】
図８に積層コイル１０Ａにおける磁界の発生状態を模式的に示し、図９に積層コイル１０Ｂにおける磁界の発生状態を模式的に示す。図８及び図９から明らかなように、第２磁性体層１４を設けた下方に指向する磁束の漏れは少なく、例えば、積層コイル１０Ａ，１０Ｂをチップコイルアンテナとして使用する場合、上方に指向する磁束を有効に利用することができる。
【0034】
ちなみに、積層コイル１０Ａのサイズと層数を示す。積層体１１は平面視で縦横が３．２ｍｍ×１．６ｍｍ、高さ０．８５ｍｍである。各シートの厚さは２５μｍで、第１磁性体層１３は平面視で縦横が１．６４ｍｍ×０．４６ｍｍとされている。また、非磁性体シート１２ａは３３層が積層され、第２磁性体シート１４ａは２９層が積層されている。
【0035】
また、コイル１５（１７）をスパイラル状とすることにより、磁界密度を高めて磁束をより多く発生させることができる。特に、第２磁性体層１４にもコイル１７を形成した実施例２では図９に示したように大きな磁界密度を形成することができる。
【0036】
一方、積層コイル１０Ｃのように、容量部２０を設ければＬＣ共振器を構成でき、第２磁性体層１４が介在することで容量部２０に磁界の影響が及ぶことを抑えることができる。
【0037】
ところで、前記積層コイル１０Ａ，１０Ｂ，１０Ｃにおいては、第２磁性体層１４の複素比透磁率の虚数部を第１磁性体層１３の複素比透磁率の虚数部よりも小さくしている。複素比透磁率の虚数部を小さくすると、損失を小さく抑えることができるが、これでは透磁率自体も低下してしまう。そこで、各実施例では、上方への磁界の指向性に影響しない第２磁性体層１４のみ複素比透磁率の虚数部を小さくしている。即ち、磁束の上方への指向性に直接関与しない第２磁性体層１４に低損失の材料を用いることで、磁束の指向性を劣化させることなく、磁束の利用効率を向上させることができる。
【0038】
具体的には、複素比透磁率の虚数部を、第１磁性体層１３では５０、第２磁性体層１４では２０とした。なお、実数部はいずれの層１３，１４にあっても７０である。
【0039】
（その他の実施例）
なお、本発明に係る積層コイルは前記実施例に限定されるものではなく、その要旨の範囲内で種々の構成とすることができる。
【0040】

例えば、前記製造方法において、積層コイル１０Ａに積層コイル１０Ｂの製造方法を適用することもでき、その逆も可能である。特に、実施例１では非磁性体シート１２ａに形成された開口部１２ａ′に磁性体シート１３ａを埋め込んでシートを形成したが、磁性体セラミック粉末及び非磁性体セラミック粉末をそれぞれペースト状にして、印刷によりシートを形成してもよい。

【図面の簡単な説明】

【0041】

【図1】本発明に係る積層コイルを示す断面図であり、（Ａ）は実施例１、（Ｂ）は実施例２、（Ｃ）は実施例３を示す。

【図2】本発明に係る積層コイルを示す外観斜視図である。

【図3】実施例１の製造工程を示す説明用の斜視図である。

【図4】実施例１の製造工程の一部を示す説明用の断面図である。

【図5】実施例２の製造工程を示す説明用の斜視図である。

【図6】実施例２の製造工程の一部を示す説明用の断面図である。

【図7】実施例３の製造工程を示す説明用の斜視図である。

【図8】実施例１における磁界ベクトルを示す模式図である。

【図9】実施例２における磁界ベクトルを示す模式図である。

【図10】従来の積層コイルを示す断面図である。

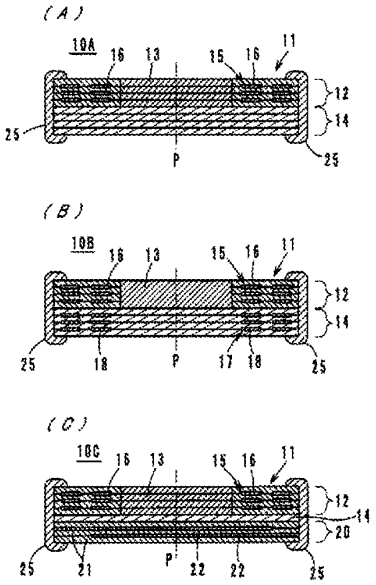
【図11】従来の積層コイルにおける磁界ベクトルを示す模式図である。

【符号の説明】

【0042】

１０（１０Ａ，１０Ｂ，１０Ｃ）…積層コイル
１１…積層体
１２…非磁性体層
１３…第１磁性体層
１４…第２磁性体層
１５…コイル
１６…コイル導体
２０…容量部
２５…外部電極

【図1】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13
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11
12
14
25
P
25
（Ｂ）
10B
16
13
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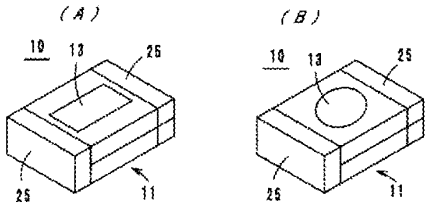
16
11
12
14
25
18
P
17
18
25
（Ｃ）
10C
16
13
15
16
11
12
14
20
25
21
P
22
22
25

【図2】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（Ｂ）
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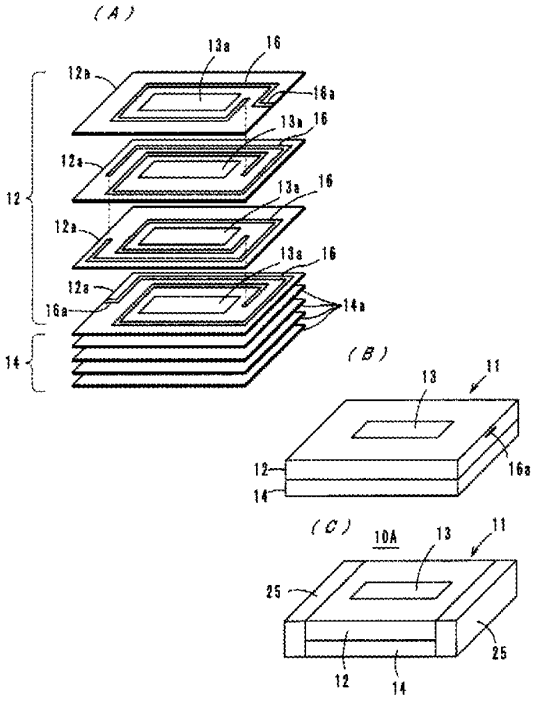
【図3】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14a
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（Ｂ）
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（Ｃ）
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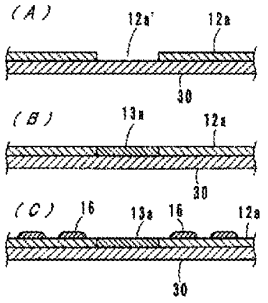
14

【図4】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（Ｂ）
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（Ｃ）
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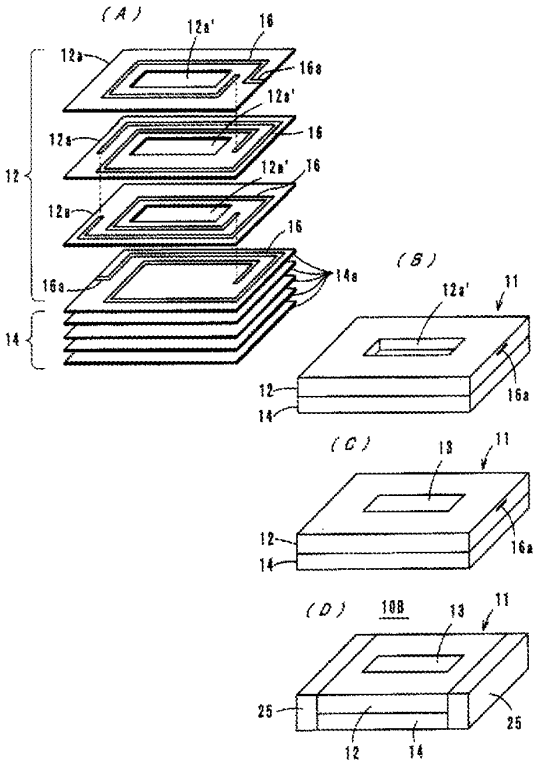
13a
16
12a
30

【図5】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(B)
12a'
11
12
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(C)
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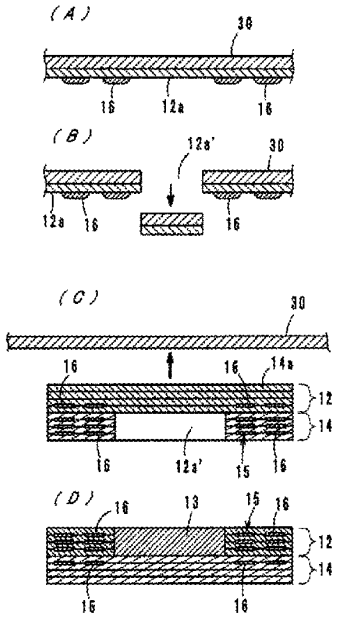
11
12
14
16a
(D)
108
13
11
25
25
12
14

【図6】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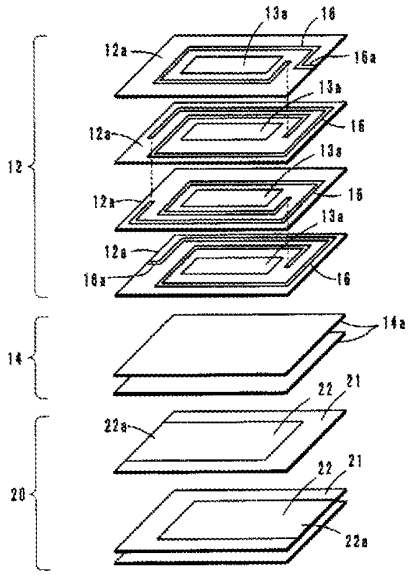
【図7】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22a
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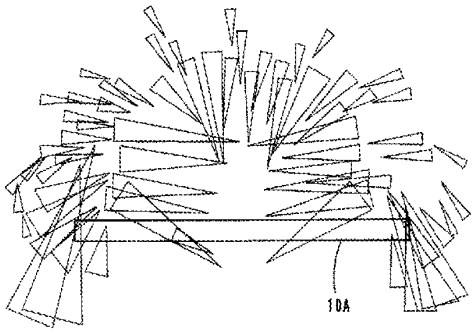
22a

【図8】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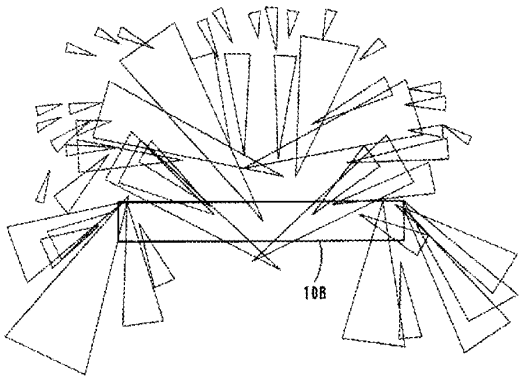

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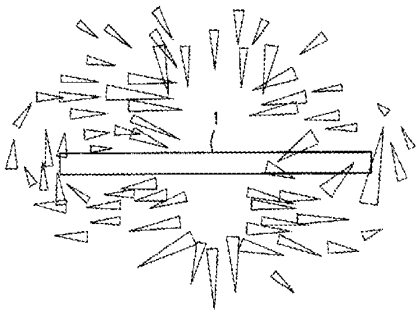
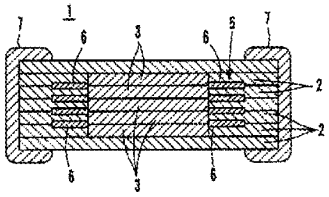


【図10】



Electronic Patent Application Fee Transmittal

Application Number:	16182258
Filing Date:	06-Nov-2018
Title of Invention:	Wireless Power Receiver and Control Method Thereof
First Named Inventor/Applicant Name:	Ki Min LEE
Filer:	Jeff Lloyd/WEA STO DOMINGO
Attorney Docket Number:	SUN.LGI.417D3

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
SUBMISSION- INFORMATION DISCLOSURE STMT	1806	1	240	240
		Total in USD ($)		**240**

Electronic Acknowledgement Receipt	
EFS ID:	37075134
Application Number:	16182258
International Application Number:	
Confirmation Number:	1026
Title of Invention:	Wireless Power Receiver and Control Method Thereof
First Named Inventor/Applicant Name:	Ki Min LEE
Customer Number:	23557
Filer:	Jeff Lloyd/WEA STO DOMINGO
Filer Authorized By:	Jeff Lloyd
Attorney Docket Number:	SUN.LGI.417D3
Receipt Date:	05-SEP-2019
Filing Date:	06-NOV-2018
Time Stamp:	13:58:57
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$240
RAM confirmation Number	E201995E01136081
Deposit Account	190065
Authorized User	WEA STO DOMINGO
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		SUN-LGI-417D3_SIDS2.pdf	216860 1ef9488d88a91f3c3a17d21eaa54a931bdeac10f	yes	3

Multipart Description/PDF files in .zip description

Document Description	Start	End
Transmittal Letter	1	2
Information Disclosure Statement (IDS) Form (SB08)	3	3

Warnings:					
Information:					
2	Foreign Reference	F1.pdf	3792008 1cc7369750b11e5c749cba983a984b6097defc4e	no	12
Warnings:					
Information:					
3	Other Reference-Patent/App/Search documents	R1.pdf	699745 95d544c8638cbcc7437a20b82f175b236fc230e4	no	7
Warnings:					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	30568 38484cc35bee9f6b03392f00f472d8ba03bcd6d3	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	4739181		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

I hereby certify that this correspondence is being electronically filed in the United States Patent and Trademark Office on September 5, 2019.

Jeff Lloyd, Patent Attorney, Reg. No. 35,589

SUPPLEMENTAL INFORMATION
DISCLOSURE STATEMENT
UNDER 37 C.F.R §§ 1.97 AND 1.98
Examining Group 2836
Patent Application
Docket No. SUN.LGI.417D3
Serial No. 16/182,258

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Examiner	:	Fleming, Fritz M.
Art Unit	:	2836
Applicants	:	Ki Min Lee, Jung Oh Lee
Serial No.	:	16/182,258
Filed	:	November 6, 2018
Conf. No.	:	1026
For	:	WIRELESS POWER RECEIVER AND CONTROL METHOD THEREOF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT
UNDER 37 C.F.R. §§ 1.97 AND 1.98

Sir:

In accordance with 37 C.F.R. § 1.56, the references listed on the attached form PTO/SB/08 are being brought to the attention of the Examiner for consideration in connection with the examination of the patent application identified above. Copies of the cited references are attached. However, Applicants have not submitted copies of the published U.S. Patent Applications cited on attached Form PTO/SB/08 pursuant to 37 CFR 1.98(a)(2)(ii).

The undersigned hereby certifies that each item of information contained in this Supplemental Information Disclosure Statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. Applicants are attaching a copy of the European Search Report.

J:\SUN\LGI\417D3\IDS-Refs\SIDS2.DOC/whs

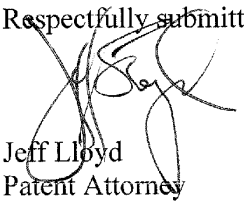
This Information Disclosure Statement is being submitted subsequent to the mailing of an Ex Parte Quayle Action but before the mailing of a Notice of Allowance. The fee of $240.00 was paid at the time this statement was filed.

It is respectfully requested that the Examiner indicate consideration of the cited references by returning a copy of the attached form PTO/SB/08 with initials or other appropriate marks.

Applicants respectfully assert that the substantive provisions of 37 C.F.R. §§ 1.56, 1.97, and 1.98 are met by the foregoing statements.

The Commissioner is hereby authorized to charge any fees under 37 C.F.R. §§ 1.16 or 1.17 as required by this paper to Deposit Account 19-0065.

Respectfully submitted,



Jeff Lloyd
Patent Attorney
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A Professional Association
P.O. Box 142950
Gainesville, FL 32614-2950

JL/whs

Attachments: Form PTO/SB/08; copies of references cited.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/182,258	11/06/2018	Ki Min LEE	SUN.LGI.417D3	1026

23557 7590 07/11/2019

SALIWANCHIK, LLOYD & EISENSCHENK
A PROFESSIONAL ASSOCIATION
PO Box 142950
GAINESVILLE, FL 32614

EXAMINER	
FLEMING, FRITZ M	

ART UNIT	PAPER NUMBER
2836	

NOTIFICATION DATE	DELIVERY MODE
07/11/2019	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

euspto@slepatents.com

Office Action Summary	Application No. 16/182,258	Applicant(s) LEE et al.	
	Examiner FRITZ M FLEMING	Art Unit 2836	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 2 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 2/25/19.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☑ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1-2 and 21-38 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☑ Claim(s) 1-2 and 21-38 is/are allowed.

7) ☐ Claim(s) _____ is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☑ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 11/6/18 is/are: a)☐ accepted or b)☑ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☑ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☑ All b)☐ Some** c)☐ None of the:

1.☑ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☑ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date 4/3/19;11/6/18.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

DETAILED ACTION

Notice of Pre-AIA or AIA Status

1. The present application is being examined under the pre-AIA first to invent provisions.

Allowable Subject Matter

2. Claims 1,2,21-38 are allowed.

3. The following is an examiner's statement of reasons for allowance: The art of record does not teach the specific structure of the independent claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Specification

4. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: the specification lacks the use of terms such as vertical, perpendicular, overlap, distance, gap, and region.

Drawings

5. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the terms noted above as not having proper antecedent basis in the specification must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing

sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Conclusion

6. This application is in condition for allowance except for the following formal matters:

While the claims set forth allowable subject matter, the specification fails to provide adequate antecedent basis for the claims. The claims appear to describe what is shown in the various Figures; however, the specification lacks the use of terms such as vertical, perpendicular, overlap, distance, gap, and region. Since the specification does not use the claim terms, the drawings thus also fail to adequately show the claimed subject matter.

Thus the specification and drawings need to be carefully reviewed and edited to ensure a proper correspondence between what is disclosed and what is claimed. The specification needs to provide proper and clear antecedent basis for what is claimed and the drawings need to clearly

show what is claimed. Prosecution on the merits is closed in accordance with the practice under *Ex parte Quayle*, 25 USPQ 74, 453 O.G. 213, (Comm'r Pat. 1935).

A shortened statutory period for reply to this action is set to expire **TWO MONTHS** from the mailing date of this letter.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to FRITZ M FLEMING whose telephone number is (571)272-4145. The examiner can normally be reached on M-F 0800-2200.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford N Barnie can be reached on 571-272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/FRITZ M FLEMING/
Primary Examiner, Art Unit 2836

Notice of References Cited	Application/Control No. 16/182,258	Applicant(s)/Patent Under Reexamination LEE et al.	
	Examiner FRITZ M FLEMING	Art Unit 2836	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-20150077053-A1	03-2015	Stamenic; Milenko	H02J7/0042	320/109
*	B	US-20130175876-A1	07-2013	Kiyota; Atsushi	H01F38/14	307/104
	C					
	D					
	E					
	F					
	G					
	H					
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/182,258	LEE et al.
	Examiner	**Art Unit**
	FRITZ M FLEMING	2836

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	07/08/2019								
	1	=								
	2	=								
	3	-								
	4	-								
	5	-								
	6	-								
	7	-								
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	9	-								
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	36	=								
	37	=								
	38	=								

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/182,258	LEE et al.
	Examiner	Art Unit
	FRITZ M FLEMING	2836

CPC - Searched*		
Symbol	Date	Examiner
H02j50/10,12,70	07/08/2019	FMF

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
EAST.	07/08/2019	FMF

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
	See interference search printout.	07/08/2019	FMF

PTO/SB/08A (08-03)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 6

Complete if Known	
Application Number	
Filing Date	November 6, 2018
First Named Inventor	Ki Min Lee
Art Unit	
Examiner Name	
Attorney Docket Number	SUN.LGI.417D3

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. [1]	Document Number Number - Kind Code [2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	U1	2004/0130915-A1	07-08-2004	David W. Baarman	ALL
	U2	2007/0182367-A1	08-09-2007	Partovi	ALL
	U3	2008/0197960-A1	08-21-2008	Hasegawa et al.	ALL
	U4	2008/0211455 -A1	09-04-2008	Park et al.	ALL
	U5	2009/0096413-A1	04-16-2009	Partovi et al.	ALL
	U6	2009/0237194-A1	09-24-2009	Waffenschmidt et al.	ALL
	U7	2009/0284082-A1	11-19-2009	Mohammadian	ALL
	U8	2009/0309550-A1	12-17-2009	Chih-Min Liu	ALL
	U9	2010/0066304-A1	03-18-2010	Masanori Oshimi	ALL
	U10	2010/0146308-A1	06-10-2010	Gioscia et al.	ALL
	U11	2010/0191306-A1	07-29-2010	Stevenson et al.	ALL
	U12	2011/0018358-A1	01-27-2011	Osamu Kozakai	ALL
	U13	2011/0025265-A1	02-03-2011	Mochida et al.	ALL
	U14	2011/0115303-A1	05-19-2011	Baarman et al.	ALL
	U15	2011/0127953-A1	06-02-2011	Walley et al.	ALL
	U16	2011/0217927-A1	09-08-2011	Ben-Shalom et al.	ALL
	U17	2011/0227420-A1	09-22-2011	Takashi Urano	ALL
	U18	2011/0316475-A1	12-29-2011	Jung et al.	ALL
	U19	2012/0205989-A1	08-16-2012	Baarman	ALL
	U20	2012/0282857-A1	11-01-2012	Zhang	ALL

Examiner Signature	/FRITZ M FLEMING/	Date Considered	07/07/2019

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kind Codes of USPTO Patent Documents at www.uspto.gov or MPEP901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard T.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /F.M.F/

PTO/SB/08B (08-03)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Substitute for form 1449B/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 2 of 6

Complete if Known	
Application Number	
Filing Date	November 6, 2018
First Named Inventor	Ki Min Lee
Group Art Unit	
Examiner Name	
Attorney Docket Number	SUN.LGI.417D3

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. [1]	Document Number Number - Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	U21	2013/0038278-A1	02-14-2013	Park et al.	ALL
	U22	2013/0113422-A1	05-09-2013	Lee et al.	ALL
	U23	5,430,618-A	07-04-1995	George Y. Huang	ALL
	U24	9,240,824-B2	01-19-2016	Hillan et al.	ALL
	U25	7,719,399-B2	05-18-2010	Iwasaki	ALL
	U26	8,922,160-B2	12-30-2014	Inoue	ALL
	U27	2008/0198560-A1	08-21-2008	FUJIWARA et al.	ALL
	U28	9,461,364-B2	10-04-2016	Lee et al.	ALL

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. [1]	Foreign Patent Document Country Code [3] - Number [4] - Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
	F1	CN-10-1964678-A (With English Abstract) (Equivalent to 2011/0018358)	02-02-2011	Sony Corp.	ALL	
	F2	CN-10-1971453-A (With English Abstract) (Equivalent to US 2009/0096413)	02-09-2011	Mojo Mobility Inc.	ALL	
	F3	CN-10-2195366-A (With English Abstract) (Equivalent to US 2011/0227420)	09-21-2011	TDK Corp.	ALL	
	F4	CN-1768462-A (With English Abstract) (Equivalent to US 2004/0130915)	05-03-2006	Access Business Group Int., LLC.	ALL	
	F5	CN-2012-15827-Y (With English Abstract)	04-01-2009	Inventec Shanghai Electronics Co., Ltd.	ALL	
	F6	CN-20-1663492-U (With English Abstract)	12-01-2010	Fudatong Technology Corp.	ALL	

Examiner Signature	/FRITZ M FLEMING/	Date Considered	07/07/2019

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[1] Applicant's unique citation designation number (optional). [2] Applicant is to place a check mark here if English language Translation is attached.

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PTO/SB/08B (08-03)
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U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Substitute for form 1449B/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 3 of 6

Complete if Known	
Application Number	
Filing Date	November 6, 2018
First Named Inventor	Ki Min Lee
Group Art Unit	
Examiner Name	
Attorney Docket Number	SUN.LGI.417D3

FOREIGN PATENT DOCUMENTS

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	F7	CN-20-1749754-U (With English Abstract)	02-16-2011	Beijing MXH Device Ltd.	ALL	
	F8	EP-2367262-A2 (Equivalent to US 2011/0316475)	09-21-2011	Hanrim Postech Co., Ltd.	ALL	
	F9	JP-2006-302567-A (With English Abstract)	11-02-2006	Nec Tokin Corp., et al.	ALL	
	F10	JP-2010-073976-A (With English Abstract)	04-02-2010	Yazaki Corp.	ALL	
	F11	JP-2011-523336-A (With English Abstract) (Equivalent to US 2009/0284082)	08-04-2011	N/A	ALL	
	F12	KR-10-1298660-B1 (With English Abstract)	08-14-2013	Seoul Electronics & Telecom	ALL	
	F13	KR-10-2005-0105200-A (With English Abstract) (Equivalent of US 2012/0205989)	11-03-2005	Access Business Group International LLC	ALL	
	F14	KR-10-2008-0074640-A (with English Translation)	08-13-2008	Anyquitous Co., Ltd.	ALL	
	F15	KR-10-2008-0095643-A (With English Abstract)	10-29-2008	LS Cable Ltd.	ALL	
	F16	KR-10-2010-0112400-A (With English Abstract)	10-19-2010	LG Innotek Co., Ltd.	ALL	
	F17	KR-10-2011-0033836-A (with English Translation)	03-31-2011	Min Sun Cho	ALL	
	F18	KR-10-2011-0056334-A (With English Abstract) (Equivalent to US 2011/0217927)	05-26-2011	Powermat Ltd.	ALL	

Examiner Signature	/FRITZ M FLEMING/	Date Considered	07/07/2019

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 4 of 6

Complete if Known	
Application Number	
Filing Date	November 6, 2018
First Named Inventor	Ki Min Lee
Group Art Unit	
Examiner Name	
Attorney Docket Number	SUN.LGI.417D3

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	F19	KR-10-2011-0120122-A (With English Abstract)	11-03-2011	Jong Ho Kim	ALL	
	F20	KR-10-2013-0015244-A (With English Abstract)	02-13-2013	LG Electronics Inc.	ALL	
	F21	KR-10-2013-0016588-A (With English Abstract) (Equivalent to US 2013/0038278)	02-18-2013	Samsung Electronics Co., Ltd.	ALL	
	F22	KR-10-2013-0049608-A (With English Abstract) (Equivalent to US 2013/0113422)	05-14-2013	LG Innotek Co., Ltd.	ALL	
	F23	KR-10-2013-0049781-A (With English Abstract)	05-14-2013	LG Innotek Co., Ltd.	ALL	
	F24	KR-10-2013-0072181-A (With English Abstract)	07-01-2013	Amosense Co., Ltd.	ALL	
	F25	TW-2009-52303-A (With English Abstract) (Equivalent to US 2009/0309550)	12-16-2009	KYE Systems Corp.	ALL	
	F26	TW-201132014-A (with English Abstract) (Equivalent to US 9,240,824)	09-16-2011	Qualcomm Incorporated	ALL	
	F27	WO-2007/015599-A1 (Equivalent to US 2008/0211455)	02-08-2007	LS Cable Ltd.	ALL	
	F28	WO-2010/047850-A1 (Equivalent to US 2009/0284082)	04-29-2010	Qualcomm Inc.	ALL	
	F29	JP-06-224043-A (with Machine Translation)	08-12-1994	-	ALL	
	F30	EP-0790667-A1 (with English Abstract)	08-20-1997	SCHLUMBERGER IND SA	ALL	
	F31	KR-10-2010-0067748-A (with English Abstract)	06-22-2010	HANRIM POSTECH CO., LTD	ALL	

Examiner Signature	/FRITZ M FLEMING/	Date Considered	07/07/2019

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 5 of 6

Complete if Known	
Application Number	
Filing Date	November 6, 2018
First Named Inventor	Ki Min Lee
Group Art Unit	
Examiner Name	
Attorney Docket Number	SUN.LGI.417D3

FOREIGN PATENT DOCUMENTS

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	F32	JP-2009-247124-A (with English Abstract)	10-22-2009	PANASONIC CORP	ALL	
	F33	CN-101983466-A (with English Abstract)	03-02-2011	PANASONIC CORP	ALL	
	F34	CN-101517666-A (with English Abstract)	08-26-2009	PHILIPS INTELLECTUAL PROPERTY; KONINKLIJKE PHILIPS ELECTRONICS N.V	ALL	
	F35	CN-101286411-A (with English Abstract)	10-15-2008	SEIKO EPSON CORP	ALL	

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. [1]	Include name of the author (in CAPITAL LETTERS), title of the article, (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T [2]
	R1	Office Action dated May 15, 2017 in Korean Application No. 10-2014-0081260.	
	R2	Office Action dated November 28, 2017 in Korean Application No. 10-2014-0081260.	
	R3	Office Action dated January 5, 2018 in Chinese Application No. 201610451640.3.	
	R4	Office Action dated January 11, 2018 in U.S. Application No. 15/195,390.	
	R5	Communication dated February 6, 2018 in European Application No. 12189931.4.	

Examiner Signature	/FRITZ M FLEMING/	Date Considered	07/07/2019

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 6 of 6

Complete if Known	
Application Number	
Filing Date	November 6, 2018
First Named Inventor	Ki Min Lee
Group Art Unit	
Examiner Name	
Attorney Docket Number	SUN.LGI.417D3

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. [1]	Include name of the author (in CAPITAL LETTERS), title of the article, (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	R6	Notice of Allowance dated October 23, 2013 in Korean Application No. 10-2011-0114721, filed November 4, 2011.	
	R7	Office Action dated December 26, 2012 in Korean Application No. 10-2011-0114721, filed November 4, 2011.	
	R8	Office Action dated January 6, 2014 in Korean Application No. 10-2013-0100314.	
	R9	Office Action dated July 22, 2013 in Korean Application No. 10-2011-0114721, filed November 4, 2011.	
	R10	Office Action dated June 26, 2014 in Chinese Application No. 201210432152.X.	
	R11	Search Report dated September 3, 2013 in Korean Application No. 10-2013-0100314, filed August 23, 2013.	
	R12	European Search Report dated February 17, 2015 in European Application No. 14167637.9.	
	R13	European Search Report dated February 18, 2015 in European Application No. 12189931.4.	
	R14	Office Action dated April 19, 2017 in Taiwanese Application No. 105133529.	
	R15	Office Action dated August 6, 2014 in Taiwanese Application No. 101139085.	
	R16	Office Action dated July 17, 2014 in Korean Application No. 10-2013-0018321.	

Examiner Signature	/FRITZ M FLEMING/	Date Considered	07/07/2019

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 1 of 2

Complete if Known	
Application Number	16/182,258
Filing Date	November 6, 2018
First Named Inventor	Ki Min Lee
Art Unit	2683
Examiner Name	
Attorney Docket Number	SUN.LGI.417D3

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. [1]	Document Number Number - Kind Code [2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	U1	2009/0010316-A1	01-08-2009	ROFOUGARAN	ALL
	U2	7,948,208-B2	05-24-2011	PARTOVI *et al.*	ALL
	U3	7,973,635-B2	07-05-2011	BAARMAN *et al.*	ALL
	U4	8,456,856-B2	06-04-2013	LIN *et al.*	ALL

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	F1	EP-2 330 683-A1	06-08-2011	SONY CORPORATION	ALL	
	F2	TW-2009-38017-A (With English Abstract) (Equivalent to US 7,973,635-B2)	09-01-2009	ACCESS BUSINESS GROUP INTERNATIONAL LLC	ALL	
	F3	WO-2010/114687-A1 (Equivalent to US 8,456,856-B2)	10-07-2010	MEGICA CORPORATION *et al.*	ALL	

Examiner Signature	/FRITZ M FLEMING/	Date Considered	07/07/2019

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 2 of 2

Complete if Known	
Application Number	16/182,258
Filing Date	November 6, 2018
First Named Inventor	Ki Min Lee
Group Art Unit	2683
Examiner Name	
Attorney Docket Number	SUN.LGI.417D3

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	R1	Office Action dated January 18, 2019 in Taiwanese Application No. 106135104, along with its English translation.	

Examiner Signature	/FRITZ M FLEMING/	Date Considered	07/07/2019

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	5668	h02j50/10,12.cpc.	USPAT	OR	ON	2019/07/08 07:41
L2	53414	h02j50/10,12.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/07/08 07:42
L3	7113	h02j50/10,12.cpc. and h02j50/70.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/07/08 07:42
L4	105	3 and (layer same (overlap or overlapping or cover or covering) same (gap or thick or thickness))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/07/08 07:43
L5	4	(shield or shielding) same wireless same power same receiver same coil same layer same (overlap or overlapping) same (gap or distance or thickness)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/07/08 07:56
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S2	0	"2011025265"	US-PGPUB; USPAT	OR	OFF	2015/09/23 19:36
S3	2	"20110025265"	US-PGPUB; USPAT	OR	OFF	2015/09/23 19:36
S4	13	("20090309550" | "20090096413" | "20100146308" | "20100191306" | "20110018358" | "20110025265" | "20120205989" | "20110227420" | "20080211455" | "20040130915" | "20110115303" | "5430618" | "20110316475").PN.	US-PGPUB; USPAT	OR	OFF	2015/09/23 19:57
S5	1	("20130113422").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/09/23 20:10
S6	6657	h04b5/0037.cpc.	US-PGPUB; USPAT; USOCR;	OR	OFF	2015/09/23 20:12

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
S7	32	S6 and (rectifier same shield$)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/23 23:25
S8	8244	h02j17/00.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/23 23:26
S9	394	S8 and nfc	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/23 23:26
S10	13278	S6 or S8	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/23 23:37
S11	77	S10 and ((shield or shielding) same (coil or antenna) same rectifier)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/23 23:38
S12	19	S10 and (("printed circuit board") same (coil or antenna) same rectifier)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/23 23:41
S13	25	S10 and (("printed circuit board") same (coil or antenna) same (shield or shielding))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/23 23:45
S14	504	S10 and ((coil or antenna) same (shield or shielding))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/23 23:46
S15	293	(US-20110096823-$).did. or (US-	US-PGPUB;	OR	OFF	2015/09/25

		4897662-$ or US-6098175-$ or US-4984291-$ or US-4989261-$ or US-5025486-$ or US-6038452-$ or US-4967108-$ or US-5524044-$ or US-5619531-$ or US-5686847-$ or US-5726636-$ or US-5727020-$ or US-5767791-$ or US-5917854-$ or US-5942946-$ or US-5964701-$ or US-6223295-$ or US-4563626-$ or US-4567557-$ or US-4955038-$ or US-5189839-$ or US-5216838-$ or US-5239779-$ or US-5278892-$ or US-5389920-$ or US-5396195-$).did. or (US-5504864-$ or US-5546051-$ or US-5565893-$ or US-5657317-$ or US-5684470-$ or US-5684828-$ or US-5689142-$ or US-5721783-$ or US-5728963-$ or US-5764693-$ or US-5822683-$ or US-5845204-$ or US-5861822-$ or US-5870389-$ or US-5887255-$ or US-5889273-$ or US-5895985-$ or US-5898904-$ or US-5926747-$ or US-5943618-$ or US-5943325-$ or US-5945936-$ or US-5949776-$ or US-5978674-$ or US-5995492-$ or US-6006116-$ or US-6009148-$).did. or (US-6023460-$ or US-6023621-$ or US-6028857-$ or US-6034999-$ or US-6049702-$ or US-6057733-$ or US-6072990-$ or US-6088600-$ or US-6097704-$ or US-6104761-$ or US-6150882-$ or US-6188718-$ or US-6188875-$ or US-6233464-$ or US-4386422-$ or US-4473905-$ or US-4502150-$ or US-4509201-$ or US-4550427-$ or US-4617002-$ or US-4630035-$ or US-4755792-$ or US-4757224-$ or US-4848823-$ or US-4852147-$ or US-4898562-$ or US-4902262-$).did. or (US-4973958-$ or US-4983892-$ or US-5014017-$ or US-5017837-$ or US-5212478-$ or US-5218356-$ or US-5289501-$ or US-5402413-$ or US-5420536-$ or US-5424859-$ or US-5426641-$ or US-5434396-$ or US-5465418-$ or US-5488737-$ or US-5490172-$ or US-5491457-$ or US-5503483-$ or US-5504780-$ or US-5511090-$ or US-5513379-$ or US-5525993-$ or US-5532470-$ or US-5539393-$ or US-5541604-$ or US-5548250-$ or US-5553101-$ or US-5563483-$).did. or (US-5579201-$ or US-5581617-$ or US-5587573-$ or US-5589859-$ or US-5592257-$ or US-5594385-$ or US-5596261-$ or US-5604462-$ or US-5608171-$ or US-5616888-$ or US-5640674-$ or US-5644172-$ or US-5678172-$ or US-5680633-$ or US-5687734-$ or US-5691691-$ or US-5692647-$ or US-5701583-$ or US-5707262-$ or US-5711480-$ or US-	USPAT			23:19	

		5721500-$ or US-5722051-$ or US-5734984-$ or US-5737707-$ or US-5745852-$ or US-5748104-$).did. or (US-5748813-$ or US-5750939-$ or US-5751693-$ or US-5768695-$ or US-5770970-$ or US-5774018-$ or US-5774043-$ or US-5781543-$ or US-5781069-$ or US-5790936-$ or US-5790536-$ or US-5793174-$ or US-5802470-$ or US-5808557-$ or US-5812012-$ or US-5815086-$ or US-5815811-$ or US-5822373-$ or US-5828367-$ or US-5832044-$ or US-5832390-$ or US-5832364-$ or US-5831593-$ or US-5842037-$ or US-5844789-$ or US-5850600-$ or US-5854793-$).did. or (US-5854592-$ or US-5859838-$ or US-5878335-$ or US-5878084-$ or US-5880633-$ or US-5883549-$ or US-5887031-$ or US-5886497-$ or US-5892758-$ or US-5896261-$ or US-5901345-$ or US-5905473-$ or US-5912919-$ or US-5912963-$ or US-5920270-$ or US-5920816-$ or US-5922650-$ or US-5926760-$ or US-5933263-$ or US-5933774-$ or US-5942981-$ or US-5946346-$ or US-5949766-$ or US-5949484-$ or US-5949309-$ or US-5953688-$ or US-5956656-$).did. or (US-5974034-$ or US-5974376-$ or US-5987338-$ or US-5987037-$ or US-5990646-$ or US-5990826-$ or US-5994985-$ or US-6002715-$ or US-6002918-$ or US-6006069-$ or US-6005840-$ or US-6005856-$ or US-6008749-$ or US-6014705-$ or US-6018232-$ or US-6023612-$ or US-6028454-$ or US-6028631-$ or US-6041241-$ or US-6046698-$ or US-6047165-$ or US-6047200-$ or US-6052509-$ or US-6052033-$ or US-6055418-$ or US-6057658-$ or US-6061389-$).did. or (US-6067297-$ or US-6067053-$ or US-6069881-$ or US-6069526-$ or US-6072784-$ or US-6073033-$ or US-6075510-$ or US-6078824-$ or US-6078222-$ or US-6085114-$ or US-6085074-$ or US-6084904-$ or US-6091296-$ or US-6092117-$ or US-6097243-$ or US-6098048-$ or US-6101174-$ or US-6104937-$ or US-6104914-$ or US-6108523-$ or US-6108367-$ or US-6111248-$ or US-6112165-$ or US-6112056-$ or US-6119009-$ or US-6118806-$ or US-6118567-$).did. or (US-6122312-$ or US-6124764-$ or US-6134437-$ or US-6141538-$ or US-6141763-$ or US-6144840-$ or US-6151308-$ or US-6151483-$ or US-6154488-$ or US-6154637-$ or US-6154663-$ or US-6163581-$ or US-6163679-$ or US-6167238-$ or US-				

		6169339-$ or US-6169884-$ or US-6173352-$ or US-6175302-$ or US-6181089-$ or US-6181916-$ or US-6184950-$ or US-6188353-$ or US-6192230-$ or US-6201372-$ or US-6212398-$ or US-6215358-$ or US-6215827-$).did. or (US-6216019-$ or US-6236866-$ or US-6243870-$ or US-6249685-$ or US-7865209-$ or US-7945282-$ or US-8582683-$ or US-3614760-$ or US-3659280-$ or US-3641540-$ or US-3641425-$ or US-3911415-$ or US-3842403-$ or US-4024502-$ or US-4025912-$ or US-4058678-$ or US-4132378-$ or US-4151407-$ or US-4078747-$ or US-4088999-$ or US-4249162-$ or US-4259743-$ or US-4272687-$).did.				
S16	255888	(communication or nfc) same (wireless or contactless or inductive) same power	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/25 23:26
S17	4879	(nfc) same (wireless or contactless or inductive) same power	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/25 23:26
S18	33	(nfc) same (wireless or contactless or inductive) same power same (shield or shielding)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/25 23:27
S19	2	("20110050164" | "20120146576").PN. OR ("8922162").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/09/25 23:29
S20	1420	(nfc) same (wireless or contactless or inductive) same power same (coil or antenna or winding)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/25 23:33
S21	4118	(nfc) same power same data	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/25 23:55
S22	1052	(nfc) same power same data same (coil or winding or antenna)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2015/09/25 23:56

			IBM_TDB			
S23	6667	h04b5/0037.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/09/26 00:12
S24	8256	h02j17/00.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/26 00:12
S25	1625	S23 and S24	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/26 00:12
S26	3663	(307/104).CCLS.	US-PGPUB; USPAT	OR	OFF	2015/09/26 00:27
S27	2493	(320/108).CCLS.	US-PGPUB; USPAT	OR	OFF	2015/09/26 00:27
S28	5795	S26 or S27	US-PGPUB; USPAT	OR	OFF	2015/09/26 00:27
S29	548	S28 and nfc	US-PGPUB; USPAT	OR	OFF	2015/09/26 00:27
S30	14905	h02j7/025.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/09/26 00:56
S31	735	S30 and nfc	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/09/26 00:56
S32	50969	communication same (wireless or contactless or inductive) same power same (coil or antenna or winding)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/26 01:08
S33	3352	communication same (wireless or contactless or inductive) same power same (coil or antenna or winding) same transfer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/26 01:09
S34	141	communication same (wireless or contactless or inductive) same power	US-PGPUB; USPAT;	OR	ON	2015/09/26 01:09

		same (coil or antenna or winding) same transfer same (pplane ir planar)	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S35	78	communication same (wireless or contactless or inductive) same power same (coil or antenna or winding) same transfer same (plane or planar)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/26 01:09
S36	30	nfc same (antenna or winding or coil) same (shield or shielding) same (pcb or "printed circuit board")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/09/26 10:36
S37	3663	(307/104).CCLS.	US-PGPUB; USPAT	OR	OFF	2015/09/26 11:41
S38	2493	(320/108).CCLS.	US-PGPUB; USPAT	OR	OFF	2015/09/26 11:41
S39	5795	S37 or S38	US-PGPUB; USPAT	OR	OFF	2015/09/26 11:42
S40	216	S39 and ((shield or shielding) same (pcb or "printed circuit board"))	US-PGPUB; USPAT	OR	ON	2015/09/26 11:42
S41	1333	S39 and embedded	US-PGPUB; USPAT	OR	OFF	2015/09/26 12:08
S42	176	S39 and zener	US-PGPUB; USPAT	OR	OFF	2015/09/26 12:29
S43	7	S39 and (groove same (pcb or "printed circuit board"))	US-PGPUB; USPAT	OR	ON	2015/09/26 12:53
S44	21	S39 and young and fritz	US-PGPUB; USPAT	OR	ON	2015/09/26 12:53
S45	341	nfc same (antenna or winding or coil) same (pcb or "printed circuit board")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/09/26 13:00
S46	532	S39 and ((antenna or coil or winding) same (pcb or "printed circuit board"))	US-PGPUB; USPAT	OR	ON	2015/09/26 13:06
S47	417	"printed circuit board coil"	US-PGPUB; USPAT	OR	ON	2015/09/26 13:46
S48	2	nfc same (shield or shielding) same rectifier	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/26 14:02
S49	3476	through same (shield or shielding) same rectifier	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2015/09/26 14:04

			DERWENT; IBM_TDB			
S50	64	phone same (shield or shielding) same rectifier	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/26 14:04
S51	69	charger same (shield or shielding) same rectifier	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/26 14:05
S52	103	charger same (shield or shielding) same ((non adj contact) or noncontact or contactless)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/26 14:09
S53	31	rectifier same (shield or shielding) same ((non adj contact) or noncontact or contactless)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/26 14:17
S54	0	rectifier same (shield or shielding) same "pronted circuit board"	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/26 14:20
S55	70	rectifier same (shield or shielding) same "printed circuit board"	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/26 14:20
S56	126	S39 and (rectifier same (shield or shielding))	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/26 14:25
S57	6677	h04b5/0037.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/09/26 14:29
S58	8269	h02j17/00.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/26 14:29

S59	14926	h02j7/025.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/09/26 14:29
S60	23176	S57 or S58 or S59	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/26 14:29
S61	246	S60 and ((shield or shielding) same (pcb or "printed circuit board"))	US-PGPUB; USPAT	OR	ON	2015/09/26 14:30
S62	256	S60 and ((shield or shielding) same (pcb or "printed circuit board"))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/26 14:30
S63	7860	h04b5/0037.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/02/22 13:33
S64	10103	h02j17/00.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/02/22 13:44
S65	4003	(307/104).CCLS.	US-PGPUB; USPAT	OR	OFF	2016/02/22 13:58
S66	2678	(320/108).CCLS.	US-PGPUB; USPAT	OR	OFF	2016/02/22 13:58
S67	6291	S65 or S66	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/02/22 13:58
S68	4203	(307/104).CCLS.	US-PGPUB; USPAT	OR	OFF	2016/05/17 12:51
S69	2811	(320/108).CCLS.	US-PGPUB; USPAT	OR	OFF	2016/05/17 12:51
S70	6604	S68 or S69	US-PGPUB; USPAT	OR	OFF	2016/05/17 12:51
S71	2984	h02j17/00.cpc.	US-PGPUB; USPAT	OR	OFF	2016/05/17 13:29
S72	7577	h02j17/00.cpc.	FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/05/17 13:32

S73	5655	h04b5/0037.cpc.	FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/05/17 14:28
S74	8167	h04b5/0037.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/05/17 14:28
S75	288	h02j50/00,10.cpc. or h02j50/00,10.ipc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/17 14:42
S77	1	("9461364").PN.	USPAT; USOCR	OR	OFF	2017/12/27 08:19
S78	1	("9461364").PN.	USPAT; USOCR	OR	OFF	2017/12/27 10:47
S79	0	S78 and layer	USPAT	OR	ON	2017/12/27 10:47
S80	293	(US-20110096823-$ or US-20170078971-$).did. or (US-4897662-$ or US-6098175-$ or US-4984291-$ or US-4989261-$ or US-5025486-$ or US-6038452-$ or US-4967108-$ or US-5524044-$ or US-5619531-$ or US-5686847-$ or US-5726636-$ or US-5727020-$ or US-5767791-$ or US-5917854-$ or US-5942946-$ or US-5964701-$ or US-6223295-$ or US-4563626-$ or US-4567557-$ or US-4955038-$ or US-5189839-$ or US-5216838-$ or US-5239779-$ or US-5278892-$ or US-5389920-$ or US-5396195-$).did. or (US-5504864-$ or US-5546051-$ or US-5565893-$ or US-5657317-$ or US-5684470-$ or US-5684828-$ or US-5689142-$ or US-5721783-$ or US-5728963-$ or US-5764693-$ or US-5822683-$ or US-5845204-$ or US-5861822-$ or US-5870389-$ or US-5887255-$ or US-5889273-$ or US-5895985-$ or US-5898904-$ or US-5926747-$ or US-5943618-$ or US-5943325-$ or US-5945936-$ or US-5949776-$ or US-5978674-$ or US-5995492-$ or US-6006116-$ or US-6009148-$).did. or (US-6023460-$ or US-6023621-$ or US-6028857-$ or US-6034999-$ or US-6049702-$ or US-6057733-$ or US-6072990-$ or US-6088600-$ or US-6097704-$ or US-6104761-$ or US-6150882-$ or US-6188718-$ or US-6188875-$ or US-6233464-$ or US-4386422-$ or US-4473905-$ or US-4502150-$ or US-4509201-$ or US-4550427-$ or US-4617002-$ or US-	US-PGPUB; USPAT	OR	OFF	2017/12/27 21:08

		4630035-$ or US-4755792-$ or US-4757224-$ or US-4848823-$ or US-4852147-$ or US-4898562-$ or US-4902262-$).did. or (US-4973958-$ or US-4983892-$ or US-5014017-$ or US-5017837-$ or US-5212478-$ or US-5218356-$ or US-5289501-$ or US-5402413-$ or US-5420536-$ or US-5424859-$ or US-5426641-$ or US-5434396-$ or US-5465418-$ or US-5488737-$ or US-5490172-$ or US-5491457-$ or US-5503483-$ or US-5504780-$ or US-5511090-$ or US-5513379-$ or US-5525993-$ or US-5532470-$ or US-5539393-$ or US-5541604-$ or US-5548250-$ or US-5553101-$ or US-5563483-$).did. or (US-5579201-$ or US-5581617-$ or US-5587573-$ or US-5589859-$ or US-5592257-$ or US-5594385-$ or US-5596261-$ or US-5604462-$ or US-5608171-$ or US-5616888-$ or US-5640674-$ or US-5644172-$ or US-5678172-$ or US-5680633-$ or US-5687734-$ or US-5691691-$ or US-5692647-$ or US-5701583-$ or US-5707262-$ or US-5711480-$ or US-5715523-$ or US-5721500-$ or US-5722051-$ or US-5734984-$ or US-5737707-$ or US-5745852-$ or US-5748104-$).did. or (US-5748813-$ or US-5750939-$ or US-5751693-$ or US-5768695-$ or US-5770970-$ or US-5774018-$ or US-5774043-$ or US-5781543-$ or US-5781069-$ or US-5790936-$ or US-5790536-$ or US-5793174-$ or US-5802470-$ or US-5808557-$ or US-5812012-$ or US-5815086-$ or US-5815811-$ or US-5822373-$ or US-5828367-$ or US-5832044-$ or US-5832390-$ or US-5832364-$ or US-5831593-$ or US-5842037-$ or US-5844789-$ or US-5850600-$ or US-5854793-$).did. or (US-5854592-$ or US-5859838-$ or US-5878335-$ or US-5878084-$ or US-5880633-$ or US-5883549-$ or US-5887031-$ or US-5886497-$ or US-5892758-$ or US-5896261-$ or US-5901345-$ or US-5905473-$ or US-5912919-$ or US-5912963-$ or US-5920270-$ or US-5920816-$ or US-5922650-$ or US-5926760-$ or US-5933263-$ or US-5933774-$ or US-5942981-$ or US-5946346-$ or US-5949766-$ or US-5949484-$ or US-5949309-$ or US-5953688-$ or US-5956656-$).did. or (US-5974034-$ or US-5974376-$ or US-5987338-$ or US-5987037-$ or US-5990646-$ or US-5990826-$ or US-5994985-$ or US-6002715-$ or US-6002918-$ or US-6006069-$ or US-6005840-$ or US-6005856-$ or US-6008749-$ or US-					

		6014705-$ or US-6018232-$ or US-6023612-$ or US-6028454-$ or US-6028631-$ or US-6041241-$ or US-6046698-$ or US-6047165-$ or US-6047200-$ or US-6052509-$ or US-6052033-$ or US-6055418-$ or US-6057658-$ or US-6061389-$).did. or (US-6067297-$ or US-6067053-$ or US-6069881-$ or US-6069526-$ or US-6072784-$ or US-6073033-$ or US-6075510-$ or US-6078824-$ or US-6078222-$ or US-6085114-$ or US-6085074-$ or US-6084904-$ or US-6091296-$ or US-6092117-$ or US-6097243-$ or US-6098048-$ or US-6101174-$ or US-6104937-$ or US-6104914-$ or US-6108523-$ or US-6108367-$ or US-6111248-$ or US-6112165-$ or US-6112056-$ or US-6119009-$ or US-6118806-$ or US-6118567-$).did. or (US-6122312-$ or US-6124764-$ or US-6134437-$ or US-6141538-$ or US-6141763-$ or US-6144840-$ or US-6151308-$ or US-6151483-$ or US-6154488-$ or US-6154637-$ or US-6154663-$ or US-6163581-$ or US-6163679-$ or US-6167238-$ or US-6169339-$ or US-6169884-$ or US-6173352-$ or US-6175302-$ or US-6181089-$ or US-6181916-$ or US-6184950-$ or US-6188353-$ or US-6192230-$ or US-6201372-$ or US-6212398-$ or US-6215358-$ or US-6215827-$).did. or (US-6216019-$ or US-6236866-$ or US-6243870-$ or US-6249685-$ or US-7865209-$ or US-7945282-$ or US-8582683-$ or US-3614760-$ or US-3659280-$ or US-3641540-$ or US-3641425-$ or US-3911415-$ or US-3842403-$ or US-4024502-$ or US-4025912-$ or US-4058678-$ or US-4132378-$ or US-4151407-$ or US-4078747-$ or US-4088999-$ or US-4249162-$ or US-4259743-$).did.				
S81	293	(US-20110096823-$ or US-20170078971-$).did. or (US-4897662-$ or US-6098175-$ or US-4984291-$ or US-4989261-$ or US-5025486-$ or US-6038452-$ or US-4967108-$ or US-5524044-$ or US-5619531-$ or US-5686847-$ or US-5726636-$ or US-5727020-$ or US-5767791-$ or US-5917854-$ or US-5942946-$ or US-5964701-$ or US-6223295-$ or US-4563626-$ or US-4567557-$ or US-4955038-$ or US-5189839-$ or US-5216838-$ or US-5239779-$ or US-5278892-$ or US-5389920-$ or US-5396195-$).did. or (US-5504864-$ or US-5546051-$ or US-5565893-$ or US-5657317-$ or US-5684470-$ or US-5684828-$ or US-5689142-$ or US-5721783-$ or US-5728963-$ or US-	US-PGPUB; USPAT	OR	OFF	2017/12/27 21:08

		5764693-$ or US-5822683-$ or US-5845204-$ or US-5861822-$ or US-5870389-$ or US-5887255-$ or US-5889273-$ or US-5895985-$ or US-5898904-$ or US-5926747-$ or US-5943618-$ or US-5943325-$ or US-5945936-$ or US-5949776-$ or US-5978674-$ or US-5995492-$ or US-6006116-$ or US-6009148-$).did. or (US-6023460-$ or US-6023621-$ or US-6028857-$ or US-6034999-$ or US-6049702-$ or US-6057733-$ or US-6072990-$ or US-6088600-$ or US-6097704-$ or US-6104761-$ or US-6150882-$ or US-6188718-$ or US-6188875-$ or US-6233464-$ or US-4386422-$ or US-4473905-$ or US-4502150-$ or US-4509201-$ or US-4550427-$ or US-4617002-$ or US-4630035-$ or US-4755792-$ or US-4757224-$ or US-4848823-$ or US-4852147-$ or US-4898562-$ or US-4902262-$).did. or (US-4973958-$ or US-4983892-$ or US-5014017-$ or US-5017837-$ or US-5212478-$ or US-5218356-$ or US-5289501-$ or US-5402413-$ or US-5420536-$ or US-5424859-$ or US-5426641-$ or US-5434396-$ or US-5465418-$ or US-5488737-$ or US-5490172-$ or US-5491457-$ or US-5503483-$ or US-5504780-$ or US-5511090-$ or US-5513379-$ or US-5525993-$ or US-5532470-$ or US-5539393-$ or US-5541604-$ or US-5548250-$ or US-5553101-$ or US-5563483-$).did. or (US-5579201-$ or US-5581617-$ or US-5587573-$ or US-5589859-$ or US-5592257-$ or US-5594385-$ or US-5596261-$ or US-5604462-$ or US-5608171-$ or US-5616888-$ or US-5640674-$ or US-5644172-$ or US-5678172-$ or US-5680633-$ or US-5687734-$ or US-5691691-$ or US-5692647-$ or US-5701583-$ or US-5707262-$ or US-5711480-$ or US-5715523-$ or US-5721500-$ or US-5722051-$ or US-5734984-$ or US-5737707-$ or US-5745852-$ or US-5748104-$).did. or (US-5748813-$ or US-5750939-$ or US-5751693-$ or US-5768695-$ or US-5770970-$ or US-5774018-$ or US-5774043-$ or US-5781543-$ or US-5781069-$ or US-5790936-$ or US-5790536-$ or US-5793174-$ or US-5802470-$ or US-5808557-$ or US-5812012-$ or US-5815086-$ or US-5815811-$ or US-5822373-$ or US-5828367-$ or US-5832044-$ or US-5832390-$ or US-5832364-$ or US-5831593-$ or US-5842037-$ or US-5844789-$ or US-5850600-$ or US-5854793-$).did. or (US-5854592-$ or US-5859838-$ or US-						

		5878335-$ or US-5878084-$ or US-5880633-$ or US-5883549-$ or US-5887031-$ or US-5886497-$ or US-5892758-$ or US-5896261-$ or US-5901345-$ or US-5905473-$ or US-5912919-$ or US-5912963-$ or US-5920270-$ or US-5920816-$ or US-5922650-$ or US-5926760-$ or US-5933263-$ or US-5933774-$ or US-5942981-$ or US-5946346-$ or US-5949766-$ or US-5949484-$ or US-5949309-$ or US-5953688-$ or US-5956656-$).did. or (US-5974034-$ or US-5974376-$ or US-5987338-$ or US-5987037-$ or US-5990646-$ or US-5990826-$ or US-5994985-$ or US-6002715-$ or US-6002918-$ or US-6006069-$ or US-6005840-$ or US-6005856-$ or US-6008749-$ or US-6014705-$ or US-6018232-$ or US-6023612-$ or US-6028454-$ or US-6028631-$ or US-6041241-$ or US-6046698-$ or US-6047165-$ or US-6047200-$ or US-6052509-$ or US-6052033-$ or US-6055418-$ or US-6057658-$ or US-6061389-$).did. or (US-6067297-$ or US-6067053-$ or US-6069881-$ or US-6069526-$ or US-6072784-$ or US-6073033-$ or US-6075510-$ or US-6078824-$ or US-6078222-$ or US-6085114-$ or US-6085074-$ or US-6084904-$ or US-6091296-$ or US-6092117-$ or US-6097243-$ or US-6098048-$ or US-6101174-$ or US-6104937-$ or US-6104914-$ or US-6108523-$ or US-6108367-$ or US-6111248-$ or US-6112165-$ or US-6112056-$ or US-6119009-$ or US-6118806-$ or US-6118567-$).did. or (US-6122312-$ or US-6124764-$ or US-6134437-$ or US-6141538-$ or US-6141763-$ or US-6144840-$ or US-6151308-$ or US-6151483-$ or US-6154488-$ or US-6154637-$ or US-6154663-$ or US-6163581-$ or US-6163679-$ or US-6167238-$ or US-6169339-$ or US-6169884-$ or US-6173352-$ or US-6175302-$ or US-6181089-$ or US-6181916-$ or US-6184950-$ or US-6188353-$ or US-6192230-$ or US-6201372-$ or US-6212398-$ or US-6215358-$ or US-6215827-$).did. or (US-6216019-$ or US-6236866-$ or US-6243870-$ or US-6249685-$ or US-7865209-$ or US-7945282-$ or US-8582683-$ or US-3614760-$ or US-3659280-$ or US-3641540-$ or US-3641425-$ or US-3911415-$ or US-3842403-$ or US-4024502-$ or US-4025912-$ or US-4058678-$ or US-4132378-$ or US-4151407-$ or US-4078747-$ or US-4088999-$ or US-4249162-$ or US-4259743-$).did.				

S82	293	S80 or S81	US-PGPUB; USPAT	OR	OFF	2017/12/27 21:09
S83	5606	h02j50/70.cpc. or h02j50/70.ipc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2017/12/27 22:27
S84	5385	h02j50/70.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2017/12/27 22:27
S85	367	h02j50/70.ipc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2017/12/27 22:27
S86	312	S83 and nfc	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2017/12/27 22:27
S87	173	S83 and nfc and layer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2017/12/27 22:32
S88	178	S83 and nfc and layer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/12/27 22:32
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S90	1006	S89 and layer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/12/28 07:51
S91	38275	h02j50/05,10,12,80.cpc.	US-PGPUB; USPAT; USOCR;	OR	ON	2017/12/28 09:21

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
S92	0	h02j50/05,10,12,80.ipc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/12/28 09:21
S93	1980	S91 and nfc	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/12/28 09:21
S94	339	S91 and nfc and (layer or sheet) and (shield or shielding)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/12/28 09:22
S95	13248	h04b5/0037.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/12/28 09:43
S96	1519	h04b5/0087.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/12/28 09:43
S97	593	S95 and (layer or sheet) and (shield or shielding)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/12/28 09:43
S98	700	S95 and (layer or sheet or board) and (shield or shielding)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/12/28 09:50
S99	1	("20150054455").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2017/12/28 10:12
S100	1	("20170338697").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2017/12/28 21:37
S101	13924	h04b5/0037.cpc.	US-PGPUB;	OR	ON	2018/04/29

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S102	782	S101 and @py="2018"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/04/29 21:43
S103	2309	h02j50/70,10,12,80.cpc. and @py="2018"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/04/29 21:50
S104	2603	S102 or S103	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/04/29 21:52
S105	44	S104 and ((shield or shielding) same (pcb or "printed circuit board"))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/04/29 21:53
S106	162	S104 and (layer or sheet) and (shield or shielding)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/04/29 21:56
S107	120	S106 not S105	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/04/29 21:57
S109	1	("9461364").PN.	USPAT; USOCR	OR	OFF	2018/08/05 23:39
S110	15225	h04b5/0037.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/08/05 23:43
S111	1822	S110 and @py="2018"	US-PGPUB; USPAT; USOCR; FPRS;	OR	ON	2018/08/05 23:43

			EPO; JPO; DERWENT; IBM_TDB			
S112	5238	h02j50/70,10,12,80.cpc. and @py="2018"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/08/05 23:43
S113	5857	S111 or S112	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/08/05 23:43
S114	45647	h02j50/70,10,12,80.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/08/05 23:45

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S76	3	(communication same (wireless or contactless or inductive) same power same (coil or antenna or winding) same transfer same (plane or planar)).clm.	US-PGPUB; USPAT	OR	ON	2016/05/17 14:35
S108	7	(communication same (wireless or contactless or inductive) same power same (coil or antenna or winding) same transfer same (plane or planar)).clm.	US-PGPUB; USPAT	OR	ON	2018/04/29 21:41
S115	7	(communication same (wireless or contactless or inductive) same power same (coil or antenna or winding) same transfer same (plane or planar)).clm.	US-PGPUB; USPAT	OR	ON	2018/08/05 23:41

7/ 8/ 2019 8:47:02 AM
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PLUS Search Results for S/N 16182258, Searched Mon Jul 08 10:14:11 EDT 2019

The Patent Linguistics Utility System (PLUS) is a USPTO automated search system for U.S. Patents from 1971 to the present PLUS is a query-by-example search system which produces a list of patents that are most closely related linguistically to the application searched. This search was prepared by the staff of the Scientific and Technical Information Center, SIRA.

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대 한 민 국 특 허 청
KOREAN INTELLECTUAL PROPERTY OFFICE

별첨 사본은 아래 출원의 원본과 동일함을 증명함.

This is to certify that the following application annexed hereto is a true copy from the records of the Korean Intellectual Property Office.

출 원 번 호 : 10-2011-0114721
Application Number

출 원 년 월 일 : 2011년 11월 04일
Filing Date Nov. 04, 2011

출 원 인 : 엘지이노텍 주식회사
Applicant(s) LG INNOTEK CO., LTD.

2019년 06월 18일

특 허 청
COMMISSIONER

제출 일자 : 2011-11-04

【서지사항】

【서류명】 특허출원서

【참조번호】 P2011C3185KR

【출원구분】 특허출원

【출원인】

【명칭】 엘지이노텍 주식회사

【특허고객번호】 1-1998-000285-5

【대리인】

【성명】 서교준

【대리인번호】 9-2004-000236-3

【포괄위임등록번호】 2009-020964-8

【발명의 국문명칭】 무선전력 수신장치 및 그 제어 방법

【발명의 영문명칭】 APPARATUS FOR RECEIVING WIRELESS POWER AND METHOD FOR CONTROLLING THEREOF

【발명자】

【성명】 이정오

【성명의 영문표기】 LEE, JUNG OH

【주민등록번호】 770427-1XXXXXX

【우편번호】 100-095

【주소】 서울특별시 중구 남대문로5가 541번지 서울스퀘어

【국적】 KR

【발명자】

제출 일자 : 2011-11-04

【성명】 이기민

【성명의 영문표기】 LEE, KI MIN

【주민등록번호】 750112-1XXXXXX

【우편번호】 100-095

【주소】 서울특별시 중구 남대문로5가 541번지 서울스퀘어

【국적】 KR

【심사청구】 청구

【취지】 위와 같이 특허청장에게 제출합니다.

대리인 서교준 (서명 또는 인)

【수수료】

【출원료】	0	면	38,000 원
【가산출원료】	30	면	0 원
【우선권주장료】	0	건	0 원
【심사청구료】	24	항	1,090,000 원
【합계】	1,128,000 원		

【발명의 설명】

【발명의 명칭】

무선전력 수신장치 및 그 제어 방법{APPARATUS FOR RECEIVING WIRELESS POWER AND METHOD FOR CONTROLLING THEREOF}

【기술분야】

【0001】 본 발명은 무선전력 수신장치 및 그 제어 방법에 관한 것이다.

【발명의 배경이 되는 기술】

【0002】 무선으로 전기 에너지를 원하는 기기로 전달하는 무선전력전송 기술(wireless power transmission 또는 wireless energy transfer)은 이미 1800년대에 전자기유도 원리를 이용한 전기 모터나 변압기가 사용되기 시작했고, 그 후로는 라디오파나 레이저와 같은 전자파를 방사해서 전기에너지를 전송하는 방법도 시도되었다. 우리가 흔히 사용하는 전동칫솔이나 일부 무선면도기도 실상은 전자기유도 원리로 충전된다. 현재까지 무선 방식에 의한 에너지 전달 방식은 전자기 유도, 자기 공진 및 단파장 무선 주파수를 이용한 원거리 송신 기술 등이 있다.

【0003】 최근에는 이와 같은 무선 전력 전송 기술 중 전자기 유도 에너지 전달 방식이 많이 사용되고 있다.

【0004】 전자기 유도를 이용한 무선전력 전송 시스템은 송신측과 수신측에 형성된 전기신호가 코일을 통해 무선으로 전달되기 때문에 사용자는 휴대용 기기와 같은 전자기기를 손쉽게 충전할 수 있다.

【0005】 그러나, 수신 측의 구성을 이루는 수신 코일, 근거리 통신안테나 및 인쇄회로기판 각각의 두께로 인해 전자기기의 전체적인 사이즈가 커지고, 전자기기에 내장하는 것이 쉽지 않았다. 특히, 수신 코일 및 근거리 통신안테나 각각의 두께만큼 사이즈가 증가하고, 근거리 통신안테나 및 인쇄회로기판 각각의 두께만큼 사이즈가 증가하는 문제가 있다.

【0006】 또한, 근거리 통신안테나의 내부에 과전류가 흐르는 경우에 효과적으로 대처할 수 없었다.

【0007】 또한, 수신 코일에 형성된 자기장은 전자기기 내부에 영향을 주어 오작동을 일으키는 문제가 있다.

【발명의 내용】

【해결하고자 하는 과제】

【0008】 본 발명은 수신 코일, 근거리 통신안테나 및 인쇄회로기판의 적절한 배치를 통해 무선전력 수신장치의 두께를 최소화하는 무선전력 수신장치의 제공을 목적으로 한다.

【0009】 본 발명은 근거리 통신안테나를 인쇄회로기판 내부에 포함시켜 두께를 감소시키는 무선전력 수신장치의 제공을 목적으로 한다.

【0010】 본 발명은 보호부를 통해 과전류가 흐르는 것을 방지하는 무선전력 수신장치 제어방법의 제공을 목적으로 한다.

【과제의 해결 수단】

【0011】 본 발명의 실시예에 따른 외부의 무선전력 송신장치로부터 무선으로 전력을 수신하는 무선전력 수신장치는 일정 영역에 수용공간이 있는 인쇄회로기판; 상기 인쇄회로기판의 수용공간 내부에 배치되어, 상기 무선전력 송신장치로부터 전력을 수신하기 위한 수신 코일; 및 상기 인쇄회로 기판에 상기 수신 코일을 감싸는 형태로 배치된 근거리 통신 안테나를 포함한다.

【0012】 본 발명의 실시예에 따른 외부의 무선전력 송신장치로부터 무선으로 전력을 수신하는 무선전력 수신장치는 근거리 통신을 수행하기 위한 근거리 통신 안테나; 상기 무선전력 송신장치로부터 무선으로 전력을 수신하기 위한 수신코일; 상기 전력의 수신여부에 따라 상기 근거리 통신안테나의 통전상태를 변경하는 스위치; 및 상기 전력의 수신여부에 따라 상기 스위치를 개방 또는 단락시키는 제어부를 포함한다.

【0013】 본 발명의 실 시예에 따른 외부와 통신하는 근거리 통신안테나를 포함한 무선전력 수신장치의 제어 방법은 송신 유도 코일로부터 전자기 유도에 의한 전력의 수신여부를 판단하는 단계; 상기 판단결과, 상기 전력을 수신하는 경우, 상기 근거리 통신안테나의 통전상태를 변경하는 스위치를 개방시키는 단계; 상기 수신한 전력의 양이 임계수치 이상인지 판단하는 단계; 및 상기 판단결과, 상기 전력의 양이 임계수치 이상인 경우, 상기 스위치를 단락시키는 단계를 포함한다.

【발명의 효과】

【0014】 본 발명의 실시예에 따르면, 다음과 같은 효과가 있다.

【0015】 첫째, 수신 코일, 근거리 통신안테나 및 인쇄회로기판의 적절한 배치를 통해 무선전력 수신장치의 두께를 최소화할 수 있다.

【0016】 둘째, 내부에 과도한 전류가 흐르는 것을 차단하여 무선전력 수신장치의 파손을 막을 수 있고, 자기장을 차단하여 기기의 오작동을 방지할 수 있는 등의 효과가 있다.

【도면의 간단한 설명】

【0017】 도 1은 본 발명의 일 실시예에 따른 무선 전력 전송 시스템을 나타낸다.

도 2는 본 발명의 일 실시예에 따른, 송신 유도 코일의 등가 회로도이다.

도 3은 본 발명의 일 실시예에 따른, 무선전력 전송 시스템의 등가회로이다.

도 4는 본 발명의 일 실시예에 따른 무선전력 수신장치의 블록도이다.

도 5는 본 발명의 일 실시예에 따른 무선전력 수신장치의 구성 예 이다.

도 6은 본 발명의 일 실시예에 따른 무선전력 수신장치의 구성형태를 도시한 도면이다.

도 7은 본 발명의 일 실시예에 따른 무선전력 수신장치의 구성요소가 배치된 상태의 단면도이다.

도 8의 (a)는 본 발명의 일 실시예에 따른 무선전력 수신장치의 하면을 도시한 도면이고, 도 8의 (b)는 무선전력 수신장치의 상면을 도시한 도면이다.

도 9는 본 발명의 일 실시예에 따른 무선전력 수신장치에 포함된 차폐부의

부착 예이다.

도 10은 본 발명의 일 실시예에 따른 무선전력 수신장치에 포함된 차폐부의 삽입 예이다.

도 11은 본 발명의 일 실시예에 따른 무선전력 수신장치의 제어방법을 나타낸 흐름도이다.

【발명을 실시하기 위한 구체적인 내용】

【0018】 이하에서는, 첨부된 도면을 참조하여 본 발명의 바람직한 실시예에 대하여 본 발명이 속하는 기술분야에서 통상의 지식을 가진 자가 용이하게 실시할 수 있도록 상세히 설명한다.

【0019】 도 1은 본 발명의 일 실시예에 따른 무선 전력 전송 시스템을 나타낸다.

【0020】 전력 소스(100)에서 생성된 전력은 무선전력 송신장치(200)로 전달되고, 전달된 전력은 다시 전자기 유도 현상에 의해 무선전력 송신장치(200)로 전달된다.

【0021】 보다 구체적으로 살펴보면, 전력 소스(100)는 소정 주파수의 교류 전력을 제공하는 교류 전력 소스이다.

【0022】 무선전력 송신장치(200)는 송신 유도 코일(210)로 구성된다. 송신 유도 코일(210)은 전력 소스(100)와 연결되며, 교류 전류가 흐른다. 송신 유도 코일(210)에 교류 전류가 흐르면, 전자기 유도에 의해 물리적으로 이격되어 있는 수

신 공진 코일(310)에도 교류 전류가 유도되어 무선전력 수신장치(300)로 전력이 전달된다.

【0023】 임피던스가 매칭된 2개의 LC 회로 사이는 전자기 유도에 의해 전력이 전송될 수 있다. 이와 전자기 유도에 의한 전력 전송은 높은 효율로 전력 전달이 가능하게 한다.

【0024】 무선전력 수신장치(300)는 수신 코일(310), 정류회로(320) 및 부하(330)로 구성된다. 송신 유도 코일(210)에 의해 송신된 전력은 전자기 유도에 의해 수신 코일(310)에 수신된다. 수신 코일(310)로 전달된 전력은 정류 회로(320)를 통해 정류되어 부하(330)로 전달된다.

【0025】 도 2는 본 발명의 일 실시예에 따른, 송신 유도 코일(210)의 등가 회로도이다. 도 2에 도시된 바와 같이 송신 유도 코일(210)은 인덕터(L1)와 캐패시터(C1)로 구성될 수 있으며, 이들에 의해 적절한 인덕턴스와 캐패시턴스 값을 갖는 회로를 구성하게 된다. 캐패시터(C1)는 가변 캐패시터일 수 있으며, 가변 캐패시터를 조절하여 임피던스 매칭을 수행할 수 있다. 수신 코일(310)의 등가 회로도 도 2에 도시된 것과 동일할 수 있다.

【0026】 도 3은 본 발명의 일 실시예에 따른, 무선전력 전송 시스템의 등가 회로이다. 도 3에 도시된 바와 같이, 송신 유도 코일(210)과 소정 인덕턴스 값과

캐패시턴스 값을 갖는 인덕터(L1)와 캐패시터(C1)로 구성될 수 있다.

【0027】 또한, 도 3에 도시된 바와 같이 수신 코일(310)은 소정 인덕턴스 값과 캐패시턴스 값을 갖는 인덕터(L2)와 캐패시터(C2)로 구성될 수 있다. 평활 회로(320)는 다이오드(D1)와 평활 캐패시터(C3)로 구성될 수 있으며, 교류 전력을 직류 전력을 변환하여 출력한다. 부하(330)는 직류 전원으로 표시되어 있으나, 직류 전력을 필요로 하는 임의의 충전지 또는 장치일 수 있다.

【0028】 도 4는 본 발명의 일 실시예에 따른 무선전력 수신장치의 블록도이다.

【0029】 무선전력 수신장치(300)는 수신 코일(310), 근거리 통신안테나(340), 스위치(350), 보호부(360), 근거리 통신모듈(370), 차폐부(380), 제어부(390)를 포함한다.

【0030】 수신 코일(310)은 무선전력 송신장치(200)의 송신 유도 코일(210)과 전자기 유도에 의해 전력을 수신한다. 즉, 송신 유도 코일(210)에 교류전류가 흘러 자기장이 발생하면, 발생된 자기장에 의해 인접한 수신 코일(310)에 전압이 유도되어 교류 전류가 흐른다. 일 실시예에서 수신 코일(310)은 인쇄회로기판(301)의 중앙에 배치될 수 있으나, 이에 한정되지 않는다.

【0031】 수신 코일(310)은 하나 이상의 도선이 감겨진 형태로 구성되며, 사각형 또는 원형의 나선 형태로 감겨져 구성될 수 있으나, 이에 한정되지 않는다.

【0032】 근거리 통신안테나(340)는 근거리 무선통신이 가능한 리더기와 통신을 수행한다. 근거리 통신안테나(340)는 상기 리더기와 정보를 송수신하는 안테나의 역할을 수행할 수 있다. 일 실시예에서 근거리 통신안테나(340)는 수신 코일(310)의 외각에 배치될 수 있다. 일 실시예에서 수신 코일(310)이 인쇄회로기판(301)의 중앙에 배치된 경우, 근거리 통신안테나(340)는 수신 코일(310)을 감싸도록 배치될 수 있다. 이러한 배치를 통해, 무선전력 수신장치(300)의 두께를 최소화할 수 있다.

【0033】 근거리 통신안테나(340)와 수신 코일(310)은 후술할 인쇄회로기판(301)에 형성될 수 있다. 일 실시예에서 근거리 통신안테나(340)만이 인쇄회로기판(301)에 형성될 수 있고, 근거리 통신안테나(340)와 수신 코일(310)이 인쇄회로기판(301)에 같이 형성될 수도 있다.

【0034】 근거리 통신안테나(340) 및 후술할 근거리 통신모듈(370)에서 사용되는 근거리 통신규격은 다양한 기술이 사용될 수 있으나, NFC(Near Field Communication)을 이용함이 바람직하다. NFC(Near Field Communication)는 13.56MHz의 대역을 가지며,가까운 거리의 무선통신을 하기 위한 기술이다.

【0035】 스위치(350)는 근거리 통신안테나(340)와 연결되고, 후술할 제어부(390)로부터 개방 또는 단락신호를 수신하여 근거리 통신안테나(340)의 통전상태를 변경할 수 있다. 제어부(390)는 수신 코일(310)이 송신 유도 코일(210)로부터 전자기 유도에 의한 전력을 수신하는 것으로 판단한 경우, 스위치(350)에 개방신호를 전송하여 근거리 통신안테나(340)에 흐르는 전류를 차단한다.

【0036】 보호부(360)는 임계전류 값 이상의 전류가 흐르는 경우에 동작하여, 근거리 통신모듈(370)에 상기 임계전류 값 이상의 전류가 전달되지 않도록 한다.

【0037】 일 실시예로 보호부(360)는 적어도 하나 이상의 제너 다이오드를 포함할 수 있다. 제너 다이오드는 회로에 임계 전류 값 이하만을 흐르게 할 수 있는 다이오드이다. 여기서, 임계전류 값은 설정에 따라 변경될 수 있는 값이고, 근거리 통신모듈(370)이 정상적으로 동작할 수 있는 한계 값일 수 있다.

【0038】 보호부(360)는 근거리 통신안테나(340)에서 전달되는 전류가 임계전류 값 이상인 경우, 전류의 이동방향 또는 흐름을 바꾸어 근거리 통신모듈(370)에 과도한 전류가 흐르지 않게 한다. 과도한 전류는 제너 다이오드를 통해 흘러 열에너지 형태로 방출된다. 보호부(360)는 근거리 통신모듈(370)에 과도한 전류가 흐르는 것을 차단하여 근거리 통신모듈(370)의 파손을 막을 수 있다.

【0039】 근거리 통신모듈(370)은 근거리 통신안테나(340)로부터 전류를 제공받을 수 있다. 근거리 통신모듈(370)은 다양한 형태의 근거리 통신 기술이 적용될 수 있으나, NFC(NEAR FIELD COMMUNICATION) 통신규격을 이용함이 바람직하다.

【0040】 차폐부(380)는 수신 코일(310)에 형성되는 자기장을 차단할 수 있다. 이는 수신 코일(310)에 형성된 자기장이 전자기기의 다른 부품에 영향을 미쳐 오작동을 방지하기 위함이다.

【0041】 차폐부(380)는 페라이트를 포함하여 구성될 수 있으나, 이에 한정되지 않는다.

【0042】 차폐부(380)는 후술할 인쇄회로기판(301) 내부에 삽입될 수 있다. 일 실시예에서 차폐부(380)는 인쇄회로기판(301)이 제작되는 공정에서 삽입되어 차폐부(380)를 부착하는 추가적인 단계가 생략될 수 있다. 이로 인해, 무선전력 수신장치(300)의 제조공정을 단순화시킬 수 있다. 또한, 양면접착제를 사용하여 인쇄회로기판(301)에 부착되는 것이 아니므로, 양면접착제의 두께만큼 무선전력 수신장치(300)의 두께를 감소시킬 수 있고, 가격이 절감된다.

【0043】 제어부(390)는 무선전력 수신장치(300)의 전반적인 동작을 제어할 수 있다.

【0044】 제어부(390)는 스위치(350)를 개방 또는 단락시켜 근거리 통신안테나(340)의 통전상태를 변경할 수 있다. 스위치(350)가 단락된 상태에서 수신 코일(310)에 전류가 유도되면, 제어부(390)는 스위치(350)를 개방시켜 근거리 통신안테나(340)에 흐르는 전류를 차단시킨다. 스위치(350)가 개방된 상태에서, 수신 코일(310)에 전류가 유도되지 않으면, 제어부(390)는 스위치(350)를 단락시킨다.

【0045】 제어부(390)는 무선전력 수신장치(300)가 수신한 전력의 양이 임계수치 이상인 경우, 스위치(350)를 단락시킬 수 있다. 일 실시예에서 임계수치는 사용자의 설정에 따라 변경 가능한 수치일 수 있다.

【0046】 도 5는 본 발명의 일 실시예에 따른 무선전력 수신장치의 구성 예이다.

【0047】 도 5를 참조하면, 인쇄회로기판(301)에 수신 코일(310)과 근거리 통신안테나(340)가 형성되어 있다. 수신 코일(310)은 인쇄회로기판(301)의 중앙에 배치되어 있고, 근거리 통신안테나(340)은 인쇄회로기판(301)의 외곽에 배치되어 수신 코일(310)을 감싸는 형태로 배치되어 있다.

【0048】 스위치(350)가 단락되어 있는 경우, 근거리 통신안테나(340)는 근거리 통신모듈(370)에 전류를 전송하여 근거리 통신모듈(370)이 동작 가능한 상태에 있도록 만든다. 만약, 외부의 영향에 의해 근거리 통신안테나(340)에 흐르는 전류가 임계 전류 값 이상이 된다면, 보호부(360)가 동작한다. 일 실시예에서 보호부(360)가 하나 이상의 제너 다이오드를 포함하여 구성되는 경우, 임계 전류 값 이상의 전류가 제너 다이오드를 통해 흐르게 된다. 도 5를 참조하면, A 방향으로 흐르는 전류가 임계 전류 값 이상인 경우, 보호부(360)의 위쪽에 위치한 제너 다이오드로 임계전류 값 이상의 전류가 흐른다. 제너 다이오드를 통해 흐르는 과도한 전류는 열 에너지의 형태로 방출된다. 이 경우, 보호부(360)는 근거리 통신모듈(370)에 과도한 전류가 흐르는 것을 방지하여 근거리 통신모듈(370)의 파손을 방지할 수 있다.

【0049】 도 5를 참조하면, B 방향으로 흐르는 전류가 임계 전류 값 이상인 경우도 위와 같은 과정을 따른다.

【0050】 도 6은 본 발명의 일 실시예에 따른 무선전력 수신장치의 구성형태를 도시한 도면이다.

【0051】 도 6을 참조하면, 일 실시예로 케이스(302)가 휴대용 단말기의 케이스인 경우를 들어 설명한다. 무선전력 수신장치(300)의 개략적인 구성요소는 케이스(302), 인쇄회로기판(301), 수신 코일(310), 근거리 통신안테나(340), 차폐부(380)를 포함한다.

【0052】 도 7은 본 발명의 일 실시예에 따른 무선전력 수신장치의 구성요소가 배치된 상태의 단면도이다.

【0053】 인쇄회로기판(301)은 일정영역에 수용공간을 가지고 있다. 일 실시예에서 일정영역은 인쇄회로기판(301)의 중앙영역을 의미할 수 있다. 일 실시예에서 일정영역은 인쇄회로기판(301)의 중앙영역을 의미할 수 있고, 상기 중앙영역은 사각형, 원형을 포함한 다각형의 형태로 수용공간을 가질 수 있다.

【0054】 수신 코일(310)은 인쇄회로기판(301)의 수용공간 내부에 배치되고, 송신 유도 코일(210)로부터 전자기 유도에 의해 전력을 수신한다. 일 실시예에서 수신 코일(310)의 두께와 인쇄회로기판(301)의 두께는 동일하도록 제작되거나 수신 코일(310)의 두께가 인쇄회로기판(301)의 두께보다 작도록 제작될 수 있다. 이 경우, 기존에 수신 코일(310)과 근거리 통신안테나(340) 각각에 대한 두께로 인해 무선전력 수신장치(300)의 두께가 증가하는 것을 방지하여, 휴대용 단말기의 케이스

에 장착시 내장이 용이한 장점이 있다.

【0055】일 실시예에서 수신 코일(310)은 인쇄회로기판(310)의 수용공간의 형태와 일치되도록 형성될 수 있다. 예를 들어, 인쇄회로기판(301)의 수용공간 형태가 사각형인 경우, 수신 코일(310) 또한, 도선이 사각형으로 감겨진 형태일 수 있고, 인쇄회로기판(301)의 수용공간 형태가 원형인 경우, 수신 코일(310) 또한, 도선이 원형으로 감겨진 형태일 수 있는 등 다양한 형태를 가질 수 있다.

【0056】근거리 통신안테나(340)는 인쇄회로기판(301) 내부에 포함되고, 수신 코일(310)을 감싸는 형태로 구성될 수 있다. 일 실시예에서 근거리 통신안테나(340)는 인쇄회로기판(301) 내부에 매립되어 제작될 수 있고, 수신 코일(310)을 원형 또는 사각형 등 다양한 형태로 수신 코일(310)의 외각을 감싸는 형태로 구성될 수 있다. 이 경우, 기존에 인쇄회로기판(301)과 근거리 통신안테나(340) 각각에 대한 두께로 인해 무선전력 수신장치(300)의 두께가 증가하는 것을 방지하여, 휴대용 단말기의 케이스에 장착시 내장이 용이한 장점이 있다.

【0057】무선전력 수신장치(300)는 수신 코일(310)에 형성되는 자기장을 차단하는 차폐부(380)를 더 포함할 수 있다. 일 실시예에서 차폐부(380)는 수신 코일(310)이 차지하는 면적에 대응되도록 수신 코일(310)의 상면에 배치될 수 있다. 일 실시예에서 차폐부(380)는 수신 코일(310) 및 근거리 통신안테나(340)이 차지하는 면적에 대응되도록 수신 코일(310) 및 근거리 통신안테나(340)의 상면에 배치될 수 있다.

【0058】일 실시예에서 차폐부(380)는 일정영역에 수용공간을 가질 수 있다.

차폐부(380)의 수용공간에는 인쇄회로기판(301)의 상면에 위치한 무선충전회로(375)가 배치될 수 있다. 무선충전회로(375)는 교류 전력을 직류전력으로 변환하는 정류회로, 노이즈 신호를 제거하는 커패시터, 무선전력 수신에 대한 전반적인 동작을 수행하는 메인IC칩 등을 포함할 수 있다.

【0059】일 실시예에서 차폐부(380)의 두께와 무선충전회로(375)의 두께는 동일하도록 제작되거나, 무선충전회로(375)의 두께가 차폐부(380)보다 작도록 제작될 수 있다. 이 경우, 기존에 차폐부(380)와 무선충전회로(375) 각각에 대한 두께로 인해 무선전력 수신장치(300)의 두께가 증가하는 것을 방지하여, 휴대용 단말기의 케이스에 장착시 내장이 용이한 장점이 있다.

【0060】도 8의 (a)는 본 발명의 일 실시예에 따른 무선전력 수신장치의 하면을 도시한 도면이고, 도 8의 (b)는 무선전력 수신장치의 상면을 도시한 도면이다.

【0061】도 8의 (a)를 참조하면, 인쇄회로기판(301), 수신 코일(310), 근거리 통신안테나(340)의 배치에 대한 일 실시예가 도시되어 있다. 인쇄회로기판(301)은 중앙영역 부분에 수용공간을 가지고, 수용공간에는 사각형 형태의 수신 코일(310)이 배치되어 있다. 근거리 통신안테나(340)는 인쇄회로기판(301)의 내부에 매립되어 있는 형태에 있다. 이 경우, 기존에 인쇄회로기판(301)과 근거리 통신안테나(340) 각각에 대한 두께로 인해 무선전력 수신장치(300)의 두께가 증가하는 것을 방지하여, 휴대용 단말기의 케이스에 장착시 내장이 용이한 장점이 있다.

【0062】 또한, 수신 코일(310)의 두께와 인쇄회로기판(301)의 두께는 동일하도록 제작되거나 수신 코일(310)의 두께가 인쇄회로기판(301)의 두께보다 작도록 제작될 수 있다. 이 경우, 기존에 수신 코일(310)과 근거리 통신안테나(340) 각각에 대한 두께로 인해 무선전력 수신장치(300)의 두께가 증가하는 것을 방지하여, 휴대용 단말기의 케이스에 장착시 내장이 용이한 장점이 있다.

【0063】 도 8의 (b)를 참조하면, 무선충전회로(375), 차폐부(380)의 배치에 대한 일 실시예가 도시되어 있다. 차폐부(380)는 일정영역에 수용공간을 가지고, 차폐부(380)의 수용공간에는 무선충전회로(375)가 배치될 수 있다.

【0064】 일 실시예에서 차폐부(380)의 두께와 무선충전회로(375)의 두께는 동일하도록 제작되거나, 무선충전회로(375)의 두께가 차폐부(380)의 두께보다 작도록 제작될 수 있다. 이 경우, 기존에 차폐부(380)와 무선충전회로(375) 각각에 대한 두께로 인해 무선전력 수신장치(300)의 두께가 증가하는 것을 방지하여, 휴대용 단말기의 케이스에 장착시 내장이 용이한 장점이 있다.

【0065】 도 9는 본 발명의 일 실시예에 따른 무선전력 수신장치에 포함된 차폐부의 부착 예이다.

【0066】 도 9을 참조하면, 무선전력 수신장치(300)를 측면에서 바라 본 구성예가 도시되어 있다. 차폐부(380)는 인쇄회로기판(301)에 근거리 통신안테나(340) 또는 도시하지는 않았지만, 수신 코일(310)을 형성한 후, 인쇄회로기판(301)의 밑

부분에 양면접착제(303)를 이용하여 차폐부(380)를 부착한다. 그러나, 이 방법은 인쇄회로기판(301)의 제작 후 별도의 차폐부(380) 부착 공정이 필요해 비용이 증가하는 문제와 무선전력 수신장치(300)의 두께가 높아지는 문제가 있다.

【0067】 도 10은 본 발명의 일 실시예에 따른 무선전력 수신장치에 포함된 차폐부의 삽입 예이다.

【0068】 도 10을 참조하면, 무선전력 수신장치(300)를 측면에서 바라 본 구성 예가 도시되어 있다. 이 방법은 인쇄회로기판(301)에 근거리 통신안테나(340) 또는 도시하지는 않았지만, 수신 코일(310)을 형성한 후, 인쇄회로기판(301)의 사이에 차폐부(380)를 삽입한다. 차폐부(380)를 인쇄회로기판(301) 내부에 삽입하면, 양면접착제의 두께만큼 무선전력 수신장치(300)의 두께를 감소시킬 수 있고, 별도의 차폐부(380)부착 공정이 필요없게 되므로 비용절감의 효과가 있다.

【0069】 도 11은 본 발명의 일 실시예에 따른 무선전력 수신장치의 제어방법을 나타낸 흐름도이다.

【0070】 제어부(390)는 수신 코일(310)이 송신 유도 코일(210)로부터 전자기 유도에 의한 전력을 수신 받는지 여부에 대한 판단을 할 수 있다(S101). 일 실시예로 무선전력 수신장치(300)는 별도의 자기장 검출수단(미도시)을 두어 전력의 수신 여부를 판단할 수 있다.

【0071】 상기 판단결과, 수신 코일(310)이 송신 유도 코일(210)로부터 전자기 유도에 의한 전력을 수신 받는 것으로 판단된 경우, 근거리 통신안테나(340)의 통전상태를 변경하는 스위치(350)를 개방시킬 수 있다(S103). 즉, 제어부(390)는 스위치(350)에 개방신호를 전송하여 근거리 통신안테나(340)에 흐르는 전류를 차단할 수 있다. 일 실시예에서 수신 코일(310)이 송신 유도 코일(210)로부터 전자기 유도에 의한 전력을 수신 받는 것으로 판단된 경우는 무선전력 수신장치(300)가 충전되는 상태를 의미할 수 있다.

【0072】 그 후, 제어부(390)는 무선전력 수신장치(300)가 수신한 전력의 양이 임계수치 이상인지 판단할 수 있다(S105). 일 실시예에서 임계수치는 사용자의 설정에 따라 변경 가능한 수치일 수 있다. 일 실시예에서 임계수치는 무선전력 수신장치(300)가 100% 충전된 상태를 의미할 수 있다.

【0073】 그 후, 제어부(390)는 상기 전력의 양이 임계수치 이상인 경우, 상기 스위치를 단락시킨다(S107). 일 실시예에서 이 경우 무선전력 수신장치(300)는 충전모드를 종료하고, 통신모드로 동작되는 상태를 의미할 수 있다.

【0074】 상기와 같은 제어를 통해 무선전력 수신장치(300)가 충전모드 또는 통신모드 중 어느 하나로 동작할 수 있다.

【0075】 그 후, 제어부(390)는 근거리 통신안테나(340)에 흐르는 전류가 임계 전류 값 이상인지 판단할 수 있다(S109). 근거리 통신안테나(340)에 흐르는 전류가 임계 전류 값 이상인 경우, 상기 전류의 이동방향을 변경할 수 있다(S111).

일 실시예에서 임계 전류 값이란, 근거리 통신모듈(370)이 정상적으로 동작할 수 한계 값을 의미할 수 있다. 일 실시예에서 임계 전류 값은 설계자의 설정에 따라 변경될 수 있는 값을 의미할 수 있다. 일 실시예에서 전류의 이동방향 변경은 제너 다이오드를 이용할 수 있다. 제너 다이오드를 통해 흐르는 임계 전류 값 이상의 전류는 열 에너지의 형태로 방출된다. 이 경우, 근거리 통신모듈(370)에 과도한 전류가 흐르는 것을 방지하여 근거리 통신모듈(370)의 파손을 방지할 수 있다.

【0076】 본 발명은 전자기 유도를 이용한 무선전력 수신장치를 예로 들어 설명하였으나, 자기 공진을 이용하는 무선전력 수신장치에도 그대로 적용 가능하며, 이러한 경우 수신 코일(310)에 전력을 전달하기 위한 수신공진코일을 추가적으로 구비할 수 있다. 이러한 수신공진코일 역시 인쇄회로기판(301)의 수용공간 내에 배치될 경우 동일한 두께 감소 효과를 발휘할 수 있다.

【0077】 또한, 이상에서는 본 발명의 바람직한 실시예에 대하여 도시하고 설명하였지만, 본 발명은 상술한 특정의 실시예에 한정되지 아니하며, 청구범위에서 청구하는 본 발명의 요지를 벗어남이 없이 당해 발명이 속하는 기술분야에서 통상의 지식을 가진 자에 의해 다양한 변형 실시가 가능한 것은 물론이고, 이러한 변형 실시들은 본 발명의 기술적 사상이나 전망으로부터 개별적으로 이해 되어서는 안될 것이다.

【부호의 설명】

【0078】 100: 전력 소스

200: 무선전력 송신장치

210: 송신 유도 코일

300: 무선전력 수신장치

301: 인쇄회로기판

302: 케이스

303: 양면 접착제

310: 수신 코일

320: 평활회로

330: 부하

340: 근거리 통신안테나

350: 스위치

360: 보호부

370: 근거리 통신모듈

375: 무선충전회로

380: 차폐부

390: 제어부

【특허청구범위】

【청구항 1】

외부의 무선전력 송신장치로부터 무선으로 전력을 수신하는 무선전력 수신장치로서,

일정 영역에 수용공간이 있는 인쇄회로 기판;

상기 인쇄회로기판의 수용공간 내부에 배치되어, 상기 무선전력 송신장치로부터 전력을 수신하기 위한 수신 코일; 및

상기 인쇄회로 기판에 상기 수신 코일을 감싸는 형태로 배치된 근거리 통신 안테나를 포함하는 무선전력 수신장치.

【청구항 2】

제1항에 있어서,

상기 수신 코일의 두께는 상기 인쇄회로기판의 두께 이하인 것을 특징으로 하는 무선전력 수신장치.

【청구항 3】

제1항에 있어서,

상기 인쇄회로기판의 수용공간 형태와 상기 수신 코일의 형태는 일치하도록 제작된 무선전력 수신장치.

【청구항 4】

제1항에 있어서,

상기 수신 코일에서 형성되는 자기장을 차단하는 차폐부를 더 포함하는 무선전력 수신장치.

【청구항 5】

제4항에 있어서, 상기 차폐부는,

상기 수신 코일이 차지하는 면적에 대응되도록 상기 수신 코일의 상면에 배치되는 무선전력 수신장치.

【청구항 6】

제4항에 있어서,

상기 차폐부의 일정영역에 수용공간을 가지고, 상기 차폐부의 수용공간에 무선충전회로를 더 포함하는 무선전력 수신장치.

【청구항 7】

제6항에 있어서,

상기 무선충전회로의 두께는 상기 차폐부의 두께 이하인 것을 특징으로 하는 무선전력 수신장치.

【청구항 8】

제1항에 있어서, 상기 근거리 통신안테나는

상기 인쇄회로기판 내부에 배치된 것을 특징으로 하는 무선전력 수신장치.

【청구항 9】

제1항에 있어서, 상기 근거리 통신안테나는

NFC(NEAR FIELD COMMUNICATION) 안테나인 것을 특징으로 하는 무선전력 수신장치.

【청구항 10】

외부의 무선전력 송신장치로부터 무선으로 전력을 수신하는 무선전력 수신장치로서,

근거리 통신을 수행하기 위한 근거리 통신 안테나;

상기 무선전력 송신장치로부터 무선으로 전력을 수신하기 위한 수신코일;

상기 전력의 수신여부에 따라 상기 근거리 통신안테나의 통전상태를 변경하는 스위치; 및

상기 전력의 수신여부에 따라 상기 스위치를 개방 또는 단락시키는 제어부를 포함하는 수신장치.

【청구항 11】

제10항에 있어서,

상기 근거리 통신안테나는 상기 수신 코일을 둘러싸는 감싸는 형태로 배치된 무선전력 수신장치.

【청구항 12】

제10항에 있어서, 상기 제어부는

상기 전력이 수신된 경우, 상기 스위치를 개방시키는 무선전력 수신장치.

【청구항 13】

제12항에 있어서, 상기 제어부는

상기 무선전력 수신장치가 수신한 전력의 양이 임계수치 이상인 경우, 상기 스위치를 단락시키는 무선전력 수신장치.

【청구항 14】

제10항에 있어서, 상기 근거리 통신안테나는

NFC(NEAR FIELD COMMUNICATION) 안테나인 것을 특징으로 하는 무선전력 수신장치.

【청구항 15】

제10항에 있어서,

상기 근거리 통신안테나로부터 전류를 공급받는 근거리 통신모듈을 더 포함하는 무선전력 수신장치.

【청구항 16】

제10항에 있어서,

상기 근거리 통신안테나에 흐르는 전류가 임계전류 값 이상인 경우, 상기 전류의 이동방향을 변경하는 보호부를 더 포함하는 무선전력 수신장치.

【청구항 17】

제10항에 있어서,

상기 수신 코일에서 형성되는 자기장을 차단하는 차폐부를 더 포함하는 무선

전력 수신장치.

【청구항 18】

제17항에 있어서, 상기 차폐부는,

상기 인쇄회로기판 내부에 삽입되는 무선전력 수신장치.

【청구항 19】

제18항에 있어서, 상기 차폐부는

페라이트를 포함한 무선전력 수신장치.

【청구항 20】

제 10항에 있어서,

일정 영역에 수용공간이 있는 인쇄회로 기판을 더 포함하고,

상기 수신 코일은 상기 인쇄회로기판의 수용공간 내부에 배치되며,

상기 근거리 통신안테나는 상기 수신 코일을 감싸는 형태로 상기 인쇄회로기판에 배치된 것을 특징으로 하는 무선전력 수신장치.

【청구항 21】

외부와 통신하는 근거리 통신안테나를 포함한 무선전력 수신장치의 제어 방법에 있어서,

송신 유도 코일로부터 전자기 유도에 의한 전력의 수신여부를 판단하는 단계;

상기 판단결과, 상기 전력을 수신하는 경우, 상기 근거리 통신안테나의 통전

상태를 변경하는 스위치를 개방시키는 단계;

상기 수신한 전력의 양이 임계수치 이상인지 판단하는 단계; 및

상기 판단결과, 상기 전력의 양이 임계수치 이상인 경우, 상기 스위치를 단락시키는 단계를 포함하는 무선전력 수신장치의 제어 방법.

【청구항 22】

제21항에 있어서, 상기 임계수치는,

사용자의 설정에 따라 변경 가능한 수치인 무선전력 수신장치의 제어 방법.

【청구항 23】

제21항에 있어서,

상기 근거리 통신안테나에 흐르는 전류가 임계전류 값 이상인 경우, 상기 전류의 이동방향을 변경하는 단계를 더 포함하는 무선전력 수신장치의 제어 방법.

【청구항 24】

제23항에 있어서, 상기 근거리 통신안테나에 흐르는 전류가 임계전류 값 이상인 경우, 상기 전류의 이동방향을 변경하는 단계는,

제너 다이오드를 이용하여 상기 전류의 이동방향을 변경하는 단계를 포함하는 무선전력 수신장치의 제어 방법.

제출 일자 : 2011-11-04

【요약서】

【요약】

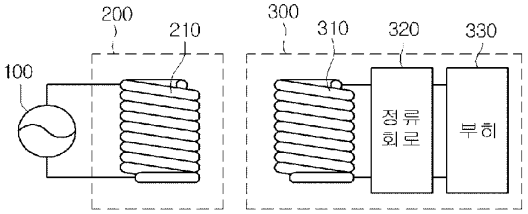
본 발명의 실시예에 따른 외부의 무선전력 송신장치로부터 무선으로 전력을 수신하는 무선전력 수신장치는 일정 영역에 수용공간이 있는 인쇄회로 기판; 상기 인쇄회로기판의 수용공간 내부에 배치되어, 상기 무선전력 송신장치로부터 전력을 수신하기 위한 수신 코일; 및 상기 인쇄회로 기판에 상기 수신 코일을 감싸는 형태로 배치된 근거리 통신 안테나를 포함한다.

【대표도】

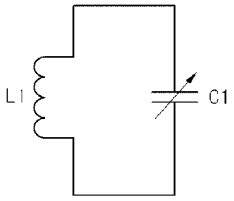
도 7

【도면】

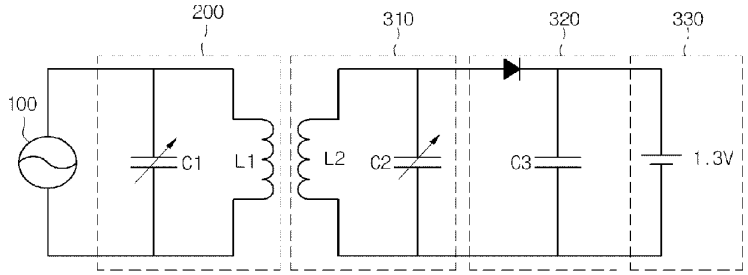
【도 1】


200
210
300
310
320
330
100
정류
회로
부하

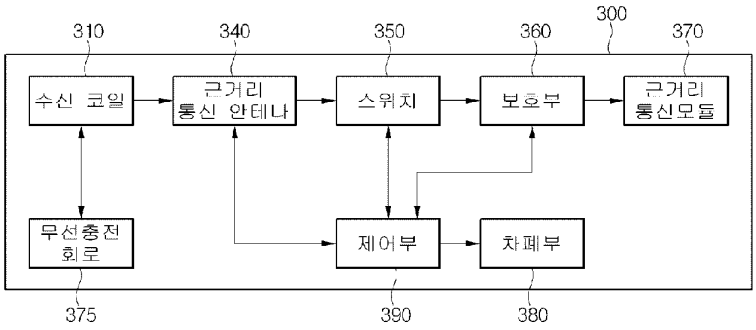
【도 2】


L1
C1

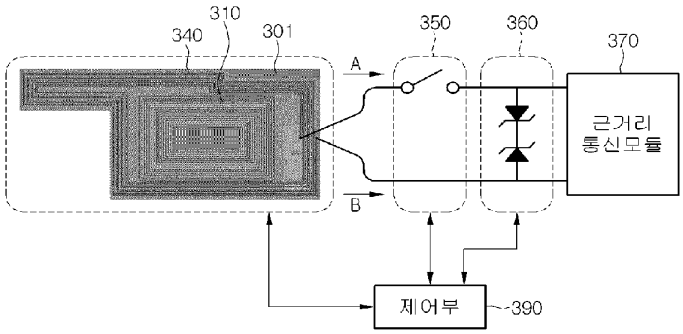
【도 3】


200
310
320
330
100
C1
L1
L2
C2
C3
1.3V

【도 4】


300
310
340
350
360
370
수신 코일
근거리 통신 안테나
스위치
보호부
근거리 통신모듈
무선충전 회로
제어부
차폐부
375
390
380

【도 5】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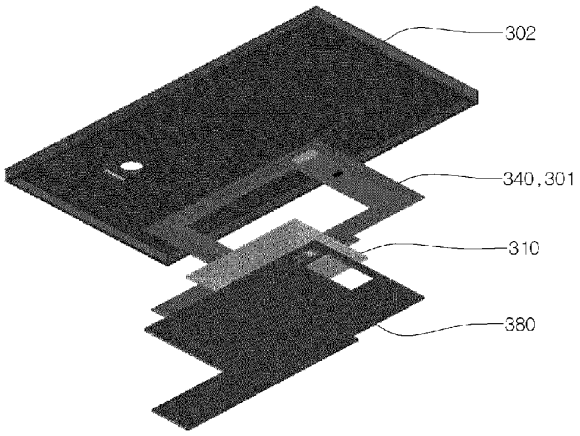

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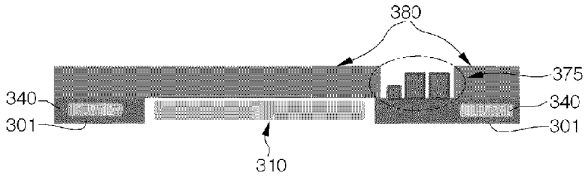

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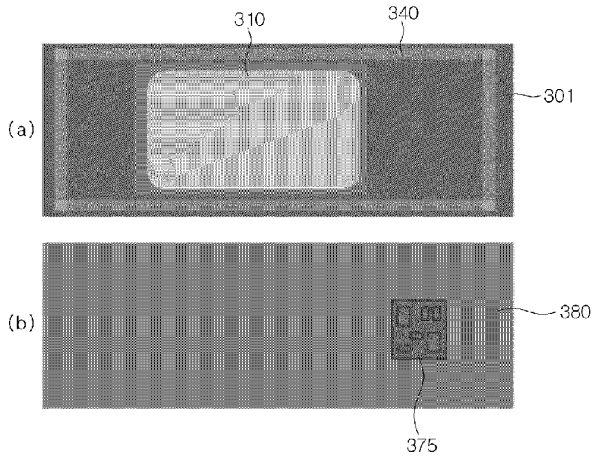

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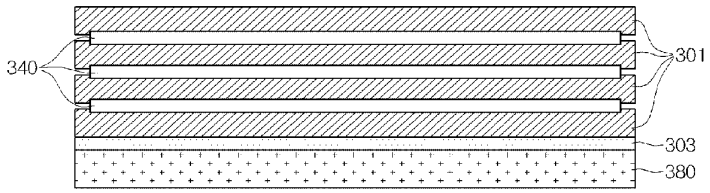

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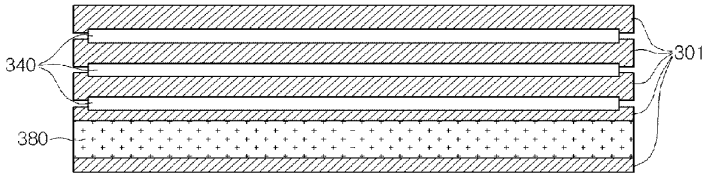

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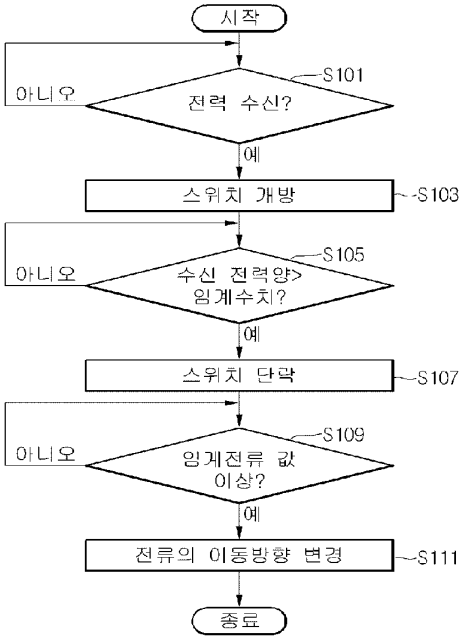
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아니오
임계전류 값
이상?
예
전류의 이동방향 변경
S111
종료

PTO/SB/08A (08-03)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 2

Complete if Known	
Application Number	16/182,258
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First Named Inventor	Ki Min Lee
Art Unit	2683
Examiner Name	
Attorney Docket Number	SUN.LGI.417D3

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. [1]	Document Number Number - Kind Code [2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	U1	2009/0010316-A1	01-08-2009	ROFOUGARAN	ALL
	U2	7,948,208-B2	05-24-2011	PARTOVI *et al.*	ALL
	U3	7,973,635-B2	07-05-2011	BAARMAN *et al.*	ALL
	U4	8,456,856-B2	06-04-2013	LIN *et al.*	ALL

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. [1]	Foreign Patent Document Country Code [3] - Number [4] - Kind Code [5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T [6]
	F1	EP-2 330 683-A1	06-08-2011	SONY CORPORATION	ALL	
	F2	TW-2009-38017-A (With English Abstract) (Equivalent to US 7,973,635-B2)	09-01-2009	ACCESS BUSINESS GROUP INTERNATIONAL LLC	ALL	
	F3	WO-2010/114687-A1 (Equivalent to US 8,456,856-B2)	10-07-2010	MEGICA CORPORATION *et al.*	ALL	

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Sheet 2 of 2

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Examiner Name	
Attorney Docket Number	SUN.LGI.417D3

NON PATENT LITERATURE DOCUMENTS

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	R1	Office Action dated January 18, 2019 in Taiwanese Application No. 106135104, along with its English translation.	

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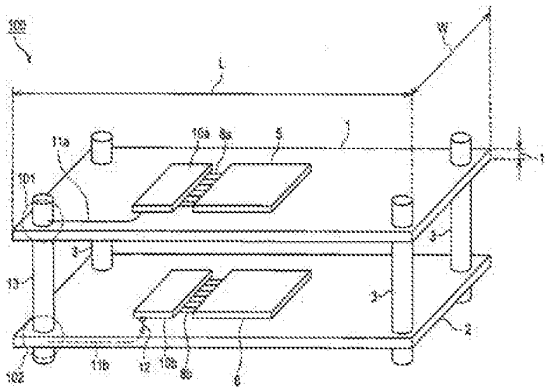
(54) **IN-MILLIMETER-WAVE DIELECTRIC TRANSMISSION DEVICE AND METHOD FOR MANUFACTURING SAME, AND WIRELESS TRANSMISSION DEVICE AND WIRELESS TRANSMISSION METHOD**

(57) An electronic device provided with a plurality of circuit boards uses a support member for supporting the circuit boards as the transmission path of a wireless signal. For example, the electronic device is provided with a first printed circuit board for processing a millimeter-wave signal, a second printed circuit board which is signal-coupled to the printed circuit board and receives the millimeter-wave signal to subject the received signal to signal processing, and a waveguide which is disposed with a predetermined dielectric constant between the printed circuit boards, wherein the waveguide constitutes the dielectric transmission path, and the waveguide supports the printed circuit boards. This configuration makes it possible to receive the electromagnetic wave based on a millimeter-wave signal radiated from one end of the waveguide constituting the dielectric transmission path, at the other end thereof.

FIG.1



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EP 2 330 683 A1

Description

Technical Field

[0001] The present invention relates to an in-millimeter-wave dielectric transmission device, a manufacturing method thereof, a wireless transmission device, and a wireless transmission method. For example, the present invention relates to a mechanism in which a carrier frequency for carrying a movie image, a computer image and the like transmits a signal of a microwave band or a millimeter wave band of 30 GHz to 300 GHz at a high speed.

Background Art

[0002] In the related art, printed boards have been used as plate-shaped parts including electronic parts such as resistors, capacitors and semiconductor integrated circuit devices mounted thereon and to perform electrical wiring. In general, when constituting an electronic device, a plurality of printed boards are provided in parallel in a housing of the electronic device to contribute to a physical configuration or a functional configuration of the electronic device. Furthermore, various methods for fixedly supporting a multi-stage structure, which is formed by stacking printed boards using support members provided at four corners thereof in a housing, have been proposed.

[0003] Meanwhile, with a recent significant increase in the amount of information such as videos and images, various devices have been used to transmit high frequency signals such as millimeter wave signals at a high speed. For such a high speed data transmission device, it is necessary to transmit high frequency signals such as millimeter wave signals with no error.

[0004] Fig. 20 is a perspective view showing an example of the configuration of a high speed data transmission device 900 according to the related art. The high speed data transmission device 900 shown in Fig. 20 has a multi-stage structure formed by stacking two printed boards 1 and 2 using fixing members 3 provided at four corners thereof in order to transmit data between the printed boards 1 and 2 at a high speed. In Fig. 20, the high speed data transmission device 900 includes the two printed boards 1 and 2 and the four fixing members 3 for normal support, and the printed boards 1 and 2 are fixed in parallel to each other by the fixing members 3 provided at the four corners thereof. According to a method of fixing the printed boards 1 and 2, through holes 4 having a predetermined shape are opened in the four corners of each of the printed boards 1 and 2, the fixing members 3 are inserted into the through holes 4, and the printed boards 1 and 2 are held by the fixing members 3 while interposing the fixing members 3 therebetween.

[0005] The printed board 1 is provided on the upper surface thereof with a signal processing unit 5, a connector 7 and an electrical wiring 8. The electrical wiring 8 of the printed board 1 connects the signal processing unit 5 to the connector 7. The printed board 2 is provided on the upper surface thereof with a signal processing unit 6, a connector 7 and an electrical wiring 8. The electrical wiring 8 of the printed board 2 connects the connector 7 to the signal processing unit 6. According to the high speed data transmission device 900, a cable 9 is connected between the connector 7 of the printed board 1 and the connector 7 of the printed board 2, so that data is transmitted between the printed boards 1 and 2 at a high speed.

[0006] Meanwhile, in order to reduce the cost of the high speed data transmission device 900 and the like and improve the arrangement efficiency of the printed boards 1 and 2, there have been attempts to remove the connector 7 and the cable 9. In relation to the improvement of such a type of high speed data transmission device 900, Patent Literature 1 discloses an electronic device that performs data exchange using a wireless communication method.

[0007] According to the electronic device, device configuration units and a wireless communication unit are provided, and the wireless communication unit relays data exchange between the device configuration units through UWB wireless communication in a housing. Based on that fact, a radio wave absorber is provided in the housing to absorb an electromagnetic wave serving as noise of communication between the device configuration units via the wireless communication unit. When the electronic device is configured as described above, the radio wave absorber absorbs an electromagnetic wave in the housing, resulting in the suppression of multipath phasing in the housing.

[0008] Furthermore, Patent Literature 2 discloses fixing members for fixing a plurality of circuit boards and a module using the fixing members. According to the module, a plurality of fixing members provided with light waveguides are provided, optical coupling is achieved between one circuit board and the other circuit board at both ends of each fixing member, and the plurality of circuit boards are fixed while being spaced apart from each other at a predetermined distance. Based on that fact, an optical signal is propagated between the circuit boards through the light waveguides of the fixing members. When the module is configured as described above, it is possible to accurately transmit information between the circuit boards using an optical signal as a medium.

Citation List

Patent Literature

[0009]

Patent Literature 1: Japanese Unexamined Patent Application Publication No 2004-220264 (3 claims Fig. 1)
Patent Literature 2: Japanese Patent Registration No 4077847 (11 claims Fig. 1)

Summary of Invention

Technical Problem

[0010] In recent years, with an increase in a signal processing speed on a printed board, when constructing the high speed data transmission device 900 according to the related art, a high speed data transmission device in which disturbance is reduced by applying a signal transmission technology of a millimeter band, or a data transmission system thereof, the following problems occur.

[0011] i. according to the high speed data transmission device 900 shown in Fig. 20, it is necessary to use the connector 7 and the cable 9 in order to electrically connect the two printed boards 1 and 2. In addition, it is necessary to ensure an area for turning the cable 9 in the housing.

[0012] ii. according to the electronic device using the wireless communication method as disclosed in Patent Literature 1, when the housing is shielded by a metal, a radio wave is reflected in a free space in the housing. The radio reflection in the housing causes multipath interference, resulting in the deterioration of data transmission performance. Thus, in order to reduce the multipath interference, employing a multi-carrier modulation method may be considered. However, this may cause an increase in a system size and power consumption.

[0013] Meanwhile, employing a method of lowering the output level of wireless power of the wireless communication unit to limit a wireless communication area may also be considered. However, the arrangement of the wireless communication unit on the printed board may be limited and the degree of freedom of the arrangement of electronic parts may be restricted.

[0014] iii. according to the module as disclosed in Patent Literature 2, since light is used in order to transmit data, it is necessary to prepare a light emitting element to send light into the light waveguide of the fixing member, a lens, a reflection plate, a light receiving element and the like. Furthermore, due to low permission for positioning of an optical axis and position deviation of the optical axis, it is difficult to configure the high speed data transmission system between the printed boards. Therefore, the structure of a signal processing board for being optically coupled to the fixing member is significantly complicated and the system size is increased, resulting in an increase in the manufacturing cost.

[0015] The present invention is made in view of the above-mentioned issue, and aims to provide a mechanism capable of solving at least one of the above problems.

Solution to Problem

[0016] According to a first aspect of the present invention in order to achieve the above-mentioned object, there is provided an in-millimeter-wave dielectric transmission device including: a first signal processing board for processing a millimeter wave signal; a second signal processing board signal-coupled to the first signal processing board to receive the millimeter wave signal and perform signal processing with respect to the millimeter wave signal; and a support member provided between the first signal processing board and the second signal processing board, wherein the support member constitutes a dielectric transmission path and supports the first signal processing board and the second signal processing board.

[0017] That is, according to the first aspect of the present invention, the in-millimeter-wave dielectric transmission device includes a support member provided between a first signal processing board for processing a millimeter wave signal and a second signal processing board for receiving a millimeter wave signal and performing signal processing with respect to the millimeter wave signal, and the support member constitutes a dielectric transmission path and supports the first signal processing board and the second signal processing board, so that it is possible to use the original support structure of the support member as a signal transmission path and to remove a communication cable, a connector and the like for connecting the first signal processing board to the second signal processing board according to the related art.

[0018] With such a mechanism, an electromagnetic wave based on a millimeter wave signal, which is radiated from one end of a support member constituting a dielectric transmission path, may be received in the other end of the support member. Consequently, since the original support structure of the support member may be used as a signal transmission path, it is possible to remove the communication cable, the connector and the like for connecting a first signal processing

board to a second signal processing board according to the related art.

[0019] A method of manufacturing an in-millimeter-wave dielectric transmission device according to the present invention includes the steps of: forming a first signal processing board for processing a millimeter wave signal; forming a second signal processing board for receiving the millimeter wave signal from the first signal processing board and performing signal processing with respect to the received millimeter wave signal; and providing a support member between the first signal processing board and the second signal processing board, allowing the support member to form a dielectric transmission path, and allowing the support member on the second signal processing board to support the first signal processing board and the second signal processing board.

[0020] In manufacturing the in-millimeter-wave dielectric transmission device according to the present invention, it is possible to manufacture an in-millimeter-wave dielectric transmission device in which the support member constitutes a dielectric transmission path and supports the first signal processing board and the second signal processing board.

[0021] According to a second aspect of the present invention in order to achieve the above-mentioned object, there are provided a wireless transmission device and a wireless transmission method including a first circuit board (of a transmission side) including a first signal converting section for converting a signal to be transmitted to a high frequency signal with a high frequency (e.g., of a millimeter wave band or a microwave band), a second circuit board (of a reception side) including a second signal converting section for receiving a wireless signal (an electromagnetic wave) based on the high frequency signal generated by the signal converting section, and converting the wireless signal to the signal to be transmitted, and a support member provided between the first circuit board and the second circuit board to support the first circuit board and the second circuit board. The wireless signal is not limited to a millimeter wave signal.

[0022] Herein, in the second aspect according to the present invention, the support member constitutes a wireless signal transmission path for transmitting a wireless signal from the first circuit board side to the second circuit board side. That is, in an electronic device including a plurality of circuit boards, it may be said that the support member for supporting the circuit boards is used as a transmission path of a wireless signal. In the support member, a shield member for blocking external radiation of a wireless signal is first provided to surround the transmission path.

[0023] According to the first aspect, the support member may be a cavity waveguide in which a transmission path inside a shield member is hollow. In such a case, the second aspect according to the present invention is characterized in that the support member is not used as a dielectric transmission path and is used as a hollow waveguide by causing the support member to have a hollow structure, as compared with the in-millimeter-wave dielectric transmission device according to the present invention. That is, the support member employing the cavity waveguide is used and the inside of the support member is used for inter-board transmission.

[0024] Furthermore, according to the second aspect, in the support member, a dielectric material may be filled in the transmission path inside the shield member. In such a case, the second aspect according to the present invention is the same in that the support member is used as a dielectric transmission path, as compared with the in-millimeter-wave dielectric transmission device according to the present invention. However, a difference exists in the fact that a wireless signal is not limited to a millimeter wave signal.

Advantageous Effects of Invention

[0025] According to the present invention, a wireless signal (an electromagnetic wave) based on a high frequency signal (including a millimeter wave signal) signal-coupled to one end of a support member constituting a wireless signal transmission path (including a dielectric transmission path) can be transmitted to the other end of the support member, and a high frequency signal (including a millimeter wave signal) signal-coupled to other end can be received. Consequently, since the original support structure of the support member can be used as a wireless signal transmission path, it is possible to remove a communication cable, a connector and the like for connecting a first signal processing board to a second signal processing board according to the related art.

[0026] Since the inside of a support member is used as a transmission path of a wireless signal, it is possible to solve a problem (e.g., multipath interference and the like) caused by reflection of an electromagnetic wave in a free space inside a housing.

[0027] Since the inside of a support member is used as a transmission path of a wireless signal, it is possible to solve a problem (complication of the structure of a signal processing board for being optically coupled to a fixing member, and the like) when employing the mechanism disclosed in Patent Literature 2.

Brief Description of Drawings

[0028]

[Fig. 1] Fig. 1 is a perspective view showing an example of the configuration of a wireless transmission device 500 as a first embodiment.

[Fig. 2A] Fig. 2A is a plan view showing an example of the configuration of an antenna coupling unit 101.
[Fig. 2B] Fig. 2B is a cross-sectional view along a line X1-X2, which shows an example of the configuration of an antenna coupling unit 101.
[Fig. 3] Fig. 3 is a perspective view showing an example of the shape of a waveguide 513 and a dielectric transmission path termination part 30.
[Fig. 4] Fig. 4 is a block diagram showing an example of the configuration of a wireless transmission device 500.
[Fig. 5] Fig. 5 is a process diagram showing an example (1) of forming a wireless transmission device 500.
[Fig. 6] Fig. 6 is a process diagram showing an example (2) of forming a wireless transmission device 500.
[Fig. 7] Fig. 7 is a process diagram showing an example (3) of forming a wireless transmission device 500.
[Fig. 8] Fig. 8 is a perspective view showing an example of a simulation model of a wireless transmission device 500.
[Fig. 9] Fig. 9 is a graph showing an example of a simulation characteristic of a wireless transmission device 500.
[Fig. 10] Fig. 10 is a perspective view showing an example of the configuration of an in-millimeter-wave dielectric transmission device 200 as a second embodiment.
[Fig. 11] Fig. 11 is a perspective view showing an example of the configuration of an in-millimeter-wave dielectric transmission device 300 with a multi-stage structure as a third embodiment.
[Fig. 12] Fig. 12 is a sectional view showing an example of the configuration of an antenna coupling unit 109 of a printed board 1.
[Fig. 13] Fig. 13 is a perspective view showing an example of the configuration of an in-millimeter-wave dielectric transmission device 400 as a fourth embodiment.
[Fig. 14] Fig. 14 is a sectional view showing an example in which an antenna coupling unit 101 is bonded to a fixing member 18.
[Fig. 15] Fig. 15 is a perspective view showing an example of the shape of a fixing member 18 and a dielectric transmission path termination part 30.
[Fig. 16] Fig. 16 is a perspective view showing an example of the configuration of a wireless transmission device 500 as a fifth embodiment.
[Fig. 17A] Fig. 17A is an overall view explaining details of an antenna coupling unit and a waveguide.
[Fig. 17B] Fig. 17B is a sectional view explaining details of an antenna coupling unit and a waveguide.
[Fig. 17C] Fig. 17C is a sectional view of an antenna coupling unit.
[Fig. 17D] Fig. 17D is a plan view showing an antenna structure.
[Fig. 18] Fig. 18 is a diagram explaining an example of a simulation characteristic of a fifth embodiment.
[Fig. 19A] Fig. 19A is a diagram explaining a modified example (a microstrip antenna) of an antenna structure.
[Fig. 19B] Fig. 19B is a diagram explaining a modified example (a patch antenna) of an antenna structure.
[Fig. 19C] Fig. 19C is a diagram explaining a modified example (an inverted-F antenna) of an antenna structure.
[Fig. 19D] Fig. 19D is a diagram explaining a modified example (a differential antenna) of an antenna structure.
[Fig. 20] Fig. 20 is a perspective view showing an example of the configuration of a high speed data transmission device 900 according to the related art.

Reference Signs List

[0029]

1 printed board (first signal processing board)
2 printed board (second signal processing board)
3, 17, 19 fixing member
4, 26 through hole
5, 6, 15 signal processing unit
8a, 8b, 8c electrical wiring
10a, 10b, 10c, 10d, 10e signal generating unit
11a, 11b, 111, 112, 113, 114, 115, 116, 117, 118 transmission line
12 contact hole (via hole)
13, 16, 18 fixing member constituting dielectric transmission path
20 conductor layer
21 transmission line layer
22 line
23a, 23b waveguide
24 conductor part
25 conductor layer
30, 34 dielectric transmission path termination part

30' fixing member termination stop part
31, 35 male thread structure
32, 37 female thread structure
33 gap part
101 ~ 109 antenna coupling unit
100, 200, 300, 400 in-millimeter-wave dielectric transmission device
201 signal input terminal
202 modulation circuit
203 frequency conversion circuit
204 amplifier
206, 207 coupling circuit
208 amplifier
209 frequency amplification circuit
210 demodulation circuit
211 signal output terminal
500 wireless transmission device
501, 502 antenna coupling unit
513 waveguide (support member constituting wireless signal transmission path)
510 dielectric board
520 microstrip line
530B patch antenna

Description of Embodiments

[0030] Hereinafter, preferred embodiments of the present invention will be described in detail with reference to the appended drawings. Note that, in this specification and the drawings, elements that have substantially the same function and structure are denoted with the same reference signs, and repeated explanation is omitted.

[0031] Further, the description will be given in the following order.

1. First embodiment (two boards are stacked using columnar support members and a support member used as a dielectric transmission path is provided at one of four corners of each board)
2. Second embodiment (two boards are stacked using columnar support members and a support member used as a dielectric transmission path is provided at four corners)
3. Third embodiment (three boards are stacked using columnar support members and a support member used as a dielectric transmission path is provided at two of four corners of each board)
4. Fourth embodiment (two boards are provided in a row and horizontally supported by fixing members having a substantially flat U shape, and a fixing member used as a dielectric transmission path is provided at one place)
5. Fifth embodiment (general purpose configuration: a waveguide is used as a support member serving as a wireless signal transmission path)

<First embodiment >

[0032] Fig. 1 is a perspective view showing an example of the configuration of an in-millimeter-wave dielectric transmission device 100 according to the first embodiment. The in-millimeter-wave dielectric transmission device 100 shown in Fig. 1 can be applied to a millimeter wave video data transmission device, a millimeter wave video data transmission system and the like, which convert data of a movie image, a computer image and the like into a millimeter wave signal and transmit the millimeter wave signal at a high speed, and have a carrier frequency of 30 GHz to 300 GHz to carry the millimeter wave signal.

[0033] The in-millimeter-wave dielectric transmission device 100 includes a first signal processing board (hereinafter, simply referred to as a printed board 1), a second signal processing board (hereinafter, simply referred to as a printed board 2), a plurality of fixing members 3 for normal support, and a support member (hereinafter, simply referred to as a fixing member 13) used as a dielectric transmission path, and has a structure in which the printed boards 1 and 2 are supported by the fixing members 3 and 13.

[0034] The printed board 1 converts data of a movie image, a computer image and the like into a millimeter wave signal. The size of the printed board 1, for example, is defined as a length L, a width W and a thickness t. The printed board 1 includes a first signal processing unit 5, a first signal generating unit 10a, a first transmission line 11 a, and a first antenna coupling unit 101.

[0035] The signal processing unit 5 performs a process such as compression with respect to the data of the movie

image, the computer image and the like based on a predetermined standard to output an electrical signal (hereinafter, referred to as an input signal). The signal processing unit 5 is connected to an electrical wiring 8a such as a wiring pattern. The electrical wiring 8a is connected to the signal generating unit 10a. The signal generating unit 10a performs signal processing with respect to the input signal to generate the millimeter wave signal.

[0036] The signal generating unit 10a is connected to one end of the transmission line 11a. The transmission line 11a is electrically connected between the signal generating unit 10a and the antenna coupling unit 101 to transmit the millimeter wave signal. In this embodiment, the transmission line 11a electrically transmits the millimeter wave signal constituting the data of the movie image, the computer image and the like. A scheme of a strip line, a microstrip line, a coplanar line, a slot line and the like is applied to the transmission line 11a on the printed board 1.

[0037] The antenna coupling unit 101 is coupled to (disposed at) the other end of the transmission line 11a. The antenna coupling unit 101 couples the millimeter wave signal, which is transmitted from the signal generating unit 10a through the transmission line 11a, to one end of the fixing member 13. In this embodiment, the antenna coupling unit 101 converts the millimeter wave signal into an electromagnetic wave, and radiates the electromagnetic wave into the fixing member 13 constituting a dielectric transmission path. At the time of bi-directional data transmission, the antenna coupling unit 101 transfers millimeter wave video data between the transmission line 11a connected to the signal generating unit 10a and the fixing member 13 constituting the dielectric transmission path.

[0038] The fixing member 13 is provided between the printed board 1 and the printed board 2 while having a predetermined dielectric constant. As the fixing member 13, a dielectric material at least including a glass epoxy-based, acryl-based, and polyethylene-based resin is used. In this embodiment, the three fixing members 3 are provided at four corners of each of the printed boards 1 and 2 together with the one fixing member 13 which divide the charge. The fixing member 13 is provided at a corner part of each of the printed boards 1 and 2, rather than the arrangement positions of the fixing members 3 for normal support.

[0039] The fixing member 13 not only constitutes the dielectric transmission path but also supports the printed board 1 and the printed board 2 together with the three fixing members 3. The support function includes a case where the printed board 2 holds up and supports the printed board 1 and a case where the printed board 1 is suspended and supports the printed board 2.

[0040] Furthermore, in the support mechanism, the fixing members 3 and 13 are fixed such that the printed board 1 and the printed board 2 are combined with each other in a predetermined direction and maintain the substantially parallel posture, for example, the printed board 1 and the printed board 2 are connected to each other in the vertical direction. When configuring the in-millimeter-wave dielectric transmission device 100 in this way, the printed board 1 and the printed board 2 can be fixedly stacked in a rack configuration in the vertical direction via the fixing members 3 and 13. In addition, the fixing members 3, for example, use a resin bar member formed in a cylindrical shape. Of course, except for the fixing member 13, the fixing members 3 may also use a metal bar member having a predetermined shape.

[0041] The printed board 2 is supported by the other ends of the fixing member 13 constituting the dielectric transmission path and the fixing members 3 for normal support. The printed board 2 is signal-coupled to the printed board 1, receives the millimeter wave signal and performs signal processing with respect to the millimeter wave signal. The printed board 2 has a size substantially equal to that of the printed board 1.

[0042] The printed board 2 includes a second antenna coupling unit 102, a second transmission line 11b, a second signal generating unit 10b, and a second signal processing unit 6. The second antenna coupling unit 102 is signal-coupled to the fixing member 13 constituting the dielectric transmission path, and receives an electromagnetic wave from the fixing member 13 to output a millimeter wave signal. In this embodiment, the second antenna coupling unit 102 converts the electromagnetic wave having been propagated through the dielectric transmission path of the fixing member 13 into the millimeter wave signal. In addition, the second antenna coupling unit 102 has a structure symmetrical to the first antenna coupling unit 101 with respect to the board surface.

[0043] One end of the transmission line 11b is coupled to (disposed at) the other end of the fixing member 13. The transmission line 11b is electrically connected between the signal generating unit 10b and the antenna coupling unit 102 to transmit the millimeter wave signal, which is output from the antenna coupling unit 102, to the signal generating unit 10b. In this embodiment, the transmission line 11b is provided on the rear surface of the printed board 2. Furthermore, the transmission line 11b on the rear surface of the printed board 2 is wired to the signal generating unit 10b on the surface of the printed board 2 through a contact hole 12 (a via hole). At the time of bi-directional data transmission, the antenna coupling unit 102 transmits millimeter wave video data between the transmission line 11b connected to the signal generating unit 10b and the fixing member 13 constituting the dielectric transmission path.

[0044] The signal generating unit 10b is connected to the other end of the transmission line 11b. The signal generating unit 10b performs signal processing with respect to the millimeter wave signal received in the antenna coupling unit 102 to generate an output signal. The signal generating unit 10b is connected to an electrical wiring 8b such as a wiring pattern. The electrical wiring 8b is connected to the signal processing unit 6. The signal processing unit 6 performs a process such as expansion with respect to the output signal, which is generated by the signal generating unit 10b, based on a predetermined standard, thereby achieving data of a movie image, a computer image and the like.

[0045] When configuring the in-millimeter-wave dielectric transmission device 100 in this way, it is possible to transmit the electromagnetic wave based on the millimeter wave signal, which is received from one end of the fixing member 13 constituting the dielectric transmission path, to the other end thereof, and a millimeter wave communication process can be performed between the printed board 1 and the printed board 2. In addition, in this embodiment, a case where a downlink data transmission path of the millimeter wave is configured has been described. However, the transmission function of the printed board 1 is provided to the printed board 2 and the reception function of the printed board 2 is provided to the printed board 1, so that data transmission/reception can be performed via the antenna coupling units 101 and 102 and the fixing member 13 constituting the dielectric transmission path.

[0046] According to the downlink data transmission path of the millimeter wave, data transmission using a millimeter wave signal as a medium is performed via the signal processing unit 5 → the signal generating unit 10a → the transmission line 11a → the antenna coupling unit 101 → the fixing member 13 → the antenna coupling unit 102 → the transmission line 11b → the signal generating unit 10b → the signal processing unit 6. According to an uplink data transmission path of the millimeter wave, data transmission using a millimeter wave signal as a medium is performed via the signal processing unit 6 → the signal generating unit 10b → the transmission line 11b → the antenna coupling unit 102 → the fixing member 13 → the antenna coupling unit 101 → the transmission line 11a → the signal generating unit 10a → the signal processing unit 5.

[0047] Fig. 2A is a plan view showing an example of the configuration of the antenna coupling unit 101 and Fig. 2B is a cross-sectional view along a line X1-X2 of Fig. 2A, which shows the example of the configuration of the antenna coupling unit 101. In this embodiment, a microstrip line is applied to the transmission line 11a connected to the antenna coupling unit 101.

[0048] The antenna coupling unit 101 shown in Fig. 2A is provided to the printed board 1 and includes a first waveguide 23a, a through hole 26 having a predetermined shape, and a first signal converting section 36. The waveguide 23a has a cylindrical shape, but the upper portion of the first waveguide 23a has a horseshoe shape (substantially a C shape) in order to avoid a contact with the microstrip line. The waveguide 23a converts the millimeter wave signal, which is electrically transmitted through the transmission line 11a, into an electromagnetic wave and transmits the electromagnetic wave to the dielectric transmission path.

[0049] The through hole 26 is an opening through which the fixing member 13 constituting the dielectric transmission path shown in Fig. 2B is fixed to the printer board 1. In this embodiment, as shown in Fig. 2A, the through hole 26 has the same horseshoe shape as the upper portion of the waveguide 23a. In Figs. 2A and 2B, a part indicated by a double dotted line denotes a dielectric transmission path termination part 30 constituting an example of a first fixing means, which fixes an end portion of the fixing member 13 to the printed board 1 (refer to Fig. 3).

[0050] The printed board 1 includes an insulation layer 1a shown in Fig. 2B. A conductive layer 20 constituting ground is provided on the insulation layer 1a and a conductive layer 25 constituting ground is also provided under the insulation layer 1a. A transmission line layer 21 having insulating properties is stacked on the conductive layer 20 and a line 22 having conductive properties is stacked on the transmission line layer 21. The line 22 is inserted into the waveguide 23a. The transmission line 11a (the microstrip line) includes the transmission line layer 21 and the line 22. For example, in the transmission line layer 21 on the conductive layer 20, the line 22 is patterned with a predetermined line width as shown in Fig. 2A, thereby forming the microstrip line. Hereinafter, the predetermined line width will be referred to as a line width W1 of the line 22. Hereinafter, the thickness of the transmission line layer 21 and the line 22 patterned on the conductive layer 20 will be generically and simply referred to as a film thickness t1.

[0051] An end portion of each of the conductive layers 20 and 25 is short-circuited (electrically conducted) by a conductor part 24 having a cylindrical shape and the conductor part 24 constitutes the waveguide 23a. The waveguide 23a, which has a cylindrical lower portion and a horseshoe-shaped upper portion, is provided by the conductor part 24 having a cylindrical shape for short-circuiting the conductive layers 20 and 25 for ground between the surface and the rear surface of the printed board 1. An inner side of the conductor part 24 is filled with a dielectric substance constituting the printed board 1, so that the dielectric transmission path is formed. Herein, a lower side surface of the waveguide 23a filled with the dielectric substance will be referred to as a waveguide surface I and a diameter of the waveguide 23a filled with the dielectric substance will be referred to as D1.

[0052] The waveguide 23a, for example, is formed as described below. First, an opening having a diameter D1 is opened in one corner of the mother board for forming the printed board 1. Next, a conductive member is provided to the inner wall of the opening to achieve conductivity, and the conductive layer 20 is electrically bonded to the conductive layer 25 by the conductor part 24 obtained through the processing of achieving the conductivity. Then, a dielectric substance constituting the printed board 1 is filled. In addition, the inner side of the conductor part 24 may be a hollow section at the time of waveguide formation.

[0053] The signal converting section 36 includes the line 22 provided to enter (be inserted into) the waveguide 23a. In this embodiment, on the basis of the waveguide 23a, the line 22 inside the waveguide 23a constitutes the signal converting section 36 and the line 22 outside the waveguide 23a constitutes the transmission line 11a. The signal converting section 36 converts a millimeter wave signal into an electromagnetic wave in the waveguide 23a. The signal

converting section 36 has a distance D3 from the center position of the waveguide 23a to an end portion of the line 22 in the waveguide 23a. The line 22 protrudes leftward (on the plane) from the center position of the waveguide 23a.

[0054] In this embodiment, the through hole 26 as shown in Fig. 2A is opened in the printed board 1 around the waveguide 23a, and the end portion of the fixing member 13 is fitted into the through hole 26. According to the antenna coupling unit 101, the electromagnetic wave converted by the signal converting section 36 is transmitted to one end of the fixing member 13 constituting the dielectric transmission path, and the one end of the fixing member 13 is fixed to the printed board 1 by the through hole 26 surrounding the waveguide 23a.

[0055] Fig. 3 is a perspective view showing an example of the shape of the fixing member 13 and the dielectric transmission path termination part 30. In this embodiment, the fixing member 13 has substantially a C shape structure at the front end thereof such that the fixing member 13 can pass through the through hole 26 shown in Fig. 2A. The end portion of the fixing member 13 having passed through the through hole 26 is bonded to the dielectric transmission path termination part 30 shown in Fig. 3, so that the fixing member 13 is fixed to the printed board 1.

[0056] The end portion of the fixing member 13 shown in Fig. 3 has a cylindrical shape, and the fixing member 13 has a cutout part 37 at a part thereof to have substantially a C shape structure at the front end thereof. The cutout part 37 defines a part crossing the waveguide 23a. Herein, the upper surface side of the end portion of the fixing member 13 having the cutout part 37 will be referred to as a dielectric surface III. This embodiment employs a contact surface structure in which the waveguide surface I of the waveguide 23a makes contact with the dielectric surface III of the fixing member 13. An outer peripheral surface of a cylindrical part of the end portion of the fixing member 13 has a male thread structure 31.

[0057] The fixing member 13 is provided at the cylindrical end portion thereof with the dielectric transmission path termination part 30 constituting the first fixing means. The dielectric transmission path termination part 30 has a cover member (a shape of a cap, a hat and the like) with a ceiling, is screw-coupled with the upper end portion of the fixing member 13 to reflect an electromagnetic wave radiated to the waveguide 23a from the transmission line 11a, and fixes the one end of the fixing member 13 to the printed board 1. In this embodiment, when the upper surface of the inner side of the cover member of the dielectric transmission path termination part 30 is defined as a ceiling surface II, the entire surface of the inner wall of the dielectric transmission path termination part 30 is made of a metal or resin plated with a metal, and an electromagnetic wave radiated from the line 22 in the waveguide 23a is reflected by the ceiling surface II.

[0058] In this embodiment, the dielectric transmission path termination part 30 is provided on the inner side surface thereof with a female thread structure 32 corresponding to the male thread structure 31 of the fixing member 13 shown in Fig. 3. The female thread structure 32 of the dielectric transmission path termination part 30 is fitted around the male thread structure 31 of the fixing member 13. For example, the female thread structure 32 of the dielectric transmission path termination part 30 is allowed to circularly move along the male thread structure 31 of the fixing member 13, so that the printed board 1 shown in Fig. 2A is fixed by the fixing member 13.

[0059] In addition, in the case where the distance between the printed board 1 and the ceiling surface II when the dielectric transmission path termination part 30 is fitted around the fixing member 13 is defined as D2, the distance D2 is set to 1/4 of the wavelength λ of a millimeter wave signal on the air and adjusted to enhance an electromagnetic wave, so that the millimeter wave signal can be efficiently converted into an electromagnetic wave.

[0060] The dielectric transmission path termination part 30 for fixing the one end of the fixing member 13 has a first gap part 33 corresponding to the cutout part 37 through which the line 22 shown in Figs. 2A and 2B crosses the waveguide 23a. The gap part 33 is set to have a predetermined width between one end and the other end of the waveguide 23a having a horseshoe shape. Hereinafter, the predetermined width will be referred to as an opening width W2 of the gap part 33. The gap part 33 having the opening width W2 is provided to prevent the conductor part 24 from making contact with the line 22 at the time of bonding the printed board 1 to the fixing member 13. In addition, the antenna coupling unit 102 has the same configuration as the antenna coupling unit 101 (refer to Fig. 5).

[0061] When configuring the in-millimeter-wave dielectric transmission device 100 in this way, it is possible to confine an electromagnetic wave based on a millimeter wave signal in the fixing member 13 constituting the dielectric transmission path. Furthermore, a millimeter wave signal can be converted into an electromagnetic wave at the one end of the fixing member 13 constituting the dielectric transmission path, and an electromagnetic wave can be converted into a millimeter wave signal at the other end of the fixing member 13.

[0062] Next, an example of the circuit configuration of the in-millimeter-wave dielectric transmission device 100 will be described. Fig. 4 is a block diagram showing an example of the configuration of the in-millimeter-wave dielectric transmission device 100. The in-millimeter-wave dielectric transmission device 100 shown in Fig. 4 constitutes an example of the downlink data transmission path of the millimeter wave, and is a millimeter wave video data transmission device which can be applied to an image processing device and the like for transmitting a millimeter wave signal with a frequency of 30 GHz to 300 GHz at a high speed.

[0063] The in-millimeter-wave dielectric transmission device 100 includes the printed board 1 on which a signal input terminal 201, the signal generating unit 10a and a coupling circuit 205 are mounted, the fixing member 13 bonded to

the printed board 1, and the printed board 2 on which a coupling circuit 207, the signal generating unit 10b and a signal output terminal 211 are mounted. The coupling circuit 205 includes the transmission line 11a and the antenna coupling unit 101 shown in Figs. 1, 2A, 2B and 3, and the coupling circuit 207 includes the transmission line 11b and the antenna coupling unit 102 shown in the same drawings. The signal generating unit 10a and the signal generating unit 10b include a CMOS-IC device.

[0064] The signal generating unit 10a connected to the signal input terminal 201, for example, includes a modulation circuit 202, a first frequency conversion circuit 203 and an amplifier 204 in order to generate a millimeter wave signal S by performing signal processing with respect to an input signal Sin. The modulation circuit 202 is connected to the signal input terminal 201 to modulate the input signal Sin. For example, a phase modulation circuit is used as the modulation circuit 202.

[0065] The frequency conversion circuit 203 is connected to the modulation circuit 202 to generate the millimeter wave signal S by frequency-converting the input signal Sin modulated by the modulation circuit 202. Herein, the millimeter wave signal S is a signal having a frequency in the range of 30 GHz to 300 GHz. The amplifier 204 is connected to the frequency conversion circuit 203 to amplify the frequency-converted millimeter wave signal S.

[0066] The coupling circuit 205 including the transmission line 11a and the antenna coupling unit 101 is connected to the amplifier 204 to transmit the millimeter wave signal S generated by the signal generating unit 10a to the one end of the fixing member 13 having a predetermined dielectric constant ε. The waveguide 23a described in Figs. 1, 2A, 2B and 3 is provided to the coupling circuit 205 so as to be coupled to the fixing member 13 having the dielectric constant ε. If the coupling circuit 205 has a fractional bandwidth (= a signal band/an operating center frequency) of about 10% to about 20%, the coupling circuit 205 may be easily formed using a resonance structure and the like. In this embodiment, an electromagnetic wave S' of a millimeter wave propagates through the fixing member 13 having the dielectric constant ε and a loss. Since the fixing member 13 has a large loss, reflection is attenuated.

[0067] The coupling circuit 207 constituting an example of the antenna coupling unit 102 is coupled to the fixing member 13 to convert the electromagnetic wave S' received from the other end of the fixing member 13 into the millimeter wave signal S. The coupling circuit 207 is provided with a waveguide 23b (not shown). The waveguide 23b has the same structure of the waveguide 23a as described with reference to Figs. 1, 2A, 2B and 3, and is coupled to the other end of the fixing member 13 having the dielectric constant ε. In addition to the waveguide 23a or 23b, the coupling circuit 207 may be formed of an antenna member having a predetermined length, for example, about 600 μm based on the wavelength λ of the millimeter wave signal S. As the antenna member, a probe antenna (a dipole antenna and the like), a loop antenna, or a small aperture coupling element (a slot antenna and the like) is used.

[0068] The signal generating unit 10b is connected to the coupling circuit 207. In order to generate an output signal Sout by performing signal processing with respect to the millimeter wave signal S received in the coupling circuit 207, the signal generating unit 10b, for example, includes an amplifier 208, a second frequency conversion circuit 209 and a demodulation circuit 210. The amplifier 208 is connected to the coupling circuit 207 to amplify the received millimeter wave signal S.

[0069] The frequency conversion circuit 209 is connected to the amplifier 208 to frequency-convert the amplified millimeter wave signal S and output a frequency-converted output signal Sout. The demodulation circuit 210 is connected to the frequency conversion circuit 209 to demodulate the frequency-converted output signal Sout.

[0070] The above-described method of frequency-converting the input signal Sin and performing data transmission is generally used for broadcasting or wireless communication. In the above use, a relatively complicated transmitter, receiver and the like are used to cope with problems such as (1) to what extent communication is possible (a problem of S/N with respect to thermal noise), (2) how to cope with reflection and a multipath, and (3) how to suppress disturbance and interference with other channels.

[0071] Since the signal generating unit 10a and the signal generating unit 10b used in the first embodiment are used in a millimeter band of a frequency higher than a frequency used in a complicated transmitter, receiver and the like generally used in broadcasting or wireless communication, and have a short wavelength X, they are advantageous in terms of the reuse of a frequency and suitable for performing communication among many devices in a neighborhood. In this embodiment, an example of the downlink data transmission path of the millimeter wave has been described. However, when configuring a bi-directional data transmission path, an uplink data transmission path of the millimeter wave is configured by providing a reception system to a transmission system of the in-millimeter-wave dielectric transmission device 100 shown in Fig. 4 and providing a transmission system to the reception system, so that the transmission system and the reception system may operate in a time division manner.

[0072] Next, examples of forming the in-millimeter-wave dielectric transmission device 100 will be described with reference to Figs. 5 to 7. Figs. 5 to 7 are process diagrams showing the examples (1 to 3) of forming the in-millimeter-wave dielectric transmission device 100. They are based on the case of manufacturing the in-millimeter-wave dielectric transmission device 100 according to the first embodiment.

[0073] First, in Fig. 5, a board 1' is prepared in order to form the printed board 1 that processes a millimeter wave signal. For example, as the board 1', a double-sided copper foil board having the insulation layer 1a and the conductive

layers 20 and 25 as shown in Fig. 2B may be used. The size of the board 1', for example, is defined as a length L, a width W and a thickness t (refer to Fig. 1).

[0074] The electrical wiring 8a, the transmission line 11a, the waveguide 23a, the four through holes 26 and the like are formed on and in the board 1'. The transmission line 11 a and the waveguide 23a constitute the antenna coupling unit 101. The conductive layers 20 and 25 formed on both surfaces of the insulation layer 1a of the board 1' are used as a ground pattern. Next, the waveguide 23a is formed at one corner of the board 1'. In this embodiment, the waveguide 23a may not be formed at the other three corners. In other embodiments, the waveguide 23a may also be formed at the other three corners.

[0075] In relation to the waveguide 23a, an opening having a diameter D1 is opened in one corner of the board 1'. Then, a conductive member is provided to the inner wall of the opening to achieve conductivity, and the conductive layer 20 is electrically bonded to the conductive layer 25 by the conductor part 24 obtained through the process of achieving the conductivity. The conductor part 24 is formed as follows. For example, the opening having the diameter D1 is formed in order to connect the conductive layers 20 and 25 to each other, which achieve ground (earth) of the surface and rear surface of the printed board 1. The opening is formed along the circumference constituting the waveguide 23a. Thereafter, the opening is made conductive, so that a contact hole (a via hole) for a conductor part is formed. At the time of forming the waveguide, the contact hole has a hollow section. Then, a dielectric substance constituting the printed board 1 is filled therein. In addition, the inner side of the conductor part 24 may have a hollow section at the time of forming the waveguide.

[0076] After forming the waveguide 23a, an insulating film having a predetermined dielectric constant is formed on the entire surface of the conductive layer 20, thereby forming the transmission line layer 21 having a thickness t1. An insulating film is filled to be buried in the waveguide 23a. As the insulating film, the dielectric substance constituting the printed board 1 is used, and the dielectric substance is filled in the conductor part 24 to form a dielectric transmission path. The lower side surface of the waveguide 23a filled with the dielectric substance serves as the waveguide surface I (refer to Fig. 2B).

[0077] Thereafter, a conductive film is formed on the entire surface of the insulating film and is subject to patterning, thereby, for example, forming 10 electrical wirings 8a and one transmission line 11a having a line width W1 and serving as a microstrip line. The transmission line 11a is obtained by forming the line 22 having a line width W1 on the transmission line layer 21. At this time, the transmission line layer 21 is disposed such that the front end of the transmission line layer 21 is inserted into the waveguide 23a, and the transmission line 11a (the line 22) is patterned such that it is lengthened by the distance D3 from the center position of the waveguide 23a. By the patterning, it is possible to form the signal converting section 36 including the line 22 disposed to enter (be inserted into) the waveguide 23a. In the waveguide 23a, the signal converting section 36 is configured to convert a millimeter wave signal into an electromagnetic wave.

[0078] Then, one through hole 26 having a horseshoe shape and three through holes 26' having a horseshoe shape are opened in four corners of the board 1'. For example, the through holes 26 and 26' are opened using a press machine provided with a machining cutter having substantially a C shape at the front end thereof. The through hole 26 is used for the fitting of the fixing member 13 and the through holes 26' are used for the fitting of the three fixing members 3.

[0079] In addition to the transmission line 11a and the antenna coupling unit 101, the signal processing unit 5 and the signal generating unit 10a are mounted on the board 1'. As the signal processing unit 5, an IC device for signal processing such as compression of data of a movie image, a computer image and the like is used. As the signal generating unit 10a, an IC device for signal generation is used to generate a millimeter wave signal by performing signal processing with respect to an input signal. In this embodiment, the signal processing unit 5 and the signal generating unit 10a are bonded at a predetermined position on the board 1', so that the signal processing unit 5 is connected to the signal generating unit 10a by the 10 electrical wirings 8a, thereby achieving the printed board 1 that converts data of a movie image, a computer image and the like into a millimeter wave signal.

[0080] Next, in Fig. 6, a board 2' is prepared in order to form the printed board 2 that receives the millimeter wave signal from the printed board 1 and performs signal processing with respect to the millimeter wave signal. For example, as the board 2', a double-sided copper foil board having the insulation layer 1a and the conductive layers 20 and 25 as shown in Fig. 2B may be used. The size of the board 2' is also defined as a length L, a width W and a thickness t (refer to Fig. 1).

[0081] The electrical wiring 8b, the transmission lines 11b, the waveguide 23b, the four through holes 26 and the like are formed on and in the board 2'. The transmission line 11b and the waveguide 23b constitute the antenna coupling unit 101. The conductive layers 20 and 25 formed on both surfaces of the insulation layer 1b of the board 2' are used as a ground pattern. Next, the waveguide 23b is formed at one corner of the board 2'. In this embodiment, the waveguide 23b may not be formed at the other three corners. When forming the waveguide 23b, a contact hole 12 is formed to obtain a connection of the transmission lines 11b on the front and the back of the board 2'.

[0082] In relation to the waveguide 23b, an opening having a diameter D1 is opened in one corner of the board 2'. Then, a conductive member is provided to the inner wall of the opening to achieve conductivity, and the conductive layer 20 is electrically bonded to the conductive layer 25 by the conductor part 24 obtained through the process of achieving

the conductivity. The conductor part 24 is formed in the same manner as the printed board 1.

[0083] In relation to the contact hole 12, an opening having a predetermined diameter is opened in a predetermined position of the board 2'. Then, a conductive member is provided to the inner wall of the opening to achieve conductivity, and it is possible to obtain a connection of the transmission lines 11b on the front and the back of the board 2' through the contact hole 12 obtained through the process of achieving the conductivity.

[0084] After forming the waveguide 23b and the contact hole 12, an insulating film having a predetermined dielectric constant is formed on the entire surface of the conductive layer 20, except for the formation position of the contact hole 12, thereby forming the transmission line layer 21 having a thickness t1. An insulating film is filled to be buried in the waveguide 23b. As the insulating film, the dielectric substance constituting the printed board 2 is used, and the dielectric substance is filled in the conductor part 24 to form a dielectric transmission path. The lower side surface of the waveguide 23b filled with the dielectric substance serves as the waveguide surface I (refer to Fig. 2B).

[0085] Thereafter, a conductive film is formed on the entire surface of the insulating film and is subject to patterning, thereby, for example, forming 10 electrical wirings 8b and one transmission line 11b having a line width W1 and serving as a microstrip line of the surface side of the printed board 2. The transmission line 11b is obtained by forming the line 22 having a line width W1 on the transmission line layer 21. The transmission line 11b on the front is connected to the contact hole 12 formed in the surface of the board 2'.

[0086] In addition, an insulating film having a predetermined dielectric constant is formed on the entire surface of the conductive layer 25, except for the formation position of the contact hole 12 of the rear surface, thereby forming the transmission line layer 21 having a thickness t1 on the rear surface side of the printed board 2. As the insulating film, the dielectric substance constituting the printed board 2 is used. At this time, the transmission line 11b on the back is also obtained by forming the line 22 having a line width W1 on the transmission line layer 21. The transmission line 11b on the back is connected to the contact hole 12 formed in the rear surface of the board 2'. Thus, the transmission line 11b on the front reaches the rear surface of the board 2' from the surface of the board 2' via the contact hole 12 and is connected to the transmission line 11b on the back.

[0087] Furthermore, the transmission line 11b on the back is disposed such that the front end of the transmission line 11b is inserted into the waveguide 23b, and the transmission line 11b (the line 22) is patterned such that it is lengthened by the distance D3 from the center position of the waveguide 23b. By the patterning, it is possible to form the signal converting section 36 including the line 22 disposed to enter (be inserted into) the waveguide 23b. In the waveguide 23b, the signal converting section 36 is configured to convert an electromagnetic wave into a millimeter wave signal.

[0088] Then, one through hole 26 having a horseshoe shape and three through holes 26' having a horseshoe shape are opened in the four corners of the board 2', in the same manner as the first printed board 1. The through hole 26 is used for the fitting of the fixing member 13 and the through holes 26' are used for the fitting of the three fixing members 3. In addition to the transmission line 11b and the antenna coupling unit 101, the signal processing unit 6 and the signal generating unit 10b are mounted on the board 2'.

[0089] As the signal processing unit 6, an IC device for signal processing such as expansion of data of a movie image, a computer image and the like is used. As the signal generating unit 10b, an IC device for signal generation is used to generate an output signal by performing signal processing with respect to a millimeter wave signal. In this embodiment, the signal processing unit 6 and the signal generating unit 10b are bonded at a predetermined position on the board 2', so that the signal processing unit 6 is connected to the signal generating unit 10b by the 10 electrical wirings 8b, thereby achieving the printed board 2 that converts the millimeter wave signal transmitted from the printed board 1 into data of a movie image, a computer image and the like.

[0090] After preparing the above-described printed board 1 and printed board 2, the fixing member 13 having a predetermined dielectric constant is provided between the printed board 1 and the printed board 2 to form the dielectric transmission path while supporting the printed board 1 and the printed board 2 by the fixing member 13. As the fixing member 3 and the fixing member 13, for example, a resultant obtained by injection-molding resin having a predetermined dielectric constant is used such that the cutout part 37 is formed at both ends of the fixing member 13.

[0091] As dielectric transmission path termination parts 30 and fixing member termination stop parts 30', for example, a resultant obtained by performing metal plating with respect to the resultant obtained by injection-molding the resin having a predetermined dielectric constant is used, which has a shape described in Fig. 3. Of course, it may also be possible to use a resultant obtained by processing a metal bar into a cover-like shape and then performing female thread processing with respect to the inner surface side of the metal bar.

[0092] In this embodiment, the three fixing members 3 and the one fixing member 13 on the printed board 2 are fitted into three fixing member termination stop parts 30' and one dielectric transmission path termination part 30 below the printed board 2 and three fixing member termination stop parts 30' and one dielectric transmission path termination part 30 on the printed board 1, respectively.

[0093] For example, the three fixing members 3 are fitted into the three through holes 26 formed in the printed board 2 from the surface side and are fixed at the rear surface side using the three fixing member termination stop parts 30', respectively. In addition, one fixing member 13 is fitted into the through hole 26 constituting one antenna coupling unit

102 of the printed board 2 from the surface side and are fixed at the rear surface side using the one dielectric transmission path termination part 30. Consequently, the four fixing members 3 and 13 can be fitted with the printed board 2.

[0094] Furthermore, the three fixing members 3 on the printed board 2 are fitted into the three through holes 26' formed in the printed board 1 from the rear surface side and are fixed at the surface side using the three fixing member termination stop parts 30', respectively. In addition, the one fixing member 13 is fitted into the through hole 26 constituting the one antenna coupling unit 101 of the printed board 1 from the rear surface side and is fixed at the surface side using the one dielectric transmission path termination part 30. Consequently, the four fixing members 3 and 13 on the printed board 2 can be fitted with the printed board 1, thereby completing the fabrication of the in-millimeter-wave dielectric transmission device 100.

[0095] As described above, when forming the in-millimeter-wave dielectric transmission device 100 such that the printed board 1 is supported by the three fixing members 3 and the one fixing member 13 on the printed board 2, it is possible to fabricate the in-millimeter-wave dielectric transmission device 100 in which the fixing member 13 constitutes the dielectric transmission path and an electromagnetic wave based on a millimeter wave received from the one end of the fixing member 13 can be transmitted to the other end of the fixing member 13.

[0096] Next, a case where a fixing member 13 made of a general plastic material is applied to the in-millimeter-wave dielectric transmission device 100 will be described based on a result obtained by simulating a pass characteristic (size of loss) and a reflection characteristic of the fixing member 13 using the CST MW-STUDIO. Fig. 8 is a perspective view showing an example of a simulation model of the in-millimeter-wave dielectric transmission device 100. As the fixing member 13, a general plastic material is assumed. However, the plastic material contains glass epoxy-based, acryl-based and polyethylene-based resin materials.

[0097] In addition, except for the conductive layer 20 and the transmission line layer 21, the insulation layer 1a and the conductive layers 20 and 25 of the printed board 1 are excluded from the simulation model because they do not significantly influence the characteristics. The fixing member 13, the printed board 2 and the dielectric transmission path termination part 30 are transparently displayed (skeleton view) for the purpose of convenience.

[0098] According to the example of the simulation model of the in-millimeter-wave dielectric transmission device 100 shown in Fig. 8, the antenna coupling unit 101 and the antenna coupling unit 102 are configured to be connected to each other through the fixing member 13. As the antenna coupling unit 101, a model having the waveguide 23a and the signal converting section 36 shown in Figs. 1 and 3 is used. The signal converting section 36 converts a millimeter wave signal into an electromagnetic wave and radiates the electromagnetic wave in the fixing member 13. As the waveguide 23a, a model having a horseshoe shape at the inner side of the through hole 26 opened in the printed board 2 is used.

[0099] The fixing member 13 is modeled such that the fixing member 13 is fitted into the through hole 26 opened in the outer peripheral portion of the waveguide 23a, and the printed board 1 and the one end of the fixing member 13 are fixed via the dielectric transmission path termination part 30. As the dielectric transmission path termination part 30 fixing the one end of the fixing member 13, a model having the gap part 33 at a position at which the transmission line 11a crosses the waveguide 23a is used. When providing the gap part 33 as described above, it is possible to avoid a contact between the one end of the fixing member 13 constituting the dielectric transmission path and the transmission line 11a and a contact between the other end of the fixing member 13 and the transmission line 11a.

[0100] The antenna coupling unit 101 is simulated such that the antenna coupling unit 101 converts a millimeter wave signal into an electromagnetic wave at the one end of the fixing member 13 constituting the dielectric transmission path and radiates the electromagnetic wave to the fixing member 13. For example, the antenna coupling unit 101 has the dielectric transmission path termination part 30, and is configured to reflect the electromagnetic wave, which has been converted into the millimeter wave signal by the signal converting section 36 and is not supplied to the one end of the fixing member 13, and to fix the one end of the fixing member 13 to the printed board 1.

[0101] An object having the second waveguide 23b and the second signal converting section 36 is applied to the antenna coupling unit 102. The second signal converting section 36 of the antenna coupling unit 102 converts the electromagnetic wave having been propagated through the fixing member 13 into a millimeter wave signal. The waveguide 23b is formed to have a horseshoe shape at the inner side of the through hole 26 opened in the printed board 2 (refer to Figs. 2A and 2B).

[0102] The antenna coupling unit 102 is a simulation model which is configured to convert the electromagnetic wave having been propagated to the other end of the fixing member 13 constituting the dielectric transmission path into the millimeter wave signal by the signal converting section 36, transmit the millimeter wave signal to the transmission line 11b via the waveguide 23b, and fix the printed board 2 and the other end of the fixing member 13 by the through hole 26 forming the waveguide 23b.

[0103] For example, the antenna coupling unit 102 has the dielectric transmission path termination part 30 constituting an example of a second fixing means, and is configured to reflect the electromagnetic wave, which has been propagated to the other end of the fixing member 13 and has not been converted into the millimeter wave signal by the signal converting section 36, and fix the other end of the fixing member 13 to the printed board 2.

[0104] The dielectric transmission path termination part 30 fixing the other end of the fixing member 13 has a second

gap part (not shown) at a position at which the transmission line 11 b crosses the waveguide 23b (refer to Fig. 2B). When providing the gap part as described above, it is possible to avoid a contact between the one end of the fixing member 13 constituting the dielectric transmission path and the transmission line 11b and a contact between the other end of the fixing member 13 and the transmission line 11b. In this way, the simulation model of the in-millimeter-wave dielectric transmission device 100 is configured.

[0105] Next, parameters provided to the simulation model of the in-millimeter-wave dielectric transmission device 100 shown in Fig. 8 will be described. At the time of the simulation, parameters are as follows. The thickness (hereinafter, simply referred to as a thickness t of a board) of the printed board 1 and the printed board 2 is 1.0 mm. The diameter D1 of the waveguide 23a is 2.5 mm. The thickness t1 of the transmission line layer 21 is 0.1 mm. The distance D2 between the printed board 1 and the ceiling surface II is 1.25 mm. The opening width W2 of the gap part 33 is 0.8 mm. The line width W1 of the line 22 is 0.2 mm. The distance D3 from the center position of the waveguide 23a to the end portion of the line 22 is 0.9 mm. When the separation distance between the printed board 1 and the printed board 2 is defined as an inter-board distance D4, the inter-board distance D4 is 20 mm.

[0106] When the diameter of the fixing member 13 is defined as D5, the diameter D5 is 4.0 mm. The specific dielectric constants εr of the printed board 1 and the printed board 2 are 3.5. The dielectric loss tangents tan δ of the printed board 1 and the printed board 2 are 0.005. δ denotes a loss angle of a dielectric substance. The specific dielectric constant εr of the fixing member 13 is 3.0. The dielectric loss tangent tan δ of the fixing member 13 is 0.003. Table 1 shows the values of the parameters at the time of the simulation

[0107]

Table 1

Parameter	Value	Unit
Thickness t of board	1.0	mm
Diameter D 1 of waveguide	2.5	mm
Thickness t1 of transmission line layer	0.1	mm
Distance D2 between board and ceiling surface II	1.25	mm
Opening width W2 of gap part 33	0.8	mm
Line width W1 of line 22	0.2	mm
Distance D3 from center position of waveguide to end portion of line 22	0.9	mm
Inter-board distance D4	20	mm
Diameter D5 of fixing member 13	4.0	mm
Specific dielectric constant of board	3.5	none
Dielectric loss tangent tan δ of board (1 GHz)	0.005	none
Specific dielectric constant of fixing member 13	3.0	none
Dielectric loss tangent tan δ of fixing member 13 (1 GHz)	0.003	none

[0108] Fig. 9 is a graph showing an example of a simulation characteristic of the in-millimeter-wave dielectric transmission device 100. The example of the simulation characteristics of the in-millimeter-wave dielectric transmission device 100 shown in Fig. 9 shows an example of a pass characteristic and an example of a reflection characteristic between ports 301 which are provided on the line 22 of the printed board 1 and the line 22 of the printed board 2 shown in Fig. 8.

[0109] In Fig. 9, a vertical axis denotes a pass characteristic S (2, 1) dB and a reflection characteristic S (1, 1) dB. A horizontal axis denotes a carrier frequency (GHz) and a scale is in units of 5 GHz. In Fig. 9, Ia denotes the example of the pass characteristic and is a frequency characteristic figure showing the example of the pass characteristic and the example of the reflection characteristic of the fixing member 13 when the transmission lines 11a an 11b are formed of a microstrip line, the antenna coupling unit 101 is formed of the waveguide 23a, and the antenna coupling unit 102 is formed of the waveguide 23b.

[0110] The pass characteristic S (2, 1) dB of the fixing member 13 is a pass characteristic of the millimeter wave signal S transmitted from the transmission line 11a of the printed board 1 having the dielectric loss tangent tan δ of 0.005 to the transmission line 11b of the printed board 2 having the same dielectric loss tangent tan δ of 0.005 through the fixing member 13 having the dielectric loss tangent tan δ of 0.003. The pass characteristic S (2, 1) dB corresponds to a case where the carrier frequency is in the range of 50 GHz to 70 GHz and increased in units of 1 GHz. According to the

simulation result, video data based on the millimeter wave signal S has passing loss of about 7.4 dB when the carrier frequency is 58.7 GHz between the ports 301.

[0111] Furthermore, in Fig. 9, IIa denotes the example of the reflection characteristic of the fixing member 13 and the reflection characteristic S (1, 1) dB of the fixing member 13 is a reflection characteristic of the millimeter wave signal S transmitted from the transmission line 11 a of the printed board 1 having the dielectric loss tangent tan δ of 0.005 to the transmission line 11b of the printed board 2 having the same dielectric loss tangent tan δ of 0.005 through the fixing member 13 having the dielectric loss tangent tan δ of 0.003.

[0112] The reflection characteristic S (1, 1) dB corresponds to a case where the carrier frequency is in the range of 50 GHz to 70 GHz and increased in units of 1 GHz. According to the simulation result, reflection loss is equal to or less than -15 dB. Furthermore, in the range in which the carrier frequency is 55.0 GHz to 62.5 GHz, reflection loss is equal to or less than -10 dB.

[0113] In the fixing member 13 having large loss as described above, since transmission loss is increased and a reflected wave is attenuated with an increase in the carrier frequency, it is also possible to reduce adverse effect of a standing wave due to the reflected wave. In this embodiment, the frequency conversion circuits 203 and 209 frequency-convert the input signal Sin into the millimeter wave signal S, so that the ratio of (a signal band)/(a center frequency) can be reduced and thus the signal generating unit 10a for transmitting a millimeter wave signal and the signal generating unit 10b for receiving a millimeter wave signal can also be easily configured.

[0114] According to the in-millimeter-wave dielectric transmission device 100 and the manufacturing method thereof in accordance with the first embodiment as described above, the fixing member 13 having a predetermined dielectric constant is provided between the printed board 1 including the signal generating unit 10a and the antenna coupling unit 101 to process the millimeter wave signal S and the printed board 2 including the antenna coupling unit 102 and the signal generating unit 10b to perform signal processing with respect to the received millimeter wave signal S, constitutes a dielectric transmission path, and supports the printed board 1 and the printed board 2 together with the other three fixing members 3.

[0115] With such a structure, the electromagnetic wave S' based on the millimeter wave signal S radiated from the one end of the fixing member 13 constituting the dielectric transmission path can be received at the other end of the fixing member 13. Consequently, since the original support structure of the fixing member 13 is used as a signal transmission path, it is possible to remove a communication cable, a connector and the like for connecting the printed board 1 to the printed board 2 according to the related art. In addition, support and high speed data transmission between the printed board 1 and the printed board 2 are performed by the fixing member 13 which is the same support member. Since the high speed data transmission in the fixing member 13 is performed by a millimeter wave (an electromagnetic wave), the fixing member 13 constituting the dielectric transmission path is finished with a single material. Thus, processing demanding accuracy as with an optical waveguide is not necessary.

[0116] Moreover, at the time of the fixing between the printed board 1 and the fixing member 13 in the antenna coupling unit 101, strictness of position adjustment for stably performing data transmission is not necessary, unlike the case of employing an optical transmission method. According to the in-millimeter-wave dielectric transmission device 100, it is possible to perform support and high speed data transmission between the printed boards 1 and 2 with a simple and inexpensive configuration, resulting in the improvement of reliability of data transmission against vibration and deviation.

<Second embodiment>

[0117] Fig. 10 is a perspective view showing an example of the configuration of an in-millimeter-wave dielectric transmission device 200 as the second embodiment. In this embodiment, a millimeter wave signal S is transmitted in parallel through fixing members 131 to 134 provided at four corners (plural) of printed boards 1 and 2 and the like (bus configuration).

[0118] The in-millimeter-wave dielectric transmission device 200 shown in Fig. 10 can be applied to a millimeter wave video data transmission device, a millimeter wave video data transmission system and the like, which convert data of a movie image, a computer image and the like into a plurality of millimeter wave signals S and transmit the millimeter wave signals at a high speed, and have a carrier frequency of 30 GHz to 300 GHz for carrying the millimeter wave signals.

[0119] In this embodiment, four fixing members 13 constituting the dielectric transmission path as described in the first embodiment are provided between the printed board 1 and the printed board 2. Hereinafter, the four fixing members will be referred to as fixing members 131 to 134. Each of the fixing members 131 to 134 supports the printed board 1 and the printed board 2 and transmits the millimeter wave signals S. The fixing members 131 to 134 are provided between the printed board 1 and the printed board 2 while having a predetermined dielectric constant.

[0120] As the fixing members 131 to 134, a dielectric material at least including a glass epoxy-based, acryl-based, polyethylene-based resin is used. When configuring the in-millimeter-wave dielectric transmission device 200 in this way, it is possible to increase transmission capacity of video data based on the millimeter wave signals S four times as compared with the first embodiment.

[0121] The printed board 1 includes a signal processing unit 5, a signal generating unit 10c, antenna coupling units 101, 103, 105 and 107 of four systems, and four transmission lines 111, 113, 115 and 117, which are mounted thereon. Similarly to the first embodiment, the signal processing unit 5 performs a process such as compression with respect to data of a movie image, a computer image and the like based on a predetermined standard to output an electrical signal (hereinafter, referred to as an input signal).

[0122] The signal processing unit 5 is connected to an electrical wiring 8a such as a wiring pattern. The electrical wiring 8a is connected to the signal generating unit 10c. Unlike the first embodiment, the signal generating unit 10c performs signal processing with respect to the input signal to generate a plurality of (in this embodiment, four systems) millimeter wave signals. The signal generating unit 10c, for example, is configured by providing the signal generating unit 10a, which is described in the first embodiment, in a row by four systems.

[0123] In this embodiment, the four transmission lines 111, 113, 115 and 117 are drawn out from the signal generating unit 10c. A scheme of a strip line, a microstrip line, a coplanar line, a slot line and the like is applied to the transmission lines 111, 113, 115 and 117 on the printed board 1.

[0124] The transmission line 111 is provided at a first corner part (corner) of the printed board 1. The transmission line 111 is bonded between the signal generating unit 10a constituting the first system at the signal generating unit 10c and the antenna coupling unit 101. The fixing member 131 is connected to the antenna coupling unit 101. The antenna coupling unit 101 couples a millimeter wave signal, which is transmitted from the signal generating unit 10c via the transmission line 111, to one end of the fixing member 131. In this embodiment also, the antenna coupling unit 101 converts the millimeter wave signal into an electromagnetic wave and radiates the electromagnetic wave into the fixing member 131 constituting a dielectric transmission path.

[0125] The fixing member 131 not only constitutes a dielectric transmission path but also supports the printed board 1 and the printed board 2 together with the other three fixing members 132 to 134. The support function includes a case where the printed board 2 holds up and supports the printed board 1 and a case where the printed board 1 is suspended and supports the printed board 2, in the same manner as that in the first embodiment.

[0126] Furthermore, the transmission line 113 is provided at a second corner part of the printed board 1. The transmission line 113 is bonded to the antenna coupling unit 103 of the second system. The transmission line 113 is bonded between the signal generating unit 10a constituting the second system at the signal generating unit 10c and the antenna coupling unit 103. The fixing member 132 is connected to the antenna coupling unit 103. The antenna coupling unit 103 couples a millimeter wave signal, which is transmitted from the signal generating unit 10c via the transmission line 113, to one end of the fixing member 132.

[0127] In this embodiment also, the antenna coupling unit 103 converts the millimeter wave signal into an electromagnetic wave and radiates the electromagnetic wave into the fixing member 132 constituting a dielectric transmission path. The fixing member 132 not only constitutes a dielectric transmission path but also supports the printed board 1 and the printed board 2 together with the other three fixing members 131, 133 and 134.

[0128] In addition, the transmission line 115 is provided at a third corner part of the printed board 1. The transmission line 115 is bonded to the antenna coupling unit 105 of the third system. The transmission line 115 is bonded between the signal generating unit 10a constituting the third system at the signal generating unit 10c and the antenna coupling unit 105. The fixing member 133 is connected to the antenna coupling unit 105. The antenna coupling unit 105 couples a millimeter wave signal, which is transmitted from the signal generating unit 10c via the transmission line 115, to one end of the fixing member 133.

[0129] In this embodiment also, the antenna coupling unit 105 converts the millimeter wave signal into an electromagnetic wave and radiates the electromagnetic wave into the fixing member 133 constituting a dielectric transmission path. The fixing member 133 not only constitutes a dielectric transmission path but also supports the printed board 1 and the printed board 2 together with the other three fixing members 131, 132 and 134.

[0130] Moreover, the transmission line 117 is provided at a fourth corner part of the printed board 1. The transmission line 117 is bonded to the antenna coupling unit 107 of the fourth system. The transmission line 117 is bonded between the signal generating unit 10a constituting the fourth system at the signal generating unit 10c and the antenna coupling unit 107. The fixing member 134 is connected to the antenna coupling unit 107. The antenna coupling unit 107 couples a millimeter wave signal, which is transmitted from the signal generating unit 10c via the transmission line 117, to one end of the fixing member 134.

[0131] In this embodiment also, the antenna coupling unit 107 converts the millimeter wave signal into an electromagnetic wave and radiates the electromagnetic wave into the fixing member 134 constituting a dielectric transmission path. The fixing member 134 not only constitutes a dielectric transmission path but also supports the printed board 1 and the printed board 2 together with the other three fixing members 131 to 133.

[0132] Meanwhile, the printed board 2, which receives the millimeter wave signals of the four systems and performs signal processing with respect to the millimeter wave signals, includes antenna coupling units 102, 104, 106 and 108 of four systems, four transmission lines 112, 114, 116 and 118, a signal generating unit 10d, and a signal processing unit 6, which are mounted thereon. In this embodiment, the four transmission lines 112, 114, 116 and 118 drawn out from

the antenna coupling units 102, 104, 106 and 108 of the four systems are connected to the signal generating unit 10d. A scheme of a strip line, a microstrip line, a coplanar line, a slot line and the like is applied to the transmission lines 112, 114, 116 and 118 on the front and the back of the printed board 2.

[0133] The other end of the above-described fixing member 131 is bonded to the antenna coupling unit 102 provided at the first corner part of the printed board 2. The antenna coupling unit 102 receives an electromagnetic wave from the fixing member 131 and converts the electromagnetic wave into a millimeter wave signal. The millimeter wave signal is output to the signal generating unit 10d through the transmission line 112. The other end of the fixing member 132 is bonded to the antenna coupling unit 104 provided at the second corner part of the printed board 2. The antenna coupling unit 104 receives an electromagnetic wave from the fixing member 132 and converts the electromagnetic wave into a millimeter wave signal. The millimeter wave signal is output to the signal generating unit 10d through the transmission line 114.

[0134] Furthermore, the other end of the fixing member 133 is bonded to the antenna coupling unit 106 provided at the third corner part of the printed board 2. The antenna coupling unit 106 receives an electromagnetic wave from the fixing member 133 and converts the electromagnetic wave into a millimeter wave signal. The millimeter wave signal is output to the signal generating unit 10d through the transmission line 116. The other end of the fixing member 134 is bonded to the antenna coupling unit 108 provided at the fourth corner part of the printed board 2. The antenna coupling unit 108 receives an electromagnetic wave from the fixing member 134 and converts the electromagnetic wave into a millimeter wave signal. The millimeter wave signal is output to the signal generating unit 10d through the transmission line 118.

[0135] Unlike the first embodiment, the signal generating unit 10d receives the respective millimeter wave signals, which are received in the antenna coupling units 102, 104, 106 and 108 of the four systems, through the four transmission lines 112, 114, 116 and 118, and generates an output signal by performing signal processing with respect to the respective millimeter wave signals which are input via the transmission lines 112, 114, 116 and 118. The signal generating unit 10d, for example, is configured by providing the signal generating unit 10b, which is described in the first embodiment, in a row by four systems.

[0136] The signal processing unit 6 is connected to the signal generating unit 10d through an electrical wiring 8b such as a wiring pattern. The signal processing unit 6 performs a process such as expansion with respect to the output signal, which is generated by the signal generating unit 10d, based on a predetermined standard, thereby achieving data of a movie image, a computer image and the like. In this way, the in-millimeter-wave dielectric transmission device 200 is configured. In addition, since an example of forming the in-millimeter-wave dielectric transmission device 200 may employ the examples (1 to 3) of forming the in-millimeter-wave dielectric transmission device 100 shown in Figs. 5 to 7 by replacing reference numerals, detailed description thereof will be omitted.

[0137] As described above, according to the in-millimeter-wave dielectric transmission device 200 as the second embodiment, the signal transmission lines of the four systems including the fixing members 131 to 134 are formed at the four corners of each of the printed board 1 and the printed board 2. According to the above-described downlink data transmission path of the millimeter wave, first data transmission using a millimeter wave signal as a medium is performed via the signal processing unit 5 of the printed board 1 → the signal generating unit 10c → the transmission line 111 → the antenna coupling unit 101 → the fixing member 131 → the antenna coupling unit 102 → the transmission line 112 → the signal generating unit 10d → the signal processing unit 6.

[0138] Similarly, second data transmission using a millimeter wave signal as a medium is performed via the signal processing unit 5 of the printed board 1 → the signal generating unit 10c → the transmission line 113 → the antenna coupling unit 103 → the fixing member 132 → the antenna coupling unit 104 → the transmission line 114 → the signal generating unit 10d → the signal processing unit 6. Third data transmission using a millimeter wave signal as a medium is performed via the signal processing unit 5 of the printed board 1 → the signal generating unit 10c → the transmission line 115 → the antenna coupling unit 105 → the fixing member 133 → the antenna coupling unit 106 → the transmission line 116 → the signal generating unit 10d → the signal processing unit 6.

[0139] Fourth data transmission using a millimeter wave signal as a medium is performed via the signal processing unit 5 of the printed board 1 → the signal generating unit 10c → the transmission line 117 → the antenna coupling unit 107 → the fixing member 134 → the antenna coupling unit 108 → the transmission line 118 → the signal generating unit 10d → the signal processing unit 6. Since the above-described first to fourth data transmission can be performed, it is possible to increase transmission capacity of video data and the like based on the millimeter wave signals four times as compared with the first embodiment.

<Third embodiment>

[0140] Fig. 11 is a perspective view showing an example of the configuration of an in-millimeter-wave dielectric transmission device 300 with a multi-stage structure as the third embodiment. In this embodiment, unlike the in-millimeter-wave dielectric transmission device 100 (a basic configuration) described in the first embodiment, a third printed board

14 is fixed above a printed board 1, and data transmission is performed between a signal processing unit 15 on the third printed board 14 and a signal processing unit 6 of a printed board 2 below the printed board 1 through a fixing member 16 constituting a dielectric transmission path.

[0141] The in-millimeter-wave dielectric transmission device 300 shown in Fig. 11 can be applied to a millimeter wave video data transmission device, a millimeter wave video data transmission system and the like, which convert data of a movie image, a computer image and the like into a plurality of millimeter wave signals S and transmit the millimeter wave signals at a high speed, and have a carrier frequency of 30 GHz to 300 GHz for carrying the millimeter wave signals.

[0142] In this embodiment, one piece of third signal processing board (hereinafter, referred to as the printed board 14) is provided above (at an outer side of) the printed board 1. In relation to the printed board 14, the fixing member 16 as a second fixing member, which is different from the first fixing member 13 provided between the printed board 1 and the printed board 2, constitutes a dielectric transmission path. The fixing member 16 not only transmits a millimeter wave signal but also supports the printed board 14 on the printed board 1 in cooperation with other fixing members 3 and 17.

[0143] The printed board 14 converts data of a movie image, a computer image and the like into a millimeter wave signal. The size of the printed board 14, for example, is defined as a length L, a width W and a thickness t, in the same manner as that in the first embodiment. The printed board 14, for example, includes the signal processing unit 15, a signal generating unit 10a, a transmission line 113, and an antenna coupling unit 103.

[0144] The signal processing unit 15 performs a process such as compression with respect to the data of the movie image, the computer image and the like based on a predetermined standard to output an electrical signal (hereinafter, referred to as an input signal). The signal processing unit 15 is connected to an electrical wiring 8c such as a wiring pattern. The electrical wiring 8c is connected to the signal generating unit 10a. The signal generating unit 10a performs signal processing with respect to the input signal to generate a millimeter wave signal.

[0145] The signal generating unit 10a is connected to one end of the transmission line 113. The transmission line 113 is electrically connected between the signal generating unit 10a and the antenna coupling unit 103 to transmit the millimeter wave signal. In this embodiment, the transmission line 113 electrically transmits the millimeter wave signal constituting the data of the movie image, the computer image and the like. A scheme of a strip line, a microstrip line, a coplanar line, a slot line and the like is applied to the transmission line 113 on the printed board 14.

[0146] The antenna coupling unit 103 is coupled to (disposed at) the other end of the transmission line 113. The antenna coupling unit 103 couples the millimeter wave signal, which is transmitted from the signal generating unit 10a via the transmission line 113, to one end of the fixing member 16. In this embodiment, the antenna coupling unit 103 converts the millimeter wave signal into an electromagnetic wave, and radiates the electromagnetic wave into the fixing member 16 constituting the dielectric transmission path. At the time of bi-directional data transmission, the antenna coupling unit 103 transmits millimeter wave video data and the like between the transmission line 11a connected to the signal generating unit 10a and the fixing member 16 constituting the dielectric transmission path.

[0147] The fixing member 16 is provided between the printed board 14 and the printed board 2 while having a predetermined dielectric constant. As the fixing member 16, a dielectric material at least including a glass epoxy-based, acryl-based, or polyethylene-based resin is used. In this embodiment, two fixing members 3 and one fixing member 17 are provided at four corners of each of the printed boards 1 and 14 together with the one fixing member 16 which divide the charge. The fixing member 16 is provided at a corner part of each of the printed boards 1 and 14, rather than the arrangement positions of the fixing members 3 and 17 for normal support.

[0148] The fixing member 16 supports the printed board 1, the printed board 2 and the printed board 14 together with the fixing member 13 constituting the dielectric transmission path and the other fixing members 3 and 17. The support function includes a case where the printed board 2 holds up and supports the printed board 1 and the printed board 14 and a case where the printed board 14 is suspended and supports the printed board 1 and the printed board 2.

[0149] In the support mechanism, the fixing members 3, 13, 16 and 17 are fixed such that the printed board 14, the printed board 1 and the printed board 2 are combined with one another in a predetermined direction and maintain the substantially parallel posture, for example, the printed board 14, the printed board 1 and the printed board 2 are connected to one another in the vertical direction.

[0150] When configuring the in-millimeter-wave dielectric transmission device 300 in this way, the printed board 14, the printed board 1 and the printed board 2 can be fixedly stacked in a rack configuration in the vertical direction via the fixing members 3, 13, 16 and 17. In addition, the fixing members 3, 13, 16 and 17, for example, use a resin bar member formed in a cylindrical shape and having a male thread structure at the front end thereof. Of course, except for the fixing members 13 and 16, the fixing members 3 and 17 may also use a metal bar member having a predetermined shape.

[0151] The printed board 2, which receives an electromagnetic wave based on a millimeter wave signal from the printed board 14, includes antenna coupling units 102 and 104 of two systems, two transmission lines 112 and 114, a signal generating unit 10e and the signal processing unit 6, which are mounted thereon, receives an electromagnetic wave based on a millimeter wave signal from the printed board 1, that is, receives the millimeter wave signals of two systems, and performs signal processing with respect to the millimeter wave signals. In this embodiment, the two transmission lines 112 and 114 drawn out from the antenna coupling units 102 and 104 of the two systems are connected

to the signal generating unit 10e. A scheme of a strip line, a microstrip line, a coplanar line, a slot line and the like is applied to the transmission lines 112 and 114 on the front and the back of the printed board 2.

[0152] The other end of the above-described fixing member 13 is bonded to the antenna coupling unit 102 provided at a first corner of the printed board 2. The antenna coupling unit 102 receives an electromagnetic wave from the fixing member 13 connected to the printed board 1 and converts the electromagnetic wave into a millimeter wave signal. The millimeter wave signal is output to the signal generating unit 10e through the transmission line 112. The other end of the fixing member 16 is bonded to the antenna coupling unit 104 provided at a second corner of the printed board 2. The antenna coupling unit 104 receives an electromagnetic wave from the fixing member 16 and converts the electromagnetic wave into a millimeter wave signal. The millimeter wave signal is output to the signal generating unit 10e through the transmission line 114.

[0153] Unlike the first and second embodiments, the signal generating unit 10e receives the respective millimeter wave signals, which are received in the antenna coupling units 102 and 104 of the two systems, via the two transmission lines 112 and 114, and generates an output signal by performing signal processing with respect to the millimeter wave signals of the two systems which are input via the transmission lines 112 and 114. The signal generating unit 10e, for example, is configured by providing the signal generating unit 10b, which is described in the first embodiment, in a row by two systems.

[0154] The signal processing unit 6 is connected to the signal generating unit 10e through an electrical wiring 8b such as a wiring pattern. The signal processing unit 6 performs a process such as expansion with respect to the output signal, which is generated by the signal generating unit 10e, based on a predetermined standard, thereby achieving data of a movie image, a computer image and the like.

[0155] The printed board 1 as described in the first embodiment is provided below the above-described printed board 14. The printed board 1 includes a signal processing unit 5, a signal generating unit 10a and a transmission line 11a, which are mounted thereon. However, unlike the first embodiment, the transmission line 11a is bonded to an antenna coupling unit 109.

[0156] Fig. 12 is a sectional view showing an example of the configuration of the antenna coupling unit 109 of the printed board 1. According to the antenna coupling unit 109 shown in Fig. 12, unlike the configuration of the dielectric transmission path termination part 30 mounted at the termination part of the fixing member 13 described in Figs. 2A, 2B and 3, a dielectric transmission path termination part 34 with a different structure is mounted. The dielectric transmission path termination part 34 is provided at the upper portion thereof with a female thread structure 36 and the lower portion thereof with a female thread structure 32, and has a part connection function of connecting the fixing member 17 provided above the dielectric transmission path termination part 34 to the fixing member 13 provided below the dielectric transmission path termination part 34. The dielectric transmission path termination part 34 uses the same material as the dielectric transmission path termination part 30, and a manufacturing method thereof is the same as that of the dielectric transmission path termination part 30.

[0157] In this embodiment, a male thread structure 38 is formed at the end portion of the fixing member 17, and the female thread structure 36 formed at the upper portion of the dielectric transmission path termination part 34 in correspondence with the male thread structure 38 is connected with the male thread structure 38 of the fixing member 17 by screwing. Since the female thread structure 32 formed at the lower portion of the dielectric transmission path termination part 34 has the same configuration and function as the dielectric transmission path termination part 30, detailed description thereof will be omitted (refer to Fig. 2B).

[0158] In addition, for a connection of the fixing member 16 constituting the dielectric transmission line in the printed board 1, the fixing member 16 is configured to be fixed in a general purpose thread structure via a through hole 4 formed in the printed board 1. Of course, it may also be possible to employ the part connection function of the dielectric transmission path termination part 34. In this way, the in-millimeter-wave dielectric transmission device 300 is configured.

[0159] Since the in-millimeter-wave dielectric transmission device 300 may employ the examples (1 to 3) of forming the in-millimeter-wave dielectric transmission device 100 shown in Figs. 5 to 7 by replacing reference numerals, except for the assembly of the fixing members 16 and 17, detailed description thereof will be omitted.

[0160] As described above, according to the in-millimeter-wave dielectric transmission device 300 as the third embodiment, the printed board 14 is provided above (at an outer side of) the printed board 1. In relation to the printed board 14, both the fixing member 13 provided between the printed board 1 and the printed board 2 and the fixing member 16 different from the fixing member 13 constitute the dielectric transmission paths. The fixing member 16 not only transmits the millimeter wave signal but also supports the printed board 1 and the printed board 14 in cooperation with the other fixing members 3 and 17.

[0161] Consequently, it is possible to process the millimeter wave signal while transmitting and receiving the millimeter wave signal among a plurality of signal processing boards via the fixing member 13 and the fixing member 16 which constitute the dielectric transmission paths. For example, according to the downlink data transmission path of the millimeter wave, data transmission of a first system using a millimeter wave signal as a medium is performed via the signal processing unit 5 of the printed board 1 → the signal generating unit 10a → the transmission line 11a → the antenna

coupling unit 102 → the fixing member 13 → the antenna coupling unit 102 → the transmission line 112 → the signal generating unit 10b → the signal processing unit 6.

[0162] Furthermore, data transmission of a second system using a millimeter wave signal as a medium is performed via the signal processing unit 15 of the printed board 14 → the signal generating unit 10a → the transmission line 113 → the antenna coupling unit 103 → the fixing member 16 → the antenna coupling unit 104 → the transmission line 114 → the signal generating unit 10b → the signal processing unit 6. In addition, it is possible to configure a three-dimensional structure suitable for a housing shape. Consequently, mutual data transmission can be performed among the printed boards 1, 2 and 14 with the three-stage configuration.

<Fourth embodiment>

[0163] Fig. 13 is a perspective view showing an example of the configuration of an in-millimeter-wave dielectric transmission device 400 as the fourth embodiment. In this embodiment, a fixing member 18 constituting a dielectric transmission path and a fixing member 19 for normal support are provided between two printed boards 1 and 2, and the printed boards 1 and 2 are horizontally supported by the fixing members 18 and 19.

[0164] The in-millimeter-wave dielectric transmission device 400 shown in Fig. 13 can be applied to a millimeter wave video data transmission device, a millimeter wave video data transmission system and the like, which convert data of a movie image, a computer image and the like into a plurality of millimeter wave signals S and transmit the millimeter wave signals at a high speed, and have a carrier frequency of 30 GHz to 300 GHz for carrying the millimeter wave signals.

[0165] According to the in-millimeter-wave dielectric transmission device 400, the fixing members 18 and 19 having a substantially flat U shape are provided, the printed board 1 and the printed board 2 are provided in a row, and the fixing members 18 and 19 are provided between the printed board 1 and the printed board 2, so that the printed board 1 and the printed board 2 are fixedly connected to each other and supported by the fixing members 18 and 19 while maintaining a substantially horizontal state. The fixing member 18 has a substantially flat U shape and is provided between the printed board 1 and the printed board 2 while having a predetermined dielectric constant. As the fixing member 18, a dielectric material at least including a glass epoxy-based, acryl-based, or polyethylene-based resin is used.

[0166] In this embodiment, four fixing members 3 having a predetermined height, one fixing member 19 and one fixing member 18 are provided at two upper corners, two lower corners and right and left connection parts of the printed boards 1 and 2 while dividing the charge. The fixing member 18 is provided at a connection part between the printed boards 1 and 2, rather than the arrangement positions of the fixing members 3 and 19 for normal support. In this embodiment, the fixing member 18 is provided at the left side of the connection part between the printed boards 1 and 2.

[0167] The fixing member 19 is provided at the right side of the connection part between the printed boards 1 and 2. The fixing member 19 has the same shape as the fixing member 18, but has no waveguide 23a or the like. That is to say, an antenna coupling unit 101 is not provided at the fourth corner of the printed board 1 and the third corner of the printed board 2. The four fixing members 3 provided at the two upper corners and the two lower corners of the printed boards 1 and 2 are configured to be fixed in a general purpose thread structure via through holes 4.

[0168] Furthermore, the printed board 1 connected by the fixing members 18 and 19 having a substantially flat U shape includes a signal processing unit 5, a signal generating unit 10a and a transmission line 11a which are mounted thereon, and the transmission line 11a is bonded to the antenna coupling unit 101. Since the functions and formation method of these members have been described in the first embodiment, detailed description thereof will be omitted. One end of the above-described fixing member 18 is bonded to the antenna coupling unit 101 provided at a first corner of the printed board 1. The antenna coupling unit 101 of the printed board 1 converts a millimeter wave signal into an electromagnetic wave and radiates the electromagnetic wave into the fixing member 18.

[0169] The printed board 2, which receives the electromagnetic wave based on the millimeter wave signal from the above-described printed board 1, includes the antenna coupling unit 101, a transmission line 11b, a signal generating unit 10b and a signal processing unit 6, which are mounted thereon, receives the electromagnetic wave based on the millimeter wave signal from the printed board 1, and performs signal processing with respect to the millimeter wave signal. A scheme of a strip line, a microstrip line, a coplanar line, a slot line and the like is applied to the transmission lines 11a and 11b on the surfaces of the printed boards 1 and 2.

[0170] The other end of the fixing member 18 is bonded to the antenna coupling unit 101 provided at a second corner of the printed board 2. The antenna coupling unit 101 of the printed board 2 receives the electromagnetic wave from the fixing member 18 and converts the electromagnetic wave into a millimeter wave signal. The millimeter wave signal is output to the signal generating unit 10b through the transmission line 11b. In addition, since the functions of the signal generating unit 10b and the signal processing unit 6 have been described in the first embodiment, detailed description thereof will be omitted.

[0171] Fig. 14 is a sectional view showing an example in which the antenna coupling unit 101 is bonded to the fixing member 18. In this embodiment, a microstrip line is applied to the transmission line 11a connected to the antenna coupling unit 101. The antenna coupling unit 101 shown in Fig. 14 is provided to the printed board 1, the printed board

2 and the like and includes a waveguide 23a, a through hole 26 and a signal converting section 36.

[0172] The shapes of the waveguide 23a and the through hole 26 are as described in the first embodiment. The waveguide 23a of the printed board 1 converts a millimeter wave signal electrically transmitted through the transmission line 11a into an electromagnetic wave, and transmits the electromagnetic wave to the dielectric transmission path. The end portion of the fixing member 18 is configured to be fixed to the printed board 1 by a dielectric transmission path termination part 30. In addition, since elements having the same reference numerals as those described in the first embodiment have the same functions and the formation method and dimensions thereof are as described in the first embodiment, detailed description thereof will be omitted.

[0173] Fig. 15 is a perspective view showing an example of the shape of the fixing member 18 and the dielectric transmission path termination part 30. In this example, the end portion of the fixing member 18 has substantially a C shape at the front end thereof such that the fixing member 18 can pass through the through hole 26 shown in Fig. 14. The end portion of the fixing member 18 having passed through the through hole 26 is bonded to the dielectric transmission path termination part 30 shown in Fig. 15, so that the fixing member 18 is fixed to the printed board 1. The fixing member 18 is also fixed to the printed board 2 in the same manner.

[0174] In this example, the front end of the fixing member 18 in the antenna coupling unit 101 has the same shape as the front end of the fixing member 13 shown in Fig. 3. However, the dielectric transmission path of the fixing member 18 is changed from a cylindrical shape of the fixing member 13 to a rectangular parallelepiped shape. Both front end portions of the fixing member 18 have a substantially flat U shape bent in an L shape. In addition, since the configuration of the dielectric transmission path termination part 30 and a mounting method thereof have been described in the first embodiment, i.e., fixing by a female thread structure 32 corresponding to a male thread structure 31 of the fixing member 18, detailed description thereof will be omitted.

[0175] In this example also, in the case where the distance between the printed board 1 and a ceiling surface II when the dielectric transmission path termination part 30 is fitted around the fixing member 18 is defined as D2, the distance D2 is set to 1/4 of the wavelength λ of a millimeter wave signal on the air and adjusted to enhance an electromagnetic wave, so that the millimeter wave signal can be efficiently converted into an electromagnetic wave.

[0176] Since this example employs a structure in which the electromagnetic wave does not propagate in the vertical direction as with the first embodiment, but propagates through the dielectric transmission path having a substantially flat U shape in the horizontal direction, a reflector may also be provided immediately below the signal converting section 36. The reflector is set to an angle of 45° with respect to the direction in which the electromagnetic wave is radiated to the fixing member 18, or the horizontal direction in which the electromagnetic wave progresses, and totally reflects the electromagnetic wave, so that the propagation direction is bent at an angle of 90°.

[0177] When configuring the in-millimeter-wave dielectric transmission device 400 in this way, it is possible to confine an electromagnetic wave based on a millimeter wave signal in the fixing member 18 constituting the dielectric transmission path. Furthermore, the millimeter wave signal can be converted into an electromagnetic wave at the one end of the fixing member 18 constituting the dielectric transmission path, and the electromagnetic wave can be converted into the millimeter wave signal at the other end of the fixing member 18. In addition, since the in-millimeter-wave dielectric transmission device 400 may employ the examples (1 to 3) of forming the in-millimeter-wave dielectric transmission device 100 shown in Figs. 5 to 7, except for the assembly of the fixing members 18 and 19, detailed description thereof will be omitted.

[0178] As described above, according to the in-millimeter-wave dielectric transmission device 400 of the fourth embodiment, the fixing member 18 constituting the dielectric transmission path and the fixing member 19 for normal support are provided between the two printed boards 1 and 2, so that the printed board 1 and the printed board 2 are fixedly connected to each other and supported by the fixing members 18 and 19.

[0179] Consequently, the printed board 1 and the printed board 2 can be expanded in the horizontal direction (two-dimensionally) via the fixing members 18 and 19. In addition, the electromagnetic wave based on the millimeter wave signal S radiated from the one end of the fixing member 18 constituting the dielectric transmission path can be received in the other end of the fixing member 18. Thus, it is possible to remove a communication cable, a connector and the like for connecting the printed board 1 to the printed board 2 according to the related art. In addition, support and high speed data transmission between the printed board 1 and the printed board 2 are performed by the fixing member 18 which is the same material. The high speed data transmission in the fixing member 18 is performed by a millimeter wave (an electromagnetic wave), the fixing member 18 constituting the dielectric transmission path is finished with a single material. Thus, processing demanding accuracy as with an optical waveguide is not necessary.

[0180] Moreover, when the printed board 1 and the fixing member 18 are fixed in the antenna coupling unit 101, strictness of position adjustment for stably performing data transmission is not necessary, unlike the case of employing an optical transmission method. According to the in-millimeter-wave dielectric transmission device 400, it is possible to perform support and high speed data transmission between the printed boards 1 and 2 with a simple and inexpensive configuration, resulting in the improvement of reliability of data transmission against vibration and deviation.

<Fifth embodiment>

[0181] Figs. 16, 17A to 17D, 18 and 19A to 19D are diagrams explaining the fifth embodiment. Fig. 16 is a perspective view showing an example of the configuration of a wireless transmission device 500 of the fifth embodiment. Figs. 17A to 17D are diagrams explaining details of an antenna coupling unit and a waveguide of the fifth embodiment. Fig. 18 is a diagram explaining an example of a simulation characteristic of the fifth embodiment. Figs. 19A to 19D are diagrams explaining a modified example of an antenna structure (specifically, an antenna pattern).

[0182] The fifth embodiment relates to a wireless transmission mechanism in which a signal (a baseband signal) to be transmitted is converted to a high frequency signal with a high frequency and a frequency band thereof is not limited to a millimeter wave band. For example, it is also considered to employ a microwave band in addition to the millimeter wave band. Furthermore, the fifth embodiment relates to a wireless transmission mechanism in which a support member for supporting a circuit board of a transmission side or a reception side is not limited to an object made of a dielectric material. Fig. 16 shows a modified example of the first embodiment. However, the method of the fifth embodiment can be applied to the second to fourth embodiments. Hereinafter, the fifth embodiment will be described while focusing on the differences between the first embodiment and the fifth embodiment.

[Entire configuration]

[0183] As shown in Fig. 16, in the wireless transmission device 500, the fixing member 13, which is an example of a support member also used as a dielectric transmission path in the in-millimeter-wave dielectric transmission device 100 of the first embodiment, is replaced with a waveguide 513 which is an example of a support member also used as a wireless signal transmission path. Furthermore, the antenna coupling unit 101 is replaced with an antenna coupling unit 501 and the antenna coupling unit 102 is replaced with an antenna coupling unit 502. The antenna coupling units 501 and 502 include dielectric boards 510 provided on printed boards 1 and 2, and antenna patterns (which will be described later) formed on the dielectric boards 510, respectively.

[0184] The antenna coupling unit 501 and the antenna coupling unit 502 form a symmetric structure with respect to opposite surfaces of the printed boards 1 and 2 because the dielectric boards 510 of the antenna coupling units 501 and 502 are provided on the surface of the printed board 1 facing the printed board 2 and the surface of the printed board 2 facing the printed board 1, respectively.

[0185] For example, in the printed board 1, the antenna coupling unit 501 is signal-coupled to the waveguide 513 constituting the wireless signal transmission path and transmits/receives an electromagnetic wave via the waveguide 513. One end of a transmission line 11a is coupled to (disposed at) the dielectric board 510_1 disposed on the surface (rear surface) of the printed board 1 facing the printed board 2. In this embodiment, the transmission line 11a is disposed on the rear surface of the printed board 1 and is wired to a signal generating unit 10a on the surface of the printed board 1 through a contact hole 12 (a via hole).

[0186] Meanwhile, in the printed board 2, the antenna coupling unit 502 is signal-coupled to the waveguide 513 constituting the wireless signal transmission path and transmits/receives an electromagnetic wave via the waveguide 513. One end of a transmission line 11b is coupled to (disposed at) the dielectric board 510_2 disposed on the surface of the printed board 2 facing the printed board 1. In this embodiment, the transmission line 11b is disposed on the surface of the printed board 2 and is connected to a signal generating unit 10b on the surface of the printed board 2.

[0187] The waveguide 513 is provided at a corner part between the printed board 1 and the printed board 2, rather than the arrangement positions of fixing members 3 for normal support. The waveguide 513 surrounds the antenna pattern, which will be described later, and, for example, adheres to the dielectric boards 510, so that relative positions thereof are fixed. In the drawing, the waveguide 513 is shown in a cylindrical shape. However, the present invention is not limited thereto. For example, the section of the waveguide 513 is not limited to a circular shape, and may have a rectangular shape, shapes other than the rectangular shape, an oval shape and the like. The waveguide 513 not only constitutes the wireless signal transmission path but also supports the printed board 1 and the printed board 2 together with the other three fixing members 3.

[0188] The waveguide 513 may also be hollow (that is, the waveguide 513 is filled with air). That is, the waveguide 513 constitutes the wireless signal transmission path (e.g., a millimeter wave signal transmission path), and a shield member (e.g., a metal material) for blocking external radiation of a wireless signal (an electric wave) may be provided to surround the transmission path so that the transmission path inside the shield member may be a hollow waveguide (a cavity waveguide).

[0189] Furthermore, filling the waveguide 513 with a dielectric material may also be considered. By filling the dielectric material, multiple reflection in the waveguide can be prevented and a sectional size (a pipe diameter) of the waveguide can be reduced. For example, in the case where the waveguide 513 is a circular waveguide, when a specific dielectric constant of filled dielectric substance is defined as ε, the diameter of the waveguide can be reduced by about $1/\sqrt{\varepsilon}$ times as compared with the case where a waveguide is hollow. Furthermore, a reflection component due to mismatching of

transmission (reception) ports is multiply reflected in the waveguide, causing adverse effect on the transmission (reception) ports. Herein, when the waveguide is filled with air, since passing loss occurs rarely, a power level is not attenuated even in the multiple reflection, resulting in large adverse effects. However, if a dielectric substance having a loss is filled, a power level of a reflected wave is attenuated, resulting in the suppression of adverse effects.

[0190] Even when the waveguide 513 is filled with a dielectric material, it is preferable that a shield member (e.g., a metal material) is used as a peripheral member of the waveguide 513. In short, a signal transmission path for transmitting an electromagnetic wave may be air (that is to say, free space). However, it is preferable to have a structure capable of transmitting an electromagnetic wave while confining an electromagnetic wave in a transmission path. In addition, in the case of creating the waveguide 513 filled with a dielectric substance, filling a cylindrical member made of a metal material with a dielectric substance or performing a surface process (called metal plating) of coating a metal thin film to cover the outer periphery of the dielectric material may be considered. According to a structure in which metal plating is performed with respect to the outer periphery of the dielectric material, along with miniaturization, lightness can be achieved as compared with the case where dielectric substance is filled in a metal housing. Meanwhile, according to a structure in which a dielectric material is filled in a cylindrical member made of a metal material, strength can be increased as compared with the case of performing metal plating.

[Electromagnetic wave coupling structure]

[0191] Figs. 17A to 17D show details of an electromagnetic wave coupling structure including the antenna coupling units 501 and 502 and the waveguide 513. Fig. 17A is an overall view and Fig. 17B is a side-sectional view thereof. Fig. 17C is a sectional view focusing on the printed boards 1 and 2 and the dielectric board 510. Fig. 17D is a view explaining an antenna pattern.

[0192] The electromagnetic wave coupling structure includes the dielectric board 510_1 constituting a part of the antenna coupling unit 501 of the printed board 1, the dielectric board 510_2 constituting a part of the antenna coupling unit 502 of the printed board 2, and the waveguide 513 constituting a transmission path (a waveguide) interposed between the dielectric board 510_1 and the dielectric board 510_2 to allow an electric wave to propagate therethrough.

[0193] As described in Fig. 16, the dielectric board 510_1 is disposed on the rear surface of the printed board 1 and the dielectric board 510_2 is disposed on the surface of the printed board 2. The printed boards 1 and 2 are provided with the antenna coupling units 501 and 502 (transmission path coupling units) including the transmission lines 11a and 11b (microstrip lines), which are an example of lines electrically connected to the signal generating units 10 (not shown), respectively. For example, the waveguide 513 is provided at both ends thereof with the antenna coupling units 501 and 502 which supply or receive an electromagnetic wave to/from the waveguide 513, respectively.

[0194] In the antenna coupling units 501 and 502, as shown in Fig. 17C, a thin conductor layer 521 serving as a ground conductor is first formed on the printed boards 1 and 2, and a dielectric board 510 serving as a dielectric layer and having a thickness d51 is disposed on the thin conductor layer 521. A conductor line 522 having a width w52 and connected to the transmission lines 11 (11a and 11b) is formed on the surface of the dielectric board 510. An antenna structure is coupled to the front end of the conductor line 522 to radiate an electromagnetic wave. The conductor layer 521, the dielectric board 510 and the conductor line 522 are configured to form a microstrip line 520.

[0195] The antenna structure provided to the front end of the conductor line 522 represents a structure in a coupling section with a signal transmission path (the conductor line 522) configured in the waveguide 513, may allow an electrical signal of a microwave band or a millimeter wave band to be coupled to a the signal transmission path, and does not represent an antenna itself. For example, the antenna structure includes an antenna terminal, a microstrip line, and an antenna.

[0196] In the fifth embodiment, as an antenna with the antenna structure, a patch antenna 530B including a rectangular patch pattern (an antenna pattern) is used as shown in Fig. 17D. A cutout structure 532 is formed at a coupling section of the conductor line 522 and the patch antenna 530B to adjust a feeding point.

[0197] The waveguide 513 is formed with a gap part 515 for preventing the waveguide 513 from making contact with the conductor line 522. The hollow waveguide 13 is disposed between the printed boards 1 and 2 such that the center of a diameter coincides with the center of the patch antenna 530B. The waveguide 61 is fixed to the dielectric board 510 using adhesive to surround the patch antenna 530B. The second floor of the dielectric board 510 serves as a conductor line (the conductor layer 521) and is terminated.

[0198] With such a configuration, a millimeter wave signal, for example, is fed from a microstrip line 520_1 of the antenna coupling unit 501 to a patch antenna 530B_1 and coupled to the waveguide 513, thereby propagating the waveguide. Then, the millimeter wave signal is coupled to a patch antenna 530B_2 of the antenna coupling unit 502 and transmitted to a microstrip line 520_2. In the case of reverse transmission, a millimeter wave signal is fed from the microstrip line 520_2 of the antenna coupling unit 502 to the patch antenna 530B_2 and coupled to the waveguide 513, thereby propagating the waveguide. Then, the millimeter wave signal is coupled to the patch antenna 530B_1 of the antenna coupling unit 501 and transmitted to the microstrip line 520_1.

[Simulation]

[0199] A case where the waveguide 513 is applied to the wireless transmission device 500 will be described based on S parameters obtained by simulating a pass characteristic (size of loss) and a reflection characteristic using the AET MW-STUDIO.

[0200] Table 1 shows parameters provided to a simulation model of the wireless transmission device 500. For example, the patch antenna 530B has an approximately square shape and one side d50 thereof is 1.3 mm. The thickness d51 of the dielectric board 510 is 0.1 mm. The conductor line 522 has a width w52 of 0.2 mm and a thickness d52 of 0.02 mm. The waveguide 513 is a hollow waveguide and has a diameter d53 of 3.45 mm and a length L53 (i.e., an inter-board distance) of 5 mm. The dielectric board 510 has specific dielectric constant of 3.4 and dielectric loss tangent tan δ 0.01. Although not shown in Table 1, similarly to the first embodiment, the printed boards 1 and 2 have thicknesses of 1.0 mm, specific dielectric constants of 3.5 and dielectric loss tangents tan δ of 0.005, respectively.

[0201]

Table 2

Parameter	Value	Unit
Diameter d50 of patch antenna 530	1.3	mm
thickness d51 of dielectric board 510	0.1	mm
width w52 of conductor line 522	0.2	mm
thickness d52 of conductor line 522	0.02	mm
diameter d53 of waveguide 513 (hollow waveguide)	3.45	mm
length L53 of waveguide 513 (hollow waveguide)	5	mm
specific dielectric constant of dielectric board 510	3.4	none
dielectric loss tangent of dielectric board 510 (1 GHz)	0.01	none

[0202] Fig. 18 is a graph showing an example of a simulation characteristic (pass characteristic S (2, 1) and a reflection characteristic S (1, 1)) of the wireless transmission device 500, and corresponds to Fig. 9 of the first embodiment.

[0203] According to a simulation result of the pass characteristic S (2, 1) dB, video data based on the millimeter wave signal S has passing loss of several dB (about 2 dB) in the vicinity of a carrier frequency of 60 GHz.

[0204] According to a simulation result of the reflection characteristic S (1, 1) dB, reflection loss of -10 dB or less is achieved in the range in which a carrier frequency is 57.7 GHz to 61.1 GHz.

[0205] As described above, in the wireless transmission device 500 of the first embodiment, at least a part of the support members of the printed boards 1 and 2 is used as a wireless signal transmission path, and the basic concept is not different from the first to fourth embodiments. Even when the patch antenna 530B is used as an antenna structure or a hollow waveguide is used as the waveguide 513, wireless transmission of a millimeter wave can be performed without inconvenience as can be seen from the simulation results.

[0206] Since the original support structure of the waveguide 513 can be used as a wireless signal transmission path, it is possible to achieve the same effects as those in the first to fourth embodiments, such as removal of a communication cable, a connector and the like for connecting the printed board 1 to the printed board 2 according to the related art.

[Modified example of antenna structure]

[0207] Figs. 19A to 19D show modified examples of an antenna structure (an antenna pattern) used in the wireless transmission device 500 of the first embodiment. The antenna pattern is not limited to the rectangular pattern forming the patch antenna 530B as shown in Fig. 17D. The antenna structure may be configured by forming an antenna pattern with a conductor pattern having a predetermined shape on the surface of the dielectric board 510 with respect to the conductor line 522 of 50 Ω formed on the surface of the dielectric board 510.

[0208] The first example shown in Fig. 19A is a microstrip antenna 530A using the end portion of the conductor line 522 as is. In such a case, a resonance structure serves as an antenna. In other words, it can be said that a microstrip line is used as an antenna.

[0209] The second example shown in Fig. 19B is the same as that shown in Fig. 17D and is a structure in which the horizontal width of a line part (a strip part) of the microstrip antenna 530A is increased in order to improve the radiation efficiency of an electrical wave, as compared with the microstrip antenna 530A. Although not shown in Fig. 19B, the

cutout structure 532 may be formed at the coupling section between the conductor line 522 and the patch antenna 530B to adjust the feeding point. In addition, in the example shown in Fig. 19B, the patch has a rectangular shape. However, the present invention is not limited thereto. For example, the patch may have a circular shape or other shapes.

[0210] The third example shown in Fig. 19C is a planar inverted-F antenna 530C. A feeding line 530Ca is connected to the conductor line 522, and a short-circuit line 530Cb is connected to a ground plane which is the conductor layer 521 formed on the surface of the lower portion of the dielectric board 510.

[0211] The fourth example shown in Fig. 19D is a differential antenna 530D and is configured by combining a phase shifter 530Da with a dipole antenna 530 Db. The phase shifter 530Da includes phase shifters 530Da_1 and 530Da_2 having line lengths different from each other. A connection point between the phase shifters 530Da_1 and 530Da_2 is connected to the conductor line 522. The other end of the phase shifter 530Da_1 is connected to one element 530Db_1 of the dipole antenna 530 Db, and the other end of the phase shifter 530Da_2 is connected to the other element 530Db_2 of the dipole antenna 530 Db. In the dipole antenna 530 Db, a phase difference is 180° at the other ends thereof by a difference between the line lengths of the phase shifters 530Da_1 and 530Da_2.

[0212] The previous embodiments are very suitable for an in-millimeter-wave dielectric transmission device, an in-millimeter-wave dielectric transmission method, an in-millimeter-wave dielectric transmission system and the like, which transmit a millimeter wave signal having a carrier frequency of 30 GHz to 300 GHz for carrying a movie image, a computer image and the like at a high speed.

[0213] The preferred embodiments of the present invention have been described above with reference to the accompanying drawings, while the present invention is not limited to the above examples, of course. A person skilled in the art may find various alternations and modifications within the scope of the appended claims, and it should be understood that they will naturally come under the technical scope of the present invention.

Claims

1. An in-millimeter-wave dielectric transmission device comprising:

   a first signal processing board for processing a millimeter wave signal;
   a second signal processing board signal-coupled to the first signal processing board to receive the millimeter wave signal and perform signal processing with respect to the millimeter wave signal; and
   a support member provided between the first signal processing board and the second signal processing board, wherein the support member constitutes a dielectric transmission path and supports the first signal processing board and the second signal processing board.

2. The in-millimeter-wave dielectric transmission device according to claim 1, wherein the first signal processing board includes:

   a first signal generating unit for generating a millimeter wave signal by performing signal processing with respect to an input signal; and
   a first signal coupling unit for coupling the millimeter wave signal generated by the first signal processing unit to the support member,
   wherein the second signal processing board provided via the support member constituting the dielectric transmission path includes:

      a second signal coupling unit for receiving the millimeter wave signal from the support member; and
      a second signal generating unit for generating an output signal by performing signal processing with respect to the millimeter wave signal received in the second signal coupling unit.

3. The in-millimeter-wave dielectric transmission device according to claim 2, wherein the first signal processing board includes a first transmission line electrically connected between the first signal generating unit and the first signal coupling unit to transmit a millimeter wave signal,
   wherein the first signal coupling unit includes:

      a first waveguide formed by a through hole which is opened in the first signal processing board and has a predetermined shape; and
      a first signal converting section disposed to enter the first waveguide and including the first transmission line to convert the millimeter wave signal into an electromagnetic wave, and
      the first signal coupling unit transmits the electromagnetic wave converted by the first signal converting section

to one end of the support member constituting the dielectric transmission path, and fixes the one end of the support member to the first signal processing board by a through hole having a predetermined shape to surround the first waveguide,

wherein the second signal processing board includes a second transmission line electrically connected between the second signal generating unit and the second signal coupling unit to transmit a millimeter wave signal, and

wherein the second signal coupling unit includes:

a second waveguide formed by a through hole which is opened in the second signal processing board and has a predetermined shape; and

a second signal converting section disposed to enter the second waveguide and including the second transmission line to convert an electromagnetic wave, which is propagated through the support member, into a millimeter wave signal, and

the second signal coupling unit converts an electromagnetic wave, which is propagated to the other end of the support member constituting the dielectric transmission path, into a millimeter wave signal by the second signal converting section, transmits the millimeter wave signal to the second transmission line via the second waveguide, and fixes the other end of the support member to the second signal processing board by a through hole having a predetermined shape to surround the second waveguide.

4. The in-millimeter-wave dielectric transmission device according to claim 3, wherein the first signal coupling unit includes a first fixing means for reflecting an electromagnetic wave radiated from the first transmission line to the first waveguide, and fixing the one end of the support member to the first signal processing board, and

wherein the second signal coupling unit includes a second fixing means for reflecting the electromagnetic wave, which is propagated to the other end of the support member and not converted into the millimeter wave signal by the second signal converting section, and fixing the other end of the support member to the second signal processing board.

5. The in-millimeter-wave dielectric transmission device according to claim 4, wherein the first fixing means for fixing the one end of the support member has a first gap part at a position at which the first transmission line crosses the first waveguide, and

wherein the second fixing means for fixing the other end of the support member has a second gap part at a position at which the second transmission line crosses the second waveguide.

6. The in-millimeter-wave dielectric transmission device according to claim 1, wherein a dielectric material at least including a glass epoxy-based, acryl-based, or polyethylene-based resin is used as the support member.

7. The in-millimeter-wave dielectric transmission device according to claim 2, wherein a modulation circuit for modulating the input signal and a first frequency conversion circuit for generating a millimeter wave signal by frequency-converting the input signal modulated by the modulation circuit are mounted on the first signal generating unit, and

wherein a second frequency conversion circuit for outputting an output signal by frequency-converting the millimeter wave signal and a demodulation circuit for demodulating the output signal, which is output from the second frequency conversion circuit, are mounted on the second signal generating unit.

8. The in-millimeter-wave dielectric transmission device according to claim 7, wherein amplifiers for amplifying a millimeter wave signal are mounted on the first signal generating unit and the second signal generating unit, respectively.

9. The in-millimeter-wave dielectric transmission device according to claim 1, wherein the support member is fixed such that the first signal processing board and the second signal processing board are combined in a predetermined direction and connected to each other while maintaining a substantially parallel posture.

10. The in-millimeter-wave dielectric transmission device according to claim 1, wherein the support member is fixed such that the first signal processing board and the second signal processing board are provided in parallel to each other and connected to each other while maintaining a substantially horizontal state.

11. The in-millimeter-wave dielectric transmission device according to claim 1, wherein a plurality of support members constituting the dielectric transmission path are provided between the first signal processing board and the second signal processing board, and each of the support members supports the first signal processing board and the second signal processing board and transmits the millimeter wave signal.

12. The in-millimeter-wave dielectric transmission device according to claim 11, wherein the first signal processing board includes:

a first signal generating unit for generating a plurality of millimeter wave signals by performing signal processing with respect to an input signal; and
a plurality of first signal coupling units for coupling each of the millimeter wave signals generated by the first signal generating unit to each of the support members, and
wherein the second signal processing board provided via the plurality of support members constituting the dielectric transmission path includes:

a plurality of second signal coupling units for receiving the millimeter wave signal from each of the support members; and
a second signal generating unit for generating an output signal by performing signal processing with respect to each of the millimeter wave signals received in the second signal coupling units.

13. The in-millimeter-wave dielectric transmission device according to claim 1, wherein at least one third signal processing board is provided at an outer side of the first signal processing board or an outer side of the second signal processing board via a second support member constituting a dielectric transmission path, which is different from a first support member provided between the first signal processing board and the second signal processing board, and
the second support member constitutes a dielectric transmission path, transmits a millimeter wave signal, and supports the third signal processing board.

14. A method of manufacturing an in-millimeter-wave dielectric transmission device, the method comprising the steps of:

forming a first signal processing board for processing a millimeter wave signal;
forming a second signal processing board for receiving the millimeter wave signal from the first signal processing board and performing signal processing with respect to the received millimeter wave signal; and
providing a support member between the first signal processing board and the second signal processing board, allowing the support member to form a dielectric transmission path, and allowing the support member on the second signal processing board to support the first signal processing board and the second signal processing board.

15. The method according to claim 14, wherein, when forming the first signal processing board, a first signal generating unit for generating a millimeter wave signal by performing signal processing with respect to an input signal and a first signal coupling unit for coupling the millimeter wave signal generated by the first signal processing unit to the support member are disposed on a predetermined board, and,
wherein when forming the second signal processing board, a second signal coupling unit for receiving the millimeter wave signal from the support member and a second signal generating unit for generating an output signal by performing signal processing with respect to the millimeter wave signal received in the second signal coupling unit are disposed on a predetermined board.

16. A wireless transmission device comprising:

a first circuit board including a first signal converting section for converting a signal to be transmitted to a high frequency signal with a high frequency;
a second circuit board including a second signal converting section for receiving a wireless signal based on the high frequency signal generated by the signal converting section, and converting the wireless signal to the signal to be transmitted; and
a support member provided between the first circuit board and the second circuit board to support the first circuit board and the second circuit board,
wherein the support member constitutes a wireless signal transmission path through which the wireless signal is transmitted from the first circuit board to the second circuit board.

17. The wireless transmission device according to claim 16, wherein, in the support member, a shield member for blocking external radiation of the wireless signal is provided to surround a transmission path, and the transmission path inside the shield member is a hollow waveguide.

18. The wireless transmission device according to claim 16, wherein, in the support member, a shield member for blocking external radiation of a wireless signal is provided to surround a transmission path, and the transmission path inside the shield member is filled with a dielectric material.

19. The wireless transmission device according to claim 16, wherein a first wireless signal coupling section is provided on the first circuit board to couple the high frequency signal generated by the first signal converting section to the support member as the wireless signal, and
wherein a second wireless signal coupling section is provided on the second circuit board to be coupled to the wireless signal transmitted via the support member as the wireless signal.

20. A wireless transmission method comprising, the steps of:

providing a support member provided between a circuit board of a transmission side and a circuit board of a reception side, and configured to support the circuit boards and constitute a wireless signal transmission path through which a wireless signal is transmitted from the circuit board of the transmission side to the circuit board of the reception side;
converting, by the circuit board of the transmission side, a signal to be transmitted to a high frequency signal with a high frequency;
transmitting the wireless signal based on the high frequency signal to the circuit board of the reception side via the support member; and
converting, by the circuit board of the reception side, the wireless signal, which is received via the support member, to the signal to be transmitted.

FIG.1

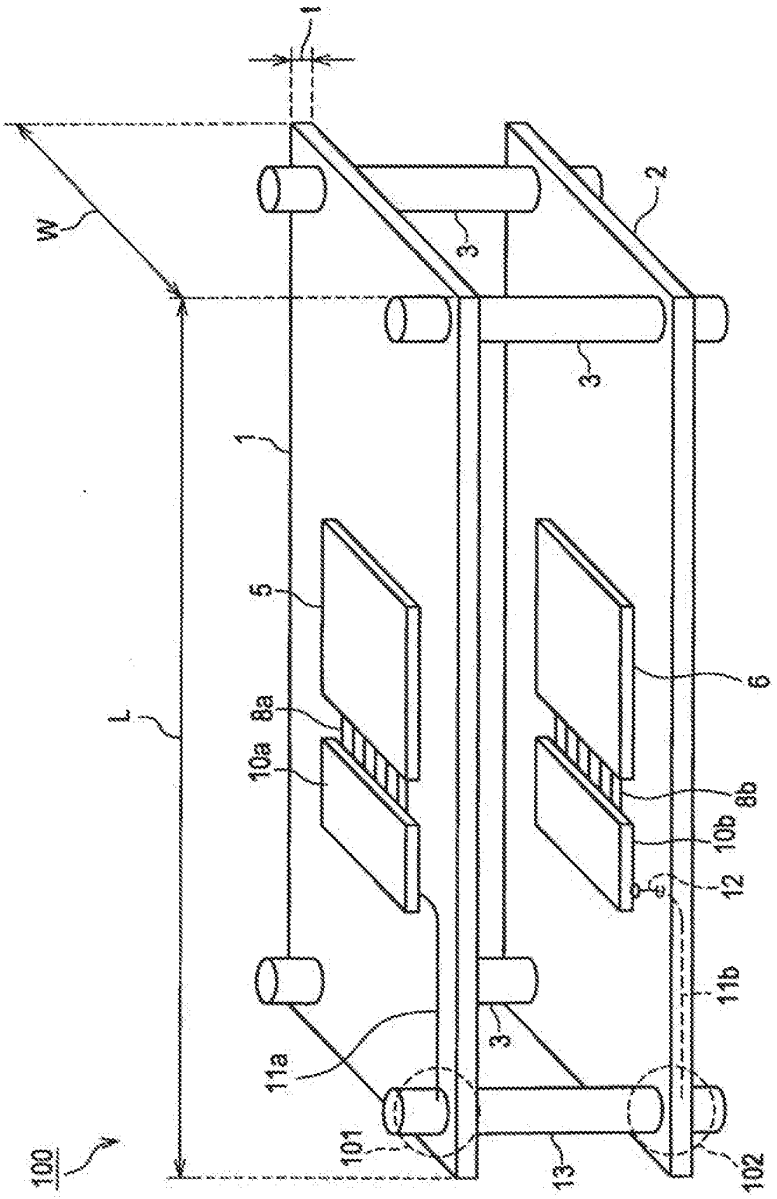


FIG.2A

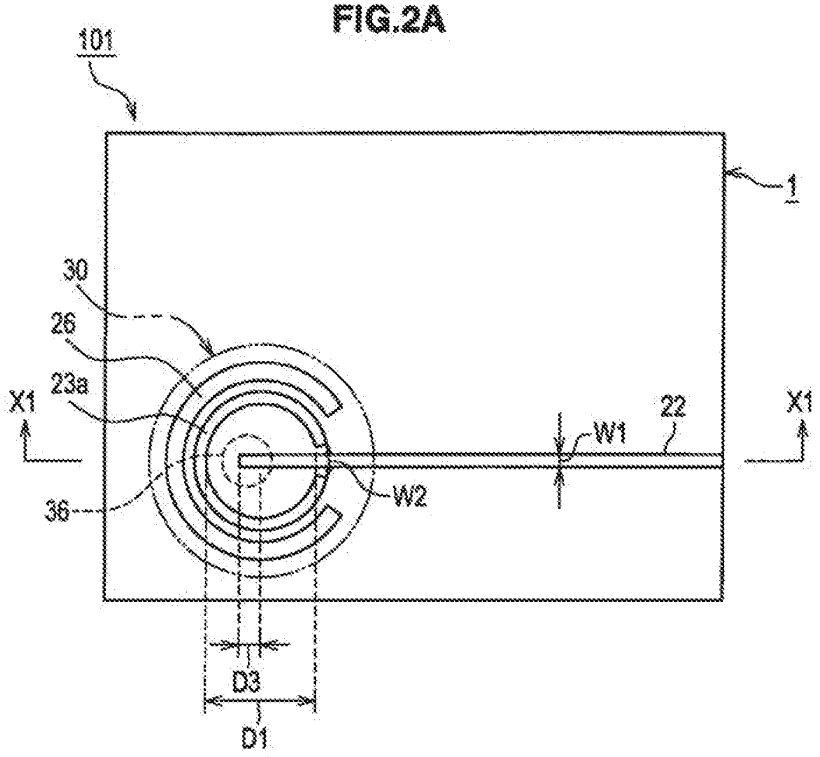


FIG.2B

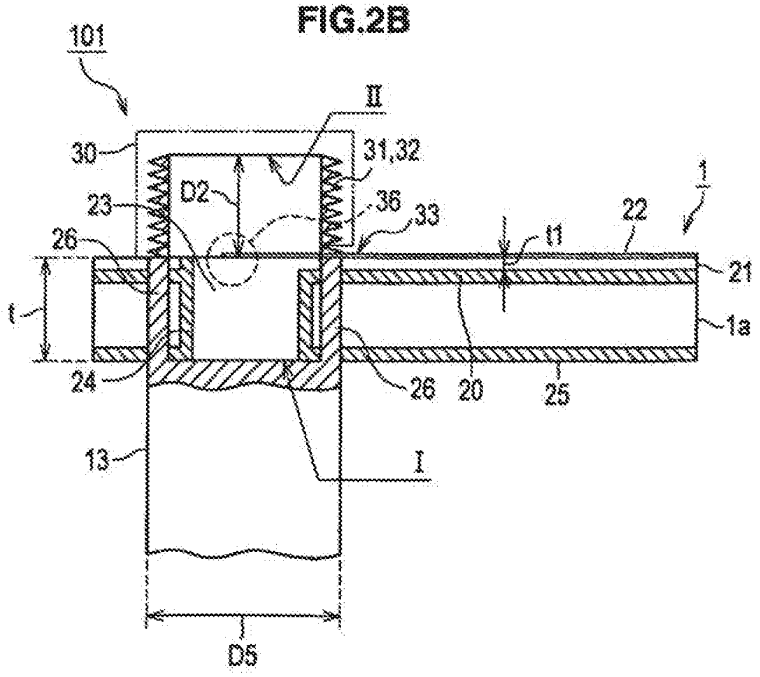


FIG.3

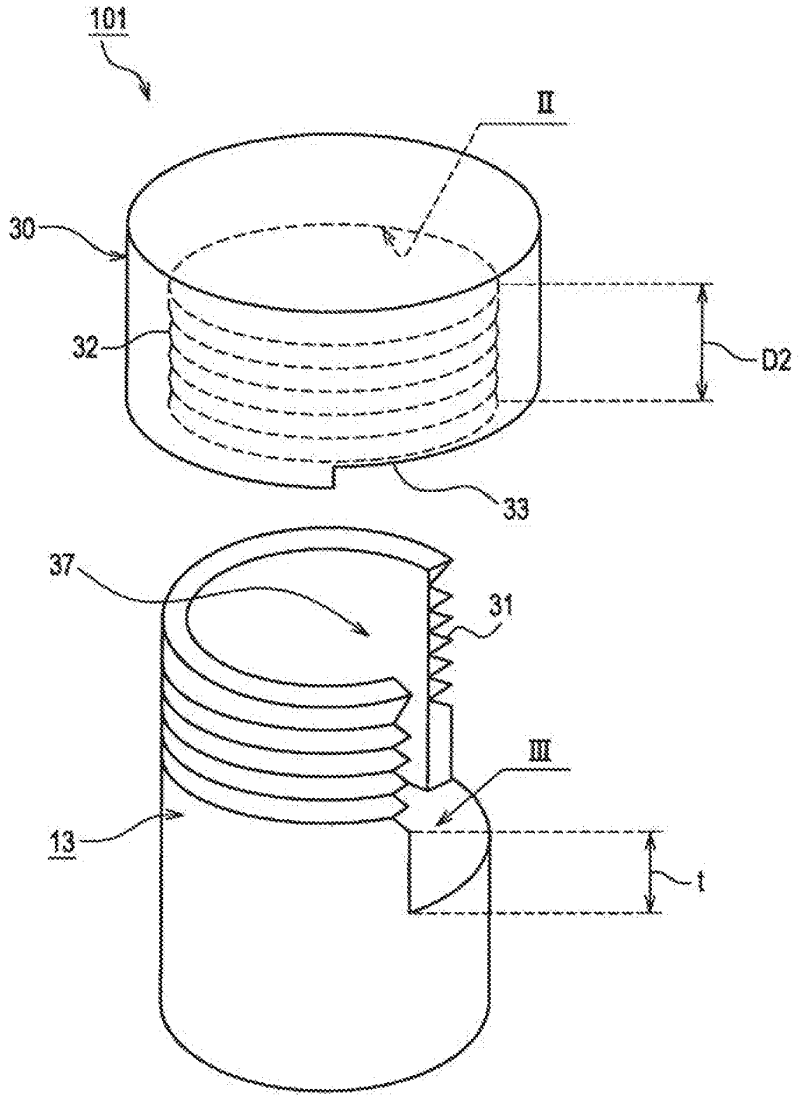


FIG.4

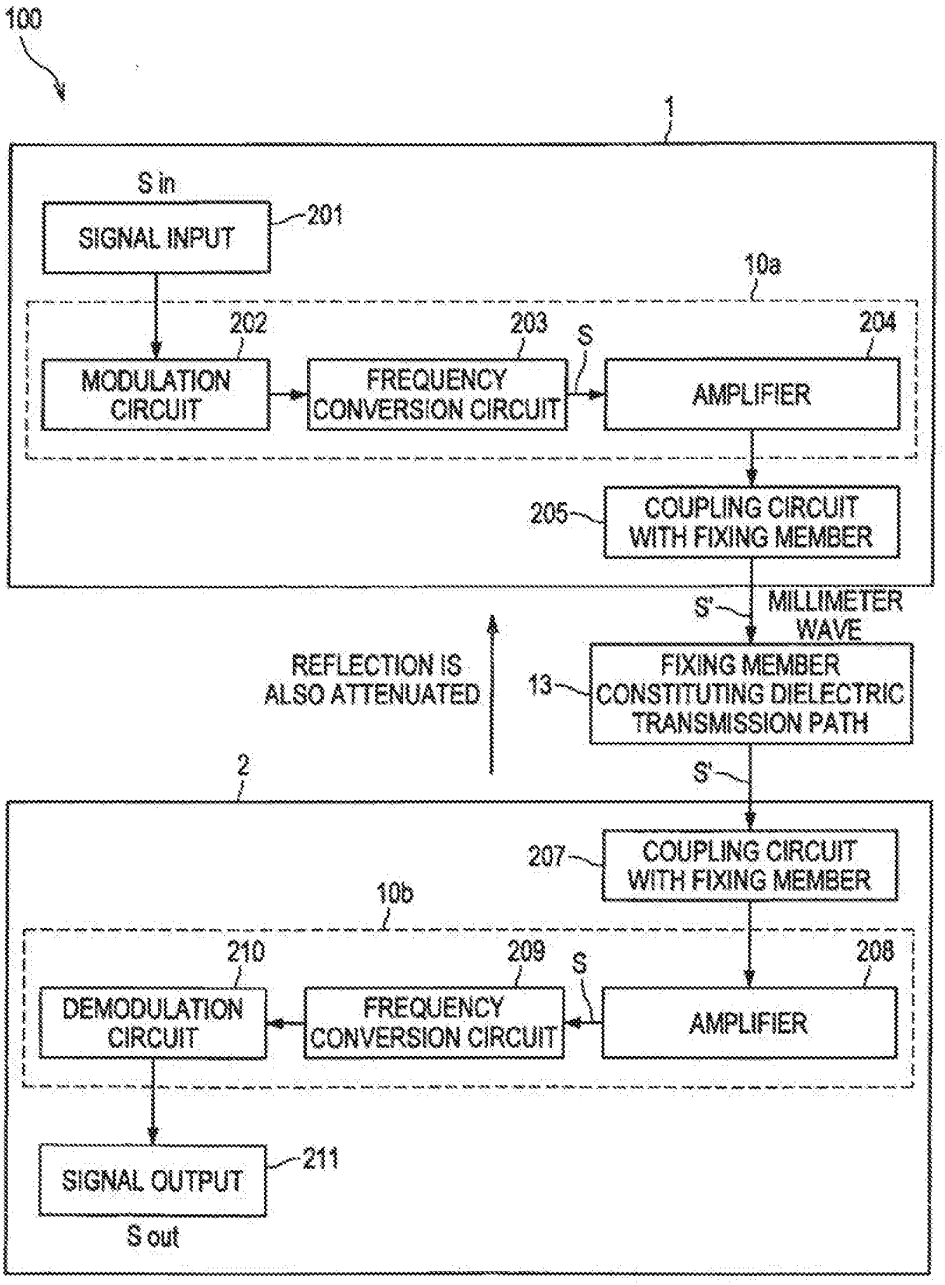


FIG.5

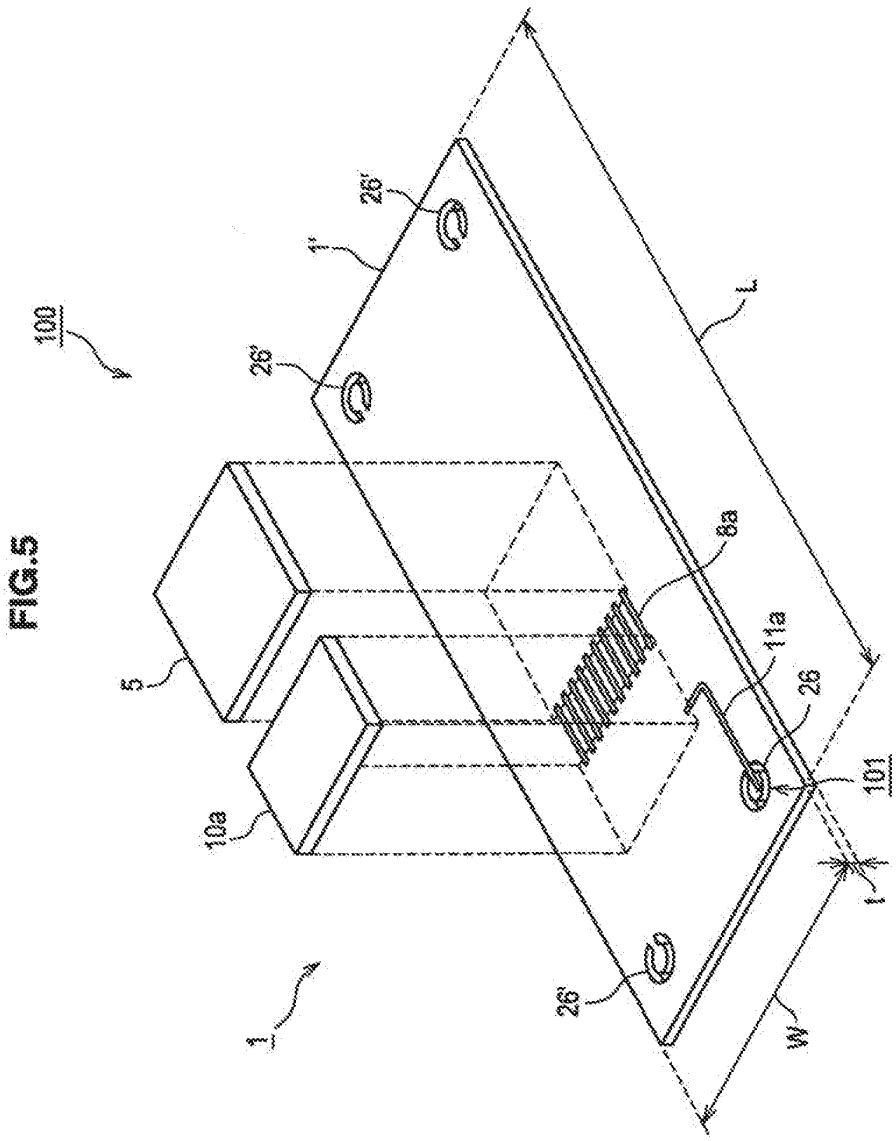


FIG.6

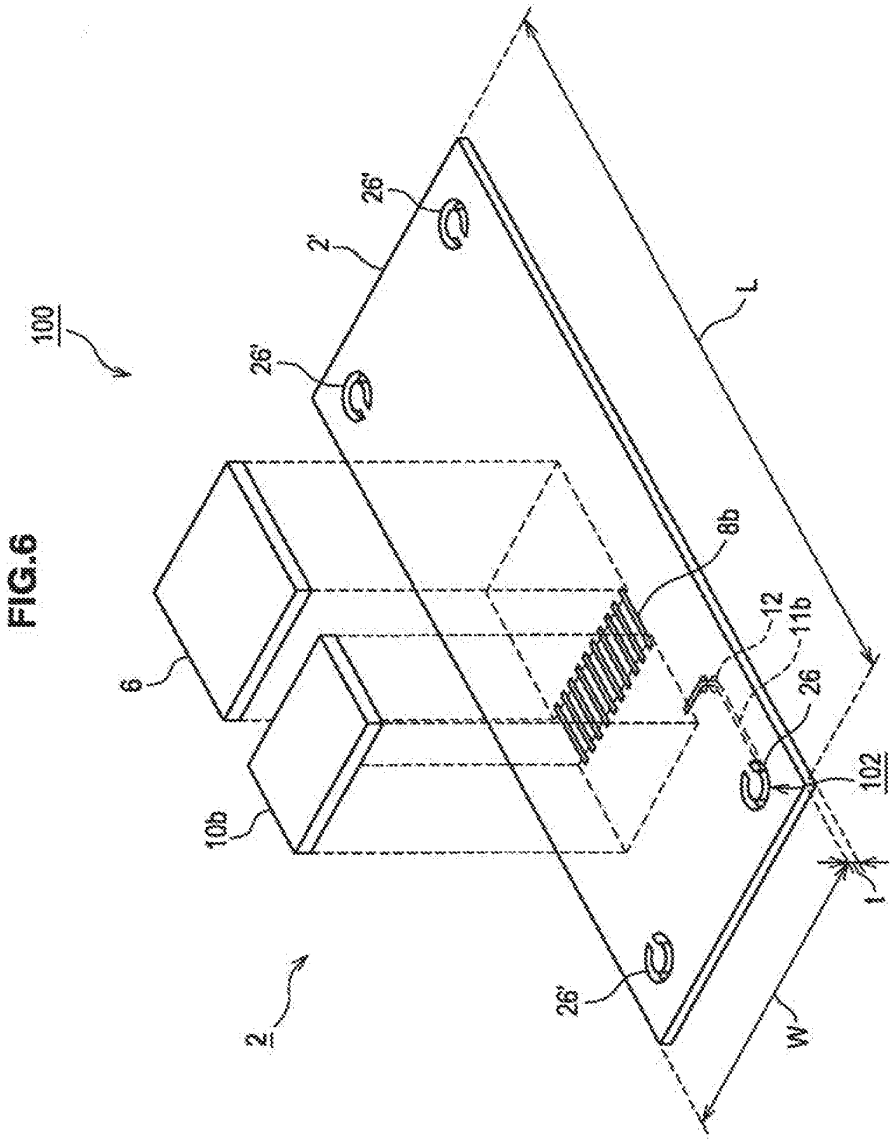


FIG.7

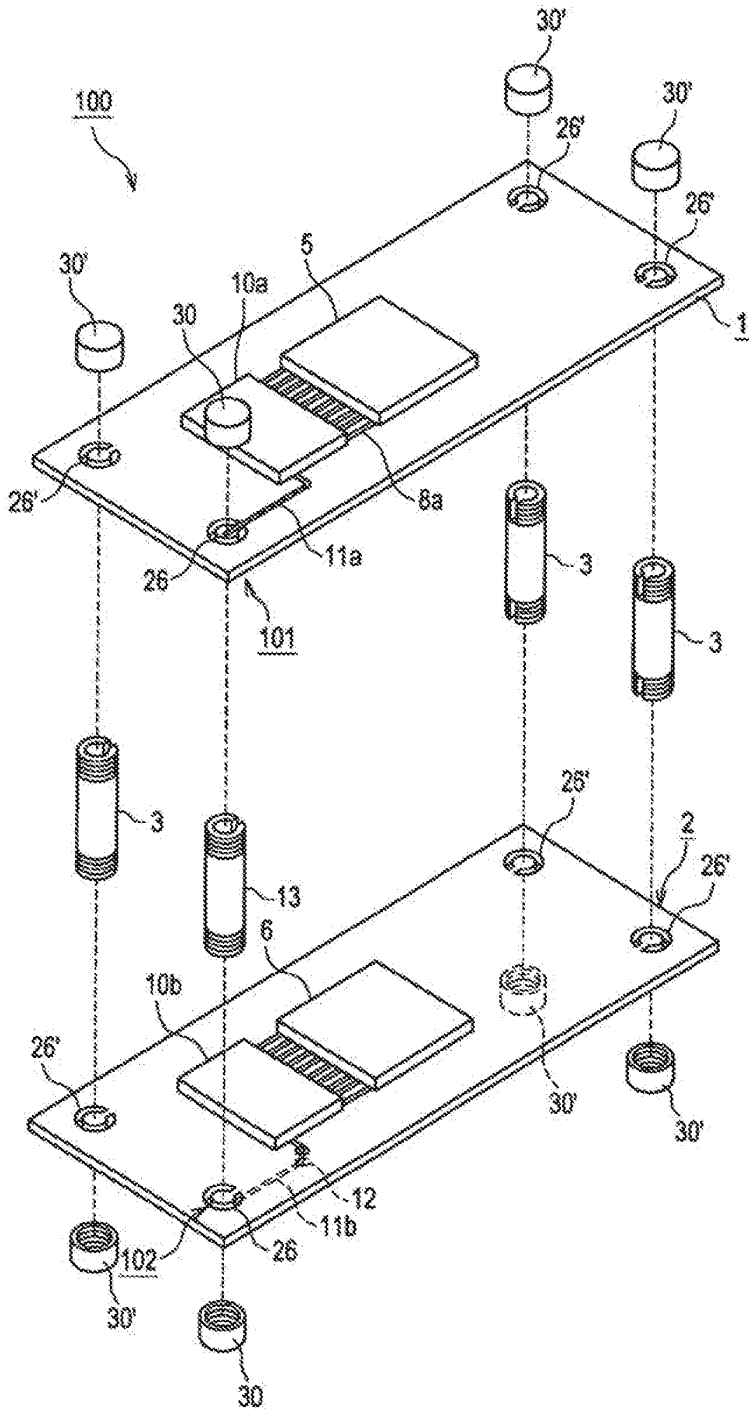

100
30'
30'
26'
26'
30'
5
10a
30
1
26'
6a
11a
26
101
3
3
3
26'
2
26'
13
6
10b
26'
30'
30'
12
11b
26
102
30'
30

FIG.8

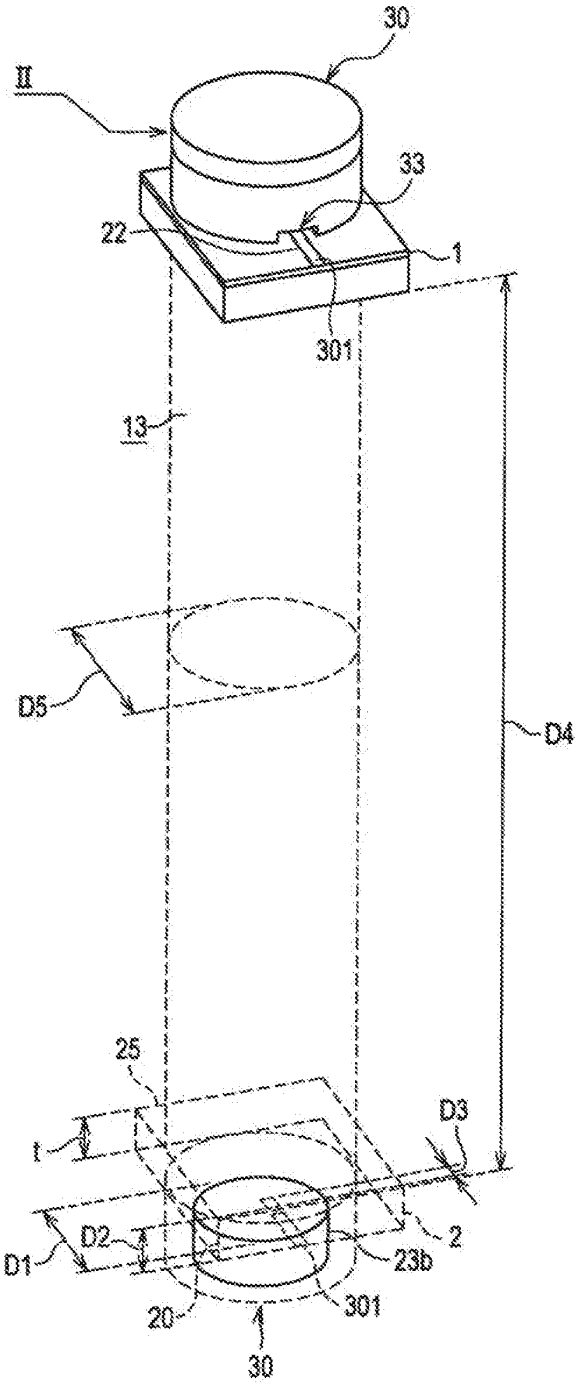


FIG.9

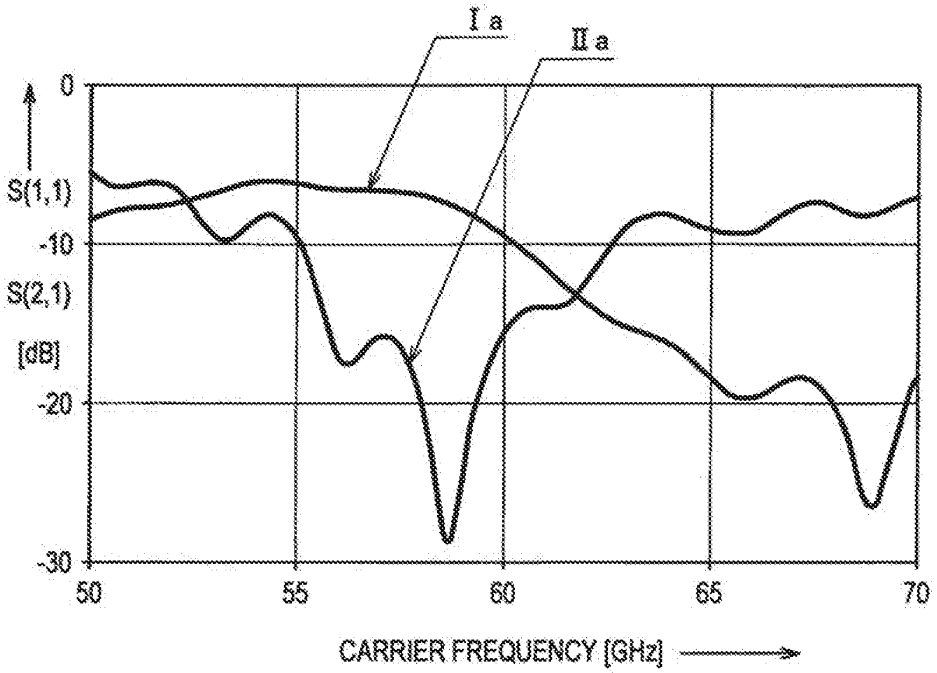


FIG.10

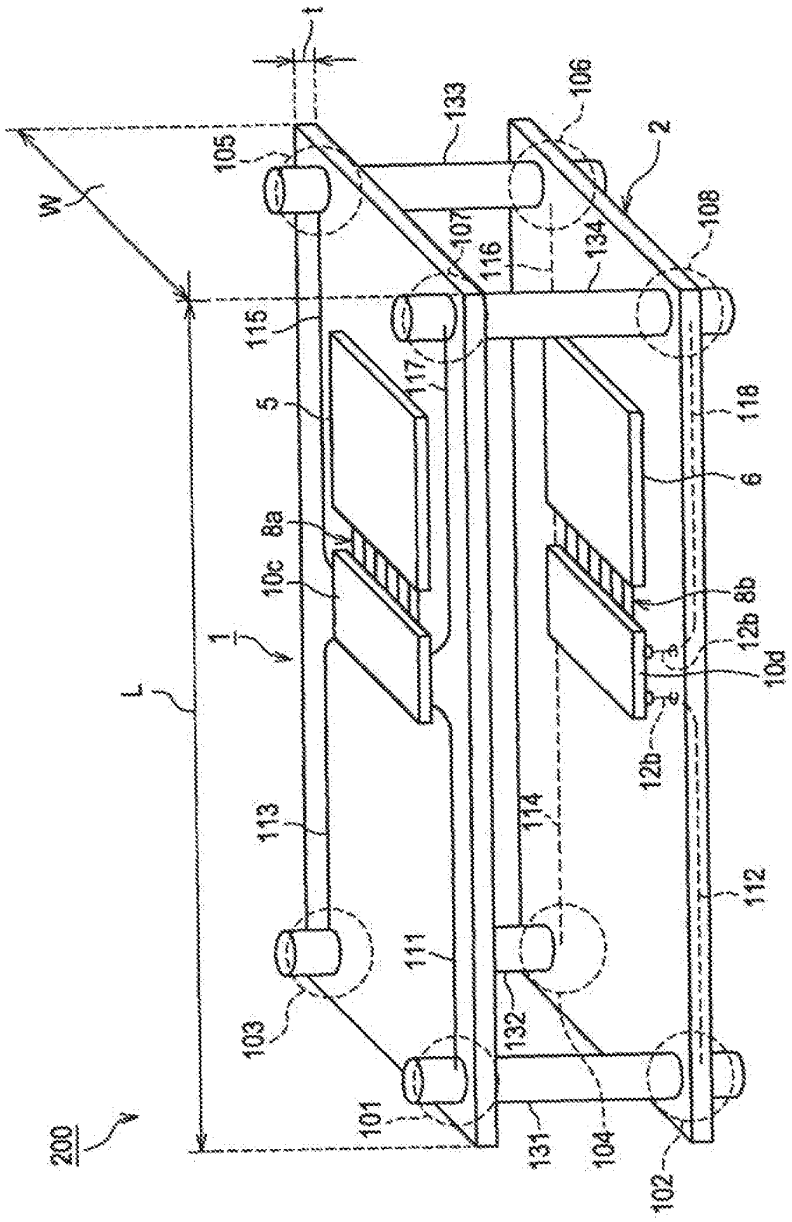


FIG.11

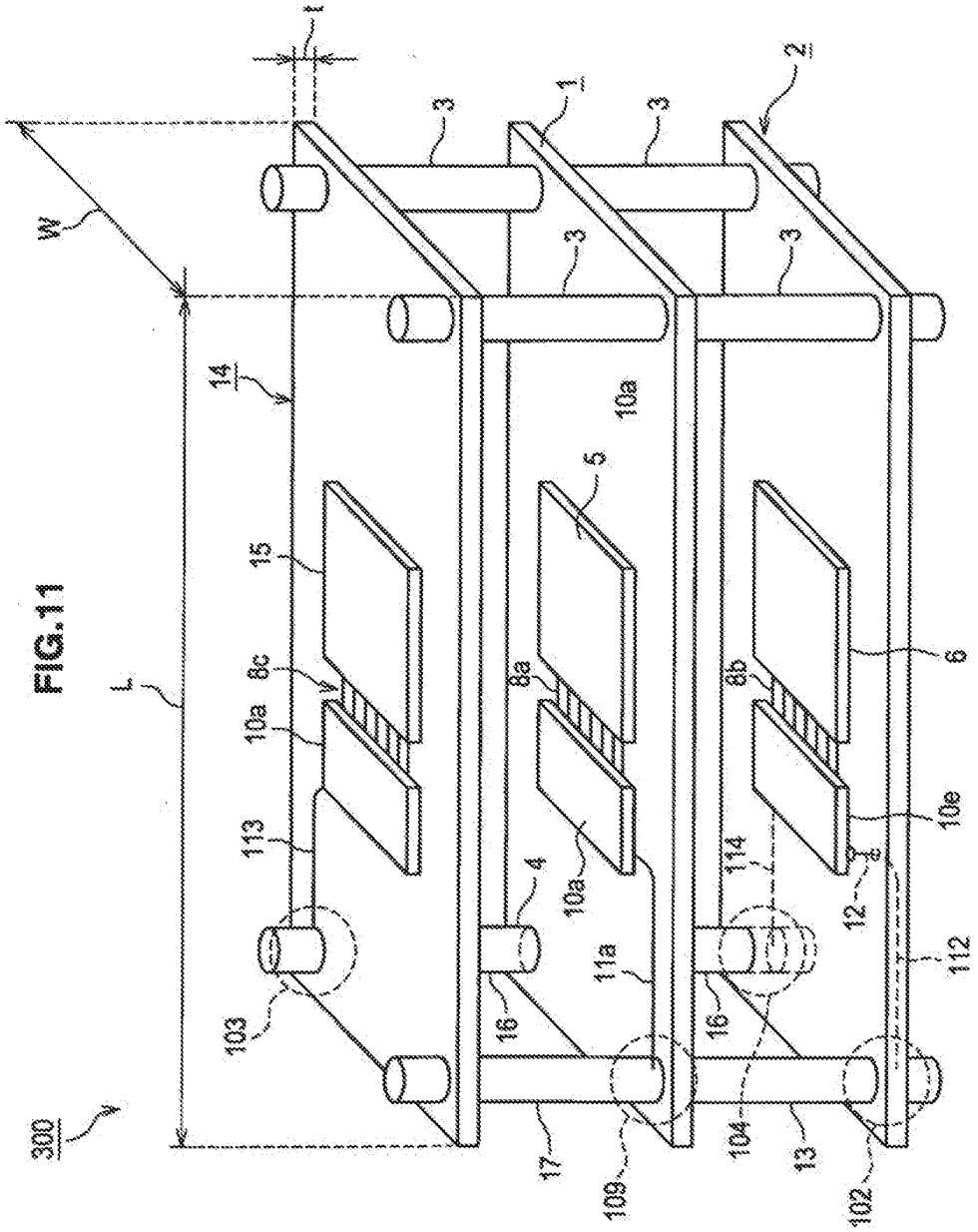


FIG12

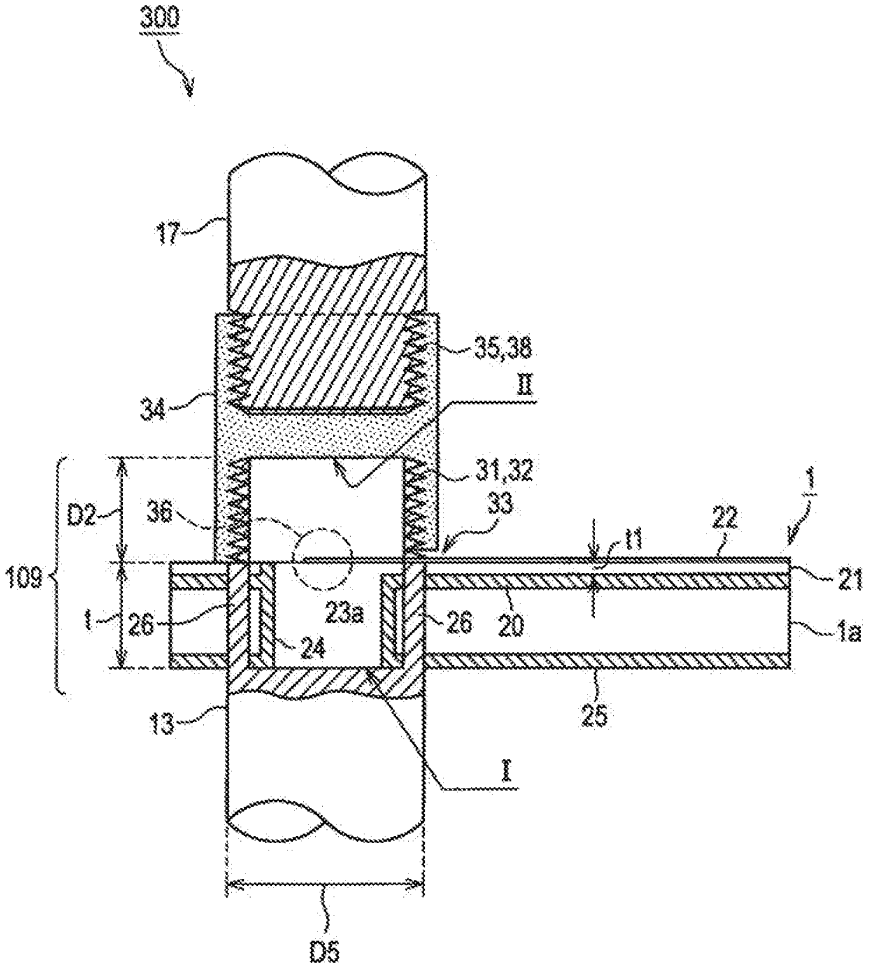


FIG.13

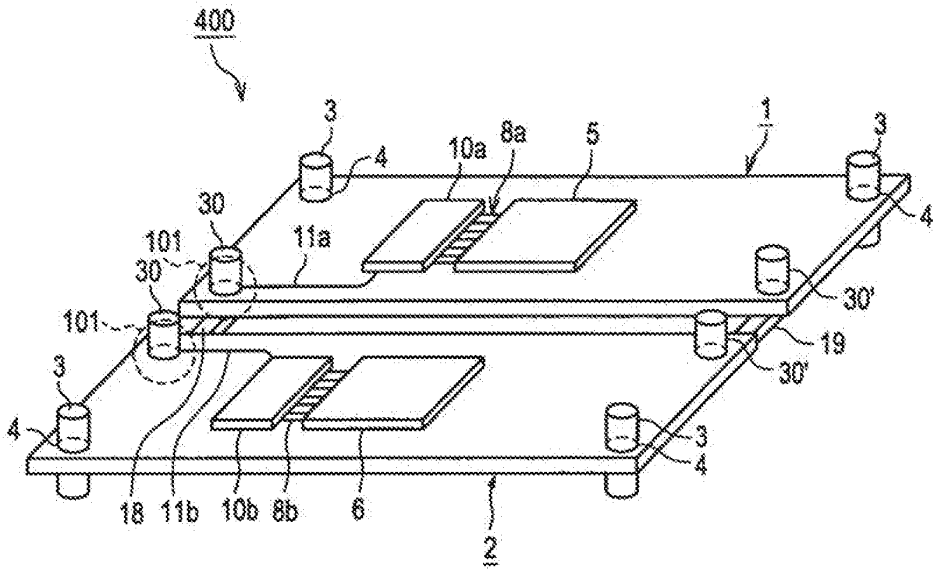


FIG.14

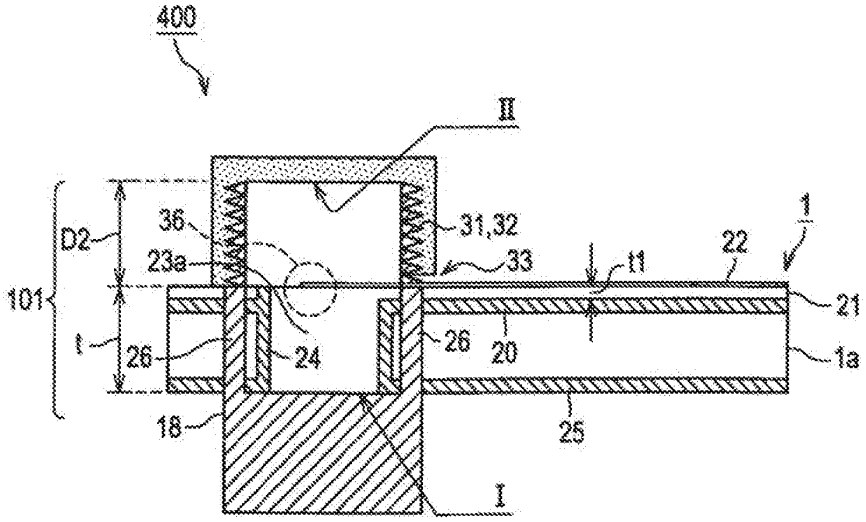


FIG.15

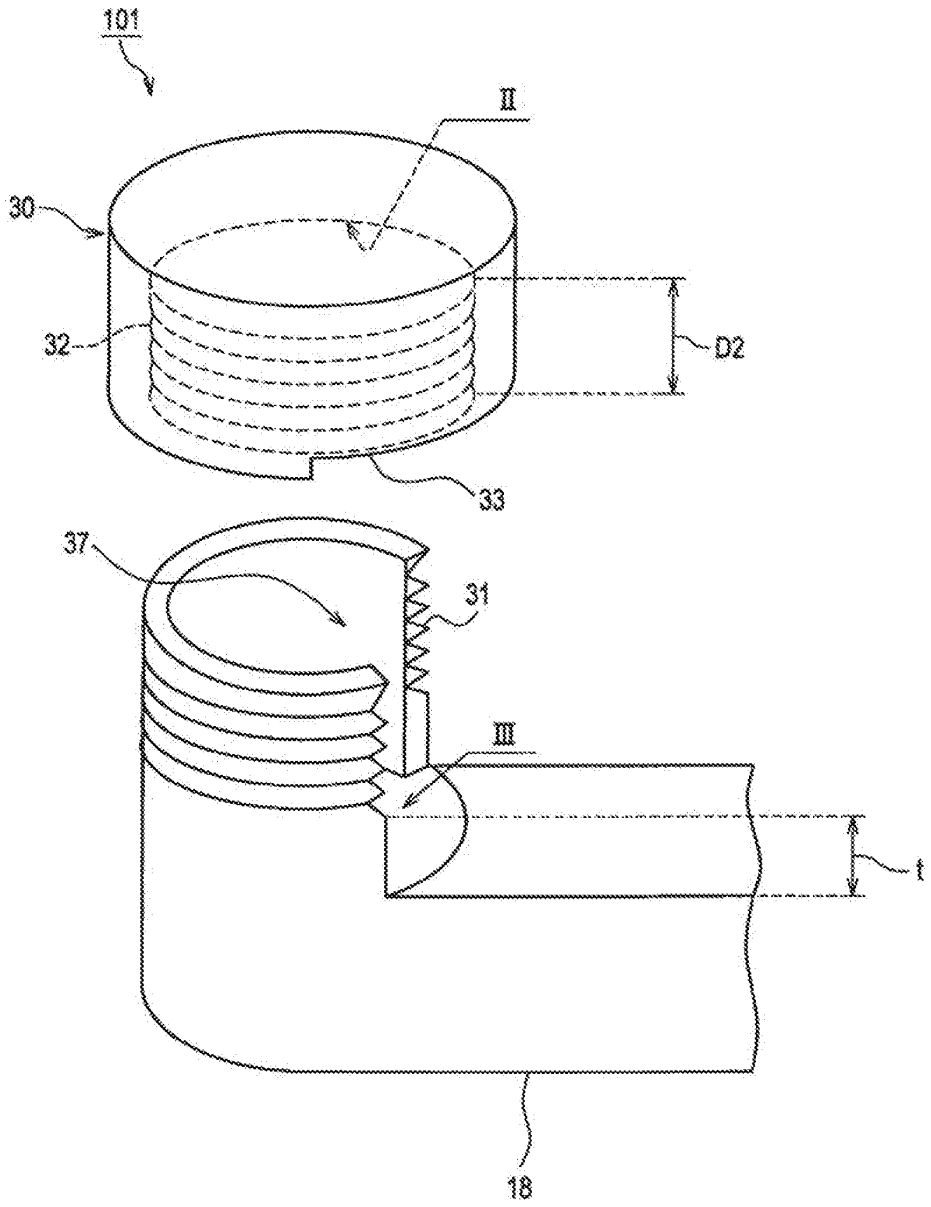


FIG.16

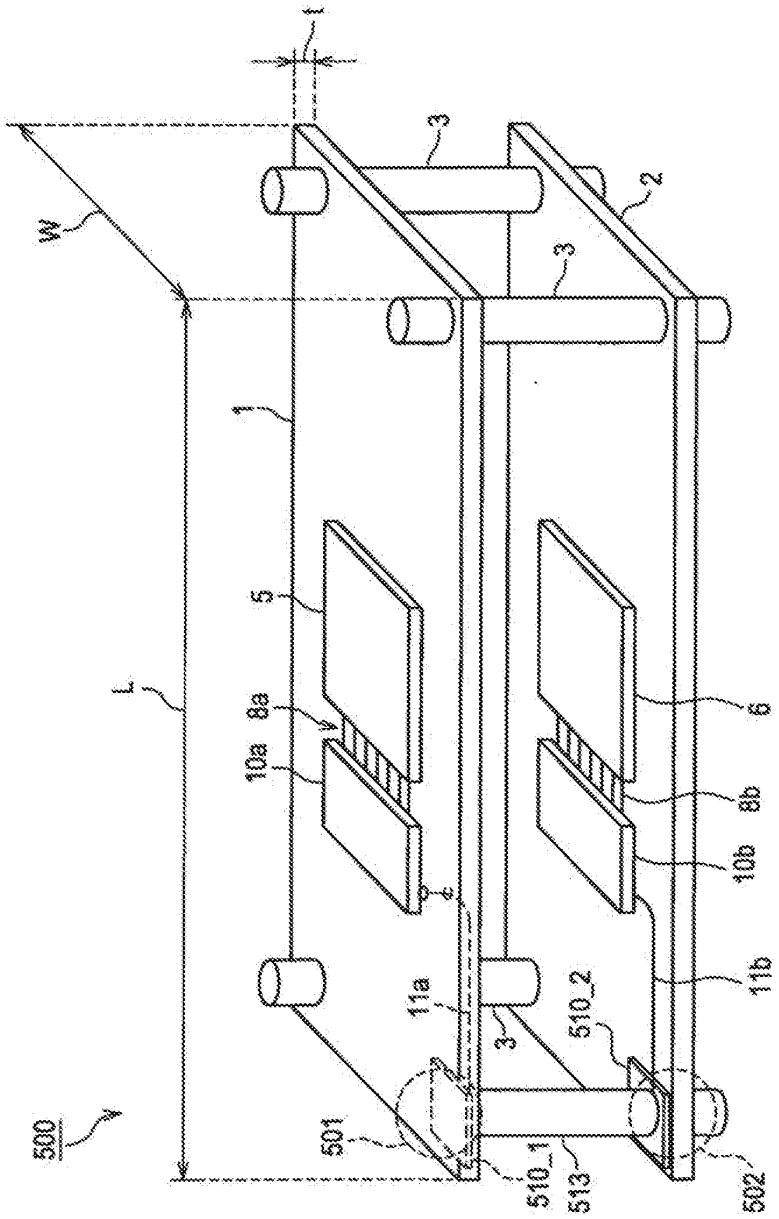


FIG.17A

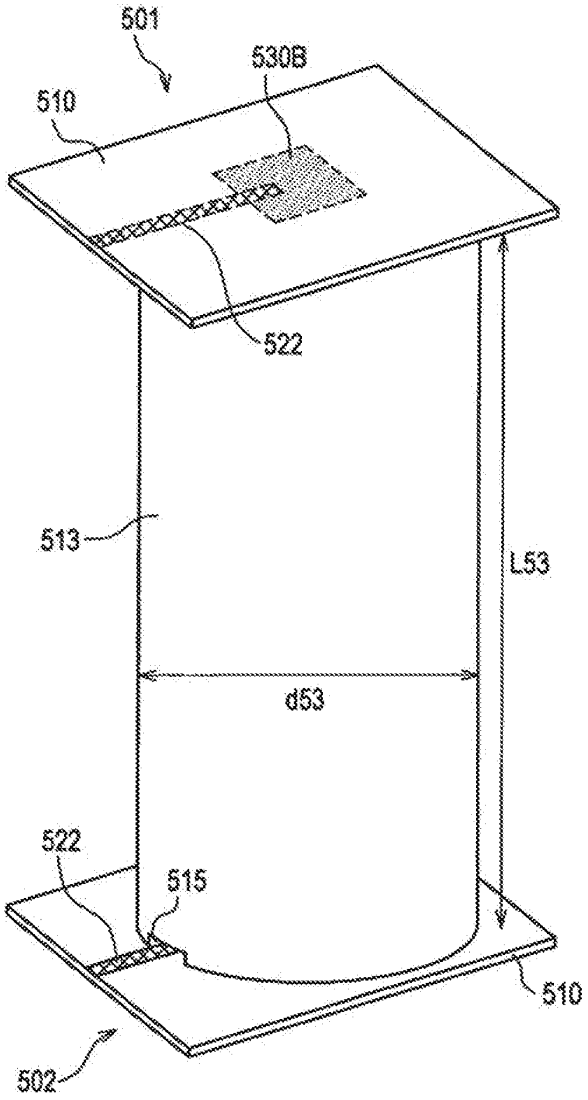


FIG.17B

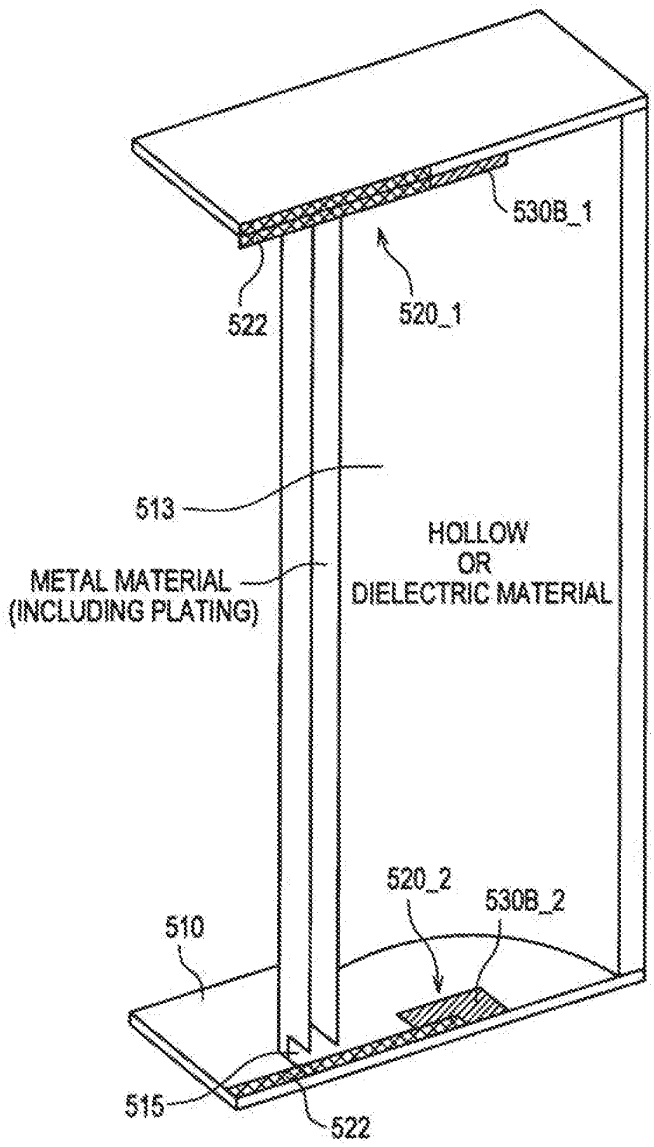

530B_1
522
520_1
513
HOLLOW
OR
DIELECTRIC MATERIAL
METAL MATERIAL
(INCLUDING PLATING)
520_2
530B_2
510
515
522

FIG.17C

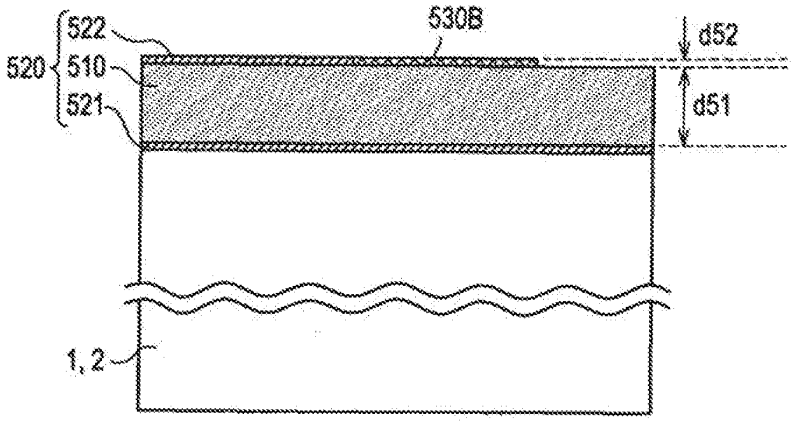


FIG.17D

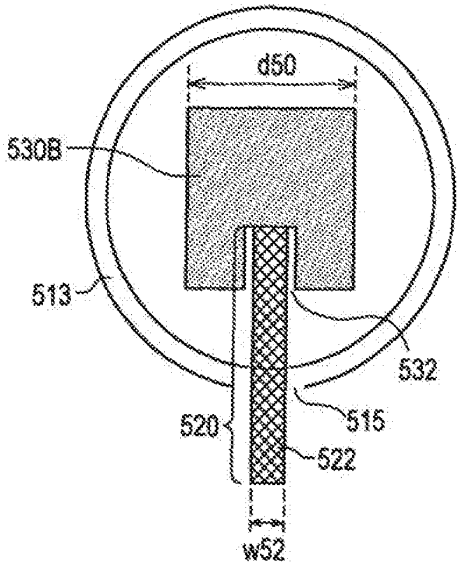


FIG.18

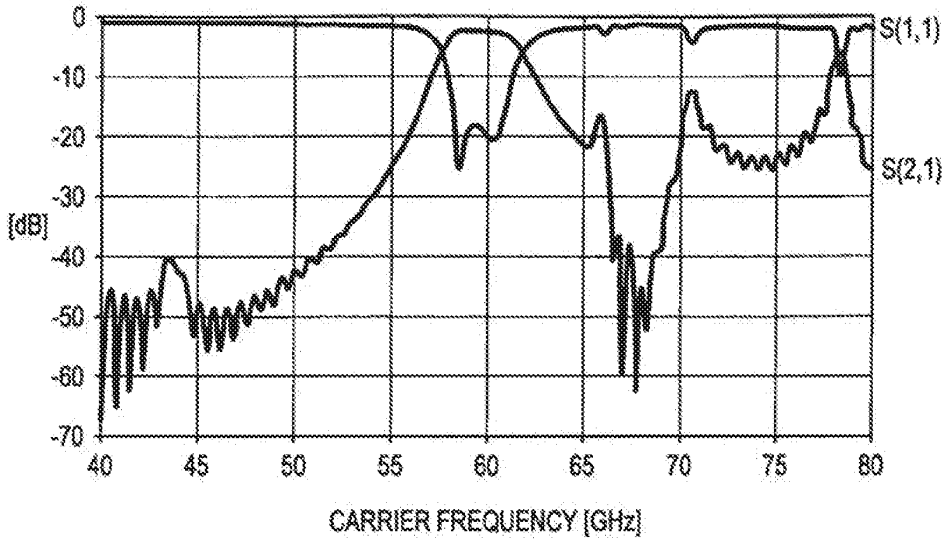


FIG.19A

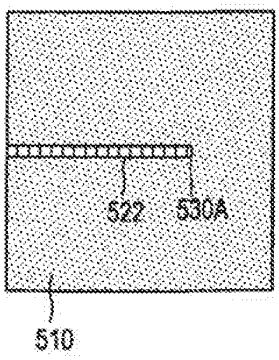


FIG.19B

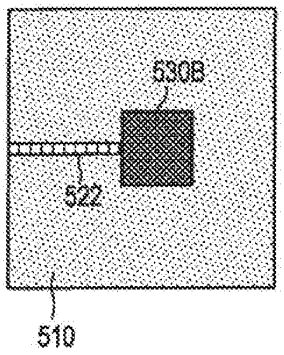


FIG.19C

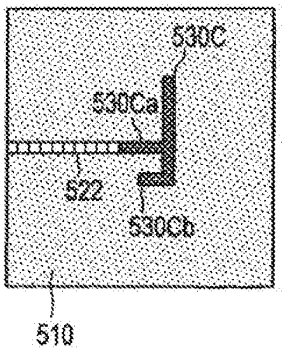


FIG.19D

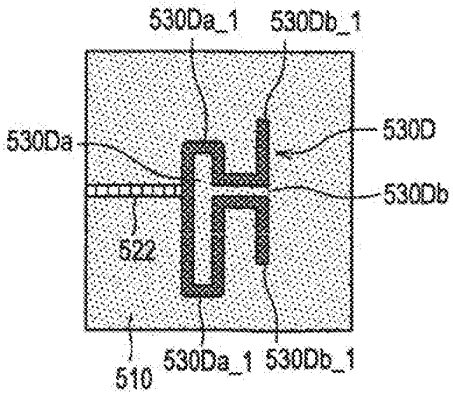
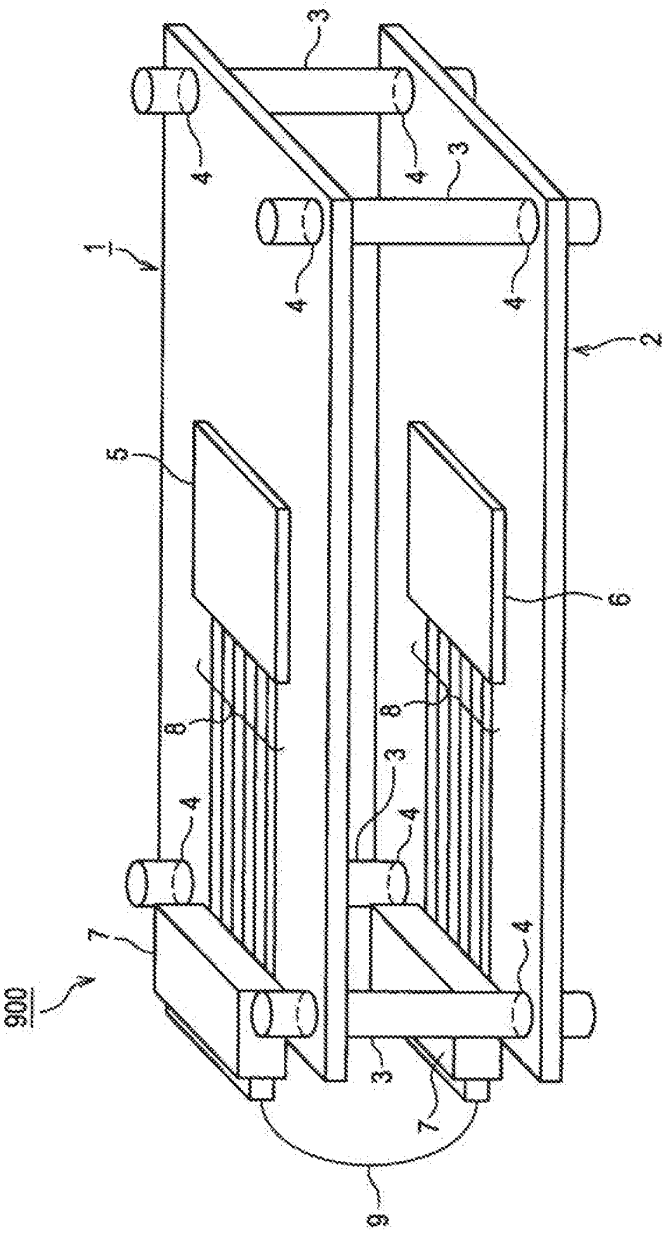


FIG.20



INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2009/066090

A. CLASSIFICATION OF SUBJECT MATTER
H01P5/107(2006.01)i, H01P3/16(2006.01)i, H01P5/08(2006.01)i, H04B3/52(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01P5/107, H01P3/16, H01P5/08, H04B3/52

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Jitsuyo Shinan Koho 1922-1996 Jitsuyo Shinan Toroku Koho 1996-2009
Kokai Jitsuyo Shinan Koho 1971-2009 Toroku Jitsuyo Shinan Koho 1994-2009

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 8-8618 A (NEC Corp.), 12 January 1996 (12.01.1996), entire text; all drawings (Family: none)	1-20
A	JP 2007-251394 A (Sony Corp.), 27 September 2007 (27.09.2007), entire text; all drawings & US 2007/0215913 A1 & KR 10-2007-0093838 A	1-20
A	JP 2008-99235 A (Sony Corp.), 24 April 2008 (24.04.2008), entire text; all drawings & US 2008/0153416 A1 & EP 1898532 A2 & SG 141315 A & EPA PI0703527 & KR 10-2008-0023630 A & CN 101145810 A	1-20

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
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"E" earlier application or patent but published on or after the international filing date
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
16 December, 2009 (16.12.09)	28 December, 2009 (28.12.09)
Name and mailing address of the ISA/ Japanese Patent Office Facsimile No.	Authorized officer Telephone No.

Form PCT/ISA/210 (second sheet) (April 2007)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2009/066090

C (Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 11-308021 A (NEC Corp.), 05 November 1999 (05.11.1999), entire text; all drawings (Family: none)	1-20
A	JP 56-103501 A (Fujitsu Ltd.), 18 August 1981 (18.08.1981), entire text; all drawings (Family: none)	1-20
A	JP 8-288738 A (Daewoo Electronics Co., Ltd.), 01 November 1996 (01.11.1996), fig. 7, 8; paragraphs [0032] to [0033] & US 5717407 A & EP 735611 A2 & CN 1138759 A	1-20

Form PCT/ISA/210 (continuation of second sheet) (April 2007)

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- JP 2004220284 A [0009]
- JP 4077847 B [0009]

Espacenet

Bibliographic data: TW200938017 (A) — 2009-09-01

Printed circuit board coil

Inventor(s): BAARMAN DAVID W [US]; SCHWANNECKE JOSHUA K [US]; GUTHRIE WARREN E [US]; WAHL RICHARD A [US]; DUCKWORTH PAUL [US] ± (BAARMAN, DAVID W, ; SCHWANNECKE, JOSHUA K, ; GUTHRIE, WARREN E, ; WAHL, RICHARD A, ; DUCKWORTH, PAUL)

Applicant(s): ACCESS BUSINESS GROUP INT LLC [US] ± (ACCESS BUSINESS GROUP INTERNATIONAL LLC)

Classification: **- international:** ***H05K1/16***
- cooperative: **H01F5/003**; **H05K1/165**; H05K1/0228; H05K2201/097

Application number: TW20080136804 20080925

Priority number(s): US20070975953P 20070928 ; US20080044298P 20080411

Also published as: AU2008308975 (A1) CA2697440 (A1) CN101810062 (A) EP2201826 (A2) JP2011504289 (A) more

Abstract of TW200938017 (A)

A multilayer printed circuit board ("PCB") coil that simulates a coil formed from litz wire. The PCB includes a plurality of alternating conductor and insulating layers interconnected to cooperatively form the coil. Each conductor layer includes a trace that follows the desired coil shape and is divided into a plurality of discrete conductor segments. The segments are electrically connected across layers to provide a plurality of current flow paths (or filaments) that undulate between the layers in a regular, repeating pattern. The coil may be configured so that each filament spends a substantially equal amount of time in proximity to the paired coil and therefore contributes substantially equally to the self or mutual inductance of the coil. Each conductor layer may include a plurality of associated traces and intralayer connector that interconnected so that each filament undulates not only upwardly/downwardly, but also inwardly/outwardly in a regular, repeating pattern.

(19)中華民國智慧財產局
(12)發明說明書公開本　(11)公開編號：200938017
(43)公開日：中華民國98(2009)年9月1日

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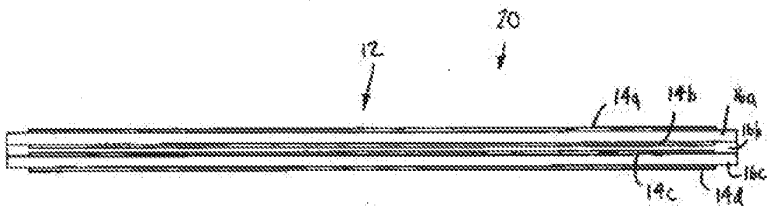
(54)名稱
印刷電路板線圈
PRINTED CIRCUIT BOARD COIL
(57)摘要

一種多層印刷電路板(PCB)線圈，其模擬李茲線(litz wire)所形成之線圈。該PCB包含多數個交流導體及絕緣層，其交互連結並共同形成線圈。每一導體層包含一軌跡，其連續所要的線圈形狀並加以分割成為多數個各別的導體片段。該片段係橫跨層體加以電連接，提供多數個電流通道(或長絲)，在層體間以規則重複的式樣起伏。線圈可加以構形以致每一長絲花費實質相等的時間接近或封線圈，因而提供實質相等於自身或線圈的交互感應。每一導體層可包含多數個相伴的軌跡及層內交連的連接器，以致每一長絲不止向上/向下起伏，也以規則而重複的式樣向內/向外起伏。



12：多層電路板
14a-d：交流導體層
16a-c：絕緣層
20：印刷電路板(PCB)線圈

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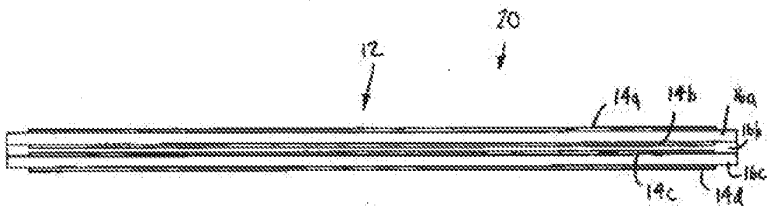

12：多層電路板
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【發明所屬之技術領域】

本發明有關電磁線圈，及更加具體地係有關多層印刷電路板電磁線圈。

【先前技術】

電磁線圈係使用於多種應用中，連接感應式電能傳輸器。例如，不同形式的電線圈係用於變壓器、感應式電能耦合器及馬達。在歷史上，電線圈已藉由纏結金屬絲股線成為一或更多之迴路而形成。典型地，線圈之直徑、金屬絲之種類及直徑、迴路之數量(或匝數，turns)，及其他金屬絲及線圈的特性係加以選擇，以提供所要的電磁能量傳輸特性。

已知的是，交流電具有一在導體內自我分佈之傾向，以致其靠近導體表面上的電流密度係大於其在核芯上者。該現象通常係指"趨膚效應"(skin effect)。趨膚效應造成導體之有效電阻隨著 AC 電流之頻率漸增。在克服趨膚效應之一努力中，高頻應用中的電磁線圈通常係由李茲線(litz wire)加以纏結。李茲線通常能以螺旋型式金屬線加以特徵化，其包含許多細線，各別地以絕緣膜加以塗覆並纏結在一起。個體金屬線係依循仔細地預定的式樣加以結合及纏結，通常牽涉數個纏結層次(已纏金屬絲族群係纏結在一起等)。典型地，金屬絲係加以纏結，以致每一個體股線花費實質相等的時間接近成對的線圈。因此，每一股線自成對的線圈截斷實質等量的磁通線並實質相等地貢獻自身或線圈之相互電感特性。由於分離之較小金屬線的結合，已結合之導體，相較於使用總橫斷面積之固態導體，具有較大的表面積，因而有下降的趨膚效應。依此結果及獨特的纏結構形，在高頻應用中，與李茲線線圈相伴隨的能量損失能實質地低於習用的固態金屬絲線圈。即使擁有這

點，李茲線承受數個缺點。首先，李茲線線圈的電阻係高於理論可取得者，因為個體股線係圈的並以絕緣體塗覆，以致全部的橫斷面包含一實質數量的非導體元件，例如，空氣及絕緣體。其次，成品結構係相對地較複雜的，及每一股線係加以打破。為保護股線，通常併入一外鞘。外鞘增加全部成本，及在相較於理論可取得值時，提供甚至更多的電阻。第三，導體係熱絕緣的及具有非攜熱路徑，遠離導體本身。如此，基於熱考量，能量處理能加以降低。第四，李茲線及李茲線線圈的製造過程，相對地係較為昂貴的，及需要特別的、昂貴的設備。第五，李茲線可能較大於所要的一些應用，此起因於金屬絲到金屬絲的包裝密度及股線間絕緣所佔據的空間。

金屬絲線圈在製造上係相對地較為昂貴的(尤其是李茲線線圈)，佔據相對較大量的空間，及通常需要機械安裝線圈至一印刷電路板。為了解決這些問題，已知直接地在印刷電路板上整合一線圈，例如，藉由在電路板上使用螺旋形狀的軌跡，形成軌跡。在某些應用中，印刷電路板包含多數層的螺旋軌跡，其藉由通道加以結合在一起，形成所要匝數的線圈(例如，2005 年七月五日頒給 Ferencz 等人的美國專利第 6914508 號)。雖然印刷電路板線圈能提供某些優點超越金屬線圈，但習用的印刷電路板線圈遭受某些習用固態金屬絲面對的問題，例如，在 PCB 線圈內所伴隨的感應電流不均勻分佈及電感的不均勻分佈。進一步地，已堆疊的 PCB 線圈能引入不想要的寄生電容(parasitic capacitance)，此起因於某些線圈相較於其他線圈，接收較多的磁場。最後，這造成較高的電阻及損失。

【發明內容】

本發明提供一種多層印刷電路板(PCB)線圈，其模擬李茲線

e)所形成之線圈。該 PCB 包含多數個交流導體及絕緣層。導體層交互連結，以致共同形成線圈。每一導體層包含一軌跡，其遵循所要的線圈形狀並加以分割成為多數個各別的導體片段。在一實施例中，每一 PCB 導體層包含一通常為螺旋形的軌跡，其具有多數個電分別的片段。該片段係橫跨層體加以電連接，提供多數個電流通道(或長絲)，在層體間以規則重複的式樣起伏。在一實施例中，線圈可加以構形以致每一長絲花費實質相等的時間接近成對線圈。因此，每一長絲提供實質相等於自身或線圈的交互電感。

在一實施例中，PCB 的層體包含實質共延伸的螺旋軌跡，其以重疊關係彼此重疊在一起。在這實施例中，軌跡可包含實質相同的片段，因而提供對齊的立體交叉道(interchange)，有助於不同層之片段的電耦合。

在一實施例中，不同層的片段係藉由在層體間延伸的通道(vias)在立體交叉道加以電耦合。每一立體交叉道可特別的塑形，以降低靠近通道的阻礙。在一實施例中，每一立體交叉道包含一分離的通道，用於每一導體層。例如，一四層的 PCB 線圈可包含四個通道。在其他實施例中，某些或全部的導體層可包含多數個通道。

如前所述，長絲在多數個導體間加以向上及向下地起伏。此外，在一實施例中，長絲可向內及向外地起伏，提供額外的移動程度。在一實施例中，每一層的線圈可包含兩個相鄰的、分段的、實質地平行螺旋形式的軌跡，其以成對關係加以延伸。在這個實施例中，線圈可包含層間及/或層內的連接器，其連接不同層的及成對軌跡的片段，其連接的式樣界定多數個向上/向下及向內/向外地起伏的長絲，以致每一股線花費實質相等的時間接近成對的線圈。每一長絲向上/向下及向內/向外地起伏，模仿李茲金屬絲線圈

 且曲本質。

本發明提供一簡單及有效的PCB線圈，其克服習知PCB線圈的數個重要缺點，同時維持許多PCB線圈的優點。多重的、起伏的電流通道之存在，相較於習知PCB線圈，降低趨膚效應及有較低的損失。使用片段及層間連接器，提供一可信賴的起伏式樣。此外，長絲的起伏式樣提供一線圈，其中每一長絲花費實質相等的時間接近成對的線圈，這進一步地改良線圈的效率，因為每一長絲提供實質相等於自身或線圈的交互電感。本發明也能以向內/向外起伏加以製造，進一步地模仿李茲線線圈股線的電流通道。使用片段及層間導體能降低寄生電容，其藉由 1)降低線圈表面積至片段表面積；及 2)引入邊緣效應(fringe effects)，其取消每一其他的流出。較低的電容允許在線圈內的電感加以放大，其造成較低的電阻及較小的損失。這些優點係全部加以提供於一PCB線圈，其線圈較薄，並且相較於較大的李茲線線圈，允許較緊密的耦合。

本發明這些及其他目標、優點及特徵，在參考本實施例之詳細描述及附圖之下，將更易於瞭解。

【實施方式】

依照本發明一實施例的印刷電路板(PCB)線圈20，係顯示於第一A圖、第一B圖及第一C圖。PCB線圈20通常包含多數個交流導體層14a-d，及絕緣層16a-c，其共同合作地形成一多層線圈(見第一A圖)。每一導體層14a-d包含一軌跡52a-d，其由多數個各別的片段18(見第一B圖)加以界定。在不同導體層14a-d之不同軌跡52a-d之片段18，由連接器40加以交連，界定"長絲" 54a-d(各別的電流通道)，其以預定式樣在層間加以起伏(見第一C圖、第六及七圖)。預定的式樣係加以設計，以致在PCB線圈與一第二感應性線圈加以成對時，在長絲54a-d之間，實質地均勻地分佈所感應的

主所示的實施例中，PCB 線圈 20 模仿一李茲線線圈，其中該長絲 54a-d 雖然偏移，但遵循實質地平行的起伏穿透導體層 14a-d。在所示的實施例中，長絲 54a-d 依照實質地規則的、重複的起伏，連同每一長絲 54a-d 花費實質地相同的總時間於 PCB 線圈 20 的每一層 14a-d。起伏通常充足地發生，以致所有長絲 54a-d 從成對的線圈(未示)截斷一實質相等的磁通線，因而，感應式地產生實質等量的電能及呈現實質等量的電感。在所示的實施例中，每一長絲 54a-d 通過每一層約 4 次，但起伏的數量係在各應用之間可加以改變。

雖然顯示與四層 PCB 線圈相關，本發明係非常適合且易於改編而用於不同層數的 PCB 線圈。例如，一較大或較小數量的層係可加以使用，提供一具有所要特性的線圈。在較大數量層體之應用中，揭示於此的片段連接式樣，能加以攜帶至額外的層中，或能開發可替換的連接計劃圖。每一層體中，軌跡及片段的尺寸、形狀及構形，係可加以改變，以提供所要特性的 PCB 線圈。例如，本發明係以相關於一般橢圓形的線圈加以圖解。線圈的形狀在各應用間可依照需要加以改變。例如，本發明能加以應用於一圓形的、矩形的、方形的、及不規則形的線圈。

本發明係相關於一無核 PCB 線圈加以顯示。本發明能併入成對的線圈組，其包含核芯，如磁核。例如，PCB 線圈可在線圈中心界定一尺寸充足的穿孔，以接收一核芯(未示)。該核芯可分離地製造，並在總成時安裝在穿孔中。如果需要，一層磁性材料，例如，鐵磁材料或鐵氧磁材料，可加以併入 PCB 基材中，以致 PCB 基材有效地作為一隔離體，以迂迴電磁場。如果需要的話，本發明可併入撓性的電路板設計。在一撓性的電路板設計中，撓性的導體層及絕緣體層可加以安置於一撓性基材上。撓性的電路設計

雖然未示，與PCB線圈共同使用的電/電子元件，可安置在載有PCB線圈之相同的PCB總成之上。本發明可加以使用於基本上任何應用中，取代金屬絲線圈或一習用的PCB線圈。在某些應用中，PCB 線圈在一耦合的成對線圈中，可取代兩線圈。在其他應用中，PCB 線圈可與習知線圈加以使用，如習知的金屬絲線或習知的PCB線圈。

基於本發明的緣故，指示性的詞包，如"頂"、"底"、"上"、"下"，係用於指稱相關於圖式中所示之PCB線圈定位的方向。相似地，"向內"及"向外"係用於指稱朝向或遠離線圈中心的方向。這些詞句係權宜使用，描述所示之實施例，並不打算限制本發明實施於任何具體之定位。

如可能最佳地示於第一B圖中者，PCB線圈20係併入一多層電路板12中。多層電路板12可依照任何適當的技術及用於製造多層電路板之技術而加以製造，包含剛性及撓性電路板結構。第一B圖之PCB線圈20係由多數個導體層14a-d加以界定，其由絕緣層16a-c加以彼此隔離。導體層14a-d及絕緣層16a-c可為基本上任何材料，其適合用於製造多層電路板者。在所示的實施例中，每一導體層14a-d係藉由薄銅層沉積在電路板基材材料層(如纖維玻璃)之主要表面上而形成。導體層能加以沉積在電路板基材材料層之兩個主要表面上，以致兩個軌跡能施加到單一的電路板基材材料層上。在需要兩個以上導體層之應用中，額外的軌跡能加以安置在額外的電路板基材材料層上。電路板基材材料層能加以堆疊在一起以形成多層的 PCB。當包含有多數個電路板基材材料層時，鄰近層可由額外的絕緣層加以分離，如薄的纖維玻璃層。若想要的話，多種PCB線圈的傳導及絕緣層能加熱並加壓在一起，

一的多層 PCB。例如，多層 PCB 可使用習知的積層技術及設備加以製造。可更換地，PCB 線圈可使用分離的印刷電路板基材堆疊加以製造，其已由絕緣層加以分隔，並且機械式地交連，例如，藉由螺絲(未示)。

在所示的實施例中，導體層 14a-d 包含通常相同的軌跡 52a-d。第二 A~二 B 圖顯示該軌跡 52a-d，用於依照本發明之一實施例製造四層的 PCB 線圈 20。第二 A 圖顯示 PCB 線圈 20 之第一及最上層的一螺旋軌跡 52a。第二 B 圖顯示第二層用的螺旋軌跡 52b。第二 C 圖顯示第三層用的螺旋軌跡。最後，第二 D 圖顯示第四及最下層之軌跡 52d。雖然通常係相同的，在軌跡 52a-d 之間有些許差異。例如，片段 18 可在層體間加以偏移，有助於不同層之片段 18 間的交連。假使螺旋軌跡 52a-d 係通常相同的，則只有最上的螺旋軌跡 52a 加以詳細描述。其餘的軌跡 52b-d 可分離地敘述至必須的範圍，以敘述最上軌跡 52a 之變型，有益於具體討論。如所示者，最上螺旋軌跡 52a 包含多數個導體片段 18，其排列成一通常為橢圓、螺旋之式樣。在軌跡 52a 中的片段 18 係電導材料之細長的片段，其彼此地分隔，以致全部均電絕緣(見，例如第 2A~ 2D 圖)。每一其餘的軌跡 52b~d 包含實質相同的片段 18 排列。當導體層 14a-d 及絕緣層 16a-c 係結合時，軌跡 52a-d 係實質地共存的。

如前文所述，不同導體層 14a-d 之片段 18 係由連接器 40 加以電交連，其將片段 18 鍵在一起而界定長絲 54a-d(在下文中更詳細地描述)。在所示實施例中，層間連接器 40 係安置在立體交叉道 22 上，其位在每一片段 18 的相對端上。如可能最佳地顯示於第七圖者，軌跡 52a-d 係在立體交叉道 22 上加以構形，以致片段 18 重疊而允許使用基本上習知之通道 24，交連不同層內的片段 18。所示實施例的最下層包含一立體交叉道，其有較複雜的形狀。最下

交叉道包含分流部 60 及 62，有助於連接最下層片段 18 的外端至最上片段的內端。通道 24 係加以排列，依照一如下文所述之式樣，從層 14a-d 之間垂直地從一層延伸至一層。每一通道 24 通常包含一穿孔 26，其穿過絕緣材料而界定，及導體 28，延伸經過穿孔 26，提供一電流通道經過該絕緣材料。通道 24 之形成，可由打洞穿過電路板堆疊形成穿孔 26，然後以銅電鍍穿孔 26 而形成導體 28。例如，可使用電鍍、無電鍍或其他電鍍技術。雖然每一通道 24 可垂直地延伸經過所有的層 14a-d，但通道 24 係只連接至那些需要電連接以產生所要電流式樣的片段 18。關於想要的電連接的片段 18，通道穿孔打洞方法將在通道穿孔 26 內暴露出片段 18 的一部份。因此，當導體 28 係添加到通道 24 時(例如，鑽出的孔以銅加以電鍍)，在片段 18 及通道 24 之間將形成一電連接。關於不想要的電連接的片段 18，片段 18 可界定一絕緣穿孔 42，其將片段 18 及通道 24 加以隔離。如第七圖所示，絕緣穿孔 42 係與通道穿孔 24 連接，並具有一直徑大於相對應之通道穿孔 26。因為絕緣穿孔 42 相較於通道穿孔 26，具有一較大的直徑，所以導體 28 將不與片段 18 形成電連接。雖然所示通道 24 中的導體 28 係由電鍍的銅加以形成，導體 28 可由其他傳導材料加以形成。例如，一導體材料，如金屬絲的片段，可加壓貼合經過 PCB 線圈 20(未示)中的通道穿孔 24。

形成絕緣穿孔 42 而移除導體材料所造成的電阻增加，為解決該潛在問題，立體交叉道 22 可有一特別形狀。例如，如可能最佳地顯示於第三及第四圖中者，每一軌跡的放大部 44，可加以提供至絕緣孔 42 及通道 24 之周圍，以提供額外的電流導體區。在所示的實施例中，想要在相鄰迴路之軌跡中提供寬度降低之部份 46 時，軌跡係在絕緣孔 42 周圍加以放大至一程度。在第五圖中圖示

換的立體交叉道結構。在這個可替換的結構中，每一軌跡係加以放大於每一絕緣穿孔 42 的周圍，但並非每一通道 24。放大的區域係不嚴格地必須的，若想要時可加以除去。例如，在某些應用中，鄰近迴路間的空間可足夠地大，避免降低鄰近迴路之軌跡寬度的需要。在其他應用中，為絕緣穿孔 42 而移除導體材料所造成的電阻之影響，可為不充足的而確保放大區在軌跡 52a-d 中。

如前文所述，片段 18 係由連接器 40 加以交連，以界定一多數的長絲 54a-d，或各別的電流通道經過線圈。第一 C 圖顯示軌跡 52a-d，連同單一長絲的片段 18a(如長絲 54a)係加陰影。加陰影的片段 18 係順序地編號，從 S1 至 S78，以顯示片段電連的次序。例如，軌跡 52a 的片段 S1 係電連至軌跡 52b 的片段 S2，片段 S2 係電連至軌跡 52c 之片段 S3 等等，一直到片段 S78。第六圖係本發明所示實施例之電連設計的代表性示意圖，顯示所有四個長絲 54a-d 的部份，每一長絲 54a-d 具有不同的陰影。圖式係線圈 20 之七個長區的側視圖，並顯示由層間連接器 40 加以交連的不同層之片段 18。所示的連接設計係打算提供一線圈，其中長絲花費實質相等時間接近成對的線圈(例如，電感地耦合至 PCB 線圈之分離的線圈)，因而相似於李茲線金屬絲線圈內的股線，每一長絲 54a-d 截斷一實質等量的磁通線，進而電感地產生一實質地相等量的電流，並貢獻實質相等於自身或線圈之交互電感。這樣在不同長絲間提供實質均勻的電流分佈，進而降低損失並改良 PCB 線圈 20 的全體效率。這些優點係部份地藉由降低線圈中的電容而加以提供。並未因為堆疊的線圈之表面積係由一距離加以分離而產生相對較大之寄生電容，一相對較小的寄生電容藉由以一距離相隔之較小的表面積加以產生。進一步地，因為片段排列，某些由片段造成的電容邊緣效應，可彼此取消。較小的電容允許電感加以放

能造成較低的電阻及較小的損失。依此方式，PCB 線圈 20 模仿一李茲線線圈，但 PCB 線圈係較薄的，及相對於因為包裝密度而較厚的李茲線線圈，可允許較緊密的耦合。連接設計在各應用間係可改變，取決於 PCB 線圈及成對線圈之設計及構形。在所示的設計中，PCB 線圈 20 包含片段 18，其加以交連以界定四個長絲(或分離的電流通道)，從層體經由螺旋軌跡到層體 14a-d 間加以起伏，並具有實質相等量的片段 18 於每一層體 14a-d 上。不同的長絲 54a-d 係呈現在第六圖，並加不同的陰影。所有界定長絲 54a 的片段 18 及連接器 40 係在第六圖加以編號。為避免雜斑，每一其餘的長絲 54c-d 只有一片段 18 加以編號。相似於長絲 54a，其餘長絲 54b-d 係由相同陰影的所有片段 18 及所有交連相同陰影片段 18 之連接器 40 加以界定。當使用所示的連接設計時，長絲的編號將等於導體層 14a-d 的編號，然而，本發明並不限於依循此規則的連接設計。為了幫助揭示用於所示實施例之連接設計，每一片段 18 係界定為具有內端 18a 及一外端 18b。內端 18a 係為最接近螺旋中心的端點，及外端 18b 係為最遠離螺旋中心的的端點。只有一例外為，每一片段的內端 18a 係電連接至最近下層內片段之外端 18b。最低層 14d 上片段 18 之內端 18a 係電連接至最上層 14a 上片段的外端 18b。依照這個連接設計，每一長絲 54a-d，在移動一片段 18 接近線圈之最內端時，下降一層 14a-d。當長絲 54a-d 到達底層 14d 時，其跳回頂層 14a，同時移動一片段 18 接近線圈的最內端，然後重複該單層下降式樣。此式樣重複於螺旋線圈長度內之每一長絲 54a-d。結果，在所示的實施例中，每一長絲 54a-d 在頂層 14a 及底層 14d 之間重複地起伏，在移動時，依次地通過中間層 14b 及 14c。如能見到者，不同的長絲 54a-d 在起伏穿透 PCB 線圈 20 時，依照實質地平行(但偏移)之路徑。具體的片段及連接

如所要的在各應用間加以改變，其目的在於提供一線圈，其中每一長絲 54a-d 從成對的線圈電感式地接收實質地相等的電能，並貢獻充足地相等於自身或感應耦合之交互電感特徵。例如，式樣可加以改變，在每一長絲通過各層體到達最上層，然後返回到底層。

如所能見到者，PCB 線圈 20 包含多數個長絲，其在螺旋地向內經過線圈 20 時，向上/向下地經過層體加以起伏。在一可替換的實施例中，PCB 線圈 20 可加以構形而額外地提供每一層內的向內/向外的長絲起伏。第八 A-八 B 及第九圖顯示一可替換的本發明實施例，其提供向上/向下及向內/向外的起伏。在這個實施例中，PCB 線圈 20 包含兩個導體層 202a-b，由絕緣層(未示)加以隔離。現在參照第八 A-八 B 圖，每一導體層 202a-b 可包含兩個相鄰的、片段的軌跡 206a 及 206b，其形式為實質平行的線加以螺旋為成對關係。PCB 線圈 220 包含層間連接器 210(見第九圖)及層內連接器 212，其共同地連接不同層 202a-b 及不同軌跡 206a 及 206b 的片段 214，界定四個分離的長絲 208a-d。

如可能最佳地示於第九圖者，層間連接器 210 連接成對的層 202a-b 的片段 214，以提供向上/向下的長絲 208a-d 之起伏。第九圖顯示 PCB 線圈 210 之層 202a-b 及軌跡 206a-b。層間連接器 210 係在第九圖中以線加以顯示，但要瞭解，層間連接器 210 可為習知的通道或其他導體，能提供在不同層 202a-b 的片段 214 間電連接。例如，層間連接器 210 可實質地相同於上述的層間連接器，且每一者可包含一立體交叉道 216 及一或更多的通道 218。本實施例的層內連接器 212 連接相同層 202a-b 內的片段 214。如所示者，層內連接 212 可整合至軌跡 206a-b。例如，在不同軌跡 206a-b 的片段 214，可由基本上同於形成片段 214 的導體材料加以整體的結

個實施例的層內連接器 212 連接相同層 202a-b 內的片段 214。如所示者，層內連接器 212 可整合至軌跡 206a-b。例如，不同軌跡 206a-b 中的片段 214 可由同於形成片段 214 的導體材料整體地結合。

在這個實施例中，PCB 線圈片段 214 係以一個式樣加以連接，以界定多數個長絲 208a-d，其向上/向下及向內/向外地起伏。式樣可加以選擇，以致每一長絲 208a-d 花費實質相同時間接近成對的線圈(未示)。這可藉由(例如)每一長絲 208a-d 以規則的、重複的式樣加以起伏加以取得，進而每一長絲花費實質相同的時間於每一層及每一軌跡中。起伏的頻率可加以選擇，以提供所要程度的單一性介於長絲 208a-d 之間。向上/向下起伏與向內/向外起伏的結合，相較於只有向上/向下起伏的 PCB 線圈，可允許每一長絲更接近地模仿李茲線線圈股線之扭曲本質。第八 A 及第八 B 圖使用參考數字以代表層間連接器 210。在本發明中，兩個相似的參考數字係代表層間連接器 210 的相對端。例如，參考數字 A 及 A'代表層間連接器 210 之相對端，其電連接至兩個相對應的片段 214，而 B 及 B'代表另一層間連接器 210 的相對端。

向上/向下及向內/向外地起伏之長絲的概念，能經由額外層及額外成對軌跡加以實現。例如，第十、十一 A~十一 C 及十二圖，顯示一第二可替換的線圈 320，具有三層 302a-c 及三倍的軌跡 304a-c(如三個螺旋在一起的軌跡)。第十圖顯示一代表性的橫斷面視圖，顯示連接 306 可連同三層及三倍軌跡包含於 PCB 線圈。每一第十圖中的箭號代表一連接，從一片段 314 之外端到下個片段 314 的內端。結果，所示的橫斷面視圖顯示一九片段長的長絲部。第九個片段的外端係連接到第十片段的內端，其係相同於第一片段之層體及軌跡-只有第九片段進一步地朝向 PCB 線圈的內端。每

316a-i 將依照一規則的、重複的方式，依循基本上相同的流動路徑。第十一 A~十一 C 圖顯示一 PCB 線圈 320 之三層體 302a-c 的軌跡。第十一 A~十一 C 圖使用同於上述第八 A~B 圖之方法，顯示 PCB 線圈 320 之層間連接器 310。例如，參考數字 A 及 A'代表層間連接器 310 之相對端，其電連接至兩個相對應的片段 314，而 B 及 B'代表另一層間連接器 310 的相對端。片段連接係進一步地圖示於第十二圖。第十二圖顯示用於部份之 PCB 線圈 320 之所有的三個層體及所有的三個軌跡。第十二圖也顯示層間連接器 310 及層內連接器 312。

第十三圖顯示其他可替換的線圈構形，使用基本上同於第十圖中用於連接的所示方法(如上文所述)。在這個可替換的實施例中，線圈 520 包含三個導體層 502a-c，其由絕緣層(未示)加以隔離。最上層 502a 包含三倍的軌跡 504a-c，第二層 502b 包含四倍的軌跡 506a-d，及最低層 502c 包含三倍的軌跡 508a-c。如所示者，第二層 502b 係連同軌跡 506a-d 加以構形，其係垂直地對齊最上層 502a 及最下層 502c 之軌跡 504a-c 及 508a-c 之間的空隙。結果，軌跡 504a-c、506a-d 及 508a-c 加以重疊，以致並無開放的垂直路徑通過 PCB 線圈 520。使用重疊的軌跡橫跨層體，可藉由降低或減去磁通可能垂直地通過而不被導體層截斷之任何潛在空隙，而改良 PCB 線圈 520 的效率。

第十四圖係另一可替換之印刷電路板線圈 620 的代表示意圖。本實施例之線圈 620 包含一可替換的立體交叉道構形，其提供降低的電阻及電容。該圖顯示線圈 620 的層體 620a-d 係彼此在頂部上安置，而片段 618 係由盒子代表及通道由交連盒子的線加以代表。在第十四圖的實施例中，線圈 620 包含四個層體 602a-d，每一層 602a-d 具有單一片段的軌跡 604a-d。立體交叉道設計提供

8a-d 給予線圈 620，其以向內/向外之螺旋沿著軌跡 604a-d 時，在層體間向上/向下地起伏。在第十四圖中，每一長絲 608a-d 係由多數個連接的盒子加以代表，其分享相同的陰影。如所示者，線圈 620 包含四個長絲 608a-d，其每一次向上/向下地移動不超過單一層。例如，跟隨著長絲 608a 經過一單一循環，我們見到，其開始於層體 602a，向下轉移至第一立體交叉道 622a 上的層體 602b，向下至第二立體交叉道 622b 上的層體 602c，及最後向下到第三立體交叉道 622c 上的層體 602d。在到達底層 602d 之後，長絲 608a 保留在底層 602d 經由第四立體交叉道 622d。在第五立體交叉道 622e 上時，長絲 608a 從其轉移開始向後朝向第一層 602a。較為具體地，長絲 608a 轉移直到第五立體交叉道 622e 上的層體 602c，直到第六立體交叉道 622f 上的層體 602b，最後回到直到第七立體交叉道 622f 上的層體 602a。回到層體 602a 之後，長絲 608a 經由下一個立體交叉道(在本例中為第八立體交叉道)保留在頂層 602a 上，然後重複該循環，並再加以重複，直到抵達線圈之相對端為止。在第十四圖的實施例中，其餘的長絲 608b-d 係依循相質相同的及平行的路徑通過線圈，其彼此加以偏移，因為它們係起始於線圈 620 內的不同層體 602b-d。

第十五 A-D 圖顯示線圈 620 的四軌跡 604a-d。四軌跡 604a-d 係相同之定位加以顯示，以致圖式可加以重疊，以顯示其在總成的線圈 620 中的對齊。第一個兩個軌跡 604a-b 可加以安置在單一電路板基板的相對側上，同時第二個兩個軌跡 604c-d 可安置於第二電路板基板的相對側上。攜帶四個軌跡的兩個電路板基板，可交互固著，形成具有四層體 602a-d 及四軌跡 604a-d 的總成。兩個電路板基板可由膠黏劑加以結合在一起，例如，一層環氧樹脂浸漬的纖維玻璃，或由任何其他的合適製造法。

本實施例的立體交叉道構形現在係相關於第十六圖來描述。第十六圖係部份之線圈 620 的代表性圖式，顯示以側對側加以排列的四個層體 a-d 的線圈之相對應片段。應加以瞭解，四個層體係在已總成之線圈 620 內的另一者頂部上堆疊。它們解開堆疊並側對側地安置，只為了有助本發明解說。一般而言，線圈 620 包含兩個不同型式的立體交叉道，其在線圈 620 的長度上彼此更迭。第一型的立體交叉道，如立體交叉道 622a 及 622c，包含在層體 602a 及 602b 之間的"盲"道，及層體 602c 及 602d 之間者。盲道交連層體 602a 內的第一片段至層體 602b 內的第二片段，及交連層體 602b 內的第一片段至層體 602a 內的第二片段。相似地，盲道連層體 602c 內的第一片段至層體 602d 內的第二片段，及交連層體 602b 內的第一片段至層體 602c 內的第二片段。如所能見到者，第一型的立體交叉道電連接第一個兩個層體 602a 及 602b，及電連接第二個兩個層體 602c 及 602d。盲道可藉由各自地在兩個電路板基板上加以打洞 626 而形成，例如，在兩個基板總成成為線圈 620 之前。打洞 626 可用銅電鍍，在頂部兩個層體 602a 及 602b 之間、及底部兩個層體 602c 及 602d 之間，提供電連接。銅電鍍可施加到兩個電路板基板上的盲道，同時它們係彼此分離的。

在一實施例中，也許最佳地顯示於第十八圖，每一層體 602a-d 包含多重通道。亦即，多重的洞 626 係鑽過每一電路板基板。在其他實施例中，打洞 626 可以銅電鍍，提供不同層體間的電連接。

立體交叉道的第二型，如立體交叉道 622b，包含在整個總延伸的通道及電連接的層體 602b 及 602c。再次參照第十六圖，第二型的立體交叉道交連層體 602b 之第二片段至層體 602c 之第三片段，及層體 602c 之第二片段至層體 602b 之第三片段。如能見到者，第二型的立體交叉道只有電連接中間的兩個層體 602b 及

602c。第二型的立體交叉道，可藉由打洞 626 穿透總成線圈(例如，兩個基板及分隔兩基板之材料)，然後施加銅電鍍至打洞 626，而加以形成。如所示者，在頂及底層 602a 及 602b 內的軌跡 604a 及 604d，具有放大的空隙 644，其分隔打洞 626 內的銅電鍍及軌跡 604a 及 604d。然而應予注意，層體 602c 包含指狀物(fringers)645，橋接偏移空隙 644 之間的距離。指狀物 645 具有降低的橫斷面積，相較於具有完整橫斷面積之軌跡的部份，可避免某些對電流之限制。結果，吾人想要的是，平衡空隙 644 之偏移的程度，在指狀物 645 長度上相對應的漸增。如可見到者，中間兩個層體 602b 及 602c 之內的軌跡 604a 及 604c，並未包含這些空隙 644，而是直接地電連接至銅鍍層。結果，銅鍍層交連第二及第三層 602b 及 602c 之片段。藉由更換第一型立體交叉道(如立體交叉道 622a)及第二型立體交叉道(如立體交叉道 622b)，線圈 620 提供上述的長絲起伏。

第十七圖為另一可替換實施例的代表，其中第十四圖之立體交叉道構形係以六層加以實施。這個圖式依循相同於第六圖及第十四圖所用之方法。如所示者，線圈 720 包含三個不同型式的立體交叉道。第一型的立體交叉道，如立體交叉道 722a、722d 及 722j，提供三組盲道。第一組的盲道交連層體 702a 及 702b，第二組交連層體 702c 及 702d，第三組交連層體 702e 及 702f。盲道可依基本上相同於前述線圈 620 盲道的方法，加以製造。第二型的立體交叉道，如立體交叉道 722b、722e 及 722h，只連接層體 702b 及 702c。就此型的立體交叉道而言，層體 702b 可包含完全的端點，相似於第十六圖之立體交叉道 622b 上的層體 602b，及層體 702c 可包含指狀物相似於第十六圖立體交叉道 622b 上的層體 602c。為了幫助需要電連接層體 702b 及 702c 的通道，層體 702a 及 702d-f 可包含空隙，相似於線圈 620 的空隙 644。第三型的立體交叉道，如立體

交叉道 722c、722f 及 722i，只交連層體 702d 及 702e。就此型的立體交叉道而言，層體 702d 可包含指狀物，相似於第十六圖立體交叉道 622b 上的層體 602c，層體 702a-c 及 702f 可包含空隙，相似於線圈 620 的空隙 644。藉由重複這些型的立體交叉道之循環，長絲 708a-f 在層體 702a-f 間上及下地起伏，每一次不超過一層。在所示的實施例中，單一長絲 708a 維持在層體 702a 上一相等於約三個片段的距離，向下轉移到一片段之層體 702b，向下轉移到層體 702c 上一相等於約兩個片段的距離，向下轉移到層體 702d 上一相等於約兩個片段的距離，向下轉移到一片段之層體 702e，然後轉移到層體 702f 上一相等於約三個片段的距離。然後長絲 708a 依循相同的式樣(雖然是小量)，其一次轉移一層再回到頂層。

上述描述的是本發明目前的實施例。許多更換及改變能加以製成而不離開本發明之精神及較寬廣的觀點，其如後附之申請專利範圍所界者，其係依照專利法原則，包括均等論而加以解釋。任何所聲請之元件的單數參考符號，如冠詞 a、an、the 或 said，並不解釋為限制元件為單數。

【圖式簡單說明】

第一 A 圖係本發明一實施例之印刷電路板(PCB)的側平面視圖。

第一 B 圖係 PCB 線圈軌跡之代表性分解立體視圖。

第一 C 圖係相似於第一 B 圖之代表性分解立體視圖，其所選的片段係加陰影，以顯示單一長絲的路徑。

第二 A 圖係 PCB 線圈的第一層(或頂)的軌跡的頂平面視圖。

第二 B 圖係 PCB 線圈的第二層的軌跡的頂平面視圖。

第二 C 圖係 PCB 線圈的第三層的軌跡的頂平面視圖。

第二 D 圖係 PCB 線圈的第四層(或底)的軌跡的頂平面視圖。

第三圖係單一螺旋軌跡之角落區的頂平面視圖。

第四圖係單一螺旋軌跡之直線區的頂平面視圖。

第五圖係一可替換之 PCB 線圈之一部份的立體圖，顯示一可替換的結構，用於降低界面上的限制。

第六圖係多層之片段間連接設計的代表性示意圖。

第七圖係立體交叉道之立體視圖，顯示片段之重疊的排列。

第八 A 圖係第一可替換 PCB 線圈之頂導體層的頂平面視圖，其具有向上/向下及向內/向外的長絲起伏。

第八 B 圖係第一可替換 PCB 線圈之底導體層的頂平面視圖。

第九圖係第一可替換 PCB 線圈之代表性分解立體視圖。

第十圖係第二可替換 PCB 線圈之代表性示意圖，其具有三層及"三倍的"軌跡。

第十一 A 圖係第二可替換 PCB 線圈之頂導體層的頂平面視圖。

第十一 B 圖係第二可替換 PCB 線圈之中導體層的頂平面視圖。

第十一 C 圖係第二可替換 PCB 線圈之底導體層的頂平面視圖。

第十二圖係第二可替換 PCB 線圈之代表性分解立體視圖。

第十三圖係第三可替換 PCB 線圈之代表性示意圖，其具有三層向上/向下及向內/向外起伏的線圈。

第十四圖係第四可替換 PCB 線圈之代表性示意圖。

第十五 A 圖係第十四圖之第四可替換 PCB 線圈的第一層之頂平面視圖。

第十五 B 圖係第十四圖之第四可替換 PCB 線圈的第二層之頂平面視圖。

第十五 C 圖係第十四圖之第四可替換 PCB 線圈的第三層之頂平面視圖。

第十五 D 圖係第十四圖之第四可替換 PCB 線圈的第四層之頂

平面視圖。

第十六圖係第十四圖之第四可替換 PCB 線圈的代表性連接示意圖。

第十七圖係第五可替換 PCB 線圈的代表性示意圖。

第十八圖係第六可替換 PCB 線圈的代表性示意圖。

【主要元件符號說明】

12 多層電路板
14a-d 交流導體層
16a-c 絕緣層
18 片段
18a 內端
18b 外端
20 印刷電路板(PCB)線圈
202a-b 導體層
206a 及 206b 軌跡
208a-d 長絲
210 層間連接器
212 層內連接器
214 片段
216 立體交叉道
218 通道
22 立體交叉道
220 PCB 線圈
24 通道
28 導體
306 連接
310 層間連接器
312 層內連接器
314 片段
316a-i 長絲
320 線圈
40 連接器
42 絕緣穿孔
44 放大部
46 寬度降低之部份
502a-c 導體層
504a-c 軌跡
506a-d 軌跡
508a-c 軌跡
520 線圈
52a-d 軌跡
54a-d 長絲
60 及 62 分流部
602a-d 層體
604a-d 軌跡
608a-d 長絲
618 片段
620 印刷電路板線圈
622a 立體交叉道
622b 立體交叉道
626 打洞
644 空隙
645 指狀物
702a 及 702b 層體
702c 及 702d 層體
720 線圈
722a、722d 及 722j 立體交叉道
722b、722e 及 722h 立體交叉道

200938017 發明專利說明書

（本說明書格式、順序，請勿任意更動，※記號部分請勿填寫）

※申請案號：97136804

※申請日：97.9.15 ※IPC分類：H05K1/16 (2006.01)

一、發明名稱：（中文/英文）

印刷電路板線圈/PRINTED CIRCUIT BOARD COIL

二、中文發明摘要：

一種多層印刷電路板(PCB)線圈，其模擬李茲線(litz wire)所形成之線圈。該PCB包含多數個交流導體及絕緣層，其交互連結並共同形成線圈。每一導體層包含一軌跡，其遵循所要的線圈形狀並加以分割成為多數個各別的導體片段。該片段係橫跨層體加以電連接，提供多數個電流通道(或長絲)，在層體間以規則重複的式樣起伏。線圈可加以構形以致每一長絲花費實質相等的時間接近成對線圈，因而提供實質相等於自身或線圈的交互感應。每一導體層可包含多數個相伴的軌跡及層內交連的連接器，以致每一長絲不止向上/向下起伏，也以規則而重複的式樣向內/向外起伏。

三、英文發明摘要：

A multilayer printed circuit board ("PCB") coil that simulates a coil formed from litz wire. The PCB includes a plurality of alternating conductor and insulating layers interconnected to cooperatively form the coil. Each conductor layer includes a trace that follows the desired coil shape and is divided into a plurality of discrete conductor segments. The segments are electrically connected across layers to provide a plurality of current flow paths (or filaments) that undulate between the layers in a regular, repeating pattern. The coil may be configured so that each filament spends a substantially equal amount of time in proximity to the paired coil and therefore contributes substantially equally to the self or mutual inductance of the coil. Each conductor layer may include a plurality of associated traces and intralayer connector that interconnected so that each filament undulates not only upwardly/downwardly, but also inwardly/outwardly in a regular, repeating pattern.

七、申請專利範圍：

1. 一種印刷電路板線圈，係連同成對線圈加以使用，包括：

一基材；

多數個導體層，每一導體層包含多數個各別線圈片段；及多數個層體間連接器，在不同層體的線圈片段間加以電連接，界定多數個各別的長絲，每一該長絲遵循實質相同但偏移的起伏穿透該多數層體。

2. 如申請專利範圍第 1 項所述的印刷電路板線圈，其中每一長絲遵循實質相同但偏移的、規則的、重複的起伏穿透該多數層體。

3. 如申請專利範圍第 1 項所述的印刷電路板線圈，其中該線圈係與一第二線圈成對的；且

其中該片段及該層間連接器係加以構形，以致每一長絲花費實質相等的時間接近該成對線圈，進而該印刷電路板模仿一李茲線的線圈。

4. 如申請專利範圍第 1 項所述的印刷電路板線圈，其中進一步包含一絕緣層,其位置介於相鄰之成對的該導體層之間。

5. 如申請專利範圍第 1 項所述的印刷電路板線圈，其中每一該多數個導體層包含一螺旋軌跡。

6. 如申請專利範圍第 5 項所述的印刷電路板線圈，其中每一該軌跡包含一立體交叉道(interchange)，該層間連接器包含多數個通道，選擇性地經由該立體交叉道加以佈排。

7. 如申請專利範圍第 1 項所述的印刷電路板線圈，其中每一螺旋軌跡包含一最內端及一最外端，每一該片段包含一內端朝向該螺旋軌跡最內端及一外端朝向該螺旋軌跡最外端；且

其中每一該長絲係由片段一者之內端，從該軌跡最外端至該軌跡最內端之成一連續鏈的方式，進行電連接該片段另一者之外端，而加以形成。

8. 如申請專利範圍第 1 項所述的印刷電路板線圈，其中該多數片段界定一第一螺旋軌跡及一第二螺旋軌跡於每一導體層上；且

進一步包含多數個層內連接器，用於在單一導體層內，電連接該來自該第一旋螺軌跡之片段至第二螺旋軌跡之片段，該內層連接器及該層內連接器共同合作界定該長絲，在每一層內，遵循實質相同但偏移的起伏並穿透每一該多數個層體。

9. 如申請專利範圍第 1 項所述的印刷電路板線圈，其中該導體層之第一者包含螺旋軌跡，其具有多數個迴路，及其中每一該第一導體層之軌跡的片段係由該第一導體層相鄰迴路的該片段加以隔離而界定一空間；且

其中該導體層之第二者包含螺旋軌跡，其具有多數個迴路，及其中每一該第二導體層之軌跡的片段係安置重疊該第一導體層的該空間。

10. 一種印刷電路板總成，包括：

一絕緣基材；

一第一導體層，安置在該基材上，該第一導體層包含一第一軌跡，其具有多數個各自的導體片段；

一第二導體層，安置在該基材上，其位置相對該第一導體層，該第二導體層包含一第二軌跡，其具有多數個各自的導體片段；及

多數個內層連接器，以預定之式樣連接該第一層之片段至該第二層之片段，其中該交互連接的片段界定至少兩個長絲，其在該第一導體層及該第二導體之間以預定之式樣加以起伏。

11. 如申請專利範圍第 10 項所述的印刷電路板線圈總成，其中進一步包含：

一第二絕緣基材，係鄰近該第一絕緣基材加以安置；

一第三導體層，安置在該第二基材上，該第三導體層具有一第

三軌跡包含多數個各自的導體片段；

一第四導體層，安置在該第二基材上，在側邊上相對該第三導體層，該第四導體層具有一第四軌跡，其具有多數個各自的導體片段；

多數個內層連接器，以一預定的式樣，交互電連接該第一層的片段，該第二層的片段，該第三層的片段，及該第四層的片段，其中該交互連接的片段界定至少兩個長絲，其在該第一導體層、第二導體層、第三導體層、及第四導體層之間，以預定的式樣加以起伏。

12. 如申請專利範圍第 10 項所述的印刷電路板線圈總成，其中該第一導體層包含一第二軌跡，具有多數個各自的導體片段；且

進一步包含多數個層內連接器，用於電連接該第一旋螺軌跡之片段至第三螺旋軌跡之片段，進而該長絲在該第一導體層及該第二導體層之間，以及在該第一軌跡及該第三軌跡之間，以預定式樣加以起伏。

14. 如申請專利範圍第 13 項所述的印刷電路板線圈總成，其中該第二導體層包含第四軌跡，其具有多數個導體片段；且

進一步包含多數個層內連接器，用於電連接該第二旋螺軌跡之片段至第四螺旋軌跡之片段，進而該長絲在該第一導體層及該第二導體層之間，以及在該第一軌跡及該第三軌跡之間，以及在該第二軌跡及該第四軌跡之間，以預定式樣加以起伏。

15. 如申請專利範圍第 10 項所述的印刷電路板線圈總成，其中該長絲遵循實質平行的但偏移的路徑，以規則的、重複的式樣在線圈周遭加以起伏。

16. 如申請專利範圍第 10 項所述的印刷電路板線圈總成，其中該線圈具有一最內端及一最外端；

每一該第一軌跡的片段具有一內端及一外端，每一該第二軌跡

的片段具有一內端及一外端，每一該長絲係由多數個交連的片段加以界定，其係該片段一者的內端與該片段另一者的外端，以該線圈之外端到該線圈之內端的連續鏈，加以電連接。

17. 一種多層電磁線圈，用於無線電能連接，包括：

一第一導體層，具有多數個各自的導體片段；

一第二導體層，加以安置鄰近該第一導體層，該第二導體層包含多數個各別的導體片段；及

多數個連接器，以預定的式樣交互連接該第一層的片段至該第二層的片段，其中該交互連接的片段界定至少兩個長絲，其在該第一導體層及該第二導體層之間以預定之式樣加以起伏。

18. 如申請專利範圍第 17 項所述的多層電磁線圈，其中該片段及該連接器係加以安排，以致每一該長絲係實質地均勻地在整個線圈內分佈，進而每一該長絲係實質相等地貢獻線圈的電感。

19. 如申請專利範圍第 17 項所述的多層電磁線圈，其中進一步地包含一第三導體層，加以安置鄰近該二導體層，該第三導體層包含多數個各別的導體片段；及

多數個連接器，以預定的式樣交互連接該第一導體層、該第二導體層及該第三導體層的片段，其中該交互連接的片段界定至少三個長絲，其在該第一導體層、該第二導體層及該第三導體層之間以預定之式樣加以起伏，進而每一該長絲係實質相等地貢獻線圈的電感。

20. 如申請專利範圍第 17 項所述的多層電磁線圈，其中結合一第二感應線圈，該第二感應線圈係感應耦合至該線圈，其中該片段及該連接器係加以安排，以致每一該長絲係實質地均勻地在整個線圈內分佈，進而每一該長絲係實質相等地從該第二線圈接收磁通量。

21. 如申請專利範圍第 17 項所述的多層電磁線圈，其中結合一第

二感應線圈，該第二感應線圈係感應耦合至該線圈；且

進一步地包含一第三導體層，加以安置鄰近該二導體層，該第三導體層包含多數個各別的導體片段，該多數個連接器，以預定的式樣交互連接該第一導體層、該第二導體層及該第三導體層的片段，其中該交互連接的片段界定至少三個長絲，其在該第一導體層、該第二導體層及該第三導體層之間以預定之式樣加以起伏，進而每一該長絲係實質相等地從該第二線圈接收磁通量。

22. 如申請專利範圍第 17 項所述的多層電磁線圈，其中該第一層的導體片段界定一第一螺旋軌跡及一第二螺旋軌跡，及

其中該多數個連接器以預定式樣交互連接該第一軌跡之片段及該第二軌跡之片段至該第二層的片段，其中該交互連接的片段界定至少兩個長絲，其在該第一導體層之第一軌跡及該第一導體層與該第二導體層之第二軌跡之間，以預定之式樣加以交連。

23. 如申請專利範圍第 17 項所述的多層電磁線圈，其中該第一及第二導體層與成對的線圈係距離相等。

24. 如申請專利範圍第 17 項所述的印刷電路板，其中每一該第一及第二導體層傳輸或接收同量的磁通。

25. 一種電磁線圈，用於無線電能連接，包括：

一第一導體層，具有一第一導體片段及一第二導體片段；

一第二導體層，安置鄰近該第一導體層，該第二導體層包含一第一導體片段、一第二導體片段及一第三導體片段；

一第三導體層，安置鄰近該第二導體層，該第三導體層包含一第一導體片段、一第二導體片段及一第三導體片段；

一第四導體層，安置鄰近該第四導體層，該第四導體層包含一第一導體片段及一第二導體片段；

一第一立體交叉道，交連該第一導體層之第一片段至該第二導

體層之第二片段；

一第二立體交叉道，交連該第一導體層之第二片段至該第二導體層之第一片段；

一第三立體交叉道，交連該第三導體層之第一片段至該第四導體層之第二片段；

一第四立體交叉道，交連該第三導體層之第二片段至該第四導體層之第一片段；

一第五立體交叉道，交連該第二導體層之第二片段至該第三導體層之第三片段；

一第六立體交叉道，交連該第二導體層之第三片段至該第三導體層之第二片段。

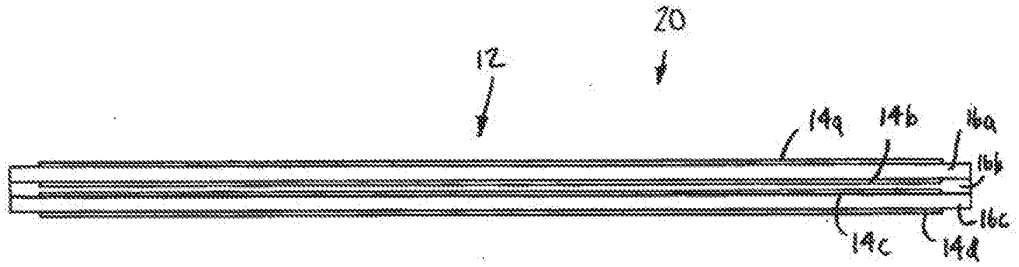
26. 如申請專利範圍第 25 項所述的多層電磁線圈，其中該第一導體層之第二片段及該第四導體層之第二片段分別包含多數個空隙，其保持該第四立體交叉道及該第六立體交叉道不與該第一導體層之第二片段及該第四導體層之第二片段進行交互連接。

27. 如申請專利範圍第 25 項所述的多層電磁線圈，其中該第一導體層、該第二導體層、該第三導體層、及該第四導體層係彼此堆疊於另一者之頂部。

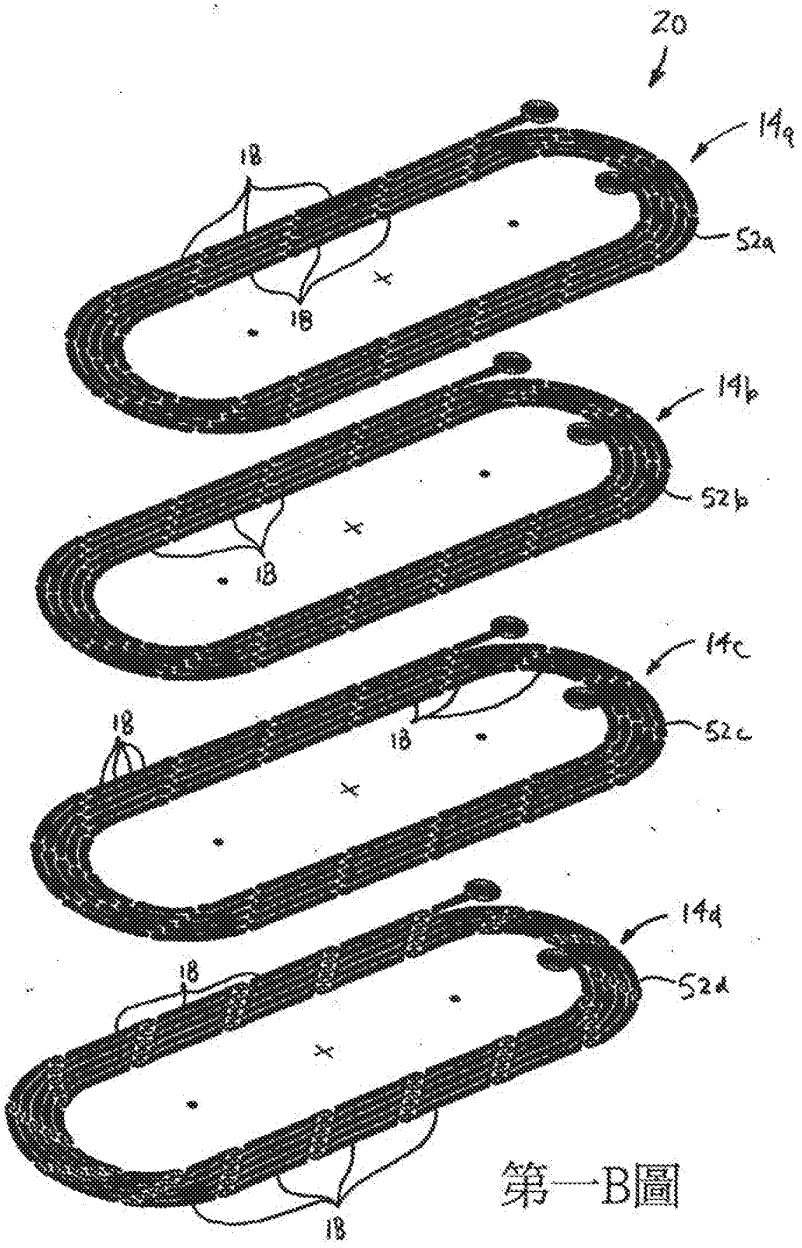
28. 如申請專利範圍第 25 項所述的多層電磁線圈，其中每一該導體層係與成對的線圈距離均等。

29. 如申請專利範圍第 25 項所述的多層電磁線圈，其中每一該導體層係傳輸或接收同量的磁通。

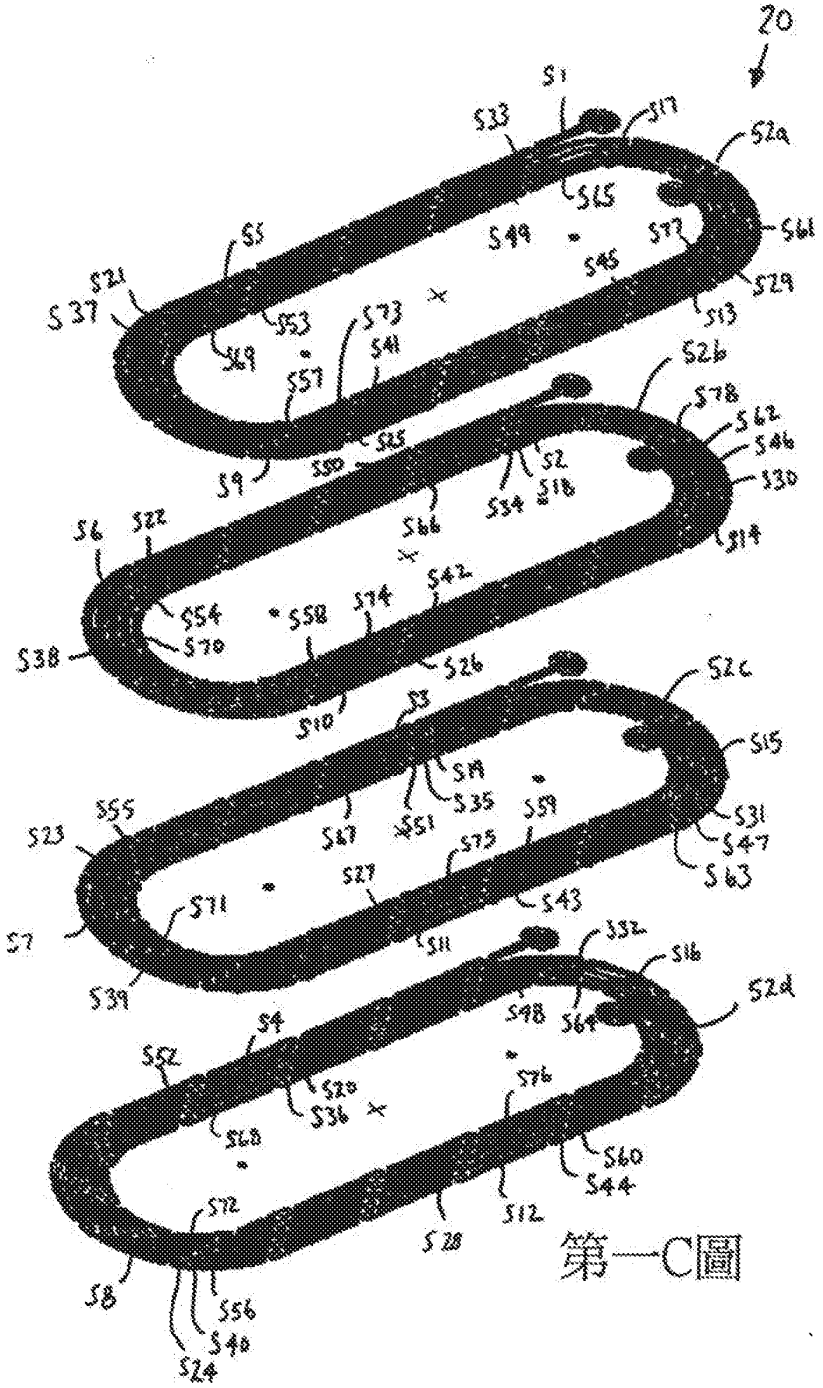
八、圖式：



第一A圖



第一B圖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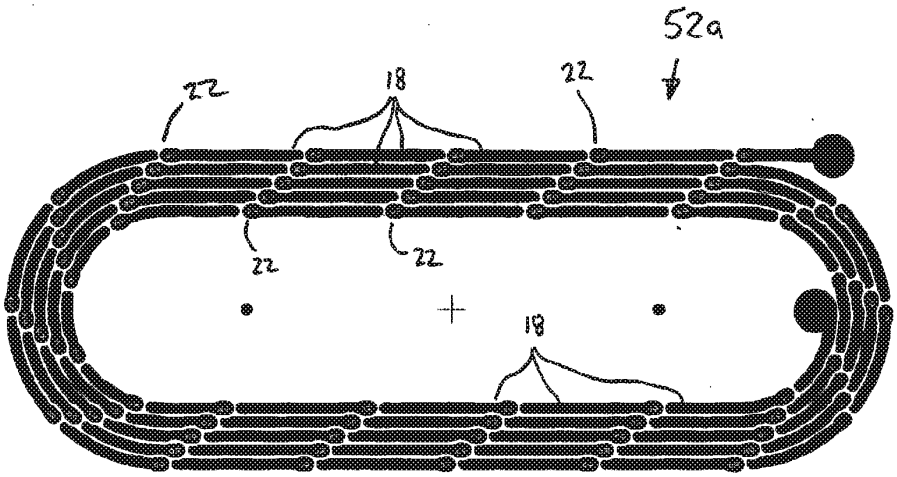
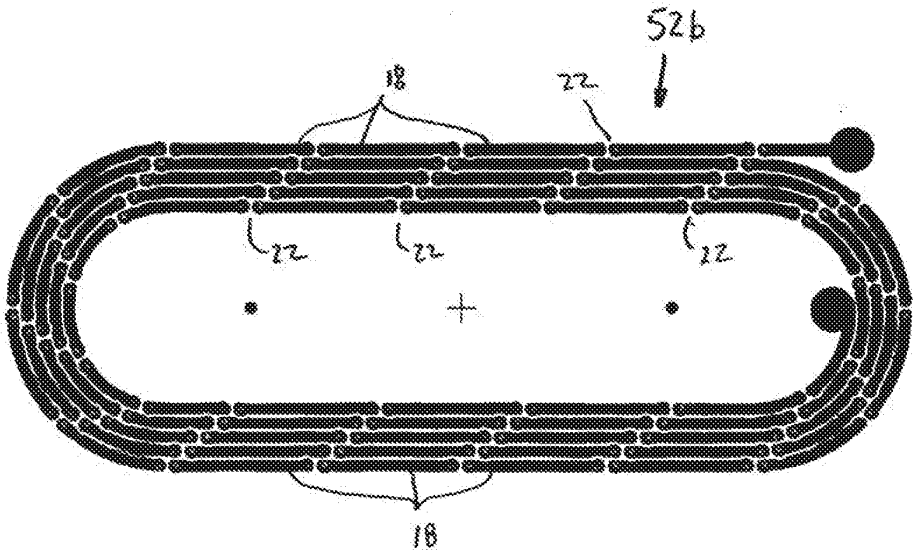
第一C圖

第一層



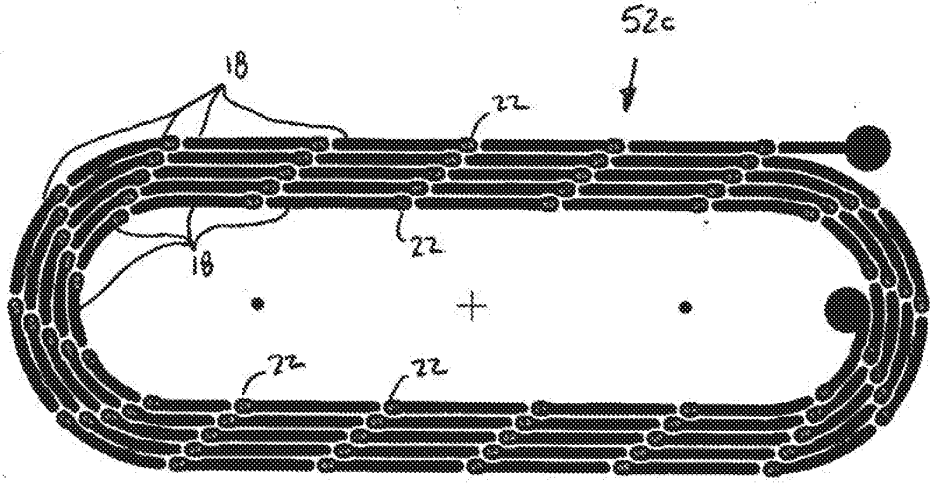
第二A圖

第二層



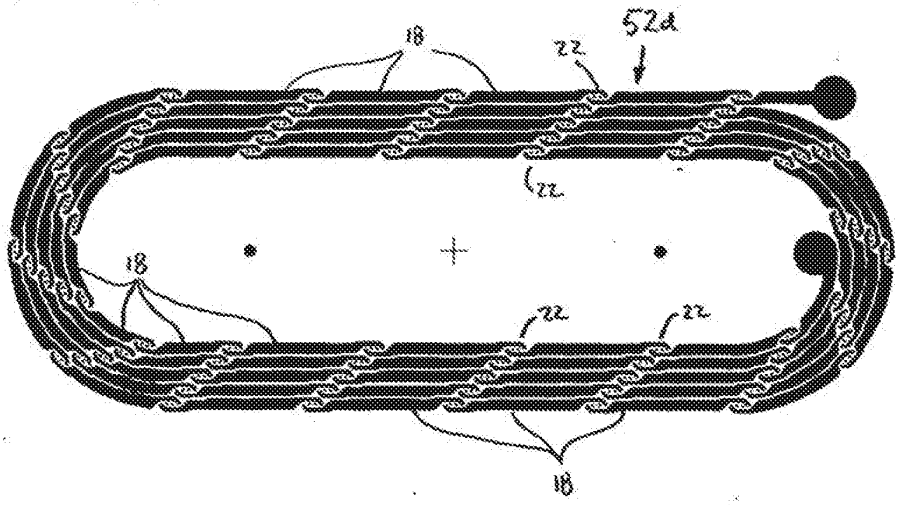
第二B圖

第三層



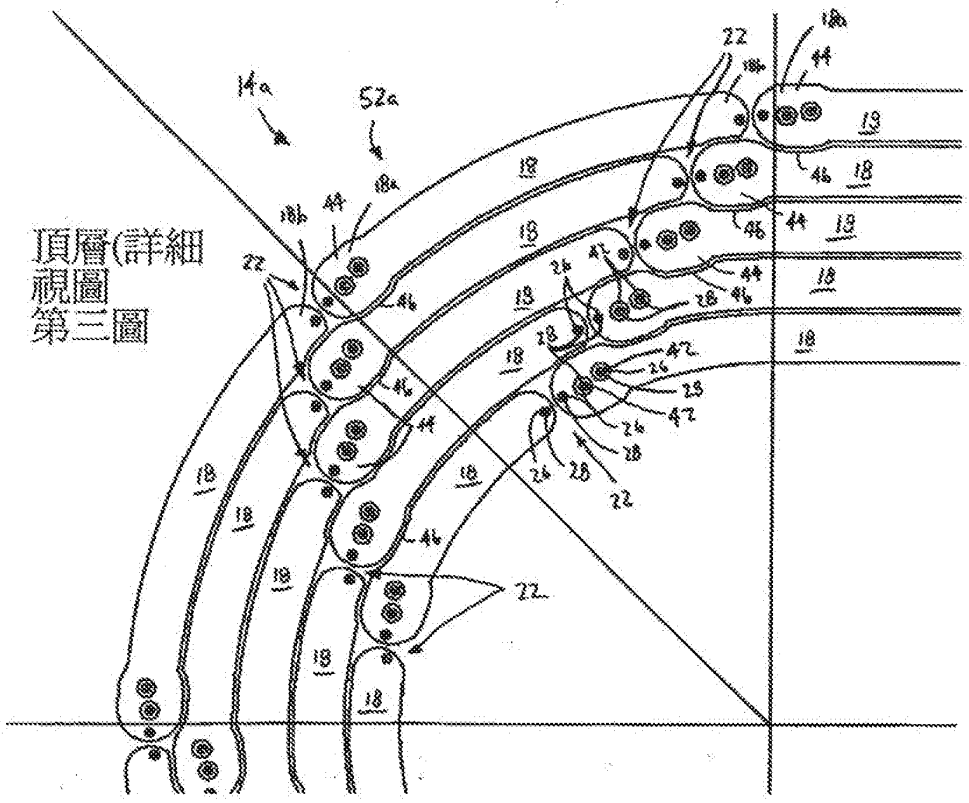
第二C圖

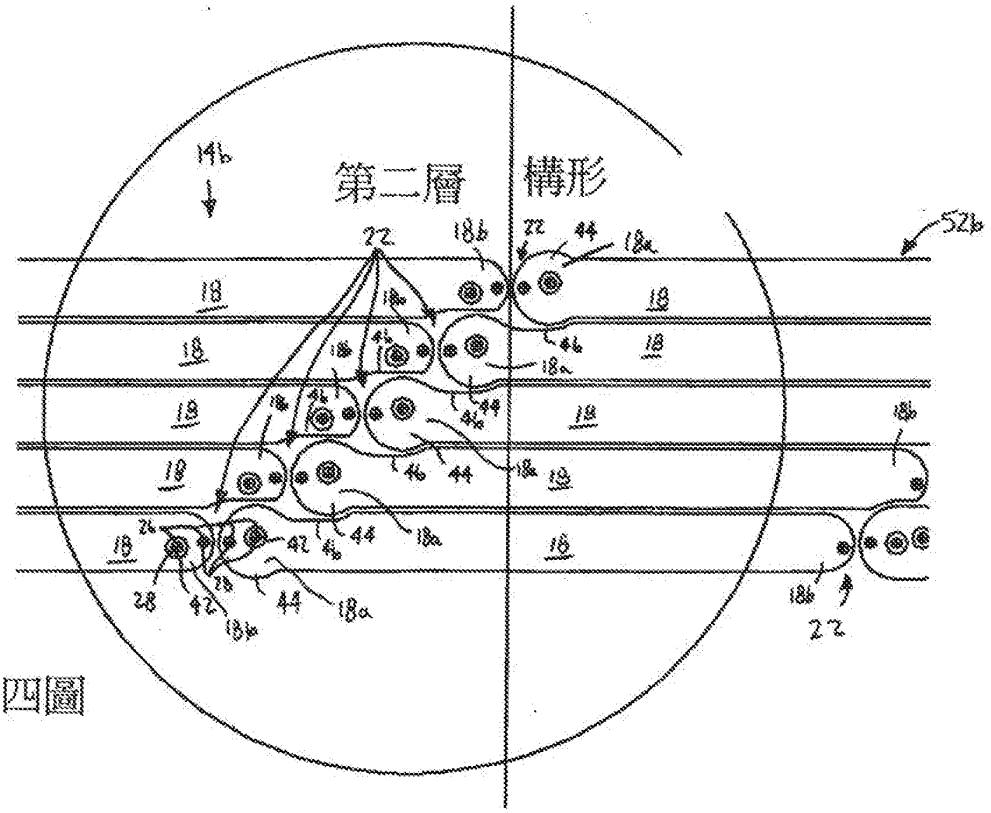
第四層



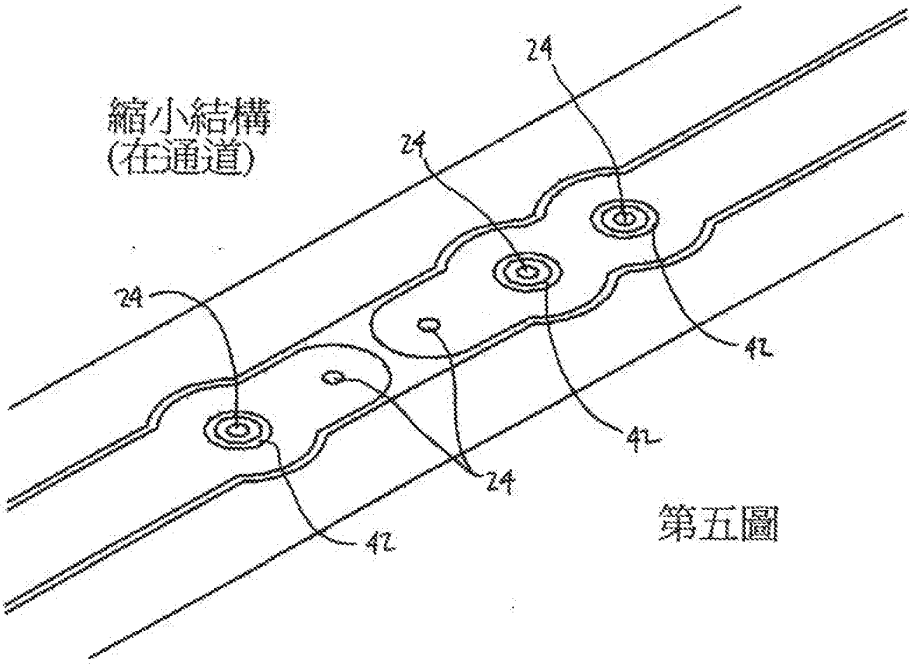
第二D圖

頂層(詳細視圖)
第三圖

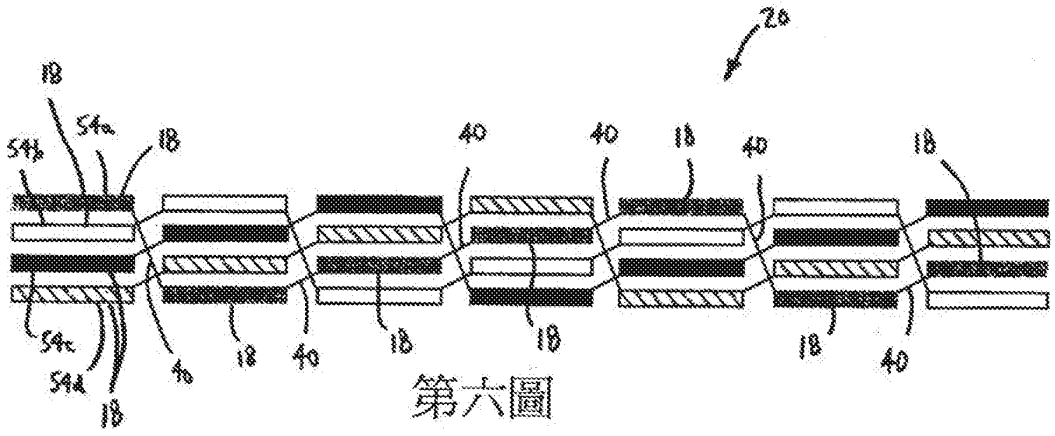




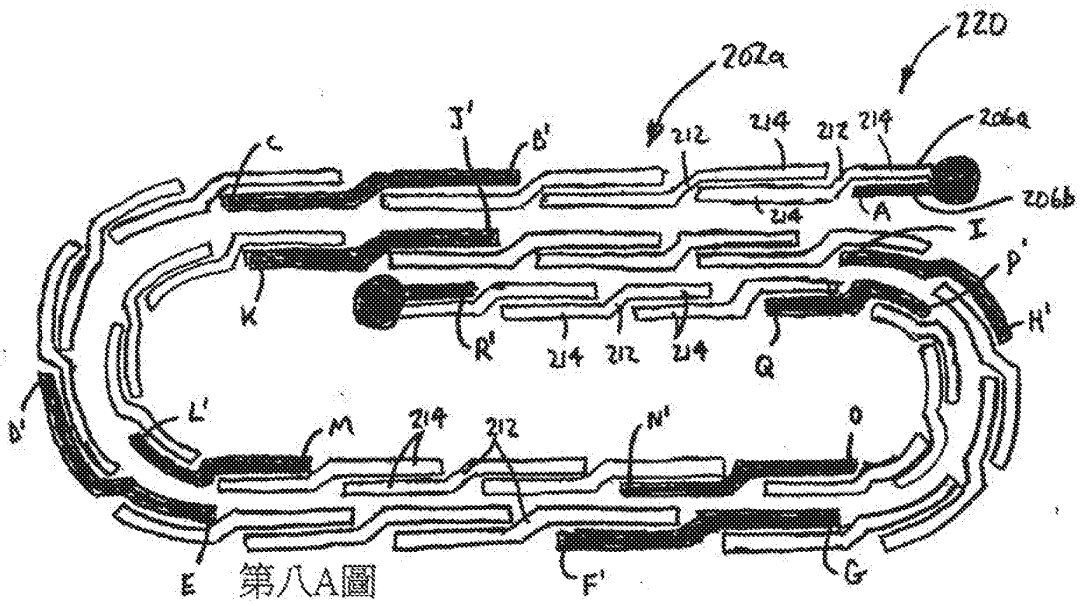
第四圖



第五圖



第六圖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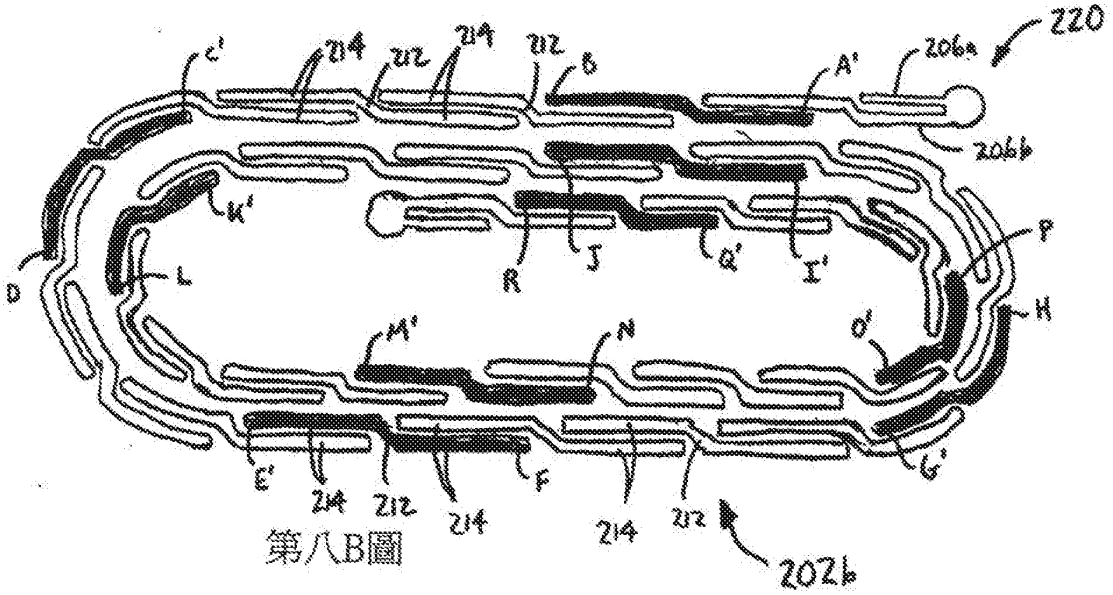
第八A圖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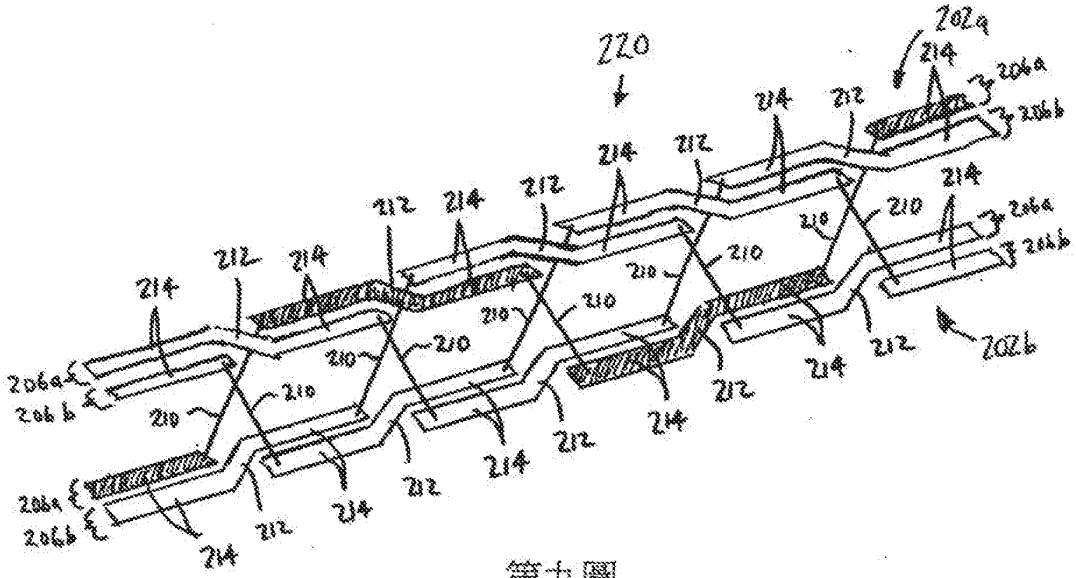
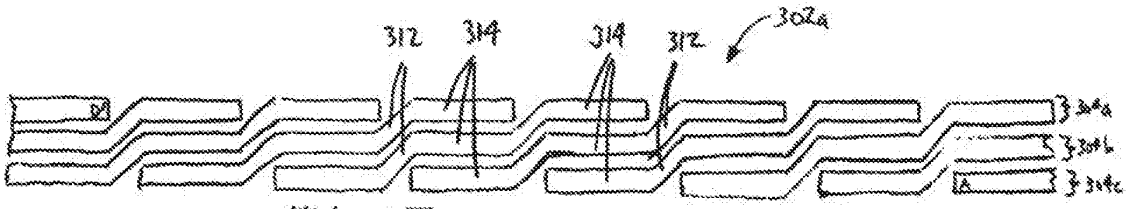
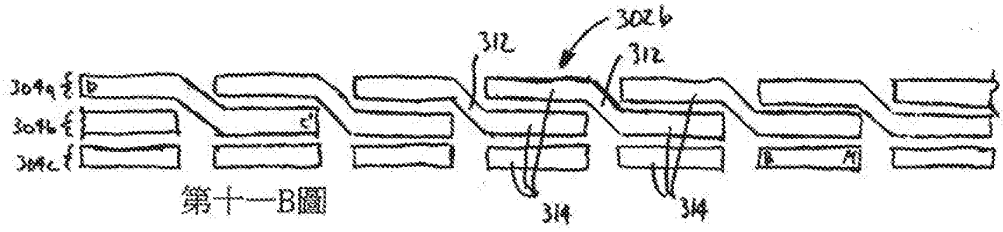
第八B圖



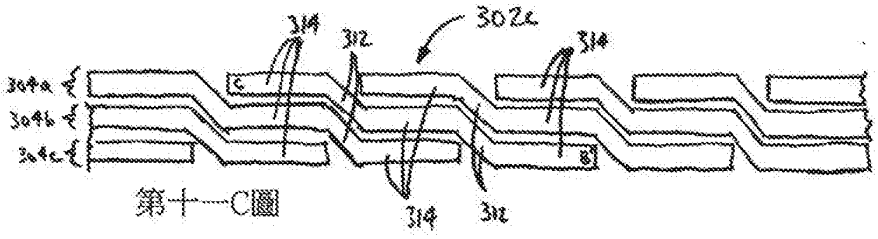
第九圖



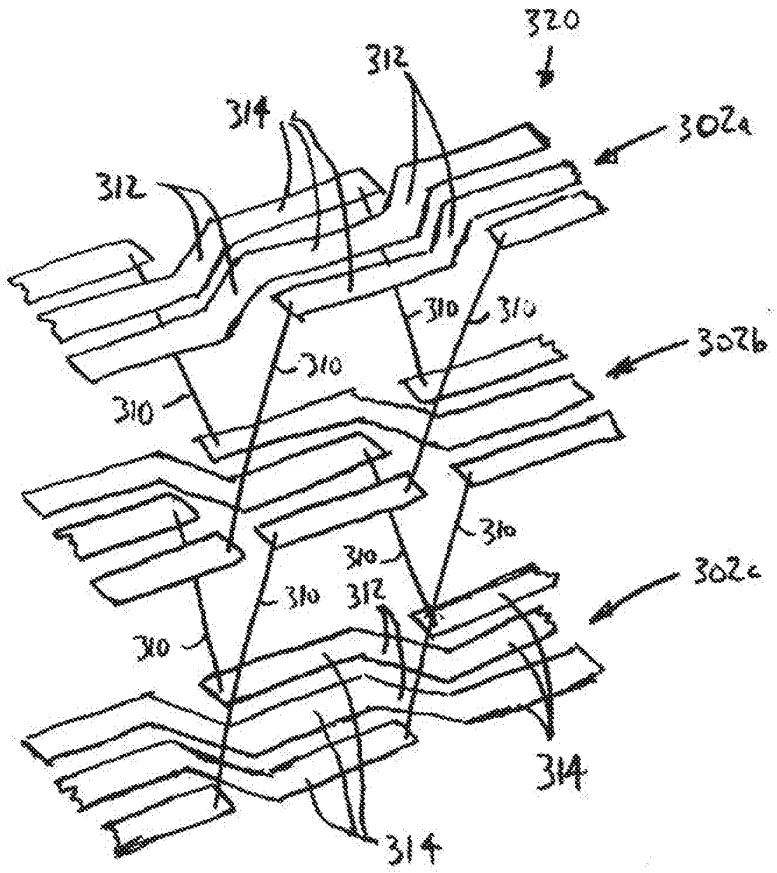
第十一A圖



第十一B圖



第十一C圖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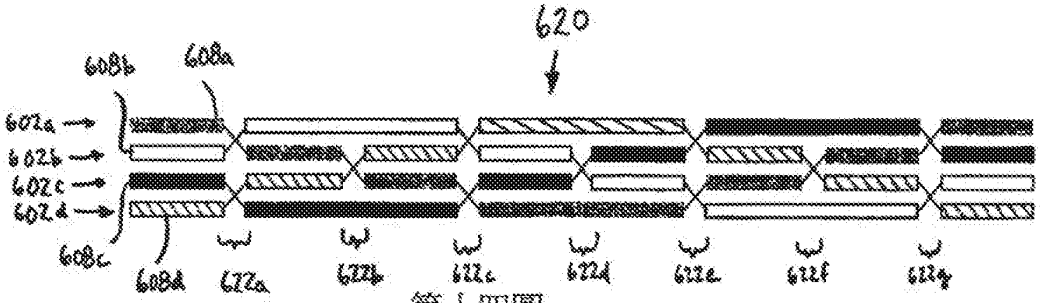
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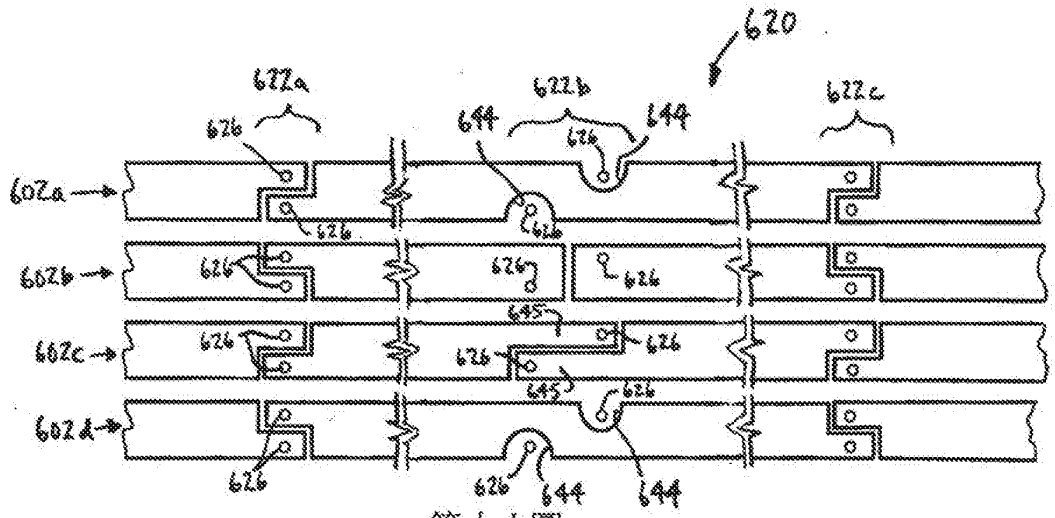
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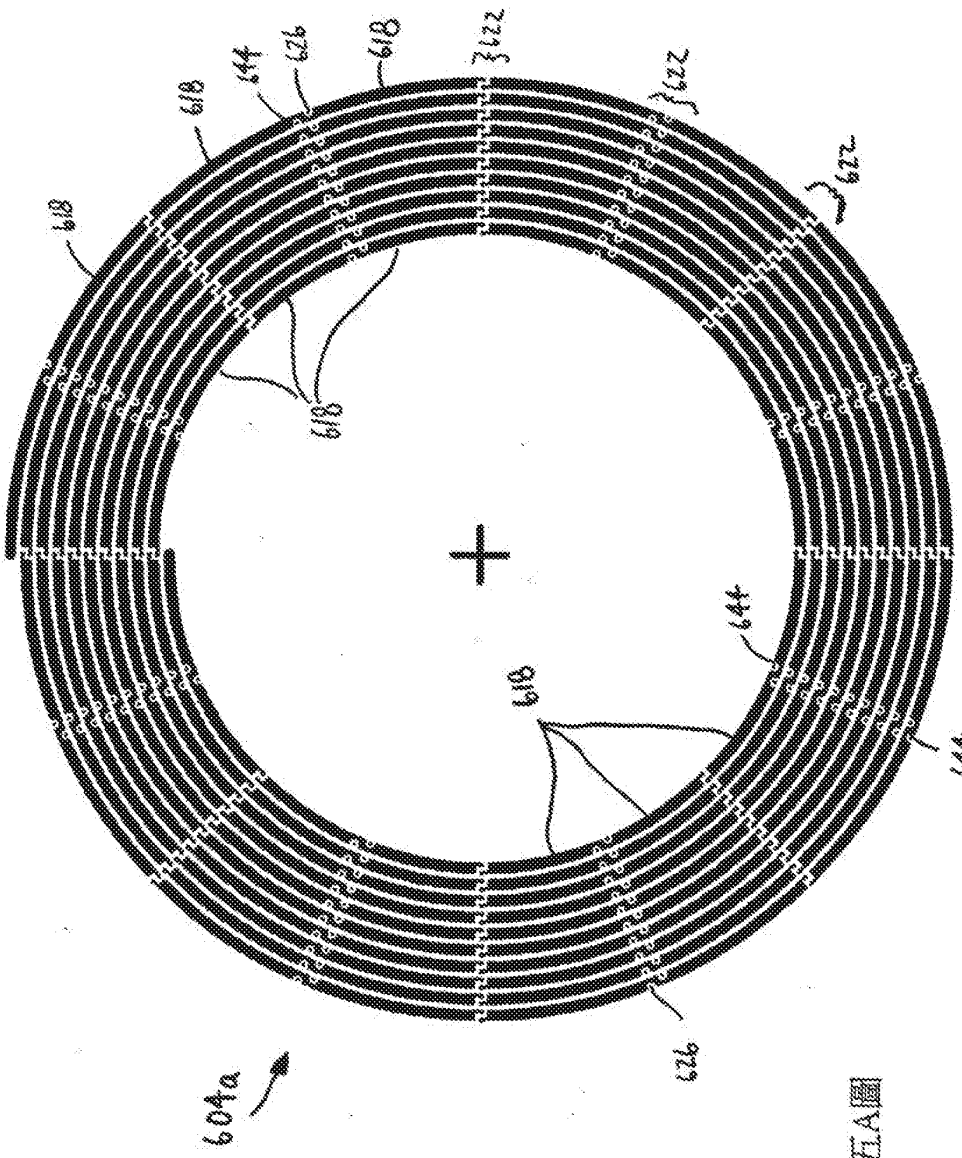

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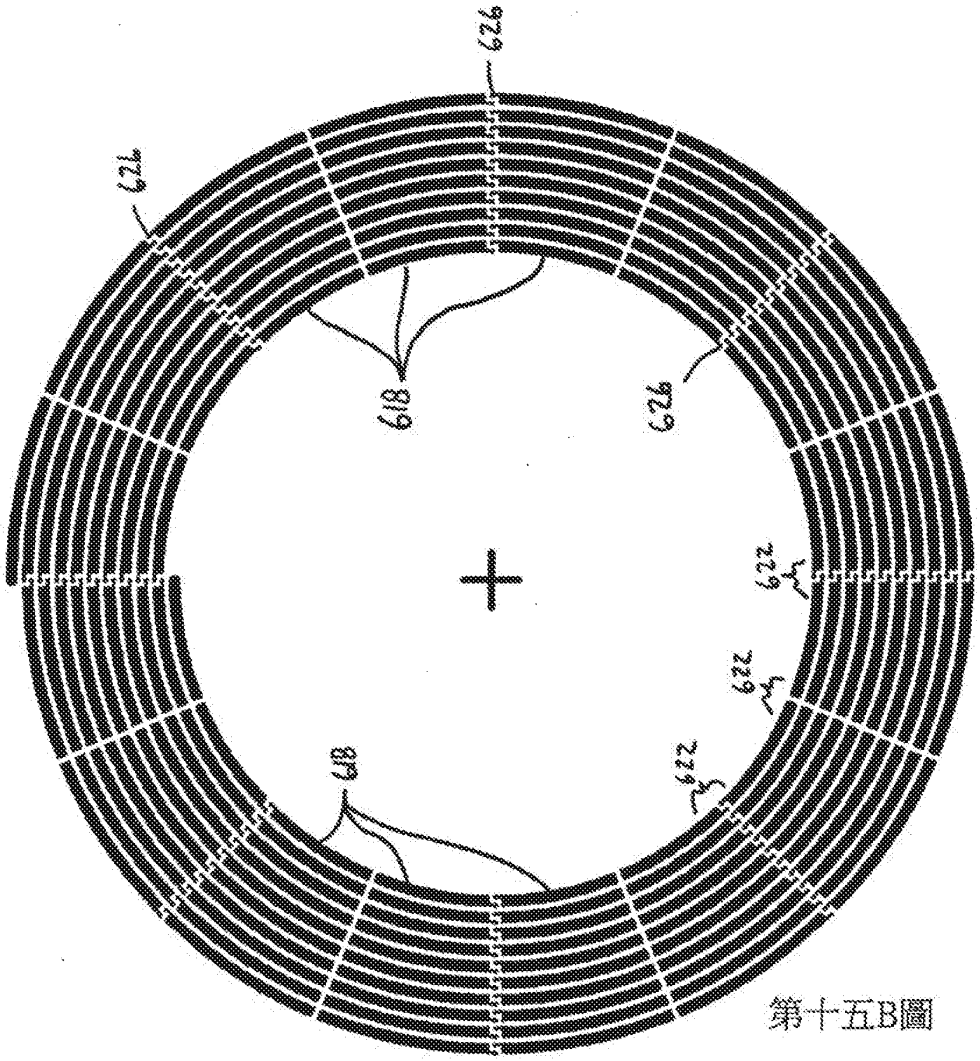

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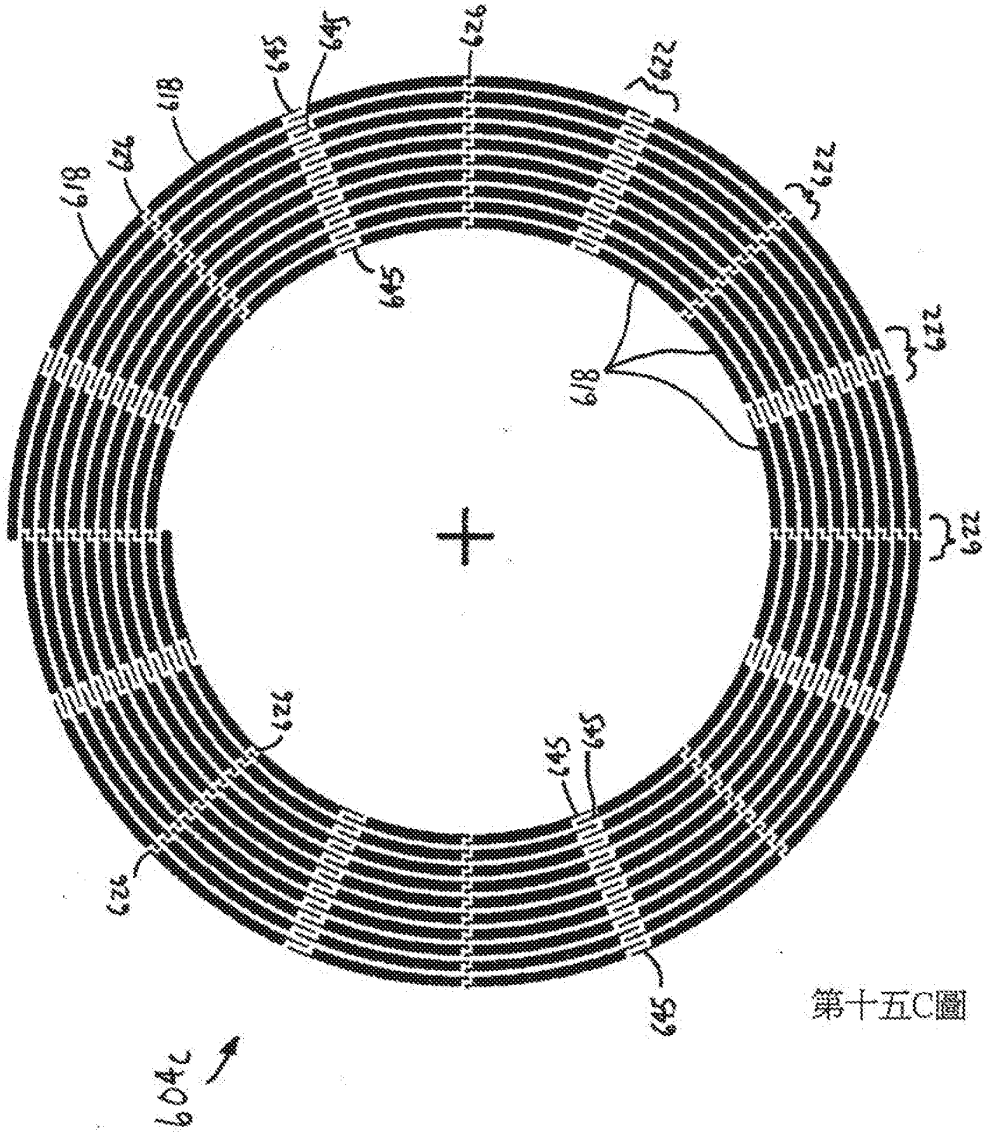

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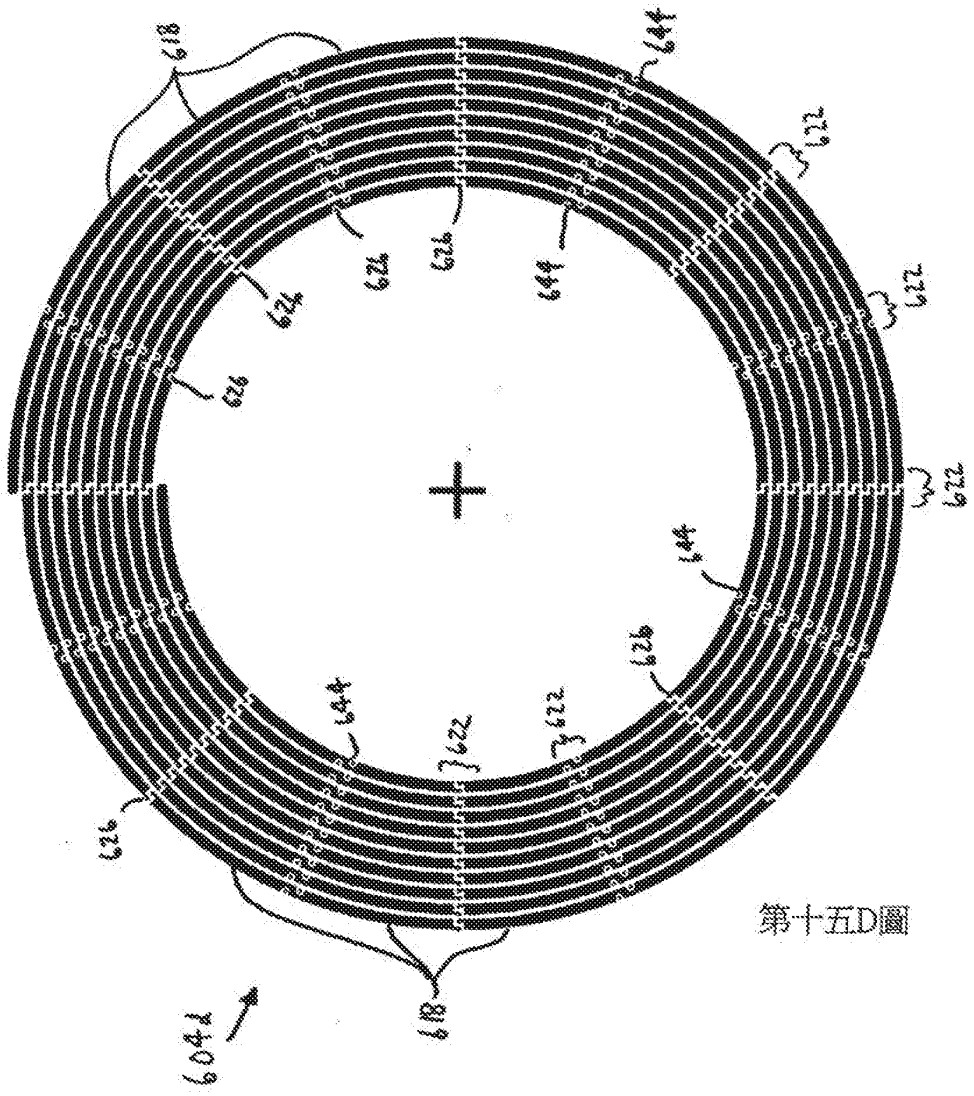
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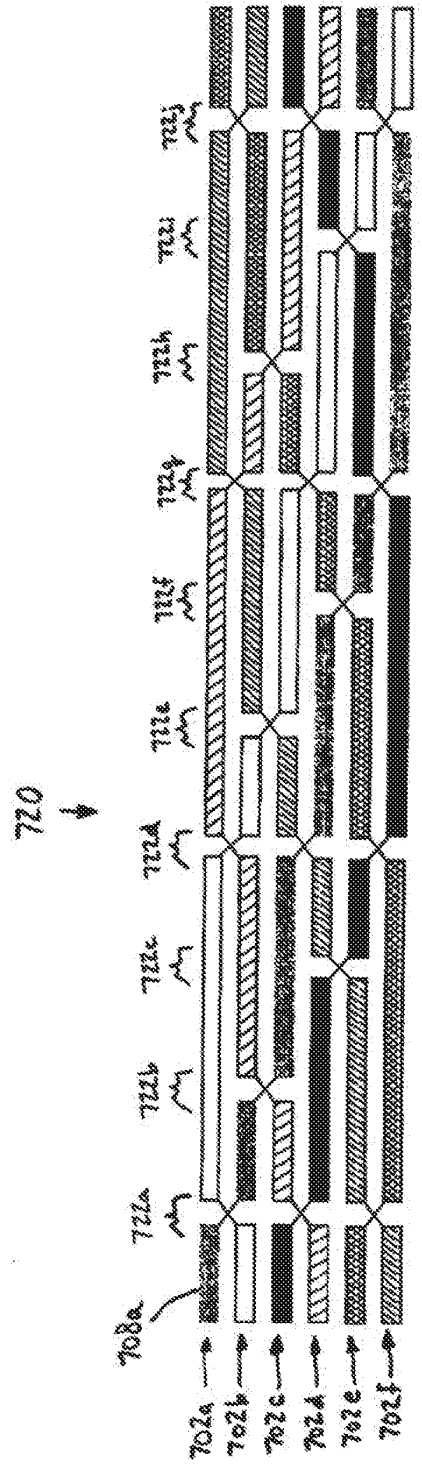
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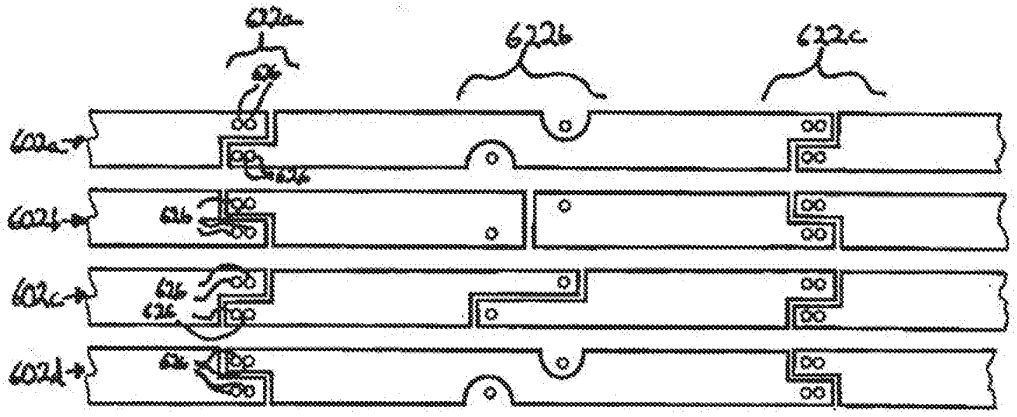


第十八圖

四、指定代表圖：

(一)本案指定代表圖為：第（ 一A ）圖。

(二)本代表圖之元件符號簡單說明：

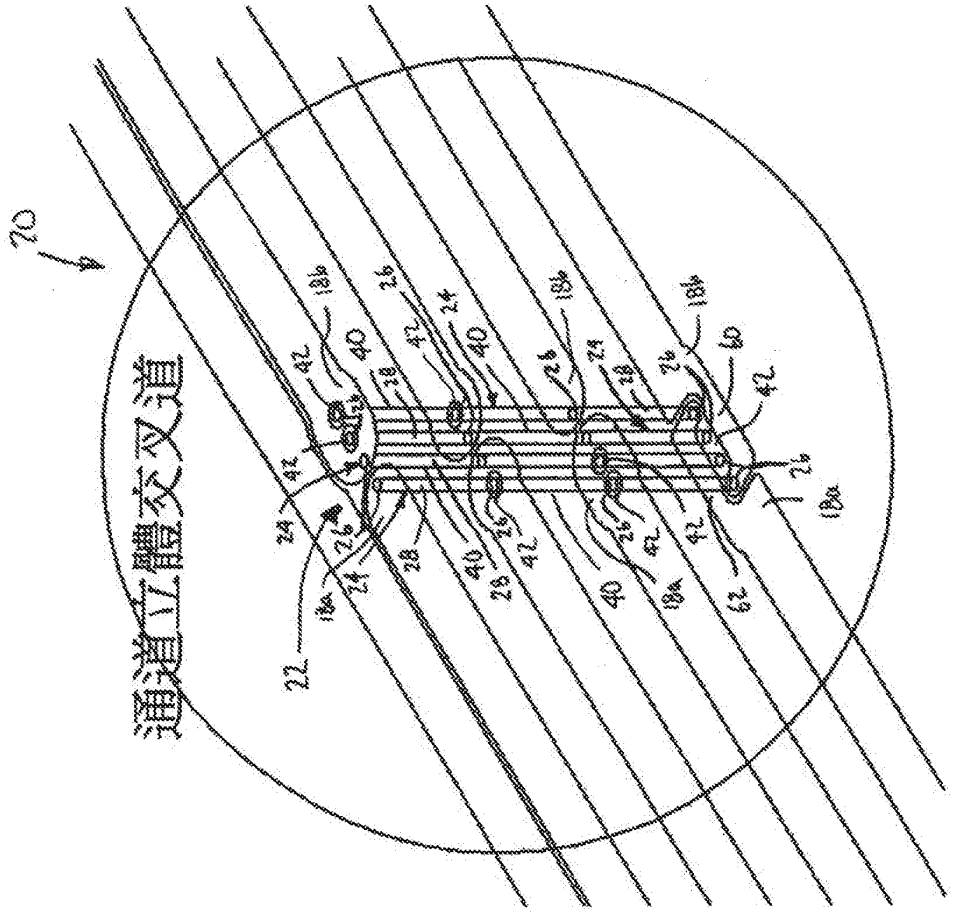
12 多層電路板

14a-d 交流導體層

16a-c 絕緣層

20 印刷電路板(PCB)線圈

五、本案若有化學式時，請揭示最能顯示發明特徵的化學式：



第七圖

Electronic Acknowledgement Receipt

EFS ID:	35618828
Application Number:	16182258
International Application Number:	
Confirmation Number:	1026
Title of Invention:	Wireless Power Receiver and Control Method Thereof
First Named Inventor/Applicant Name:	Ki Min LEE
Customer Number:	23557
Filer:	Jeff Lloyd/Natalie Stevenson
Filer Authorized By:	Jeff Lloyd
Attorney Docket Number:	SUN.LGI.417D3
Receipt Date:	03-APR-2019
Filing Date:	06-NOV-2018
Time Stamp:	16:05:48
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		SIDS1-AF.pdf	271865 ff2c75b8c47c513c3a8f26150f39f44f8f55f8a8	yes	4

	Multipart Description/PDF files in .zip description				
	Document Description	**Start**	**End**		
	Transmittal Letter	1	2		
	Information Disclosure Statement (IDS) Form (SB08)	3	4		
Warnings:					
Information:					
2	Foreign Reference	F1.pdf	9362493 58211697e4f6139d21a541af8db08481d23cbcc4	no	52
Warnings:					
Information:					
3	Foreign Reference	F2.pdf	7023549 74f33650af88385b6fd67309ba99d8193c6c6b31	no	54
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		Total Files Size (in bytes):	130715368		

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

I hereby certify that this correspondence is being electronically filed in the United States Patent and Trademark Office on April 3, 2019.

/NATALIE STEVENSON/

Natalie Stevenson

SUPPLEMENTAL INFORMATION
DISCLOSURE STATEMENT
UNDER 37 C.F.R §§ 1.97 AND 1.98
Examining Group 2683
Patent Application
Docket No. SUN.LGI.417D3
Serial No. 16/182,258

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Art Unit	:	2683
Applicants	:	Ki Min Lee, Jung Oh Lee
Serial No.	:	16/182,258
Filed	:	November 6, 2018
Conf. No.	:	1026
For	:	Wireless Power Receiver and Control Method Thereof

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT
UNDER 37 C.F.R. §§ 1.97 AND 1.98

Sir:

In accordance with 37 C.F.R. § 1.56, the references listed on the attached form PTO/SB/08 are being brought to the attention of the Examiner for consideration in connection with the examination of the patent application identified above. Copies of the cited references are attached. However, Applicants have not submitted copies of the U.S. Patents and published U.S. Patent Application cited on attached Form PTO/SB/08 pursuant to 37 CFR 1.98(a)(2)(ii).

The undersigned hereby certifies that each item of information contained in this Supplemental Information Disclosure Statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Supplemental Information Disclosure Statement. Applicants are attaching a copy of the Taiwanese Office Action.

J:\SUN\LGI\417D3\IDS-Refs\4-3-19\SIDS1.doc/njs

It is respectfully requested that the Examiner indicate consideration of the cited references by returning a copy of the attached form PTO/SB/08 with initials or other appropriate marks.

Applicants respectfully assert that the substantive provisions of 37 C.F.R. §§ 1.56, 1.97, and 1.98 are met by the foregoing statements.

The Commissioner is hereby authorized to charge any fees under 37 C.F.R. §§ 1.16 or 1.17 as required by this paper to Deposit Account 19-0065.

Respectfully submitted,

/JEFF LLOYD/

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JL/njs

Attachments: Form PTO/SB/08; copies of references cited.

J:\SUN\LGI\417D3\IDS-Refs\4-3-19\SIDS1.doc/njs

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G01L 7/00 (2006.01) *G06F 19/00* (2006.01)

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11 March 2010 (11.03.2010)

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61/164,473 30 March 2009 (30.03.2009) US

(71) Applicant *(for all designated States except US)*: **MEGICA CORPORATION**; 8F.-1, No 29, Puding Road, East District, Hsin-Chu, 30072 (TW).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **LIN, Mou-Shiung** [US/—]; 28 Ginsan 10th Street, Hsin-Chu, 30072 (TW). **LEE, Jin-Yuan**; No. 11, Lane 4, An-Ho Street, Hsin-Chu, 30072 (TW). **LO, Hsin-Jung**; 11F-1, No. 274 Yongjhen Road, Jhonghe City, Taipei County (TW). **YANG, Ping-Jung**; 2 Nioupu S. Road, Siangshan District, Hsinchu, 30072 (TW). **LIU, Te-Sheng**; No. 41, Li-oujia 6th Street, Jhubei City, Hsinchu County (TW).

(74) Agents: **DUCHENE, Dennis.** et al.; McDermott Will & Emery LLP, 11682 El Camino Real, Suite 400, San Diego, CA 92130-2047 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

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— *with amended claims (Art. 19(1))*

(54) Title: INTEGRATED CIRCUIT CHIP USING TOP POST-PASSIVATION TECHNOLOGY AND BOTTOM STRUCTURE TECHNOLOGY

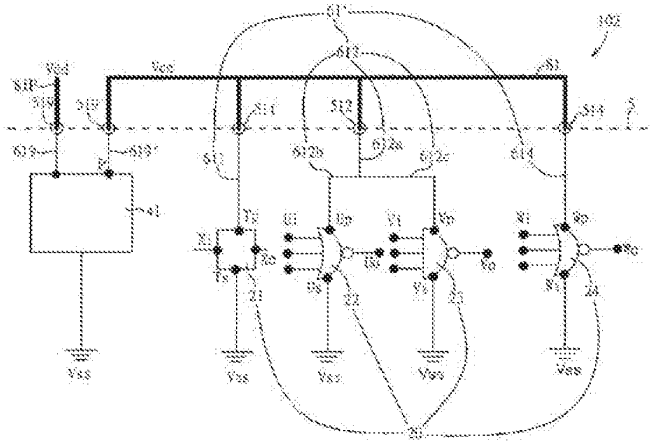

Fig. 1B

(57) Abstract: Integrated circuit chips and chip packages are disclosed that include an over-passivation scheme at a top of the integrated circuit chip and a bottom scheme at a bottom of the integrated circuit chip using a top post-passivation technology and a bottom structure technology. The integrated circuit chips can be connected to an external circuit or structure, such as ball-grid-array (BGA) substrate, printed circuit board, semiconductor chip, metal substrate, glass substrate or ceramic substrate, through the over-passivation scheme or the bottom scheme. Related fabrication techniques are described.

WO 2010/114687 A1

INTEGRATED CIRCUIT CHIP USING TOP POST-PASSIVATION TECHNOLOGY AND BOTTOM STRUCTURE TECHNOLOGY

[0001] This application claims priority to U.S. provisional application No. 61/164,473, filed on Mar. 30, 2009, which is herein incorporated by reference in its entirety.

BACKGROUND OF THE DISCLOSURE

Field of the Disclosure

[0002] The disclosure relates to integrated circuit chips and chip packages, and more particularly, to integrated circuit chips and packages that utilize differing interconnection schemes for different sides of the circuit chips and packages.

Brief Description of the Related Art

[0003] Semiconductor chips can be found in many electronic devices, and today many electronic devices are required to run at high speed and/or low power consumption conditions. In traditional semiconductor fabrication, a chip can use wirebonding wires or solder balls bonded with pads, exposed by openings in a passivation layer of the chip, of the chip to connect with a ball grid array (BGA) substrate. Modern electronic systems, modules, and/or circuit boards typically contain many different types of chips, such central processing units (CPUs), digital signal processors (DSPs), analog chips, dynamic random access memory (DRAM) chips, static random access memory (SRAM) chips, flash memory chips, and the like.

[0004] Each chip is typically fabricated using different types and/or different generations of IC manufacturing process technologies. For example, in some notebook personal computers, a CPU chip might be fabricated using a 65 nm IC process technology with a power supply voltage of 1.2V, an analog chip might be fabricated using an older 0.25 micron (250 nm) IC process technology with a power supply voltage of 3.3V, and a DRAM chip might be fabricated using a 90 nm IC process technology at 1.5V, and a flash memory chip might be fabricated using a 0.18 micron (180 nm) IC process technology with power supply voltage at 2.5V.

[0005] Each different type of chip can require a different voltage requirement for its supplied power. For example, a given DRAM chip might require an on-chip voltage converter to convert 3.3V to 1.5V while a flash memory chip might at the same time require an on-chip

voltage converter to convert 3.3V to 2.5V. With a variety of supply voltages in a single system, voltage regulation and conversion can be problematic, complicated, and costly.

[0006] Interconnection schemes include the metal connections that connect an IC to other circuit or system components. Such interconnection schemes have become of relative importance and have, with the further miniaturization of the IC, an increasingly negative impact on the circuit performance, including for chip voltage and regulation. For example, the parasitic capacitance and resistance of the metal interconnections increase with smaller scale, which degrades the chip performance significantly. Of significant concern in this respect is the voltage drop along the power and ground buses and the RC delay of the critical signal paths. Attempts to reduce the resistance by using wider metal lines result in higher capacitance of these wires.

[0007] To solve this problem, one approach has been to develop low resistance metal (such as copper) for the wires while low dielectric materials are used in between signal lines. Current practice is to create metal interconnection networks under a layer of passivation, this approach however limits the interconnect network to fine line interconnects and the therewith associated high parasitic capacitance and high line resistivity. The latter two parameters, because of their relatively high values, degrade device performance, an effect which becomes even more severe for higher frequency applications and for long interconnect lines that are, for instance, used for clock distribution lines. Also, fine line interconnect metal cannot carry high values of current that is typically needed for ground busses and for power busses.

SUMMARY OF THE DISCLOSURE

[0008] The present disclosure is directed to integrated circuit chips and chip packages that utilize over-passivation and bottom interconnection schemes (or, "technologies") for the respective major sides of the chip or chip packages.

[0009] An aspect of the present disclosure is directed to chips or chip packages including one interconnection scheme at one side of a chip or chip package and/or another interconnection scheme at another side of a chip or chip package, e.g., an over-passivation scheme at a top of a chip and a bottom scheme at a bottom of the same chip. The integrated circuit chips can be connected to an external circuit or structure, such as ball-grid-array (BGA) substrate, printed circuit board, semiconductor chip, metal substrate, glass substrate or ceramic substrate, through the over-passivation scheme or the bottom scheme.

[0010] Another aspect of the present disclosure is directed to on-chip voltage-regulating and/or converting devices and circuits.

[0011] Exemplary embodiments of the present disclosure provide chips having an over-passivation scheme at a passivation layer of the chip and a bottom scheme at a backside of a semiconductor substrate of the chip. Exemplary embodiments can include post-passivation schemes for either side of a chip or chip package, e.g., a top of a chip or bottom (backside) of a chip.

[0012] Exemplary embodiments of the present disclosure can provide on-chip voltage-regulating and/or converting devices or circuits that can send electrical power to multiple devices or circuit units (e.g., sub circuits or circuitry portions) requiring different voltage characteristics.

[0013] Furthermore, exemplary embodiments can supply voltage or power to one or more devices or circuit units with little loss due to parasitic effects.

[0014] Further embodiments can provide for the delivery of electrical power to one or more devices or circuit units through a passivation layer and by way of a coarse conductor deposited over the passivation layer.

[0015] Embodiments can further provide an over-passivation metal interconnection that can distribute signals, power, and/or ground output from at least one internal circuit or internal device to at least one other internal circuit or device. Exemplary embodiment can provide for such without connection to ESD, driver, or receiver circuitry.

[0016] Embodiments can further provide an over-passivation metal interconnection that can distribute signals, power, and/or ground output from at least one internal circuit or internal device to at least one other internal circuit or device and/or to external (outside of chip) circuitry, including other chips and chip packages according to the present disclosure.

[0017] These, as well as other components, steps, features, benefits, and advantages of the present disclosure, will now become clear from a review of the following detailed description of illustrative embodiments, the accompanying drawings, and the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] The drawings disclose illustrative embodiments of the present disclosure. They do not set forth all embodiments. Other embodiments may be used in addition or instead. Details that may be apparent or unnecessary may be omitted to save space or for more effective

illustration. Conversely, some embodiments may be practiced without all of the details that are disclosed. When the same numeral appears in different drawings, it refers to the same or like components or steps.

[0019] Aspects of the disclosure may be more fully understood from the following description when read together with the accompanying drawings, which are to be regarded as illustrative in nature, and not as limiting. The drawings are not necessarily to scale, emphasis instead being placed on the principles of the disclosure.

[0020] Fig. 1A is a schematic representation of a prior art voltage regulator or converter circuit connected to multiple internal circuits through a fine-line metallization.

[0021] Fig. 1B is a schematic representation of a voltage regulator or converter circuit connected to multiple internal circuits through an over-passivation power bus (metal line, trace, or plane), according to an embodiment.

[0022] Figs. 1C and 1D are schematic representation of a voltage regulator or a voltage converter connected to multiple internal circuits through over-passivation power and ground buses (metal lines, traces, or planes), according to an embodiment.

[0023] Fig. 2A is a top view layout of a prior art voltage regulator or converter circuit connected to multiple internal circuits through a fine-line metallization.

[0024] Fig. 2B is a top view layout of a voltage regulator or converter circuit connected to multiple internal circuits through an over-passivation power bus (metal line, trace or plane), according to an embodiment.

[0025] Fig. 2C is a top view layout of a voltage regulator or converter circuit connected to multiple internal circuits through over-passivation power and ground buses (metal lines, traces or planes), according to an embodiment.

[0026] Fig. 3A is a cross-sectional representation of a prior art voltage regulator or converter circuit connected to multiple internal circuits through a fine-line metallization.

[0027] Fig. 3B is a cross-sectional representation of a voltage regulator or converter circuit connected to multiple internal circuits through an over-passivation power bus (metal line, trace or bus), according to an embodiment.

[0028] Fig. 3C is a cross-sectional representation of a voltage regulator or converter circuit connected to multiple internal circuits through over-passivation power and ground buses (metal lines, traces or planes in two patterned circuit metal layers), according to an embodiment.

[0029] Fig. 3D is a cross-sectional representation of a voltage regulator or converter circuit connected to multiple internal circuits through an over-passivation power bus (metal line, trace or bus), according to an embodiment. This figure is similar to Fig. 3B except that an additional polymer layer is provided between the bottom-most over-passivation metal layer and the passivation layer.

[0030] Fig. 4 is a schematic representation of an example of a CMOS voltage converter circuit, according to an embodiment.

[0031] Fig. 5A is a schematic representation of multiple internal circuits connected through a fine-line metallization structure under a passivation layer, according to an embodiment.

[0032] Fig. 5B is a schematic representation of multiple internal circuits connected through a thick and wide metal layer over a passivation layer to transmit a signal, according to an embodiment.

[0033] Fig. 5C shows a circuit diagram of an inverter, which can be applied to the internal circuit 21 shown in Fig. 5B, according to an embodiment.

[0034] Fig. 5D shows a circuit diagram of an internal driver, which can be applied to the internal circuit 21 shown in Fig. 5B, according to an embodiment.

[0035] Fig. 5E shows a circuit diagram of a tri-state buffer, which can be applied to the internal circuit 21 shown in Fig. 5B, according to an embodiment.

[0036] Fig. 5F shows a circuit diagram of a tri-state buffer, which can be applied to the internal circuit 21 shown in Fig. 5B, connected to a sense amplifier connected to a memory cell, according to an embodiment.

[0037] Fig. 5G shows a circuit diagram of a gate switch, which can be applied to the internal circuit 21 shown in Fig. 5B, connected to a sense amplifier connected to a memory cell, according to an embodiment.

[0038] Fig. 5H shows a circuit diagram of a latch circuit, which can be applied to the internal circuit 21 shown in Fig. 5B, connected to a sense amplifier connected to a memory cell, according to an embodiment.

[0039] Fig. 5I shows a circuit diagram of a gate switch and internal driver, which can be applied to the internal circuit 21 shown in Fig. 5B, connected to a sense amplifier connected to a memory cell, according to an embodiment.

[0040] Fig. 5J shows a circuit diagram of a latch circuit and internal driver, which can be applied to the internal circuit 21 shown in Fig. 5B, connected to a sense amplifier connected to a memory cell, according to an embodiment.

[0041] Fig. 5K is a schematic representation of multiple internal circuits connected through a thick and wide metal layer over a passivation layer to transmit a signal, according to an embodiment.

[0042] Fig. 5L shows a circuit diagram of an internal receiver, which can be applied to the internal circuit 21 shown in Fig. 5K, according to an embodiment.

[0043] Fig. 5M shows a circuit diagram of a tri-state buffer, which can be applied to the internal circuit 21 shown in Fig. 5K, according to an embodiment.

[0044] Fig. 5N shows a circuit diagram of a tri-state buffer, which can be applied to the internal circuit 21 shown in Fig. 5K, connected to a sense amplifier connected to a memory cell, according to an embodiment.

[0045] Fig. 5O shows a circuit diagram of a gate switch, which can be applied to the internal circuit 21 shown in Fig. 5K, connected to a sense amplifier connected to a memory cell, according to an embodiment.

[0046] Fig. 5P shows a circuit diagram of a latch circuit, which can be applied to the internal circuit 21 shown in Fig. 5K, connected to a sense amplifier connected to a memory cell, according to an embodiment.

[0047] Fig. 5Q shows a circuit diagram of a gate switch and internal receiver, which can be applied to the internal circuit 21 shown in Fig. 5K, connected to a sense amplifier connected to a memory cell, according to an embodiment.

[0048] Fig. 5R shows a circuit diagram of a latch circuit and internal receiver, which can be applied to the internal circuit 21 shown in Fig. 5K, connected to a sense amplifier connected to a memory cell, according to an embodiment.

[0049] Fig. 5S is a schematic representation of multiple internal circuits connected through a thick and wide metal layer over a passivation layer to transmit an analog signal, according to an embodiment.

[0050] Fig. 5T shows a circuit diagram of a differential amplifier, which can be applied to the internal circuit 21 shown in Fig. 5S, according to an embodiment.

[0051] Figs. 5U-5Z show a schematic representation of a memory chip with an address bus and a data bus over a passivation layer, according to an embodiment.

[0052] Fig. 6A is a top view layout of a distribution of signals from an internal circuit to other internal circuits, according to an embodiment.

[0053] Fig. 6B is a top view layout of signal distribution, and an internal circuit sends signals to other internal circuits through an over-passivation interconnection scheme, requiring no solder bump and no off-chip circuits, according to an embodiment.

[0054] Fig. 7A is a cross-sectional representation of a distribution of signals from an internal circuit to other internal circuits, according to an embodiment.

[0055] Fig. 7B is a cross-sectional representation of signal distribution, and an internal circuit sends signals to other internal circuits through an over-passivation interconnection scheme, requiring no solder bump and no off-chip circuits, according to an embodiment.

[0056] Fig. 7C is a cross-sectional representation of signal distribution, and an internal circuit sends signals to other internal circuits through an over-passivation scheme, requiring no solder bump and no off-chip circuits, according to an embodiment. Two over-passivation scheme includes two metal layers.

[0057] Fig. 7D is a cross-sectional representation of signal distribution, and an internal circuit sends signals to other internal circuits through an over-passivation interconnection scheme, according to an embodiment. This figure is similar to Fig. 7B except that an additional polymer layer is provided between the passivation layer and the bottom-most over-passivation metal layer.

[0058] Fig. 8A is a schematic representation of a distribution of signals from internal circuits to the external circuits through off-chip circuits using fine-line scheme, according to an embodiment.

[0059] Figs. 8B, 8D, 8E and 8F are schematic representations of a signal generated in the internal circuits propagated to an external circuit through over-passivation metals and fine-line metals, and through off-chip circuits, according to an embodiment.

[0060] Fig. 8C is a schematic representation of a signal transmitted from an external circuit to an internal circuit through over-passivation metals and fine-line metals, and through off-chip circuits, according to an embodiment.

[0061] Fig. 9A is a top view layout of a distribution of signals from internal circuits to the external circuits through off-chip circuits using a fine-line scheme, according to an embodiment.

[0062] Figs. 9B is a top view layout of multiple internal circuits connected to an off-chip circuit through a thick and wide metal trace, bus or plane over a passivation layer, according to an embodiment.

[0063] Fig. 9C is a top view layout of multiple internal circuits connected to an off-chip circuit through a thick and wide metal trace, bus or plane over a passivation layer, and the off-chip circuit includes two-stage cascade off-chip driver 421, according to an embodiment.

[0064] Fig. 9D is a top view layout of multiple internal circuits connected to an off-chip circuit through a thick and wide metal trace, bus or plane over a passivation layer, and the off-chip circuit includes four-stage cascade off-chip driver 42, according to an embodiment.

[0065] Fig. 10A is a cross-sectional representation of a distribution of signals from internal circuits to the external circuits through off-chip circuits using fine-line scheme, according to an embodiment.

[0066] Figs. 10B-10E and 10G-10I are cross-sectional representations of multiple internal circuits connected to an off-chip circuit through a thick and wide metal trace, bus or plane over a passivation layer, according to an embodiment.

[0067] Fig. 10F is a cross-sectional representation of multiple internal circuits connected to an off-chip circuit through a metal trace, bus or plane under a passivation layer, with a wire wirebonded to a relocated pad on a passivation layer, according to an embodiment.

[0068] Fig. 11A is a schematic representation of an example of an off-chip driver circuit, which can be applied to the off-chip buffer 42 shown in Fig. 8B, according to an embodiment.

[0069] Fig. 11B is a schematic representation of an example of an off-chip receiver circuit, which can be applied to the off-chip buffer 42 shown in Fig. 8C, according to an embodiment.

[0070] Fig. 11C is a schematic representation of an example of an off-chip tri-state buffer, which can be applied to the off-chip buffer 42 shown in Fig. 8B, according to an embodiment.

[0071] Fig. 11D is a schematic representation of an example of an off-chip driver circuit, which can be applied to the off-chip buffer 42 shown in Fig. 8E, according to an embodiment.

[0072] Fig. 11E is a schematic representation of an example of an off-chip tri-state buffer, which can be applied to the off-chip buffer 42 shown in Fig. 8C, according to an embodiment.

[0073] Fig. 11F is a schematic representation of an example of an ESD connection, which can be applied to the off-chip ESD circuit 43 shown in Figs. 8B, 8C, 8E and 8F, according to an embodiment.

[0074] Fig. 11G is a schematic representation of an example of a four-stage cascade off-chip driver circuit, which can be applied to the off-chip buffer 42 shown in Fig. 8F, according to an embodiment.

[0075] Fig. 11H is a schematic representation of an example of two ESD connections, which can be applied to the off-chip ESD circuit 43 shown in Fig. 8D, according to an embodiment.

[0076] Fig. 12A is a schematic representation of a distribution of external power supply to internal circuits, according to an embodiment.

[0077] Fig. 12B is a schematic representation of distribution of external power supply to internal circuits through over-passivation metals, according to an embodiment. An ESD protection circuit is connected to the over-passivation metals.

[0078] Fig. 12C is a schematic representation of distribution of external power supply and external ground to internal circuits through over-passivation metals, according to an embodiment. Both power and ground nodes of internal circuits are connected to the over-passivation metals. An ESD circuit is connected to the over-passivation metals.

[0079] Fig. 12D is a schematic representation of distribution of external power supply and external ground to internal circuits through over-passivation metals, according to an embodiment. More than one ESD circuits are connected to the over-passivation metals.

[0080] Fig. 12E is a schematic representation of an example of an ESD circuit, which can be applied to the ESD circuit 44 or 45 shown in Figs. 12B-12D, according to an embodiment.

[0081] Fig. 13A is a top view layout of a distribution of external power supply to internal circuits, according to an embodiment.

[0082] Fig. 13B is a top view layout of distribution of external power supply to internal circuits through over-passivation metals, according to an embodiment. An ESD protection circuit is connected to the over-passivation metals.

[0083] Fig. 13C is a top view layout of distribution of external power supply and external ground to internal circuits through over-passivation, according to an embodiment. Both power and ground nodes of internal circuits are connected to the over-passivation metals. An ESD protection circuit is connected to the over-passivation power and ground traces, buses or planes.

[0084] Fig. 14A is a cross-sectional representation of a distribution of external power supply to internal circuits, according to an embodiment.

[0085] Fig. 14B is a cross-sectional representation of distribution of external power supply to internal circuits through over-passivation metals, according to an embodiment. An ESD protection circuit is connected to the over-passivation metals.

[0086] Fig. 14C is a cross-sectional representation of distribution of external power supply and external ground to internal circuits through over-passivation metals, according to an embodiment. Both power and ground nodes of internal circuits are connected to the over-passivation metals. The power lines, traces or planes are in the second over-passivation metal layer, while the ground lines, traces or planes are in the first over-passivation metal layer under the second over-passivation metal layer. An ESD protection circuit is connected to the over-passivation metals.

[0087] Fig. 14D is a cross-sectional representation of distribution of external power supply to internal circuits through over-passivation metals, according to an embodiment. An ESD protection circuit is connected to the over-passivation metals. This figure is similar to Fig. 14B except that an additional polymer layer is formed between the bottom-most over-passivation metal layer and the passivation layer.

[0088] Fig. 15A and Fig. 15B are depictions of starting materials, according to an embodiment. The starting materials are wafers. An over-passivation scheme of present

disclosure is to be built over the wafer. Fig. 15B differs from Fig. 15A in having an optional metal cap over a metal pad or trace exposed by an opening in the passivation layer.

[0089] Fig. 15C to Fig. 15L show process steps of forming an over-passivation scheme with two metal layers, with each metal layer being formed by an embossing process, according to an embodiment.

[0090] Fig. 15M is a cross-sectional view showing a process of forming a semiconductor wafer including an over-passivation scheme at a passivation layer of the semiconductor wafer, according to an embodiment.

[0091] Fig. 16A to Fig. 16M show process steps of forming an over-passivation scheme with two metal layers, in which the first over-passivation metal layer is formed by a double-embossing process, while the second over-passivation metal layer is formed by a single-embossing (an embossing) process, according to an embodiment.

[0092] Fig. 17A to Fig. 17J show process steps of forming an over-passivation scheme with three metal layers, according to an embodiment. The first and second over-passivation metal layers are formed by a suitable process or processes, e.g., by a double-embossing process, while the third (top-most) over-passivation metal layer is formed by a suitable process or processes, e.g., by a single-embossing (an embossing) process.

[0093] Fig. 18A to Fig. 18I show process steps of forming an over-passivation scheme with three metal layers, according to an embodiment. The first and third over-passivation metal layers are formed by a suitable process or processes, e.g., by a single-embossing (an embossing) process, while the second over-passivation metal layer is formed by a suitable process or processes, e.g., by a double-embossing process.

[0094] Fig. 19A to Fig. 19I show process steps of forming an over-passivation scheme with two metal layers, according to an embodiment. The first over-passivation metal layer is formed by a suitable process or processes, e.g., by a double-embossing process, while the second (top-most) over-passivation metal layer is formed by a suitable process or processes, e.g., by a single-embossing (an embossing) process.

[0095] Fig. 20 illustrates models for calculating capacitance per unit length for metal lines or traces in the over-passivation scheme and the fine-line scheme, according to an embodiment.

[0096] Figs. 21 and 22 show top views of a MOS transistor that can be a PMOS transistor or an NMOS transistor, according to an embodiment.

[0097] Figs. 23A-23M show cross-sectional views for packaging a DRAM chip, according to an embodiment.

[0098] Fig. 23N shows a top view of a chip package for a DRAM chip, according to an embodiment.

[0099] Fig. 24A shows a cross-sectional view of a semiconductor wafer, according to an embodiment.

[00100] Fig. 24B is a cross-sectional view showing a process of thinning a silicon substrate of the semiconductor wafer shown in Fig. 24A, according to an embodiment.

[00101] Fig. 24C is a cross-sectional view of the semiconductor wafer, shown in Fig. 24B, including through-silicon vias in the silicon substrate of the semiconductor wafer and including an insulating layer on sidewalls of the through-silicon vias and on a backside of the silicon substrate, according to an embodiment.

[00102] Figs. 24D-24H are cross-sectional views showing a process of forming through-silicon vias in the silicon substrate of the semiconductor wafer shown in Fig. 24B and forming an insulating layer on sidewalls of the through-silicon vias and on a backside of the silicon substrate, according to an embodiment.

[00103] Figs. 24I-24N are cross-sectional views showing another process of forming through-silicon vias in the silicon substrate of the semiconductor wafer shown in Fig. 24B and forming an insulating layer on sidewalls of the through-silicon vias and on a backside of the silicon substrate, according to an embodiment.

[00104] Figs. 25A-25L are cross-sectional views showing a process for forming a bottom scheme of a bottom structure technology at a backside of the semiconductor wafer shown in Fig. 24C, according to an embodiment.

[00105] Figs. 25M-25T are cross-sectional views of semiconductor wafers, according to an embodiment.

[00106] Figs. 25U, 25V and 25W are cross-sectional views of packages, according to an embodiment.

[00107] Figs. 26A-26G are cross-sectional views showing a process for forming a bottom scheme of a bottom structure technology at a backside of the semiconductor wafer shown in Fig. 24C, according to an embodiment.

[00108] Figs. 26H-26K are cross-sectional views of semiconductor wafers, according to an embodiment.

[00109] Figs. 27A-27Q are cross-sectional views showing a process for forming a bottom scheme of a bottom structure technology at a backside of the semiconductor wafer shown in Fig. 24C, according to an embodiment.

[00110] Figs. 27R-27T are cross-sectional views of semiconductor wafers, according to an embodiment.

[00111] Figs. 28A-28F are cross-sectional views showing a process for forming a bottom scheme of a bottom structure technology at a backside of the semiconductor wafer shown in Fig. 24C, according to an embodiment.

[00112] Figs. 28G-28I are cross-sectional views of semiconductor wafers, according to an embodiment.

[00113] Fig. 28J is a cross-sectional view of a chip package, according to an embodiment.

[00114] Figs. 29A-29T show simplified circuit diagrams of semiconductor chips, according to an embodiment.

[00115] Figs. 30A-30I are cross-sectional views showing a process for forming a bottom scheme of a bottom structure technology at a backside of a semiconductor wafer, according to an embodiment.

[00116] Figs. 30J, 30K and 30L are cross-sectional views showing a process for forming a semiconductor wafer including an over-passivation scheme at a passivation layer of the semiconductor wafer and a bottom scheme at a backside of the semiconductor wafer, according to an embodiment.

[00117] Figs. 30M and 30N are cross-sectional views showing a process for forming a semiconductor wafer including metal pads, bumps or traces at an active side of a silicon substrate of the semiconductor wafer and including a bottom scheme at a backside of the silicon side, according to an embodiment.

[00118] Figs. 31A-31G are cross-sectional views showing a process for forming a bottom scheme of a bottom structure technology at a backside of a semiconductor wafer, according to an embodiment.

[00119] Figs. 31H and 31I are cross sectional views showing a process for forming a semiconductor wafer including an over-passivation scheme at a passivation layer of the semiconductor wafer and a bottom scheme at a backside of the semiconductor wafer, according to an embodiment.

[00120] Fig. 31J is a cross sectional view showing a process for forming a semiconductor wafer including metal pads, bumps or traces at an active side of a silicon substrate of the semiconductor wafer and including a bottom scheme at a backside of the silicon side, according to an embodiment.

[00121] Figs. 32A-32R are cross-sectional views showing a process for forming a bottom scheme of a bottom structure technology at a backside of a semiconductor wafer, according to an embodiment.

[00122] Figs. 32S and 32T are cross sectional views showing a process for forming a semiconductor wafer including metal pads, bumps or traces at an active side of a silicon substrate of the semiconductor wafer and including a bottom scheme at a backside of the silicon side, according to an embodiment.

[00123] Fig. 32U is a cross sectional view showing a process for forming a semiconductor wafer, according to an embodiment.

[00124] Figs. 33A-33K are cross-sectional views showing a process for forming a bottom scheme of a bottom structure technology at a backside of a semiconductor wafer, according to an embodiment.

[00125] Fig. 33L is a cross sectional view showing the semiconductor wafer illustrated in Fig. 33K with an over-passivation scheme at an active side of a silicon substrate of the semiconductor wafer, according to an embodiment.

[00126] Fig. 33M is a cross sectional view showing the semiconductor wafer illustrated in Fig. 33K with metal pads, bumps or traces at an active side of a silicon substrate of the semiconductor wafer, according to an embodiment.

[00127] Figs. 33N-33S are cross-sectional views showing a process for forming a bottom scheme of a bottom structure technology at a backside of a semiconductor wafer, according to an embodiment.

[00128] Figs. 33T and 33U are cross sectional views of semiconductor wafers, according to an embodiment.

[00129] Fig. 33V shows a top view of a capacitor of a semiconductor wafer, according to an embodiment.

[00130] Fig. 33W shows a cross sectional view cut along the dot line A-A in Fig. 33V, according to an embodiment.

[00131] Fig. 33X shows a top view of a capacitor of a semiconductor wafer, according to an embodiment.

[00132] Fig. 33Y shows a cross sectional view cut along the dot line A-A in Fig. 33X, according to an embodiment.

[00133] Figs. 34A-34G are cross sectional views showing a process of forming a super capacitor, a patterned circuit layer, metal bumps or pillars and two polymer layers at passivation layer of a semiconductor wafer, according to an embodiment.

[00134] Figs. 35A-35D are cross sectional views showing a process of forming a semiconductor wafer including an over-passivation scheme at a passivation layer of the semiconductor wafer and including a bottom scheme, a discrete inductor and a discrete capacitor at a backside of the semiconductor wafer, according to an embodiment.

[00135] Figs. 36A-36D are cross sectional views of chip-package modules, according to an embodiment.

[00136] Figs. 37A-37D and 38A-38D are cross sectional views of modules, according to an embodiment.

[00137] Figs. 39A, 39H, 39I and 39J are circuit diagrams each showing interface circuits of a cache memory chip and a chip, according to an embodiment.

[00138] Figs. 39B and 39C show circuit diagrams of inter-chip circuits in a cache memory chip, according to an embodiment.

[00139] Figs. 39D and 39E show circuit diagrams of inter-chip circuits in a chip, according to an embodiment.

[00140] Figs. 39F and 39G show circuit diagrams of off-chip buffers in a chip, according to an embodiment.

[00141] Figs. 40A-40F show how to calculate an active area of an ESD unit of a chip and define a size of an ESD circuit composed of one or more the ESD units, according to an embodiment.

[00142] Fig. 41 shows a cross sectional view of a module including a substrate, a radio frequency (RF) module, and a wirebonded stacked memory BGA package, according to an embodiment.

[00143] Figs. 42A-42O are cross-sectional views showing a process for forming a chip, according to an embodiment.

[00144] Figs. 43A-43E are cross-sectional views showing a process for forming a semiconductor wafer finalized to be cut into a plurality of a cache memory chip, according to an embodiment.

[00145] Figs. 44A-44C are cross-sectional views showing a process for bonding the chip shown in Fig. 42N with the semiconductor wafer shown in Fig 43D, according to an embodiment.

[00146] Figs. 45A and 45B are circuit diagrams each showing interface circuits of a cache memory chip and a chip, according to an embodiment.

[00147] Figs. 46A-46N are cross-sectional views showing a process for forming a semiconductor wafer finalized to be cut into a plurality of a cache memory chip, according to an embodiment.

[00148] Figs. 47A-47C are cross-sectional views showing a process for forming a processor unit, according to an embodiment.

[00149] Figs. 47D-47F are cross-sectional views showing a process for forming a processor unit, according to an embodiment.

[00150] Figs. 47G-47I are cross-sectional views showing a process for forming a processor unit, according to an embodiment.

[00151] Figs. 47J-47L are cross-sectional views showing a process for forming a processor unit, according to an embodiment.

[00152] Fig. 48A shows another stacked DRAM BGA package 1390, according to an embodiment.

[00153] Fig. 48B shows a top view of a DRAM chip 1392 assembled in the stacked DRAM BGA package 1390 shown in Fig. 48A, according to an embodiment.

[00154] Figs. 48C and 48D show cross-sectional views of various types of a DRAM chip 1392 assembled in the stacked DRAM BGA package 1390 shown in Fig. 48A along a cut

line of F-F' of Fig. 48B, and the redistribution circuit layer 1411 is made mainly of sputtered aluminum, according to an embodiment.

[00155] Figs. 48E and 48F shows cross-sectional views of various types of a DRAM chip 1392 assembled in the stacked DRAM BGA package 1390 shown in Fig. 48A along a cut line of F-F' of Fig. 48B, and the redistribution circuit layer 1411 is made mainly of electroplated copper or gold, according to an embodiment.

[00156] Fig. 48G shows a top view of a DRAM chip 1392 assembled in the stacked DRAM BGA package 1390 shown in Fig. 48A, according to an embodiment.

[00157] Figs. 48H and 48I show cross-sectional views of various types of a DRAM chip 1392 placed, assembled, or incorporated in the stacked DRAM BGA package 1390 shown in Fig. 48A along a cut line of G-G' of Fig. 48Q and the redistribution circuit layer 1411 is made mainly of sputtered aluminum, according to an embodiment.

[00158] Figs. 48J and 48K shows cross-sectional views of various types of a DRAM chip 1392 assembled in the stacked DRAM BGA package 1390 shown in Fig. 48A along a cut line of G-G' of Fig. 48Q and the redistribution circuit layer 1411 is made mainly of electroplated copper or gold, according to an embodiment.

[00159] While certain embodiments are depicted in the drawings, one skilled in the art will appreciate that the embodiments depicted are illustrative and that variations of those shown, as well as other embodiments described herein, may be envisioned and practiced within the scope of the present disclosure.

DETAILED DESCRIPTION OF THE DISCLOSURE

[00160] Illustrative embodiments are now discussed. Other embodiments may be used in addition or instead. Details that may be apparent or unnecessary may be omitted to save space or for a more effective presentation. Conversely, some embodiments may be practiced without all of the details that are disclosed.

[00161] The present disclosure provides for integrated circuit chips and chip packages that utilize over-passivation and bottom interconnection schemes (or, "technologies") for the respective major sides of the chip or chip packages.

[00162] An aspect of the present disclosure is directed to chips or chip packages including one interconnection scheme at one side of a chip or chip package and/or another

interconnection scheme at another at another side of a chip or chip package, e.g., an over-passivation scheme at a top of a chip and a bottom scheme at a bottom of the same chip.

[00163] Another aspect of the present disclosure is directed to on-chip voltage-regulating and/or converting devices and circuits. Such on-chip voltage regulators and converters can provide a constant voltage source for semiconductor devices located at different locations on an IC chip through on-chip power/ground buses. The voltage can be provided with minimized/reduced parasitic loss, minimized/reduced energy consumption, and/or minimized/reduced ripple effect.

[00164] Figs. 1A, 2A, and 3A show a circuit diagram, a top view and a cross-sectional view, respectively, of a prior art chip structure useful for discussing embodiments of the present disclosure. The voltage regulator or converter circuit 41 receives an external power voltage Vdd, outputs a power voltage Vcc, and delivers the power Vcc to the internal circuits 20, including 21, 22, 23 and 24, using IC fine-line metal traces 6191 and 61 under a passivation layer 5. The IC fine-line metal traces 61 include segments of 618, 6111, 6121a, 6121b, 6121c and 6141. The fine-line metal traces 6191 and 61 are under the passivation layer 5.

[00165] Exemplary embodiments of the present disclosure are described below.

First Embodiment: Over-passivation power/ground buses with a voltage regulator-converter

[00166] Figs. 1B, 1C, 2B, 2C, 3B, 3C, and 3D illustrate a first exemplary embodiment of the present disclosure. Figs. 1B and 1C show a simplified circuit diagram where metal traces 81 and/or 82 over a passivation layer 5 connect a voltage regulator or converter circuit 41 and internal circuits 21, 22, 23 and 24 to distribute a power voltage or a ground reference voltage, and a dotted line 5 indicates a passivation layer, coarse traces indicate traces of an over-passivation scheme 102 formed over the passivation layer 5, and fine traces indicate traces formed under the passivation layer 5. Figs. 2B and 2C show top views of semiconductor chips realizing the circuitry shown in Figs. 1B and 1C, respectively, and coarse traces mean the traces of the over-passivation scheme 102 formed over the passivation layer 5, and fine traces mean the traces formed under the passivation layer 5. Figs. 3B and 3C show cross-sectional views of semiconductor chips realizing the circuitry shown in Figs. 1B and 1C, respectively. Figs. 2B and 2C show top views of the semiconductor chips shown in Figs. 3B and 3C, respectively. The over-passivation scheme 102 shown in Fig. 3B includes a polymer layer 99

and two metal traces 81 and 81P provided by a patterned circuit layer 811, and an opening 9919 in the polymer layer 99 is over a contact point 8110 of the metal trace 81P and exposes it. The over-passivation scheme 102 shown in Fig. 3C includes a metal traces 81 provided by a patterned circuit layer 812, a metal trace 82 provided by a patterned circuit layer 821, and two polymer layers 98 and 99, and an opening 9929 in the polymer layer 99 is over a contact point 8120 of the patterned circuit layer 812 and exposes it. The over-passivation scheme 102 shown in Fig. 3D includes two polymer layers 95 and 99 and two metal traces 81 and 81P provided by the patterned circuit layer 811, and multiple openings 9519, 9519', 9511, 9512 and 9514 are in the polymer layer 95, and an opening 9919 in the polymer layer 99 is over a contact point 8110 of the metal trace 81P and exposes it.

[00167] For embodiments of the present disclosure, an on-chip voltage regulator or converter circuit 41 is configured to send electrical power to several internal devices 21, 22, 23 and 24 (or circuits), and the voltage regulator or converter circuit 41 and the internal devices 21, 22, 23 and 24 are formed in and/or on a silicon substrate 1 within a same IC chip. Through openings 511, 512 and 514 in a passivation layer 5, and by way of a coarse metal conductor 81 deposited over the passivation layer, electrical power output from the voltage regulator or converter circuit 41 is delivered to several devices or circuit units 21, 22, 23 and 24 with little loss or parasitic effects. The advantage of this design is that, affiliated with the regulated power source and with the coarse metal conductor, the voltage to the next level at the load of internal circuits can be controlled at a voltage level with high precision. When the reference number of 41 is a voltage regulator, the output voltage Vcc of the voltage regulator 41 is within +10% and −10% of the desired voltage level, and exemplary within +5% and −5% of the desired voltage level, insensitive to voltage surge or large fluctuation at the input node connected with an external power supply Vdd input from the power metal trace 81P. Alternatively, the voltage regulator 41 may have an output node at a voltage level of Vcc output from the voltage regulator 41 and an input node at a voltage level of Vdd supplied from an external circuit, and a ratio of a difference of the voltage level of Vdd minus the voltage level of Vcc to the voltage level of Vdd is less than 10%. Hence, circuit performance can be improved. The voltage regulator 41 may have an output of between 1 volt and 10 volts, and exemplary between 1 volt and 5 volts.

[00168] In some applications, if the chip requires a voltage level Vcc different from the voltage level Vdd of the external power supply, a voltage converter may be installed in the chip. The reference number of 41 may indicate the voltage converter. The on-chip voltage converter

41, in addition to the voltage regulating circuit, is desirable in this case to convert the voltage level Vdd of the external power supply to the voltage level Vcc required in the chip. The converter may output a voltage level Vcc higher than the voltage Vdd at the input node. Alternatively, the converter may output a voltage level Vcc lower than the voltage Vdd at the input node. The voltage converter may have an output of between 1 volt and 10 volts, and exemplary between 1 volt and 5 volts. When the voltage level of Vcc ranges from 0.6 volts to 3 volts, the voltage level of Vdd ranges from 3 volts to 5 volts. When the voltage level of Vcc ranges from 0.6 volts to 2 volts, the voltage level of Vdd ranges from 2 volts to 3 volts. For example, when the voltage level of Vcc is 2.5 volts, the voltage level of Vdd is 3.3 volts. When the voltage level of Vcc is 1.8 volts, the voltage level of Vdd is 3.3 volts. When the voltage level of Vcc is 1.8 volts, the voltage level of Vdd is 2.5 volts. When the voltage level of Vcc is 3.3 volts, the voltage level of Vdd is 5 volts.

[00169] Fig. 1B shows circuit schematics of exemplary embodiments of the present disclosure. As shown, the voltage regulator or converter circuit 41 receives a voltage Vdd from an external power supply, and outputs a voltage Vcc for the internal circuits 20, including 21, 22 23, and 24. The output voltage Vcc at node P is distributed to the power nodes Tp, Up, Vp and Wp of the internal circuits 21, 22, 23 and 24, respectively, first up through a passivation opening 519' in the passivation layer 5, then through a thick metal trace 81 over the passivation layer 5, then down through the passivation openings 511, 512, and 514 in the passivation layer 5, and then through the fine-line metal traces 61' to the internal circuits 20: particularly through the segment 611 of the fine-line metal traces 61' to the internal circuit 611; particularly through the segments 612a and 612b of the fine-line metal traces 61' to the internal circuit 22; particularly through the segments 612a and 612c of the fine-line metal traces 61' to the internal circuit 23; and through the segment 614 of the fine-line metal traces 61' to the internal circuit 24.

[00170] Each of the internal circuits 20, including 21, 22, 23 and 24, includes at least a PMOS transistor having a source connected to the fine-line metal traces 61', for example. Each of the internal circuits 20, including 21, 22, 23 and 24, may include a NMOS transistor having a ratio of a physical channel width thereof to a physical channel length ranging from, e.g., about 0.1 and 20, ranging from, e.g., about 0.1 and 10 or preferably ranging from, e.g., about 0.2 and 2. Alternatively, each of the internal circuits 20, including 21, 22, 23 and 24, may include a PMOS transistor having a ratio of a physical channel width thereof to a physical

channel length ranging from, e.g., about 0.2 and 40, ranging from, e.g., about 0.2 and 40 or preferably ranging from, e.g., about 0.4 and 4.

[00171] The chip structure in Fig. 1B can utilize a coarse metal conductor 81 as a carrier of the power/ground lines, traces, or planes. In this case, the voltage drop and noise is much reduced since the coarse metal conductor 81 has lower resistance and capacitance than the fine-line metal traces.

[00172] The internal circuits, or internal circuit units 20, shown in all of the embodiments, include two NOR gates 22 and 24, one NAND gate 23, and one internal circuit 21, for example. The internal circuits 20, 21, 22, 23, and 24 can be any type of IC circuits, such as NOR gate, NAND gate, AND gate, OR gate, operational amplifier, adder, multiplexer, diplexer, multiplier, A/D converter, D/A converter, CMOS transistor, bipolar CMOS transistor or bipolar circuit. The NOR gate 22 or 24 or NAND gate 23 has three input nodes Ui, Wi or Vi, one output node Uo, Wo or Vo, one Vcc node Up, Wp or Vp, and one Vss node Us, Ws or Vs. The internal circuit 21 has one input node Xi, one output node Xo, one Vcc node Tp and one Vss node Ts. Each of the internal circuits or internal circuit units 20, including 21, 22, 23, and 24, usually has signal nodes, power nodes, and ground nodes.

[00173] Figs. 2B and 3B provide the top view and cross-sectional view, respectively, of the circuit diagram shown in Fig. 1B. It is noted that, in Fig. 3B, the fine-line metal structures 611, 612, 614, 619 and 619' can be composed of stacked fine-line metal pads 60 and via plugs 60' filled in the vias 30'. The upper vias 30' are substantially aligned with the lower ones; the upper fine-line metal pads 60 are substantially aligned with the lower ones; the upper via plugs 60 are substantially aligned with the lower ones. Referring to Figs. 1B, 2B and 3B, the fine-line metal traces or plane 612 includes multiple portions 612a, 612b and 612c, and is used for the local power distribution.

[00174] The thick metal traces or plane 81 over the passivation layer 5 is used for global power distribution and connects the fine-line metal traces or plane 619', 611, 612 and 614. The thick metal trace or plane 81 over the passivation layer 5, shown in Figs. 1B and 2B, may be composed of only one patterned circuit layer 811, as shown in Fig. 3B, or multiple patterned circuit layers, not shown. The patterned circuit layer 811, such as a power plane, bus, trace or line, to distribute a power voltage Vcc is realized from the concept of the coarse trace 81 shown in Figs. 1B and 2B. When the thick metal traces or plane 81 over the passivation layer 5, shown in Fig. 2, is composed of multiple patterned circuit layers, a polymer layer, such as

polyimide (PI), benzocyclobutene (BCB), parylene, epoxy-based material, photoepoxy SU-8, elastomer or silicone, may be between the neighboring patterned circuit layers, separating the patterned circuit layers. A polymer layer 99, such as polyimide (PI), benzocyclobutene (BCB), parylene, epoxy-based material, photoepoxy SU-8, elastomer or silicone, may be on the topmost one of the patterned circuit layers, separated by the above mentioned polymer layers, over the passivation layer, not shown, or on the only one patterned circuit layer 811, as shown in Figs. 3B and 3D. Alternatively, A polymer layer 95, such as polyimide (PI), benzocyclobutene (BCB), parylene, epoxy-based material, photoepoxy SU-8, elastomer or silicone, may be between the passivation layer and the bottommost one of the patterned circuit layers, separated by the above mentioned polymer layers, not shown, or between the passivation layer 5 and the only one patterned circuit layer 811, as shown in Fig. 3D. The polymer layer 95 may have a thickness larger than 2 micrometers, such as between 2 and 30 micrometers. Multiple openings 9519, 9519', 9511, 9512 and 9514 in the polymer layer 95 are substantially aligned with the openings 519, 519', 511, 512 and 514 in the passivation layer 5, respectively. The openings 9519, 9519', 9511, 9512 and 9514 in the polymer layer 95 expose the pads (including 6190 and 6190') exposed by the openings 519, 519', 511, 512 and 514 in the passivation layer 5, respectively.

[00175] Some openings 9519 and 9519' in the polymer layer 95 have lower portions having widths or transverse dimensions smaller than those of the openings 519 and 519' in the passivation layer 5 aligned with the openings 9519 and 9519', respectively. The polymer layer 95 covers a portion of the pads 6190 and 6190' exposed by the openings 519 and 519' in the passivation layer 5. The shape of the openings 519 and 519' from a top perspective view may be round, square, rectangular or polygon. If the openings 519 and 519' are round, the openings 519 and 519' may have a diameter of between 0.1 and 200 microns, between 1 and 100 microns, or, preferably, between 0.5 and 30 microns. If the openings 519 and 519' are square, the openings 519 and 519' may have a width of between 0.1 and 200 microns, between 1 and 100 microns, or, preferably, between 0.1 and 30 microns. If the openings 519 and 519' are rectangular, the openings 519 and 519' may have a width of between 0.1 and 200 microns, between 1 and 100 microns, or, preferably, between 0.1 and 30 microns, and a length of between 1 micron and 1 centimeter. If the openings 519 and 519' are polygon having more than five sides, the openings 519 and 519' have a largest diagonal length of between 0.1 and 200 microns, between 0.5 and 100 microns, or, preferably, between 0.1 and 30 microns. Alternatively, the openings 519 and 519' have a largest transverse dimension of between 0.1

and 200 microns, between 1 and 100 microns, or, preferably, between 0.1 and 30 microns. In a case, the openings 519 and 519' have a width of between 30 and 100 microns, with the lower portion of the openings 9519 and 9519' in the polymer layer 95 having a width of between 20 and 100 microns.

[00176] Some openings 9511, 9512 and 9514 in the polymer layer 95 have lower portions having widths or transverse dimensions larger than those of the openings 511, 512 and 514 in the passivation layer 5 aligned with the openings 9511, 9512 and 9514, respectively. The openings 9511, 9512 and 9514 in the polymer layer 95 further expose the passivation layer 5 close to the openings 511, 512 and 514. The shape of the openings 511, 512 and 514 from a top perspective view may be round, square, rectangular or polygon. If the openings 511, 512 and 514 are round, the openings 511, 512 and 514 may have a diameter of between 0.1 and 200 microns, between 1 and 100 microns, or, preferably, between 0.5 and 30 microns. If the openings 511, 512 and 514 are square, the openings 511, 512 and 514 may have a width of between 0.1 and 200 microns, between 1 and 100 microns, or, preferably, between 0.1 and 30 microns. If the openings 511, 512 and 514 are rectangular, the openings 511, 512 and 514 may have a width of between 0.1 and 200 microns, between 1 and 100 microns, or, preferably, between 0.1 and 30 microns, and a length of between 1 micron and 1 centimeter. If the openings 511, 512 and 514 are polygon having more than five sides, the openings 511, 512 and 514 have a largest diagonal length of between 0.1 and 200 microns, between 1 and 100 microns, or, preferably, between 0.1 and 30 microns. Alternatively, the openings 511, 512 and 514 have a largest transverse dimension of between 0.1 and 200 microns, between 1 and 100 microns, or, preferably, between 0.1 and 30 microns. In a case, the openings 511, 512 and 514 have a width of between 5 and 30 microns, with the lower portion of the openings 9511, 9512 and 9514 in the polymer layer 95 having a width of between 20 and 100 microns.

[00177] The previous description concerning the openings 519, 519', 511, 512 and 514 in the passivation layer 5 and the openings 9519, 9519', 9511, 9512 and 9514 in the polymer layer 95 can be applied to the embodiments shown in 15A-15L, 16A-16M, 17A-17J, 18A-18I and 19A-19I.

[00178] One of the patterned circuit layers, such as 811 shown in Figs. 3B and 3D, composing the thick metal trace or plane 81 over the passivation layer 5 may include an adhesion/barrier/seed layer 8111, and a bulk conduction metal layer 8112. The methods to form the patterned circuit layer 811 and the specification thereof may follow the methods to form the

patterned circuit layer 801, 802 or 803 and the specification thereof shown in Figs. 15A-15M, 16A-16M, 17A-17J, 18A-18I and 19A-19I.

[00179] In Figs. 1B, 2B and 3B, an external power supplies a voltage level Vdd at a metal pad 8110 connected to a metal pad 6190 of a topmost one of fine-line circuit metal layers 619 under the passivation layer 5 through an opening 519 in the passivation layer 5, and inputs to the voltage regulator or converter circuit 41. The voltage regulator or converter circuit 41 outputs a power voltage to supply the internal circuits 21, 22, 23 and 24 through the fine-line circuit metal layers 619', thick patterned trace or plane 811 and fine-line circuit metal layers 611, 612 and 614. The fine-line circuit layers 619, 619', 611, 612 and 614 are separated by thin-film insulating layers 30, such as silicon oxide.

[00180] Though Fig. 3B shows only one patterned circuit layer 81 for distributing a regulated or converted power voltage of Vcc, multiple patterned circuit layers with one or more polymer layers deposited there between can be formed over the passivation layer 5 and used to distribute a regulated or converted power voltage of Vcc. Metal traces or planes in different patterned circuit layers are connected through the openings in the polymer layer there between.

[00181] Figs. 1A, 2A and 3A reveal the external power supply at a voltage level Vdd inputs the voltage regulator or converter circuit 41 through the pad 6190 exposed by the opening 519 in the passivation layer 5 and through the fine-line circuit layers 619 (including stacked fine-line metal pads and vias). The output power at voltage level Vcc outputs from the voltage regulator or converter circuit 41 is distributed to supply the voltage of Vcc to the internal circuits 21, 22, 23 and 24 only through IC fine line interconnection 61 including segments 6191', 618, 6111, 6121 and 6141.

[00182] In Figs. 1B, 2B, 3B and 3D, the ground voltage is denoted as Vss without detailing the circuit schematics, layout and structure for distributing the ground voltage. Figs. 1C, 2C and 3C describe the circuit schematics, top view and cross-sectional view, respectively, showing the thick metal traces or planes 81 and 82 over the passivation layer 5 for distributing both of the power supply voltage of Vcc and the ground reference voltage of Vss. The structure 82 of distributing the ground reference voltage of Vss is similar to the above mentioned structure 81 of distributing the power supply voltage of Vcc, except that a common ground voltage Vss is provided for the voltage regulator or converter circuit 41 and the internal circuits 21, 22, 23 and 24 through the thick metal trace or plane 82. That means the external ground node Es may be connected to the ground node Rs of the voltage regulator or converter circuit

41 and to the internal ground node Ts, Us, Vs, Ws of the internal circuits 21, 22, 23 and 24. In Figs. 1C, 2C and 3C, the point Es connected to a ground source of an external circuitry at a voltage level Vss is connected to (1) the ground node Rs of the voltage regulator or converter circuit 41 through an opening 529 in the passivation layer 5, and (2) the ground nodes Ts, Us, Vs and Ws of the internal circuits 21, 22, 23 and 24 through the thick metal lines, buses or traces 82 over the passivation layer 5, the openings, 521, 522 and 524 in the passivation layer 5, and fine-line metal structures 621, 622 (including 622a, 622b and 622c) and 624.

[00183] Fig. 3C shows two patterned circuit layers 812 and 821 over the passivation layer 5, used for distributing a power voltage Vcc and a ground reference voltage Vss, respectively. The bottom one 821 of the patterned circuit layers 812 and 821, such as a ground plane, bus, trace or line, to distribute a ground reference voltage Vss is realized from the concept of the coarse trace 82 shown in Figs. 1C and 2C. The top one 812 of the patterned circuit layers 812 and 821, such as a power plane, bus, trace or line, to distribute a power voltage Vcc is realized from the concept of the coarse trace 81 shown in Figs. 1C and 2C. A polymer layer 98, such as polyimide, benzocyclobutene (BCB), parylene, epoxy-based material, photoepoxy SU-8, elastomer or silicone, having a thickness of between 2 and 30 microns, separates the patterned circuit layers 821 and 812. Another polymer layer 99, such as polyimide, benzocyclobutene (BCB), parylene, epoxy-based material, photoepoxy SU-8, elastomer or silicone, having a thickness of between 2 and 30 microns, covers the top patterned circuit layer 812. Alternatively, another polymer layer, such as benzocyclobutene (BCB), polyimide, parylene, epoxy-based material, photoepoxy SU-8, elastomer or silicone, having a thickness of between 2 and 30 microns, may be provided between the bottom-most patterned circuit layer 821 and the passivation layer 5, described as the polymer layer 95 shown in Fig. 3D. In Figs. 1C, 2C and 3C, the ground plane, trace or line 82 over the passivation layer 5, used to distribute a ground reference voltage of Vss, is connected to the ground nodes Ts, Us, Vs and Ws of the internal circuits 21, 22, 23 and 24 and the ground node Rs of the voltage regulator or converter circuit 41 through the openings 521, 522, 524 and 529 in the passivation layer 5 and the fine-line metal structures 621, 622, 624 and 629, respectively. The power plane, trace or line 81 or 812 used to distribute a power voltage of Vcc is connected to the power nodes Tp, Up, Vp and Wp (not shown) of the internal circuits 21, 22, 23 and 24 and to the output nodes P of the voltage regulator or converter circuit 41 through the openings (not shown) in the polymer layer 98 and in the passivation layer 5 and through the fine-line metal structures 611, 612, 614 and 619', respectively, as illustrated in Fig. 3B.

[00184] In Fig. 3B, there is only one patterned circuit layer 811, including a portion serving as the previously described thick and wide metal trace 81P, power bus or plane delivering a power voltage input from an external circuit, over the passivation layer 5, and another portion serving as the previously described thick and wide metal trace 81, power bus or plane delivering a power voltage output from the voltage regulator or converter circuit 41, over the passivation layer 5. The patterned circuit layer 811 may contain an adhesion/barrier layer, a seed layer on the adhesion/barrier layer, and an electroplated metal layer 8112 on the seed layer, the adhesion/barrier layer and the seed layer composing the bottom layer 8111.

[00185] Referring to Fig. 3B, regards to the process for forming the patterned circuit layer 811, the adhesion/barrier layer may be formed by a suitable process or processes, e.g., by sputtering a titanium-containing layer, such as titanium layer or a titanium-tungsten-alloy layer, having a thickness between 1000 and 6000 angstroms, sputtering a chromium-containing layer, such as chromium layer, having a thickness between 1000 and 6000 angstroms, or sputtering a tantalum-containing layer, such as tantalum layer or tantalum-nitride layer, having a thickness between 1000 and 6000 angstroms, on a silicon-nitride layer of the passivation layer 5 and on contact pads 6490, principally made of aluminum or copper, exposed by multiple openings 549, 511, 512 and 514 in the passivation layer 5. Thereafter, the seed layer may be formed by a suitable process or processes, e.g., by sputtering a copper layer having a thickness between 200 and 3000 angstroms on the adhesion/barrier layer of any previously described material or by sputtering a gold layer having a thickness between 200 and 3000 angstroms on the adhesion/barrier layer of any previously described material. Thereafter, a photoresist layer may be formed on the seed layer, multiple openings in the photoresist layer exposing the seed layer. Thereafter, the metal layer 8112 may be formed by a suitable process or processes, e.g., by electroplating a copper layer having a thickness between 2 and 30 micrometers on the copper layer serving as the seed layer, exposed by the openings in the photoresist layer, by electroplating a copper layer having a thickness between 2 and 30 micrometers on the copper layer serving as the seed layer, exposed by the openings in the photoresist layer and then electroplating a nickel layer having a thickness between 0.5 and 10 micrometers on the electroplated copper layer in the openings in the photoresist layer, by electroplating a copper layer having a thickness between 2 and 30 micrometers on the copper layer serving as the seed layer, exposed by the openings in the photoresist layer, electroplating a nickel layer having a thickness between 0.5 and 10 micrometers on the electroplated copper layer in the openings in the photoresist layer and then electroplating a gold layer, platinum layer, palladium layer or

ruthenium layer having a thickness between 0.05 and 2 micrometers on the electroplated nickel layer in the openings in the photoresist layer, or by electroplating a gold layer having a thickness between 2 and 30 micrometers on the gold layer serving as the seed layer, exposed by the openings in the photoresist layer. Thereafter, the photoresist layer may be removed. Thereafter, the seed layer not under the metal layer 8112 is removed using a wet-etching process or using a dry-etching process. Thereafter, the adhesion/barrier layer not under the metal layer 8112 is removed using a wet-etching process or using a dry-etching process.

[00186] After the patterned circuit layer 811 is formed, a polymer layer 99 can be formed by a suitable process or processes, e.g., by spin-on coating a negative photosensitive polyimide layer, such as ester type, on the patterned circuit layer 811 and on the nitride layer of the passivation layer 5, exposing the spin-on coated photosensitive polyimide layer, developing the exposed polyimide layer and then curing the developed polyimide layer at the temperature between 265 and 285°C for a time between 30 and 240 minutes in a nitrogen or oxygen-free ambient. Accordingly, an opening 9949 may be formed in the polymer layer 99, exposing a contact pad 8110 of the patterned circuit layer 811.

[00187] Referring to Fig. 3B, for forming a metal bump over the contact pad 8110, an adhesion/barrier layer may be formed by a suitable process or processes, e.g., by sputtering a titanium-containing layer, such as titanium layer or a titanium-tungsten-alloy layer, having a thickness between 1000 and 6000 angstroms, sputtering a chromium-containing layer, such as chromium layer, having a thickness between 1000 and 6000 angstroms, or sputtering a tantalum-containing layer, such as tantalum layer or tantalum-nitride layer, having a thickness between 1000 and 6000 angstroms, on the polymer layer 99 and on the contact pad 8110 exposed by the opening 9919. Thereafter, the seed layer may be formed by a suitable process or processes, e.g., by sputtering a copper layer having a thickness between 200 and 3000 angstroms on the adhesion/barrier layer of any previously described material. Thereafter, a photoresist layer may be formed on the seed layer, multiple openings in the photoresist layer exposing the seed layer. Thereafter, the metal bump may be formed by a suitable process or processes, e.g., by electroplating a copper layer having a thickness between 0.5 and 10 micrometers on the copper layer serving as the seed layer, exposed by the openings in the photoresist layer, electroplating a nickel layer having a thickness between 0.5 and 10 micrometers on the electroplated copper layer in the openings in the photoresist layer, and then electroplating a tin-containing layer, such as a tin-lead alloy, a tin-silver alloy or a tin-silver-copper alloy, having a thickness between 60 and 200 micrometers on the

electroplated nickel layer in the openings in the photoresist layer. Thereafter, the photoresist layer may be removed. Thereafter, the seed layer not under the metal bump is removed using a wet-etching process or using a dry-etching process. Thereafter, the adhesion/barrier layer not under the metal bump is removed using a wet-etching process or using a dry-etching process. Thereafter, the metal bump can be reflowed to be shaped like a ball for a flip-chip assembly. The metal bump can be connected to a printed circuit board, ceramic substrate or another semiconductor chip.

[00188] Referring to Fig. 3B, for forming another kind of metal bump over the contact pad 8110, an adhesion/barrier layer may be formed by a suitable process or processes, e.g., by sputtering a titanium-containing layer, such as titanium layer or a titanium-tungsten-alloy layer, having a thickness between 1000 and 6000 angstroms, or sputtering a tantalum-containing layer, such as tantalum layer or tantalum-nitride layer, having a thickness between 1000 and 6000 angstroms, on the polymer layer 99 and on the contact pad 8110 exposed by the opening 9919. Thereafter, the seed layer may be formed by a suitable process or processes, e.g., by sputtering a gold layer having a thickness between 200 and 3000 angstroms on the adhesion/barrier layer of any previously described material. Thereafter, a photoresist layer may be formed on the seed layer, multiple openings in the photoresist layer exposing the seed layer. Thereafter, the metal bump may be formed by a suitable process or processes, e.g., by electroplating a gold layer having a thickness between 6 and 25 micrometers on the gold layer serving as the seed layer, exposed by the openings in the photoresist layer. Thereafter, the photoresist layer may be removed. Thereafter, the seed layer not under the metal bump is removed using a wet-etching process or using a dry-etching process. Thereafter, the adhesion/barrier layer not under the metal bump is removed using a wet-etching process or using a dry-etching process. The metal bump can be connected to a flexible substrate by a tape-automated bonding (TAB) process, or a glass substrate via anisotropic conductive film or paste (ACF or ACP).

[00189] Alternatively, referring to Fig. 3B, a nickel layer having a thickness between 0.05 and 2 micrometers can be electroless plated on the contact pad 8110 exposed by the opening 9919, and a gold layer, platinum layer, palladium layer or ruthenium layer having a thickness between 0.05 and 2 micrometers can be electroless plated on the electroless plated nickel layer in the opening 9919 in the polymer layer 99. Thereafter, a gold wire can be bonded onto the electroless plated gold layer in the opening 9919 in the polymer layer 99 using a wirebonding process.

[00190] Alternatively, referring to Fig. 3B, a gold wire can be bonded onto a gold layer, platinum layer, palladium layer or ruthenium layer of the patterned circuit layer 811, exposed by the openings 9919 in the polymer layer 99 using a wirebonding process.

[00191] Referring to Fig. 3D, before the patterned circuit layer 811 is formed, a polymer layer 95 can be optionally formed by a suitable process or processes, e.g., by spin-on coating a negative photosensitive polyimide layer, such as ester type, on the nitride layer of the passivation layer 5 and on the contact pads 6490, exposing the spin-on coated photosensitive polyimide layer, developing the exposed polyimide layer and then curing the developed polyimide layer at the temperature between 265 and 285°C for a time between 30 and 240 minutes in a nitrogen or oxygen-free ambient. Accordingly, multiple openings 9519, 9519', 9511, 9512 and 9514 may be formed in the polymer layer 95, exposing multiple contact pads 6190 exposed by the openings 519, 519', 511, 512 and 514 in the passivation layer 5. After the polymer layer 95 is formed, the patterned circuit layer 811 can be formed on the polymer layer 95 and on the contact pads 6190 exposed by the openings 519, 519', 511, 512 and 514. The adhesion/barrier layer of any previously described material may be sputtered on the polymer layer 95 and on the contact pads 6190 exposed by the openings 9519, 9511, 9512 and 9514 in the polymer layer 95.

[00192] One of the patterned circuit layers 812 and 821 shown in Fig. 3C, composing the thick metal traces or planes 81 and 82 over the passivation layer 5 may include an adhesion/barrier/seed layer 8111, and a bulk conduction metal layer 8112. The methods to form the patterned circuit layers 812 and 821 and the specification thereof may be based on the methods to form the patterned circuit layer 801, 802 or 803 and the specification thereof shown in Figs. 15A-15L, 16A-16M, 17A-17J, 18A-18I and 19A-19I.

[00193] In Fig. 3C, the thick and wide metal trace, bus or plane 82, used to deliver a ground voltage, may have a lower patterned circuit layer under an upper patterned circuit layer of the thick and wide metal trace, bus or plane 81, used to deliver a power voltage Vcc output from the voltage regulator or converter circuit 41. Alternatively, the thick and wide metal trace, bus or plane 82, used to deliver a ground voltage, may have an upper patterned circuit layer over a lower patterned circuit layer of the thick and wide metal trace, bus or plane 81, used to deliver a power voltage Vcc output from the voltage regulator or converter circuit 41. A polymer layer having a thickness between 2 and 30 micrometers may be between the upper and

lower patterned circuit layers. Each of the lower and upper patterned circuit layers may have an electroplated copper layer having a thickness between 2 and 30 micrometers.

[00194] Referring to Fig. 3C, there may be multiple patterned circuit layers 821 and 812, including the previously described ground bus or plane 82 and the previously described power bus or plane 81, used to deliver a power voltage output from the voltage regulator or converter circuit 41, over the ground bus or plane 82, over the passivation layer 5. The process for forming the patterned circuit layer 821 on the passivation layer 5 and on the contact pads 6290 exposed by the openings 529, 521, 522 and 524 can be referred to as the process for forming the patterned circuit layer 811 shown in Fig. 3B on the passivation layer 5 and on the contact pads 6190 exposed by the openings 519, 511, 512 and 514. The patterned circuit layer 821 may contain an adhesion/barrier layer, a seed layer on the adhesion/barrier layer, and an electroplated metal layer 8212 on the seed layer, the adhesion/barrier layer and the seed layer composing the bottom layer 8211. The patterned circuit layer 812 may contain an adhesion/barrier layer, a seed layer on the adhesion/barrier layer, and an electroplated metal layer 8122 on the seed layer, the adhesion/barrier layer and the seed layer composing the bottom layer 8121.

[00195] Referring to Fig. 3C, after the patterned circuit layer 821 is formed, a polymer layer 98 can be formed by a suitable process or processes, e.g., by spin-on coating a negative photosensitive polyimide layer, such as ester type, on the patterned circuit layer 821 and on the nitride layer of the passivation layer 5, exposing the spin-on coated photosensitive polyimide layer, developing the exposed polyimide layer and then curing the developed polyimide layer at the temperature between 265 and 285°C for a time between 30 and 240 minutes in a nitrogen or oxygen-free ambient. Accordingly, an opening 9829 may be formed in the polymer layer 98, exposing a contact pad of the patterned circuit layer 821.

[00196] Referring to Fig. 3C, regards to the process for forming the patterned circuit layer 812, the adhesion/barrier layer may be formed by a suitable process or processes, e.g., by sputtering a titanium-containing layer, such as titanium layer or a titanium-tungsten-alloy layer, having a thickness between 1000 and 6000 angstroms, sputtering a chromium-containing layer, such as chromium layer, having a thickness between 1000 and 6000 angstroms, or sputtering a tantalum-containing layer, such as tantalum layer or tantalum-nitride layer, having a thickness between 1000 and 6000 angstroms, on the polymer layer 98 and on the contact pad of the patterned circuit layer 821 exposed by the opening 9829 in the polymer layer 98. Thereafter,

the seed layer may be formed by a suitable process or processes, e.g., by sputtering a copper layer having a thickness between 200 and 3000 angstroms on the adhesion/barrier layer of any previously described material or by sputtering a gold layer having a thickness between 200 and 3000 angstroms on the adhesion/barrier layer of any previously described material. Thereafter, a photoresist layer may be formed on the seed layer, multiple openings in the photoresist layer exposing the seed layer. Thereafter, the metal layer 8122 may be formed by a suitable process or processes, e.g., by electroplating a copper layer having a thickness between 2 and 30 micrometers on the copper layer serving as the seed layer, exposed by the openings in the photoresist layer, by electroplating a copper layer having a thickness between 2 and 30 micrometers on the copper layer serving as the seed layer, exposed by the openings in the photoresist layer and then electroplating a nickel layer having a thickness between 0.5 and 10 micrometers on the electroplated copper layer in the openings in the photoresist layer, by electroplating a copper layer having a thickness between 2 and 30 micrometers on the copper layer serving as the seed layer, exposed by the openings in the photoresist layer, electroplating a nickel layer having a thickness between 0.5 and 10 micrometers on the electroplated copper layer in the openings in the photoresist layer and then electroplating a gold layer, platinum layer, palladium layer or ruthenium layer having a thickness between 0.05 and 2 micrometers on the electroplated nickel layer in the openings in the photoresist layer, or by electroplating a gold layer having a thickness between 2 and 30 micrometers on the gold layer serving as the seed layer, exposed by the openings in the photoresist layer. Thereafter, the photoresist layer may be removed. Thereafter, the seed layer not under the metal layer 8122 is removed using a wet-etching process or using a dry-etching process. Thereafter, the adhesion/barrier layer not under the metal layer 8122 is removed using a wet-etching process or using a dry-etching process.

[00197] After the patterned circuit layer 812 is formed, a polymer layer 99 can be formed by a suitable process or processes, e.g., by spin-on coating a negative photosensitive polyimide layer, such as ester type, on the patterned circuit layer 812 and on the polymer layer 98, exposing the spin-on coated photosensitive polyimide layer, developing the exposed polyimide layer and then curing the developed polyimide layer at the temperature between 265 and 285°C for a time between 30 and 240 minutes in a nitrogen or oxygen-free ambient. Accordingly, an opening 9929 may be formed in the polymer layer 99, exposing a contact pad 8120 of the patterned circuit layer 812.

[00198] Referring to Fig. 3C, for forming a metal bump over the contact pad 8120, an adhesion/barrier layer may be formed by a suitable process or processes, e.g., by sputtering a titanium-containing layer, such as titanium layer or a titanium-tungsten-alloy layer, having a thickness between 1000 and 6000 angstroms, sputtering a chromium-containing layer, such as chromium layer, having a thickness between 1000 and 6000 angstroms, or sputtering a tantalum-containing layer, such as tantalum layer or tantalum-nitride layer, having a thickness between 1000 and 6000 angstroms, on the polymer layer 99 and on the contact pad 8120 exposed by the opening 9929. Thereafter, the seed layer may be formed by a suitable process or processes, e.g., by sputtering a copper layer having a thickness between 200 and 3000 angstroms on the adhesion/barrier layer of any previously described material. Thereafter, a photoresist layer may be formed on the seed layer, multiple openings in the photoresist layer exposing the seed layer. Thereafter, the metal bump may be formed by a suitable process or processes, e.g., by electroplating a copper layer having a thickness between 0.5 and 10 micrometers on the copper layer serving as the seed layer, exposed by the openings in the photoresist layer, electroplating a nickel layer having a thickness between 0.5 and 10 micrometers on the electroplated copper layer in the openings in the photoresist layer, and then electroplating a tin-containing layer, such as a tin-lead alloy, a tin-silver alloy or a tin-silver-copper alloy, having a thickness between 60 and 200 micrometers on the electroplated nickel layer in the openings in the photoresist layer. Thereafter, the photoresist layer may be removed. Thereafter, the seed layer not under the metal bump is removed using a wet-etching process or using a dry-etching process. Thereafter, the adhesion/barrier layer not under the metal bump is removed using a wet-etching process or using a dry-etching process. Thereafter, the metal bump can be reflowed to be shaped like a ball. The metal bump can be connected to a printed circuit board, ceramic substrate or another semiconductor chip.

[00199] Referring to Fig. 3C, for forming another kind of metal bump over the contact pad 8120, an adhesion/barrier layer may be formed by a suitable process or processes, e.g., by sputtering a titanium-containing layer, such as titanium layer or a titanium-tungsten-alloy layer, having a thickness between 1000 and 6000 angstroms, or sputtering a tantalum-containing layer, such as tantalum layer or tantalum-nitride layer, having a thickness between 1000 and 6000 angstroms, on the polymer layer 99 and on the contact pad 8120 exposed by the opening 9929. Thereafter, the seed layer may be formed by a suitable process or processes, e.g., by sputtering a gold layer having a thickness between 200 and 3000 angstroms on the adhesion/barrier layer of any previously described material. Thereafter, a photoresist layer may

be formed on the seed layer, multiple openings in the photoresist layer exposing the seed layer. Thereafter, the metal bump may be formed by a suitable process or processes, e.g., by electroplating a gold layer having a thickness between 6 and 25 micrometers on the gold layer serving as the seed layer, exposed by the openings in the photoresist layer. Thereafter, the photoresist layer may be removed. Thereafter, the seed layer not under the metal bump is removed using a wet-etching process or using a dry-etching process. Thereafter, the adhesion/barrier layer not under the metal bump is removed using a wet-etching process or using a dry-etching process. The metal bump can be connected to a flexible substrate by a tape-automated bonding (TAB) process, or a glass substrate via anisotropic conductive film or paste (ACF or ACP).

[00200] Alternatively, referring to Fig. 3C, a nickel layer having a thickness between 0.05 and 2 micrometers can be electroless plated on the contact pad 8120 exposed by the opening 9929 in layer polymer layer 99, and a gold layer, platinum layer, palladium layer or ruthenium layer having a thickness between 0.05 and 2 micrometers can be electroless plated on the electroless plated nickel layer in the opening 9929 in the polymer layer 99. Thereafter, a gold wire can be bonded onto the electroless plated gold layer in the opening 9929 in the polymer layer 99 using a wirebonding process.

[00201] Alternatively, referring to Fig. 3C, a gold wire can be bonded onto a gold layer, platinum layer, palladium layer or ruthenium layer of the patterned circuit layer 812, exposed by the openings 9929 in the polymer layer 99 using a wirebonding process.

[00202] Alternatively, before the patterned circuit layer 821 is formed, a polymer layer can be optionally formed by a suitable process or processes, e.g., by spin-on coating a negative photosensitive polyimide layer, such as ester type, on the nitride layer of the passivation layer 5 and on the contact pads 6290, exposing the spin-on coated photosensitive polyimide layer, developing the exposed polyimide layer and then curing the developed polyimide layer at the temperature between 265 and 285°C for a time between 30 and 240 minutes in a nitrogen or oxygen-free ambient. Accordingly, multiple openings may be formed in the polymer layer, exposing multiple contact pads 6290 exposed by the openings 529, 521, 522 and 524 in the passivation layer 5. After the polymer layer is formed, the patterned circuit layer 821 can be formed on the polymer layer and on the contact pads 6290 exposed by the openings 529, 521, 522 and 524. The adhesion/barrier layer of any previously described material may be sputtered

on the polymer layer and on the contact pads 6290 exposed by the openings in the polymer layer.

[00203] In some applications, some metal lines, traces or planes used to transmit a digital signal or analog signal can be provided on the polymer layer 98 and at the same level as the power traces, buses or planes 812. Alternatively, some metal lines, traces or planes used to transmit a digital signal or analog signal can be provided on the passivation layer 5 and at the same level as the ground traces, buses or planes 82. There are more other structures formed over the passivation layer 5, described as below: (1) in the first application for high performance circuits or high precision analog circuits, another patterned circuit layer, such as signal planes, buses, traces or lines, used to transmit a digital signal or an analog signal (not shown) may be added between the power lines, buses or planes 812 and the ground lines, buses or planes 821. Polymer layers, such as polyimide, benzocyclobutene (BCB), parylene, epoxy-based material, photoepoxy SU-8, elastomer or silicone, (not shown) over and under the signal planes, buses, traces or lines are provided to separate the signal planes, buses, traces or lines from the power traces, buses or planes 812 and to separate the signal planes, buses, traces or lines from the ground traces, buses or planes 821, respectively; (2) in the second application of the high current or the high precision circuit, another patterned circuit layer, such as ground planes, buses, traces or lines, (not shown) used to distribute a ground reference voltage may be added over the power traces, buses or planes 812. The power traces, buses or planes 812 are sandwiched by the ground traces, buses or planes 821 under the power traces, buses or planes 812 and the newly-added ground traces, buses or planes over the power traces, buses or planes 812, therefore, forming a Vss/Vcc/Vss structure (the stack is from the bottom to the top) over the passivation layer 5. A polymer layer, such as polyimide, benzocyclobutene (BCB), parylene, epoxy-based material, photoepoxy SU-8, elastomer or silicone, having a thickness of between 2 and 30 microns, is provided between the newly-added ground planes, buses, traces or lines and the power traces, buses or planes 812. A cap polymer layer, such as polyimide, benzocyclobutene (BCB), parylene, epoxy-based material, photoepoxy SU-8, elastomer or silicone, having a thickness of between 2 and 30 microns, covers the newly-added ground planes, buses, traces or lines; (3) in the third application of the high current or the high precision circuit, if required, based on the second application of the Vss/Vcc/Vss structure, another patterned circuit layer, such as power planes, buses, traces or lines, (not shown) used to distribute a power voltage can be further formed over the top ground planes, buses, traces or lines (not shown) over the power traces, buses or planes 812, creating a Vss/Vcc/Vss,/Vcc

structure, (the stack is from the bottom to the top) over the passivation layer 5. A polymer layer, such as polyimide, benzocyclobutene (BCB), parylene, epoxy-based material, photoepoxy SU-8, elastomer or silicone, having a thickness of between 2 and 30 microns, is provided between the newly-added power planes, buses, traces or lines and the top ground traces, buses or planes 81. A cap polymer layer, such as polyimide, benzocyclobutene (BCB), parylene, epoxy-based material, photoepoxy SU-8, elastomer or silicone, having a thickness of between 2 and 30 microns, covers the newly-added power planes, buses, traces or lines. The previously described structures provide a robust power supply for high current circuits, high precision analog circuits, high speed circuits, low power circuits, power management circuits, and high performance circuits.

[00204] Fig. 4 shows a circuit design for the voltage regulator or converter circuit 41 in Figs. 1B, 1C, 2B, 2C, 3B, 3C and 3D. This circuit design is for a voltage regulator or converter circuit 41 usually used in the modern DRAM design as described in "Semiconductor Memories: A handbook of Design, Manufacture and Application" Second Edition, By B. Prince, published by John Wiley & Sons, 1991. The voltage regulator or converter circuit 41 shown in Fig. 4 provides both voltage regulating function and voltage converting function. The external voltage Vdd can be converted to an output voltage Vcc varying at a desired voltage level Vcc0, and the ratio of the difference of between Vcc and Vcc0 to Vcc0 is less than 10%, and preferably less than 5%. As discussed in the section of "description of related arts", more modern IC chips require on-chip voltage converters to convert the external (system, board, module, or card level) power supply voltage to a voltage level required by the chip. Moreover, some chips, such as a DRAM chip, even require dual or even triple voltage levels on the same chip: for example, 3.3 V for peripheral control circuits, while 1.5 V for the memory cells in the cell array area.

[00205] The voltage regulator or converter circuit 41 in Fig. 4 includes two circuit blocks: a voltage reference generator 410 and a current mirror circuit 410'. The voltage reference generator 410 generates a reference voltage V_R at the node R, insensitive to the voltage fluctuation of the external power supply voltage Vdd at node 4199. Vdd is also the input supply voltage of the reference voltage generator 410. The voltage reference generator 410 includes two paths of voltage divider. One path includes three p-channel MOS transistors, 4101, 4103 and 4105 connected in series, and the other path includes two p-channel MOS transistors 4102 and 4104 connected in series. With the drain of the MOS transistor 4103 coupled to the gate of the MOS transistor 4104, the output reference voltage V_R is regulated.

When Vdd is fluctuated with a rise, the voltage level at node G will rise, resulting in a weaker turn-on of the MOS transistor 4104. When the MOS transistor 4104 is turned-on weaker, V_R drops or rises with a smaller extent. Similarly, V_R rises or drops with a smaller extent, when Vdd is fluctuated with a drop. This explains the voltage regulation behavior of the voltage reference generator 410. The output of the voltage reference generator 410 is used as a reference voltage of the current mirror circuit 410'. The current mirror circuit 410' provides a power supply with voltage at a desired constant level and with large current capability for an IC chip. The current mirror circuit 410' also eliminates possible huge power consumption or waste by avoiding a direct high current path from Vdd to Vss in the paths of voltage dividers. With the drain of the p-channel MOS transistor 4109 coupled to the gate of the output p-channel MOS transistor 4106, and with the output voltage node P coupled to the gate of the reference-voltage-mirror p-channel MOS transistor 4110, the output voltage Vcc is regulated, and accordingly the output voltage level Vcc can be designed at a desired level. The conductance transistor 4112 is a small p-channel MOS transistor with a gate connected to Vss, hence the transistor 4112 is always turned on. The conductance transistor 4111 is a large p-channel MOS, and its gate is controlled by a signal Φ. The transistor 4111 is turned on when the internal circuits or internal circuit units are in an active cycle, resulting in a fast response of the current path provided by the p-channel MOS transistor 4109 and n-channel MOS transistor 4107, and of the current path provided by the p-channel MOS transistor 4110 and n-channel MOS transistor 4108. The turn-on of the transistor 4111 minimizes the output supply Vcc bounce caused by a large transient current demanded by the internal circuits, such as 21, 22, 23 and 24, shown in Figs. 1B, 1C, 2B, 2C, 3B, 3C and 3D. When the internal circuits or internal circuit units are in idle cycle, the transistor 4111 is turned off to save power consumption.

Second Embodiment: Over-passivation Interconnection for Internal Circuits

[00206] The coarse traces over the passivation layer 5 described in the first embodiment can be alternatively used as an interconnection of IC internal circuits to transmit a signal from an internal circuit to another one or other ones. In this application, the coarse metal conductor over a passivation layer is used to transmit a signal or data from an output node Xo of an internal circuit 21 to input nodes Ui, Vi and Wi of other internal circuits 22, 23 and 24, as shown in Fig. 5B. When designed as a bundle of metal lines or metal traces that connects a set of similar nodes for inputting or outputting data signals, bit signals or address signals, for example, between two internal functional circuits separated in a longer distance (for example,

in the distance of 1 mm or more 500 microns), such as the 8-, 16-, 32-, 64-, 128-, 256-, 512-, or 1024-bits of data (or address) connection between a processor unit and a memory unit on the same chip, the lines or traces are often referred to as buses, such as word buses or bit buses used in a memory. For these applications, the disclosure provides a thick metal trace, bus or plane 83 over a passivation layer 5, far away from underlying MOS devices, to connect multiple internal circuits 21, 22, 23 and 24, as shown in Fig. 5B, and accordingly allows the electrical signal to pass over MOS devices without perturbing the underlying MOS devices and without significant degradation of signal integrity. It is noted that the thick metal trace, bus or plane 83 over the passivation layer 5 connects the nodes of the internal circuits 21, 22, 23 and 24 not through any off-chip input/output circuit connected with an external circuit, and is not connected up to an external circuit. As the previously described thick metal trace, bus or plane 83 over the passivation layer 5 may induce only very low parasitic capacitance, the signal passing through the thick metal trace, bus or plane 83 will not be dramatically degraded. It makes this disclosure very suitable for high-speed, low power, high current or low voltage applications. In most cases of this disclosure, no additional amplifier, driver/receiver or repeater is required to help sustain the integrity of the signal passing through the thick metal trace, bus or plane 83. In some cases of this disclosure, an internal driver, internal receiver, internal tri-state buffer, or repeater, including MOS transistors with a smaller size as compared to those of the off-chip circuits connected with an external circuit, is required to transmit a signal passing through a long path, such as the thick metal trace, bus or plane 83 having a length of larger than 500 microns or larger than 1000 microns.

[00207] Figs. 5B, 6B, and 7B show a second exemplary embodiment of the disclosure. Fig. 5B shows a simplified circuit diagram where a metal trace, bus or plane 83 over the passivation layer 5 connects multiple internal circuits 21, 22, 23 and 24 to transmit a signal from an output node Xo of an internal circuit 21 to input nodes Ui, Vi and Wi of the internal circuits 22, 23 and 24. Fig. 6B shows a top view of the semiconductor chip realizing the circuitry shown in Fig. 5B. Fig. 7B shows a cross-sectional view of the semiconductor chips realizing the circuitry shown in Figs. 5B. Fig. 6B shows a top view of the semiconductor chip shown in Fig. 7B, and the patterned circuit layer 831, such as signal plane, bus, trace or line, to transmit a signal from the internal circuit 21 to the internal circuits 22, 23 and 24 is realized from the concept of the coarse trace 83 shown in Figs. 5B and 6B. The coarse trace 83 shown in Figs. 5B and 6B indicates a trace of an over-passivation scheme 102 formed over the passivation layer 5, and the fine traces 631, 632 (including 632a, 632b and 632c) and 634

shown in Fig. 5B and the fine traces 632a, 632b and 632c shown in Figs. 6B indicate traces formed under the passivation layer 5.

[00208] As shown in Figs. 5B, 6B and 7B, the internal circuit 21 includes an input node Xi to receive a signal and an output node Xo to output an electrical signal to the internal circuits 22, 23 and 24. The internal circuit 21 can be a logic gate, such as inverter, NOR gate, NAND gate, OR gate, AND gate, or an internal buffer (an inverter, an internal driver, or an internal tri-state buffer, shown in Figs. 5C, 5D, and 5E, respectively). Through the coarse metal scheme 83 over the passivation layer 5, the input nodes Ui, Vi and Wi of the internal logic circuits 22, 23 and 24 (two NOR gates 22 and 24, and one NAND gate 23) are able to receive data or signal sent from the internal circuit 21. The voltage level at input nodes Ui, Vi and Wi are between Vdd and V_{ss} with very minimal degradation and noise in that the interconnecting metal trace or bus 83 over the passivation layer 5 has low resistance and create low capacitance. It is noted that in this design the thick metal trace or bus 83 is not connected to off-chip circuits connected to an external circuit, such as ESD circuit, off-chip driver, off-chip receiver, or off-chip tri-state buffer circuit, resulting in speed improvement and power consumption reduction.

[00209] Figs. 5A, 6A and 7A illustrate the connection between the internal circuits 21, 22, 23 and 24. The technique illustrated in Figs. 5A, 6A and 7A relies on the fine-line metal traces 6311, 6321, 6341 and 638 under the passivation layer 5 to pass data output from the internal circuit 21 to the internal circuits 22, 23 and 24, without relying on any patterned circuit layer over the passivation layer 5.

[00210] Figs. 5B and 6B reveal that the coarse metal scheme 83 is built over the passivation layer 5 of the IC chip, and is connected to the internal circuits 21, 22, 23 and 24. Figs. 5A, 6A and 7A show that the internal circuit 21 is connected to a NOR gate 22 through segments 6311, 638, 6321a and 6321b of the fine-line metal structures under the passivation layer 5, to a NAND gate 23 through segments 6311, 638, 6321a and 6321c of the fine-line metal structures under the passivation layer 5, and to another NOR gate 24 through segments 6311, 638 and 6341 of the fine-line metal structures under the passivation layer 5. In the present disclosure, the second segment 638 of the fine-line metal structure is replaced by a coarse metal conductor 83 over the passivation layer 5, as shown in Figs. 5B and 6B. A signal output from an output node (usually the drain of a MOS transistor in the internal circuit 21) of the internal circuit 21 may pass through a segment 631 of the fine-line metal structure under

the passivation layer 5, then through an opening 531 in the passivation layer 5, then through the interconnection scheme 83 over the passivation layer 5, then through an opening 534 in the passivation layer 5, then through a segment 634 of the fine-line metal structure under the passivation layer 5, and then to an input node (usually the gate of an MOS transistor in the NOR gate 24) of the NOR gate 24. A signal output from an output node (usually the drain of an MOS transistor in the internal circuit 21) of the internal circuit 21 may pass through a segment 631 of the fine-line metal structure under the passivation layer 5, then through the opening 531 in the passivation layer 5, then through the interconnection scheme 83 over the passivation layer 5, then through an opening 532 in the passivation layer 5, then through a segment 632a and a segment 632b or 632c of the fine-line metal interconnection scheme under the passivation layer 5, and then to the input nodes (usually the gates of MOS transistors in the NOR gate 22 and the NAND gate 23, respectively) of a NOR gate 22 and a NAND gate 23.

[00211] Alternatively, when the internal circuit 21 is a NOR gate, the internal circuits 22, 23 and 24 may be NOR gates, OR gates, NAND gate or AND gates. When the internal circuit 21 is an OR gate, the internal circuits 22, 23 and 24 may be NOR gates, OR gates, NAND gate or AND gates. When the internal circuit 21 is a NAND gate, the internal circuits 22, 23 and 24 may be NOR gates, OR gates, NAND gate or AND gates. When the internal circuit 21 is a AND gate, the internal circuits 22, 23 and 24 may be NOR gates, OR gates, NAND gate or AND gates. When a NMOS transistor in the internal circuit 21 having a drain as the output node Xo of the internal circuit 21 has a ratio of a physical channel width thereof to a physical channel length thereof ranging from, e.g., about 0.1 to 20, ranging from, e.g., about 0.1 to 10, or preferably ranging from, e.g., about 0.2 to 2, a NMOS transistor in the internal circuit 22, 23 or 24 having a gate as the input node Ui, Vi and Wi of the internal circuit 22, 23 or 24 has a ratio of a physical channel width thereof to a physical channel length thereof ranging from, e.g., about 0.1 to 20, ranging from, e.g., about 0.1 to 10 or preferably ranging from, e.g., about 0.2 to 2. When a NMOS transistor in the internal circuit 21 having a drain as the output node Xo of the internal circuit 21 has a ratio of a physical channel width thereof to a physical channel length thereof ranging from, e.g., about 0.1 to 20, ranging from, e.g., about 0.1 to 10, or preferably ranging from, e.g., about 0.2 to 2, a PMOS transistor in the internal circuit 22, 23 or 24 having a gate as the input node Ui, Vi and Wi of the internal circuit 22, 23 or 24 has a ratio of a physical channel width thereof to a physical channel length thereof ranging from, e.g., about 0.2 to 40, ranging from, e.g., about 0.2 to 20, or preferably ranging from, e.g., about 0.4 to 4. When a PMOS transistor in the internal circuit 21 having a drain as the output node Xo of

the internal circuit 21 has a ratio of a physical channel width thereof to a physical channel length thereof ranging from, e.g., about 0.2 to 40, ranging from, e.g., about 0.2 to 20, or preferably ranging from, e.g., about 0.4 to 4, a NMOS transistor in the internal circuit 22, 23 or 24 having a gate as the input node Ui, Vi and Wi of the internal circuit 22, 23 or 24 has a ratio of a physical channel width thereof to a physical channel length thereof ranging from, e.g., about 0.1 to 20, ranging from, e.g., about 0.1 to 10, or preferably ranging from, e.g., about 0.2 to 2. When a PMOS transistor in the internal circuit 21 having a drain as the output node Xo of the internal circuit 21 has a ratio of a physical channel width thereof to a physical channel length thereof ranging from, e.g., about 0.2 to 40, ranging from, e.g., about 0.2 to 20, or preferably ranging from, e.g., about 0.4 to 4, a PMOS transistor in the internal circuit 22, 23 or 24 having a gate as the input node Ui, Vi and Wi of the internal circuit 22, 23 or 24 has a ratio of a physical channel width thereof to a physical channel length thereof ranging from, e.g., about 0.2 to 40, ranging from, e.g., about 0.2 to 20, or preferably ranging from, e.g., about 0.4 to 4. In the previously described case, a signal output from the output node Xo of the internal circuit 21 may pass through the thick metal plane, bus, trace or line 83 to the internal circuits 22, 23 and 24, with a current, passing through the thick metal plane, bus, trace or line 83, ranging from, e.g., about 50 microamperes to 2 milliamperes, and preferably ranging from, e.g., about 100 microamperes to 1 milliampere. The fine line metal structures 634, 632 and 631 shown in 7B, 7C and 7D may be formed with multiple circuit layers 60 and multiple stacked plugs 60', upper plugs 60' being aligned with bottom plugs 60'. When the circuit layers 60 are formed with electroplated copper, the stacked plugs 60' may be formed with electroplated copper. When the circuit layers 60 are formed with sputtered aluminum, the stacked plugs 60' may be formed with chemical vapor deposited tungsten. There are multiple insulating layers 30 under the passivation layer 5, and each one is positioned between the neighboring two of the circuit layers 60. The insulating layers 30 made of one or more inorganic materials may include a layer of silicon oxide with a thickness of between 0.01 and 2 micrometers, may include a layer of fluorine doped silicate glass (FSG) with a thickness of between 0.01 and 2 micrometers, or may include a layer with a lower dielectric constant, such as between 1.5 and 3.5, having a thickness of between 0.01 and 2 micrometers, such as black diamond film or a material containing hydrogen, carbon, oxygen and silicon.

[00212] The thick metal trace or plane 83 over the passivation layer 5, shown in Fig. 5B and 6B, may be composed of only one patterned circuit layer 831, as shown in Fig. 7B, or multiple patterned circuit layers 831 and 832, as shown in Fig. 7C. In Fig. 7B, the patterned

circuit layer 831, such as a signal plane, bus, trace or line, to transmit a signal is realized from the concept of the coarse trace 83 shown in Figs. 5B and 6B. In Fig. 7C, the patterned circuit layers 831 and 832, such as signal planes, buses, traces or lines, to transmit a signal is realized from the concept of the coarse trace 83 shown in Figs. 5B and 6B. When the thick metal traces or plane 83 over the passivation layer 5, shown in Figs. 5B and 6B, is composed of multiple patterned circuit layers 831 and 832, as shown in Fig. 7C, a polymer layer 98, such as polyimide (PI), benzocyclobutene (BCB), parylene, photoepoxy SU-8, epoxy-based material, elastomer or silicone, may be between the neighboring patterned circuit layers 831 and 832, separating the patterned circuit layers 831 and 832. The polymer layer 98 may have a thickness between 2 and 30 micrometers. A polymer layer 99, such as polyimide (PI), benzocyclobutene (BCB), parylene, epoxy-based material, photoepoxy SU-8, elastomer or silicone, may be on the topmost one 832 of the patterned circuit layers 831 and 832, separated by the above mentioned polymer layers 98, over the passivation layer 5, as shown in Fig. 7C, or on the only one patterned circuit layer 831, as shown in Figs. 7B and 7D. The polymer layer 99 may have a thickness between 2 and 30 micrometers. It is noted that no opening in the polymer layer 99 exposes the patterned circuit layer 831 or 832, and the patterned circuit layer 831 or 832 has no pad connected up to an external circuit, as shown in Figs. 7B, 7C and 7D. Alternatively, a polymer layer 95, such as polyimide (PI), benzocyclobutene (BCB), parylene, epoxy-based material, photoepoxy SU-8, elastomer or silicone, may be between the passivation layer 5 and the bottommost one 831 of the patterned circuit layers 831 and 832, separated by the above mentioned polymer layers 98, for the structure shown in Fig. 7C, or between the passivation layer 5 and the only one patterned circuit layer 831, as shown in Fig. 7D. The polymer layer 95 may have a thickness between 2 and 30 micrometers. Multiple openings 9519, 9519', 9511, 9512 and 9514 in the polymer layer 95 are substantially aligned with the openings 519, 519', 511, 512 and 514 in the passivation layer 5, respectively. The openings 9531, 9532 and 9534 in the polymer layer 95 expose the pads exposed by the openings 531, 532 and 534 in the passivation layer 5, respectively.

[00213] The openings 9531, 9532 and 9534 in the polymer layer 95 have lower portions having widths or transverse dimensions larger than those of the openings 531, 532 and 534 in the passivation layer 5 aligned with the openings 9531, 9532 and 9534, respectively. The openings 9531, 9532 and 9534 in the polymer layer 95 further expose the passivation layer 5 close to the openings 531, 532 and 534. The shape of the openings 531, 532 and 534 from a top perspective view may be round, square, rectangular or polygon. If the openings 531, 532 and

534 are round, the openings 531, 532 and 534 may have a diameter of between 0.1 and 200 microns, between 1 and 100 microns, or, preferably, between 0.1 and 30 microns. If the openings 531, 532 and 534 are square, the openings 531, 532 and 534 may have a width of between 0.1 and 200 microns, between 1 and 100 microns, or, preferably, between 0.1 and 30 microns. If the openings 531, 532 and 534 are rectangular, the openings 531, 532 and 534 may have a width of between 0.1 and 200 microns, between 1 and 100 microns, or, preferably, between 0.1 and 30 microns, and a length of between 1 micron and 1 centimeter. If the openings 531, 532 and 534 are polygon having more than five sides, the openings 531, 532 and 534 have a largest diagonal length of between 0.1 and 200 microns, between 1 and 100 microns, or, preferably, between 0.1 and 30 microns. Alternatively, the openings 531, 532 and 534 have a largest transverse dimension of between 0.1 and 200 microns, between 1 and 100 microns, or, preferably, between 0.1 and 30 microns. In a case, the openings 531, 532 and 534 have a width of between 0.1 and 30 microns, with the lower portion of the openings 9531, 9532 and 9514 in the polymer layer 95 having a width of between 20 and 100 microns.

[00214] Each of the patterned circuit layers 831 and 832 composing the thick metal trace or plane 83 over the passivation layer 5, shown in Figs 7B, 7C and 7D, may include an adhesion/barrier/seed layer 8311, 8311a, 8311b or 8321 and a bulk conduction metal layer 8112, 8312a, 8312b or 8322. The methods to form the patterned circuit layer 831 or 832 and the specification thereof may follow the methods to form the patterned circuit layer 801, 802 or 803 and the specification thereof shown in Figs. 15A-15L, 16A-16M, 17A-17J, 18A-18I and 19A-19I.

[00215] In Figs. 7B and 7D, there is only one patterned circuit layer 831, including a portion serving as the previously described thick and wide metal trace 83 over the passivation layer 5. The patterned circuit layer 831 may contain an adhesion/barrier layer, a seed layer on the adhesion/barrier layer, and an electroplated metal layer 8312 on the seed layer, the adhesion/barrier layer and the seed layer composing the bottom layer 8311.

[00216] Referring to Fig. 7B, regards to the process for forming the patterned circuit layer 831, the adhesion/barrier layer may be formed by a suitable process or processes, e.g., by sputtering a titanium-containing layer, such as titanium layer or a titanium-tungsten-alloy layer, having a thickness between 1000 and 6000 angstroms, sputtering a chromium-containing layer, such as chromium layer, having a thickness between 1000 and 6000 angstroms, or sputtering a tantalum-containing layer, such as tantalum layer or tantalum-nitride layer, having a thickness