between 1000 and 6000 angstroms, on a silicon-nitride layer of the passivation layer 5 and on contact pads 6390, principally made of aluminum or copper, exposed by multiple openings 531, 532 and 534 in the passivation layer 5. Thereafter, the seed layer may be formed by a suitable process or processes, e.g., by sputtering a copper layer having a thickness between 200 and 3000 angstroms on the adhesion/barrier layer of any previously described material or by sputtering a gold layer having a thickness between 200 and 3000 angstroms on the adhesion/barrier layer of any previously described material. Thereafter, a photoresist layer may be formed on the seed layer, multiple openings in the photoresist layer exposing the seed layer. Thereafter, the metal layer 8312 may be formed by a suitable process or processes, e.g., by electroplating a copper layer having a thickness between 2 and 30 micrometers on the copper layer serving as the seed layer, exposed by the openings in the photoresist layer, by electroplating a copper layer having a thickness between 2 and 30 micrometers on the copper layer serving as the seed layer, exposed by the openings in the photoresist layer and then electroplating a nickel layer having a thickness between 0.5 and 10 micrometers on the electroplated copper layer in the openings in the photoresist layer, by electroplating a copper layer having a thickness between 2 and 30 micrometers on the copper layer serving as the seed layer, exposed by the openings in the photoresist layer, electroplating a nickel layer having a thickness between 0.5 and 10 micrometers on the electroplated copper layer in the openings in the photoresist layer and then electroplating a gold layer, platinum layer, palladium layer or ruthenium layer having a thickness between 0.05 and 2 micrometers on the electroplated nickel layer in the openings in the photoresist layer, or by electroplating a gold layer having a thickness between 2 and 30 micrometers on the gold layer serving as the seed layer, exposed by the openings in the photoresist layer. Thereafter, the photoresist layer may be removed. Thereafter, the seed layer not under the metal layer 8312 is removed using a wet-etching process or using a dry-etching process. Thereafter, the adhesion/barrier layer not under the metal layer 8312 is removed using a wet-etching process or using a dry-etching process.

[00217] After the patterned circuit layer 831 is formed, a polymer layer 99 can be formed by a suitable process or processes, e.g., by spin-on coating a negative photosensitive polyimide layer, such as ester type, on the patterned circuit layer 831 and on the nitride layer of the passivation layer 5 and then curing the spin-on coated polyimide layer at the temperature between 265 and 285°C for a time between 30 and 240 minutes in a nitrogen or oxygen-free ambient. No opening is formed in the polymer layer 99 to expose the thick and wide metal trace 83.

[00218] Referring to Fig. 7D, before the patterned circuit layer 831 is formed, a polymer layer 95 can be optionally formed by a suitable process or processes, e.g., by spin-on coating a negative photosensitive polyimide layer, such as ester type, on the nitride layer of the passivation layer 5 and on the contact pads exposed by the openings 531, 532 and 534 in the passivation layer 5, exposing the spin-on coated photosensitive polyimide layer, developing the exposed polyimide layer and then curing the developed polyimide layer at the temperature between 265 and 285°C for a time between 30 and 240 minutes in a nitrogen or oxygen-free ambient. Accordingly, multiple openings 9531, 9532 and 9534 may be formed in the polymer layer 95, exposing multiple contact pads exposed by the openings 531, 532 and 533 in the passivation layer 5. After the polymer layer 95 is formed, the patterned circuit layer 831 can be formed on the polymer layer 95 and on the contact pads exposed by the openings 531, 532 and 533. The adhesion/barrier layer of any previously described material may be sputtered on the polymer layer 95 and on the contact pads exposed by the openings 9531, 9532 and 9534 in the polymer layer 95.

[00219] Alternatively, referring to Fig. 7C, there may be multiple patterned circuit layers 831 and 832, including a portion serving as the previously described thick and wide metal trace 83, over the passivation layer 5. The process for forming the patterned circuit layer 831 shown in Fig. 7C can be referred to as the process for forming the patterned circuit layer 831 shown in Fig. 10B. The patterned circuit layer 832 may contain an adhesion/barrier layer, a seed layer on the adhesion/barrier layer, and an electroplated metal layer 8322 on the seed layer, the adhesion/barrier layer and the seed layer composing the bottom layer 8321.

[00220] Referring to Fig. 7C, after the patterned circuit layer 831 is formed, a polymer layer 98 can be formed by a suitable process or processes, e.g., by spin-on coating a negative photosensitive polyimide layer, such as ester type, on the patterned circuit layer 831 and on the nitride layer of the passivation layer 5, exposing the spin-on coated photosensitive polyimide layer, developing the exposed polyimide layer and then curing the developed polyimide layer at the temperature between 265 and 285°C for a time between 30 and 240 minutes in a nitrogen or oxygen-free ambient. Accordingly, multiple openings 9831 and 9834 may be formed in the polymer layer 98, exposing multiple contact pads of the patterned circuit layer 831.

[00221] Referring to Fig. 7C, regards to the process for forming the patterned circuit layer 832, the adhesion/barrier layer may be formed by a suitable process or processes, e.g., by sputtering a titanium-containing layer, such as titanium layer or a titanium-tungsten-alloy layer,

having a thickness between 1000 and 6000 angstroms, sputtering a chromium-containing layer, such as chromium layer, having a thickness between 1000 and 6000 angstroms, or sputtering a tantalum-containing layer, such as tantalum layer or tantalum-nitride layer, having a thickness between 1000 and 6000 angstroms, on the polymer layer 98 and on the contact pads of the patterned circuit layer 831 exposed by multiple openings 9831 and 9834 in the polymer layer 98. Thereafter, the seed layer may be formed by a suitable process or processes, e.g., by sputtering a copper layer having a thickness between 200 and 3000 angstroms on the adhesion/barrier layer of any previously described material or by sputtering a gold layer having a thickness between 200 and 3000 angstroms on the adhesion/barrier layer of any previously described material. Thereafter, a photoresist layer may be formed on the seed layer, multiple openings in the photoresist layer exposing the seed layer. Thereafter, the metal layer 8322 may be formed by a suitable process or processes, e.g., by electroplating a copper layer having a thickness between 2 and 30 micrometers on the copper layer serving as the seed layer, exposed by the openings in the photoresist layer, by electroplating a copper layer having a thickness between 2 and 30 micrometers on the copper layer serving as the seed layer, exposed by the openings in the photoresist layer and then electroplating a nickel layer having a thickness between 0.5 and 10 micrometers on the electroplated copper layer in the openings in the photoresist layer, by electroplating a copper layer having a thickness between 2 and 30 micrometers on the copper layer serving as the seed layer, exposed by the openings in the photoresist layer, electroplating a nickel layer having a thickness between 0.5 and 10 micrometers on the electroplated copper layer in the openings in the photoresist layer and then electroplating a gold layer, platinum layer, palladium layer or ruthenium layer having a thickness between 0.05 and 2 micrometers on the electroplated nickel layer in the openings in the photoresist layer, or by electroplating a gold layer having a thickness between 2 and 30 micrometers on the gold layer serving as the seed layer, exposed by the openings in the photoresist layer. Thereafter, the photoresist layer may be removed. Thereafter, the seed layer not under the metal layer 8322 is removed using a wet-etching process or using a dry-etching process. Thereafter, the adhesion/barrier layer not under the metal layer 8322 is removed using a wet-etching process or using a dry-etching process.

[00222] After the patterned circuit layer 832 is formed, a polymer layer 99 can be formed by a suitable process or processes, e.g., by spin-on coating a negative photosensitive polyimide layer, such as ester type, on the patterned circuit layer 832 and on the polymer layer

98, and then curing the spin-on coated polyimide layer at the temperature between 265 and 285°C for a time between 30 and 240 minutes in a nitrogen or oxygen-free ambient.

[00223] Alternatively, referring to Fig. 7C, before the patterned circuit layer 831 is formed, a polymer layer 95 as mentioned in Fig. 7D can be optionally formed by a suitable process or processes, e.g., by spin-on coating a negative photosensitive polyimide layer, such as ester type, on the nitride layer of the passivation layer 5 and on the contact pads exposed by the openings 531, 532 and 534 in the passivation layer 5, exposing the spin-on coated photosensitive polyimide layer, developing the exposed polyimide layer and then curing the developed polyimide layer at the temperature between 265 and 285°C for a time between 30 and 240 minutes in a nitrogen or oxygen-free ambient. Accordingly, multiple openings 9531, 9532 and 9534 may be formed in the polymer layer 95 as mentioned in Fig. 7D, exposing multiple contact pads exposed by the openings 531, 532 and 533 in the passivation layer 5. After the polymer layer 95 is formed, the patterned circuit layer 831 can be formed on the polymer layer 95 and on the contact pads exposed by the openings 531, 532 and 533. The adhesion/barrier layer of any previously described material may be sputtered on the polymer layer 95 and on the contact pads exposed by the openings 9531, 9532 and 9534 in the polymer layer 95.

[00224] Fig. 7C is similar to Fig. 7B except the thick metal planes, buses or traces 83 are composed of two patterned circuit layers 831 and 832; the bottom one is composed of segments 831a and 831b. A polymer layer 98 separates the patterned circuit layer 831 from the patterned circuit layer 832. In Fig. 7C, the thick metal plane, trace or bus 831 in Fig. 7B is replaced by the thick metal plane, trace or bus 831a, 831b and 832. Referring to Fig. 7C, a signal output from the output node (usually the drain of an MOS transistor in the internal circuit 21) of the internal circuit 21 passes through the fine-line metal buses or traces 631 under the passivation layer 5, then through the opening 531 in the passivation layer 5, then through the metal trace or bus 831b over the passivation layer 5, (1) in a first path, then up through an opening 9831 in the polymer layer 98, then through the metal bus or trace 832 on the polymer layer 98, then down through an opening 9834 in the polymer layer 98, then through the metal trace or bus 831a over the passivation layer 831a, then through an opening 534 in the passivation layer 5, then through the fine-line metal structure 634 under the passivation layer 5, and to the input node (usually the gate of an MOS transistor in the NOR gate 24) of the NOR gate 24; (2) in a second path, then down through an opening 532 in the passivation layer 5, then through the fine-line metal interconnection scheme 632 under the passivation layer 5, and

then to the input nodes (usually the gates of MOS transistors in the NOR gate 24 and the NAND gate 23, respectively) of the NOR gate 22 and the NAND gate 23.

[00225] Referring to 5B, 6B, 7B, 7C and 7D, the metal trace or bus 83 over the passivation layer 5 can be connected to an off-chip I/O circuit connected to an external circuit, and accordingly the thick metal trace or bus 83 has no significant voltage drop or signal degradation. The over-passivation scheme 102 shown in Fig. 7B includes the polymer layer 99 and the metal trace 83 provided by the patterned circuit layer 831. The over-passivation scheme 102 shown in Fig. 7C includes two polymer layers 98 and 99 and the metal trace 83 provided by the patterned circuit layers 831 and 832, and the openings 9831 and 9834 in the polymer layer 98 are over the patterned circuit layers 831. The over-passivation scheme 102 shown in Fig. 7D includes two polymer layers 95 and 99 and the metal trace 83 provided by the patterned circuit layer 831, and the openings 9531, 9532 and 9534 are in the polymer layer 95.

[00226] Now refer to Figs. 5C-5E showing internal buffer circuits applied to the internal circuit 21. The internal circuit 21 shown in Fig. 5B, 6B, 7B, 7C and 7D may be an internal inverter shown in Fig. 5C. In a first application, the size of the n-channel MOS 2101 and p-channel MOS 2102 can be designed in a size often employed in the internal circuits 22, 23 and 24. The size of an MOS transistor is defined as a ratio of a physical channel width thereof to a physical channel length thereof. The n-channel MOS transistor 2101 may have a ratio of a physical channel width thereof to a physical channel length thereof ranging from, e.g., about 0.1 to 20, ranging from, e.g., about 0.1 to 10, or preferably ranging from, e.g., about 0.2 to 2. The p-channel MOS transistor 2102 may have a ratio of a physical channel width thereof to a physical channel length thereof ranging from, e.g., about 0.2 to 40, ranging from, e.g., about 0.2 to 20, or preferably ranging from, e.g., about 0.4 to 4. In the first application, a current passing through the thick metal trace 83 over the passivation layer 5 and outputting from the node Xo of the internal circuit 21 may be in a range of between 50 μA and 2 mA, and preferably of between 100 μA and 1 mA. In a second application, a larger drive current is required for the output of the inverter 211, for example, when a heavy load is demanded by the load internal circuits 22, 23 and 24, or when the internal circuits 22, 23 and 24 are located far away from the internal circuit 21, requiring interconnection metal lines or traces connecting the internal circuit 21 and the internal circuits 22, 23 and 24 in a distance of larger than 1 mm or of larger than 3mm, for example. In the second application, the current output from the inverter 211 is higher than that output from the regular internal circuit, and is, for example, at 1mA or 5

mA, or in a range of between 500 μA and 10 mA, and preferably of between 700 μA and 2 mA. Hence, in the second application, the n-channel MOS transistor 2101 may have a ratio of a physical channel width thereof to a physical channel length thereof ranging from, e.g., about 1.5 to 30, and preferably ranging from, e.g., about 2.5 to 10. The p-channel MOS transistor 2102 may have a ratio of a physical channel width thereof to a physical channel length thereof ranging from, e.g., about 3 to 60, and preferably ranging from, e.g., about 5 to 20.

[00227] When the inverter 211 shown in Fig. 5C is applied to the internal circuit 21 as shown in Figs. 5B, 6B, 7B, 7C and 7D, the drains of the n-channel MOS transistor 2101 and p-channel MOS transistor 2102, serving as the output node Xo of the internal circuit 21, are connected to the thick metal traces or buses 83, 831 or 832 over the passivation layer 5 as shown in Figs. 5B, 6B, 7B, 7C and 7D. The gates of the n-channel MOS transistor 2101 and p-channel MOS transistor 2102 serve as the input node Xi of the internal circuit 21.

[00228] Referring to Fig. 5C, the previously described power plane, bus or trace 81, 811 or 812, as shown in Figs. 1B, 1C, 2B, 2C, 3B, 3C and 3D, over the passivation layer 5 may connect the node P of the voltage regulator or converter circuit 41 and the source of the p-channel MOS device 2102. The previously described power plane, bus or trace 81, 811 or 812 may contain a patterned circuit layer over the patterned circuit layers 831 and/or 832 of the thick and wide signal trace, bus or plane 83 as shown in Figs 7B-7D. Alternatively, the thick and wide signal trace, bus or plane 83 as shown in Figs 7B-7D may contain a patterned circuit layer over that of the previously described power plane, bus or trace 81. The previously described ground plane, bus or trace 82 or 821, as shown in Figs. 1C, 2C and 3C, over the passivation layer 5 may connect the node Rs of the voltage regulator or converter circuit 41 and the source of the n-channel MOS device 2101. The previously described ground plane, bus or trace 82 or 821 may contain a patterned circuit layer over the patterned circuit layers 831 and/or 832 of the thick and wide signal trace, bus or plane 83 as shown in Figs 7B-7D. Alternatively, the thick and wide signal trace, bus or plane 83 as shown in Figs 7B-7D may contain a patterned circuit layer over that of the previously described ground plane, bus or trace 82.

[00229] Figs. 5D and 5E show an internal driver 212 and internal tri-state output buffer 213, respectively. When the internal driver 212 shown in Fig. 5D is applied to the internal circuit 21 as shown in Figs. 5B, 6B, 7B, 7C and 7D, the drains of a n-channel MOS transistor 2103 and p-channel MOS transistor 2104, serving as the output node Xo of the internal circuit

21, are connected to the thick metal traces or buses 83, 831 or 832 over the passivation layer 5. The gates of a n-channel MOS transistor 2103' and p-channel MOS transistor 2104' serve as the input node Xi of the internal circuit 21. The drains of the n-channel MOS transistor 2103' and p-channel MOS transistor 2104' are connected to the gates of the n-channel MOS transistor 2103 and p-channel MOS transistor 2104.

[00230] When the internal tri-state output buffer 213 shown in Fig. 5E is applied to the internal circuit 21 as shown in Figs. 5B, 6B, 7B, 7C and 7D, the drains of a n-channel MOS transistor 2107' and p-channel MOS transistor 2108' with a switch function controlled by an Enable signal transmitted to the gate of the n-channel MOS transistor 2107' and Enable(bar) signal transmitted to the gate of the p-channel MOS transistor 2108', serving as the output node Xo of the internal circuit 21, are connected to the thick metal traces or buses 83, 831 or 832 over the passivation layer 5 as shown in Figs. 5B, 6B, 7B, 7C and 7D. The gates of a n-channel MOS transistor 2107 and p-channel MOS transistor 2108 serve as the input node Xi of the internal circuit 21. The drains of a n-channel MOS transistor 2107 and p-channel MOS transistor 2108 are connected to the sources of the n-channel MOS transistor 2107' and p-channel MOS transistor 2108', respectively.

[00231] The internal driver 212 or internal tri-state output buffer 213, used to drive a signal through the post-passivation metal traces 83 and to the internal circuits 22, 23 and 24, as shown in Fig. 5D or 5E, is similar to the off-chip driver or off-chip tri-state output buffer used to drive an external circuitry, to be discussed in the following Fig. 11A or 11D, respectively, except that (1) the output node Xo of the internal driver 212 or internal tri-state output buffer 213 is not connected to an external circuit; (2) the largest one of p-MOS transistors in the internal driver 212 or internal tri-state output buffer 213 has a ratio of a physical channel width thereof to a physical channel length thereof smaller than that of the largest one of p-MOS transistors in the off-chip driver or off-chip tri-state output buffer connected to an external circuit. The internal tri-state output buffer 213 provides drive capability and switch capability, and is particularly useful to transmit a data signal or an address signal in a memory chip through the thick metal lines or traces 83 over the passivation layer 5 acting as data or address buses.

[00232] In Fig. 5B, a relatively large drive current may be required at the output node Xo of the internal circuit 21 when a heavy load is demanded by the internal circuits 22, 23 and 24, or when the internal circuits 22, 23 and 24 are far away from the internal circuit 21 in a

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distance of larger than 1 mm or of larger than 3mm. To provide a relatively large drive current, the internal circuit 21 can be designed as an internal driver 212 shown in Fig. 5D or an internal tri-state output buffer 213 shown in Fig. 5E.

[00233] IIn Figs. 5D and 5E, the n-channel MOS transistors 2103, 2107 and 2107' may have a ratio of a physical channel width thereof to a physical channel length thereof ranging from, e.g., about 1.5 to 30, and preferably ranging from, e.g., about 2.5 to 10. The p-channel MOS transistors 2104, 2108 and 2108' may have a ratio of a physical channel width thereof to a physical channel length thereof ranging from, e.g., about 3 to 60, and preferably ranging from, e.g., about 5 to 20. In Fig. 5D, the n-channel MOS transistor 2103' may have a ratio of a physical channel width thereof to a physical channel length thereof ranging from, e.g., about 0.1 to 20, ranging from, e.g., about 0.1 to 10, or preferably ranging from, e.g., about 0.2 to 2, and the p-channel MOS transistor 2104' may have a ratio of a physical channel width thereof to a physical channel length thereof ranging from, e.g., about 0.2 to 40, ranging from, e.g., about 0.2 to 20, or preferably ranging from, e.g., about 0.4 to 4. Referring to Figs. 5B, 5D and 5E, the internal driver 212 or internal tri-state buffer 213 may drive a signal output from the output node Xo thereof through the thick metal trace or bus 83 over the passivation layer 5 to the input nodes Ui, Vi and Wi of the internal circuits 22, 23 and 24 but not to an external circuit. A current passing through the thick metal trace or line 83 over the passivation layer 5 and outputting from the node Xo of the internal circuit 21, provided by the internal driver 212 or internal tri-state buffer 213, may be between 500 μA and 10 mA, and preferably between 700 μA and 2 mA.

[00234] Referring to Fig. 5D, the previously described power plane, bus or trace 81, 811 or 812, as shown in Figs. 1B, 1C, 2B, 2C, 3B, 3C and 3D, over the passivation layer 5 can connect the node P of the voltage regulator or converter circuit 41 and the sources of the p-channel MOS devices 2104 and 2104'. The previously described power plane, bus or trace 81, 811 or 812 may contain a patterned circuit layer over the patterned circuit layers 831 and/or 832 of the thick and wide signal trace, bus or plane 83 as shown in Figs 7B-7D. Alternatively, the thick and wide signal trace, bus or plane 83 as shown in Figs 7B-7D may contain a patterned circuit layer over that of the previously described power plane, bus or trace 81. The previously described ground plane, bus or trace 82 or 821, as shown in Figs. 1C, 2C and 3C, over the passivation layer 5 can connect the node Rs of the voltage regulator or converter circuit 41 and the sources of the n-channel MOS devices 2103 and 2103'. The previously described ground plane, bus or trace 82 or 821 may contain a patterned circuit layer over the

patterned circuit layers 831 and/or 832 of the thick and wide signal trace, bus or plane 83 as shown in Figs 7B-7D. Alternatively, the thick and wide signal trace, bus or plane 83 as shown in Figs 7B-7D may contain a patterned circuit layer over that of the previously described ground plane, bus or trace 82.

[00235] Referring to Fig. 5E, the previously described power plane, bus or trace 81, 811 or 812, as shown in Figs. 1B, 1C, 2B, 2C, 3B, 3C and 3D, over the passivation layer 5 can connect the node P of the voltage regulator or converter circuit 41 and the source of the p-channel MOS device 2108. The previously described power plane, bus or trace 81, 811 or 812 may contain a patterned circuit layer over the patterned circuit layers 831 and/or 832 of the thick and wide signal trace, bus or plane 83 as shown in Figs 7B-7D. Alternatively, the thick and wide signal trace, bus or plane 83 as shown in Figs 7B-7D may contain a patterned circuit layer over that of the previously described power plane, bus or trace 81. The previously described ground plane, bus or trace 82 or 821, as shown in Figs. 1C, 2C and 3C, over the passivation layer 5 can connect the node Rs of the voltage regulator or converter circuit 41 and the source of the n-channel MOS device 2107. The previously described ground plane, bus or trace 82 or 821 may contain a patterned circuit layer over the patterned circuit layers 831 and/or 832 of the thick and wide signal trace, bus or plane 83 as shown in Figs 7B-7D. Alternatively, the thick and wide signal trace, bus or plane 83 as shown in Figs 7B-7D may contain a patterned circuit layer over that of the previously described ground plane, bus or trace 82.

[00236] Alternatively, when a NMOS transistor in the internal circuit 21 having a drain as the output node Xo of the internal circuit 21 has a ratio of a physical channel width to a physical channel length ranging from, e.g., about 1.5 to 30, and preferably ranging from, e.g., about 2.5 to 10, a NMOS transistor in the internal circuit 22, 23 or 24 having a gate as the input node Ui, Vi and Wi of the internal circuit 22, 23 or 24 has a ratio of physical channel width to physical channel length ranging from, e.g., about 0.1 to 20, ranging from, e.g., about 0.1 to 10, or preferably ranging from, e.g., about 0.2 to 2. When a NMOS transistor in the internal circuit 21 having a drain as the output node Xo of the internal circuit 21 has a ratio of a physical channel width to a physical channel length ranging from, e.g., about 1.5 to 30, and preferably ranging from, e.g., about 2.5 to 10, a PMOS transistor in the internal circuit 22, 23 or 24 having a gate as the input node Ui, Vi and Wi of the internal circuit 22, 23 or 24 has a ratio of a physical channel width to a physical channel length ranging from, e.g., about 0.2 to 40, ranging from, e.g., about 0.2 to 20, or preferably ranging from, e.g., about 0.4 to 4. When a PMOS

transistor in the internal circuit 21 having a drain as the output node Xo of the internal circuit 21 has a ratio of a physical channel width to a physical channel length ranging from, e.g., about 3 to 60, and preferably ranging from, e.g., about 5 to 20, a NMOS transistor in the internal circuit 22, 23 or 24 having a gate as the input node Ui, Vi and Wi of the internal circuit 22, 23 or 24 has a ratio of a physical channel width to a physical channel length ranging from, e.g., about 0.1 to 20, ranging from, e.g., about 0.1 to 10, or preferably ranging from, e.g., about 0.2 to 2. When a PMOS transistor in the internal circuit 21 having a drain as the output node Xo of the internal circuit 21 has a ratio of a physical channel width to a physical channel length ranging from, e.g., about 3 to 60, and preferably ranging from, e.g., about 5 to 20, a PMOS transistor in the internal circuit 22, 23 or 24 having a gate as the input node Ui, Vi and Wi of the internal circuit 22, 23 or 24 has a ratio of a physical channel width to a physical channel length ranging from, e.g., about 0.2 to 40, ranging from, e.g., about 0.2 to 20, or preferably ranging from, e.g., about 0.4 to 4. In the previously described case, a signal output from the output node Xo of the internal circuit 21 may pass through the thick metal plane, bus, trace or line 83 to the internal circuits 22, 23 and 24, with a current, passing through the thick metal plane, bus, trace or line 83, ranging from, e.g., about 500 microamperes to 10 milliamperes, and preferably ranging from, e.g., about 700 microamperes to 2 milliamperes.

[00237] The concept shown in Fig. 5B can be applied to a memory chip, as illustrated in Figs. 5F-5J.

[00238] Referring to Fig. 5F, the previously described tri-state output buffer 213 is employed to be the internal circuit 21 shown in Figs. 5B, 6B, 7B, 7C and 7D and has an input node Xi connected to an output node of an amplifier 214 and an output node Xo connected to the internal circuits 22, 23 and 24, such as logic gates, through the above mentioned thick metal plane, bus or trace 83, 831 or 832 over the passivation layer 5, as shown in Figs. 5B, 6B, 7B, 7C and 7D, and the internal circuits 22, 23 and 24 may alternatively be NOR gate, NAND gate, AND gate, OR gate, operational amplifier, adder, multiplexer, diplexer, multiplier, A/D converter, D/A converter, CMOS transistor, bipolar CMOS transistor or bipolar circuit. The semiconductor chip may include a memory array including multiple memory cells connected to word lines, bit lines and bit (bar) lines. Each pair of bit line, such as 2171, and bit (bar) line, such as 2172, is connected to one of the amplifiers, such as 214, through the channel of the n-channel MOS transistors 2123 and 2122 controlled by CS1 node. When the n-channel MOS transistors 2122 and 2123 are turned off in an inactive cycle, the noise on the bit line 2171 or

on the bit (bar) line 2172 can not be transmitted to the sense amplifier 214 nor has a negative impact on the sense amplifier 214.

[00239] In this case, the memory cell 215 is a static random access memory (SRAM) cell. Alternatively, the memory cell 215 may be a dynamic random access memory (DRAM) cell, an erasable programmable read only memory (EPROM) cell, an electronic erasable programmable read only memory (EEPROM) cell, a flash memory cell, a read only memory (ROM) cell, or a magnetic random access memory (MRAM) cell, which is connected to one or more logic gates 22, 23 and 24 through a thick metal traces 83, 831 or 832 over the passivation layer 5, as shown in Figs. 5B, 6B, 7B, 7C and 7D. A sense amplifier 214, tri-state buffer 213, pass gate 216, latch memory 217 or internal driver 212, as shown in Figs. 5F-5J, may be optionally set on the path between any kind of memory cell 215 and the thick metal traces 83, 831 or 832 over the passivation layer 5.

[00240] In case of SDRAM cell acting as the memory cell 215, a plurality of the memory cell 215 may be arranged in an array. A plurality of bit line 2171 and bit (bar) line 2172 arranged in parallel are connected to the sources or drains of NMOS transistors 2120 and 2119 of the memory cells 215 arranged in a column, respectively. A plurality of word line arranged in parallel and in vertical to the bit line 2171 and bit (bar) line 2172 is connected to the gate of NMOS transistors 2120 and 2119 of the memory cells 215 arranged in a row. The memory cell 215 further includes two PMOS transistors 2116 and 2118 and two NMOS transistors 2115 and 2117, and the gates of the PMOS transistor 2116 and the NMOS transistor 2115 and the drains of the PMOS transistor 2118 and the NMOS transistor 2117 are connected to the bit line 2171 through the channel of the NMOS transistor 2120, and the gates of the PMOS transistor 2118 and the NMOS transistor 2117 and the drains of the PMOS transistor 2116 and the NMOS transistor 2115 are connected to the bit (bar) line 2172 through the channel of the NMOS transistor 2119.

[00241] The sense amplifier 214, such as differential amplifier, can be coupled to multiple memory cells 215 arranged in a column through the bit line 2171 and the bit (bar) line 2172. The sense amplifier 214 includes two PMOS transistors 2112 and 2114 and two NMOS transistors 2111 and 2113, and the gates of the PMOS transistors 2112 and 2114 are connected to the drains of the NMOS transistor 2111 and the PMOS transistor 2112, and the drains of the PMOS transistor 2114 and the NMOS transistor 2113 serving as an output node of the sense amplifier 214 are connected to the gates of the PMOS transistor 2108 and the NMOS

transistor 2107 in the previously described tri-state buffer 213. The gate of the NMOS transistor 2113 is connected to the bit line 2171. The gate of the NMOS transistor 2111 is connected to the bit (bar) line 2172. The description and specification of the tri-state buffer 213 may be referred to the above illustration shown in Fig. 5E.

[00242] Referring to Fig. 5F, the node P of the voltage regulator or converter circuit 41 can be connected to the sources of the PMOS transistors 2116 and 2118 of the memory cell 215, the sources of the PMOS transistors 2112 and 2114 of the sense amplifier 214 and the source of the PMOS transistor 2108 of the tri-state output buffer 213 through the previously described power plane, bus or trace 81, 811 or 812, as shown in Figs. 1B, 1C, 2B, 2C, 3B, 3C and 3D, over the passivation layer 5. The previously described power plane, bus or trace 81, 811 or 812 may contain a patterned circuit layer over the patterned circuit layers 831 and/or 832 of the thick and wide signal trace, bus or plane 83 as shown in Figs 7B-7D. Alternatively, the thick and wide signal trace, bus or plane 83 as shown in Figs 7B-7D may contain a patterned circuit layer over that of the previously described power plane, bus or trace 81. The node Rs of the voltage regulator or converter circuit 41 can be connected to the sources of the NMOS transistors 2115 and 2117 of the memory cell 215, the sources of the NMOS transistors 2111 and 2113 of the sense amplifier 214 and the source of the NMOS transistor 2107 of the tri-state output buffer 213 through the previously described ground plane, bus or trace 82 or 821, as shown in Figs. 1C, 2C and 3C, over the passivation layer 5. The differential sense amplifier 214 is isolated from Vss by a transistor 2121, and controlled by a column selection signal (CS2) to save power consumption. The transistor 2121 is turned off when the memory cell 215 is not read. The previously described ground plane, bus or trace 82 or 821 may contain a patterned circuit layer over the patterned circuit layers 831 and/or 832 of the thick and wide signal trace, bus or plane 83 as shown in Figs 7B-7D. Alternatively, the thick and wide signal trace, bus or plane 83 as shown in Figs 7B-7D may contain a patterned circuit layer over that of the previously described ground plane, bus or trace 82.

[00243] When the memory cell 215 is in a "READ" operation with the NMOS transistors 2120 and 2119 being turned on, the state latched in the memory cell 215, such as bit data and bit (bar) data, may be output to the bit line 2171 and bit (bar) line 2172 through the channels of the NMOS transistors 2120 and 2119, respectively. The bit data and bit (bar) data may be transmitted to the sense amplifier 214 through the bit line 2171 and bit (bar) line 2172, respectively, to initially amplify the bit data and the bit (bar) data, leading the bit data and the bit (bar) data to have a desirable waveform or voltage level. The initially amplified bit data or

bit (bar) data output from the amplifier 214 may be transmitted to a tri-state output buffer 213 to further amplify the initially amplified bit data or bit (bar) data, but Fig. 5F only show the initially amplified bit (bar) data output from the amplifier 214 is transmitted to the input node Xi of the tri-state output buffer 213. Further amplified bit (bar) data or bit data output from a tri-state buffer can be transmitted to the internal circuits 22, 23 and 24 through the thick metal planes or buses 83, 831 or 832, as shown in Figs. 5B, 6B, 7B, 7C and 7D, but Fig. 5F only show the further amplified bit data is output from the tri-state output buffer 213.

[00244] The bit line 2171 and bit (bar) line 2172 may be provided by fine-line metal layers, made of sputtered aluminum or damascene copper, only under the passivation layer 5. Alternatively, the bit line 2171 and bit (bar) line 2172 may be provided by the interconnecting structure over the passivation layer 5 and under the passivation layer 5, and the portion under the passivation layer 5 may include sputtered aluminum layer or damascene copper layer having a thickness of between 0.01 and 2 microns, and the portion over the passivation layer 5 may include electroplated copper or electroplated gold having a thickness of between 2 and 20 microns.

[00245] In this case, the thick metal buses or traces 83, 831 or 832 shown in Figs. 5B, 6B, 7B, 7C and 7D may be called as bit buses to transmit further amplified bit data or bit (bar) data with 4 bits width, 8 bits width, 16 bits width, 32 bits width, 64 bits width, 128 bits width, 256 bits width, 512 bits width, 1024 bits width, 2048 bits width or 4096 bits width, output from the tri-state buffers 213. Accordingly, 4, 8, 16, 32, 64, 128, 256, 512, 1024, 2048 or 4098 bit buses arranged in parallel and over the passivation layer 5, may connect the output nodes Xo of multiple internal circuits 21, the tri-state buffers 213 in this case, to multiple internal circuits 22, 23 and 24, such as NOR gates, NAND gates, AND gates, OR gates, operational amplifiers, adders, multiplexers, diplexers, multipliers, A/D converters, D/A converters, CMOS transistors, bipolar CMOS transistors or bipolar circuits.

[00246] Alternatively, multiple address buses 85 connecting an address decoder 205 and the outputs of multiple internal circuits 25 and 26 can be formed over the passivation layer 5, as shown in Fig. 5U, to transmit an address data from one of the internal circuits 25 and 26 to the address decoder 205 during a "READ" operation, and the internal circuits 25 and 26 may be NOR gate, NAND gate, AND gate, OR gate, operational amplifier, adder, multiplexer, diplexer, multiplier, A/D converter, D/A converter, CMOS transistor, bipolar CMOS transistor or bipolar circuit. The address decoder 205 is connected to multiple word lines coupled with

multiple memory cells in a memory array. Referring to Figs. 5F and 5U, one of the word lines 2175 is connected to the gates of the NMOS transistors 2120 and 2119 of the memory cell 115, transmitting a signal from the address decoder 205 to the memory cell to control whether the logic level of bit data saved in the trace connecting the drains of the PMOS transistor 2118 and NMOS transistor 2117 and the gates of the PMOS transistor 2116 and NMOS transistor 2115 and the logic level of bit (bar) data saved in the trace connecting the drains of the PMOS transistor 2116 and NMOS transistor 2115 and the gates of the PMOS transistor 2118 and NMOS transistor 2117 are transmitted to the bit line 2171 and the bit (bar) line 2172 through the channels of the NMOS transistors 2120 and 2119, respectively. The sense amplifier 214 receives the bit data and bit (bar) data and initially amplifies the bit (bar) data. The initially amplified the bit (bar) data output from the sense amplifier 214 may be transmitted to the gates of the PMOS transistor 2108 and NMOS transistor 2107 of the tri-state buffer 213 through the trace 2179 under the passivation layer 5. Two traces 2177 and 2178 connect the address decoder 205 and the tri-state buffer 213, transmitting an ENABLE signal and an ENABLE (bar) signal from the address decoder 205 to the tri-state buffer 213 to control whether the previously described further amplified bit signal is output from the tri-state buffer 213 to the data bus 83 over the passivation layer 5.

[00247] Other embodiments as described below can be alternatively attained. Same reference numbers in this patent application indicate same or similar elements.

[00248] Referring to Figs. 5B, 6B, 7B, 7C and 7D, the internal circuit 21 may be a pass gate 216 as shown in Fig. 5G. The pass gate 216 may include an NMOS transistor 2124 having a gate connected to an address decoder 205 through a trace 2180 under the passivation layer 5, as shown in Fig. 5V. In a "READ" operation, the address decoder 205 receives an address data through multiple address buses 85 over the passivation layer 5. The address decoder 205 output a READ ENABLE data to the gate of the NMOS transistor 2124 through the trace 2180 to control whether the NMOS transistor 2124 is turned on or off. When the NMOS transistor 2124 of the pass gate 216 is turned on, the initially amplified bit (bar) data output from the sense amplifier 214 can be transmitted to the data bus 83, 831 or 832 over the passivation layer 5 through the channel of the NMOS transistor 2124.

[00249] Referring to Figs. 5B, 6B, 7B, 7C and 7D, the internal circuit 21 may be a latch circuit 217 as shown in Fig. 5H. The latch circuit 217 may temporally store the data output from the sense amplifier 214. The latch circuit 217 includes two PMOS transistors 2901 and

2902 and two NMOS transistors 2903 and 2904. A trace 2905 connects the gates of the PMOS transistor 2902 and NMOS transistor 2904 and the drains of the PMOS transistor 2901 and NMOS transistor 2903. A trace 2906 connects the gates of the PMOS transistor 2901 and NMOS transistor 2903 and the drains of the PMOS transistor 2902 and NMOS transistor 2904. The latch circuit 217 may further include two NMOS transistors 2129 and 2130 having the gates connected to an address decoder 205 through metal traces 2181 and 2182 under the passivation layer 5, as shown in Fig. 5W. In a "READ" operation, the address decoder 205 receives an address data through multiple address buses 85 over the passivation layer 5. The address decoder 205 output READ ENABLE data (RE1 and RE2) to the gates of the NMOS transistors 2129 and 2130 through the traces 2181 and 2182 to control whether the NMOS transistors 2129 and 2130 are turned on or off, respectively. When the NMOS transistor 2129 is turned on, the initially amplified bit (bar) data output from the sense amplifier 214 can be transmitted to the trace 2905 through the channel of the NMOS transistor 2129. The trace 2905 latches the bit (bar) data and the trace 2906 latches the bit data. When the NMOS transistor 2130 is turned on, the bit data output from the trace 2906 of the latch circuit 217 can be transmitted to the data bus 83, 831 or 832 through the channel of the NMOS transistor 2130.

[00250] Referring to Fig. 5H, the node P of the voltage regulator or converter circuit 41 can be connected to the sources of the PMOS transistors 2116 and 2118 of the memory cell 215, the sources of the PMOS transistors 2112 and 2114 of the sense amplifier 214 and the sources of the PMOS transistors 2901 and 2902 of the latch circuit 217 through the previously described power plane, bus or trace 81, 811 or 812, as shown in Figs. 1B, 1C, 2B, 2C, 3B, 3C and 3D, over the passivation layer 5. The previously described power plane, bus or trace 81, 811 or 812 may contain a patterned circuit layer over the patterned circuit layers 831 and/or 832 of the thick and wide signal trace, bus or plane 83 as shown in Figs 7B-7D. Alternatively, the thick and wide signal trace, bus or plane 83 as shown in Figs 7B-7D may contain a patterned circuit layer over that of the previously described power plane, bus or trace 81. The node Rs of the voltage regulator or converter circuit 41 can be connected to the sources of the NMOS transistors 2115 and 2117 of the memory cell 215, the sources of the NMOS transistors 2111 and 2113 of the sense amplifier 214 and the sources of the NMOS transistors 2903 and 2904 of the latch circuit 217 through the previously described ground plane, bus or trace 82 or 821, as shown in Figs. 1C, 2C and 3C, over the passivation layer 5. The previously described ground plane, bus or trace 82 or 821 may contain a patterned circuit layer over the patterned circuit layers 831 and/or 832 of the thick and wide signal trace, bus or plane 83 as shown in

Figs 7B-7D. Alternatively, the thick and wide signal trace, bus or plane 83 as shown in Figs 7B-7D may contain a patterned circuit layer over that of the previously described ground plane, bus or trace 82.

[00251] However, the pass gate 216 in Fig. 5G or the latch circuit 217 in Fig. 5H does not provide large drive capability. To drive heavy load of the logic circuits 22, 23 and 24, or to transmit bit (bar) data output from the pass circuit 216 or bit data output from the latch circuit 217 to the logic circuits 22, 23 and 24 in a long distance, the internal circuit 21 may include the previously described internal driver 212 connected to the output node of the pass gate 216, as shown in Fig. 5I, or connected to the output node of the latch circuit 217, as shown in Fig. 5J, to amplify bit (bar) data output from the pass gate 216 or bit data output from the latch circuit 217. Referring to Fig.5I, the amplified bit (bar) data output from the internal driver 212 may be transmitted to the internal circuits 22, 23 and 24 through the data bus 83, 831 or 832 over the passivation layer 5, as shown in Figs. 5B, 6B, 7B, 7C and 7D. Referring to Fig.5J, the amplified bit data output from the internal driver 212 may be transmitted to the internal circuits 22, 23 and 24 through the data bus 83, 831 or 832 over the passivation layer 5, as shown in Figs. 5B, 6B, 7B, 7C and 7D.

[00252] Referring to Fig. 5I, the node P of the voltage regulator or converter circuit 41 can be connected to the sources of the PMOS transistors 2116 and 2118 of the memory cell 215, the sources of the PMOS transistors 2112 and 2114 of the sense amplifier 214 and the sources of the PMOS transistors 2104' and 2104 of the internal driver 212 through the previously described power plane, bus or trace 81, 811 or 812, as shown in Figs. 1B, 1C, 2B, 2C, 3B, 3C and 3D, over the passivation layer 5. The previously described power plane, bus or trace 81, 811 or 812 may contain a patterned circuit layer over the patterned circuit layers 831 and/or 832 of the thick and wide signal trace, bus or plane 83 as shown in Figs 7B-7D. Alternatively, the thick and wide signal trace, bus or plane 83 as shown in Figs 7B-7D may contain a patterned circuit layer over that of the previously described power plane, bus or trace 81. The node Rs of the voltage regulator or converter circuit 41 can be connected to the sources of the NMOS transistors 2115 and 2117 of the memory cell 215, the sources of the NMOS transistors 2111 and 2113 of the sense amplifier 214 and the sources of the NMOS transistors 2103' and 2103 of the driver circuit 212 through the previously described ground plane, bus or trace 82 or 821, as shown in Figs. 1C, 2C and 3C, over the passivation layer 5. The previously described ground plane, bus or trace 82 or 821 may contain a patterned circuit layer over the patterned circuit layers 831 and/or 832 of the thick and wide signal trace, bus or plane 83 as

shown in Figs 7B-7D. Alternatively, the thick and wide signal trace, bus or plane 83 as shown in Figs 7B-7D may contain a patterned circuit layer over that of the previously described ground plane, bus or trace 82.

[00253] Referring to Fig. 5J, the node P of the voltage regulator or converter circuit 41 can be connected to the sources of the PMOS transistors 2116 and 2118 of the memory cell 215, the sources of the PMOS transistors 2112 and 2114 of the sense amplifier 214, the sources of the PMOS transistors 2901 and 2902 of the latch circuit 217 and the sources of the PMOS transistors 2104' and 2104 of the internal driver 212 through the previously described power plane, bus or trace 81, 811 or 812, as shown in Figs. 1B, 1C, 2B, 2C, 3B, 3C and 3D, over the passivation layer 5. The previously described power plane, bus or trace 81, 811 or 812 may contain a patterned circuit layer over the patterned circuit layers 831 and/or 832 of the thick and wide signal trace, bus or plane 83 as shown in Figs 7B-7D. Alternatively, the thick and wide signal trace, bus or plane 83 as shown in Figs 7B-7D may contain a patterned circuit layer over that of the previously described power plane, bus or trace 81. The node Rs of the voltage regulator or converter circuit 41 can be connected to the sources of the NMOS transistors 2115 and 2117 of the memory cell 215, the sources of the NMOS transistors 2111 and 2113 of the sense amplifier 214, the sources of the NMOS transistors 2903 and 2904 of the latch circuit 217 and the sources of the NMOS transistors 2103' and 2103 of the internal driver 212 through the previously described ground plane, bus or trace 82 or 821, as shown in Figs. 1C, 2C and 3C, over the passivation layer 5. The previously described ground plane, bus or trace 82 or 821 may contain a patterned circuit layer over the patterned circuit layers 831 and/or 832 of the thick and wide signal trace, bus or plane 83 as shown in Figs 7B-7D. Alternatively, the thick and wide signal trace, bus or plane 83 as shown in Figs 7B-7D may contain a patterned circuit layer over that of the previously described ground plane, bus or trace 82.

[00254] Alternatively, referring to Fig. 5K, the output node Wo of the internal circuit 24 is connected to the input nodes Xi, Ui and Vi of the internal circuits 21, 22 and 23 through the thick metal plane, bus, trace or line 83' over the passivation layer 5. The internal circuit 24, such as NOR gate, may send a signal or data from the output node Wo thereof to the input node Xi' of the internal circuit 21, such as a receiver 212' shown in Fig. 5L, a tri-state input buffer 213' shown in Fig. 5M or other internal circuits, through a fine-line metal structure 634' under the passivation layer 5, then through an opening 534' in the passivation layer 5, then through the thick metal plane, line or trace 83' over the passivation layer 5, then through another opening 531' in the passivation layer 5, and then through a fine-line metal structure 631' under

the passivation layer 5. Besides, a signal or data output from the output node Wo of the internal circuit 24 may be also transmitted to the input node Ui of the internal circuit 22, such as NOR gate, through the fine-line metal structure 634' under the passivation layer 5, then through the opening 534' in the passivation layer 5, then through the thick metal plane, line or trace 83' over the passivation layer 5, then through another opening 532' in the passivation layer 5, then through the fine-line metal structures 632a' and 632b' under the passivation layer 5. Besides, a signal or data output from the output node Wo of the NOR gate 24 may be also transmitted to the input node Vi of the internal circuit 23, such as NAND gate, through the fine-line metal structure 634' under the passivation layer 5, then through the opening 534' in the passivation layer 5, then through the thick metal plane, line or trace 83' over the passivation layer 5, then through another opening 532' in the passivation layer 5, then through the fine-line metal structures 632a' and 632c' under the passivation layer 5.

[00255] The fine-line metal structures 634', 632' and 631' can be formed with stacked metal plugs, having a similar structure of the fine line metal structures 634, 632 and 631, respectively, as shown in 7B, 7C and 7D. The internal circuits 21, 22 and 23 may receive a signal output from the output node Wo of the internal circuit 24 at the input node Xi', Ui and Vi thereof, and may output a signal from the output node Xo', Uo and Vo thereof to other internal circuits through metal traces under the passivation layer 5.

[00256] The structure over the passivation layer 5 shown in Figs. 7B-7D, providing the previously described thick metal trace, line or plane 83, can also be applied to forming the thick metal trace, line or plane 83' illustrated in Fig. 5K. All combinations for the polymer layers 99, 98 and 95 and the circuit metal layers 831 and 832 illustrated in Figs. 7B-7D can be applied to the combinations for one or more polymer layers and one or more circuit metal layers over the passivation layer 5, illustrated in Fig. 5K.

[00257] In a case, the internal circuit 21 may be an internal receiver 212' as shown in Fig. 5L, or an internal input tri-state buffer 213' as shown in Fig. 5M. Referring to Figs. 5K and 5L, the internal receiver 212' may receive a signal passing through the thick metal trace or bus 83 over the passivation layer 5 and then may output an amplified signal from the output node Xo' thereof to other internal circuits but not to an external circuit through a metal trace under the passivation layer 5. Referring to Figs. 5K and 5M, the internal input tri-state buffer 213' may receive a signal passing through the thick metal trace or bus 83 over the passivation layer 5 and then may output an amplified signal from the output node Xo' thereof to other

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internal circuits but not to an external circuit through a metal trace under the passivation layer 5.

[00258] The internal receiver 212' in Fig. 5L has a similar circuit design to the internal driver 212 in Fig. 5D. In Figs. 5D and 5L, same reference numbers indicate same elements with same characteristics. The internal input tri-state buffer 213' in Fig. 5M has a similar circuit design to the internal output tri-state buffer 213 in Fig. 5E. In Figs. 5E and 5M, same reference numbers indicate same elements with same characteristics.

[00259] The output node Xo' of the internal receiver 212' or internal tri-state input buffer 213' is not connected to an external circuit but connected to an internal circuit under the passivation layer 5. The internal tri-state input buffer 213' provides amplifying capability and switch capability, and is particularly useful to amplify a data signal or an address signal having passed through the thick metal lines or traces 83' over the passivation layer 5 acting as data or address buses.

[00260] In Fig. 5K, a relatively large output current is required at the output node Xo' of the internal circuit 21 when a heavy load is demanded by an internal circuit connected to the output node Xo' of the internal circuit 21, or when the internal circuit 24 is far away from the internal circuit 21 in a distance of larger than 1 mm or of larger than 3mm. To provide a relatively large output current, the internal circuit 21 can be designed as an internal receiver 212' shown in Fig. 5L or an internal tri-state input buffer 213' shown in Fig. 5M.

[00261] Referring to Fig. 5K, a signal output from the internal circuit 24 can be transmitted to an n-channel MOS transistor of the internal circuit 21, and the n-channel MOS transistor may have a ratio of a physical channel width thereof to a physical channel length thereof ranging from, e.g., about 0.1 to 20, ranging from, e.g., about 0.1 to 10, or preferably ranging from, e.g., about 0.2 to 2. Alternatively, a signal output from the internal circuit 24 can be transmitted to a p-channel MOS transistor of the internal circuit 21, and the p-channel MOS transistor 2102 may have a ratio of a physical channel width thereof to a physical channel length thereof ranging from, e.g., about 0.2 to 40, ranging from, e.g., about 0.2 to 20, or preferably ranging from, e.g., about 0.4 to 4. In this application, the current level output from the internal circuit 24 and transmitted through the thick metal trace 83' over the passivation layer 5 is, for example, in a range of between 50 µA and 2 mA, and preferably of between 100 µA and 1 mA.

[00262] In Figs. 5L and 5M, the n-channel MOS transistors 2103, 2107 and 2107' may have a ratio of a physical channel width thereof to a physical channel length thereof ranging from, e.g., about 1.5 to 30, and preferably ranging from, e.g., about 2.5 to 10. The p-channel MOS transistors 2104, 2108 and 2108' may have a ratio of a physical channel width thereof to a physical channel length thereof ranging from, e.g., about 3 to 60, and preferably ranging from, e.g., about 5 to 20. In Fig. 5L, the n-channel MOS transistor 2103' may have a ratio of a physical channel width thereof to a physical channel length thereof ranging from, e.g., about 0.1 to 20, ranging from, e.g., about 0.1 to 10, or preferably ranging from, e.g., about 0.2 to 2, and the p-channel MOS transistor 2104' may have a ratio of a physical channel width thereof to a physical channel length thereof ranging from, e.g., about 0.2 to 40, ranging from, e.g., about 0.2 to 20, or preferably ranging from, e.g., about 0.4 to 4. Referring to Figs. 5K, 5L and 5M, the internal receiver 212 or internal tri-state input buffer 213 may receive a signal output from the output node Wo of the internal circuit 24 and transmitted through the thick metal trace or bus 83' over the passivation layer 5 but not to an external circuit. A current passing through the thick metal trace or line 83' over the passivation layer 5 and inputting the node Xi' of the internal circuit 21, provided by the internal driver 212 or internal tri-state buffer 213, may be between 500 μA and 10 mA, and preferably between 700 μA and 2 mA.

[00263] The concept shown in Fig. 5K can be applied to a memory chip, as illustrated in Figs. 5N-5R. The memory chip includes memory cells 215 and sense amplifiers 214 that can be referred to those illustrated in Fig. 5F. In Figs. 5F and 5N-5R, same reference numbers indicate same elements.

[00264] Referring to Fig. 5N, the previously described tri-state input buffer 213' is employed to be the internal circuit 21 shown in Figs. 5K and has an output node Xo' connected to the bit (bar) line 2172 and an input node Xi' connected to the internal circuits 22, 23 and 24, such as logic gates, through the above mentioned thick metal plane, bus or trace 83' over the passivation layer 5, and the internal circuit 24 may alternatively be NOR gate, NAND gate, AND gate, OR gate, operational amplifier, adder, multiplexer, diplexer, multiplier, A/D converter, D/A converter, CMOS transistor, bipolar CMOS transistor or bipolar circuit.

[00265] In this case, the memory cell 215 is a static random access memory (SRAM) cell. Alternatively, the memory cell 215 may be a dynamic random access memory (DRAM) cell, an erasable programmable read only memory (EPROM) cell, an electronic erasable programmable read only memory (EEPROM) cell, a flash memory cell, a read only memory

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(ROM) cell, or a magnetic random access memory (MRAM) cell, which is connected to the output node Wo of the logic gate 24 through a thick metal traces 83' over the passivation layer 5. A tri-state input buffer 213', pass gate 216', latch memory 217' or internal receiver 212', as shown in Figs. 5N-5R, may be optionally set on the path between any kind of the exampled memory cell 215 and the thick metal traces 83' over the passivation layer 5.

[00266] Referring to Fig. 5N, the node P of the voltage regulator or converter circuit 41 can be connected to the sources of the PMOS transistors 2116 and 2118 of the memory cell 215, the sources of the PMOS transistors 2112 and 2114 of the sense amplifier 214 and the source of the PMOS transistor 2108 of the tri-state input buffer 213' through the previously described power plane, bus or trace 81, 811 or 812, as shown in Figs. 1B, 1C, 2B, 2C, 3B, 3C and 3D, over the passivation layer 5. The previously described power plane, bus or trace 81, 811 or 812 may contain a patterned circuit layer over the patterned circuit layers 831 and/or 832 of the thick and wide signal trace, bus or plane 83 as shown in Figs 7B-7D. Alternatively, the thick and wide signal trace, bus or plane 83 as shown in Figs 7B-7D may contain a patterned circuit layer over that of the previously described power plane, bus or trace 81. The node Rs of the voltage regulator or converter circuit 41 can be connected to the sources of the NMOS transistors 2115 and 2117 of the memory cell 215, the sources of the NMOS transistors 2111 and 2113 of the sense amplifier 214 and the source of the NMOS transistor 2107 of the tri-state input buffer 213' through the previously described ground plane, bus or trace 82 or 821, as shown in Figs. 1C, 2C and 3C, over the passivation layer 5. The previously described ground plane, bus or trace 82 or 821 may contain a patterned circuit layer over the patterned circuit layers 831 and/or 832 of the thick and wide signal trace, bus or plane 83 as shown in Figs 7B-7D. Alternatively, the thick and wide signal trace, bus or plane 83 as shown in Figs 7B-7D may contain a patterned circuit layer over that of the previously described ground plane, bus or trace 82.

[00267] Referring to Fig. 5N, when the memory cell 215 is in a "WRITE" operation, a bit signal can be transmitted to the input node Xi' of the tri-state input buffer 213', that is, the gates of the PMOS transistors 2108 and the NMOS transistor 2107, through the thick metal line, trace or plane 83' over the passivation layer 5, from the output node Wo of the internal circuit 24. An amplified bit (bar) signal having a desirable waveform or voltage level can be output from the output node Xo' of the tri-state input buffer 213', that is, the source of the PMOS transistor 2108' or the source of the NMOS transistor 2107', to the bit (bar) line 2172. With the NMOS transistors 2122 and 2119 being turned on, the bit (bar) signal on the bit (bar)

line can be saved on the trace connecting the gates of the PMOS transistor 2118 and NMOS transistor 2117 and the sources of the PMOS transistor 2116 and NMOS transistor 2115, and the bit signal can be saved on the trace connecting the gates of the PMOS transistor 2116 and NMOS transistor 2115 and the sources of the PMOS transistor 2118 and NMOS transistor 2117.

[00268] In this case, the thick metal buses or traces 83' may be called as bit buses to transmit to-be-written bit data or bit (bar) data with 4 bits width, 8 bits width, 16 bits width, 32 bits width, 64 bits width, 128 bits width, 256 bits width, 512 bits width, 1024 bits width, 2048 bits width or 4096 bits width, output from the tri-state buffers 213. Accordingly, 4, 8, 16, 32, 64, 128, 256, 512, 1024, 2048 or 4098 bit buses arranged in parallel and over the passivation layer 5, may connect the input nodes Xi' of multiple internal circuits 21, the tri-state input buffers 213' in this case, to multiple output nodes of multiple internal circuits 24, such as NOR gates, NAND gates, AND gates, OR gates, operational amplifiers, adders, multiplexers, diplexers, multipliers, A/D converters, D/A converters, CMOS transistors, bipolar CMOS transistors or bipolar circuits.

[00269] Alternatively, multiple address buses 85 connecting an address decoder 205 and the outputs of multiple internal circuits 25 and 26 can be formed over the passivation layer 5, as shown in Fig. 5X, to transmit an address data from one of the internal circuits 25 and 26 to the address decoder 205 during a "WRITE" operation, and the internal circuits 25 and 26 may be NOR gate, NAND gate, AND gate, OR gate, operational amplifier, adder, multiplexer, diplexer, multiplier, A/D converter, D/A converter, CMOS transistor, bipolar CMOS transistor or bipolar circuit. The address decoder 205 is connected to multiple word lines coupled with multiple memory cells in a memory array. Referring to Figs. 5N and 5X, one of the word lines 2175 is connected to the gates of the NMOS transistors 2120 and 2119 of the memory cell 115, transmitting a signal from the address decoder 205 to the memory cell to control whether the logic level of bit data on the bit line 2171 is saved in the trace connecting the drains of the PMOS transistor 2118 and NMOS transistor 2117 and the gates of the PMOS transistor 2116 and NMOS transistor 2115 through the channel of the NMOS transistor 2120 and whether the logic level of bit (bar) data on the bit (bar) line 2172 is saved in the trace connecting the drains of the PMOS transistor 2116 and NMOS transistor 2115 and the gates of the PMOS transistor 2118 and NMOS transistor 2117 are transmitted to the bit line 2171 and the bit (bar) line 2172 through the channel of the NMOS transistor 2119. Two traces 2177' and 2178' connect the address decoder 205 and the tri-state input buffer 213', transmitting an ENABLE signal and an

ENABLE (bar) signal from the address decoder 205 to the tri-state input buffer 213' to control whether the amplified bit (bar) signal is output from the tri-state input buffer 213' to the bit (bar) line 2172.

[00270] Other embodiments as described below can be alternatively attained. Same reference numbers in this patent application indicate same or similar elements.

[00271] Referring to Figs. 5K, the internal circuit 21 may be a pass gate 216' as shown in Fig. 5O. The pass gate 216' may include an NMOS transistor 2124' having a gate connected to an address decoder 205 through a trace 2180' under the passivation layer 5, as shown in Fig. 5Y. In a "WRITE" operation, the address decoder 205 receives an address data through multiple address buses 85 over the passivation layer 5. The address decoder 205 output a WRITE ENABLE data to the gate of the NMOS transistor 2124' through the trace 2180' to control whether the NMOS transistor 2124' is turned on or off. When the NMOS transistor 2124' of the pass gate 216' is turned on, the bit data transmitted through the thick metal line, trace or plane 83' can be output from the pass gate 216' to the bit line 2171 through the channel of the NMOS transistor 2124'.

[00272] Referring to Figs. 5K, the internal circuit 21 may be a latch circuit 217' as shown in Fig. 5P. The latch circuit 217' may temporally store the data transmitted through the thick metal line, trace or plane 83'. The latch circuit 217' includes two PMOS transistors 2901' and 2902' and two NMOS transistors 2903' and 2904'. A trace 2905' connects the gates of the PMOS transistor 2902' and NMOS transistor 2904' and the drains of the PMOS transistor 2901' and NMOS transistor 2903'. A trace 2906' connects the gates of the PMOS transistor 2901' and NMOS transistor 2903' and the drains of the PMOS transistor 2902' and NMOS transistor 2904'. The latch circuit 217' may further include two NMOS transistors 2129' and 2130' having the gates connected to an address decoder 205 through metal traces 2181' and 2182' under the passivation layer 5, as shown in Fig. 5Z. In a "WRITE" operation, the address decoder 205 receives an address data output from the output nodes Ao or Bo of the internal circuit 25 or 26 through multiple address buses 85 over the passivation layer 5. The address decoder 205 output WRITE ENABLE data (WE1 and WE2) to the gates of the NMOS transistors 2129' and 2130' through the traces 2181' and 2182' to control whether the NMOS transistors 2129' and 2130' are turned on or off, respectively. When the NMOS transistor 2130' is turned on, the bit (bar) data output from the internal circuit 24 through the thick metal line, trace or plane 83', data bus, over the passivation layer 5 can be latched in the trace 2906'

through the channel of NMOS transistor 2130', and the bit data is latched in the trace 2905'. When the NMOS transistor 2129' is turned on, the bit data latched in the trace 2905' can be output to the bit line 2171 through the channel of the NMOS transistor 2129'.

[00273] Referring to Fig. 5P, the node P of the voltage regulator or converter circuit 41 can be connected to the sources of the PMOS transistors 2116 and 2118 of the memory cell 215, the sources of the PMOS transistors 2112 and 2114 of the sense amplifier 214 and the sources of the PMOS transistors 2901' and 2902' of the latch circuit 217 through the previously described power plane, bus or trace 81, 811 or 812, as shown in Figs. 1B, 1C, 2B, 2C, 3B, 3C and 3D, over the passivation layer 5. The previously described power plane, bus or trace 81, 811 or 812 may contain a patterned circuit layer over the patterned circuit layers 831 and/or 832 of the thick and wide signal trace, bus or plane 83 as shown in Figs 7B-7D. Alternatively, the thick and wide signal trace, bus or plane 83 as shown in Figs 7B-7D may contain a patterned circuit layer over that of the previously described power plane, bus or trace 81. The node Rs of the voltage regulator or converter circuit 41 can be connected to the sources of the NMOS transistors 2115 and 2117 of the memory cell 215, the sources of the NMOS transistors 2111 and 2113 of the sense amplifier 214 and the sources of the NMOS transistors 2903' and 2904' of the latch circuit 217 through the previously described ground plane, bus or trace 82 or 821, as shown in Figs. 1C, 2C and 3C, over the passivation layer 5. The previously described ground plane, bus or trace 82 or 821 may contain a patterned circuit layer over the patterned circuit layers 831 and/or 832 of the thick and wide signal trace, bus or plane 83 as shown in Figs 7B-7D. Alternatively, the thick and wide signal trace, bus or plane 83 as shown in Figs 7B-7D may contain a patterned circuit layer over that of the previously described ground plane, bus or trace 82.

[00274] However, the pass gate 216' in Fig. 5O or the latch circuit 217' in Fig. 5P may not provide the enough sensitivity to detect a weak voltage variation at the input node of the pass gate 216' or the latch circuit 217' in a "WRITE" operation. To amplify the voltage level of a signal transmitted through the thick metal line, trace or plane 83' in a long distance and output from the logic circuit 24, the internal circuit 21 may include the previously described internal receiver 212' connected to the input node of the pass gate 216', as shown in Fig. 5Q, or connected to the input node of the latch circuit 217', as shown in Fig. 5R, to amplify bit data inputting to the pass gate 216' or to the latch circuit 217'. Referring to Figs.5Q and 5R, the input node of the internal receiver 212' is connected to the output node Wo of the internal circuit 24 through the thick metal line, trace or plane 83' as shown in Fig. 5K.

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[00275] Referring to Fig. 5Q, the node P of the voltage regulator or converter circuit 41 can be connected to the sources of the PMOS transistors 2116 and 2118 of the memory cell 215, the sources of the PMOS transistors 2112 and 2114 of the sense amplifier 214 and the sources of the PMOS transistors 2104' and 2104 of the internal receiver 212' through the previously described power plane, bus or trace 81, 811 or 812, as shown in Figs. 1B, 1C, 2B, 2C, 3B, 3C and 3D, over the passivation layer 5. The previously described power plane, bus or trace 81, 811 or 812 may contain a patterned circuit layer over the patterned circuit layers 831 and/or 832 of the thick and wide signal trace, bus or plane 83 as shown in Figs 7B-7D. Alternatively, the thick and wide signal trace, bus or plane 83 as shown in Figs 7B-7D may contain a patterned circuit layer over that of the previously described power plane, bus or trace 81. The node Rs of the voltage regulator or converter circuit 41 can be connected to the sources of the NMOS transistors 2115 and 2117 of the memory cell 215, the sources of the NMOS transistors 2111 and 2113 of the sense amplifier 214 and the sources of the NMOS transistors 2103' and 2103 of the receiver circuit 212' through the previously described ground plane, bus or trace 82 or 821, as shown in Figs. 1C, 2C and 3C, over the passivation layer 5. The previously described ground plane, bus or trace 82 or 821 may contain a patterned circuit layer over the patterned circuit layers 831 and/or 832 of the thick and wide signal trace, bus or plane 83 as shown in Figs 7B-7D. Alternatively, the thick and wide signal trace, bus or plane 83 as shown in Figs 7B-7D may contain a patterned circuit layer over that of the previously described ground plane, bus or trace 82.

[00276] Referring to Fig. 5R, the node P of the voltage regulator or converter circuit 41 can be connected to the sources of the PMOS transistors 2116 and 2118 of the memory cell 215, the sources of the PMOS transistors 2112 and 2114 of the sense amplifier 214, the sources of the PMOS transistors 2901' and 2902' of the latch circuit 217' and the sources of the PMOS transistors 2104' and 2104 of the internal receiver 212' through the previously described power plane, bus or trace 81, 811 or 812, as shown in Figs. 1B, 1C, 2B, 2C, 3B, 3C and 3D, over the passivation layer 5. The previously described power plane, bus or trace 81, 811 or 812 may contain a patterned circuit layer over the patterned circuit layers 831 and/or 832 of the thick and wide signal trace, bus or plane 83 as shown in Figs 7B-7D. Alternatively, the thick and wide signal trace, bus or plane 83 as shown in Figs 7B-7D may contain a patterned circuit layer over that of the previously described power plane, bus or trace 81. The node Rs of the voltage regulator or converter circuit 41 can be connected to the sources of the NMOS transistors 2115 and 2117 of the memory cell 215, the sources of the NMOS transistors 2111 and 2113 of the

sense amplifier 214, the sources of the NMOS transistors 2903' and 2904' of the latch circuit 217' and the sources of the NMOS transistors 2103' and 2103 of the internal receiver 212' through the previously described ground plane, bus or trace 82 or 821, as shown in Figs. 1C, 2C and 3C, over the passivation layer 5. The previously described ground plane, bus or trace 82 or 821 may contain a patterned circuit layer over the patterned circuit layers 831 and/or 832 of the thick and wide signal trace, bus or plane 83 as shown in Figs 7B-7D. Alternatively, the thick and wide signal trace, bus or plane 83 as shown in Figs 7B-7D may contain a patterned circuit layer over that of the previously described ground plane, bus or trace 82.

[00277] Referring to Fig. 5S, another important application of the thick metal line, trace or plane 83 over the passivation layer 5 may be used to transport a precise analog signal. The thick metal line, trace or plane 83 has low resistance and capacitance per unit length characteristics and accordingly offers a low signal distortion of analog signals. Fig. 5S shows a circuit design with an over-passivation metal bus, trace or line 83 connecting multiple analog circuits 21, 22, 23 and 24. The design is similar to Fig. 5B except that the internal circuits 21, 22, 23 and 24 are analog circuits, or mixed-mode circuits including an analog circuit and a digital circuit. The thick metal bus, trace or line 83 over the passivation layer 5 connects the analog circuits 21, 22, 23 and 24. An analog signal output from the output node Yo of the analog circuit 21 can be transmitted to the input node Ui' of the internal circuit 22 through the fine-line metal structure 631 under the passivation layer 5, then through the thick metal bus, trace or plane 83 over the passivation layer 5, and then through the fine-line metal structures 632a and 632b under the passivation layer 5. An analog signal output from the output node Yo of the analog circuit 21 can be transmitted to the input node Vi' of the internal circuit 23 through the fine-line metal structure 631 under the passivation layer 5, then through the thick metal bus, trace or plane 83 over the passivation layer 5, and then through the fine-line metal structures 632a and 632c under the passivation layer 5. An analog signal output from the output node Yo of the analog circuit 21 can be transmitted to the input node Wi' of the internal circuit 24 through the fine-line metal structure 631 under the passivation layer 5, then through the thick metal bus, trace or plane 83 over the passivation layer 5, and then through the fine-line metal structure 634 under the passivation layer 5.

[00278] The analog circuits 21, 22, 23 and 24 can be an operational amplifier, amplifier, pre-amplifier, a power amplifier, an analog to digital (A/D) converter, a digital to analog (D/A) converter, a pulse reshaping circuit, a switched capacitor filter, a RC filter, or other kind of analog circuits. Fig. 5T shows a case where the internal circuit 21 in Fig. 5S is an operational

amplifier 218 with an output node Yo connected to the metal interconnection lines or traces 83 over the passivation layer 5. The operational amplifier 218 is designed based on a CMOS technology, referring to "CMOS Digital Circuit Technology" by M. Shoji, published by Prentice-Hall, Inc, New Jersey in 1987. Differential analog signals can be input into two input nodes Yi+ and Yi- of a differential circuit 219 provided in the operational amplifier 218 and with two n-MOS transistors 2125 and 2127 and two p-MOS transistors 2126 and 2128, and the input nodes Yi+ and Yi- are connected to the gates of the p-MOS transistors 2128 and 2126, respectively. The sources of the p-MOS transistors 2126 and 2128 are connected to a drain of a p-MOS transistor 2132 that is controlled by a voltage at the node 2138 determined by resistance of a resistor 2134. The output of the differential circuit 219 at the drains of the n-channel MOS transistor 2127 and the p-channel MOS transistor 2128 is connected to a gate of an n-channel MOS transistor 2135 and to a top electrode 21331 of the capacitor 2133. An output node Yo is at a bottom electrode 21332 of the capacitor 2133, at the drain of the n-channel MOS transistor 2135, and at a drain of the p-channel MOS transistor 2136. The p-MOS transistor 2136 is controlled by a voltage at the node 2138 determined by resistance of a resistor 2134. Accordingly, the voltage at the output node Yo is controlled by what degree the n-MOS transistor 2135 is turned on and by the output of the differential circuit 219. The capacitor 2133 are often used for an analog circuit, and are usually formed by a suitable process or processes, e.g., by a MOS capacitor (using the poly gate and the silicon substrate as two electrodes of the capacitor 2133), or a poly-to-poly capacitor (using a first poly silicon and a second poly silicon as two electrodes of the capacitor 2133). The capacitor 2133 may have a function to reduce a noise input from the input nodes Yi+ and Yi-. The resistor 2134 is also often used for an analog circuit, and is usually provided by an impurity-doped diffusion area with doping density of 10^{15}-10^{17}/cm^3, such as n well or p well, or of 10^{19}-10^{21}/cm^3, such as N$^+$ diffusion or P$^+$ diffusion, in the silicon substrate, and/or an impurity-doped poly silicon. The circuit shown in Fig. 5T can output a voltage Yo proportionally amplifying the differential value of the input voltages Yi+ and Yi-.

[00279] The thick metal bus, trace or plane 83 and 83' illustrated in Figs. 5B-5Z can be realized by forming the circuit metal layers 831 and/or 832 and the polymer layers 95, 98 and/or 99 shown in Figs 7B-7D, or by forming the circuit metal layers 801 and/or 802 and the polymer layers 95, 97, 98 and/or 99 shown in Figs 15A-21K.

[00280] In Figs. 5B, 5K, 5S, 7B, 7C and 7D, the thick metal trace, bus or plane 83 over the passivation layer 5 can be used to transport signals input to or output from the internal

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circuits 21, 22, 23 or 24. In Figs. 5K, 5S, 5U and 5V-5Z, a dotted line 5 indicates the passivation layer, coarse traces indicate traces of the over-passivation scheme 102 formed over the passivation layer 5, and fine traces indicate traces formed under the passivation layer 5.

Third Embodiment: Complete Architecture

[00281] Schemes or technology for forming coarse metal conductors, according to the present disclosure, can provide other advantages for IC chip. For example, the metal trace, bus or plane 83 or 83' over the passivation layer 5 may include gold, copper, silver, palladium, rhodium, platinum, ruthenium, nickel, aluminum or solder; various kinds of contacting structures, such as solder bumps, solder pads, solder balls, gold bumps, gold pads, Pd pads, aluminum pads or wire bonding pads, can be formed on the metal trace, bus or plane 83 to connect the IC chip to an external circuit easily. An IC chip may be connected to and communicated with an external circuit. When a signal is transmitted to external circuits or components, some off-chip circuitry is required to (1) drive the large current load of external circuits, parasitics or components, (2) detect noisy signals from the external circuits or components, and (3) prevent the internal circuits from being damaged by the surge electrical stimulus from external circuits or components.

[00282] Figs. 8B, 9B and 10B depict a schematic architecture according to a third exemplary embodiment of the present disclosure. Fig. 8B shows a circuit diagram according to the third exemplary embodiment of the present disclosure. Fig. 9B shows a top view realizing the circuit diagram of Fig. 8B. Fig. 10B shows a cross-sectional view realizing the circuit diagram of Fig. 8B.

[00283] Referring to Figs. 8B, 9B and 10B, an off-chip buffer 42 is connected to the output node Xo of the internal circuit 21 and to the input nodes Ui, Vi and Wi of the internal circuits 22, 23 and 24 through the metal trace, bus or plane 83. A metal bump 89 for being connected to an external circuit, such as printed circuit board, ball-grid-array (BGA) substrate, flexible substrate, semiconductor chip, metal substrate, glass substrate or ceramic substrate, may be formed on a contact point 8310 of the redistributed metal trace 83r. The contact point 8310 can be connected to the original pad 6390 exposed by an opening 539 in the passivation layer 5 through the redistributed metal trace 83r, and the position of the contact point 8310 from a top perspective view is different from that of the original pad 6390. The original pad 6390 is connected to the off-chip buffer 42 and to the off-chip ESD circuit 43. A signal may be

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transmitted from the internal circuit 21 to an external circuit through the thick metal bus, trace or plane 83, then through the off-chip buffer 42, and then through the thick metal bus, trace or plane 83r; a signal may be transmitted from an external circuit to the internal circuits 22, 23 and/or 24 through the thick metal traces, buses or plane 83r, through the off-chip buffer 42 and then through the thick metal bus, trace or plane 83; a signal may be transmitted from the internal circuit 21 to the internal circuits 22, 23 and/or 24 through the thick metal bus, trace or plane 83. The total length of the metal trace 83 over the passivation layer 5, connecting the off-chip buffer 42 to the internal circuit 24, can be between 250 micrometers and 2.5 millimeters, preferably between 500 and 1 millimeter, and preferably between 1000 and 8000 micrometers.

[00284] The shape of the openings 531, 532, 534 and 539' from a top perspective view may be round, square, rectangular or polygon. If the openings 531, 532, 534 and 539' are round, the openings 531, 532 and 534 may have a diameter of between 0.1 and 200 microns, between 1 and 100 microns, or, preferably, between 0.1 and 30 microns. If the openings 531, 532 and 534 are square, the openings 531, 532 and 534 may have a width of between 0.1 and 200 microns, between 1 and 100 microns, or, preferably, between 0.1 and 30 microns. If the openings 531, 532 and 534 are rectangular, the openings 531, 532 and 534 may have a width of between 0.1 and 200 microns, between 1 and 100 microns, or, preferably, between 0.1 and 30 microns, and a length of between 1 micron and 1 centimeter. If the openings 531, 532 and 534 are polygon having more than five sides, the openings 531, 532 and 534 have a largest diagonal length of between 0.1 and 200 microns, between 1 and 100 microns, or, preferably, between 0.1 and 30 microns. Alternatively, the openings 531, 532 and 534 have a largest transverse dimension of between 0.1 and 200 microns, between 1 and 100 microns, or, preferably, between 0.1 and 30 microns. In a case, the openings 531, 532 and 534 have a width of between 0.1 and 30 microns, with the lower portion of the openings 9531, 9532 and 9514 in the polymer layer 95 having a width of between 20 and 100 microns.

[00285] Alternatively, referring to Fig. 8C, the element 42 may be an off-chip receiver. The off-chip receiver 42 is connected to the input nodes of the internal circuits 21, 22, 23 and 24 through the thick metal bus, trace or plane 83.

[00286] Alternatively, referring to Fig. 8G, the element 42 may be an off-chip driver. The off-chip driver 42 is connected only to the output nodes of the internal circuits 21, 22, 23 and 24 through the thick metal bus, trace or plane 83.

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[00287] Figs. 8B and 8C show a simplified circuit diagram where a thick metal trace 83 over a passivation layer 5 connects an off-chip buffer 42, such as external driver or external receiver, and internal circuits 21, 22, 23 and 24. Fig. 9B shows a top view of a semiconductor chip realizing the circuitry shown in Figs. 8B and 8C, and coarse traces 83 and 83r shown in Fig. 9B mean the traces formed over the passivation layer 5, and fine traces 69, 632a, 632b and 632c shown in Fig. 9B mean the traces formed under the passivation layer 5. Fig. 10B shows a cross-sectional view of a semiconductor chip realizing the circuitry shown in Figs. 8B and 8C. Fig. 9B shows a top view of the semiconductor chip shown in Fig. 10B. Figs. 8B, 9B, 10B, 10C, 10D and 10E show the circuitry architecture of the disclosure using the two hierarchies of the fine-line IC metal structures 639, 639', 631, 632, 634 and 69 under the passivation layer 5 and the coarse metal traces 83, 831, 832 and 83r over the passivation layer 5, with the consideration of whole chip design of the internal and external circuit connection.

[00288] Referring to Figs. 8B, 9B and 10B, the internal circuit 21 may output a signal to other internal circuits 22, 23 and 24 through the thick metal bus, trace or plane 83 over the passivation layer 5, as described in Figs. 5B-5J and 5S-5T, and, besides, the internal circuit 21 may output a signal to an external circuit through, in sequence, the fine-line metal trace 631 under the passivation layer 5, the thick metal trace 83 over the passivation layer 5, the fine-line metal trace 639' under the passivation layer 5, the off-chip buffer 42, such as external driver, the fine-line metal trace 69 under the passivation layer 5, the redistributed trace 83r over the passivation layer 5 and the metal bump 89 on the redistributed trace 83r.

[00289] Referring to Fig. 8C, 9B and 10B, a signal output from the internal circuit 24 may be transmitted to the internal circuit 21 through the thick metal bus, trace or plane 83' over the passivation layer 5, as described in Figs. 5K-5R, and, besides, a signal output from an external circuit may be transmitted to the internal circuit 21 through the metal bump 89, the redistributed trace 83r, the fine-line metal trace 69 under the passivation layer 5, the off-chip buffer 42, such as external receiver, the fine-line metal trace 639' under the passivation layer 5, the thick metal bus, trace or plane 83' over the passivation layer 5 and the fine-line metal trace 631' under the passivation layer 5. A signal output from the internal circuit 24 may be transmitted to the internal circuit 22 through the thick metal bus, trace or plane 83' over the passivation layer 5, as described in Figs. 5K-5R, and, besides, a signal output from an external circuit may be transmitted to the internal circuit 22 through the metal bump 89, the redistributed trace 83r, the fine-line metal trace 69 under the passivation layer 5, the off-chip buffer 42, such as external receiver, the fine-line metal trace 639' under the passivation layer 5,

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the thick metal bus, trace or plane 83' over the passivation layer 5, the fine-line metal trace 632a' and 632b' under the passivation layer 5. A signal output from the internal circuit 24 may be transmitted to the internal circuit 23 through the thick metal bus, trace or plane 83' over the passivation layer 5, as described in Figs. 5K-5R, and, besides, a signal output from an external circuit may be transmitted to the internal circuit 23 through the metal bump 89, the redistributed trace 83r, the fine-line metal trace 69 under the passivation layer 5, the off-chip buffer 42, such as external receiver, the fine-line metal trace 639' under the passivation layer 5, the thick metal bus, trace or plane 83' over the passivation layer 5, the fine-line metal trace 632a' and 632c' under the passivation layer 5.

[00290] In this embodiment, referring to Figs. 8B and 8C, a signal transmitted through the thick metal bus, trace or plane 83 or 83' over the passivation layer 5 in the internal scheme 200 can be transmitted to or from the external circuit (not shown) through an off-chip circuit 40 including an off-chip buffer 42, such as external driver or receiver, and an off-chip ESD (electro static discharge) circuit 43. The off-chip ESD circuit 43 is connected in parallel with the off-chip buffer 42 through the trace 69 under the passivation layer 5. The redistributed metal trace 83r can be used for redistribution of the IC fine-line metal (I/O) pads 6390 in Fig. 10B, relocated to a different location, for example an over-passivation metal pads 8310 in Fig. 10B, resulting in readily being connected to an external circuit, such as another semiconductor chip, ball-grid-array (BGA) substrate or ceramic substrate through the metal bump 89 or through a wirebonded wire bonded onto the pad 8310, to a flexible substrate through the metal bump 89 preferably including a gold layer having a thickness between 7 and 25 micrometers using a gold-to-gold bonding technology or using a gold-to-tin bonding technology, or to a glass substrate through the metal bump 89 preferably including a gold layer having a thickness between 7 and 25 micrometers via an anisotropic conductive film (ACF) or anisotropic conductive paste ACP. The redistributed metal line, trace or plane 83r can be formed during forming the over-passivation interconnection scheme 83.

[00291] Referring to Fig. 11F, the off-chip circuitry 40, in Figs. 8B and 8C, for being connected to the external circuitry may include an off-chip ESD circuit 43, composed of two diodes 4331 and 4332, and an off-chip buffer 42.

[00292] In a first aspect, the off-chip buffer 42 may be an off-chip driver 421, as shown in Fig. 11A, in application to the circuit architecture shown in Fig. 8B, having an input node F connected to the internal circuits 20 through the thick and wide circuit trace 83, and an output

node E connected, in parallel with the off-chip ESD circuit 43, to the metal bump 89. Fig. 11A shows an example of a two-stage cascade off-chip driver 421, CMOS cascade driver. The cascade driver may include several stages of inverters. The off-chip driver 421 may include two inverters 421' and 421", and the inverter 421' is composed of an NMOS device 4201 and a PMOS device 4202, and the inverter 421" is composed of an NMOS device 4203 and a PMOS device 4204. The gates of the PMOS device 4202 and the NMOS device 4201 serve as the input node F, and the drains of the PMOS device 4204 and the NMOS device 4203 serve as the output node E. The drains of the PMOS device 4202 and the NMOS device 4201 are connected to the gates of the PMOS device 4204 and the NMOS device 4203.

[00293] Referring to Fig. 11A, the previously described power plane, bus or trace 81, 811 or 812, as shown in Figs. 1B, 1C, 2B, 2C, 3B, 3C and 3D, over the passivation layer 5 can connect the node P of the voltage regulator or converter circuit 41 and the sources of the PMOS devices 4202 and 4204. The previously described power plane, bus or trace 81, 811 or 812 may contain a patterned circuit layer over the patterned circuit layers 831 and/or 832 of the thick and wide signal trace, bus or plane 83 as shown in Figs 10B-10D and 10G. Alternatively, the thick and wide signal trace, bus or plane 83 as shown in Figs 10B-10D and 10G may contain a patterned circuit layer over that of the previously described power plane, bus or trace 81. The previously described ground plane, bus or trace 82 or 821, as shown in Figs. 1C, 2C and 3C, over the passivation layer 5 can connect the node Rs of the voltage regulator or converter circuit 41 and the sources of the NMOS devices 4201 and 4203. The previously described ground plane, bus or trace 82 or 821 may contain a patterned circuit layer over the patterned circuit layers 831 and/or 832 of the thick and wide signal trace, bus or plane 83 as shown in Figs 10B-10E and 10G. Alternatively, the thick and wide signal trace, bus or plane 83 as shown in Figs 10B-10E and 10G may contain a patterned circuit layer over that of the previously described ground plane, bus or trace 82.

[00294] The first stage 421'of the off-chip driver in Fig. 11A is an inverter with the NMOS device 4201 having a ratio of a physical channel width thereof to a physical channel length thereof larger than those of all NMOS devices in the internal circuits 20 connected to the input node F of the off-chip driver 421, and with the PMOS device 4202 having a ratio of a physical channel width thereof to a physical channel length thereof larger than those of all PMOS devices in the internal circuits 20 connected to the input node F of the off-chip driver 421. The NMOS transistor 4203 may have a ratio of a physical channel width thereof to a physical channel length thereof ranging from, e.g., about 20 to 20,000, and preferably ranging

from, e.g., about 30 to 300. The PMOS transistor 4204 may have a ratio of a physical channel width thereof to a physical channel length thereof ranging from, e.g., about 40 to 40,000, and preferably ranging from, e.g., about 60 to 600. The output current of an off-chip driver 421 is proportional to the number of stages and the size (W/L, MOS transistor's channel width to length ratio, more precisely, the MOS effective channel width to effective channel length ratio) of transistors used in each stage of the off-chip driver. The off-chip driver 421 may output a driving current of between 5 mA and 5 A and, preferably, between 10 mA and 100 mA.

[00295] Provided that the off-chip driver 421 shown in Fig. 11A is applied to the circuit architecture shown in Fig. 8B for a power management chip, the NMOS transistor 4203 of the off-chip driver 421 may have a ratio of a physical channel width thereof to a physical channel length thereof ranging from, e.g., about 2,000 to 200,000, and preferably ranging from, e.g., about 2,000 to 20,000. The PMOS transistor 4204 may have a ratio of a physical channel width thereof to a physical channel length thereof ranging from, e.g., about 4,000 to 400,000, and preferably ranging from, e.g., about 4,000 to 40,000. The off-chip driver 421 may output a driving current of between 500 mA and 50 A and, preferably, between 500 mA and 5 A.

[00296] In a second aspect, the off-chip buffer 42 may be an off-chip receiver 422, as shown in Fig. 11B, in application to the circuit architecture shown in Fig. 8C, having an output node F connected to the internal circuits 21, 22 and 23 through the thick and wide circuit trace 83, and an input node E connected, in parallel with the off-chip ESD circuit 43, to the metal bump 89. Fig. 11B shows an example of a two-stage cascade off-chip receiver 422, CMOS cascade receiver. The off-chip receiver 422 may receive a signal from an external circuitry through the metal bump 89 and output an amplified signal to the internal circuits 21, 22 and 23 through the thick and wide trace or bus 83'. The first stage 422', close to the external circuitry, of the off-chip receiver 422 is an inverter having an NMOS device 4205 and a PMOS device 4206 with a size designed to detect a noisy external signal. The first stage receives a noisy signal at point E from the external circuits or components, such as signal from another chip. The second stage 422" of the off-chip receiver 422 is also an inverter except that it is formed by a suitable process or processes, e.g., by a larger size of NMOS device 4207 and PMOS device 4208. The second stage of the inverter is used to restore the integrity of the noisy external signal for the internal circuit. The gates of the PMOS device 4205 and the NMOS device 4206 serve as the input node E, and the drains of the PMOS device 4208 and the NMOS device 4207 serve as the output node F. The drains of the PMOS device 4206 and the NMOS device 4205 are connected to the gates of the PMOS device 4208 and the NMOS device 4207.

[00297] Referring to Fig. 11B, the previously described power plane, bus or trace 81, 811 or 812, as shown in Figs. 1B, 1C, 2B, 2C, 3B, 3C and 3D, over the passivation layer 5 can connect the node P of the voltage regulator or converter circuit 41 and the sources of the PMOS devices 4206 and 4208. The previously described power plane, bus or trace 81, 811 or 812 may contain a patterned circuit layer over the patterned circuit layers 831 and/or 832 of the thick and wide signal trace, bus or plane 83 as shown in Figs 10B-10D and 10G. Alternatively, the thick and wide signal trace, bus or plane 83 as shown in Figs 10B-10D and 10G may contain a patterned circuit layer over that of the previously described power plane, bus or trace 81. The previously described ground plane, bus or trace 82 or 821, as shown in Figs. 1C, 2C and 3C, over the passivation layer 5 can connect the node Rs of the voltage regulator or converter circuit 41 and the sources of the NMOS devices 4205 and 4207. The previously described ground plane, bus or trace 82 or 821 may contain a patterned circuit layer over the patterned circuit layers 831 and/or 832 of the thick and wide signal trace, bus or plane 83 as shown in Figs 10B-10E and 10G. Alternatively, the thick and wide signal trace, bus or plane 83 as shown in Figs 10B-10E and 10G may contain a patterned circuit layer over that of the previously described ground plane, bus or trace 82.

[00298] The first stage 422'of the off-chip receiver in Fig. 11B is an inverter with the NMOS device 4205 having a ratio of a physical channel width thereof to a physical channel length thereof larger than those of all NMOS devices in the internal circuits 20 connected to the output node F of the off-chip receiver 422, and with the PMOS device 4206 having a ratio of a physical channel width thereof to a physical channel length thereof larger than those of all PMOS devices in the internal circuits 20 connected to the output node F of the off-chip receiver 422. The NMOS transistor 4207 may have a ratio of a physical channel width thereof to a physical channel length thereof ranging from, e.g., about 10 to 20,000, and preferably ranging from, e.g., about 10 to 300. The PMOS transistor 4208 may have a ratio of a physical channel width thereof to a physical channel length thereof ranging from, e.g., about 20 to 40,000, and preferably ranging from, e.g., about 20 to 600. The off-chip receiver 422 may output a driving current of between 2 mA and 5 A and, preferably, between 3 mA and 100 mA.

[00299] Provided that the off-chip receiver 422 shown in Fig. 11B is applied to the circuit architecture shown in Fig. 8C for a power management chip, the NMOS transistor 4207 of the off-chip receiver 422 may have a ratio of a physical channel width thereof to a physical channel length thereof ranging from, e.g., about 10 to 20,000, and preferably ranging from, e.g., about 10 to 300. The PMOS transistor 4208 may have a ratio of a physical channel width

thereof to a physical channel length thereof ranging from, e.g., about 20 to 40,000, and preferably ranging from, e.g., about 20 to 600. The off-chip receiver 422 may output a driving current of between 150 mA and 50 A and, preferably, between 150 mA and 5 A.

[00300] In a third aspect, the off-chip buffer 42 may be a tri-state buffer 423, as shown in Fig. 11C, in application to the circuit architecture shown in Fig. 8B, having an input node F connected to the internal circuits 20 through the thick and wide circuit trace 83, and an output node E, in parallel with the off-chip ESD circuit 43, connected to the metal bump 89. Fig. 11C shows an example of an off-chip tri-state buffer 423; as an off-chip driver, a common design in IC chips to allow multiple logic gates to drive the same output, such as a bus. The tri-state buffer 423, serving as an off-chip driver, may include two PMOS devices 4210 and 4212 and two NMOS devices 4209 and 4211. The gates of the PMOS device 4210 and the NMOS device 4209 serve as the input node F, and the drains of the PMOS device 4212 and the NMOS device 4211 serve as the output node E. The drain of the PMOS device 4210 is connected to the source of the PMOS device 4212. The drain of the NMOS device 4209 is connected to the source of the NMOS device 4211. The tri-state buffer 423 may have a switch function controlled by an Enable signal transmitted to the gate of the NMOS device 4211 and an Enable(bar) signal transmitted to the gate of the PMOS device 4212. The off-chip tri-state buffer in Fig. 11C can be viewed as a gated inverter. When the enabling signal En is high ($\overline{En}$ is low), the off-chip tri-state buffer outputs a signal to an external circuit. When the signal En is set at low ($\overline{En}$ is high), no signal will be output to an external circuit. The off-chip tri-state buffer 423 is set to drive the external data bus.

[00301] Referring to Fig. 11C, the previously described power plane, bus or trace 81, 811 or 812, as shown in Figs. 1B, 1C, 2B, 2C, 3B, 3C and 3D, over the passivation layer 5 can connect the node P of the voltage regulator or converter circuit 41 and the source of the PMOS device 4210. The previously described power plane, bus or trace 81, 811 or 812 may contain a patterned circuit layer over the patterned circuit layers 831 and/or 832 of the thick and wide signal trace, bus or plane 83 as shown in Figs 10B-10D and 10G. Alternatively, the thick and wide signal trace, bus or plane 83 as shown in Figs 10B-10D and 10G may contain a patterned circuit layer over that of the previously described power plane, bus or trace 81. The previously described ground plane, bus or trace 82 or 821, as shown in Figs. 1C, 2C and 3C, over the passivation layer 5 can connect the node Rs of the voltage regulator or converter circuit 41 and the source of the NMOS device 4209. The previously described ground plane, bus or trace 82

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or 821 may contain a patterned circuit layer over the patterned circuit layers 831 and/or 832 of the thick and wide signal trace, bus or plane 83 as shown in Figs 10B-10E and 10G. Alternatively, the thick and wide signal trace, bus or plane 83 as shown in Figs 10B-10E and 10G may contain a patterned circuit layer over that of the previously described ground plane, bus or trace 82.

[00302] The NMOS transistors 4209 and 4211 may have a ratio of a physical channel width thereof to a physical channel length thereof ranging from, e.g., about 20 to 20,000, and preferably ranging from, e.g., about 30 to 300. The PMOS transistors 4210 and 4212 may have a ratio of a physical channel width thereof to a physical channel length thereof ranging from, e.g., about 40 to 40,000, and preferably ranging from, e.g., about 60 to 600. The tri-state buffer 423 may output a driving current of between 5 mA and 5 A and, preferably, between 10 mA and 100 mA.

[00303] Provided that the tri-state buffer 423 shown in Fig. 11A is applied to the circuit architecture shown in Fig. 8B for a power management chip, the NMOS transistors 4209 and 4211 of the tri-state buffer 423 may have a ratio of a physical channel width thereof to a physical channel length thereof ranging from, e.g., about 2,000 to 200,000, and preferably ranging from, e.g., about 2,000 to 20,000. The PMOS transistors 4210 and 4212 may have a ratio of a physical channel width thereof to a physical channel length thereof ranging from, e.g., about 4,000 to 400,000, and preferably ranging from, e.g., about 4,000 to 40,000. The tri-state buffer 423 may output a driving current of between 500 mA and 50 A and, preferably, between 500 mA and 5 A.

[00304] In a fourth aspect, the off-chip buffer 42 may be a tri-state buffer 423, as shown in Fig. 11E, in application to the circuit architecture shown in Fig. 8C, having an output node F connected to the internal circuits 21, 22 and 23 through the thick and wide circuit trace 83', and an input node E, in parallel with the off-chip ESD circuit 43, connected to the metal bump 89. Fig. 11E shows an example of an off-chip tri-state buffer 423, as an off-chip receiver. The tri-state buffer 423, serving as an off-chip receiver, may include two PMOS devices 4210 and 4212 and two NMOS devices 4209 and 4211. The gates of the PMOS device 4210 and the NMOS device 4209 serve as the input node E, and the drains of the PMOS device 4212 and the NMOS device 4211 serve as the output node F. The drain of the PMOS device 4210 is connected to the source of the PMOS device 4212. The drain of the NMOS device 4209 is connected to the source of the NMOS device 4211. The tri-state buffer 423 may have a switch

function controlled by an Enable signal transmitted to the gate of the NMOS device 4211 and an Enable(bar) signal transmitted to the gate of the PMOS device 4212. When the enabling signal En is high ($\overline{En}$ is low), the off-chip tri-state buffer outputs a signal to the internal circuits 20. When the signal En is set at low ($\overline{En}$ is high), no signal will be output to the internal circuits 20.

[00305] Referring to Fig. 11E, the previously described power plane, bus or trace 81, 811 or 812, as shown in Figs. 1B, 1C, 2B, 2C, 3B, 3C and 3D, over the passivation layer 5 can connect the node P of the voltage regulator or converter circuit 41 and the source of the PMOS device 4210. The previously described power plane, bus or trace 81, 811 or 812 may contain a patterned circuit layer over the patterned circuit layers 831 and/or 832 of the thick and wide signal trace, bus or plane 83 as shown in Figs 10B-10D and 10G. Alternatively, the thick and wide signal trace, bus or plane 83 as shown in Figs 10B-10D and 10G may contain a patterned circuit layer over that of the previously described power plane, bus or trace 81. The previously described ground plane, bus or trace 82 or 821, as shown in Figs. 1C, 2C and 3C, over the passivation layer 5 can connect the node Rs of the voltage regulator or converter circuit 41 and the source of the NMOS device 4209. The previously described ground plane, bus or trace 82 or 821 may contain a patterned circuit layer over the patterned circuit layers 831 and/or 832 of the thick and wide signal trace, bus or plane 83 as shown in Figs 10B-10E and 10G. Alternatively, the thick and wide signal trace, bus or plane 83 as shown in Figs 10B-10E and 10G may contain a patterned circuit layer over that of the previously described ground plane, bus or trace 82.

[00306] The NMOS transistors 4209 and 4211 may have a ratio of a physical channel width thereof to a physical channel length thereof ranging from, e.g., about 20 to 20,000, and preferably ranging from, e.g., about 30 to 300. The PMOS transistors 4210 and 4212 may have a ratio of a physical channel width thereof to a physical channel length thereof ranging from, e.g., about 40 to 40,000, and preferably ranging from, e.g., about 60 to 600. The tri-state buffer 423 may output a driving current of between 5 mA and 5 A and, preferably, between 10 mA and 100 mA.

[00307] Provided that the tri-state buffer 423 shown in Fig. 11E is applied to the circuit architecture shown in Fig. 8C for a power management chip, the NMOS transistors 4209 and 4211 of the tri-state buffer 423 may have a ratio of a physical channel width thereof to a physical channel length thereof ranging from, e.g., about 2,000 to 200,000, and preferably

ranging from, e.g., about 2,000 to 20,000. The PMOS transistors 4210 and 4212 may have a ratio of a physical channel width thereof to a physical channel length thereof ranging from, e.g., about 4,000 to 400,000, and preferably ranging from, e.g., about 4,000 to 40,000. The tri-state buffer 423 may output a driving current of between 500 mA and 50 A and, preferably, between 500 mA and 5 A.

[00308] There may be various off-chip input and output buffers. The above examples are for the CMOS level signals. If the external signal is a transistor-transistor logic (TTL) level, a CMOS/TTL buffer is required. If the external signal is an emitter coupled logic (ECL) level, a CMOS/ECL interface buffer is required. One or more stages of inverters can be added between the internal circuits 20 and the off-chip tri-state buffer 423 serving as an off-chip driver as shown in Fig. 11C or as an off-chip receiver as shown in Fig. 11E.

[00309] In a fifth aspect, the off-chip buffer 42 may be an off-chip driver 421 composed of a first level of inverter 421' and a second level of inverters 421", as shown in Fig. 11D, in application to the circuit architecture shown in Fig. 8B, and the first level of inverter 421' is connected in series to the second level of inverters 421", and the second level of inverters 421" are connected in parallel with one another to the first level of inverter 421'. Fig. 8E shows a circuit diagram with the off-driver 421 of Fig. 11D applied to the circuit architecture shown in Fig. 8C. Fig. 9C shows a top perspective view realizing the circuit diagram of Fig. 8E. Fig. 10H shows a chip structure realizing the circuit diagram of Fig. 8E. The off-chip driver 421 has an input node F connected to the internal circuits 20 through the thick and wide circuit trace 83, and an output node E connected, in parallel with the off-chip ESD circuit 43, to the metal bump 89. The gates of the PMOS device and the NMOS device in the first level of inverter 421' serve as the input node F, and the drains of the PMOS devices and the NMOS devices in the second level of inverters 421" serve as the output node E. The drains of the PMOS device and the NMOS device in the first level of inverter 421' are connected to the gates of the PMOS devices and the NMOS devices in the second level of inverters 421" through a thick and wide metal trace or bus 83s over the passivation layer 5. The drains of the PMOS devices and the NMOS devices in the second level of inverters 421" are connected to the metal bump 89 through a thick and wide metal trace or bus 83r over the passivation layer 5. A patterned circuit layer 831 formed on the polymer layer 95, such as polyimide, having a thickness of between 2 and 30 micrometers may be composed of the thick and wide metal traces or buses 83r, 83s and 83, that is, the thick and wide metal traces or buses 83r, 83s and 83 may be formed at the same time, as shown in Fig. 10H.

[00310] Alternatively, multiple patterned circuit layers and multiple polymer layers may be formed over the passivation layer 5, one of the polymer layers is between neighboring two of the patterned circuit layers. The thick and wide metal traces or buses 83s may be formed in the lower one of the patterned circuit layers, and the thick and wide metal traces or buses 83s may be formed in the upper one of the patterned circuit layers and over the thick and wide metal traces or buses 83s. The thick and wide metal traces or buses 83 may have a portion in the lower one of the patterned circuit layers and another portion in the upper one of the patterned circuit layers.

[00311] Referring to Fig. 11D, the previously described power plane, bus or trace 81, 811 or 812, as shown in Figs. 1B, 1C, 2B, 2C, 3B, 3C and 3D, over the passivation layer 5 can connect the node P of the voltage regulator or converter circuit 41 to the source of the PMOS device in the first level of inverter 421' and to the sources of the PMOS devices in the second level of inverter 421". The previously described power plane, bus or trace 81, 811 or 812 may contain a patterned circuit layer over the patterned circuit layer 831 of the thick and wide signal trace, bus or plane 83 as shown in Fig. 10H. Alternatively, the thick and wide signal trace, bus or plane 83 as shown in Fig. 10H may contain a patterned circuit layer over that of the previously described power plane, bus or trace 81. The previously described ground plane, bus or trace 82 or 821, as shown in Figs. 1C, 2C and 3C, over the passivation layer 5 can connect the node Rs of the voltage regulator or converter circuit 41, the source of the NMOS device in the first level of inverter 421', and the sources of the NMOS devices in the second level of inverters 421". The previously described ground plane, bus or trace 82 or 821 may contain a patterned circuit layer over the patterned circuit layer 831 of the thick and wide signal trace, bus or plane 83 as shown in Fig 10H. Alternatively, the thick and wide signal trace, bus or plane 83 as shown in Fig. 10H may contain a patterned circuit layer over that of the previously described ground plane, bus or trace 82.

[00312] Each of the NMOS transistors in the second level of inverters 421" may have a ratio of a physical channel width thereof to a physical channel length thereof ranging from, e.g., about 20 to 20,000, and preferably ranging from, e.g., about 30 to 300, larger than that of NMOS transistor in the first level inverter 421' by between 1.5 times and 5 times, and preferably by natural exponential times. Each of the PMOS transistors in the second level of inverters 421" may have a ratio of a physical channel width thereof to a physical channel length thereof ranging from, e.g., about 40 to 40,000, and preferably ranging from, e.g., about 60 to 600, larger than that of PMOS transistor in the first level inverter 421' by between 1.5

times and 5 times, and preferably by natural exponential times. The off-chip driver 421 may output a driving current of between 5 mA and 5 A and, preferably, between 10 mA and 100 mA to an external circuit through the metal bump 89.

[00313] Provided that the off-chip driver 421 shown in Fig. 11D is applied to the circuit architecture shown in Fig. 8B for a power management chip, each of the NMOS transistors in the second level of inverters 421" may have a ratio of a physical channel width thereof to a physical channel length thereof ranging from, e.g., about 2,000 to 200,000, and preferably ranging from, e.g., about 2,000 to 20,000. Each of the PMOS transistors in the second level of inverters 421" may have a ratio of a physical channel width thereof to a physical channel length thereof ranging from, e.g., about 4,000 to 400,000, and preferably ranging from, e.g., about 4,000 to 40,000. The off-chip driver 421 may output a driving current of between 500 mA and 50 A and, preferably, between 500 mA and 5 A to an external circuit through the metal bump 89.

[00314] In a sixth aspect, the off-chip buffer 42 may be an off-chip driver 421 composed of a first level of inverter 421', a second level of inverters 421", a third level of inverter 421"' and a fourth level of inverter 421"", as shown in Fig. 11G in application to the circuit architecture shown in Fig. 8B, and the first level of inverter 421' is connected in series to the second level of inverters 421", the second level of inverter 421" is connected in series to the third level of inverters 421"', and the third level of inverter 421' is connected in series to the fourth level of inverters 421"". Fig. 8F shows a circuit diagram with the off-driver 421 of Fig. 11G applied to the circuit architecture shown in Fig. 8C. Fig. 9D shows a top perspective view realizing the circuit diagram of Fig. 8F. Fig. 10I shows a chip structure realizing the circuit diagram of Fig. 8F. The off-chip driver 421 has an input node F connected to the internal circuits 20 through the thick and wide circuit trace 83, and an output node E connected, in parallel with the off-chip ESD circuit 43, to the metal bump 89. The gates of the PMOS device and the NMOS device in the first level of inverter 421' serve as the input node F, and the drains of the PMOS device and the NMOS device in the fourth level of inverter 421"" serve as the output node E. The drains of the PMOS device and the NMOS device in the first level of inverter 421' are connected to the gates of the PMOS device and the NMOS device in the second level of inverter 421" through a fine-line metal trace or bus under the passivation layer 5. The drains of the PMOS device and the NMOS device in the second level of inverter 421" are connected to the gates of the PMOS device and the NMOS device in the third level of inverter 421"' through a fine-line metal trace or bus under the passivation layer 5. The drains

of the PMOS device and the NMOS device in the third level of inverter 421''' are connected to the gates of the PMOS device and the NMOS device in the fourth level of inverter 421'''' through a fine-line metal trace or bus under the passivation layer 5. The drains of the PMOS device and the NMOS device in the fourth level of inverters 421'''' are connected to the metal bump 89 through the thick and wide metal trace or bus 83r over the passivation layer 5. A patterned circuit layer 831 formed on the polymer layer 95, such as polyimide, having a thickness of between 2 and 30 micrometers may be composed of the thick and wide metal traces or buses 83r and 83, that is, the thick and wide metal traces or buses 83r and 83 may be formed at the same time, as shown in Fig. 10I.

[00315] Referring to Fig. 11G, the previously described power plane, bus or trace 81, 811 or 812, as shown in Figs. 1B, 1C, 2B, 2C, 3B, 3C and 3D, over the passivation layer 5 can connect the node P of the voltage regulator or converter circuit 41 to the source of the PMOS device in the first level of inverter 421', to the source of the PMOS device in the second level of inverter 421'', to the source of the PMOS device in the third level of inverter 421''' and to the source of the PMOS device in the fourth level of inverter 421''''. The previously described power plane, bus or trace 81, 811 or 812 may contain a patterned circuit layer over the patterned circuit layer 831 of the thick and wide signal trace, bus or plane 83 as shown in Fig. 10I. Alternatively, the thick and wide signal trace, bus or plane 83 as shown in Fig. 10I may contain a patterned circuit layer over that of the previously described power plane, bus or trace 81. The previously described ground plane, bus or trace 82 or 821, as shown in Figs. 1C, 2C and 3C, over the passivation layer 5 can connect the node Rs of the voltage regulator or converter circuit 41, the source of the NMOS device in the first level of inverter 421', the source of the NMOS device in the second level of inverter 421'', the source of the NMOS device in the third level of inverter 421''', and the source of the NMOS device in the fourth level of inverter 421''''. The previously described ground plane, bus or trace 82 or 821 may contain a patterned circuit layer over the patterned circuit layer 831 of the thick and wide signal trace, bus or plane 83 as shown in Fig. 10I. Alternatively, the thick and wide signal trace, bus or plane 83 as shown in Fig. 10I may contain a patterned circuit layer over that of the previously described ground plane, bus or trace 82.

[00316] The NMOS transistor in the fourth level of inverter 421'''' may have a ratio of a physical channel width thereof to a physical channel length thereof larger than that of the NMOS transistor in the third level of inverter 421''' by between 1.5 and 5 times, and preferably by natural exponential times, that is larger than that of the NMOS transistor in the second level

of inverter 421'' by between 1.5 and 5 times, and preferably by natural exponential times, that is larger than that of the NMOS transistor in the first level of inverter 421' by between 1.5 and 5 times, and preferably by natural exponential times. The PMOS transistor in the fourth level of inverter 421'''' may have a ratio of a physical channel width thereof to a physical channel length thereof larger than that of the PMOS transistor in the third level of inverter 421''' by between 1.5 and 5 times, and preferably by natural exponential times, that is larger than that of the PMOS transistor in the second level of inverter 421'' by between 1.5 and 5 times, and preferably by natural exponential times, that is larger than that of the PMOS transistor in the first level of inverter 421' by between 1.5 and 5 times, and preferably by natural exponential times. The off-chip driver 421 may output a driving current of between 5 mA and 5 A and, preferably, between 10 mA and 100 mA to an external circuit through the metal bump 89.

[00317] The NMOS transistor in the fourth level of inverter 421'''' may have a ratio of a physical channel width thereof to a physical channel length thereof ranging from, e.g., about 20 to 20,000, and preferably ranging from, e.g., about 30 to 300. The PMOS transistor in the fourth level of inverter 421'''' may have a ratio of a physical channel width thereof to a physical channel length thereof ranging from, e.g., about 40 to 40,000, and preferably ranging from, e.g., about 60 to 600. The NMOS transistor in the third level of inverter 421''' may have a ratio of a physical channel width thereof to a physical channel length thereof ranging from, e.g., about 7 to 7,000, and preferably ranging from, e.g., about 10 to 100. The PMOS transistor in the third level of inverter 421''' may have a ratio of a physical channel width thereof to a physical channel length thereof ranging from, e.g., about 13 to 13,000, and preferably ranging from, e.g., about 20 to 200. The NMOS transistor in the second level of inverter 421'' may have a ratio of a physical channel width thereof to a physical channel length thereof ranging from, e.g., about 2 to 2,000, and preferably ranging from, e.g., about 3 to 30. The PMOS transistor in the second level of inverter 421'' may have a ratio of a physical channel width thereof to a physical channel length thereof ranging from, e.g., about 4 to 4,000, and preferably ranging from, e.g., about 6 to 70.

[00318] Provided that the off-chip driver 421 shown in Fig. 11D is applied to the circuit architecture shown in Fig. 8B for a power management chip, the NMOS transistor in the fourth level of inverter 421'''' may have a ratio of a physical channel width thereof to a physical channel length thereof ranging from, e.g., about 2,000 to 200,000, and preferably ranging from, e.g., about 2,000 to 20,000. The PMOS transistor in the fourth level of inverter 421'''' may have a ratio of a physical channel width thereof to a physical channel length thereof ranging

from, e.g., about 4,000 to 400,000, and preferably ranging from, e.g., about 4,000 to 40,000. The NMOS transistor in the third level of inverter 421''' may have a ratio of a physical channel width thereof to a physical channel length thereof ranging from, e.g., about 700 to 70,000, and preferably ranging from, e.g., about 700 to 7,000. The PMOS transistor in the third level of inverter 421''' may have a ratio of a physical channel width thereof to a physical channel length thereof ranging from, e.g., about 1,300 to 130,000, and preferably ranging from, e.g., about 1,300 to 13,000. The NMOS transistor in the second level of inverter 421'' may have a ratio of a physical channel width thereof to a physical channel length thereof ranging from, e.g., about 230 to 23,000, and preferably ranging from, e.g., about 230 to 2,300. The PMOS transistor in the second level of inverter 421'' may have a ratio of a physical channel width thereof to a physical channel length thereof ranging from, e.g., about 400 to 40,000, and preferably ranging from, e.g., about 400 to 4,000. The off-chip driver 421 may output a driving current of between 500 mA and 50 A and, preferably, between 500 mA and 5 A to an external circuit through the metal bump 89.

[00319] Referring to Figs. 8B, 8C, 8E and 8F, the off-chip buffer 42 is connected, in parallel with the off-chip ESD circuit 43, to the metal bump 89. The detail of the off-chip ESD circuit 43 may be referred to as Fig. 11F. The off-chip ESD circuit 43 is composed of two reverse-biased diodes 4331 and 4332, and the node E is connected to the anode of the diode 4332, to the cathode of the diode 4331, to the off-chip buffer 42, such as off-chip driver 421 of Fig. 11A, 11D or 11G, off-chip receiver 422 of Fig. 11B, or tri-state buffer 423 of Fig. 11C or 11E, and to the metal bump 89. The diode 4331 is reverse-biased between an external voltage and the ground voltage Vss, and the diode 4332 is reverse-biased between the external voltage and the power voltage Vdd or Vcc.

[00320] Referring to Fig. 11F, an external power voltage Vdd can be provided to the cathode of the diode 4332 through a power bus or plane over the passivation layer 5. The previously described ground plane, bus or trace 82 or 821, as shown in Figs. 1C, 2C and 3C, over the passivation layer 5 can connect the node Rs of the voltage regulator or converter circuit 41 and the cathode of the diode 4331.

[00321] Accordingly, the voltage at the node E can be clamped between the power voltage Vdd input from an external circuit and the ground voltage Vss or between the power voltage Vdd and the ground voltage Vss. When the voltage at the node E suddenly exceeds the power voltage Vdd, a current will discharge from the node E to the external circuit through the

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diode 4332. When the voltage at the node E dramatically drop under the ground voltage Vss, a current will flow from the external circuit to the node E through the diode 4331.

[00322] Alternatively, the node E in the circuit diagrams in Figs. 8B, 8C, 8E and 8F can be protected by multiple off-chip ESD circuits 43, which can be referred to as Fig. 11H. For example, referring to Fig. 8D, the node E connecting the off-chip driver 42 to the metal bump 89 may be protected by multiple off-chip ESD circuits 43. Each of the off-chip ESD circuits 43 is composed of two reverse-biased diodes 4331 and 4332, and the node E is connected to the anodes of the diodes 4332, to the cathodes of the diodes 4331, to the off-chip buffer 42, such as off-chip driver 421 of Fig. 11A, 11D or 11G, off-chip receiver 422 of Fig. 11B, or tri-state buffer 423 of Fig. 11C or 11E, and to the metal bump 89. The diodes 4331 are reverse-biased between an external voltage and the ground voltage Vss, and the diodes 4332 are reverse-biased between the external voltage and the power voltage Vdd or Vcc.

[00323] Referring to Fig. 11H, an external power voltage Vdd can be provided to the cathodes of the diodes 4332 through a power bus or plane over the passivation layer 5. The previously described ground plane, bus or trace 82 or 821, as shown in Figs. 1C, 2C and 3C, over the passivation layer 5 can connect the node Rs of the voltage regulator or converter circuit 41 and the cathodes of the diodes 4331.

[00324] Accordingly, the voltage at the node E can be clamped between the power voltage Vdd input from an external circuit and the ground voltage Vss. When the voltage at the node E suddenly exceeds the power voltage Vdd, a current will discharge from the node E to the external circuit through the diodes 4332. When the voltage at the node E dramatically drop under the ground voltage Vss, a current will flow from the external circuit to the node E through the diodes 4331.

[00325] In Figs. 10B, 10D, 10G, 10H and 10I, there is only one patterned circuit layer 831, including a portion serving as the previously described thick and wide metal trace 83 and another portion serving as the previously described thick and wide metal trace 83r, over the passivation layer 5. The patterned circuit layer 831 may contain an adhesion/barrier layer, a seed layer on the adhesion/barrier layer, and an electroplated metal layer 8312 on the seed layer, the adhesion/barrier layer and the seed layer composing the bottom layer 8311.

[00326] Referring to Fig. 10B, regards to the process for forming the patterned circuit layer 831, the adhesion/barrier layer may be formed by a suitable process or processes, e.g., by sputtering a titanium-containing layer, such as titanium layer or a titanium-tungsten-alloy layer,

having a thickness between 1000 and 6000 angstroms, sputtering a chromium-containing layer, such as chromium layer, having a thickness between 1000 and 6000 angstroms, or sputtering a tantalum-containing layer, such as tantalum layer or tantalum-nitride layer, having a thickness between 1000 and 6000 angstroms, on a silicon-nitride layer of the passivation layer 5 and on contact pads 6390, principally made of aluminum or copper, exposed by multiple openings 539, 539', 531, 532 and 534 in the passivation layer 5. Thereafter, the seed layer may be formed by a suitable process or processes, e.g., by sputtering a copper layer having a thickness between 200 and 3000 angstroms on the adhesion/barrier layer of any previously described material or by sputtering a gold layer having a thickness between 200 and 3000 angstroms on the adhesion/barrier layer of any previously described material. Thereafter, a photoresist layer may be formed on the seed layer, multiple openings in the photoresist layer exposing the seed layer. Thereafter, the metal layer 8312 may be formed by a suitable process or processes, e.g., by electroplating a copper layer having a thickness between 2 and 30 micrometers on the copper layer serving as the seed layer, exposed by the openings in the photoresist layer, by electroplating a copper layer having a thickness between 2 and 30 micrometers on the copper layer serving as the seed layer, exposed by the openings in the photoresist layer and then electroplating a nickel layer having a thickness between 0.5 and 10 micrometers on the electroplated copper layer in the openings in the photoresist layer, by electroplating a copper layer having a thickness between 2 and 30 micrometers on the copper layer serving as the seed layer, exposed by the openings in the photoresist layer, electroplating a nickel layer having a thickness between 0.5 and 10 micrometers on the electroplated copper layer in the openings in the photoresist layer and then electroplating a gold layer, platinum layer, palladium layer or ruthenium layer having a thickness between 0.05 and 2 micrometers on the electroplated nickel layer in the openings in the photoresist layer, or by electroplating a gold layer having a thickness between 2 and 30 micrometers on the gold layer serving as the seed layer, exposed by the openings in the photoresist layer. Thereafter, the photoresist layer may be removed. Thereafter, the seed layer not under the metal layer 8312 is removed using a wet-etching process or using a dry-etching process. Thereafter, the adhesion/barrier layer not under the metal layer 8312 is removed using a wet-etching process or using a dry-etching process.

[00327] After the patterned circuit layer 831 is formed, a polymer layer 99 can be formed by a suitable process or processes, e.g., by spin-on coating a negative photosensitive polyimide layer, such as ester type, on the patterned circuit layer 831 and on the nitride layer of the passivation layer 5, exposing the spin-on coated photosensitive polyimide layer, developing

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the exposed polyimide layer and then curing the developed polyimide layer at the temperature between 265 and 285°C for a time between 30 and 240 minutes in a nitrogen or oxygen-free ambient. Accordingly, an opening 9939 may be formed in the polymer layer 99, exposing the contact point 8310 of the patterned circuit layer 831.

[00328] The process of forming the metal bump 89 on the polymer layer 99 and on the contact point 8310 exposed by the opening 9939 as shown in Figs. 10B and 10D can be referred to as the process of forming the metal bumps 89 on the polymer layer 98 and on the regions 801a exposed by the openings 980 as illustrated in Fig. 15M. The specification of the metal bump 89 as shown in Figs. 10B and 10D can be referred to as the specification of the metal bumps 89 as illustrated in Fig. 15M.

[00329] The metal bump 89 can be used to be connected to a printed circuit board, a ceramic substrate, another semiconductor chip, a flexible substrate by a tape-automated bonding (TAB) process, or a glass substrate via anisotropic conductive film or paste (ACF or ACP).

[00330] Alternatively, referring to Fig. 10B, a nickel layer having a thickness between 0.05 and 2 micrometers can be electroless plated on the contact point 8310 exposed by the opening 9939, and a gold layer, platinum layer, palladium layer or ruthenium layer having a thickness between 0.05 and 2 micrometers can be electroless plated on the electroless plated nickel layer in the opening 9939 in the polymer layer 99. Thereafter, a gold wire or a copper wire can be bonded onto the electroless plated gold layer in the opening 9939 in the polymer layer 99 using a wirebonding process.

[00331] Alternatively, referring to Fig. 10B, a gold wire or a copper wire can be bonded onto a gold layer, platinum layer, palladium layer or ruthenium layer of the patterned circuit layer 831, exposed by the openings 9939 in the polymer layer 99 using a wirebonding process.

[00332] Alternatively, referring to Fig. 10C, there may be multiple patterned circuit layers 831 and 832, including a portion serving as the previously described thick and wide metal trace 83 and another portion serving as the previously described thick and wide metal trace 83r, over the passivation layer 5. The process for forming the patterned circuit layer 831 shown in Fig. 10C can be referred to as the process for forming the patterned circuit layer 831 shown in Fig. 10B. The patterned circuit layer 832 may contain an adhesion/barrier layer, a seed layer on the adhesion/barrier layer, and an electroplated metal layer 8322 on the seed layer, the adhesion/barrier layer and the seed layer composing the bottom layer 8321.

[00333] Referring to Fig. 10C, after the patterned circuit layer 831 is formed, a polymer layer 98 can be formed by a suitable process or processes, e.g., by spin-on coating a negative photosensitive polyimide layer, such as ester type, on the patterned circuit layer 831 and on the nitride layer of the passivation layer 5, exposing the spin-on coated photosensitive polyimide layer, developing the exposed polyimide layer and then curing the developed polyimide layer at the temperature between 265 and 285°C for a time between 30 and 240 minutes in a nitrogen or oxygen-free ambient. Accordingly, multiple openings 9831, 9834 and 9839 may be formed in the polymer layer 98, exposing multiple contact pads of the patterned circuit layer 831.

[00334] Referring to Fig. 10C, regards to the process for forming the patterned circuit layer 832, the adhesion/barrier layer may be formed by a suitable process or processes, e.g., by sputtering a titanium-containing layer, such as titanium layer or a titanium-tungsten-alloy layer, having a thickness between 1000 and 6000 angstroms, sputtering a chromium-containing layer, such as chromium layer, having a thickness between 1000 and 6000 angstroms, or sputtering a tantalum-containing layer, such as tantalum layer or tantalum-nitride layer, having a thickness between 1000 and 6000 angstroms, on the polymer layer 98 and on the contact pads of the patterned circuit layer 831 exposed by multiple openings 9839, 9831 and 9834 in the polymer layer 98. Thereafter, the seed layer may be formed by a suitable process or processes, e.g., by sputtering a copper layer having a thickness between 200 and 3000 angstroms on the adhesion/barrier layer of any previously described material or by sputtering a gold layer having a thickness between 200 and 3000 angstroms on the adhesion/barrier layer of any previously described material. Thereafter, a photoresist layer may be formed on the seed layer, multiple openings in the photoresist layer exposing the seed layer. Thereafter, the metal layer 8322 may be formed by a suitable process or processes, e.g., by electroplating a copper layer having a thickness between 2 and 30 micrometers on the copper layer serving as the seed layer, exposed by the openings in the photoresist layer, by electroplating a copper layer having a thickness between 2 and 30 micrometers on the copper layer serving as the seed layer, exposed by the openings in the photoresist layer and then electroplating a nickel layer having a thickness between 0.5 and 10 micrometers on the electroplated copper layer in the openings in the photoresist layer, by electroplating a copper layer having a thickness between 2 and 30 micrometers on the copper layer serving as the seed layer, exposed by the openings in the photoresist layer, electroplating a nickel layer having a thickness between 0.5 and 10 micrometers on the electroplated copper layer in the openings in the photoresist layer and then electroplating a gold layer, platinum layer, palladium layer or ruthenium layer having a

thickness between 0.05 and 2 micrometers on the electroplated nickel layer in the openings in the photoresist layer, or by electroplating a gold layer having a thickness between 2 and 30 micrometers on the gold layer serving as the seed layer, exposed by the openings in the photoresist layer. Thereafter, the photoresist layer may be removed. Thereafter, the seed layer not under the metal layer 8322 is removed using a wet-etching process or using a dry-etching process. Thereafter, the adhesion/barrier layer not under the metal layer 8322 is removed using a wet-etching process or using a dry-etching process.

[00335] After the patterned circuit layer 832 is formed, a polymer layer 99 can be formed by a suitable process or processes, e.g., by spin-on coating a negative photosensitive polyimide layer, such as ester type, on the patterned circuit layer 832 and on the polymer layer 98, exposing the spin-on coated photosensitive polyimide layer, developing the exposed polyimide layer and then curing the developed polyimide layer at the temperature between 265 and 285°C for a time between 30 and 240 minutes in a nitrogen or oxygen-free ambient. Accordingly, an opening 9939' may be formed in the polymer layer 99, exposing a contact point 8320 of the patterned circuit layer 832.

[00336] The process of forming the metal bump 89 on the polymer layer 99 and on the contact point 8320 exposed by the opening 9939' as shown in Figs. 10C and 10E can be referred to as the process of forming the metal bumps 89 on the polymer layer 98 and on the regions 801a exposed by the openings 980 as illustrated in Fig. 15M. The specification of the metal bump 89 as shown in Figs. 10C and 10E can be referred to as the specification of the metal bumps 89 as illustrated in Fig. 15M.

[00337] The metal bump 89 shown in Figs. 10C and 10E can be used to be connected to a printed circuit board, a ceramic substrate, another semiconductor chip, a flexible substrate by a tape-automated bonding (TAB) process, or a glass substrate via anisotropic conductive film or paste (ACF or ACP).

[00338] Alternatively, referring to Fig. 10C, a nickel layer having a thickness between 0.05 and 2 micrometers can be electroless plated on the contact point 8320 exposed by the opening 9939' in layer polymer layer 99, and a gold layer, platinum layer, palladium layer or ruthenium layer having a thickness between 0.05 and 2 micrometers can be electroless plated on the electroless plated nickel layer in the opening 9939' in the polymer layer 99. Thereafter, a gold wire or a copper wire can be bonded onto the electroless plated gold layer in the opening 9939' in the polymer layer 99 using a wirebonding process.

[00339] Alternatively, referring to Fig. 10C, a gold wire or a copper wire can be bonded onto a gold layer, platinum layer, palladium layer or ruthenium layer of the patterned circuit layer 832, exposed by the openings 9939' in the polymer layer 99 using a wirebonding process.

[00340] Referring to Figs. 10D and 10E, before the patterned circuit layer 831 is formed, a polymer layer 95 can be optionally formed by a suitable process or processes, e.g., by spin-on coating a negative photosensitive polyimide layer, such as ester type, on the nitride layer of the passivation layer 5 and on the contact pads 6390, exposing the spin-on coated photosensitive polyimide layer, developing the exposed polyimide layer and then curing the developed polyimide layer at the temperature between 265 and 285°C for a time between 30 and 240 minutes in a nitrogen or oxygen-free ambient. Accordingly, multiple openings 9539, 9539', 9531, 9532 and 9534 may be formed in the polymer layer 95, exposing multiple contact pads 6390 exposed by the openings 539, 539', 531, 532 and 533 in the passivation layer 5. After the polymer layer 95 is formed, the patterned circuit layer 831 can be formed on the polymer layer 95 and on the contact pads 6390 exposed by the openings 539, 539', 531, 532 and 533. The adhesion/barrier layer of any previously described material may be sputtered on the polymer layer 95 and on the contact pads 6390 exposed by the openings 9539, 9539', 9531, 9532 and 9534 in the polymer layer 95.

[00341] Alternatively, referring to Fig. 10F, the off-chip buffer 42, such as off-chip driver of Figs. 11A, 11D or 11E, off-chip receiver of Fig. 11B or tri-state buffer of Figs. 11C or 11E, can be connected to the internal circuits 20 through the fine-line metal trace 638 under the passivation layer 5 but not through any trace or bus over the passivation layer 5. There may be only one patterned circuit layer 831 including a portion serving as the previously described thick and wide metal trace 83r, over the passivation layer 5. The position of the contact point 8310 of the previously described thick and wide metal trace 83r for being wirebonded thereto from a top perspective view is different from that of the contact pad exposed by the opening 539 in the passivation layer 5. The process for forming the patterned circuit layer 831 can be referred to as that for forming the patterned circuit layer 831 shown in Fig. 10B. The process for forming the polymer layer 99 can be referred to as that for forming the polymer layer 99 shown in Fig. 10B.

[00342] Referring to Fig. 10F, a gold wire pr a copper wire can be bonded onto a gold layer, platinum layer, palladium layer or ruthenium layer of the patterned circuit layer 831, exposed by the openings 9939 in the polymer layer 99 using a wirebonding process.

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[00343] As an alternate, referring to Fig. 10F, a nickel layer having a thickness between 0.05 and 2 micrometers can be electroless plated on the contact point 8310 exposed by the opening 9939 in the polymer layer 99, and a gold layer, platinum layer, palladium layer or ruthenium layer having a thickness between 0.05 and 2 micrometers can be electroless plated on the electroless plated nickel layer in the opening 9939 in the polymer layer 99. Thereafter, a gold wire or a copper wire can be bonded onto the electroless plated gold layer in the opening 9939 in the polymer layer 99 using a wirebonding process.

[00344] Referring to Figs. 10G-10I, a gold wire or a copper wire can be bonded onto a gold layer, platinum layer, palladium layer or ruthenium layer of the patterned circuit layer 831, exposed by the openings 9939 in the polymer layer 99 using a wirebonding process.

[00345] As an alternate, referring to Figs. 10G-10I, a nickel layer having a thickness between 0.05 and 2 micrometers can be electroless plated on the contact point 8310 exposed by the opening 9939 in the polymer layer 99, and a gold layer, platinum layer, palladium layer or ruthenium layer having a thickness between 0.05 and 2 micrometers can be electroless plated on the electroless plated nickel layer in the opening 9939 in the polymer layer 99. Thereafter, a gold wire can be bonded onto the electroless plated gold layer in the opening 9939 in the polymer layer 99 using a wirebonding process.

[00346] The circuitry shown in Figs. 8B-8F, 9B-9B and 10B-10I can be used in a flash memory chip, in a DRAM memory chip or in a SRAM memory chip. The I/O pad relocation using the redistribution layer 83r is particularly useful for the stacked packaging with flash, DRAM or SRAM memory chips. The I/O pads of a DRAM chip are usually designed roughly along the centerline of the chip, and cannot be used for stacked packages. The redistribution layer 83r relocates the center pad to the peripheral of the chip for the wirebonding in the stacked package. Figs. 10F and 10G show specific examples, with a wire bonded on the contact point 8310 connected to the original pad 6390 exposed by the opening 539 in the passivation layer 5 via the thick and wide metal trace of bus 83r. In Figs. 8B, 9B, 10B-10G, in an application to a memory chip, an SRAM cell, or a flash memory cell, or a DRAM cell is connected to the input node Xi of the internal circuit 21, such as sense amplifier, internal tri-state buffer 213 of Fig. 5F, pass circuit 216 of Fig. 5G, latch circuit 217 of Fig. 5H, circuit of pass circuit 216 and internal driver 212 shown in Fig. 5I, or circuit of latch circuit 217 and internal driver 212 shown in Fig. 5J. The various detailed internal circuit 21 and methods connecting a memory cell to the internal circuit 21 can be referred to as shown in Figs. 5F-5J.

Referring to Figs. 8B, 8D-8F, 9B-9D and 10B-10I, an SRAM cell, or a flash cell or a DRAM cell is connected to external circuit (1) through sense amplifier 214 of Figs. 5F-5J; (2) through an internal tri-state buffer 213 of Fig. 5F, a pass circuit 216 of Fig. 5G, a latch circuit 217 of Fig. 5H, a circuit of a pass circuit 216 and an internal driver 212 as shown in Fig. 5I, or a circuit of a latch circuit 217 and an internal driver 212 as shown in Fig. 5J; (3) through a first fine-line structure formed by a suitable process or processes, e.g., by stacked vias and metals 631; (4) up through a first passivation opening 531; (5) for 10G, also through a first polymer opening 9531; (6) through a fine-line metal 638 under the passivation layer 5 for Fig. 10F; while through an over-passivation metal lines, traces or planes 83 in one or more metal layers over the passivation layer 5 for Fig. 10G; (7) for Fig. 10G, down through a second polymer opening 9539'; (8) through a second passivation opening 539'; (9) through a fine-line metal structure formed by a suitable process or processes, e.g., by stacked vias and metal pads 639', connected to the input of an off-chip buffer 42, (10) through the output of the off-chip buffer 42 connected to an off-chip ESD circuit 43, and to a stacked fine-line metal vias and metal pads 639, (11) through an passivation opening 539, (12) for 10G, also through a third polymer opening 9539; and (13) through an over-passivation redistribution metal lines or traces or planes 83r, (14) through over-passivation metal pad 8310 exposed by a polymer opening 9939; (15) through a bonding wire 89' on the contact point 8310 or a metal bump 89.

[00347] Note that as in Fig. 10G, there may be a polymer layer under or over the redistribution metal layer 83r. The redistribution metal lines, traces or planes 83r can be formed by a suitable process or processes, e.g., by a (electroplated or electroless plated) gold layer with thickness within a range between 1.5 µm and 30 µm, exemplary 2 µm and 10 µm; or by a (electroplated) copper layer with thickness within a range between 2 µm and 100 µm, exemplary 3 µm and 20 µm, a Ni cap layer (thickness between 0.5 µm and 5µm) on the copper layer and an assembly metal layer of Au or Pd, or Ru (thickness between 0.05 µm and 5µm) on the Ni cap layer. A wirebonding is performed on the surface of the gold, palladium, platinum or ruthenium layer of the over- passivation metal pad 8310.

[00348] Referring to Figs. 8B-8F, 9B-9D, 10B-10E and 10G-10I, the shape of the openings 531, 532, 534 and 539' in the passivation layer 5 from a top perspective view may be round, square, rectangular or polygon. If the openings 531, 532, 534, 539 and 539' are round, the openings 531, 532, 534, 539 and 539' may have a diameter of between 0.1 and 200 microns, between 1 and 100 microns, or, preferably, between 0.1 and 30 microns. If the openings 531, 532, 534, 539 and 539' are square, the openings 531, 532, 534, 539 and 539' may have a width

of between 0.1 and 200 microns, between 1 and 100 microns, or, preferably, between 0.1 and 30 microns. If the openings 531, 532, 534, 539 and 539' are rectangular, the openings 531, 532, 534, 539 and 539' may have a width of between 0.1 and 200 microns, between 1 and 100 microns, or, preferably, between 0.1 and 30 microns, and a length of between 1 micron and 1 centimeter. If the openings 531, 532, 534, 539 and 539' are polygon having more than five sides, the openings 531, 532, 534, 539 and 539' have a largest diagonal length of between 0.1 and 200 microns, between 1 and 100 microns, or, preferably, between 0.1 and 30 microns. Alternatively, the openings 531, 532, 534, 539 and 539' have a largest transverse dimension of between 0.1 and 200 microns, between 1 and 100 microns, or, preferably, between 0.1 and 30 microns. In a case shown in Figs. 10C-10E, 10G, 10H and 10I, the openings 531, 532, 534, 539 and 539' have a width of between 0.1 and 30 microns, with the lower portion of the openings 9531, 9532, 9534, 9539 and 9539' in the polymer layer 95 having a width of between 20 and 100 microns. The openings 9531, 9532 and 9534 in the polymer layer 95 have lower portions having widths or transverse dimensions larger than those of the openings 531, 532 and 534 in the passivation layer 5 aligned with the openings 9531, 9532 and 9534, respectively. The openings 9531, 9532 and 9534 in the polymer layer 95 further expose the passivation layer 5 close to the openings 531, 532 and 534. The polymer layer 95 covers the peripheral region of the contact pad exposed by the openings 539 and 539' in the passivation layer 5, but the openings 9539 and 9539' in the polymer layer 95 exposes the center region of the contact pad exposed by the openings 539 and 539' in the passivation layer 5. The widths or transverse dimensions of the openings 539 and 539' in the passivation layer 5 are larger than those of the openings 9539 and 9539', respectively.

[00349] In Figs. 8A-8F, a dotted line 5 indicates the passivation layer, coarse traces indicate traces of an over-passivation scheme 102 formed over the passivation layer 5, and fine traces indicate traces formed under the passivation layer 5. In Figs. 9A-9D, coarse traces indicate the traces of the over-passivation scheme 102 formed over the passivation layer 5, and fine traces indicate the traces formed under the passivation layer 5. The over-passivation scheme 102 shown in Fig. 10A includes the polymer layer 99, the metal trace 83r provided by the patterned circuit layer 831, and the metal bump 89, and the opening 9939 in polymer layer 99 is over the contact point 8310 of the metal trace 83r, and the metal bump 89 is in the opening 9939, on the contact point 8310 and on the polymer layer 99. The over-passivation scheme 102 shown in Fig. 10B includes the polymer layer 99, the metal traces 83 and 83r provided by the patterned circuit layer 831, and the metal bump 89, and the opening 9939 in

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polymer layer 99 is over the contact point 8310 of the metal trace 83r, and the metal bump 89 is in the opening 9939, on the contact point 8310 and on the polymer layer 99. The over-passivation scheme 102 shown in Fig. 10C includes the polymer layers 98 and 99, the metal traces 83 and 83r provided by the patterned circuit layers 831 and 832, and the metal bump 89, and the opening 9939' in polymer layer 99 is over the contact point 8320 of the metal trace 83r, and the metal bump 89 is in the opening 9939', on the contact point 8320 and on the polymer layer 99. The over-passivation scheme 102 shown in Fig. 10D includes the polymer layers 95 and 99, the metal traces 83 and 83r provided by the patterned circuit layer 831, and the metal bump 89, and the openings 9539, 9539', 9531, 9532 and 9534 are in the polymer layer 95, and the opening 9939 in polymer layer 99 is over the contact point 8320 of the metal trace 83r, and the metal bump 89 is in the opening 9939, on the contact point 8320 and on the polymer layer 99. The over-passivation scheme 102 shown in Fig. 10E includes the polymer layers 95, 98 and 99, the metal traces 83 and 83r provided by the patterned circuit layers 831 and 832, and the metal bump 89, and the openings 9539, 9539', 9531, 9532 and 9534 are in the polymer layer 95, and the openings 9831, 9834 and 9839 in the polymer layer 98 are over the patterned circuit layer 831, and the opening 9939' in polymer layer 99 is over the contact point 8320 of the metal trace 83r, and the metal bump 89 is in the opening 9939', on the contact point 8320 and on the polymer layer 99. The over-passivation scheme 102 shown in Fig. 10F includes the polymer layer 99 and the metal trace 83r provided by the patterned circuit layer 831, and the opening 9939 in the polymer layer 99 is over the contact point 8310 of the metal trace 83r and exposes it. The over-passivation scheme 102 shown in Figs. 10G-10I includes the polymer layers 95 and 99 and the metal traces 83 and 83r provided by the patterned circuit layer 831, and the openings 9539, 9539', 9531, 9532 and 9534 are in the polymer layer 95, and the opening 9939 in the polymer layer 99 is over the contact point 8310 of the metal trace 83r and exposes it.

Fourth Embodiment: Power/Ground Buses Design Architecture

[00350] In the first embodiment of present disclosure described previously, an external power supply Vdd is provided to the voltage regulator or converter circuit 41, and the voltage regulator or converter circuit 41 outputs a power supply Vcc to the internal circuits 20. Alternatively, the external power supply Vdd can be input from an external circuit to the internal circuits 20, including 21, 22, 23 and 24, with an ESD protection circuit 44 required to prevent the voltage or current surge from damaging the internal circuits 20. The ESD circuit 44 is connected in parallel with the internal circuits 21, 22, 23 and 24. In the first embodiment in

Figs. 1B, 1C, 2B, 2C, 3B, 3C and 3D, an ESD circuit can be also added and connected in parallel with the voltage regulator or converter circuit 41, and with the internal circuits 21, 22, 23 and 24. For example, the circuit shown in Fig. 1D contains the circuit of Fig. 1C in addition with an ESD circuit 44. The ESD circuit 44 includes a power node Dp connected to a thick and wide power bus or plane 81P, delivering an external power voltage Vdd, and a ground node Dg connected to a thick and wide ground bus or plane 82. The thick and wide power bus or plane 81P connects the power node Dp of the ESD circuit 44 and the power node of the voltage regulator or converter circuit 41. The thick and wide ground bus or plane 82 connects the ground node Dg of the ESD circuit 44 and the ground node Rs of the voltage regulator or converter circuit 41. The ESD circuit 44 in the circuitry of Fig. 1D may be a reverse biased diode 4333, as shown in Fig. 12E, having an anode connected to the thick and wide ground bus or plane 82 and a cathode connected to the thick and wide power bus or plane 81P. An element in Fig. 1D can be referred to as the element in Fig. 1C indicated by a reference number identical to the element in Fig. 1D.

[00351] Fig. 12B shows a circuit diagram including a thick and wide power bus or plane 81P over the passivation layer 5, connecting an ESD circuit 44 and internal circuits 20. Fig. 13B shows a top view realizing the circuit diagram of Fig. 12B, and the bold lines shown in Fig. 13B means a thick and wide metal trace or bus over a passivation layer, and the fine lines shown in Fig. 13B means a fine metal trace under a passivation layer. Fig. 14B shows a cross-sectional view realizing the circuit diagram of Fig. 12B. In Fig. 12B, an external power supply voltage Vdd is input at a node Ep and distributed to the Vdd nodes, power nodes, Tp, Up, Vp and Wp of the internal circuits 21, 22, 23 and 24 through a thick and wide power bus or plane 81P over the passivation layer 5, through passivation openings 511, 512 and 514, and through power fine-line metal traces 611, 612 and 614 under the passivation layer 5. A power node Dp of an ESD circuit 44 is connected to a thick and wide metal trace, bus or plane 81P, power bus, through a fine-line metal trace or bus 649, and through an opening 549 in the passivation layer 5. The thick and wide power bus 81P can be connected to the power nodes Tp, Up, Vp and Wp of the internal circuits 21, 22, 23 and 24 that may include a NOR gate, NAND gate, AND gate, OR gate, operational amplifier, adder, multiplexer, diplexer, multiplier, A/D converter, D/A converter, CMOS device, bi-polar CMOS device, bipolar circuit, SRAM cell, DRAM cell, non-volatile memory cell, flash memory cell, EPROM cell, ROM cell, magnetic RAM (MRAM) or sense amplifier. The above mentioned power bus 81P shown in Fig. 12B, over the passivation layer 5, can be connected to the power nodes of the internal circuits 20 or

other circuits in the previously described four embodiments provided with access to a power voltage Vdd. The ESD circuit 44 in the circuitry of Fig. 12B may be a reverse biased diode 4333, as shown in Fig. 12E, having an anode connected to ground and a cathode connected to the thick and wide power bus or plane 81P.

[00352] In Fig. 14B, there is only one patterned circuit layer 811, including a portion serving as the previously described thick and wide metal trace 81P, power bus or plane, over the passivation layer 5. The patterned circuit layer 811 may contain an adhesion/barrier layer, a seed layer on the adhesion/barrier layer, and an electroplated metal layer 8112 on the seed layer, the adhesion/barrier layer and the seed layer composing the bottom layer 8111.

[00353] Referring to Fig. 14B, regards to the process for forming the patterned circuit layer 811, the adhesion/barrier layer may be formed by a suitable process or processes, e.g., by sputtering a titanium-containing layer, such as titanium layer or a titanium-tungsten-alloy layer, having a thickness between 1000 and 6000 angstroms, sputtering a chromium-containing layer, such as chromium layer, having a thickness between 1000 and 6000 angstroms, or sputtering a tantalum-containing layer, such as tantalum layer or tantalum-nitride layer, having a thickness between 1000 and 6000 angstroms, on a silicon-nitride layer of the passivation layer 5 and on contact pads 6490, principally made of aluminum or copper, exposed by multiple openings 549, 511, 512 and 514 in the passivation layer 5. Thereafter, the seed layer may be formed by a suitable process or processes, e.g., by sputtering a copper layer having a thickness between 200 and 3000 angstroms on the adhesion/barrier layer of any previously described material or by sputtering a gold layer having a thickness between 200 and 3000 angstroms on the adhesion/barrier layer of any previously described material. Thereafter, a photoresist layer may be formed on the seed layer, multiple openings in the photoresist layer exposing the seed layer. Thereafter, the metal layer 8112 may be formed by a suitable process or processes, e.g., by electroplating a copper layer having a thickness between 2 and 30 micrometers on the copper layer serving as the seed layer, exposed by the openings in the photoresist layer, by electroplating a copper layer having a thickness between 2 and 30 micrometers on the copper layer serving as the seed layer, exposed by the openings in the photoresist layer and then electroplating a nickel layer having a thickness between 0.5 and 10 micrometers on the electroplated copper layer in the openings in the photoresist layer, by electroplating a copper layer having a thickness between 2 and 30 micrometers on the copper layer serving as the seed layer, exposed by the openings in the photoresist layer, electroplating a nickel layer having a thickness between 0.5 and 10 micrometers on the electroplated copper layer in the openings in

the photoresist layer and then electroplating a gold layer, platinum layer, palladium layer or ruthenium layer having a thickness between 0.05 and 2 micrometers on the electroplated nickel layer in the openings in the photoresist layer, or by electroplating a gold layer having a thickness between 2 and 30 micrometers on the gold layer serving as the seed layer, exposed by the openings in the photoresist layer. Thereafter, the photoresist layer may be removed. Thereafter, the seed layer not under the metal layer 8112 is removed using a wet-etching process or using a dry-etching process. Thereafter, the adhesion/barrier layer not under the metal layer 8112 is removed using a wet-etching process or using a dry-etching process.

[00354] After the patterned circuit layer 811 is formed, a polymer layer 99 can be formed by a suitable process or processes, e.g., by spin-on coating a negative photosensitive polyimide layer, such as ester type, on the patterned circuit layer 811 and on the nitride layer of the passivation layer 5, exposing the spin-on coated photosensitive polyimide layer, developing the exposed polyimide layer and then curing the developed polyimide layer at the temperature between 265 and 285°C for a time between 30 and 240 minutes in a nitrogen or oxygen-free ambient. Accordingly, an opening 9949 may be formed in the polymer layer 99, exposing a contact pad 8110 of the patterned circuit layer 811.

[00355] Referring to Fig. 14B, for forming a metal bump over the contact pad 8110, an adhesion/barrier layer may be formed by a suitable process or processes, e.g., by sputtering a titanium-containing layer, such as titanium layer or a titanium-tungsten-alloy layer, having a thickness between 1000 and 6000 angstroms, sputtering a chromium-containing layer, such as chromium layer, having a thickness between 1000 and 6000 angstroms, or sputtering a tantalum-containing layer, such as tantalum layer or tantalum-nitride layer, having a thickness between 1000 and 6000 angstroms, on the polymer layer 99 and on the contact pad 8110 exposed by the opening 9949. Thereafter, the seed layer may be formed by a suitable process or processes, e.g., by sputtering a copper layer having a thickness between 200 and 3000 angstroms on the adhesion/barrier layer of any previously described material. Thereafter, a photoresist layer may be formed on the seed layer, multiple openings in the photoresist layer exposing the seed layer. Thereafter, the metal bump may be formed by a suitable process or processes, e.g., by electroplating a copper layer having a thickness between 0.5 and 10 micrometers on the copper layer serving as the seed layer, exposed by the openings in the photoresist layer, electroplating a nickel layer having a thickness between 0.5 and 10 micrometers on the electroplated copper layer in the openings in the photoresist layer, and then electroplating a tin-containing layer, such as a tin-lead alloy, a tin-silver alloy or a

tin-silver-copper alloy, having a thickness between 60 and 200 micrometers on the electroplated nickel layer in the openings in the photoresist layer. Thereafter, the photoresist layer may be removed. Thereafter, the seed layer not under the metal bump is removed using a wet-etching process or using a dry-etching process. Thereafter, the adhesion/barrier layer not under the metal bump is removed using a wet-etching process or using a dry-etching process. Thereafter, the metal bump can be reflowed to be shaped like a ball for a flip-chip assembly. The metal bump can be connected to a printed circuit board, ceramic substrate or another semiconductor chip.

[00356] Referring to Fig. 14B, for forming another kind of metal bump over the contact pad 8110, an adhesion/barrier layer may be formed by a suitable process or processes, e.g., by sputtering a titanium-containing layer, such as titanium layer or a titanium-tungsten-alloy layer, having a thickness between 1000 and 6000 angstroms, or sputtering a tantalum-containing layer, such as tantalum layer or tantalum-nitride layer, having a thickness between 1000 and 6000 angstroms, on the polymer layer 99 and on the contact pad 8110 exposed by the opening 9949. Thereafter, the seed layer may be formed by a suitable process or processes, e.g., by sputtering a gold layer having a thickness between 200 and 3000 angstroms on the adhesion/barrier layer of any previously described material. Thereafter, a photoresist layer may be formed on the seed layer, multiple openings in the photoresist layer exposing the seed layer. Thereafter, the metal bump may be formed by a suitable process or processes, e.g., by electroplating a gold layer having a thickness between 6 and 25 micrometers on the gold layer serving as the seed layer, exposed by the openings in the photoresist layer. Thereafter, the photoresist layer may be removed. Thereafter, the seed layer not under the metal bump is removed using a wet-etching process or using a dry-etching process. Thereafter, the adhesion/barrier layer not under the metal bump is removed using a wet-etching process or using a dry-etching process. The metal bump can be connected to a flexible substrate by a tape-automated bonding (TAB) process, or a glass substrate via anisotropic conductive film or paste (ACF or ACP).

[00357] Alternatively, referring to Fig. 14B, a nickel layer having a thickness between 0.05 and 2 micrometers can be electroless plated on the contact pad 8110 exposed by the opening 9949, and a gold layer, platinum layer, palladium layer or ruthenium layer having a thickness between 0.05 and 2 micrometers can be electroless plated on the electroless plated nickel layer in the opening 9949 in the polymer layer 99. Thereafter, a gold wire can be bonded

onto the electroless plated gold layer in the opening 9949 in the polymer layer 99 using a wirebonding process.

[00358] Alternatively, referring to Fig. 14B, a gold wire can be bonded onto a gold layer, platinum layer, palladium layer or ruthenium layer of the patterned circuit layer 811, exposed by the openings 9949 in the polymer layer 99 using a wirebonding process.

[00359] Referring to Fig. 14D, before the patterned circuit layer 811 is formed, a polymer layer 95 can be optionally formed by a suitable process or processes, e.g., by spin-on coating a negative photosensitive polyimide layer, such as ester type, on the nitride layer of the passivation layer 5 and on the contact pads 6490, exposing the spin-on coated photosensitive polyimide layer, developing the exposed polyimide layer and then curing the developed polyimide layer at the temperature between 265 and 285°C for a time between 30 and 240 minutes in a nitrogen or oxygen-free ambient. Accordingly, multiple openings 9549, 9511, 9512 and 9514 may be formed in the polymer layer 95, exposing multiple contact pads 6490 exposed by the openings 549, 511, 512 and 514 in the passivation layer 5. After the polymer layer 95 is formed, the patterned circuit layer 811 can be formed on the polymer layer 95 and on the contact pads 6490 exposed by the openings 549, 511, 512 and 514. The adhesion/barrier layer of any previously described material may be sputtered on the polymer layer 95 and on the contact pads 6490 exposed by the openings 9549, 9511, 9512 and 9514 in the polymer layer 95.

[00360] Fig.12C shows, in addition to the power Vdd connection in Fig. 12B, a ground Vss connection. Fig. 13C shows a top view realizing the circuit diagram of Fig. 12C, and the bold lines shown in Fig. 13C means a thick and wide metal trace or bus over a passivation layer, and the fine lines shown in Fig. 13C means a fine metal trace under a passivation layer. Fig. 14C shows a cross-sectional view realizing the circuit diagram of Fig. 12C. In Fig. 12C, the external ground Vss is input at a node Eg and provided to the Vss nodes Ts, Us, Vs and Ws of the internal circuits 21, 22, 23 and 24 through a thick and wide metal trace, bus or plane 82, ground bus or plane, over the passivation layer 5, through openings 521, 522 and 524 in the passivation layer 5, and through fine-line metal traces 621, 622 and 624 under the passivation layer 5. The thick and wide ground bus or plane 82 is connected to a Vss node Dg of the ESD circuit 44 through an opening 549` in the passivation layer 5 and through a fine-line ground metal bus 649' under the passivation layer 5. The above mentioned power bus 81P shown in Fig. 12C, over the passivation layer 5, can be connected to the power nodes of the internal

circuits 20 or other circuits in the previously described four embodiments provided with access to a power voltage Vdd. The above mentioned ground bus 82 shown in Fig. 12C, over the passivation layer 5, can be connected to the ground nodes of the internal circuits 20 or other circuits in the previously described four embodiments provided with access to a ground voltage Vss. The ESD circuit 44 in the circuitry of Fig. 12C may be a reverse biased diode 4333, as shown in Fig. 12E, having an anode connected to the thick and wide ground bus or plane 82 and a cathode connected to the thick and wide power bus or plane 81P.

[00361] Referring to Fig. 14C, there may be multiple patterned circuit layers 821 and 812, including the previously described ground bus or plane 82 and the previously described power bus or plane 81P over the ground bus or plane 82, over the passivation layer 5. The process for forming the patterned circuit layer 821 on the passivation layer 5 and on the contact pads 6490' exposed by the openings 549', 521, 522 and 524 can be referred to as the process for forming the patterned circuit layer 811 shown in Fig. 14B on the passivation layer 5 and on the contact pads 6490 exposed by the openings 549, 511, 512 and 514. The patterned circuit layer 821 may contain an adhesion/barrier layer, a seed layer on the adhesion/barrier layer, and an electroplated metal layer 8212 on the seed layer, the adhesion/barrier layer and the seed layer composing the bottom layer 8211. The patterned circuit layer 812 may contain an adhesion/barrier layer, a seed layer on the adhesion/barrier layer, and an electroplated metal layer 8122 on the seed layer, the adhesion/barrier layer and the seed layer composing the bottom layer 8121.

[00362] Referring to Fig. 14C, after the patterned circuit layer 821 is formed, a polymer layer 98 can be formed by a suitable process or processes, e.g., by spin-on coating a negative photosensitive polyimide layer, such as ester type, on the patterned circuit layer 821 and on the nitride layer of the passivation layer 5, exposing the spin-on coated photosensitive polyimide layer, developing the exposed polyimide layer and then curing the developed polyimide layer at the temperature between 265 and 285°C for a time between 30 and 240 minutes in a nitrogen or oxygen-free ambient. Accordingly, an opening 9849' may be formed in the polymer layer 98, exposing a contact pad of the patterned circuit layer 821.

[00363] Referring to Fig. 14C, regards to the process for forming the patterned circuit layer 812, the adhesion/barrier layer may be formed by a suitable process or processes, e.g., by sputtering a titanium-containing layer, such as titanium layer or a titanium-tungsten-alloy layer, having a thickness between 1000 and 6000 angstroms, sputtering a chromium-containing layer,

such as chromium layer, having a thickness between 1000 and 6000 angstroms, or sputtering a tantalum-containing layer, such as tantalum layer or tantalum-nitride layer, having a thickness between 1000 and 6000 angstroms, on the polymer layer 98 and on the contact pad of the patterned circuit layer 821 exposed by the opening 9849' in the polymer layer 98. Thereafter, the seed layer may be formed by a suitable process or processes, e.g., by sputtering a copper layer having a thickness between 200 and 3000 angstroms on the adhesion/barrier layer of any previously described material or by sputtering a gold layer having a thickness between 200 and 3000 angstroms on the adhesion/barrier layer of any previously described material. Thereafter, a photoresist layer may be formed on the seed layer, multiple openings in the photoresist layer exposing the seed layer. Thereafter, the metal layer 8122 may be formed by a suitable process or processes, e.g., by electroplating a copper layer having a thickness between 2 and 30 micrometers on the copper layer serving as the seed layer, exposed by the openings in the photoresist layer, by electroplating a copper layer having a thickness between 2 and 30 micrometers on the copper layer serving as the seed layer, exposed by the openings in the photoresist layer and then electroplating a nickel layer having a thickness between 0.5 and 10 micrometers on the electroplated copper layer in the openings in the photoresist layer, by electroplating a copper layer having a thickness between 2 and 30 micrometers on the copper layer serving as the seed layer, exposed by the openings in the photoresist layer, electroplating a nickel layer having a thickness between 0.5 and 10 micrometers on the electroplated copper layer in the openings in the photoresist layer and then electroplating a gold layer, platinum layer, palladium layer or ruthenium layer having a thickness between 0.05 and 2 micrometers on the electroplated nickel layer in the openings in the photoresist layer, or by electroplating a gold layer having a thickness between 2 and 30 micrometers on the gold layer serving as the seed layer, exposed by the openings in the photoresist layer. Thereafter, the photoresist layer may be removed. Thereafter, the seed layer not under the metal layer 8122 is removed using a wet-etching process or using a dry-etching process. Thereafter, the adhesion/barrier layer not under the metal layer 8122 is removed using a wet-etching process or using a dry-etching process.

[00364] After the patterned circuit layer 812 is formed, a polymer layer 99 can be formed by a suitable process or processes, e.g., by spin-on coating a negative photosensitive polyimide layer, such as ester type, on the patterned circuit layer 812 and on the polymer layer 98, exposing the spin-on coated photosensitive polyimide layer, developing the exposed polyimide layer and then curing the developed polyimide layer at the temperature between 265

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and 285°C for a time between 30 and 240 minutes in a nitrogen or oxygen-free ambient. Accordingly, an opening 9949' may be formed in the polymer layer 99, exposing a contact pad 8120 of the patterned circuit layer 812.

[00365] Referring to Fig. 14C, for forming a metal bump over the contact pad 8120, an adhesion/barrier layer may be formed by a suitable process or processes, e.g., by sputtering a titanium-containing layer, such as titanium layer or a titanium-tungsten-alloy layer, having a thickness between 1000 and 6000 angstroms, sputtering a chromium-containing layer, such as chromium layer, having a thickness between 1000 and 6000 angstroms, or sputtering a tantalum-containing layer, such as tantalum layer or tantalum-nitride layer, having a thickness between 1000 and 6000 angstroms, on the polymer layer 99 and on the contact pad 8120 exposed by the opening 9949'. Thereafter, the seed layer may be formed by a suitable process or processes, e.g., by sputtering a copper layer having a thickness between 200 and 3000 angstroms on the adhesion/barrier layer of any previously described material. Thereafter, a photoresist layer may be formed on the seed layer, multiple openings in the photoresist layer exposing the seed layer. Thereafter, the metal bump may be formed by a suitable process or processes, e.g., by electroplating a copper layer having a thickness between 0.5 and 10 micrometers on the copper layer serving as the seed layer, exposed by the openings in the photoresist layer, electroplating a nickel layer having a thickness between 0.5 and 10 micrometers on the electroplated copper layer in the openings in the photoresist layer, and then electroplating a tin-containing layer, such as a tin-lead alloy, a tin-silver alloy or a tin-silver-copper alloy, having a thickness between 60 and 200 micrometers on the electroplated nickel layer in the openings in the photoresist layer. Thereafter, the photoresist layer may be removed. Thereafter, the seed layer not under the metal bump is removed using a wet-etching process or using a dry-etching process. Thereafter, the adhesion/barrier layer not under the metal bump is removed using a wet-etching process or using a dry-etching process. Thereafter, the metal bump can be reflowed to be shaped like a ball. The metal bump can be connected to a printed circuit board, ceramic substrate or another semiconductor chip.

[00366] Referring to Fig. 14C, for forming another kind of metal bump over the contact pad 8120, an adhesion/barrier layer may be formed by a suitable process or processes, e.g., by sputtering a titanium-containing layer, such as titanium layer or a titanium-tungsten-alloy layer, having a thickness between 1000 and 6000 angstroms, or sputtering a tantalum-containing layer, such as tantalum layer or tantalum-nitride layer, having a thickness between 1000 and 6000 angstroms, on the polymer layer 99 and on the contact pad 8120 exposed by the opening

9949'. Thereafter, the seed layer may be formed by a suitable process or processes, e.g., by sputtering a gold layer having a thickness between 200 and 3000 angstroms on the adhesion/barrier layer of any previously described material. Thereafter, a photoresist layer may be formed on the seed layer, multiple openings in the photoresist layer exposing the seed layer. Thereafter, the metal bump may be formed by a suitable process or processes, e.g., by electroplating a gold layer having a thickness between 6 and 25 micrometers on the gold layer serving as the seed layer, exposed by the openings in the photoresist layer. Thereafter, the photoresist layer may be removed. Thereafter, the seed layer not under the metal bump is removed using a wet-etching process or using a dry-etching process. Thereafter, the adhesion/barrier layer not under the metal bump is removed using a wet-etching process or using a dry-etching process. The metal bump can be connected to a flexible substrate by a tape-automated bonding (TAB) process, or a glass substrate via anisotropic conductive film or paste (ACF or ACP).

[00367] Alternatively, referring to Fig. 14C, a nickel layer having a thickness between 0.05 and 2 micrometers can be electroless plated on the contact pad 8120 exposed by the opening 9949' in layer polymer layer 99, and a gold layer, platinum layer, palladium layer or ruthenium layer having a thickness between 0.05 and 2 micrometers can be electroless plated on the electroless plated nickel layer in the opening 9949' in the polymer layer 99. Thereafter, a gold wire can be bonded onto the electroless plated gold layer in the opening 9949' in the polymer layer 99 using a wirebonding process.

[00368] Alternatively, referring to Fig. 14C, a gold wire can be bonded onto a gold layer, platinum layer, palladium layer or ruthenium layer of the patterned circuit layer 812, exposed by the openings 9949' in the polymer layer 99 using a wirebonding process.

[00369] Alternatively, before the patterned circuit layer 821 is formed, a polymer layer can be optionally formed by a suitable process or processes, e.g., by spin-on coating a negative photosensitive polyimide layer, such as ester type, on the nitride layer of the passivation layer 5 and on the contact pads 6490', exposing the spin-on coated photosensitive polyimide layer, developing the exposed polyimide layer and then curing the developed polyimide layer at the temperature between 265 and 285°C for a time between 30 and 240 minutes in a nitrogen or oxygen-free ambient. Accordingly, multiple openings may be formed in the polymer layer, exposing multiple contact pads 6490' exposed by the openings 549', 521, 522 and 524 in the passivation layer 5. After the polymer layer is formed, the patterned circuit layer 821 can be

formed on the polymer layer and on the contact pads 6490' exposed by the openings 549', 521, 522 and 524. The adhesion/barrier layer of any previously described material may be sputtered on the polymer layer and on the contact pads 6490' exposed by the openings in the polymer layer.

[00370] Alternatively, the previously described power bus or plane 81P and the previously described ground bus or plane 82 can be connected to two ESD circuits 44 and 45, as shown in Fig. 12D. The previously described power bus or plane 81P may connect the power nodes Tp, Up, Vp and Wp of the internal circuits 21, 22, 23 and 24 and the power nodes Dp and Dp' of the ESD circuits 44 and 45. The previously described ground bus or plane 82 may connect the ground nodes Ts, Us, Vs and Ws of the internal circuits 21, 22, 23 and 24 and the ground nodes Dg and Dg' of the ESD circuits 44 and 45. The above mentioned power bus 81P shown in Fig. 12D, over the passivation layer 5, can be connected to the power nodes of the internal circuits 20 or other circuits in the previously described four embodiments provided with access to a power voltage Vdd. The above mentioned ground bus 82 shown in Fig. 12D, over the passivation layer 5, can be connected to the ground nodes of the internal circuits 20 or other circuits in the previously described four embodiments provided with access to a ground voltage Vss. Each of the ESD circuit 44 and 45 in the circuitry of Fig. 12D may be a reverse biased diode 4333, as shown in Fig. 12E, having an anode connected to the thick and wide ground bus or plane 82 and a cathode connected to the thick and wide power bus or plane 81P.

[00371] Referring to Figs. 12B-12D, 13B, 13C and 14B-14D, the shape of the openings 511, 512, 514, 521, 522, 524, 549 and 549' in the passivation layer 5 from a top perspective view may be round, square, rectangular or polygon. If the openings 511, 512, 514, 521, 522, 524, 549 and 549' are round, the openings 511, 512, 514, 521, 522, 524, 549 and 549' may have a diameter of between 0.1 and 200 microns, between 1 and 100 microns, or, preferably, between 0.1 and 30 microns. If the openings 511, 512, 514, 521, 522, 524, 549 and 549' are square, the openings 511, 512, 514, 521, 522, 524, 549 and 549' may have a width of between 0.1 and 200 microns, between 1 and 100 microns, or, preferably, between 0.1 and 30 microns. If the openings 511, 512, 514, 521, 522, 524, 549 and 549' are rectangular, the openings 511, 512, 514, 521, 522, 524, 549 and 549' may have a width of between 0.1 and 200 microns, between 1 and 100 microns, or, preferably, between 0.1 and 30 microns, and a length of between 1 micron and 1 centimeter. If the openings 511, 512, 514, 521, 522, 524, 549 and 549' are polygon having more than five sides, the openings 511, 512, 514, 521, 522, 524, 549 and 549' have a largest diagonal length of between 0.1 and 200 microns, between 1 and 100

microns, or, preferably, between 0.1 and 30 microns. Alternatively, the openings 511, 512, 514, 521, 522, 524, 549 and 549' have a largest transverse dimension of between 0.1 and 200 microns, between 1 and 100 microns, or, preferably, between 0.1 and 30 microns. In a case shown in Fig. 14D, the openings 511, 512, 514 and 549 have a width of between 0.1 and 30 microns, with the lower portion of the openings 9511, 9512, 9514 and 9549 in the polymer layer 95 having a width of between 20 and 100 microns. The openings 9511, 9512 and 9514 in the polymer layer 95 have lower portions having widths or transverse dimensions larger than those of the openings 511, 512 and 514 in the passivation layer 5 aligned with the openings 9511, 9512 and 9514, respectively. The openings 9511, 9512 and 9514 in the polymer layer 95 further expose the passivation layer 5 close to the openings 511, 512 and 514. The polymer layer 95 covers the peripheral region of the contact pad exposed by the opening 549 in the passivation layer 5, but the opening 9549 in the polymer layer 95 exposes the center region of the contact pad exposed by the openings 549 in the passivation layer 5. The width or transverse dimension of the opening 549 in the passivation layer 5 is larger than that of the opening 9549.

[00372] In Figs. 12B-12D, a dotted line 5 indicates the passivation layer, coarse traces indicate traces of an over-passivation scheme 102 formed over the passivation layer 5, and fine traces indicate traces formed under the passivation layer 5. In Figs. 13B and 13C, coarse traces indicate the traces of the over-passivation scheme 102 formed over the passivation layer 5, and fine traces indicate the traces formed under the passivation layer 5. The over-passivation scheme 102 shown in Fig. 14B includes the polymer layer 99 and the metal trace 81P provided by the patterned circuit layer 811, and the opening 9949 in the polymer layer 99 is over the contact point 8110 of the metal trace 81P and exposes it. The over-passivation scheme 102 shown in Fig. 14C includes the polymer layers 98 and 99, the metal trace 81P provided by the patterned circuit layer 812, and the metal trace 82 provided by the patterned circuit layer 821, and the opening 9849' in the polymer layer 98 is over the metal trace 82, and the opening 9949' in the polymer layer 99 is over the contact point 8120 of the patterned circuit layer 812 and exposes it. The over-passivation scheme 102 shown in Fig. 14D includes the polymer layers 95 and 99 and the metal trace 81P provided by the patterned circuit layer 811, and the openings 9549, 9511, 9512 and 9514 are in the polymer layer 95, and the opening 9949 in the polymer layer 99 is over the contact point 8110 of the metal trace 81P and exposes it.

Formation of an Over-Passivation Scheme

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[00373] A main characteristics of the over-passivation schemes in exemplary embodiments of this disclosure are thick metal layers each having a thickness larger than 1 micrometer, such as between 2 and 200 micrometers, and preferably between 2 and 30 micrometers, and thick dielectric layers each having a thickness larger than 2 micrometers, such as between 2 and 300 micrometers, and preferably between 2 and 30 micrometers.

[00374] Figs. 15C-15H show an embossing process to fabricate a patterned circuit layer 801 over the passivation layer 5 and on the polymer layer 95, which can be applied to all embodiments in this disclosure. Figs. 15I-15J show an embossing process to fabricate a patterned circuit layer 802 on the patterned circuit layer 801 and on the polymer layer 98, which can be applied to all embodiments in this disclosure. Figs. 15C-15G and Figs. 16A-16K show a double embossing process to fabricate one or more patterned circuit layers 801 and 802 over the passivation layer 5, which can be applied to all embodiments in this disclosure. A polymer layer 95 may be provided under the patterned circuit layer 801 and over the passivation layer 5. A polymer layer 98 may provided between the patterned circuit layers 801 and 802 and over the passivation layer 5. A polymer layer 19 may be provided over the patterned circuit layer 802 and over the passivation layer 5. Figs. 15A-15M and Figs. 16A-16M are based on the structure of Fig.10E in the third embodiment, and are used as examples to illustrate methods for forming the over-passivation scheme for all embodiments in this disclosure. In other words, the methods described and the specification specified in the following paragraphs can be applied to all metal traces, buses or planes 81, 81P, 82, 83, 83' and 85 and all metal layers 811, 821, 831, 812 and 832 in this disclosure.

[00375] Fig. 15A shows a starting material for the over-passivation process. The over-passivation process starts on a wafer 10 finalized to be cut into chips after the over-passivation scheme of the top post-passivation technology is formed on the wafer 10.

[00376] The semiconductor wafer 10 includes elements, as follows:

[00377] Reference number of 1 indicates a substrate, usually a silicon substrate, having a thickness between 600 and 1000 micrometers, between 50 micrometers and 1 millimeter or between 75 and 250 micrometers. The silicon substrate can be an intrinsic, a p-type, or an n-type silicon substrate. For a high performance chip, a SiGe or Silicon-On-Insulator (SOI) substrate can be used. A SiGe substrate includes an epitaxial layer on the surface of a silicon substrate. An SOI substrate includes an insulating layer (exemplary silicon oxide) on a silicon substrate, and a Si or SiGe epitaxial layer formed over the insulating layer.

[00378] Reference number of 2 indicates a device layer, usually a semiconductor device, in and/or on the substrate 1. The semiconductor device includes an MOS transistor 2', either an n-MOS or a p-MOS transistor. The MOS transistor includes a gate (usually a poly-silicon, a tungsten poylcide, a tungsten silicide, titanium silicide, cobalt silicide, or a salicide gate), a source, and a drain. Other devices are bipolar transistors, DMOS (Diffused MOS), LDMOS (Lateral Diffused MOS), CCD (Charged-Coupled Device), CMOS sensors, photo-sensitive diodes, resistors (formed by the polysilicon layer or the diffusion area in the silicon substrate). The devices form various circuits, such as CMOS circuits, NMOS circuits, PMOS circuits, BiCMOS circuits, CMOS sensor circuits, DMOS power circuits, or LDMOS circuits. The layer includes the internal circuits 20 (including 21, 22, 23 and 24) in all embodiments; the voltage regulator or converter circuit 41 in the first embodiment; the off-chip circuit 40 (including 42 and 43) in the third embodiment, and the ESD circuit 44 in the fourth embodiment.

[00379] Reference number of 6 indicates a fine-line scheme, including fine-line metal layers 60 and fine-line via plugs 60' in vias 30' of fine-line dielectric layers 30. The fine-line scheme 6 includes fine-line metal traces in all embodiments of this disclosure: (1) 611, 612, 614, 619, 619', 621, 622, 624 and 629 of the first embodiment; (2) 631, 632 and 634 of the second embodiment; (3) 631, 632, 634, 639, 639', 6391, 6391', 6311, 6321 and 6341 of the third embodiment; (4) 611, 612, 614, 649, 621, 622, 624 and 649' of the fourth embodiment. The fine-line metal layers 60 can be aluminum or copper layers, or more specifically, sputtered aluminum layers or damascene copper layers. The fine-line metal layers 60 can be (1) all fine-line metal layers are aluminum layers, (2) all fine-line metal layers are copper layers, (3) the bottom layers are aluminum layers and the top layers are copper layer, or (4) the bottom layers are copper layers and the top layers are aluminum layers. The fine-line metal layers 60 may have a thickness between 0.05 and 2 micrometers, and preferably between 0.2 and 1 micrometers, with horizontal design rules (the width) of lines or traces smaller than 1 micrometer, such as between 0.05 and 0.95 micrometers, or larger than 20 nanometers, such as between 20 nanometers and 15 micrometers, and preferably between 20 nanometers and 2 micrometers. The aluminum layer is usually formed by a suitable process or processes, e.g., by a physical vapor deposition (PVD) method, such as the sputtering method, and then patterned by depositing a photoresist layer with thickness between 0.1 and 4 micrometers, and preferably 0.3 and 2 micrometers, followed by a wet or dry etching, exemplary dry plasma etch (usually containing fluorine plasma). As an option, an adhesion/barrier (Ti, TiW, TiN or a composit layer of above metals) may be added under the aluminum layer, and/or an anti-reflection layer

(TiN) may be also added over the aluminum layer. The vias 30' are optionally filled with blanketed CVD tungsten deposition, followed by a chemical mechanical polishing (CMP) of the tungsten metal layer to form via plugs 60'. The copper layer is usually formed by a suitable process or processes, e.g., by a damascene process including an electroplating process as follows: (1) depositing a copper diffusion barrier layer (such as oxynitride or nitride layer of thickness between 0.05 and 0.25μm); (2) depositing a dielectric layer 30 of a thickness between 0.1 and 2.5μm, exemplary between 0.3 and 1.5μm by PECVD, spin-on coating, and/or High-Density Plasma (HDP) CVD methods; (3) patterning the dielectric layer 30 by depositing a photoresist layer with a thickness between 0.1 and 4μm, and preferably between 0.3 and 2μm, then exposing and developing the photoresist layer to form openings and/or trenches, and then stripping the photoresist layer; (4) depositing an adhesion/barrier layer and an electroplating seed layer by sputtering and/or CVD methods. The adhesion/barrier layer includes Ta, TaN, TiN, Ti or TiW or a composite layer formed by a suitable process or processes, e.g., by above materials. The electroplating seed layer, formed on the adhesion/barrier layer, is usually a copper layer formed by a suitable process or processes, e.g., by sputtering Cu or CVD copper or a CVD Cu followed by a sputtering Cu; (5) electroplating a copper layer over the electroplating seed layer to a thickness smaller than 1 micrometer, such as between 0.05 and 1 micrometers, and preferably between 0.2 and 1 micrometers; (6) removing the electroplated copper layer, the electroplating seed layer and the adhesion/barrier layer not in the openings or trenches of the dielectric layer 30 by polishing (exemplary chemical mechanical polishing, CMP) the wafer until the dielectric layer underlying the adhesion/barrier layer exposed. Only the metals in the openings or trenches remain after CMP; and the remained metals are used as metal conductors (lines, traces and/or planes) or via plugs 60' connecting two adjacent metal layers 60. As another alternative, a double-damascene process is used to form metal via plugs and metal traces, lines, or planes simultaneously with one electroplating process, one CMP process. Two photolithography processes, and two dielectric depositing processes are applied in the double-damascene process. The double-damascene process adds more process steps of deposing and patterning another layer of dielectrics between step (3) of patterning a dielectric layer and step (4) of depositing the metal layer in the above single damascene process. The dielectric layer 30 is formed by a suitable process or processes, e.g., by CVD (Chemical Vapor Deposition), PECVD (Plasma-Enhanced CVD), High-Density-Plasma (HDP) CVD, or a spin-on method. The materials of dielectric layers 30 include layers of silicon oxide, silicon nitride, silicon oxynitride, PECVD TEOS, Spin-On Glass (SOG, silicate-based or

siloxane-based), Fluorinated Silicate Glass (FSG), or a low-K dielectric material such as Black Diamond (generated by machines of Applied Materials, Inc.), or ULK CORAL (generated by machines of Novellus Inc.), or SiLK (of IBM Corp.) low k dielectrics. The PECVD silicon oxide or PECVD TEOS or HDP oxide has a dielectric constant K between 3.5 and 4.5; the PECVD FSG or HDP FSG has a K value between 3.0 and 3.5, and the low K dielectric material has a K value between 1.5 and 3.0. The low K dielectric material, such as Black Diamond, is porous, and includes hydrogen and carbon in addition to silicon and oxygen, the formula is $H_wC_xSi_yO_z$. The fine-line dielectric layers 30 usually include inorganic materials. The dielectric layers 30 may have a thickness between 0.05 and 2 micrometers. The vias 30' in the dielectric layer 30 is formed by a suitable process or processes, e.g., by wet and/or dry etching with photoresist patterning, exemplary dry etching. The dry etch species include fluorine plasma.

[00380] Reference number of 5 indicates a passivation layer. The passivation layer 5 plays a very important role in this disclosure. The passivation layer 5 is an insulating, protective layer that prevents mechanical and chemical damage during assembly and packaging. In addition to preventing mechanical scratch, it prevents the penetration of mobile ions, such as sodium, and transition metal, such as gold or copper, into the underlying IC devices. It also protects the underlying devices and interconnection (metals and dielectrics) from moisture penetration or other containments. The passivation layer 5 can be formed by a suitable process or processes, e.g., by a chemical vapor deposition (CVD) method, and typically has a thickness larger than 0.2 micrometers, such as between 0.3 and 1.5 micrometers or between 0.4 and 0.8 micrometers.

[00381] The passivation layer 5 can be composed of one or more inorganic layers. For example, the passivation layer 5 can be a composite layer of an oxide layer, such as silicon-oxide layer or silicon-oxycarbide (SiOC) layer, having a thickness smaller than 1.5 micrometers, such as between 0.1 and 1 micrometers, and preferably between 0.3 and 0.7 micrometers, and a nitride layer, such as silicon-nitride layer, silicon-oxynitride layer or silicon-carbon-nitride (SiCN) layer, having a thickness smaller than 1.5 micrometers, such as between 0.25 and 1.2 micrometers, and preferably between 0.35 and 1 micrometers, on the oxide layer. Alternatively, the passivation layer 5 can be a single layer of silicon nitride, silicon oxynitride or silicon carbon nitride (SiCN) having a thickness smaller than 1.5 micrometers, such as between 0.2 and 1.5 micrometers, and preferably between 0.3 and 1 micrometers. In a exemplary case, the passivation layer 5 includes a topmost inorganic layer of the

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semiconductor wafer 10, and the topmost inorganic layer of the semiconductor wafer 10 can be a silicon-nitride layer having a thickness larger than 0.2 micrometers, such as between 0.2 and 1.5 micrometers, or a silicon-oxide layer having a thickness larger than 0.2 micrometers, such as between 0.2 and 1.5 micrometers. Alternatively, the passivation layer 5 can be a composite layer of an oxynitride layer with a thickness smaller than 1 micrometer, such as between 0.05 and 0.35 micrometers, and preferably between 0.1 and 0.2 micrometers, a first oxide layer with a thickness smaller than 1.2 micrometers, such as between 0.2 and 1.2 micrometers, and preferably between 0.3 and 0.6 micrometers, on the oxynitride layer, a nitride layer, such as silicon-nitride layer, with a thickness smaller than 1.2 micrometers, such as between 0.2 and 1.2 micrometers, and preferably between 0.3 and 0.5 micrometers, on the first oxide layer, and a second oxide layer with a thickness smaller than 1.2 micrometers, such as between 0.2 and 1.2 micrometers, and preferably between 0.3 and 0.6 micrometers, on the nitride layer. The first and second oxide layers can be PECVD silicon oxide, PETEOS oxide or high-density plasma (HDP) oxide.

[00382] The above description and specification for the substrate 1, the device layer 2, the fine-line metal scheme 6, the dielectric layers 30 and the passivation layer 5 can be applied to all embodiments in this disclosure.

[00383] Openings 50 are formed in the passivation layer 5 by an etching process, such as a wet etching process or a dry etching process. The specification of the openings 50 and the process of forming the same can be applied to openings 511, 512, 514, 519, 519', 521, 522, 524, 529, 531, 532, 534, 534', 531', 532', 539, 539', 549, 549', 559 and 559' in this disclosure. The width of the opening 50 can be larger than 0.1 micrometers, such as between 0.1 and 200 micrometers, between 1 and 100 micrometers, between 0.5 and 30 micrometers or between 5 and 30 micrometers. The shape of the opening 50 from a top view may be a circle, and the diameter of the circle-shaped opening 50 may be larger than 0.1 micrometers, such as between 0.1 and 30 micrometers or between 30 and 200 micrometers. Alternatively, the shape of the opening 50 from a top view may be a square, and the width of the square-shaped opening 50 may be larger than 0.1 micrometers, such as between 0.1 and 30 micrometers or between 30 and 200 micrometers. Alternatively, the shape of the opening 50 from a top view may be a polygon, such as hexagon or octagon, and the polygon-shaped opening 50 may have a width larger than 0.1 micrometers, such as between 0.1 and 30 micrometers or between 30 and 200 micrometers. Alternatively, the shape of the opening 50 from a top view may be a rectangle, and the rectangle-shaped opening 50 may have a shorter width larger than 0.1 micrometers,

such as between 0.1 and 30 micrometers or between 30 and 200 micrometers. The width of the openings 531, 532, 534, 531', 532', 534', 511, 512 and 514 in the passivation layer 5 for the internal circuits 20 (including 21, 22, 23 and 24) may be larger than 0.1 micrometers, such as between 0.1 and 100 micrometers, and preferably between 0.1 and 30 micrometers. The openings 519, 519' and 529 for the voltage regulator or converter circuit 41, the openings 539 and 539' for the off-chip buffer 42 and the off-chip ESD circuit 43, and the openings 549, 549', 559 and 559' for the ESD circuit 44 may have a width larger than those of the openings 531, 532, 534, 511, 512 and 514, in a range between 1 and 150 micrometers, and preferably between 5 and 100 micrometers. Alternatively, the openings 519, 519' and 529 for the voltage regulator or converter circuit 41, the openings 539 and 539' for the off-chip buffer 42 and the off-chip ESD circuit 43, and the openings 549, 549', 559 and 559' for the ESD circuit 44 may have a width larger than those of the openings 531, 532 and 534, in a range between 0.1 and 30 micrometers. The openings 50 in the passivation layer 5 are over multiple regions of multiple metal pads or traces 600 of the fine-line metal layers 60 and expose them, and the regions of the metal pads or traces 600 are at bottoms of the openings 50. The metal pads or traces 600 may include aluminum or electroplated copper.

[00384] The wafer 10 can be fabricated using different generations of IC process technologies, such as 1 μm, 0.8 μm, 0.6 μm, 0.5 μm, 0.35 μm, 0.25 μm, 0.18 μm, 0.25 μm, 0.13 μm, 90 nm, 65 nm, 45 nm, 35 nm or 25 nm technologies, defined by the gate length or effective channel length of the MOS transistors 2'. The wafer 10 can be processed using photolithography process. The photolithography process can include coating, exposing and developing the photoresist. The photoresist used to process the wafer 10 has a thickness between 0.1 and 4 micrometers. A stepper or a scanner, e.g., a 5X stepper or scanner) can be used to expose the photoresist. The 5X means that the dimension on a photo mask (usual made of quartz) is reduced on the wafer when light beam is projected from the photo mask onto the wafer, and the dimension of a feature on the photo mask is 5 times of the dimension on the wafer. The scanner is used in advanced generations of IC process technologies, and is usually with 4X dimension reduction to improve the resolution. The wavelength of the light beam used in the stepper or the scanner can be 436 nm (g-line), 365 nm (i-line), 248 nm (Deep Ultraviolet, DUV), 193 nm (DUV), or 157 nm (DUV), or 13.5 nm (Extreme UV, EUV). The high-index immersion photolithography is also used to achieve fine-line features in the wafer 10.

[00385] The wafer 10 is preferably processed in a clean room with Class 10 or better, for example Class 1. A Class 10 clean room allows maximum number of particles per cubic foot: 1

larger than 1μm, 10 larger than 0.5μm, 30 larger than 0.3μm, 75 larger than 0.2μm, 350 larger than 0.1μm, while a Class 1 clean room allows maximum number of particles per cubic foot: 1 larger than 0.5μm, 3 larger than 0.3μm, 7 larger than 0.2μm, 35 larger than 0.1μm.

[00386] When copper is used as the fine-line metal layers 60, and exposed by the openings 50 in the passivation layer 5, a metal cap 66, including 661, 662, 664, 669 and 669', is preferably used to protect the exposed copper pad or trace from corrosion as shown in Fig. 15B. The metal cap 66 having a thickness between 0.4 and 3 micrometers includes an aluminum-containing layer (such as aluminum layer, aluminum-copper alloy layer or Al-Si-Cu alloy layer), a gold layer, a Ti layer, a TiW layer, a Ta layer, a TaN layer, or a Ni layer. If the metal cap 66 is an aluminum-containing layer (such as aluminum layer, aluminum-copper alloy layer or Al-Si-Cu alloy layer), a barrier layer having a thickness between 0.01 and 0.7 micrometers is formed between the aluminum cap 66 and the copper pad or trace, and the barrier layer includes Ti, TiW, TiN, Ta, TaN, Cr or Ni. For example, a barrier layer having a thickness between 0.01 and 0.7 micrometers can be formed on the copper pad or trace exposed by the opening 50, and an aluminum-containing layer having a thickness between 0.4 and 3 micrometers is formed on the barrier layer, and the barrier layer may be made of titanium, a titanium-tungsten alloy, titanium nitride, tantalum, tantalum nitride, chromium or alloy of refractory metal, and the aluminum-containing layer may be an aluminum layer, an aluminum-copper alloy layer or an Al-Si-Cu alloy layer. The wafer or chip with metal caps 66 can be used as options in all embodiments in this disclosure.

[00387] Figs. 15C-15K show process steps of fabricating an over-passivation scheme 102 over the wafer 10 shown in Fig. 15A or Fig 15B. The process steps shown in Figs. 15C-15K are used to form the structure shown in Fig. 10E, for example, with two layers of over-passivation metals, and with complete design architecture for interconnecting the internal circuits 20 and off-chip circuits 40. This example shows two over-passivation metal layers, while one metal layer, three metal layers, four metal layers or more metal layers over the passivation layer 5 can be formed using the same or similar methods, and the same or similar specification described in Figs. 15C-15K. In other words, the following description and specification apply to all embodiments in this disclosure.

[00388] Referring to Fig. 15K, the over-passivation scheme 102 can be formed over the wafer 10 described in Fig. 15A or Fig. 15B. The over-passivation scheme 102 includes over-passivation metals 80 and over-passivation polymers or insulators 90. The

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over-passivation metals 80 include one, two, three, four or more metal layers. In the example of including two metal layers, the over-passivation metals 80 include a first metal layer 801 and a second metal layer 802. The specification of the metal layer 801 and the process of forming the same can be applied to the metal layers 811, 821 and 831 in the disclosure, and the specification of the metal layer 802 and the process of forming the same can be applied to the metal layers 812 and 832 in the disclosure.

[00389] The metals used in the over-passivation metal layers 80 are mainly copper, gold, silver, palladium, rhodium, platinum, ruthenium, and nickel. The metal line, trace, or plane in the over-passivation metal scheme 80 usually includes composite layers of metals in a stack. The cross-section in Fig. 15K shows two composite layers 8001 and 8002 in each of the over-passivation metal layers 80, which can be applied to as the two composite layers 8111 and 8112 of the patterned circuit layer 811, respectively, as the two composite layers 8211 and 8212 of the patterned circuit layer 821, respectively, as the two composite layers 8121 and 8122 of the patterned circuit layer 812, respectively, as the two composite layers 8311 and 8312 of the patterned circuit layer 831, respectively, and as the two composite layers 8321 and 8322 of the patterned circuit layer 832, respectively.

[00390] The bottom layer of each over-passivation metal layers 80 is an adhesion/barrier/seed layer 8001 (including 8011 and 8021), including an adhesion/barrier layer (not shown) and a seed layer (not shown) on the adhesion/barrier layer. The specification of the adhesion/barrier/seed layers 8001 (including 8011 and 8021) and the process of forming the same can be applied to the adhesion/barrier/seed layers 8111, 8121, 8211, 8311 and 8321. The top layer of each over-passivation metal layers 80 is a bulk metal layer 8002, including 8012 and 8022. The specification of the bulk metal layers 8002 (including 8012 and 8022) and the process of forming the same can be applied to the bulk metal layers 8112, 8122, 8212, 8312 and 8322.

[00391] The material of the adhesion/barrier layer at the bottom of the adhesion/barrier/seed layer 8001 can be Ti (titanium), W, Co, Ni, TiN (titanium nitride), TiW (titanium-tungsten alloy), V, Cr (chromium), Cu, CrCu, Ta (tantalum), TaN (tantalum nitride), or alloy or composite layer of above materials. The adhesion/barrier layer can be formed by a suitable process or processes, e.g., by electroplating, electroless plating, chemical vapor deposition (CVD), or PVD (such as sputtering or evaporation), exemplary deposited by PVD (physical vapor deposition) such as metal sputtering process. The thickness of the

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adhesion/barrier layer is smaller than 1 micrometer, such as between 0.02 and 0.8 micrometers, and preferably between 0.05 and 0.5 micrometers.

[00392] For example, the adhesion/barrier layer at the bottom of the adhesion/barrier/seed layer 8011 may be formed by a suitable process or processes, e.g., by sputtering a titanium layer with a thickness between 0.02 and 0.8 micrometers, and preferably between 0.05 and 0.5 micrometers, on the polymer layer 95 and on the pads, principally made of aluminum, exposed by openings 950 in the polymer layer 95. Alternatively, the adhesion/barrier layer at the bottom of the adhesion/barrier/seed layer 8011 may be formed by a suitable process or processes, e.g., by sputtering a titanium-tungsten-alloy layer with a thickness of between 0.02 and 0.8μm, and preferably of between 0.05 and 0.5μm, on the polymer layer 95 and on the pads, principally made of aluminum, exposed by the openings 950 in the polymer layer 95. Alternatively, the adhesion/barrier layer at the bottom of the adhesion/barrier/seed layer 8011 may be formed by a suitable process or processes, e.g., by sputtering a titanium-nitride layer with a thickness of between 0.02 and 0.8μm, and preferably of between 0.05 and 0.5μm, on the polymer layer 95 and on the pads, principally made of aluminum, exposed by the openings 950 in the polymer layer 95. Alternatively, the adhesion/barrier layer at the bottom of the adhesion/barrier/seed layer 8011 may be formed by a suitable process or processes, e.g., by sputtering a chromium layer with a thickness of between 0.02 and 0.8μm, and preferably of between 0.05 and 0.5μm, on the polymer layer 95 and on the pads, principally made of aluminum, exposed by the openings 950 in the polymer layer 95. Alternatively, the adhesion/barrier layer at the bottom of the adhesion/barrier/seed layer 8011 may be formed by a suitable process or processes, e.g., by sputtering a tantalum-nitride layer with a thickness of between 0.02 and 0.8μm, and preferably of between 0.05 and 0.5μm, on the polymer layer 95 and on the pads, principally made of aluminum, exposed by the openings 950 in the polymer layer 95. Alternatively, the adhesion/barrier layer at the bottom of the adhesion/barrier/seed layer 8011 may be formed by a suitable process or processes, e.g., by sputtering a tantalum layer with a thickness of between 0.02 and 0.8μm, and preferably of between 0.05 and 0.5μm, on the polymer layer 95 and on the pads, principally made of aluminum, exposed by the openings 950 in the polymer layer 95.

[00393] For example, the adhesion/barrier layer at the bottom of the adhesion/barrier/seed layer 8011 may be formed by a suitable process or processes, e.g., by sputtering a titanium layer with a thickness of between 0.02 and 0.8μm, and preferably of between 0.05 and 0.5μm, on the polymer layer 95 and on the pads, principally made of copper,

exposed by the openings 950 in the polymer layer 95. Alternatively, the adhesion/barrier layer at the bottom of the adhesion/barrier/seed layer 8011 may be formed by a suitable process or processes, e.g., by sputtering a titanium-tungsten-alloy layer with a thickness of between 0.02 and 0.8μm, and preferably of between 0.05 and 0.5μm, on the polymer layer 95 and on the pads, principally made of copper, exposed by the openings 950 in the polymer layer 95. Alternatively, the adhesion/barrier layer at the bottom of the adhesion/barrier/seed layer 8011 may be formed by a suitable process or processes, e.g., by sputtering a titanium-nitride layer with a thickness of between 0.02 and 0.8μm, and preferably of between 0.05 and 0.5μm, on the polymer layer 95 and on the pads, principally made of copper, exposed by the openings 950 in the polymer layer 95. Alternatively, the adhesion/barrier layer at the bottom of the adhesion/barrier/seed layer 8011 may be formed by a suitable process or processes, e.g., by sputtering a chromium layer with a thickness of between 0.02 and 0.8μm, and preferably of between 0.05 and 0.5μm, on the polymer layer 95 and on the pads, principally made of copper, exposed by the openings 950 in the polymer layer 95. Alternatively, the adhesion/barrier layer at the bottom of the adhesion/barrier/seed layer 8011 may be formed by a suitable process or processes, e.g., by sputtering a tantalum-nitride layer with a thickness of between 0.02 and 0.8μm, and preferably of between 0.05 and 0.5μm, on the polymer layer 95 and on the pads, principally made of copper, exposed by the openings 950 in the polymer layer 95. Alternatively, the adhesion/barrier layer at the bottom of the adhesion/barrier/seed layer 8011 may be formed by a suitable process or processes, e.g., by sputtering a tantalum layer with a thickness of between 0.02 and 0.8μm, and preferably of between 0.05 and 0.5μm, on the polymer layer 95 and on the pads, principally made of copper, exposed by the openings 950 in the polymer layer 95.

[00394] For example, the adhesion/barrier layer at the bottom of the adhesion/barrier/seed layer 8011 may be formed by a suitable process or processes, e.g., by sputtering a titanium layer with a thickness of between 0.02 and 0.8μm, and preferably of between 0.05 and 0.5μm, on the polymer layer 95 and on the aluminum-containing layer (such as aluminum layer, aluminum-copper alloy layer or Al-Si-Cu alloy layer), exposed by the openings 950 in the polymer layer 95, of the metal caps 66 over the copper pads. Alternatively, the adhesion/barrier layer at the bottom of the adhesion/barrier/seed layer 8011 may be formed by a suitable process or processes, e.g., by sputtering a titanium-tungsten-alloy layer with a thickness of between 0.02 and 0.8μm, and preferably of between 0.05 and 0.5μm, on the polymer layer 95 and on the aluminum-containing layer (such as aluminum layer,

aluminum-copper alloy layer or Al-Si-Cu alloy layer) of the metal caps 66, exposed by the openings 950 in the polymer layer 95, over the copper pads. Alternatively, the adhesion/barrier layer at the bottom of the adhesion/barrier/seed layer 8011 may be formed by a suitable process or processes, e.g., by sputtering a titanium-nitride layer with a thickness of between 0.02 and 0.8μm, and preferably of between 0.05 and 0.5μm, on the polymer layer 95 and on the aluminum-containing layer (such as aluminum layer, aluminum-copper alloy layer or Al-Si-Cu alloy layer), exposed by the openings 950 in the polymer layer 95, of the metal caps 66 over the copper pads. Alternatively, the adhesion/barrier layer at the bottom of the adhesion/barrier/seed layer 8011 may be formed by a suitable process or processes, e.g., by sputtering a chromium layer with a thickness of between 0.02 and 0.8μm, and preferably of between 0.05 and 0.5μm, on the polymer layer 95 and on the aluminum-containing layer (such as aluminum layer, aluminum-copper alloy layer or Al-Si-Cu alloy layer) of the metal caps 66, exposed by the openings 950 in the polymer layer 95, over the copper pads. Alternatively, the adhesion/barrier layer at the bottom of the adhesion/barrier/seed layer 8011 may be formed by a suitable process or processes, e.g., by sputtering a tantalum-nitride layer with a thickness of between 0.02 and 0.8μm, and preferably of between 0.05 and 0.5μm, on the polymer layer 95 and on the aluminum-containing layer (such as aluminum layer, aluminum-copper alloy layer or Al-Si-Cu alloy layer), exposed by the openings 950 in the polymer layer 95, of the metal caps 66 over the copper pads. Alternatively, the adhesion/barrier layer at the bottom of the adhesion/barrier/seed layer 8011 may be formed by a suitable process or processes, e.g., by sputtering a tantalum layer with a thickness of between 0.02 and 0.8μm, and preferably of between 0.05 and 0.5μm, on the polymer layer 95 and on the aluminum-containing layer (such as aluminum layer, aluminum-copper alloy layer or Al-Si-Cu alloy layer) of the metal caps 66, exposed by the openings 950 in the polymer layer 95, over the copper pads.

[00395] For example, the adhesion/barrier layer at the bottom of the adhesion/barrier/seed layer 8021 may be formed by a suitable process or processes, e.g., by sputtering a titanium layer with a thickness of between 0.02 and 0.8μm, and preferably of between 0.05 and 0.5μm, on a polymer layer 98 and on a gold layer of the conduction bulk layer 8012 exposed by openings 980 in the polymer layer 98. Alternatively, the adhesion/barrier layer at the bottom of the adhesion/barrier/seed layer 8021 may be formed by a suitable process or processes, e.g., by sputtering a titanium-tungsten-alloy layer with a thickness of between 0.02 and 0.8μm, and preferably of between 0.05 and 0.5μm, on the polymer layer 98 and on the gold layer of the conduction bulk layer 8012 exposed by the

openings 980 in the polymer layer 98. Alternatively, the adhesion/barrier layer at the bottom of the adhesion/barrier/seed layer 8021 may be formed by a suitable process or processes, e.g., by sputtering a titanium-nitride layer with a thickness of between 0.02 and 0.8μm, and preferably of between 0.05 and 0.5μm, on the polymer layer 98 and on the gold layer of the conduction bulk layer 8012 exposed by the openings 980 in the polymer layer 98. Alternatively, the adhesion/barrier layer at the bottom of the adhesion/barrier/seed layer 8021 may be formed by a suitable process or processes, e.g., by sputtering a chromium layer with a thickness of between 0.02 and 0.8μm, and preferably of between 0.05 and 0.5μm, on the polymer layer 98 and on the gold layer of the conduction bulk layer 8012 exposed by the openings 980 in the polymer layer 98. Alternatively, the adhesion/barrier layer at the bottom of the adhesion/barrier/seed layer 8021 may be formed by a suitable process or processes, e.g., by sputtering a tantalum-nitride layer with a thickness of between 0.02 and 0.8μm, and preferably of between 0.05 and 0.5μm, on the polymer layer 98 and on the gold layer of the conduction bulk layer 8012 exposed by the openings 980 in the polymer layer 98. Alternatively, the adhesion/barrier layer at the bottom of the adhesion/barrier/seed layer 8021 may be formed by a suitable process or processes, e.g., by sputtering a tantalum layer with a thickness of between 0.02 and 0.8μm, and preferably of between 0.05 and 0.5μm, on the polymer layer 98 and on the gold layer of the conduction bulk layer 8012 exposed by the openings 980 in the polymer layer 98.

[00396] For example, the adhesion/barrier layer at the bottom of the adhesion/barrier/seed layer 8021 may be formed by a suitable process or processes, e.g., by sputtering a titanium layer with a thickness of between 0.02 and 0.8μm, and preferably of between 0.05 and 0.5μm, on a polymer layer 98 and on a copper layer of the conduction bulk layer 8012 exposed by multiple openings 980 in the polymer layer 98. Alternatively, the adhesion/barrier layer at the bottom of the adhesion/barrier/seed layer 8021 may be formed by a suitable process or processes, e.g., by sputtering a titanium-tungsten-alloy layer with a thickness of between 0.02 and 0.8μm, and preferably of between 0.05 and 0.5μm, on the polymer layer 98 and on the copper layer of the conduction bulk layer 8012 exposed by the openings 980 in the polymer layer 98. Alternatively, the adhesion/barrier layer at the bottom of the adhesion/barrier/seed layer 8021 may be formed by a suitable process or processes, e.g., by sputtering a titanium-nitride layer with a thickness of between 0.02 and 0.8μm, and preferably of between 0.05 and 0.5μm, on the polymer layer 98 and on the copper layer of the conduction bulk layer 8012 exposed by the openings 980 in the polymer layer 98. Alternatively, the

adhesion/barrier layer at the bottom of the adhesion/barrier/seed layer 8021 may be formed by a suitable process or processes, e.g., by sputtering a chromium layer with a thickness of between 0.02 and 0.8μm, and preferably of between 0.05 and 0.5μm, on the polymer layer 98 and on the copper layer of the conduction bulk layer 8012 exposed by the openings 980 in the polymer layer 98. Alternatively, the adhesion/barrier layer at the bottom of the adhesion/barrier/seed layer 8021 may be formed by a suitable process or processes, e.g., by sputtering a tantalum-nitride layer with a thickness of between 0.02 and 0.8μm, and preferably of between 0.05 and 0.5μm, on the polymer layer 98 and on the copper layer of the conduction bulk layer 8012 exposed by the openings 980 in the polymer layer 98. Alternatively, the adhesion/barrier layer at the bottom of the adhesion/barrier/seed layer 8021 may be formed by a suitable process or processes, e.g., by sputtering a tantalum layer with a thickness of between 0.02 and 0.8μm, and preferably of between 0.05 and 0.5μm, on the polymer layer 98 and on the copper layer of the conduction bulk layer 8012 exposed by the openings 980 in the polymer layer 98.

[00397] The seed layer at the top of the adhesion/barrier/seed layer 8001, for the subsequent electroplating process, usually formed by a suitable process or processes, e.g., by electroplating, electroless, CVD, or PVD (such as sputtering), exemplary deposited by PVD such as metal sputtering process. The material used for the seed layer, usually made of the same metal material as the conduction bulk metal formed in the subsequent electroplating process, can be Au, Cu, Ag, Ni, Pd, Rh, Pt or Ru. The material of the seed layer varies with the material of the electroplated metal layer formed on the seed layer. When a gold layer is to be electroplated on the seed layer, gold is a preferable material to the seed layer. When a copper layer is to be electroplated on the seed layer, copper is a preferable material to the seed layer. The thickness of the electroplating seed layer is between 0.05 and 1.2μm, exemplary between 0.05 and 0.8μm.

[00398] For example, when the adhesion/barrier layer at the bottom of the adhesion/barrier/seed layer 8001 is formed by a suitable process or processes, e.g., by sputtering a titanium layer with a thickness of between 0.02 and 0.8μm, and preferably of between 0.05 and 0.5μm, the seed layer at the top of the adhesion/barrier/seed layer 8001 can be formed by a suitable process or processes, e.g., by sputtering a gold layer with a thickness of between 0.05 and 1.2μm, and preferably of between 0.05 and 0.8μm, on the titanium layer. When the adhesion/barrier layer at the bottom of the adhesion/barrier/seed layer 8001 is formed by a suitable process or processes, e.g., by sputtering a titanium-tungsten-alloy layer

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with a thickness of between 0.02 and 0.8μm, and preferably of between 0.05 and 0.5μm, the seed layer at the top of the adhesion/barrier/seed layer 8001 can be formed by a suitable process or processes, e.g., by sputtering a gold layer with a thickness of between 0.05 and 1.2μm, and preferably of between 0.05 and 0.8μm, on the titanium-tungsten-alloy layer. When the adhesion/barrier layer at the bottom of the adhesion/barrier/seed layer 8001 is formed by a suitable process or processes, e.g., by sputtering a titanium-nitride layer with a thickness of between 0.02 and 0.8μm, and preferably of between 0.05 and 0.5μm, the seed layer at the top of the adhesion/barrier/seed layer 8001 can be formed by a suitable process or processes, e.g., by sputtering a gold layer with a thickness of between 0.05 and 1.2μm, and preferably of between 0.05 and 0.8μm, on the titanium-nitride layer. When the adhesion/barrier layer at the bottom of the adhesion/barrier/seed layer 8001 is formed by a suitable process or processes, e.g., by sputtering a chromium layer with a thickness of between 0.02 and 0.8μm, and preferably of between 0.05 and 0.5μm, the seed layer at the top of the adhesion/barrier/seed layer 8001 can be formed by a suitable process or processes, e.g., by sputtering a gold layer with a thickness of between 0.05 and 1.2μm, and preferably of between 0.05 and 0.8μm, on the chromium layer. When the adhesion/barrier layer at the bottom of the adhesion/barrier/seed layer 8001 is formed by a suitable process or processes, e.g., by sputtering a tantalum-nitride layer with a thickness of between 0.02 and 0.8μm, and preferably of between 0.05 and 0.5μm, the seed layer at the top of the adhesion/barrier/seed layer 8001 can be formed by a suitable process or processes, e.g., by sputtering a gold layer with a thickness of between 0.05 and 1.2μm, and preferably of between 0.05 and 0.8μm, on the tantalum-nitride layer. When the adhesion/barrier layer at the bottom of the adhesion/barrier/seed layer 8001 is formed by a suitable process or processes, e.g., by sputtering a tantalum layer with a thickness of between 0.02 and 0.8μm, and preferably of between 0.05 and 0.5μm, the seed layer at the top of the adhesion/barrier/seed layer 8001 can be formed by a suitable process or processes, e.g., by sputtering a gold layer with a thickness of between 0.05 and 1.2μm, and preferably of between 0.05 and 0.8μm, on the tantalum layer.

[00399] For example, when the adhesion/barrier layer at the bottom of the adhesion/barrier/seed layer 8001 is formed by a suitable process or processes, e.g., by sputtering a titanium layer with a thickness of between 0.02 and 0.8μm, and preferably of between 0.05 and 0.5μm, the seed layer at the top of the adhesion/barrier/seed layer 8001 can be formed by a suitable process or processes, e.g., by sputtering a copper layer with a thickness of between 0.05 and 1.2μm, and preferably of between 0.05 and 0.8μm, on the titanium layer.

When the adhesion/barrier layer at the bottom of the adhesion/barrier/seed layer 8001 is formed by a suitable process or processes, e.g., by sputtering a titanium-tungsten-alloy layer with a thickness of between 0.02 and 0.8μm, and preferably of between 0.05 and 0.5μm, the seed layer at the top of the adhesion/barrier/seed layer 8001 can be formed by a suitable process or processes, e.g., by sputtering a copper layer with a thickness of between 0.05 and 1.2μm, and preferably of between 0.05 and 0.8μm, on the titanium-tungsten-alloy layer. When the adhesion/barrier layer at the bottom of the adhesion/barrier/seed layer 8001 is formed by a suitable process or processes, e.g., by sputtering a titanium-nitride layer with a thickness of between 0.02 and 0.8μm, and preferably of between 0.05 and 0.5μm, the seed layer at the top of the adhesion/barrier/seed layer 8001 can be formed by a suitable process or processes, e.g., by sputtering a copper layer with a thickness of between 0.05 and 1.2μm, and preferably of between 0.05 and 0.8μm, on the titanium-nitride layer. When the adhesion/barrier layer at the bottom of the adhesion/barrier/seed layer 8001 is formed by a suitable process or processes, e.g., by sputtering a chromium layer with a thickness of between 0.02 and 0.8μm, and preferably of between 0.05 and 0.5μm, the seed layer at the top of the adhesion/barrier/seed layer 8001 can be formed by a suitable process or processes, e.g., by sputtering a copper layer with a thickness of between 0.05 and 1.2μm, and preferably of between 0.05 and 0.8μm, on the chromium layer. When the adhesion/barrier layer at the bottom of the adhesion/barrier/seed layer 8001 is formed by a suitable process or processes, e.g., by sputtering a tantalum-nitride layer with a thickness of between 0.02 and 0.8μm, and preferably of between 0.05 and 0.5μm, the seed layer at the top of the adhesion/barrier/seed layer 8001 can be formed by a suitable process or processes, e.g., by sputtering a copper layer with a thickness of between 0.05 and 1.2μm, and preferably of between 0.05 and 0.8μm, on the tantalum-nitride layer. When the adhesion/barrier layer at the bottom of the adhesion/barrier/seed layer 8001 is formed by a suitable process or processes, e.g., by sputtering a tantalum layer with a thickness of between 0.02 and 0.8μm, and preferably of between 0.05 and 0.5μm, the seed layer at the top of the adhesion/barrier/seed layer 8001 can be formed by a suitable process or processes, e.g., by sputtering a copper layer with a thickness of between 0.05 and 1.2μm, and preferably of between 0.05 and 0.8μm, on the tantalum layer.

[00400] The conduction bulk layer 8002 is formed for the low resistance conduction, usually formed by a suitable process or processes, e.g., by electroplating, with a thickness between 2 and 100μm, exemplary between 3 and 20μm. The metal material of the conduction bulk layer 8002, formed by a suitable process or processes, e.g., by a process including an

electroplating process or an electroless plating process, includes Au, Cu, Ag, Ni, Pd, Rh, Pt or Ru.

[00401] For example, the conduction bulk layer 8002 may be formed by a suitable process or processes, e.g., by electroplating a gold layer with a thickness of between 2 and 100μm, and preferably of between 3 and 20μm, on the seed layer, made of gold, at the top of the adhesion/barrier/seed layer 8001. Alternatively, the conduction bulk layer 8002 may be formed by a suitable process or processes, e.g., by electroplating a copper layer with a thickness of between 2 and 100μm, and preferably of between 3 and 20μm, on the seed layer, made of copper, at the top of the adhesion/barrier/seed layer 8001. Alternatively, the conduction bulk layer 8002 may be formed by a suitable process or processes, e.g., by electroplating a copper layer with a thickness of between 1.5 and 90μm, and preferably of between 2.5 and 10μm, on the seed layer, made of copper, at the top of the adhesion/barrier/seed layer 8001, and then electroplating a gold layer with a thickness of between 0.5 and 10μm on the copper layer, and the thickness of the copper layer and the gold layer is between 2 and 100μm, and preferably of between 3 and 20μm. Alternatively, the conduction bulk layer 8002 may be formed by a suitable process or processes, e.g., by electroplating a copper layer with a thickness of between 3 and 20μm, and preferably of between 3 and 15μm, on the seed layer, made of copper, at the top of the adhesion/barrier/seed layer 8001, then electroplating a nickel layer with a thickness of between 0.5 and 5μm, and preferably of between 1 and 3μm, on the copper layer, and then electroplating a gold layer with a thickness of between 0.03 and 0.5μm, and preferably of between 0.05 and 0.1μm, on the nickel layer. Alternatively, the conduction bulk layer 8002 may be formed by a suitable process or processes, e.g., by electroplating a copper layer with a thickness of between 3 and 20μm, and preferably of between 3 and 15μm, on the seed layer, made of copper, at the top of the adhesion/barrier/seed layer 8001, then electroplating a nickel layer with a thickness of between 0.5 and 5μm, and preferably of between 1 and 3μm, on the copper layer, and then electroless plating a gold layer with a thickness of between 0.03 and 0.5μm, and preferably of between 0.05 and 0.1μm, on the nickel layer. Alternatively, the conduction bulk layer 8002 may be formed by a suitable process or processes, e.g., by electroplating a copper layer with a thickness of between 3 and 20μm, and preferably of between 3 and 15μm, on the seed layer, made of copper, at the top of the adhesion/barrier/seed layer 8001, then electroplating a nickel layer with a thickness of between 0.5 and 5μm, and preferably of between 1 and 3μm, on the copper layer, and then electroplating a palladium layer with a thickness of between 0.03 and

0.5μm, and preferably of between 0.05 and 0.1μm, on the nickel layer. Alternatively, the conduction bulk layer 8002 may be formed by a suitable process or processes, e.g., by electroplating a copper layer with a thickness of between 3 and 20μm, and preferably of between 3 and 15μm, on the seed layer, made of copper, at the top of the adhesion/barrier/seed layer 8001, then electroplating a nickel layer with a thickness of between 0.5 and 5μm, and preferably of between 1 and 3μm, on the copper layer, and then electroless plating a palladium layer with a thickness of between 0.03 and 0.5μm, and preferably of between 0.05 and 0.1μm, on the nickel layer.

[00402] As an option, a cap/barrier metal layer (not shown) for protection or diffusion barrier purpose is added. The cap/barrier layer can be formed by a suitable process or processes, e.g., by electroplating, electroless plating, CVD or PVD sputtered metal, exemplary deposited by electroplating. The thickness of the cap/barrier layer is of a range between 0.05 and 5μm, exemplary 0.5 and 3μm. The cap/barrier layer can be a Ni, Co or V layer. As another option, an assembly-contact layer (not shown) over the conduction bulk metal layer 8002 and the cap/barrier layer (not shown) for assembly or packaging purpose, especially for the top-most metal layer of the over-passivation metals 80 (in one or more metal layers with polymer dielectric between two adjacent metal layers).

[00403] Openings 990 (including 9919 and 9929 in the first embodiment, 9939 and 9939' in the third embodiment, 9949 and 9949' in the fourth embodiment) in the topmost polymer layer 99 expose the contact points 8000 (including the contact points 8110 and 8120 in the first embodiment, the contact points 8310 and 8320 in the third embodiment, and the contact points 8110 and 8120 in the fourth embodiment) of the topmost over-passivation metal layer. The assembly-contact metal layer is wirebondable and/or solder wettable used for wirebonding, gold connection, solder ball mounting, and/or solder connection. The assembly-contact metal layer can be Au, Ag, Pt, Pd, Rh or Ru. Joining to the assembly-contact metal layer exposed by the polymer openings 900 can be a bonding wire, a solder ball (solder ball mounting), a metal ball (metal ball mounting), a metal bumps on the other substrate or chip, a gold bump on the other substrate or chip, a metal post on the other substrate or chip, a copper post on the other substrate or chip.

[00404] The over-passivation metal lines, traces or planes can be, as some examples, one of the following stacks, from bottom to top: (1) TiW / sputtered seed Au / electroplated Au, (2) Ti / sputtered seed Au / electroplated Au, (3) Ta / sputtered seed Au / electroplated Au, (4) Cr /

sputtered seed Cu / electroplated Cu, (5) TiW / sputtered seed Cu / electroplated Cu, (6) Ta / sputtered seed Cu / electroplated Cu, (7) Ti / sputtered seed Cu / electroplated Cu, (8) Cr, TiW, Ti or Ta / sputtered seed Cu / electroplated Cu / electroplated Ni, (9) Cr, TiW, Ti or Ta / sputtered seed Cu / electroplated Cu / electroplated Ni / electroplated Au, Ag, Pt, Pd, Rh or Ru, (10) Cr, TiW, Ti or Ta / sputtered seed Cu / electroplated Cu / electroplated Ni / electroless Au, Ag, Pt, Pd, Rh or Ru. Each of over-passivation metal layers 80 has thickness between 2 and 150μm, exemplary between 3 and 20μm, with horizontal design rules (the width) of over-passivation metal lines or traces between 1 and 200μm, exemplary 2 and 50μm. An over-passivation metal plane is also exemplary, particularly for power, or ground plane, with a width larger than 200μm. The minimum space between two adjacent metal lines, traces and/or planes is between 1 and 500μm, exemplary 2 and 150μm.

[00405] In some application of this disclosure, the metal lines, traces or planes can only include sputtered aluminum with thickness between 2 and 6μm, exemplary between 3 and 5 μm, with an optional adhesion/barrier layer (including Ti, TiW, TiN, Ta or TaN layer) under the aluminum layer.

[00406] Referring to Fig. 15L, as an option, a contact structure 89 can be formed on the contact point 8000, exposed by the opening 990, of the over-passivation metal scheme 80. The contact structure 89 can be a metal bump, a solder bump, a solder ball, a gold bump, a copper bump, a metal pad, a solder pad, a gold pad, a metal post, a solder post, a gold post or a copper post. The contact structure 89 may include metal layers 891 and 89c. The metal layer 891 under the metal layer 89c includes Au, Ti, TiW, TiN, Cr, Cu, CrCu, Ta, TaN, Ni, NiV, V or Co layer, or composite layers of the above materials. The exemplary stacks of the contact structure 89 (including metal layers 891 and 89c), from the bottom to the top are (1) Ti / Au pad (Au layer thickness 1-10μm), (2) TiW / Au pad (Au layer thickness 1-10μm), (3) Ni / Au pad (Ni layer thickness 0.5-10μm, Au layer thickness 0.2-10μm), (4) Ti / Au bump (Au layer thickness 7-40μm), (5) TiW / Au bump (Au layer thickness 7-40μm), (6) Ni / Au bump (Ni layer thickness 0.5-10μm, Au layer thickness 7-40μm), (7) Ti, TiW or Cr / Cu / Ni / Au pad, (copper layer thickness 0.1-10μm, Au layer thickness 0.2-10μm), (8) Ti, TiW, Cr, CrCu or NiV / Cu / Ni / Au bump, (copper layer thickness 0.1-10μm, Au layer thickness 7-40μm), (9) Ti, TiW, Cr, CrCu or NiV / Cu / Ni / solder pad, (copper layer thickness 0.1-10μm, solder layer thickness 0.2-30μm), (10) Ti, TiW, Cr, CrCu or NiV / Cu / Ni / solder bump or solder ball, (copper layer thickness 0.1-10μm, solder layer thickness 10-500μm), (11) Ti, TiW, Cr, CrCu or NiV / Cu post, (copper layer thickness 10-300μm), (11) Ti, TiW, Cr, CrCu or NiV / Cu post /Ni, (copper layer

thickness 10-300μm), (12) Ti, TiW, Cr, CrCu or NiV / Cu post / Ni / Solder (copper layer thickness 10-300μm, solder layer thickness 1-20μm), (13) Ti, TiW, Cr, CrCu or NiV / Cu post / Ni / Solder (copper layer thickness 10-300μm, solder layer thickness 20-100μm). The assembly methods can be wirebonding, TAB bonding, chip-on-glass (COG), chip-on-board (COB), flip chip on BGA substrate, chip-on-film (COF), chip-on-chip stack interconnection, chip-on-Si-substrate stack interconnection and etc.

[00407] For example, the contact structure 89 may be formed by a suitable process or processes, e.g., by sputtering a titanium-containing layer, such as titanium layer or titanium-tungsten-alloy layer, with a thickness between 0.02 and 0.8μm, and preferably between 0.05 and 0.5μm, on the polymer layer 99 and on the contact point 8000 of copper, nickel or gold exposed by the opening 990, then sputtering a seed layer, made of gold, with a thickness between 0.05 and 1.2μm, and preferably between 0.05 and 0.8μm, on the titanium-containing layer, then spin-on coating a photoresist layer, such as positive-type photoresist layer, on the seed layer, then exposing the photoresist layer using a 1X stepper or 1X contact aligner with at least two of G-line having a wavelength ranging from, e.g., about 434 to 438nm, H-line having a wavelength ranging from, e.g., about 403 to 407nm, and I-line having a wavelength ranging from, e.g., about 363 to 367nm, illuminating the photoresist layer, that is, G-line and H-line, G-line and I-line, H-line and I-line, or G-line, H-line and I-line illuminate the photoresist layer, then developing the exposed photoresist layer, an opening in the developed photoresist layer exposing the seed layer over the contact point 8000, then removing the residual polymeric material or other contaminants from the seed layer with an O_2 plasma or a plasma containing fluorine of below 200PPM and oxygen, then electroplating a gold layer with a thickness between 1 and 10μm on the seed layer exposed by the opening in the photoresist layer, then removing the developed photoresist layer using an organic solution with amide, then removing the residual polymeric material or other contaminants from the seed layer and from the gold layer with an O_2 plasma or a plasma containing fluorine of below 200PPM and oxygen, then removing the seed layer not under the gold layer with a dry etching method or a wet etching method, and then removing the titanium-containing layer not under the gold layer with a dry etching method or a wet etching method. As to the wet etching method, the seed layer of gold can be etched with an iodine-containing solution, such as solution containing potassium iodide. When the titanium-containing layer is titanium layer, the titanium layer can be wet etched with a solution containing hydrogen fluoride. When the titanium-containing layer is titanium-tungsten-alloy layer, the titanium-tungsten-alloy layer can

be wet etched with a solution containing hydrogen peroxide. As to the dry etching method, the seed layer of gold can be removed with an ion milling process or with an Ar sputtering etching process, and the titanium-containing layer can be etched with a chlorine-containing plasma etching process or with an RIE process. Accordingly, the metal layer 891 can be formed of the titanium-containing layer and the seed layer, made of gold, on the titanium-containing layer, and the metal layer 89c can be formed of gold that is on the seed layer of the metal layer 891.

[00408] For example, the contact structure 89 may be formed by a suitable process or processes, e.g., by sputtering a titanium-containing layer, such as titanium layer or titanium-tungsten-alloy layer, with a thickness of between 0.02 and 0.8μm, and preferably of between 0.05 and 0.5μm, on the polymer layer 99 and on the contact point 8000 of copper, nickel or gold exposed by the opening 990, then sputtering a seed layer, made of copper, with a thickness of between 0.05 and 1.2μm, and preferably of between 0.05 and 0.8μm, on the titanium-containing layer, then spin-on coating a photoresist layer, such as positive-type photoresist layer, on the seed layer, then exposing the photoresist layer using a 1X stepper or 1X contact aligner with at least two of G-line having a wavelength ranging from, e.g., about 434 to 438nm, H-line having a wavelength ranging from, e.g., about 403 to 407nm, and I-line having a wavelength ranging from, e.g., about 363 to 367nm, illuminating the photoresist layer, that is, G-line and H-line, G-line and I-line, H-line and I-line, or G-line, H-line and I-line illuminate the photoresist layer, then developing the exposed photoresist layer, an opening in the developed photoresist layer exposing the seed layer over the contact point 8000, then removing the residual polymeric material or other contaminants from the seed layer with an O_2 plasma or a plasma containing fluorine of below 200PPM and oxygen, then electroplating a copper layer with a thickness of between 1 and 10μm, and preferably of between 1 and 5μm, on the seed layer exposed by the opening in the photoresist layer, then electroplating a nickel layer with a thickness of between 0.5 and 5μm, and preferably of between 0.5 and 1μm, on the copper layer in the opening, then electroplating a tin-containing layer, such as a tin-lead alloy, a tin-silver alloy or a tin-silver-copper alloy, with a thickness of between 50 and 150μm, and preferably of between 80 and 130μm, on the nickel layer in the opening, then removing the developed photoresist layer using an organic solution with amide, then removing the residual polymeric material or other contaminants from the seed layer and from the tin-containing layer with an O_2 plasma or a plasma containing fluorine of below 200PPM and oxygen, then removing the seed layer not under the copper layer with a dry etching method or a wet etching method, then removing the titanium-containing layer not under the copper layer with a dry

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etching method or a wet etching method, and then reflowing the tin-containing layer. As to the wet etching method, the seed layer of copper can be etched with a solution containing NH_4OH. When the titanium-containing layer is titanium layer, the titanium layer can be wet etched with a solution containing hydrogen fluoride. When the titanium-containing layer is titanium-tungsten-alloy layer, the titanium-tungsten-alloy layer can be wet etched with a solution containing hydrogen peroxide. As to the dry etching method, the seed layer of copper can be removed with an Ar sputtering etching process, and the titanium-containing layer can be etched with a chlorine-containing plasma etching process or with an RIE process. Accordingly, the metal layer 891 can be formed of the titanium-containing layer and the seed layer, made of copper, on the titanium-containing layer, and the metal layer 89c can be formed of the copper layer on the seed layer, the nickel layer on the copper layer, and the tin-containing layer on the nickel layer.

[00409] For example, the contact structure 89 may be formed by a suitable process or processes, e.g., by sputtering a chromium layer with a thickness of between 0.02 and 0.8μm, and preferably of between 0.05 and 0.5μm, on the polymer layer 99 and on the contact point 8000 of copper, nickel or gold exposed by the opening 990, then sputtering a seed layer, made of copper, with a thickness of between 0.05 and 1.2μm, and preferably of between 0.05 and 0.8μm, on the chromium layer, then spin-on coating a photoresist layer, such as positive-type photoresist layer, on the seed layer, then exposing the photoresist layer using a 1X stepper or 1X contact aligner with at least two of G-line having a wavelength ranging from, e.g., about 434 to 438nm, H-line having a wavelength ranging from, e.g., about 403 to 407nm, and I-line having a wavelength ranging from, e.g., about 363 to 367nm, illuminating the photoresist layer, that is, G-line and H-line, G-line and I-line, H-line and I-line, or G-line, H-line and I-line illuminate the photoresist layer, then developing the exposed photoresist layer, an opening in the developed photoresist layer exposing the seed layer over the contact point 8000, then removing the residual polymeric material or other contaminants from the seed layer with an O_2 plasma or a plasma containing fluorine of below 200PPM and oxygen, then electroplating a copper layer with a thickness of between 1 and 10μm, and preferably of between 1 and 5μm, on the seed layer exposed by the opening in the photoresist layer, then electroplating a nickel layer with a thickness of between 0.5 and 5μm, and preferably of between 0.5 and 1μm, on the copper layer in the opening, then electroplating a tin-containing layer, such as a tin-lead alloy, a tin-silver alloy or a tin-silver-copper alloy, with a thickness of between 50 and 150μm, and preferably of between 80 and 130μm, on the nickel layer in the opening, then removing the

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developed photoresist layer using an organic solution with amide, then removing the residual polymeric material or other contaminants from the seed layer and from the tin-containing layer with an O_2 plasma or a plasma containing fluorine of below 200PPM and oxygen, then removing the seed layer not under the copper layer with a dry etching method or a wet etching method, then removing the chromium layer not under the copper layer with a dry etching method or a wet etching method, and then reflowing the tin-containing layer. As to the wet etching method, the seed layer of copper can be etched with a solution containing NH_4OH, and the chromium layer can be etched with a solution containing potassium ferricyanide. As to the dry etching method, the seed layer of copper can be removed with an Ar sputtering etching process. Accordingly, the metal layer 891 can be formed of the chromium layer and the seed layer, made of copper, on the chromium layer, and the metal layer 89c can be formed of the copper layer on the seed layer, the nickel layer on the copper layer, and the tin-containing layer on the nickel layer.

[00410] For example, the contact structure 89 may be formed by a suitable process or processes, e.g., by sputtering a tantalum-containing layer, such as tantalum layer or tantalum-nitride layer, with a thickness of between 0.02 and 0.8μm, and preferably of between 0.05 and 0.5μm, on the polymer layer 99 and on the contact point 8000 of copper, nickel or gold exposed by the opening 990, then sputtering a seed layer, made of copper, with a thickness of between 0.05 and 1.2μm, and preferably of between 0.05 and 0.8μm, on the tantalum-containing layer, then spin-on coating a photoresist layer, such as positive-type photoresist layer, on the seed layer, then exposing the photoresist layer using a 1X stepper or 1X contact aligner with at least two of G-line having a wavelength ranging from, e.g., about 434 to 438nm, H-line having a wavelength ranging from, e.g., about 403 to 407nm, and I-line having a wavelength ranging from, e.g., about 363 to 367nm, illuminating the photoresist layer, that is, G-line and H-line, G-line and I-line, H-line and I-line, or G-line, H-line and I-line illuminate the photoresist layer, then developing the exposed photoresist layer, an opening in the developed photoresist layer exposing the seed layer over the contact point 8000, then removing the residual polymeric material or other contaminants from the seed layer with an O_2 plasma or a plasma containing fluorine of below 200PPM and oxygen, then electroplating a copper layer with a thickness of between 1 and 10μm, and preferably of between 1 and 5μm, on the seed layer exposed by the opening in the photoresist layer, then electroplating a nickel layer with a thickness of between 0.5 and 5μm, and preferably of between 0.5 and 1μm, on the copper layer in the opening, then electroplating a tin-containing layer, such as a tin-lead alloy, a

tin-silver alloy or a tin-silver-copper alloy, with a thickness between 50 and 150 micrometers, and preferably between 80 and 130 micrometers, on the nickel layer in the opening, then removing the developed photoresist layer using an organic solution with amide, then removing the residual polymeric material or other contaminants from the seed layer and from the tin-containing layer with an O_2 plasma or a plasma containing fluorine of below 200PPM and oxygen, then removing the seed layer not under the copper layer with a dry etching method or a wet etching method, then removing the tantalum-containing layer not under the copper layer with a dry etching method or a wet etching method, and then reflowing the tin-containing layer. As to the wet etching method, the seed layer of copper can be etched with a solution containing NH_4OH. As to the dry etching method, the seed layer of copper can be removed with an Ar sputtering etching process. Accordingly, the metal layer 891 can be formed of the tantalum-containing layer and the seed layer, made of copper, on the tantalum-containing layer, and the metal layer 89c can be formed of the copper layer on the seed layer, the nickel layer on the copper layer, and the tin-containing layer on the nickel layer.

[00411] For example, the contact structure 89 may be formed by a suitable process or processes, e.g., by sputtering a titanium-containing layer, such as titanium layer or titanium-tungsten-alloy layer, with a thickness between 0.02 and 0.8 micrometers, and preferably between 0.05 and 0.5 micrometers, on the polymer layer 99 and on the contact point 8000 of copper, nickel or gold exposed by the opening 990, then sputtering a seed layer, made of copper, with a thickness between 0.05 and 1.2 micrometers, and preferably between 0.05 and 0.8 micrometers, on the titanium-containing layer, then spin-on coating a photoresist layer, such as positive-type photoresist layer, on the seed layer, then exposing the photoresist layer using a 1X stepper or 1X contact aligner with at least two of G-line having a wavelength ranging from, e.g., about 434 to 438nm, H-line having a wavelength ranging from, e.g., about 403 to 407nm, and I-line having a wavelength ranging from, e.g., about 363 to 367nm, illuminating the photoresist layer, that is, G-line and H-line, G-line and I-line, H-line and I-line, or G-line, H-line and I-line illuminate the photoresist layer, then developing the exposed photoresist layer, an opening in the developed photoresist layer exposing the seed layer over the contact point 8000, then removing the residual polymeric material or other contaminants from the seed layer with an O_2 plasma or a plasma containing fluorine of below 200PPM and oxygen, then electroplating a nickel layer with a thickness of between 0.5 and 5μm, and preferably of between 0.5 and 1μm, on the seed layer exposed by the opening in the photoresist layer, then electroplating a tin-containing layer, such as a tin-lead alloy, a tin-silver alloy or a

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tin-silver-copper alloy, with a thickness of between 50 and 150μm, and preferably of between 80 and 130μm, on the nickel layer in the opening, then removing the developed photoresist layer using an organic solution with amide, then removing the residual polymeric material or other contaminants from the seed layer and from the tin-containing layer with an O_2 plasma or a plasma containing fluorine of below 200PPM and oxygen, then removing the seed layer not under the copper layer with a dry etching method or a wet etching method, then removing the titanium-containing layer not under the copper layer with a dry etching method or a wet etching method, and then reflowing the tin-containing layer. As to the wet etching method, the seed layer of copper can be etched with a solution containing NH_4OH. When the titanium-containing layer is titanium layer, the titanium layer can be wet etched with a solution containing hydrogen fluoride. When the titanium-containing layer is titanium-tungsten-alloy layer, the titanium-tungsten-alloy layer can be etched with a solution containing hydrogen peroxide. As to the dry etching method, the seed layer of copper can be removed with an Ar sputtering etching process, and the titanium-containing layer can be etched with a chlorine-containing plasma etching process or with an RIE process. Accordingly, the metal layer 891 can be formed of the titanium-containing layer and the seed layer, made of copper, on the titanium-containing layer, and the metal layer 89c can be formed of the nickel layer on the seed layer and the tin-containing layer on the nickel layer.

[00412] For example, the contact structure 89 may be formed by a suitable process or processes, e.g., by sputtering a chromium layer with a thickness of between 0.02 and 0.8μm, and preferably of between 0.05 and 0.5μm, on the polymer layer 99 and on contact point 8000 of copper, nickel or gold exposed by the opening 990, then sputtering a seed layer, made of copper, with a thickness of between 0.05 and 1.2μm, and preferably of between 0.05 and 0.8μm, on the chromium layer, then spin-on coating a photoresist layer, such as positive-type photoresist layer, on the seed layer, then exposing the photoresist layer using a 1X stepper or 1X contact aligner with at least two of G-line having a wavelength ranging from, e.g., about 434 to 438nm, H-line having a wavelength ranging from, e.g., about 403 to 407nm, and I-line having a wavelength ranging from, e.g., about 363 to 367nm, illuminating the photoresist layer, that is, G-line and H-line, G-line and I-line, H-line and I-line, or G-line, H-line and I-line illuminate the photoresist layer, then developing the exposed photoresist layer, an opening in the developed photoresist layer exposing the seed layer over the contact point 8000, then removing the residual polymeric material or other contaminants from the seed layer with an O_2 plasma or a plasma containing fluorine of below 200PPM and oxygen, then electroplating a

nickel layer with a thickness of between 0.5 and 5μm, and preferably of between 0.5 and 1μm, on the seed layer exposed by the opening in the photoresist layer, then electroplating a tin-containing layer, such as a tin-lead alloy, a tin-silver alloy or a tin-silver-copper alloy, with a thickness of between 50 and 150μm, and preferably of between 80 and 130μm, on the nickel layer in the opening, then removing the developed photoresist layer using an organic solution with amide, then removing the residual polymeric material or other contaminants from the seed layer and from the tin-containing layer with an O_2 plasma or a plasma containing fluorine of below 200PPM and oxygen, then removing the seed layer not under the copper layer with a dry etching method or a wet etching method, then removing the chromium layer not under the copper layer with a dry etching method or a wet etching method, and then reflowing the tin-containing layer. As to the wet etching method, the seed layer of copper can be etched with a solution containing NH_4OH, and the chromium layer can be etched with a solution containing potassium ferricyanide. As to the dry etching method, the seed layer of copper can be removed with an Ar sputtering etching process. Accordingly, the metal layer 891 can be formed of the chromium layer and the seed layer, made of copper, on the chromium layer, and the metal layer 89c can be formed of the nickel layer on the seed layer and the tin-containing layer on the nickel layer.

[00413] For example, the contact structure 89 may be formed by a suitable process or processes, e.g., by sputtering a tantalum-containing layer, such as tantalum layer or tantalum-nitride layer, with a thickness of between 0.02 and 0.8μm, and preferably of between 0.05 and 0.5μm, on the polymer layer 99 and on the contact point 8000 of copper, nickel or gold exposed by the opening 990, then sputtering a seed layer, made of copper, with a thickness of between 0.05 and 1.2μm, and preferably of between 0.05 and 0.8μm, on the tantalum-containing layer, then spin-on coating a photoresist layer, such as positive-type photoresist layer, on the seed layer, then exposing the photoresist layer using a 1X stepper or 1X contact aligner with at least two of G-line having a wavelength ranging from, e.g., about 434 to 438nm, H-line having a wavelength ranging from, e.g., about 403 to 407nm, and I-line having a wavelength ranging from, e.g., about 363 to 367nm, illuminating the photoresist layer, that is, G-line and H-line, G-line and I-line, H-line and I-line, or G-line, H-line and I-line illuminate the photoresist layer, then developing the exposed photoresist layer, an opening in the developed photoresist layer exposing the seed layer over the contact point 8000, then removing the residual polymeric material or other contaminants from the seed layer with an O_2 plasma or a plasma containing fluorine of below 200PPM and oxygen, then electroplating a

nickel layer with a thickness of between 0.5 and 5μm, and preferably of between 0.5 and 1μm, on the seed layer exposed by the opening in the photoresist layer, then electroplating a tin-containing layer, such as a tin-lead alloy, a tin-silver alloy or a tin-silver-copper alloy, with a thickness of between 50 and 150μm, and preferably of between 80 and 130μm, on the nickel layer in the opening, then removing the developed photoresist layer using an organic solution with amide, then removing the residual polymeric material or other contaminants from the seed layer and from the tin-containing layer with an O_2 plasma or a plasma containing fluorine of below 200PPM and oxygen, then removing the seed layer not under the copper layer with a dry etching method or a wet etching method, then removing the tantalum-containing layer not under the copper layer with a dry etching method or a wet etching method, and then reflowing the tin-containing layer. As to the wet etching method, the seed layer of copper can be etched with a solution containing NH_4OH. As to the dry etching method, the seed layer of copper can be removed with an Ar sputtering etching process. Accordingly, the metal layer 891 can be formed of the tantalum-containing layer and the seed layer, made of copper, on the tantalum-containing layer, and the metal layer 89c can be formed of the nickel layer on the seed layer and the tin-containing layer on the nickel layer.

[00414] There is another important feature of the over-passivation scheme 8: using polymer material as the dielectric or insulating layer 90, over, under or between the over-passivation metal layers 80. Referring to Fig. 15K, use of polymer layers 90 (including 95, 98 and 99 in all embodiments of this disclosure) provides the possibility of fabricating thicker than 2 μm dielectric layer. The thickness of the polymer layer 90 can be between 2 and 100μm, and preferably of between 3 and 30μm. The polymer layers 90 used in the over-passivation scheme 102 can be polyimide (PI), benzocyclobutene (BCB), elastomer (such as silicone), parylene, epoxy-based material (such as photoepoxy SU-8 supplied by Sotec Microsystems, Renens, Switzerland). A solder mask material used in the printing circuit board industry can be used as the cap layer 99 (the topmost polymer layer over all the over-passivation metal layers 80). A photosensitive polyimide can be used as the polymer layers 90 (including 95, 98 and 99 in all embodiments of this disclosure). Furthermore, the polymer layers 90 (including 95, 98 and 99 in all embodiments of this disclosure) can be a non-ionic polyimide, such as an ether-based polyimide, PIMEL™, supplied by Asahi Chemical, Japan. Copper does not diffuse or penetrate through the non-ionic polyimide, therefore, it is allowed to have a direct contact between copper and polyimide. With the non-ionic polyimide, spacing between copper lines or traces or planes in the over-passivation metal scheme 80 can be as close as 1μm, i.e. the

spacing between two metal traces or planes can be larger 1μm. Furthermore, no protection cap, such as nickel layer, over the copper layer is required for copper lines, traces or planes.

[00415] Referring to Fig. 15K now, openings 900 in the polymer layers 90 are formed for interconnection between different over-passivation metal layers 80, or for connection to the underlying fine-line metal layers 60, or for connection to an external circuits. The polymer openings 900 (including 950, 980 and 990) includes (1) 9919, 9929, 9829, 9519, 9519', 9511, 9512 and 9514 in the first embodiment; (2) 9831, 9834, 9531, 9532 and 9534 in the second embodiment; (3) 9939, 9939', 9839, 9831, 9834, 9539, 9539', 9531, 9532 and 9534 in the third embodiment; and (4) 9949, 9949', 9849', 9511, 9512, 9514 and 9549 in the fourth embodiment. The material of the polymer layers 90 can be a photo-sensitive or non-photo-sensitive. For the photo-sensitive polymer layers 90, the polymer openings 900 are defined and patterned by light exposure and developing. While for the non-photo-sensitive polymer layer 90, the openings 900 are defined by first coating a photoresist layer over the polymer layer, exposing and developing the photoresist to create openings in the photoresist, wet or dry etching the polymer layer exposed by the photoresist openings, creating openings 900 in the polymer layer 90, and then stripping the photoresist. The width of the polymer openings 900 is between 2 and 1,000μm, exemplary between 5 and 200μm. In some designs, the polymer layer 90 may be removed in a large with dimension larger than 1,000μm. The openings 900 are designed in circles, corner-rounded squares, rectangles, or polygons.

[00416] The polymer layer 95 is between the passivation layer 5 and the bottom-most over-passivation metal layer 801. Through openings 950 in the polymer layer 95, the signal, power (Vdd or Vcc) and/or ground (Vss) passes between the fine-line metal scheme 6 and the over-passivation metal scheme 80. The process for forming the openings 950 in the polymer layer 95 can be applied to the process for (1) forming the openings 9519, 9519', 9511, 9512 and 9514 in Fig. 3D in the polymer layer 95; (2) forming the openings 9531, 9532 and 9534 in Fig. 7D in the polymer layer 95; (3) forming the openings 9539, 9539', 9531, 9532 and 9534 in Figs. 10D, 10E, 10G, 10H and 10I in the polymer layer 95; or (4) forming the opening 9549, 9511, 9512 and 9514 in Fig. 14D in the polymer layer 95. The width of the polymer openings 9531, 9532, 9534, 9511, 9512 and 9514, aligned with the passivation openings 531, 532, 534, 511, 512 and 514, respectively, for the internal circuits 20 (including 21, 22, 23 and 24) is between 1 and 300μm, exemplary between 3 and 100μm. The width of the openings 9519 and 9519', aligned with the openings 519 and 519', respectively, for the voltage regulator or converter circuit 41, the width of the openings 9539 and 9539', aligned with the openings 539

and 539', respectively, for the off-chip circuit 40 (including 42 and 43), or the width of the opening 9549, aligned with the opening 549, respectively, for the ESD circuit 44 may be larger than those of the openings 9531, 9532, 9534, 9511, 9512 and 9514, in a range between 5 and 1,000 micrometers, exemplary 10 and 200 micrometers. Note that two types of stacked vias of a polymer opening 950 over a passivation opening 50. In a first type of stacked vias, the polymer openings, for example the opening 9531 shown in Fig. 10E, has a width larger than that of the underlying passivation opening 531 shown in Fig. 10E. The opening 9531 exposes a top surface of the passivation layer 5 adjacent to the contact pad 6390 exposed by the opening 531, in addition to exposing the contact pad 6390. In this case, a smaller passivation opening 531 can be formed; hence a smaller contact pad of the top-most fine-line metal layer 60 can be formed. This type of stacked vias allows higher routing density of the top-most fine-line metal layer 60. In a second type of stacked vias, the polymer openings, for example the opening 9539 shown in Fig. 10E, is smaller than the underlying passivation opening 539 shown in Fig. 10E. The polymer layer 95 covers a peripheral region of the contact pad 6390 exposed by the opening 539 and the passivation layer 5, an opening 9531 in the polymer layer 95 exposing a center region of the contact pad 6390 exposed by the opening 539. In this type, the polymer layer 95 covers the sidewall of the passivation openings. The sidewall of the polymer openings provides a gentle, better slope than the slope of the passivation opening sidewall, and resulting in a better step coverage for the subsequent metal sputtering for the adhesion/barrier/seed layer 8011. A better adhesion/barrier metal step coverage is important for the reliability of the chip, since it prevent the inter-metallic compound (IMC) from happening.

[00417] The openings 980 in the polymer layer 98 are between two over-passivation metal layers 801 and 802. The process for forming the openings 980 in the polymer layer 98 can be applied to the process for (1) forming the opening 9829 in Fig. 3C in the polymer layer 98; (2) forming the openings 9831 and 9834 in Fig. 7C in the polymer layer 98; (3) forming the openings 9831, 9834 and 9839 in Figs. 10C and 10E in the polymer layer 98; or (4) forming the opening 9849' in Fig. 14C in the polymer layer 98. The width of the polymer openings 9831 and 9834 for the internal circuits 20 (including 21, 22, 23 and 24) is between 1 and 300μm, exemplary between 3 and 100μm. The width of the polymer opening 9829 for the voltage regulator or converter circuit 41, the width of the polymer opening 9839 for the off-chip circuit 40 (including 42 and 43), or the width of the polymer opening 9849' for the ESD circuit 44 may be larger than those of the openings 9831 and 9834, in a range between 5 and 1,000μm, exemplary 10 and 200μm.

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[00418] The opening 990 in the cap polymer layer 99 exposes the contact point 8000 of the top-most metal layer 802 for connecting to the external circuits or for the probe contacting in chip testing. The process for forming the openings 990 in the polymer layer 99 can be applied to the process for (1) forming the opening 9919 in Figs. 3B and 3D in the polymer layer 99; (2) forming the opening 9929 in Fig. 3C in the polymer layer 99; (3) forming the opening 9939 in Figs. 10B, 10D, 10F, 10G, 10H and 10I in the polymer layer 99; (4) forming the opening 9939' in Figs. 10C and 10E in the polymer layer 99; (5) forming the opening 9949 in Figs. 14B and 14D in the polymer layer 99; or (6) forming the opening 9949' in Fig. 14C in the polymer layer 99. There are no openings in the cap polymer layer 99 for the internal circuits 20 (including 21, 22, 23 and 24) being connected to an external circuit. The width of the polymer openings 9919 and 9929 for the voltage regulator or converter circuit 41, the width of the polymer openings 9939 and 9939' for the off-chip circuit 40 (including 42 and 43), or the width of the polymer openings 9949 and 9949' for the ESD circuit 44, can be in a range between 5 and 1,000μm, exemplary 10 and 200μm.

[00419] The signal, power or ground stimuli in the over-passivation metal layers 80 of the over-passivation scheme 102 is delivered to the internal circuits 20, the voltage regulator or converter circuit 41, the off-chip circuits 40 or the ESD circuits 44 through the fine-line scheme 6. The fine-line metals 631, 632, 634, 639 and 639' shown in Fig. 15A can be composed of stacked via plugs 60', and preferably, the upper one may be directly over the lower one. . Alternative, the fine-line metal 632 may include a local fine-line metal layer 632c shown in Fig. 15A, and as well as in all embodiments of this disclosure.

[00420] The photolithography used to fabricate the over-passivation scheme 102 is significantly different from that of convention IC process. Similarly, the over-passivation photolithography process includes coating, exposing and developing the photoresist. Two types of photoresist are used to form the over-passivation scheme 8: (1) liquid photoresist, formed by a suitable process or processes, e.g., by one or multiple spin-on coating, or printing. The liquid photoresist has a thickness between 3 and 60μm, exemplary between 5 and 40μm; (2) dry-film photoresist, formed by a suitable process or processes, e.g., by a laminating method. The dry-film photoresist has a thickness between 30 and 300μm, exemplary between 50 and 150μm. The photoresist can be positive-type or negative-type, exemplary positive-type thick photoresist for better resolution. If the polymer is photo-sensitive, the same photolithography process for the photoresist can be applied to pattern the polymer. An aligner or 1X stepper exposes the photoresist. The 1X means that the dimension on a photo mask (usual made of

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quartz or glass) is reduced on the wafer when light beam is projected from the photo mask onto the wafer, and the dimension of a feature on the photo mask is the same of the dimension on the wafer. The wavelength of the light beam used in the aligner or 1X stepper can be a 436nm (g-line), 397nm (h-line), 365nm (i-line), g/h-line (combination of g-line and h-line), or g/h/i-line (combination of g-line, h-line and i-line). The g/h-line or g/h/i-line 1X stepper (or 1X aligner) provides strong light intensity for thick photoresist or thick photo-sensitive polymer exposure.

[00421] Sine the passivation layer 5 protects underlying MOS transistors and fine-line scheme 6 from the penetration of moisture, sodium or other mobile ions, gold, copper or other transition metals, the over-passivation scheme 102 on the wafer can be processed in a clean room with Class 10 or less stringent environment, for example Class 100. A Class 100 clean room allows maximum number of particles per cubic foot: 1 larger than 5μm, 10 larger than 1μm, 100 larger than 0.5μm, 300 larger than 0.3μm, 750 larger than 0.2μm, 3500 larger than 0.1μm.

[00422] The device layer 2 includes the internal circuits 20 (including 21, 22, 23 and 24) in all embodiments, the voltage regulator or converter circuit 41 in the first embodiment, the off-chip circuits 40 (including 42 and 43) in the third embodiment, and the ESD circuit 44 in the fourth embodiment.

[00423] An internal circuit or an internal circuit unit 20, including 21, 22, 23 and 24, in all embodiments of this disclosure, is defined as a circuit whose signal nodes are not connected to the external (outside the chip) circuits. If a signal of an internal circuit or internal circuit unit 20 needs to connect to an external circuit, it must go through an off-chip circuit first, for example, ESD circuits, off-chip drivers or off-chip receivers and/or other off-chip I/O circuits, before connecting to the external circuit. In other definition, the internal circuits or the internal circuit units 20 do not include off-chip circuits. The internal circuits or internal circuit units 20, including 21, 22, 23 and 24, in this disclosure may, in addition to a NOR gate and a NAND gate, be an inverter, an AND gate, an OR gate, an SRAM cell, a DRAM cell, a non-volatile memory cell, a flash memory cell, an EPROM cell, a ROM cell, a magnetic RAM (MRAM) cell, a sense amplifier, an operational amplifier, an adder, a multiplexer, a diplexer, a multiplier, an A/D converter, a D/A converter, or other CMOS, BiCMOS, and/or bipolar circuit, analog circuit, a CMOS sensor cell, or a photo-sensitive diode.

[00424] Moreover, an internal circuit or an internal circuit unit 20 can be defined by its peak input or output current, or it can be defined as its MOS transistor size, as discussed in the third embodiment. The off-chip circuits 40, including the off-chip buffer 42 and the off-chip ESD circuit 43, can also be defined by its peak input or output current, or defined as its MOS transistor size, also as discussed in the third embodiment. The definition of the internal circuit 20 and the off-chip circuit 40 apply to all other embodiments in this disclosure.

[00425] In a case, a gate of a MOS device may be connected to another gate of another MOS device through the above mentioned thick and wide metal trace, bus or plane 81, 81P, 82, 83, 83' or 85 over the passivation layer 5. In another case, a gate of a MOS device may be connected to a source of another MOS device through the above mentioned thick and wide metal trace, bus or plane 81, 81P, 82, 83, 83' or 85 over the passivation layer 5. In another case, a gate of a MOS device may be connected to a drain of another MOS device through the above mentioned thick and wide metal trace, bus or plane 81, 81P, 82, 83, 83' or 85 over the passivation layer 5. In another case, a source of a MOS device may be connected to another source of another MOS device through the above mentioned thick and wide metal trace, bus or plane 81, 81P, 82, 83, 83' or 85 over the passivation layer 5. In another case, a source of a MOS device may be connected to a drain of another MOS device through the above mentioned thick and wide metal trace, bus or plane 81, 81P, 82, 83, 83' or 85 over the passivation layer 5. In another case, a drain of a MOS device may be connected to another drain of another MOS device through the above mentioned thick and wide metal trace, bus or plane 81, 81P, 82, 83, 83' or 85 over the passivation layer 5.

[00426] In following paragraphs, the dimension of features and electrical characteristics are described and compared between metal lines or metal traces 80, 60 in the over-passivation scheme 102 and in the fine-line scheme 6 for exemplary embodiments in this disclosure:

[00427] (1). Thickness of metal lines, metal traces: Each of the over-passivation metal layers 80 has thickness between 2 and 150μm, exemplary between 3 and 20μm, while each of the fin-line metal layers 60 has thickness between 0.05 and 2μm, exemplary between 0.2 and 1μm. For an IC chip designed with embodiments in this disclosure, the thickness of an over-passivation metal line or metal trace is thicker than the thickness of any fine-line metal lines or metal traces, with the thickness ratio in a range between 2 and 250, exemplary between 4 and 20.

[00428] (2). Thickness of dielectric layers: Each of the over-passivation dielectric (usually an organic material, such as polymer) layers 90 has thickness between 2 and 150μm, exemplary between 3 and 30μm, while each of the fine-line dielectric (usually inorganic material, such as oxide or nitride) layers 30 has thickness between 0.05 and 2μm, exemplary between 0.2 and 1μm. For an IC chip designed with embodiments in this disclosure, the thickness of an over-passivation dielectric layer 90 (separated by two neighboring metal layers) is thicker than the thickness of any fine-line dielectric layer 30 (separated by two neighboring metal layers), with the thickness ratio in a range between 2 and 250, exemplary between 4 and 20.

[00429] (3). Sheet resistance and resistance of metal lines or metal traces: Sheet resistance of a metal line or metal trace is computed by dividing metal resistivity by metal thickness. The sheet resistance of a copper (5μm thick) over-passivation metal line or trace is about 4 milli-ohms per square, while for a gold (4μm thick) over-passivation metal line or trace is about 5.5 milli-ohms per square. The sheet resistance of an over-passivation metal line, or trace, or plane is in a range between 0.1 and 10 milli-ohms per square, exemplary between 1 and 7 milli-ohms per square. The sheet resistance of a sputtered aluminum (0.8μm thick) fine-line metal line or trace is about 35 milli-ohms per square, while for a damascene copper (0.9μm thick) fine-line metal line or trace is about 20 milli-ohms per square. The sheet resistance of a fine-line metal line, or trace, or plane is in a range between 10 and 400 milli-ohms per square, exemplary between 15 and 100 milli-ohms per square. The resistance per unit length of a metal line or trace is calculated by dividing the sheet resistance by its width. The horizontal design rules (the width) of over-passivation metal lines or traces between 1 and 200μm, exemplary 2 and 50μm, while the horizontal design rules (the width) of lines or traces between 20 nano-meter and 15μm, exemplary 20 nano-meter and 2μm. The resistance per mm of an over-passivation metal line or trace is between 2 milli-ohms per mm length and 5 ohms per mm length, exemplary between 50 milli-ohms per mm length and 2.5 ohms per mm length. The resistance per mm of a fine-line metal line or trace is between 1 ohm per mm length and 3,000 ohms per mm length, exemplary between 500 milli-ohms per mm length and 500 ohms per mm length. For an IC chip designed with embodiments in this disclosure, the resistance per unit length of an over-passivation metal line or metal trace is smaller than that of any fine-line metal lines or metal traces, with the ratio of resistance per unit length (fine-line to over-passivation) in a range between 3 and 250, exemplary between10 and 30.

[00430] (4). Capacitance per unit length of metal lines or metal traces: Capacitance per unit length is related to dielectric types, thickness, and metal line width, spacing, and thickness, and the surrounding metals in horizontal and vertical directions. The dielectric constant of polyimide is about 3.3; the dielectric constant of BCB is about 2.5. Fig. 20 shows an example of a typical over-passivation metal line or trace 802x with two neighboring metal lines or traces 802y and 802z on both sides on the same metal layer 802, and a metal line or trace 801w on a metal layer 801 under the metal layer 802, separating by a polymer layer 98. Similarly, Fig. 20 shows an example of a typical fine-line metal line or trace 602x with two neighboring metal lines or traces 602y and 602z on both sides on the same metal layer 602, and a metal line or trace 601w on a metal layer 601 under the metal layer 602, separating by a dielectric layer 30. The typical capacitance per unit length of the typical metal lines or traces 802x, 602x include three components: 1) plate capacitance, Cxw (pF/mm) which is a function of the metal width to dielectric thickness aspect ratio, 2) coupling capacitance, Ccx (= Cxy +Cxz), which is a function of the metal thickness to line spacing aspect ratio, and 3) fringing capacitance, Cfx (= Cfl +Cfr), which is a function of metal thickness, spacing, and dielectric thickness. The capacitance per mm of an over-passivation metal line or trace is between 0.1 pF (pico Farads) per mm length and 2 pF per mm length, exemplary between 0.3 pF per mm length and 1.5 pF per mm length. The capacitance per mm of a fine-line metal line or trace is between 0.2 pF per mm length and 4 pF per mm length, exemplary between 0.4 pF per mm length and 2 pF per mm length. For an IC chip designed with embodiments in this disclosure, the capacitance per unit length of an over-passivation metal line or metal trace is smaller than that of any fine-line metal lines or metal traces, with the ratio of capacitance per unit length (fine-line to over-passivation) in a range between 1.5 and 20, exemplary between 2 and 10. An over-passivation scheme 102 shown in Fig. 20 includes the polymer layers 95, 98 and 99, the patterned circuit layers 801 and 802, and the metal bump 89, and the openings 950 in the polymer layer 95 are over the regions of the metal pads or traces 600 exposed by the openings 50 in the passivation layer 5, and the opening 980 in the polymer layer 98 is over the patterned circuit layer 801, and the opening 990 in the polymer layer 99 is over the contact point 8000 of the patterned circuit layer 802, and the metal bump 89 is in the opening 990, on the contact point 8000 and on the polymer layer 99.

[00431] (5). RC constant of metal lines or metal traces: The signal propagation time on a metal line or metal trace is computed by the RC delay. Based on the description of previous two paragraphs (3) and (4), the RC delay in an over-passivation metal line or trace is in a range

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between 0.003 and 10 ps (pico second) per mm length, exemplary between 0.25 and 2 ps (pico second) per mm length; while the RC delay in a fine-line metal line or trace is in a range between 10 and 2,000 ps (pico second) per mm length, exemplary between 40 and 500 ps (pico second) per mm length. For an IC chip designed with embodiments in this disclosure, the RC propagation time per unit length of an over-passivation metal line or metal trace is smaller than that of any fine-line metal lines or metal traces, with the ratio of RC propagation delay time per unit length (fine-line to over-passivation) in a range between 5 and 500, exemplary between 10 and 30.

[00432] Figs. 15C-15K show the process steps to form the over-passivation scheme 102 on the wafer 10 shown in Fig. 15A or Fig. 15B. Each of the over-passivation metal layers 80 is formed by a suitable process or processes, e.g., by an embossing process (as contrast to the damascene copper process under the passivation layer 5).

[00433] Referring to Fig. 15C, a polymer layer 95 can be formed on the passivation layer 5 of the wafer 10. If the polymer layer 95 is in liquid form, it can be deposited by spin-on coating or printing. If the polymer layer 95 is a dry film, the dry film is formed by a suitable process or processes, e.g., by a laminating method. For a photo-sensitive polymer, the polymer layer 95 is exposed by light of an aligner or a 1X stepper through a photo mask. Multiple openings 950 in the polymer layer 95 are over the regions of the metal pads or traces 600 exposed by the openings 50 and expose them. If the polymer is non-photo-sensitive, a photolithography process using a photoresist is required to pattern the openings 950. A hard mask (such as a silicon oxide layer, not shown), with a slow differentiating etch rate during the polymer opening etch, may optionally be deposited on the polymer layer 95 before coating the photoresist. As an alternative, the patterned polymer layer 95 (that is a polymer layer with openings 950) can also be formed by a suitable process or processes, e.g., by screening printing methods using a metal screen with patterned holes. No exposure and developing are required in the screen-printing method. If the polymer layer 95 is a dry film, as another alternative, holes can be formed in a sheet of dry film before laminated on the wafer. No exposure and developing are required in this alternative.

[00434] For example, the polymer layer 95 can be formed by a suitable process or processes, e.g., by spin-on coating a negative-type photosensitive polyimide layer, containing ester-type precursor, having a thickness between 6 and 50 micrometers on the passivation layer 5 and on the metal pads or traces 600 exposed by the openings 50 in the passivation layer 5,

then baking the spin-on coated polyimide layer, then exposing the baked polyimide layer using a 1X stepper or 1X contact aligner with at least two of G-line having a wavelength ranging from, e.g., about 434 to 438nm, H-line having a wavelength ranging from, e.g., about 403 to 407nm, and I-line having a wavelength ranging from, e.g., about 363 to 367nm, illuminating the baked polyimide layer, that is, G-line and H-line, G-line and I-line, H-line and I-line, or G-line, H-line and I-line illuminate the baked polyimide layer, then developing the exposed polyimide layer to form multiple openings in the exposed polyimide layer exposing the metal pads re traces 600, then curing or heating the developed polyimide layer at a peak temperature of between 290 and 400°C for a time of between 20 and 150 minutes in a nitrogen ambient or in an oxygen-free ambient, the cured polyimide layer having a thickness between 3 and 25 micrometers, and then removing the residual polymeric material or other contaminants from the upper surfaces of the metal pads or traces 600 exposed by the openings in the polyimide layer with an O_2 plasma or a plasma containing fluorine of below 200PPM and oxygen, such that the polymer layer 95 can be patterned with the openings 950 in the polymer layer 95 exposing the metal pads or traces 600. Alternatively, the developed polyimide layer can be cured or heated at a temperature between 150 and 290°C, and preferably of between 260 and 280°C, for a time of between 20 and 150 minutes in a nitrogen ambient or in an oxygen-free ambient.

[00435] The polymer layer 95 between the bottom-most patterned metal layer 801 and the passivation layer 5 planarizes the surface of the passivation layer 5, and decouples the over-passivation metal scheme 80 from the underlying fine-line metal scheme 6, resulting in high electrical performance. In some applications, the polymer layer 95 may be omitted to for cost saving. Note that openings 950 are aligned with the passivation openings 50. Note also that the polymer openings 950 can be either larger or smaller than the passivation openings 50. As an alternative, regards to the wafer 10 in Fig. 15A, there are no openings in the passivation layer 5, next the polymer layer 95 is spin coated on the passivation layer 5, followed by forming the openings 950 in the polymer layer 95 exposing the passivation layer 5, and then forming the openings 50 in the passivation layer 5 under the openings 950, exposing the contact pads of the fine-line metal scheme 6. In this option, the polymer openings 950 are about the same size as the openings 50 in the passivation layer 5.

[00436] Figs. 15D-15H show an embossing process to form the patterned metal layer 801. Referring to Fig. 15D, after forming the polymer layer 95 illustrated in Fig. 15C, an adhesion/barrier/seed layer 8011 is formed on the polymer layer 95 and on the regions of the

metal pads or traces 600 exposed by the openings 950 in the polymer layer 95 by using a physical vapor deposition (PVD) process, such as sputtering process or evaporation process. The adhesion/barrier/seed layer 8011 includes an adhesion/barrier layer on the polymer layer 95 and on the regions of the metal pads or traces 600 exposed by the openings 950, and a seed layer on the adhesion/barrier layer. The material of the adhesion/barrier layer may include titanium, a titanium-tungsten alloy, titanium nitride, chromium, tantalum, tantalum nitride or a composite of the previously described materials, and the material of the seed layer may include copper, nickel, aluminum, gold, silver, platinum or palladium.

[00437] For example, when the adhesion/barrier layer of the adhesion/barrier/seed layer 8011 is formed by a suitable process or processes, e.g., by sputtering a titanium-containing layer, such as a single layer of titanium-tungsten alloy, titanium or titanium nitride, having a thickness smaller than 1 micrometer, such as between 0.005 and 0.8 micrometers, and preferably between 0.02 and 0.8 micrometers, on the polymer layer 95 and on the regions of the metal pads or traces 600 exposed by the openings 950, the seed layer of the adhesion/barrier/seed layer 8011 can be formed by a suitable process or processes, e.g., by sputtering a copper layer, a nickel layer, an aluminum layer, a gold layer, a silver layer, a platinum layer or a palladium layer with a thickness smaller than 1 micrometer, such as between 0.005 and 0.7 micrometers, and preferably between 0.05 and 0.2 micrometers, on the titanium-containing layer.

[00438] Alternatively, when the adhesion/barrier layer of the adhesion/barrier/seed layer 8011 is formed by a suitable process or processes, e.g., by sputtering a tantalum-containing layer, such as a single layer of tantalum or tantalum nitride, having a thickness smaller than 1 micrometer, such as between 0.005 and 0.8 micrometers, and preferably between 0.02 and 0.8 micrometers, on the polymer layer 95 and on the regions of the metal pads or traces 600 exposed by the openings 950, the seed layer of the adhesion/barrier/seed layer 8011 can be formed by a suitable process or processes, e.g., by sputtering a copper layer, a nickel layer, an aluminum layer, a gold layer, a silver layer, a platinum layer or a palladium layer with a thickness smaller than 1 micrometer, such as between 0.005 and 0.7 micrometers, and preferably between 0.05 and 0.2 micrometers, on the tantalum-containing layer.

[00439] Alternatively, when the adhesion/barrier layer of the adhesion/barrier/seed layer 8011 is formed by a suitable process or processes, e.g., by sputtering a chromium-containing layer, such as a single layer of chromium layer, having a thickness smaller than 1 micrometer,

such as between 0.005 and 0.8 micrometers, and preferably between 0.02 and 0.8 micrometers, on the polymer layer 95 and on the regions of the metal pads or traces 600 exposed by the openings 950, the seed layer of the adhesion/barrier/seed layer 8011 can be formed by a suitable process or processes, e.g., by sputtering a copper layer, a nickel layer, an aluminum layer, a gold layer, a silver layer, a platinum layer or a palladium layer with a thickness smaller than 1 micrometer, such as between 0.005 and 0.7 micrometers, and preferably between 0.05 and 0.2 micrometers, on the chromium-containing layer.

[00440] Referring to Fig. 15E, after forming the adhesion/barrier/seed layer 8011 illustrated in Fig. 15D, a photoresist layer 71 is formed on the seed layer of the adhesion/barrier/seed layer 8011, and multiple openings 710 in the photoresist layer 71 expose the seed layer of the adhesion/barrier/seed layer 8011. The openings 710 defined the metal lines, traces or planes to be formed in the subsequent process, and contacts in the polymer openings 950 and the passivation openings 50. The contacts are over and connected to the exposed fine-line metal pads or traces 600.

[00441] For example, the photoresist layer 71 can be formed by a suitable process or processes, e.g., by spin-on coating a positive-type photosensitive polymer layer on the seed layer of the adhesion/barrier/seed layer 8011, then exposing the photosensitive polymer layer using a 1X stepper or 1X contact aligner with at least two of G-line having a wavelength ranging from, e.g., about 434 to 438nm, H-line having a wavelength ranging from, e.g., about 403 to 407nm, and I-line having a wavelength ranging from, e.g., about 363 to 367nm, illuminating the photosensitive polymer layer, that is, G-line and H-line, G-line and I-line, H-line and I-line, or G-line, H-line and I-line illuminate the photosensitive polymer layer, then developing the exposed polymer layer, and then removing the residual polymeric material or other contaminants from the seed layer with an O_2 plasma or a plasma containing fluorine of below 200PPM and oxygen, such that the photoresist layer 71 can be patterned with the openings 710 exposing the seed layer of the adhesion/barrier/seed layer 8011.

[00442] Referring to Fig. 15F, a bulk metal layer 8012 can be formed on the seed layer, exposed by the openings 710 in the photoresist layer 71, of the adhesion/barrier/seed layer 8011 and in the openings 710 by a process including an electroplating process and/or an electroless plating process. The bulk metal layer 8012 may have a thickness larger than 2 micrometers, such as between 2 and 100 micrometers, and preferably between 3 and 20 micrometers, and larger than that of the adhesion/barrier/seed layer 8011 and that of each of the

fine-line metal layers 60, respectively. The bulk metal layer 8012 may have a width larger than 1 micrometer, such as between 5 and 150 micrometers, and preferably between 5 and 50 micrometers, and larger than that of each of the fine-line metal layers 60.

[00443] The bulk metal layer 8012 having a thickness larger than 2 micrometers, such as between 2 and 200 micrometers, between 2 and 50 micrometers or between 2 and 30 micrometers, may be a single layer of gold, copper, silver, aluminum, palladium, platinum, rhodium, ruthenium, rhenium or nickel, or a composite layer made of the previously described metals.

[00444] For example, the bulk metal layer 8012 can be composed of a single metal layer formed by a suitable process or processes, e.g., by electroplating a gold layer, to a thickness larger than 2 micrometers, such as between 2 and 50 micrometers, and preferably between 2 and 30 micrometers, in the openings 710 and on the seed layer, preferably the previously described gold layer, of the adhesion/barrier/seed layer 8011 exposed by the openings 710.

[00445] Alternatively, the bulk metal layer 8012 can be composed of a single metal layer formed by a suitable process or processes, e.g., by electroplating a copper layer, to a thickness larger than 2 micrometers, such as between 2 and 200 micrometers, and preferably between 2 and 30 micrometers, in the openings 710 and on the seed layer, preferably the previously described copper layer, of the adhesion/barrier/seed layer 8011 exposed by the openings 710.

[00446] Alternatively, the bulk metal layer 8012 can be composed of a single metal layer formed by a suitable process or processes, e.g., by electroplating a nickel layer, to a thickness larger than 2 micrometers, such as between 2 and 100 micrometers, and preferably between 2 and 30 micrometers, in the openings 710 and on the seed layer, preferably the previously described copper or nickel layer, of the adhesion/barrier/seed layer 8011 exposed by the openings 710.

[00447] Alternatively, the bulk metal layer 8012 can be composed of double metal layers formed by a suitable process or processes, e.g., by electroplating a copper layer, to a thickness larger than 2 micrometers, such as between 2 and 30 micrometers, and preferably between 3 and 15 micrometers, in the openings 710 and on the seed layer, preferably the previously described copper layer, of the adhesion/barrier/seed layer 8011 exposed by the openings 710, and then electroplating or electroless plating a gold layer, to a thickness larger than 0.5 micrometers, such as between 0.05 and 10 micrometers, and preferably between 0.5

and 1 micrometers, in the openings 710 and on the electroplated copper layer in the openings 710.

[00448] Alternatively, the bulk metal layer 8012 can be composed of triple metal layers formed by a suitable process or processes, e.g., by electroplating a copper layer, to a thickness larger than 2 micrometers, such as between 2 and 30 micrometers, and preferably between 3 and 15 micrometers, in the openings 710 and on the seed layer, preferably the previously described copper layer, of the adhesion/barrier/seed layer 8011 exposed by the openings 710, then electroplating or electroless plating a nickel layer, to a thickness larger than 0.5 micrometers, such as between 0.5 and 5 micrometers, and preferably between 1 and 3 micrometers, in the openings 710 and on the electroplated copper layer in the openings 710, and then electroplating or electroless plating a gold layer, a palladium layer or a platinum layer, to a thickness larger than 0.03 micrometers, such as between 0.03 and 0.5 micrometers, and preferably between 0.05 and 0.1 micrometers, in the openings 710 and on the electroplated or electroless plated nickel layer in the openings 710.

[00449] A cap/barrier layer (not shown) can be optionally formed by a suitable process or processes, e.g., by electroplating or electroless plating over the bulk metal layer 8012. An assembly/contact layer (not shown) can also be further formed, as an option also, over the bulk metal layer 8012 and the cap/barrier layer by electroplating or electroless plating. The assembly/contact layer can be a gold layer, a palladium layer or a ruthenium layer with a thickness between 0.01 and 5 micrometers.

[00450] Next, referring to Fig. 15G, the photoresist layer 71 is removed using an inorganic solution or using an organic solution with amide. However, some residuals from the photoresist layer 71 could remain on the bulk metal layer 8012 and on the seed layer of the adhesion/barrier/seed layer 8011. Thereafter, the residuals can be removed from the bulk metal layer 8012 and from the seed layer of the adhesion/barrier/seed layer 8011 with a plasma, such as O_2 plasma or plasma containing fluorine of below 200PPM and oxygen.

[00451] Referring to Fig. 15H, the adhesion/barrier/seed layer 8011 not under the bulk metal layer 8012 is then removed by self-aligned wet and/or dry etching. In the case of wet etching to remove the bottom metal layer 8011 not under the bulk metal layer 8012, an undercut 8011' with a sidewall of the bottom metal layer 8011 recessed from a sidewall of the bulk metal layer 8012 is formed. No undercut 8011' exists when an anisotropies dry etching is used to remove the bottom metal layer 8011 not under the bulk metal layer 8012.

[00452] For example, when the seed layer of the adhesion/barrier/seed layer 8011 is a gold layer, it can be etched with an iodine-containing solution, such as solution containing potassium iodide, with an ion milling process or with an Ar sputtering etching process. Alternatively, when the seed layer of the adhesion/barrier/seed layer 8011 is a copper layer, it can be etched with a solution containing NH_4OH or with an Ar sputtering etching process.

[00453] For example, when the adhesion/barrier layer of the adhesion/barrier/seed layer 8011 is a titanium-tungsten-alloy layer, it can be etched with a solution containing hydrogen peroxide, with a chlorine-containing plasma etching process or with an RIE process. Alternatively, when the adhesion/barrier layer of the adhesion/barrier/seed layer 8011 is a titanium layer, it can be etched with a solution containing hydrogen fluoride, with a chlorine-containing plasma etching process or with an RIE process. Alternatively, when the adhesion/barrier layer of the adhesion/barrier/seed layer 8011 is a chromium layer, it can be etched with a solution containing potassium ferricyanide.

[00454] Accordingly, the patterned circuit layer 801 composed of the metal layers 8011 and 8012 can be formed on the polymer layer 95 and on the regions of the metal pads or traces 600 exposed by the openings 950, and can be connected to the fine-line metal layers 60 through the openings 50 and 950. Alternatively, the polymer layer 95 can be omitted, that is, the adhesion/barrier layer of the adhesion/barrier/seed layer 8011 can be formed on the passivation layer 5 and on the regions of the metal pads or traces 600 exposed by the openings 50 in the passivation layer 5. After the step illustrated in Fig. 15H, the semiconductor wafer 10 can be optionally cut into a plurality of individual semiconductor chip by a die-sawing process.

[00455] An over-passivation scheme 102 shown in Fig. 15H includes the polymer layer 95 and the patterned circuit layer 801, and the openings 950 in the polymer layer 95 are over the regions of the metal pads or traces 600 exposed by the openings 50 in the passivation layer 5.

[00456] Figs. 15I and 15J show a process of forming the additional polymer layer 98 and patterned circuit layer 802 using the above mentioned process illustrated in Figs. 15C-15H. First, after the step illustrated in Fig. 15H, the polymer layer 98 is formed on the polymer layer 95 and on the bulk metal layer 8012 of the patterned circuit layer 801, and multiple openings 980 in the polymer layer 98 are over multiple regions of the bulk metal layer 8012 of the patterned circuit layer 801 and expose them. Next, an adhesion/barrier layer of an adhesion/barrier/seed layer 8021 is formed on the polymer layer 98 and on the regions of the

bulk metal layer 8012 exposed by the openings 980. Next, a seed layer of the adhesion/barrier/seed layer 8021 can be formed on the adhesion/barrier layer of the adhesion/barrier/seed layer 8021. Next, a photoresist layer is formed on the seed layer of the adhesion/barrier/seed layer 8021, and multiple openings in the photoresist layer expose the seed layer of the adhesion/barrier/seed layer 8021. Next, a bulk metal layer 8022 is formed on the seed layer of the adhesion/barrier/seed layer 8021 exposed by the openings in the photoresist layer. Next, the photoresist layer is removed using an inorganic solution or using an organic solution with amide. Next, the adhesion/barrier/seed layer 8021 not under the bulk metal layer 8022 is removed. The specification of the polymer layer 98, the adhesion/barrier/seed layer 8021 and the bulk metal layer 8022 as shown in Figs. 15I-15L can be referred to as the specification of the polymer layer 95, the adhesion/barrier/seed layer 8011 and the bulk metal layer 8012, respectively, as illustrated in Figs. 15C-15H. The process of forming the polymer layer 98 as shown in Figs. 15I-15J can be referred to as the process of forming the polymer layer 95 as illustrated in Figs. 15C-15H. The process of forming the adhesion/barrier/seed layer 8021 as shown in Figs. 15I-15J can be referred to as the process of forming the adhesion/barrier/seed layer 8011 as illustrated in Figs. 15C-15H. The process of forming the bulk metal layer 8022 as shown in Figs. 15I-15J can be referred to as the process of forming the bulk metal layer 8012 as illustrated in Figs. 15C-15H. The process illustrated in Figs. 15I and 15J can be repeated for forming one ore more polymer layer and one or more patterned circuit layer over the patterned circuit layer 802 and over the polymer layer 98.

[00457] Referring to Fig. 15K, after removing the adhesion/barrier/seed layer 8021 not under the bulk metal layer 8022 as illustrated in Fig. 15J, a polymer layer 99 can be formed on the bulk metal layer 8022 of the patterned circuit layer 802 and on the polymer layer 98 not covered by the patterned circuit layer 802. Multiple openings 990 (only one of them shown) in the polymer layer 99 can be over multiple contact points 8000 (only one of them shown) of the bulk metal layer 8022 of the patterned circuit layer 802 and expose the contact points 8000. In some applications, for example, in the gold over-passivation metal system used for the topmost patterned circuit layer 802, the polymer layer 99 may optionally be omitted. An over-passivation scheme 102 shown in Fig. 15K includes the polymer layers 95, 98 and 99, and the patterned circuit layers 801 and 802, and the openings 950 in the polymer layer 95 are over the regions of the metal pads or traces 600 exposed by the openings 50 in the passivation layer 5, and the openings 980 in the polymer layer 98 are over the patterned circuit layer 801, and

the opening 990 in the polymer layer 99 is over the contact point 8000 of the patterned circuit layer 802 and exposes it.

[00458] After forming the over-passivation scheme 102 of the top post-passivation technology shown in Fig. 15K, the semiconductor wafer 10 can be cut into a plurality of individual semiconductor chip by a die-sawing process. The contact points 8000 of the semiconductor chip cut from the semiconductor wafer 10 can be used for connecting to an external circuit by (1) wires (such as gold wires, aluminum wires or copper wires) of a wirebonding process; (2) bumps (such as gold bumps, copper bumps, solder bumps, nickel bumps or other metal bumps) on the other substrates (such as silicon chips, silicon substrates, ceramic substrates, organic substrates, BGA substrates, flexible substrates, flexible tapes or glass substrates). The bumps on the substrates have a height larger than 1 micrometer, such as between 1 and 30 micrometers, and preferably between 5 and 20 micrometers; (3) posts (such as gold posts, copper posts, solder posts, nickel posts or other metal posts) on the other substrates (such as silicon chips, silicon substrates, ceramic substrates, organic substrates, BGA substrates, flexible substrates, flexible tapes or glass substrates). The posts on the substrates have a height larger than 10 micrometers, such as between 10 and 200 micrometers, and preferably between 30 and 120 micrometers; (4) bumps (such as gold bumps, copper bumps, solder bumps, nickel bumps or other metal bumps) on the terminals of metal leads of a lead-frames or a flexible tape. The bumps on the metal leads have a height larger than 1 micrometer, such as between 1 and 30 micrometers, and preferably between 5 and 20 micrometers.

[00459] Alternatively, referring to Fig. 15L, after forming the structure shown in Fig. 15K, the contact structure 89 can be formed over the contact point 8000 for connection to an external circuit, such as ball-grid-array (BGA) substrate, printed circuit board, semiconductor chip, metal substrate, glass substrate or ceramic substrate. The contact structure 89 can be (1) solder pad (with a thickness between 0.1 and 30 micrometers, and preferably between 1 and 10 micrometers) or solder bump (with a height larger than 8 micrometers, such as between 10 and 200 micrometers, and preferably between 30 and 120 micrometers) formed by a suitable process or processes, e.g., by electroplating, or screen printing. A solder reflow process is required to form a ball-shaped solder ball. Solder pad or bump 89 may include high lead solder (PbSn, with Pb composition larger than 85% weight percentage), eutectic solder (PbSn, with ~37% Pb weight percentage, and ~63% Sn weight percentage), lead-free solder including SnAg or SnCuAg, bismuth or indium; (2) gold pads (with a thickness between 0.1 and 10

micrometers, and preferably between 1 and 5 micrometers) or gold bumps (with a height larger than 5 micrometers, such as between 5 and 40 micrometers, and preferably between 10 and 20 micrometers) formed by a suitable process or processes, e.g., by electroplating; (3) metal balls formed by a suitable process or processes, e.g., by ball mounting. The metal ball can be a solder ball, a copper ball with surface coating of a Ni layer, or a copper ball with surface coating of a Ni layer and a solder layer, or a copper ball with surface coating of a Ni layer and a gold layer. A diameter of the metal ball is between 10 and 500 micrometers, and preferably between 50 and 300 micrometers. A metal ball can be mounted directly on the contact point 8000 exposed by the polymer opening 990, or on the metal layer 891. The metal layer 891 formed for the metal ball mounting may include a composite layer of Ti/Ni, Ti/Cu/Ni, TiW/Ni, TiW/Cu/Ni, Ti/Ni/Au, Ti/Cu/Ni/Au, TiW/Ni/Au, TiW/Cu/Ni/Au, Ti/Cu/Ni/Pd, TiW/Cu/Ni/Pd, Cr/CrCu, NiV/Cu, NiV/Cu, NiV/Au, Ni/Au, Ni/Pd, all layers are from bottom to top. After the metal ball mounting, a solder reflow process is usually required. After forming the contact structure 89, the wafer 10 can be cut into a plurality of individual semiconductor chip by a die-sawing process for packaging or assembly to connect to external circuits. The assembly methods can be wirebonding (to pads on external organic, ceramic, glass, or silicon substrates, or to leads of a leadframe or a flexible tape), TAB bonding, tape-chip-carrier packaging (TCP), chip-on-glass (COG), chip-on-board (COB), chip-on-film (COF), flip chip on a BGA substrate, chip-on-flex, chip-on-chip stack interconnection or chip-on-Si-substrate stack interconnection.

[00460] An over-passivation scheme 102 shown in Fig. 15L includes the polymer layers 95, 98 and 99, the patterned circuit layers 801 and 802, and the contact structure 89, and the openings 950 in the polymer layer 95 are over the regions of the metal pads or traces 600 exposed by the openings 50 in the passivation layer 5, and the openings 980 in the polymer layer 98 are over the patterned circuit layer 801, and the opening 990 in the polymer layer 99 is over the contact point 8000 of the patterned circuit layer 802, and the contact structure 89 is in the opening 990, on the contact point 8000 and on the polymer layer 99.

[00461] Fig. 15M is a cross-sectional view showing a semiconductor wafer, which can be formed by a suitable process or processes, e.g., by the following steps. First, after the steps illustrated in Fig. 15A and 15C-15H, the polymer layer 98 is formed on the polymer layer 95 and on the bulk metal layer 8012 of the patterned circuit layer 801, and multiple openings 980 in the polymer layer 98 are over multiple regions 801a of the topmost layer of gold, copper, silver, aluminum, palladium, platinum, rhodium, ruthenium, rhenium or nickel of the previously described various the bulk metal layer 8012 and expose them. Next, a metal layer

89a can be formed on the polymer layer 98 and on the regions 801a of the topmost layer of gold, copper, silver, aluminum, palladium, platinum, rhodium, ruthenium, rhenium or nickel of the previously described various the bulk metal layer 8012 exposed by the openings 980. Next, a metal layer 89b can be formed on the metal layer 89a. The material of the metal layer 89a may include titanium, a titanium-tungsten alloy, titanium nitride, chromium, tantalum, tantalum nitride or a composite of the previously described materials, and the material of the metal layer 89b may include copper, nickel, aluminum, gold, silver, platinum or palladium. The metal layers 89a and 89b may be formed by a suitable process or processes, e.g., by a physical vapor deposition (PVD) process, such as sputtering process or evaporation process. The metal layer 89a may have a thickness smaller than 1 micrometer, such as between 0.02 and 0.5 micrometers, and preferably between 0.1 and 0.2 micrometers, and the metal layer 89b may have a thickness smaller than 1 micrometer, such as between 0.05 and 0.5 micrometers, and preferably between 0.08 and 0.15 micrometers.

[00462] For example, when the metal layer 89a is formed by a suitable process or processes, e.g., by sputtering a titanium-containing layer, such as a single layer of titanium-tungsten alloy, titanium or titanium nitride, having a thickness smaller than 1 micrometer, such as between 0.02 and 0.5 micrometers, and preferably between 0.1 and 0.2 micrometers, on the polymer layer 98 and on the regions 801a of the topmost layer of gold, copper, silver, aluminum, palladium, platinum, rhodium, ruthenium, rhenium or nickel of the previously described various the bulk metal layer 8012 exposed by the openings 980, the metal layer 89b can be formed by a suitable process or processes, e.g., by sputtering a copper layer, a nickel layer, an aluminum layer, a gold layer, a silver layer, a platinum layer or a palladium layer with a thickness smaller than 1 micrometer, such as between 0.05 and 0.5 micrometers, between 0.08 and 0.15 micrometers, between 0.1 and 1 micrometers or between 0.2 and 0.5 micrometers, on the titanium-containing layer.

[00463] Alternatively, when the metal layer 89a is formed by a suitable process or processes, e.g., by sputtering a tantalum-containing layer, such as a single layer of tantalum or tantalum nitride, having a thickness smaller than 1 micrometer, such as between 0.02 and 0.5 micrometers, and preferably between 0.1 and 0.2 micrometers, on the polymer layer 98 and on the regions 801a of the topmost layer of gold, copper, silver, aluminum, palladium, platinum, rhodium, ruthenium, rhenium or nickel of the previously described various the bulk metal layer 8012 exposed by the openings 980, the metal layer 89b can be formed by a suitable process or processes, e.g., by sputtering a copper layer, a nickel layer, an aluminum layer, a gold layer, a

silver layer, a platinum layer or a palladium layer with a thickness smaller than 1 micrometer, such as between 0.05 and 0.5 micrometers, between 0.08 and 0.15 micrometers, between 0.1 and 1 micrometers or between 0.2 and 0.5 micrometers, on the tantalum-containing layer.

[00464] Alternatively, when the metal layer 89a is formed by a suitable process or processes, e.g., by sputtering a chromium-containing layer, such as a single layer of chromium layer, having a thickness smaller than 1 micrometer, such as between 0.02 and 0.5 micrometers, and preferably between 0.1 and 0.2 micrometers, on the polymer layer 98 and on the regions 801a of the topmost layer of gold, copper, silver, aluminum, palladium, platinum, rhodium, ruthenium, rhenium or nickel of the previously described various the bulk metal layer 8012 exposed by the openings 980, the metal layer 89b can be formed by a suitable process or processes, e.g., by sputtering a copper layer, a nickel layer, an aluminum layer, a gold layer, a silver layer, a platinum layer or a palladium layer with a thickness smaller than 1 micrometer, such as between 0.05 and 0.5 micrometers, between 0.08 and 0.15 micrometers, between 0.1 and 1 micrometers or between 0.2 and 0.5 micrometers, on the chromium-containing layer.

[00465] After forming the metal layer 89b, a photoresist layer can be formed on the metal layer 89b, and multiple openings in the photoresist layer are over the regions 801a of the topmost layer of gold, copper, silver, aluminum, palladium, platinum, rhodium, ruthenium, rhenium or nickel of the previously described various the bulk metal layer 8012 exposed by the openings 980 and expose the metal layer 89b. Next, a metal layer 89c can be formed on the metal layer 89b exposed by the openings in the photoresist layer by a process including an electroplating process. The metal layer 89c may have a thickness larger than 3 micrometer, such as between 3 and 200 micrometers, and preferably between 5 and 100 micrometers, and larger than that of the metal layer 89b, that of the metal layer 89a and that of each of the fine-line metal layers 60, respectively. The metal layer 89c may have a width larger than 1 micrometer, such as between 5 and 200 micrometers, and preferably between 5 and 50 micrometers, and larger than that of each of the fine-line metal layers 60. The metal layer 89c may include copper, gold, nickel, aluminum, silver, platinum, solder or a composite of the previously described materials.

[00466] For example, the metal layer 89c can be composed of a single metal layer formed by a suitable process or processes, e.g., by electroplating a copper layer, to a thickness larger than 3 micrometers, such as between 10 and 150 micrometers, and preferably between

20 and 100 micrometers, on the metal layer 89b, preferably the previously described copper layer 89b, exposed by the openings in the photoresist layer.

[00467] Alternatively, the metal layer 89c can be composed of a single metal layer formed by a suitable process or processes, e.g., by electroplating a gold layer, to a thickness larger than 3 micrometers, such as between 5 and 150 micrometers, and preferably between 10 and 100 micrometers, on the metal layer 89b, preferably the previously described gold layer 89b, exposed by the openings in the photoresist layer.

[00468] Alternatively, the metal layer 89c can be composed of a single metal layer formed by a suitable process or processes, e.g., by electroplating a nickel layer, to a thickness larger than 3 micrometers, such as between 5 and 150 micrometers, and preferably between 10 and 100 micrometers, on the metal layer 89b, preferably the previously described copper layer or nickel layer 89b, exposed by the openings in the photoresist layer.

[00469] Alternatively, the metal layer 89c can be composed of a single metal layer formed by a suitable process or processes, e.g., by electroplating a solder layer, such as a bismuth-containing layer, an indium-containing layer or a tin-containing layer of a tin-lead alloy, a tin-silver alloy or a tin-silver-copper alloy, to a thickness larger than 5 micrometers, such as between 5 and 200 micrometers, and preferably between 10 and 150 micrometers, on the metal layer 89b, preferably the previously described copper layer or nickel layer 89b, exposed by the openings in the photoresist layer.

[00470] Alternatively, the metal layer 89c can be composed of triple metal layers formed by a suitable process or processes, e.g., by electroplating a copper layer, to a thickness larger than 1 micrometer, such as between 3 and 150 micrometers, and preferably between 5 and 100 micrometers, on the metal layer 89b, preferably the previously described copper layer 89b, exposed by the openings in the photoresist layer, next electroplating or electroless plating a nickel layer, to a thickness larger than 1 micrometer, such as between 1 and 15 micrometers, and preferably between 2 and 10 micrometers, on the electroplated copper layer in the openings in the photoresist layer, and then electroplating or electroless plating a gold layer or a palladium layer, to a thickness larger than 0.005 micrometers, such as between 0.005 and 10 micrometers, and preferably between 0.05 and 1 micrometers, on the electroplated or electroless plated nickel layer in the openings in the photoresist layer.

[00471] Alternatively, the metal layer 89c can be composed of triple metal layers formed by a suitable process or processes, e.g., by electroplating a copper layer, to a thickness larger

than 1 micrometer, such as between 5 and 150 micrometers, and preferably between 10 and 100 micrometers, on the metal layer 89b, preferably the previously described copper layer 89b, exposed by the openings in the photoresist layer, next electroplating or electroless plating a nickel layer, to a thickness larger than 1 micrometer, such as between 1 and 15 micrometers, and preferably between 2 and 10 micrometers, on the electroplated copper layer in the openings in the photoresist layer, and then electroplating or electroless plating a solder layer, such as a bismuth-containing layer, an indium-containing layer or a tin-containing layer of a tin-lead alloy, a tin-silver alloy or a tin-silver-copper alloy, to a thickness larger than 1 micrometer, such as between 5 and 100 micrometers, and preferably between 10 and 50 micrometers, on the electroplated or electroless plated nickel layer in the openings in the photoresist layer.

[00472] After forming the metal layer 89c, the photoresist layer is removed using an inorganic solution or using an organic solution with amide. Next, the metal layer 89b not under the metal layer 89c is removed by an etching process, and then the metal layer 89a not under the metal layer 89c is removed by an etching process. The process of removing the metal layer 89b not under the metal layer 89c as shown in Fig. 15M can be referred to as the process of removing the seed layer of the adhesion/barrier/seed layer 8011 not under the bulk metal layer 8012 as illustrated in Fig. 15H. The process of removing the metal layer 89a not under the metal layer 89c as shown in Fig. 15M can be referred to as the process of etching the adhesion/barrier layer of the adhesion/barrier/seed layer 8011 not under the bulk metal layer 8012 as illustrated in Fig. 15H.

[00473] Accordingly, the metal bumps 89 provided by the metal layers 89a, 89b and 89c can be formed on the polymer layer 98 and on the regions 801a of the topmost layer of gold, copper, silver, aluminum, palladium, platinum, rhodium, ruthenium, rhenium or nickel of the previously described various the bulk metal layer 8012 exposed by the openings 980. The metal layer 89c of the metal bumps 89 can be used to be connected to an external circuit, such as ball-grid-array (BGA) substrate, printed circuit board, semiconductor chip, metal substrate, glass substrate or ceramic substrate, by bonding the metal layer 89c with the external circuit. After removing the metal layer 89a not under the metal layer 89c, the semiconductor wafer 10 can be cut into a plurality of individual semiconductor chip by a die-sawing process.

[00474] An over-passivation scheme 102 shown in Fig. 15M includes the polymer layers 95 and 98, the patterned circuit layer 801 and the metal bumps 89, and the openings 950 in the

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polymer layer 95 are over the regions of the metal pads or traces 600 exposed by the openings 50 in the passivation layer 5, and the openings 980 in the polymer layer 98 are over the contact points 801a of the patterned circuit layer 801, and the metal bumps 89 are in the openings 980, on the contact points 801a and on the polymer layer 98.

[00475] The emboss process shown in Figs. 15C to 15K describes a metal layer is formed by a suitable process or processes, e.g., by only one photoresist patterning process for electroplating a metal layer in an opening in the only one photoresist layer. This type of process is a single-emboss process that means the process includes one and only one photolithography process before removing the adhesion/barrier/seed layer not under the electroplated metal layer. A double-emboss process can be implemented to form a metal trace and a via plug on the metal trace by electroplating metal layers with different patterns using only one adhesion/barrier/seed layer, while performing two photolithography processes, before removing the adhesion/barrier/seed layer not under an electroplated metal layer. The first photolithography process is performed for defining the pattern of the metal trace, while the second photolithography process is performed for defining the pattern of the via plug. Figs 15C-15G and Figs. 16A-16D show a double-embossing process to form an over-passivation scheme over the wafer 10 shown in Fig. 15A or Fig. 15B. The double-embossing process has front steps same as the steps shown in Figs. 15C-15G. The steps of Figs. 16A-16D follow the steps of Figs. 15C-15G for a double embossing process. In Fig. 15G, the photoresist layer 71 is stripped, leaving the adhesion/barrier/seed layer 8011 not under the bulk metal layer 8012 exposed to the ambient. Figs. 16A-16M show an example to form an over-passivation scheme for all embodiments in this disclosure by using a double-embossing process to form the metal layer 801 and the via plugs 898, using a single embossing to form the metal layer 802, and using a single embossing to form the metal bump 89.

[00476] Referring to Fig. 16A, a first photolithography and electroplating process is performed to form the first metal layer 801, which can be referred to as the step illustrated in Figs. 15D-15G, and then a second photoresist layer 72 is deposited and patterned on the seed layer of the adhesion/barrier/seed layer 8011 and on the bulk metal layer 8012. It is noted that openings 720 in the photoresist layer 72 expose the bulk metal layer 8012; openings 720' in the photoresist layer 72 expose the seed layer of the adhesion/barrier/seed layer 8011.

[00477] For example, the photoresist layer 72 can be formed by a suitable process or processes, e.g., by spin-on coating a positive-type photosensitive polymer layer on the seed

layer of the adhesion/barrier/seed layer 8011 and on the electroplated bulk metal layer 8012, then exposing the photosensitive polymer layer using a 1X stepper or 1X contact aligner with at least two of G-line having a wavelength ranging from, e.g., about 434 to 438nm, H-line having a wavelength ranging from, e.g., about 403 to 407nm, and I-line having a wavelength ranging from, e.g., about 363 to 367nm, illuminating the photosensitive polymer layer, that is, G-line and H-line, G-line and I-line, H-line and I-line, or G-line, H-line and I-line illuminate the photosensitive polymer layer, then developing the exposed polymer layer, and then removing the residual polymeric material or other contaminants from the seed layer and form the bulk metal layer 8012 with an O_2 plasma or a plasma containing fluorine of below 200PPM and oxygen, such that the photoresist layer 72 can be patterned with the openings 720 and 720' exposing the bulk metal layer 8012 and the seed layer of the adhesion/barrier/seed layer 8011, respectively.

[00478] Referring to Fig. 16B, since the seed layer of the adhesion/barrier/seed layer 8011 is not removed, a second electroplating process can be performed to form via plugs 898. Note that a metal piece 898'on the seed layer of the adhesion/barrier/seed layer 8011 is also formed at a horizontal level lower than via plugs 898. The metal piece 898' can be used for packaging purposes. The metal piece 898' may be thinner or thicker than the bulk metal layer 8012. It can be used for higher density interconnection (in case of thinner) or used for lower resistance interconnection (in case of thicker).

[00479] The material of the via plug 898 and metal piece 898' may be gold or copper. For example, the via plug 898 and metal piece 898' may be formed by a suitable process or processes, e.g., by electroplating a gold layer with a thickness of between 1 and 100μm, and preferably of between 2 and 30μm, on the gold layer, exposed by the openings 720, of the bulk metal layer 8012, and on the seed layer, made of gold, of the adhesion/barrier/seed layer 8011 exposed by the openings 720'. Alternatively, the via plug 898 and metal piece 898' may be formed by a suitable process or processes, e.g., by electroplating a copper layer with a thickness of between 1 and 100μm, and preferably of between 2 and 30μm, on the copper layer, exposed by the openings 720, of the bulk metal layer 8012, and on the seed layer, made of copper, of the adhesion/barrier/seed layer 8011 exposed by the openings 720'.

[00480] Referring to Fig. 16C, the second photoresist 72 is then removed using an organic solution with amide, exposing the via plugs 898, the bulk metal layer 8012 not under the via plugs 898, the seed layer of the adhesion/barrier/seed layer 8011 not under the bulk

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metal layer 8012, and the metal piece 898'. However, some residuals from the photoresist layer 72 could remain on the bulk metal layer 8012 and on the seed layer of the adhesion/barrier/seed layer 8011. Thereafter, the residuals can be removed from the seed layer of the adhesion/barrier/seed layer 8011 and from the bulk metal layer 8012 with a plasma, such as O_2 plasma or plasma containing fluorine of below 200PPM and oxygen.

[00481] Referring to Fig. 16D, the adhesion/barrier/seed layer 8011 not under the bulk metal layer 8012 and not under the metal piece 898' is removed by wet and/or dry etching. In the case of wet etching to remove the bottom metal layer 8011 not under the electroplated metal layer 8012 and not under the electroplated metal layer 898, an undercut 8011' with a sidewall of the bottom metal layer 8011 recessed from a sidewall of the electroplated metal layer 8012 and with a sidewall of the bottom metal layer 8011 recessed from a sidewall of the electroplated metal layer 898' is formed. No undercut 8011' exists when an anisotropies dry etching is used to remove the bottom metal layer 8011 not under the electroplated metal layer 8012 and not under the electroplated metal layer 898'.

[00482] For example, when the seed layer of the adhesion/barrier/seed layer 8011 is a gold layer, it can be etched with an iodine-containing solution, such as solution containing potassium iodide, with an ion milling process or with an Ar sputtering etching process. Alternatively, when the seed layer of the adhesion/barrier/seed layer 8011 is a copper layer, it can be etched with a solution containing NH_4OH or with an Ar sputtering etching process.

[00483] For example, when the adhesion/barrier layer of the adhesion/barrier/seed layer 8011 is a titanium-tungsten-alloy layer, it can be etched with a solution containing hydrogen peroxide, with a chlorine-containing plasma etching process or with an RIE process. Alternatively, when the adhesion/barrier layer of the adhesion/barrier/seed layer 8011 is a titanium layer, it can be etched with a solution containing hydrogen fluoride, with a chlorine-containing plasma etching process or with an RIE process. Alternatively, when the adhesion/barrier layer of the adhesion/barrier/seed layer 8011 is a chromium layer, it can be etched with a solution containing potassium ferricyanide.

[00484] Referring to Fig. 16E, a second polymer layer 98 is deposited on the via plugs 898, on the metal pieces 898', on the metal layer 801 and on the exposed first polymer layer 95. The second polymer layer 98 can be formed by a suitable process or processes, e.g., by a spin-on coating process, a lamination process or a screen-printing process.

[00485] For example, the polymer layer 98 can be formed by a suitable process or processes, e.g., by spin-on coating a negative-type photosensitive polyimide layer, containing ester-type precursor, having a thickness of between 6 and 50μm on the via plugs 898, on the metal pieces 898', on the bulk metal layer 8012 and on the exposed polymer layer 95, then baking the spin-on coated polyimide layer, and then curing or heating the baked polyimide layer at a peak temperature of between 290 and 400°C for a time of between 20 and 150 minutes in a nitrogen ambient or in an oxygen-free ambient, the cured polyimide layer having a thickness of between 3 and 25μm. Alternatively, the baked polyimide layer can be cured or heated at a temperature between 150 and 290°C, and preferably of between 260 and 280°C, for a time of between 20 and 150 minutes in a nitrogen ambient or in an oxygen-free ambient.

[00486] Referring to Fig. 16F, a polishing or mechanical polishing process, and preferably a chemical-mechanical polishing (CMP) process, is used to planarize the surface of the second polymer layer 98, exposing the via plugs 898. The polymer layer 98, after being planarized, may have a thickness t between 5 and 50 micrometers.

[00487] Figs. 16G-16K show process steps to form a second over-passivation metal layer 802 using a single-embossing process same as described in Figs. 15D-15H, that is, an adhesion/barrier/seed layer 8021 is formed, exemplary by sputtering, on the second polymer layer 98 and on the exposed via plugs 898, followed by forming a photoresist layer 73 on the adhesion/barrier/seed layer 8021, openings 730 in the photoresist layer 73 exposing the seed layer of the adhesion/barrier/seed layer 8021, followed by forming a bulk conduction metal layer 8022 on the seed layer exposed by the openings 730, followed by removing the photoresist layer 73, followed by removing the adhesion/barrier/seed layer 8021 not under the bulk conduction metal layer 8022. The specification of the adhesion/barrier/seed layer 8021 and the bulk conduction metal layer 8022 shown in Figs. 16G-16K can be referred to as the specification of the adhesion/barrier/seed layer 8011 and the bulk metal layer 8012 illustrated in Figs. 15D-15K, respectively. The process of forming the adhesion/barrier/seed layer 8021 shown in Figs. 16G-16K can be referred to as the process of forming the adhesion/barrier/seed layer 8011 illustrated in Figs. 15D-15K. The process of forming the bulk conduction metal layer 8022 shown in Figs. 16G-16K can be referred to as the process of forming the bulk metal layer 8012 illustrated in Figs. 15D-15K.

[00488] Referring to Fig. 16L, a polymer layer 99 is then formed and patterned to complete a two-metal-layer over-passivation scheme. An over-passivation scheme 102 shown

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in Fig. 16L includes the polymer layers 95, 98 and 99, the patterned circuit layers 801 and 802, the via plugs 898, and the metal piece 898', and the openings 950 in the polymer layer 95 are over the regions of the metal pads or traces 600 exposed by the openings 50 in the passivation layer 5, and the opening 990 in the polymer layer 99 is over the contact point 8000 of the patterned circuit layer 802 and exposes it. After the step illustrated in Fig. 16L, the semiconductor wafer 10 can be optionally cut into a plurality of individual semiconductor chip by a die-sawing process.

[00489] Alternatively, referring to Fig. 16M, after the step illustrated in Fig. 16L, the contact structure 89 illustrated in Fig. 15L or Fig. 15M can be formed on the exposed contact point 8000 for assembly and/or packaging purposes. The specification of the contact structure 89 shown in Fig. 16M can be referred to as the specification of the contact structure 89 illustrated in Fig. 15L or Fig 15M. The process of forming the contact structure 89 as shown in Fig. 16M can be referred to as the process of forming the contact structure 89 illustrated in Fig. 15L or Fig. 15M. As an alternative, the double-emboss process steps in Figs. 15D-15G and 16A-16D for forming the first metal layer 801 and the first via plug 898 can be repeated to form additional metal layer (not shown) on the polymer layer 98 and on the via plugs 898, and to form additional via plug (not shown) on the additional metal layer. In this alternative, the additional via plug can be joined with a wirebonded wire using a wirebonding process, with a solder bump using a ball-mounting process or with a flexible substrate using a TAB process. The description and specification in Figs. 16A-16M can be applied to forming the thick and wide power metal trace, bus or plane 81 over the passivation layer 5 in the disclosure, to forming the thick and wide ground metal trace, bus or plane 82 over the passivation layer 5 in the disclosure, to forming the thick and wide power metal trace, bus or plane 81P over the passivation layer 5 in the disclosure, and to forming the thick and wide signal metal trace, bus or plane 83, 83' or 85 over the passivation layer 5 in the disclosure.

[00490] After forming the over-passivation scheme of the top post-passivation technology shown in Fig. 16M, the semiconductor wafer 10 can be cut into a plurality of individual semiconductor chip by a die-sawing process. An over-passivation scheme 102 shown in Fig. 16M includes the polymer layers 95, 98 and 99, the patterned circuit layers 801 and 802, the via plugs 898, the metal piece 898', and the metal bump 89, and the openings 950 in the polymer layer 95 are over the regions of the metal pads or traces 600 exposed by the openings 50 in the passivation layer 5, and the opening 990 in the polymer layer 99 is over

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the contact point 8000 of the patterned circuit layer 802, and the metal bump 89 is in the opening 990, on the contact point 8000 and on the polymer layer 99.

[00491] Figs. 17A to 17J show process steps to form an over-passivation scheme 102 with three metal layers 801, 802 and 803. Metal layers 801 and 802 are formed by a suitable process or processes, e.g., by a double-emboss process, while the metal layer 803 is formed by a suitable process or processes, e.g., by a single-emboss process. A first double-embossing process is used to form the first metal layer 801 and the first via plug 898 as described in Figs. 15D-15G and 16A-16D. A first inter-metal polymer layer 98 is formed and planarized to expose the first via plugs 898, shown in process steps of Figs. 16E-16F. Fig. 17A is at the same step as Fig. 16J when the first metal layer 801, the first via plugs 898 and the metal piece 898' are formed by a suitable process or processes, e.g., by a double-emboss metal process, and the inter-metal dielectric polymer layer 98 is formed with the first via plugs 898 being exposed. The design of the first metal layer 801 and the first via plugs 898 in Fig. 17A is slightly different from that in Fig. 16J to accommodate an additional metal layer. The process for forming the bottom metal layer 8021 in Fig. 17A can be referred to as the process for forming the bottom metal layer 8011 in Fig. 15D or the bottom metal layer 8021 in Fig. 16G; the process for forming the metal layer 8022 in Fig. 17A can be referred to as the process for forming the metal layer 8012 in Fig. 15E or the metal layer 8022 in Figs. 16H-16J. The specification of the adhesion/barrier/seed layer 8021 and the bulk conduction metal layer 8022 shown in Figs. 17A-17J can be referred to as the specification of the adhesion/barrier/seed layer 8011 and the bulk metal layer 8012, respectively, illustrated in Figs. 15D-15K.

[00492] Referring to Fig. 17B now, a second photoresist layer 74 is then deposited and patterned to form openings 740 over the bulk conduction metal layer 8022 and/or to optionally form openings 740' directly on the seed layer of the second adhesion/barrier/seed layer 8021.

[00493] For example, the photoresist layer 74 can be formed by a suitable process or processes, e.g., by spin-on coating a positive-type photosensitive polymer layer on the seed layer of the adhesion/barrier/seed layer 8021 and on the bulk conduction metal layer 8022, then exposing the photosensitive polymer layer using a 1X stepper or 1X contact aligner with at least two of G-line having a wavelength ranging from, e.g., about 434 to 438nm, H-line having a wavelength ranging from, e.g., about 403 to 407nm, and I-line having a wavelength ranging from, e.g., about 363 to 367nm, illuminating the photosensitive polymer layer, that is, G-line and H-line, G-line and I-line, H-line and I-line, or G-line, H-line and I-line illuminate the

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photosensitive polymer layer, then developing the exposed polymer layer, and then removing the residual polymeric material or other contaminants from the seed layer and form the bulk conduction metal layer 8022 with an O_2 plasma or a plasma containing fluorine of below 200PPM and oxygen, such that the photoresist layer 74 can be patterned with the openings 740 and 740' exposing the bulk conduction metal layer 8022 and the seed layer of the adhesion/barrier/seed layer 8021, respectively.

[00494] Referring to Fig. 17C, a second via plug layer is electroplated in the photoresist openings 740 and 740' to form the second via plugs 897 and the second metal piece 897'. The second metal piece 897' can be used as described for the first metal piece 989'. The material of the via plug 897 and metal piece 897' may be gold or copper. For example, the via plug 897 and metal piece 897' may be formed by a suitable process or processes, e.g., by electroplating a gold layer with a thickness of between 1 and 100μm, and preferably of between 2 and 30μm, on the gold layer, exposed by the openings 740, of the bulk conduction metal layer 8022, and on the seed layer, made of gold, of the adhesion/barrier/seed layer 8021 exposed by the openings 740'. Alternatively, the via plug 897 and metal piece 897' may be formed by a suitable process or processes, e.g., by electroplating a copper layer with a thickness of between 1 and 100μm, and preferably of between 2 and 30μm, on the copper layer, exposed by the openings 740, of the bulk conduction metal layer 8022, and on the seed layer, made of copper, of the adhesion/barrier/seed layer 8021 exposed by the openings 740'.

[00495] Referring to Fig. 17D, the second photoresist layer 74 is then stripped using an organic solution with amide. However, some residuals from the photoresist layer 74 could remain on the bulk conduction metal layer 8022 and on the seed layer of the adhesion/barrier/seed layer 8021. Thereafter, the residuals can be removed from the bulk conduction metal layer 8022 and from the seed layer with a plasma, such as O_2 plasma or plasma containing fluorine of below 200PPM and oxygen.

[00496] Alternatively, after the bulk conduction metal layer 8022 is formed on the seed layer of the adhesion/barrier/seed layer 8021 exposed by the openings 730 illustrated in Fig. 16I, without removing the photoresist layer 73, the photoresist layer 74 shown in Fig. 17B can be formed on the photoresist layer 73 and on the bulk conduction metal layer 8022. The openings 740 in the photoresist layer 74 expose the bulk conduction metal layer 8022, respectively, for defining the pattern of the via plugs 897. The process for forming the via plugs 897 can be referred to as the above disclosure. Finally, the photoresist layers 73 and 74

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are removed using an organic solution with amide. However, some residuals from the photoresist layers 73 and 74 could remain on the bulk conduction metal layer 8022, on the via plugs 897 and on the seed layer of the adhesion/barrier/seed layer 8021. Thereafter, the residuals can be removed from the seed layer of the adhesion/barrier/seed layer 8021, from the via plugs 897 and from the bulk conduction metal layer 8022 with a plasma, such as O_2 plasma or plasma containing fluorine of below 200PPM and oxygen. Next, the adhesion/barrier/seed layer 8021 not under the bulk conduction metal layer 8022 can be removed, as mentioned in the above description.

[00497] Referring to Fig. 17E, the second adhesion/barrier/seed layer 8021 not under the second bulk conduction metal layer 8022 and not under the second metal piece 987' is removed. The process of removing the second adhesion/barrier/seed layer 8021 not under the second bulk conduction metal layer 8022 and not under the second metal piece 897', as shown in Fig. 17E, can be referred to as the process of removing the first adhesion/barrier/seed layer 8011 not under the first bulk metal layer 8012 and not under the metal piece 898', as illustrated in Fig. 16D.

[00498] Referring to Figs. 17F-17G, a second inter-metal dielectric polymer layer 97 is then deposited and planarized to expose the second via plugs 897. The material of the polymer layer 97 may be polyimide (PI), benzocyclobutane (BCB), polyurethane, epoxy resin, a parylene-based polymer, a solder-mask material, an elastomer, silicone or a porous dielectric material. The process for forming the polymer layer 97 in Fig. 17F can be as referred to as the process for forming the polymer layer 98 in Fig. 16E; the process for planarizing the polymer layer 97 in Fig. 17G can be as referred to as the process for planarizing the polymer layer 98 in Fig. 16F.

[00499] For example, the polymer layer 97 can be formed by a suitable process or processes, e.g., by spin-on coating a negative-type photosensitive polyimide layer, containing ester-type precursor, having a thickness of between 10 and 120μm on the exposed bulk conduction metal layer 8022, on the via plugs 897, on the metal piece 897' and on the exposed polymer layer 98, then baking the spin-on coated polyimide layer, then curing or heating the baked polyimide layer at a peak temperature of between 290 and 400°C for a time of between 20 and 150 minutes in a nitrogen ambient or in an oxygen-free ambient, the cured polyimide layer having a thickness of between 5 and 60μm, and then polishing or mechanical polishing, exemplary chemical-mechanical polishing, an upper surface of the polymer layer 97 to uncover

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the via plugs 897 and to planarize the upper surface thereof. Alternatively, the baked polyimide layer can be cured or heated at a temperature between 150 and 290°C, and preferably of between 260 and 280°C, for a time of between 20 and 150 minutes in a nitrogen ambient or in an oxygen-free ambient.

[00500] Figs. 17H and 17I show a single-embossing process is used to form a third metal layer 803 by first depositing an adhesion/barrier/seed layer 8031, depositing and patterning a photoresist layer, electroplating a bulk conduction metal layer 8032, stripping the photoresist layer and self-aligned etch the adhesion/barrier/seed layer 8031. The specification of the adhesion/barrier/seed layer 8031 and the bulk conduction metal layer 8032 shown in Figs. 17H-17I can be referred to as the specification of the adhesion/barrier/seed layer 8011 and the bulk metal layer 8012, respectively, illustrated in Figs. 15D-15H. The process of forming the adhesion/barrier/seed layer 8031 shown in Figs. 17H-17I can be referred to as the process of forming the adhesion/barrier/seed layer 8011 illustrated in Figs. 15D-15H. The process of forming the bulk conduction metal layer 8032 shown in Figs. 17H-17I can be referred to as the process of forming the bulk metal layer 8012 illustrated in Figs. 15D-15H.

[00501] Fig. 17J shows a completed structure by forming a polymer layer 99 on the exposed polymer layer 97 and on the third metal layer 803, and an opening 990 in the polymer layer 99 exposes a contact point 8000 for interconnection to an external circuit. The polymer layer 99 may be formed by a suitable process or processes, e.g., by a spin-on coating process, a lamination process or a screen-printing process. The polymer layer 99 may include polyimide (PI), benzocyclobutane (BCB), polyurethane, epoxy resin, a parylene-based polymer, a solder-mask material, an elastomer, silicone or a porous dielectric material.

[00502] For example, the polymer layer 99 can be formed by a suitable process or processes, e.g., by spin-on coating a negative-type photosensitive polyimide layer, containing ester-type precursor, having a thickness of between 6 and 50μm on the exposed polymer layer 97 and on the bulk conduction metal layer 8032, then baking the spin-on coated polyimide layer, then exposing the baked polyimide layer using a 1X stepper or 1X contact aligner with at least two of G-line having a wavelength ranging from, e.g., about 434 to 438nm, H-line having a wavelength ranging from, e.g., about 403 to 407nm, and I-line having a wavelength ranging from, e.g., about 363 to 367nm, illuminating the baked polyimide layer, that is, G-line and H-line, G-line and I-line, H-line and I-line, or G-line, H-line and I-line illuminate the baked polyimide layer, then developing the exposed polyimide layer to form a polyimide opening in

the exposed polyimide layer exposing the contact point 8000, then curing or heating the developed polyimide layer at a peak temperature of between 290 and 400°C for a time of between 20 and 150 minutes in a nitrogen ambient or in an oxygen-free ambient, the cured polyimide layer having a thickness of between 3 and 25μm, and then removing the residual polymeric material or other contaminants from the contact point 8000 exposed by the polyimide opening with an O_2 plasma or a plasma containing fluorine of below 200PPM and oxygen, such that the polymer layer 99 can be patterned with an opening 990 in the polymer layer 99 exposing the contact point 8000. Alternatively, the developed polyimide layer can be cured or heated at a temperature between 150 and 290°C, and preferably of between 260 and 280°C, for a time of between 20 and 150 minutes in a nitrogen ambient or in an oxygen-free ambient.

[00503] The contact point 8000 can be used to be connected to an external circuit via a wirebonding process, a solder bonding process or a tape-automated-bonding (TAB) process, and the external circuit may be another semiconductor chip, a flexible substrate including a polymer layer (such as polyimide) having a thickness between 30 and 200 micrometers and not including any polymer layer with glass fiber, a glass substrate, a ceramic substrate including a ceramic material as insulating layers between circuit layers, a silicon substrate, an organic substrate, a printed circuit board (PCB) or a ball grid array (BGA) substrate.

[00504] After forming the over-passivation scheme of the top post-passivation technology shown in Fig. 17J, the semiconductor wafer 10 can be cut into a plurality of individual semiconductor chip by a die-sawing process. An over-passivation scheme 102 shown in Fig. 17J includes the polymer layers 95, 97, 98 and 99, the patterned circuit layers 801, 802 and 803, the via plugs 897 and 898, and the metal pieces 897' and 898', and the openings 950 in the polymer layer 95 are over the regions of the metal pads or traces 600 exposed by the openings 50 in the passivation layer 5, and the opening 990 in the polymer layer 99 is over the contact point 8000 of the patterned circuit layer 803 and exposes it.

[00505] Figs. 18A to 18I show another alternative of process steps to form an over-passivation scheme with three metal layers 801, 802 and 803. Metal layers 801 and 803 are formed by a suitable process or processes, e.g., by a single-emboss process, while the metal layer 802 is formed by a suitable process or processes, e.g., by a double-emboss process.

[00506] Referring to Fig. 18A, a first single-embossing process is used to form the first metal layer 801 as described in Figs. 15D-15H. Next, a first inter-metal polymer layer 98 is

deposited and patterned with openings 980 to expose the first metal layer 801, as shown in process step of Fig. 15I. Fig. 18A is at the same process step as Fig. 15I when the first metal layer 801 and the first inter-metal dielectric polymer layer 98 are formed by a suitable process or processes, e.g., by a single-emboss metal process, and the inter-metal dielectric polymer layer 98 is deposited and patterned with openings 980 exposing the first metal layer 801. The design of the first metal layer 801 and the first inter-metal polymer openings 980 in Fig. 18A is slightly different from that in Fig. 15I to accommodate an additional metal layer. The process steps in Figs. 18B-18G show a double-embossing process to form a second metal layer 802 and via plugs 897. The specification of the polymer layer 95, the metal layer 801 and the polymer layer 98 shown in Figs. 18A-18I can be referred to as the specification of the polymer layer 95, the metal layer 801 and the polymer layer 98, respectively, illustrated in Figs. 15C-15K. The process of forming the polymer layer 95 shown in Fig. 18A can be referred to as the polymer layer 95 illustrated in Figs. 15C-15K. The process of forming the metal layer 801 shown in Fig. 18A can be referred to as the metal layer 801 illustrated in Figs. 15C-15K. The process of forming the polymer layer 98 shown in Fig. 18A can be referred to as the polymer layer 98 illustrated in Figs. 15C-15K.

[00507] Referring to Fig. 18B, a second adhesion/barrier/seed layer 8021 is deposited on the polymer layer 98 and on the first metal layer 801 exposed by the openings 980. The specification of the second adhesion/barrier/seed layer 8021 shown in Figs. 18B-18I can be referred to as the specification of the second adhesion/barrier/seed layer 8021 illustrated in Figs. 15J-15K. The process of forming the second adhesion/barrier/seed layer 8021 shown in Fig. 18B can be referred to as the process of forming the second adhesion/barrier/seed layer 8021 illustrated in Figs. 15J-15K.

[00508] Referring to Fig. 18C, a photoresist layer 73, such as positive-type photoresist layer, is deposited on the seed layer of the second adhesion/barrier/seed layer 8021. Next, the photoresist layer 73 is patterned with exposure and development processes to form openings 730 in the photoresist layer 73 exposing the seed layer of the second adhesion/barrier/seed layer 8021. A 1X stepper or 1X contact aligner can be used to expose the photoresist layer 73 during the process of exposure.

[00509] For example, the photoresist layer 73 can be formed by a suitable process or processes, e.g., by spin-on coating a positive-type photosensitive polymer layer on the seed layer of the second adhesion/barrier/seed layer 8021, then exposing the photosensitive polymer

layer using a 1X stepper or 1X contact aligner with at least two of G-line having a wavelength ranging from, e.g., about 434 to 438nm, H-line having a wavelength ranging from, e.g., about 403 to 407nm, and I-line having a wavelength ranging from, e.g., about 363 to 367nm, illuminating the photosensitive polymer layer, that is, G-line and H-line, G-line and I-line, H-line and I-line, or G-line, H-line and I-line illuminate the photosensitive polymer layer, then developing the exposed polymer layer, and then removing the residual polymeric material or other contaminants from the seed layer with an O_2 plasma or a plasma containing fluorine of below 200PPM and oxygen, such that the photoresist layer 73 can be patterned with openings 730 in the photoresist layer 73 exposing the seed layer.

[00510] Next, a bulk conduction layer 8022 can be electroplated and/or electroless plated over the seed layer exposed by the openings 730. The bulk conduction layer 8022 may be a single layer of gold, copper, silver, palladium, platinum, rhodium, ruthenium, rhenium or nickel, or a composite layer made of the previously described metals. The specification of the bulk conduction metal layer 8022 shown in Figs. 18C-18I can be referred to as the specification of the bulk metal layer 8012 illustrated in Figs. 15F-15K. The process of forming the bulk conduction metal layer 8022 shown in Figs. 18C-18I can be referred to as the process of forming the bulk metal layer 8012 illustrated in Figs. 15F-15K.

[00511] Referring to Fig. 18D, the photoresist layer 73 is then stripped using an organic solution with amide. However, some residuals from the photoresist layer 73 could remain on the bulk conduction metal layer 8022 and on the seed layer of the adhesion/barrier/seed layer 8021. Thereafter, the residuals can be removed from the seed layer of the adhesion/barrier/seed layer 8021 and from the bulk conduction metal layer 8022 with a plasma, such as O_2 plasma or plasma containing fluorine of below 200PPM and oxygen.

[00512] Referring to Fig. 18E, a photoresist layer 74 is then deposited and patterned to form openings 740 over the second bulk conduction metal layer 8022 and/or to optionally form openings 740' directly on the seed layer of the second adhesion/barrier/seed layer 8021. For example, the photoresist layer 74 can be formed by a suitable process or processes, e.g., by spin-on coating a positive-type photosensitive polymer layer on the seed layer of the adhesion/barrier/seed layer 8021 and on the bulk conduction metal layer 8022, then exposing the photosensitive polymer layer using a 1X stepper or 1X contact aligner with at least two of G-line having a wavelength ranging from, e.g., about 434 to 438nm, H-line having a wavelength ranging from, e.g., about 403 to 407nm, and I-line having a wavelength ranging

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from, e.g., about 363 to 367nm, illuminating the photosensitive polymer layer, that is, G-line and H-line, G-line and I-line, H-line and I-line, or G-line, H-line and I-line illuminate the photosensitive polymer layer, then developing the exposed polymer layer, and then removing the residual polymeric material or other contaminants from the seed layer and form the bulk conduction metal layer 8022 with an O_2 plasma or a plasma containing fluorine of below 200PPM and oxygen, such that the photoresist layer 74 can be patterned with the openings 740 and 740' exposing the bulk conduction metal layer 8022 and the seed layer of the adhesion/barrier/seed layer 8021, respectively.

[00513] Next, a via plug layer is electroplated in the photoresist openings 740 and 740' to form via plugs 897 and metal piece 897'. The metal piece 897' can be used as described for the metal piece 898' in Fig. 16D.

[00514] The material of the via plug 897 and metal piece 897' may be gold or copper. For example, the via plug 897 and metal piece 897' may be formed by a suitable process or processes, e.g., by electroplating a gold layer with a thickness of between 1 and 100μm, and preferably of between 2 and 30μm, on the gold layer, exposed by the openings 740, of the bulk conduction metal layer 8022, and on the seed layer, made of gold, of the adhesion/barrier/seed layer 8021 exposed by the openings 740'. Alternatively, the via plug 897 and metal piece 897' may be formed by a suitable process or processes, e.g., by electroplating a copper layer with a thickness of between 1 and 100μm, and preferably of between 2 and 30μm, on the copper layer, exposed by the openings 740, of the bulk conduction metal layer 8022, and on the seed layer, made of copper, of the adhesion/barrier/seed layer 8021 exposed by the openings 740'.

[00515] Referring to Fig. 18F, the photoresist layer 74 is then stripped using an organic solution with amide. However, some residuals from the photoresist layer 74 could remain on the exposed bulk conduction metal layer 8022, on the via plugs 897, on the metal piece 897' and on the seed layer of the adhesion/barrier/seed layer 8021. Thereafter, the residuals can be removed from the seed layer, from the via plugs 897, from the metal piece 897' and from the bulk conduction metal layer 8022 with a plasma, such as O_2 plasma or plasma containing fluorine of below 200PPM and oxygen.

[00516] Alternatively, after the bulk conduction metal layer 8022 is formed on the seed layer of the adhesion/barrier/seed layer 8021 exposed by the openings 730 illustrated in Fig. 18C, without removing the photoresist layer 73, the photoresist layer 74 shown in Fig. 18E can be formed on the photoresist layer 73 and on the bulk conduction metal layer 8022. The

openings 740 in the photoresist layer 74 expose the bulk conduction metal layer 8022, respectively, for defining the pattern of the via plugs 897. The process for forming the via plugs 897 can be referred to as the above disclosure. Finally, the photoresist layers 73 and 74 are removed using an organic solution with amide. However, some residuals from the photoresist layers 73 and 74 could remain on the bulk conduction metal layer 8022, on the via plugs 897 and on the seed layer of the adhesion/barrier/seed layer 8021. Thereafter, the residuals can be removed from the seed layer of the adhesion/barrier/seed layer 8021, from the via plugs 897 and from the bulk conduction metal layer 8022 with a plasma, such as O_2 plasma or plasma containing fluorine of below 200PPM and oxygen. Next, the adhesion/barrier/seed layer 8021 not under the bulk conduction metal layer 8022 can be removed, as mentioned in the above description.

[00517] Referring to Fig. 18G, the adhesion/barrier/seed layer 8021 not under the bulk conduction metal layer 8022 and not under the metal piece 897' can be removed. The process of removing the adhesion/barrier/seed layer 8021 not under the bulk conduction metal layer 8022 and not under the second metal piece 897', as shown in Fig. 18G, can be referred to as the process of removing the adhesion/barrier/seed layer 8011 not under the bulk metal layer 8012 and not under the metal piece 898', as illustrated in Fig. 16D.

[00518] Referring to Fig. 18H, a second inter-metal dielectric polymer layer 97 is then deposited and planarized to expose the second via plugs 897. The material of the polymer layer 97 may be polyimide (PI), benzocyclobutane (BCB), polyurethane, epoxy resin, a parylene-based polymer, a solder-mask material, an elastomer, silicone or a porous dielectric material.

[00519] For example, the polymer layer 97 can be formed by a suitable process or processes, e.g., by spin-on coating a negative-type photosensitive polyimide layer, containing ester-type precursor, having a thickness of between 10 and 120μm on the exposed bulk conduction metal layer 8022, on the via plugs 897, on the metal piece 897' and on the exposed polymer layer 98, then baking the spin-on coated polyimide layer, then curing or heating the baked polyimide layer at a peak temperature of between 290 and 400°C for a time of between 20 and 150 minutes in a nitrogen ambient or in an oxygen-free ambient, the cured polyimide layer having a thickness of between 5 and 60μm, and then polishing or mechanical polishing, exemplary chemical-mechanical polishing, an upper surface of the polymer layer 97 to uncover the via plugs 897 and to planarize the upper surface thereof. Alternatively, the baked polyimide

layer can be cured or heated at a temperature between 150 and 290°C, and preferably of between 260 and 280°C, for a time of between 20 and 150 minutes in a nitrogen ambient or in an oxygen-free ambient.

[00520] Fig. 18I shows a completed structure by first forming the third metal layer 803 is formed by a suitable process or processes, e.g., by a single-embossing process as described in Figs 17H-17I. Next, a polymer layer 99 is spin coated on the patterned circuit layer 803, and an opening 990 is formed in the polymer layer 99 to expose a contact point 8000 for interconnection to an external circuit. The specification of the adhesion/barrier/seed layer 8031 and the bulk conduction metal layer 8032 shown in Fig. 18I can be referred to as the specification of the adhesion/barrier/seed layer 8011 and the bulk metal layer 8012, respectively, illustrated in Figs. 15D-15H. The process of forming the adhesion/barrier/seed layer 8031 shown in Fig. 18I can be referred to as the process of forming the adhesion/barrier/seed layer 8011 illustrated in Figs. 15D-15H. The process of forming the bulk conduction metal layer 8032 shown in Fig. 18I can be referred to as the process of forming the bulk metal layer 8012 illustrated in Figs. 15D-15H. The specification of the polymer layer 99 shown in Fig. 18I can be referred to as the specification of the polymer layer 99 illustrated in Fig. 17J. The process of forming the polymer layer 99 shown in Fig. 18I can be referred to as the process of forming the polymer layer 99 and the opening 990 illustrated in Fig. 17J.

[00521] The contact point 8000 can be used to be connected to an external circuit via a wirebonding process, a solder bonding process or a tape-automated-bonding (TAB) process, and the external circuit may be another semiconductor chip, a flexible substrate including a polymer layer (such as polyimide) having a thickness of between 30 and 200 micrometers and not including any polymer layer with glass fiber, a glass substrate, a ceramic substrate including a ceramic material as insulating layers between circuit layers, a silicon substrate, an organic substrate, a printed circuit board (PCB) or a ball grid array (BGA) substrate.

[00522] After forming the over-passivation scheme of the top post-passivation technology shown in Fig. 18I, the semiconductor wafer 10 can be cut into a plurality of individual semiconductor chip by a die-sawing process. An over-passivation scheme 102 shown in Fig. 18I includes the polymer layers 95, 97, 98 and 99, the patterned circuit layers 801, 802 and 803, the via plugs 897, and the metal piece 897', and the openings 950 in the polymer layer 95 are over the regions of the metal pads or traces 600 exposed by the openings 50 in the passivation layer 5, and the openings 980 in the polymer layer 98 are over the

patterned circuit layer 801, and the opening 990 in the polymer layer 99 is over the contact point 8000 of the patterned circuit layer 803 and exposes it.

[00523] Figs. 19A to 19H show another alternative of process steps to form an over-passivation scheme with two metal layers 801 and 802. The metal layer 801 is formed by a suitable process or processes, e.g., by a double-emboss process, while the metal layer 802 is formed by a suitable process or processes, e.g., by a single-emboss process.

[00524] Referring to Fig. 19A, after the process steps of Figs. 15C-15G and 16A-16F for forming the polymer layer 95, the openings 950, the metal layer 801, the via plugs 898, the metal pieces 898` and the polymer layer 98 are completed, a polymer layer 97 can be formed on the polymer layer 98, multiple openings 970 in the polymer layer 97 exposing the via plugs 898. The material of the polymer layer 97 may be polyimide (PI), benzocyclobutane (BCB), polyurethane, epoxy resin, a parylene-based polymer, a solder-mask material, an elastomer, silicone or a porous dielectric material.

[00525] For example, the polymer layer 97 can be formed by a suitable process or processes, e.g., by spin-on coating a negative-type photosensitive polyimide layer, containing ester-type precursor, having a thickness of between 6 and 50μm on the polymer layer 98 and on the exposed via plugs 898, then baking the spin-on coated polyimide layer, then exposing the baked polyimide layer using a 1X stepper or 1X contact aligner with at least two of G-line having a wavelength ranging from, e.g., about 434 to 438nm, H-line having a wavelength ranging from, e.g., about 403 to 407nm, and I-line having a wavelength ranging from, e.g., about 363 to 367nm, illuminating the baked polyimide layer, that is, G-line and H-line, G-line and I-line, H-line and I-line, or G-line, H-line and I-line illuminate the baked polyimide layer, then developing the exposed polyimide layer to form polyimide openings in the exposed polyimide layer exposing the exposed via plugs 898, then curing or heating the developed polyimide layer at a peak temperature of between 290 and 400°C for a time of between 20 and 150 minutes in a nitrogen ambient or in an oxygen-free ambient, the cured polyimide layer having a thickness of between 3 and 25μm, and then removing the residual polymeric material or other contaminants from the upper surface of the via plugs 898 exposed by the polyimide openings with an O_2 plasma or a plasma containing fluorine of below 200PPM and oxygen, such that the polymer layer 97 can be patterned with openings 970 exposing the via plugs 898. Alternatively, the developed polyimide layer can be cured or heated at a temperature between 150 and 290°C, and preferably of between 260 and 280°C, for a time of between 20 and 150

minutes in a nitrogen ambient or in an oxygen-free ambient. [0051] Referring to Fig. 19B, an adhesion/barrier/seed layer 8021 is deposited, exemplary by sputtering, on the polymer layer 97 and on the via plugs 898 exposed by the openings 970. Alternatively, the adhesion/barrier/seed layer 8021 can be formed by a suitable process or processes, e.g., by a process including a vapor deposition method, an evaporation method, a CVD method, an electroless plating method or a PVD method. The specification of the adhesion/barrier/seed layer 8021 shown in Figs. 19B-19I can be referred to as the specification of the adhesion/barrier/seed layer 8011 illustrated in Figs. 15D-15K. The process of forming the adhesion/barrier/seed layer 8021shown in Fig. 19B can be referred to as the process of forming the adhesion/barrier/seed layer 8011 illustrated in Figs. 15D-15K.

[00526] Referring to Fig. 19C, a photoresist layer 73, such as positive-type photoresist layer, is formed on the adhesion/barrier/seed layer 8021. Next, the photoresist layer 73 is patterned with exposure and development processes to form openings 730 in the photoresist layer 73 exposing the adhesion/barrier/seed layer 8021. A 1X stepper or 1X contact aligner can be used to expose the photoresist layer 730 during the process of exposure. The process of forming the photoresist layer 73 and the openings 730 in the photoresist layer 73 shown in Fig. 19C can be referred to as the process of forming the photoresist layer 73 and the openings 730 in the photoresist layer 73 illustrated in Fig. 18C.

[00527] Referring to Fig. 19D, a bulk conduction metal layer 8022 can be electroplated and/or electroless plated over the adhesion/barrier/seed layer 8021 exposed by the openings 730. The bulk conduction layer 8022 may be a single layer of gold, copper, silver, palladium, platinum, rhodium, ruthenium, rhenium or nickel, or a composite layer made of the previously described metals. The specification of the bulk conduction metal layer 8022 shown in Figs. 19D-19I can be referred to as the specification of the bulk metal layer 8012 illustrated in Figs. 15F-15K. The process of forming the bulk conduction metal layer 8022 shown in Figs. 19D can be referred to as the process of forming the bulk metal layer 8012 illustrated in Figs. 15F-15K.

[00528] Referring to Fig. 19E, after the bulk conduction metal layer 8022 is formed, most of the photoresist layer 73 can be removed using an organic solution with amide. However, some residuals from the photoresist layer 73 could remain on the bulk conduction metal layer 8022 and on the seed layer of the adhesion/barrier/seed layer 8021. Thereafter, the

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residuals can be removed from the bulk conduction metal layer 8022 and from the seed layer with a plasma, such as O_2 plasma or plasma containing fluorine of below 200PPM and oxygen.

[00529] Referring to Fig. 19F, the adhesion/barrier/seed layer 8021 not under the bulk conduction metal layer 8022 is removed with a dry etching method or a wet etching method. As to the wet etching method, when the seed layer of the adhesion/barrier/seed layer 8021 is a gold layer, it can be etched with an iodine-containing solution, such as solution containing potassium iodide; when the seed layer of the adhesion/barrier/seed layer 8021 is a copper layer, it can be etched with a solution containing NH_4OH; when the adhesion/barrier layer of the adhesion/barrier/seed layer 8021 is a titanium-tungsten-alloy layer, it can be etched with a solution containing hydrogen peroxide; when the adhesion/barrier layer of the adhesion/barrier/seed layer 8021 is a titanium layer, it can be etched with a solution containing hydrogen fluoride; when the adhesion/barrier layer of the adhesion/barrier/seed layer 8021 is a chromium layer, it can be etched with a solution containing potassium ferricyanide. As to the dry etching method, when the seed layer of the adhesion/barrier/seed layer 8021 is a gold layer, it can be removed with an ion milling process or with an Ar sputtering etching process; when the adhesion/barrier layer of the adhesion/barrier/seed layer 8021 is a titanium layer or a titanium-tungsten-alloy layer, it can be etched with a chlorine-containing plasma etching process or with an RIE process. Generally, the dry etching method to etch the adhesion/barrier/seed layer 8021 not under the bulk conduction metal layer 8022 may include a chemical plasma etching process, a sputtering etching process, such as argon sputter process, or a chemical vapor etching process.

[00530] Accordingly, a second metal layer 802 can be formed on the polymer layer 97 and on the via plugs 898 exposed by the openings 970, and the second metal layer 802 is formed with the adhesion/barrier/seed layer 8021 and the bulk conduction metal layer 8022 on the adhesion/barrier/seed layer 8021.

[00531] Referring to Fig. 19G, a polymer layer 99 is formed on the exposed polymer layer 97 and on the bulk metal layer 8022 via a spin-on coating process. Referring to Fig. 19H, the polymer layer 99 is patterned with exposure and development processes to form an opening 990 in the polymer layer 99 exposing the contact point 8000. Alternatively, the polymer layer 99 may be formed by a suitable process or processes, e.g., by a lamination process or a screen-printing process. The polymer layer 99 may include polyimide (PI), benzocyclobutane

(BCB), polyurethane, epoxy resin, a parylene-based polymer, a solder-mask material, an elastomer, silicone or a porous dielectric material.

[00532] For example, the polymer layer 99 can be formed by a suitable process or processes, e.g., by spin-on coating a negative-type photosensitive polyimide layer, containing ester-type precursor, having a thickness of between 6 and 50μm on the exposed polymer layer 97 and on the bulk conduction metal layer 8022, then baking the spin-on coated polyimide layer, then exposing the baked polyimide layer using a 1X stepper or 1X contact aligner with at least two of G-line having a wavelength ranging from, e.g., about 434 to 438nm, H-line having a wavelength ranging from, e.g., about 403 to 407nm, and I-line having a wavelength ranging from, e.g., about 363 to 367nm, illuminating the baked polyimide layer, that is, G-line and H-line, G-line and I-line, H-line and I-line, or G-line, H-line and I-line illuminate the baked polyimide layer, then developing the exposed polyimide layer to form an polyimide opening in the exposed polyimide layer exposing the contact point 8000, then curing or heating the developed polyimide layer at a peak temperature of between 290 and 400°C for a time of between 20 and 150 minutes in a nitrogen ambient or in an oxygen-free ambient, the cured polyimide layer having a thickness of between 3 and 25μm, and then removing the residual polymeric material or other contaminants from the contact point 8000 exposed by the polyimide opening with an O_2 plasma or a plasma containing fluorine of below 200PPM and oxygen, such that the polymer layer 99 can be patterned with an opening 990 in the polymer layer 99 exposing the contact point 8000. Alternatively, the developed polyimide layer can be cured or heated at a temperature between 150 and 290°C, and preferably of between 260 and 280°C, for a time of between 20 and 150 minutes in a nitrogen ambient or in an oxygen-free ambient.

[00533] After forming the over-passivation scheme of the top post-passivation technology shown in Fig. 19H, the semiconductor wafer 10 can be cut into a plurality of individual semiconductor chip by a die-sawing process. The method of connecting the contact point 8000 in Fig.19H to an external circuit can be referred to as the method of connecting the contact point 8000 in Fig. 15K to an external circuit. The external circuit may be another semiconductor chip, a flexible substrate including a polymer layer (such as polyimide) having a thickness between 30 and 200μm and not including any polymer layer with glass fiber, a glass substrate, a ceramic substrate including a ceramic material as insulating layers between circuit layers, a silicon substrate, an organic substrate, a printed circuit board (PCB) or a ball grid array (BGA) substrate. For example, referring to Fig. 19I, via a wirebonding process, a

wire 89', such as gold wire, copper wire or aluminum wire, can be bonded to the contact point 8000 of the semiconductor chip cut from the wafer 10.

[00534] Alternatively, the contact structure 89 illustrated in Fig. 15L or Fig. 15M can be formed on the contact point 8000 exposed by the opening 990. After the contact structure 89 is formed on the contact point 8000 of the wafer 10 shown in Fig. 19H, the wafer 10 can be diced into a plurality of individual semiconductor chip. An over-passivation scheme 102 shown in Fig. 19H includes the polymer layers 95, 97, 98 and 99, the patterned circuit layers 801 and 802, the via plugs 898, and the metal piece 898', and the openings 950 in the polymer layer 95 are over the regions of the metal pads or traces 600 exposed by the openings 50 in the passivation layer 5, and the openings 970 in the polymer layer 97 are over the via plugs 898, and the opening 990 in the polymer layer 99 is over the contact point 8000 of the patterned circuit layer 802 and exposes it.

[00535] Figs. 21 and 22 show top views of a MOS transistor that can be a PMOS transistor or an NMOS transistor. Referring to Fig. 21, a transistor includes an active region 200, diffusion region, in or over the silicon substrate 1, a field oxide region 202 on the silicon substrate 1 and around the active region 200, a gate 204 on the field oxide region 202 and across the active region 200, and a gate oxide (not shown) between the active region 200 and the gate 204. The active region 200 can be defined as a source 206 at a side of the gate 204, and a drain 208 at the other side of the gate 204. The material of the gate 204 may be poly silicon, metal silicide or composite layer of above materials, and the metal silicide may be NiSi, CoS, $TiSi_2$ or WSi. Alternatively, the material of the gate 204 may be a metal, such as W, WN, TiN, Ta, TaN, Mo, or alloy or composite layer of above materials. The material of the gate oxide may be silicon oxide or high k oxide, such as Hf containing oxide. The Hf containing oxide may be HfO_2, HfSiON or HfSiO. The previously described physical channel width and physical channel length in the disclosure can be defined in Fig. 21. The reference mark of W is defined as the physical channel width of the transistor, the length of the gate 204 crossing over the diffusion region 200; the reference mark of L is defined as the physical channel length of the transistor, the width of the gate 204 over the diffusion region 200.

[00536] Referring to Fig. 22, alternatively, a transistor may include a gate 204 with multiple portions 204_1-204_n over one or more diffusion regions 200. The reference marks of W_1-W_n are defined as the physical channel width of each portion 204_1-204_n of the gate 204, the length of each portion 204_1-204_n of the gate 204 crossing over the diffusion region 200; the

reference mark of L is defined as the physical channel length of one of the portions 204_1-204_n of the gate 204, the width of one of the portions 204_1-204_n of the gate 204 over the diffusion region 200. In this case, the physical channel width W of the transistor is the summation of the physical channel widths W_1-W_n of each portions 204_1-204_n of the gate 204, and the physical channel length L of the transistor is the physical channel length L of one of the portions 204_1-204_n of the gate 204.

[00537] Figs. 23A-23M show cross-sectional views for packaging a DRAM chip using the previously described process, and the elements, shown in Figs. 23A-23M, indicated by same reference numbers as those indicating the previously described elements can be referred to as the above description about them. Referring to Figs. 23A, a DRAM wafer 10 includes multiple memory cells (not shown), multiple off-chip circuits and multiple internal circuits 20 in or on the silicon substrate 1. The DRAM wafer 10 may include an electrical fuse 25 and a laser fuse 26 over the silicon substrate 1, and the electrical fuse 25 and laser fuse 26 are connected to fine-line metal layers 30 over the silicon substrate 1. The electrical fuse 25 is composed of a polysilicon layer 251 having a thickness between 200 and 2,000 angstroms and a metal-silicide layer 252 having a thickness between 1,000 and 3,000 angstroms on the polysilicon layer 251. The metal-silicide layer 252 may contain titanium, cobalt, nickel or tungsten. The electrical fuse 25 in an unblown condition may have a sheet resistance of between 1 and 15 ohms/square. There may be an oxide-containing insulating layer having a dielectric constant of less than 3 on and/or under the electrical fuse 25. The laser fuse 26 may contain copper, aluminum or polysilicon. An opening 526 in the passivation layer 5 is formed over the laser fuse 26 and exposes a silicon-oxide layer over the laser fuse 26.

[00538] Next, an electrical testing process in a wafer level can be performed to verify good dies, non-repairable bad dies and repairable bad dies. Next, a step of laser repairing the repairable bad dies can be performed. In the step of laser repairing the repairable bad dies, the laser fuse 26 can be blown by laser light, such that the metal traces connected to both ends of the laser fuse 26 becomes an open circuit, as shown in Fig. 23B. Accordingly, the repairable bad dies possibly turn out to be good dies.

[00539] Next, referring to Fig. 23C, a polymer layer 95 can be formed on the passivation layer 5, on the silicon-oxide layer on the laser fuse 26 and on the blown portion of the laser fuse 26, with multiple openings 950 in the polymer layer 95 exposing multiple contact pads 600, such as aluminum pads or copper pads, exposed by multiple openings 50 in the

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passivation layer 5. The step of forming the polymer layer 95 can be referred to as the step of forming the polymer layer 95 on the passivation layer 5 as shown in Fig. 15C.

[00540] Next, referring to Fig. 23D, an adhesion/barrier/seed layer 8011 is formed on the polymer layer 95 and on the contact pads 600, which can be referred to as the step of forming the adhesion/barrier/seed layer 8011 on the polymer layer 95 and on the contact pads 600 as shown in Fig. 15D. Next, referring to Fig. 23E, a photoresist layer 71 is formed on the adhesion/barrier/seed layer 8011, with multiple openings 710 in the photoresist layer 71 exposing a seed layer of the adhesion/barrier/seed layer 8011, which can be referred to as the step of forming the photoresist layer 71 on the adhesion/barrier/seed layer 8011 as shown in Fig. 15E. Next, referring to Fig. 23F, a bulk conduction layer 8012 is formed over the adhesion/barrier/seed layer 8011 exposed by the openings 710 in the photoresist layer 71, which can be referred to as the step of forming the bulk conduction layer 8012 on the adhesion/barrier/seed layer 8011 as shown in Fig. 15F. Next, referring to Fig. 23G, the photoresist layer 71 is removed from the seed layer of the adhesion/barrier/seed layer 8011, which can be referred to as the step of removing the photoresist layer 71 as shown in Fig. 15G. Next, referring to Fig. 23H, the adhesion/barrier/seed layer 8011 not under the bulk conduction layer 8012 is removed, which can be referred to as the step of removing the adhesion/barrier/seed layer 8011 not under the bulk conduction layer 8012 as shown in Fig. 15H. Accordingly, the patterned circuit layer 801 can be formed with the adhesion/barrier/seed layer 8011 and the bulk conduction layer 8012 over the adhesion/barrier/seed layer 8011. The patterned circuit layer 801 may have a left portion connecting multiple of the internal circuits 20, without being connected to an external circuit through an opening in the polymer layer 99, and a right portion, for a relocation objective, readily connecting an off-chip circuit 40 to an external circuit through the opening 990 in the polymer layer 99.

[00541] Next, referring to Fig. 23I, a polymer layer 99 can be formed on the patterned circuit layer 801 and on the polymer layer 95, with multiple openings 990 in the polymer layer 99 exposing multiple contact points 8000 of the patterned circuit layer 801. The step of forming the polymer layer 99 on the patterned circuit layer 801 and on the polymer layer 95 can be referred to as the step of forming the polymer layer 99 on the patterned circuit layer 802 and on the polymer layer 98 as shown in Fig. 15K. The patterned circuit layer 801 may have a left portion connecting multiple of the internal circuits 20, without being connected to an external circuit through any opening in the polymer layer 99, and all of the left portion is covered by the polymer layer 99, and a right portion, for a relocation objective, readily

connecting an off-chip circuit 40 to an external circuit through the opening 990 in the polymer layer 99.

[00542] Next, referring to Fig. 23J, another electrical testing process in a wafer level can be optionally performed to verify good dies, non-repairable bad dies and repairable bad dies. Next, a step of E-fuse repairing the repairable bad dies can be performed. In the step of E-fuse repairing the repairable bad dies, an electric current between 0.05 and 2 amperes passes through the electrical fuse 25 for a time between 50 and 1,800 microseconds, and preferably an electric current between 0.1 and 1 amperes passes through the electrical fuse 25 for a time between 100 and 900 microseconds, leading the electrical fuse 25 to be blown. At this time, the electrical fuse 25 has a portion having an electrical current only pass through the polysilicon layer 251 thereof but not pass through the metal-silicide layer 252 thereof. Accordingly, the repairable bad dies possibly turn out to be good dies. The blown electrical fuse 25 may have a sheet resistance between 100 and 10,000 ohms/square. After the step of E-fuse repairing the repairable bad dies, another electrical testing process in a wafer level can be optionally performed to verify good dies, non-repairable bad dies and repairable bad dies.

[00543] Next, the DRAM wafer 10 can be cut into multiple DRAM chips 10' using a mechanical cutting process or using a laser cutting process, as shown in Fig. 23K. The non-repairable bad dies can be discarded without being packaged in the following processes. An over-passivation scheme 102 shown in Fig. 23K includes the patterned circuit layer 801 and the polymer layers 95 and 99, and the openings 950 in the polymer layer 95 are over the regions of the metal pads or traces 600 exposed by the openings 50 in the passivation layer 5, and the opening 990 in the polymer layer 99 is over the contact point 8000 of the patterned circuit layer 801 and exposes it.

[00544] Next, referring to Fig. 23L, one of the DRAM chips 10' can be mounted to a printed circuit board (PCB) 13, ball-grid-array (BGA) substrate, via an adhesive material 11, such as silver epoxy. Next, a wire 89', such as gold wire, copper wire or aluminum wire, can be ball bonded on the contact point 8000 exposed by the opening 990 in the polymer layer 99 and wedge bonded on a contact point 15 of the printed circuit board 13. Next, a polymer material, such as epoxy-based material, can be molded over the printed circuit board (PCB) 13, enclosing the wire 89' and the DRAM chip 10'. Next, the printed circuit board (PCB) 13 can be singularized into multiple portions using a mechanical cutting process. Next, multiple solder balls 19 containing bismuth, indium, a tin-lead alloy, a tin-silver alloy or a tin-silver-copper

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alloy can be ball mounted onto a bottom surface of the singularized printed circuit board (PCB) 13.

[00545] Alternatively, multiple DRAM chips 10' can be stacked over the printed circuit board (PCB) 13, as shown in Fig. 23M. A bottom one of the DRAM chips 10' can be first mounted to the printed circuit board (PCB) 13, ball-grid-array (BGA) substrate, via an adhesive material 11, such as silver epoxy. Next, a wire 89', such as gold wire, copper wire or aluminum wire, can be ball bonded on the contact point 8000 of the bottom one of the DRAM chips 10', exposed by the opening 990 in the polymer layer 99 and wedge bonded on a contact point 15 of the printed circuit board 13. Next, a dump bump, such as silicon or copper, can be adhered to a top surface of the bottom one of the DRAM chips 10' via an adhesive material 11, such as silver epoxy. Next, a top one of the DRAM chips 10' can be mounted to the dummy bump 19, via an adhesive material 11, such as silver epoxy. Next, a wire 89', such as gold wire, copper wire or aluminum wire, can be ball bonded on the contact point 8000 of the top one of the DRAM chips 10', exposed by the opening 990 in the polymer layer 99 and wedge bonded on the contact point 15 of the printed circuit board 13. The only one contact pad 15 of the printed circuit board (PCB) 13 can be connected to the two contact points 8000 of the top and bottom chips 10' through the two wirebonded wires 89'.

[00546] Referring to Fig. 23N showing a top view of a chip package for the DRAM chip 10' and to Figs. 23A-23M, original pads 600 exposed by openings in a passivation layer 5 are aligned in a center line of the DRAM chip 10', and relocated pads 8000 connected to the original pads 600 through the patterned circuit layer 801 over the passivation layer 5 are arranged close to the edges of the DRAM chip 10', leading the relocated pads 8000 to be readily wirebonded by the wires 89'.

[00547] After one or more DRAM chips 10' are packaged as shown in Figs. 21L and 21M, an electrical testing process can be performed to initially verify good packages, non-repairable bad packages and repairable bad packages. The initially verified repairable bad packages can be repaired by the previously described E-fuse repairing process. Next, another electrical testing process can be performed to check if the repaired packages are good. Next, the initially verified good packages and the repaired good packages can be burned in. Next, another electrical testing process can be performed to check if the burned-in packages continue good.

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[00548] Alternatively, other chips, such as flash memory chips, SRAM chips or logic chips, can be packaged as the process for packaging the DRAM chips 10' as shown in Figs. 23A-23M is performed.

[00549] The above description focus on a top post-passivation technology, that is, the over-passivation scheme 102 can be formed over the passivation layer 5 at the active side of the silicon substrate 1. Figs. 1B-1D, 3B-3D, 5B, 5K, 5S, 5U, 5V-5Z, 7B-7D, 8A-8F, 10A-10I, 12B-12D, 14B-14D, 15H, 15K-15M, 16L, 16M, 17J, 18I, 19H, 20 and 23K show that various types of the over-passivation schemes 102 formed over the passivation layer 5 at the active side of the silicon substrate 1. The below description focus on a bottom structure technology, that is, a bottom scheme 103 can be formed at the backside 1a of the thinned silicon substrate 1. The elements having same reference numbers in this specification can be reference to one another.

[00550] Fig. 24A shows the silicon substrate 1 and other elements as described above in the semiconductor wafer 10, and the silicon substrate 1 has a thickness t1 between 600 and 1000 micrometers, between 50 micrometers and 1 millimeter or between 75 and 250 micrometers. Alternatively, the silicon substrate 1 can be replaced with other semiconductor substrate, such as silicon-germanium (SiGe) substrate or gallium arsenide (GaAs) substrate.

[00551] Referring to Fig. 24B, the semiconductor wafer 10 is flipped over, and then the silicon substrate 1 is thinned to a thickness t2 between 1 and 10 micrometers, between 3 and 50 micrometers or between 10 and 150 micrometers by mechanically grinding or chemically mechanically polishing (CMP) a backside 1a of the silicon substrate 1. Alternatively, the previously described step of flipping over the semiconductor wafer 10 can be performed after the previously described step of thinning the silicon substrate 1, to perform the following processes.

[00552] Next, referring to Fig. 24C, multiple through-silicon vias (TSV) 11a, 11b, 11c, 11d and 11e are formed in the thinned silicon substrate 1 and in at least one dielectric layer 30, exposing regions 60a of the fine-line metal layers 60 and 632c, and an insulating layer 3 is formed on the backside 1a of the thinned silicon substrate 1 and on sidewalls of the through-silicon vias 11a, 11b, 11c, 11d and 11e. The through-silicon vias 11a, 11b, 11c, 11d and 11e penetrate completely through the thinned silicon substrate 1 and the dielectric layer(s) 30. The through-silicon vias 11a, 11b, 11c, 11d and 11e may have a diameter or width W1 between 5 and 100 micrometers or between 3 and 50 micrometers, and a depth between 1 and 10 micrometers, between 3 and 50 micrometers or between 10 and 150 micrometers. The

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insulating layer 3, for example, may include a nitride layer, such as silicon-nitride layer, a polymer layer, such as polyimide layer, benzocyclobutene layer or polybenzoxazole layer, a silicon-oxynitride layer, a silicon-carbon-nitride (SiCN) layer, a silicon-oxycarbide (SiOC) layer or a silicon-oxide layer.

[00553] Figs. 24D-24H are cross-sectional views showing a process of forming the through-silicon vias 11a, 11b, 11c, 11d and 11e and the insulating layer 3 according to the present disclosure. Referring to Fig. 24D, after the step illustrated in Fig. 24B, a photoresist layer 28 is spin-on coated or laminated on the backside 1a of the thinned silicon substrate 1, and multiple ring-shaped openings 28a are formed in the photoresist layer 28, exposing the backside 1a of the thinned silicon substrate 1, using an exposure process and developing process. Fig. 24E is a schematic top view showing the ring-shaped openings 28a in the photoresist layer 28. Next, referring to Fig. 24F, multiple through-silicon ring-shaped openings 11g each having a transverse width W2 between 1 and 20 micrometer are formed in the thinned silicon substrate 1 and in at least one dielectric layer 30, penetrating completely through the thinned silicon substrate 1 and the dielectric layer(s) 30, by dry etching the thinned silicon substrate 1 and the dielectric layer(s) 30 under the ring-shaped openings 28a in the photoresist layer 28, for example, using anisotropic reactive ion etching. Next, the photoresist layer 28 is removed, as shown in Fig. 24G. Next, referring to Fig. 24H, the insulating layer 3, such as polymer layer, polyimide layer, benzocyclobutene (BCB) layer, polybenzoxazole (PBO) layer, silicon-nitride layer, silicon-oxide layer, silicon-oxynitride layer, silicon-oxycarbide (SiOC) layer or silicon-carbon-nitride (SiCN) layer, having a thickness t3 between 0.5 and 20 micrometers or between 0.01 and 5 micrometers is formed in the through-silicon ring-shaped openings 11g and on the backside 1a of the thinned silicon substrate 1. Next, multiple portions of the thinned silicon substrate 1 surrounded by the insulating layer 3 in the through-silicon ring-shaped openings 11g are removed using a dry etching process, such as fluorine and carbon based anisotropic reactive ion etching, and accordingly the through-silicon vias 11a, 11b, 11c, 11d and 11e are formed in the thinned silicon substrate 1 and in at least one dielectric layer 30, exposing the regions 60a of the fine-line metal layers 60 and 632c, as shown in Fig. 24C, and the insulating layer 3 is formed on the backside 1a of the thinned silicon substrate 1 and on the sidewalls of the through-silicon vias 11a, 11b, 11c, 11d and 11e.

[00554] Figs. 24I-24N are cross-sectional views showing another process of forming the through-silicon vias 11a, 11b, 11c, 11d and 11e and the insulating layer 3 according to the present disclosure. Referring to Fig. 24I, an etching stop layer 3a, such as silicon-nitride layer,

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silicon-oxide layer or polymer layer, having a thickness t4 between 0.3 and 40 micrometers is formed on the backside 1a of the thinned silicon substrate 1. For example, the etching stop layer 3a can be formed by a suitable process or processes, e.g., by depositing a silicon-nitride or silicon-carbon-nitride layer having a thickness between 0.2 and 1.2 micrometers on the backside 1a of the thinned silicon substrate 1 using a chemical mechanical deposition (CVD) process. Alternatively, the etching stop layer 3a can be formed by a suitable process or processes, e.g., by depositing a silicon-oxide or silicon-oxycarbide layer having a thickness between 0.2 and 1.2 micrometers on the backside 1a of the thinned silicon substrate 1 using a chemical mechanical deposition (CVD) process, and then depositing a silicon-nitride or silicon-carbon-nitride layer having a thickness between 0.2 and 1.2 micrometers on the silicon-oxide or silicon-oxycarbide layer using a chemical mechanical deposition (CVD) process. Alternatively, the etching stop layer 3a can be formed by a suitable process or processes, e.g., by depositing a silicon-nitride layer having a thickness between 0.2 and 1.2 micrometers on the bottom backside 1a of the thinned silicon substrate 1 using a chemical mechanical deposition (CVD) process, and then coating a polymer layer having a thickness between 2 and 30 micrometers on the silicon-nitride or silicon-carbon-nitride layer.

[00555] Referring to Fig. 24J, after the step illustrated in Fig. 24I, a photoresist layer 54 is spin-on coated or laminated on the etching stop layer 3a, and multiple openings 54a are formed in the photoresist layer 54 and expose the etching stop layer 3a using an exposure process and developing process. Next, referring to Fig. 24K, the through-silicon vias 11a, 11b, 11c, 11d and 11e are formed in the thinned silicon substrate 1 and in at least one dielectric layer 30, penetrating completely through the etching stop layer 3a, the thinned silicon substrate 1 and the dielectric layer(s) 30 and exposing the regions 60a of the fine-line metal layers 60 and 632c, by dry etching the etching stop layer 3a, the thinned silicon substrate 1 and the dielectric layer(s) 30 under the openings 54a in the photoresist layer 54, for example, using fluorine and carbon based anisotropic reactive ion etching. Next, the photoresist layer 28 is removed, as shown in Fig. 24L. Next, referring to Fig. 24M, an insulating layer 3b, such as polymer layer, polyimide layer, benzocyclobutene (BCB) layer, polybenzoxazole (PBO) layer, silicon-nitride layer, silicon-oxide layer, silicon-oxynitride layer, silicon-oxycarbide (SiOC) layer or silicon-carbon-nitride (SiCN) layer, having a thickness t5 between 0.1 and 10 micrometers is formed on the sidewalls of the through-silicon vias 11a, 11b, 11c, 11d and 11e, on the etching stop layer 3a and on the regions 60a of the fine-line metal layers 60 and 632c exposed by the through-silicon vias 11a, 11b, 11c, 11d and 11e. Next,

referring to Fig. 24N, the insulating layer 3b formed on the etching stop layer 3a and on the regions 60a of the fine-line metal layers 60 and 632c are removed using a dry etching process, such as anisotropic reactive ion etching. Accordingly, the regions 60a of the fine-line metal layers 60 and 632c are exposed through the through-silicon vias 11a, 11b, 11c, 11d and 11e and the etching stop layer 3a has a top surface uncovered by the insulating layer 3b. The etching stop layer 3a and the insulating layer 3b composes the insulating layer 3.

[00556] For easy description, the insulating layer 3 shown in the following process can be referenced by the insulating layer 3 made as illustrated in Figs. 24D-24H or the insulating layer 3, composed of the etching stop layer 3a and the insulating layer 3b, made as illustrated in Figs. 24I-24N.

[00557] Figs. 25A-25L are cross-sectional views showing a process for forming a bottom scheme 103 of a bottom structure technology at a backside of a semiconductor wafer according to the present disclosure. Referring to Fig. 25A, after forming the insulating layer 3 and the through-silicon vias 11a, 11b, 11c, 11d and 11e, a metal layer 4 can be formed on the insulating layer 3, on the regions 60a of the fine-line metal layers 60 and 632c exposed by the through-silicon vias 11a, 11b, 11c, 11d and 11e and in the through-silicon vias 11a, 11b, 11c, 11d and 11e. The metal layer 4 can be formed by a suitable process or processes, e.g., by depositing an adhesion/barrier layer 4a on the insulating layer 3, in the through-silicon vias 11a, 11b, 11c, 11d and 11e, and on the regions 60a of the fine-line metal layers 60 and 632c exposed by the through-silicon vias 11a, 11b, 11c, 11d and 11e, and then depositing a seed layer 4b on the adhesion/barrier layer 4a.

[00558] The adhesion/barrier layer 4a at the bottom of the metal layer 4 may be formed by a suitable process or processes, e.g., by sputtering or chemical vapor depositing (CVD) a titanium-containing layer, such as titanium-nitride layer, titanium layer or titanium-tungsten-alloy layer, having a thickness smaller than 1 micrometer, such as between 0.005 and 0.8 micrometers, and preferably between 0.05 and 0.5 micrometers, on the insulating layer 3, at the sidewalls of the through-silicon vias 11a, 11b, 11c, 11d and 11e, and on an aluminum layer, an electroplated copper layer, a tantalum-nitride layer, a titanium-nitride layer, a tantalum layer or a titanium layer of the fine-line metal layers 60 and 632c exposed by the through-silicon vias 11a, 11b, 11c, 11d and 11e. Alternatively, the adhesion/barrier layer 4a at the bottom of the metal layer 4 may be formed by a suitable process or processes, e.g., by sputtering or chemical vapor depositing a chromium-containing layer, such as chromium layer,

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having a thickness smaller than 1 micrometer, such as between 0.005 and 0.8 micrometers, and preferably between 0.05 and 0.5 micrometers, on the insulating layer 3, at the sidewalls of the through-silicon vias 11a, 11b, 11c, 11d and 11e, and on an aluminum layer, an electroplated copper layer, a tantalum-nitride layer, a titanium-nitride layer, a tantalum layer or a titanium layer of the fine-line metal layers 60 and 632c exposed by the through-silicon vias 11a, 11b, 11c, 11d and 11e. Alternatively, the adhesion/barrier layer 4a at the bottom of the metal layer 4 may be formed by a suitable process or processes, e.g., by sputtering or chemical vapor depositing a tantalum-containing layer, such as tantalum layer or tantalum-nitride layer, having a thickness smaller than 1 micrometer, such as between 0.005 and 0.8 micrometers, and preferably between 0.05 and 0.5 micrometers, on the insulating layer 3, at the sidewalls of the through-silicon vias 11a, 11b, 11c, 11d and 11e, and on an aluminum layer, an electroplated copper layer, a tantalum-nitride layer, a titanium-nitride layer, a tantalum layer or a titanium layer of the fine-line metal layers 60 and 632c exposed by the through-silicon vias 11a, 11b, 11c, 11d and 11e.

[00559] The seed layer 4b at the top of the metal layer 4 may be formed by a suitable process or processes, e.g., by sputtering or chemical vapor depositing a copper layer, an aluminum layer, a nickel layer or a silver layer with a thickness smaller than 1 micrometer, such as between 0.005 and 1 micrometers, and preferably between 0.05 and 0.5 micrometers, on the adhesion/barrier layer 4a of any previously described material. Alternatively, the seed layer 4b at the top of the metal layer 4 may be formed by a suitable process or processes, e.g., by sputtering or chemical vapor depositing a gold layer with a thickness smaller than 1 micrometer, such as between 0.005 and 0.5 micrometers, and preferably between 0.05 and 0.2 micrometers, on the adhesion/barrier layer 4a of any previously described material.

[00560] Referring to Fig. 25B, after forming the metal layer 4, a photoresist layer 29, such as positive-type photoresist layer or negtive-type photoresist layer, having a thickness larger than 1.5 micrometers, such as between 5 and 50 micrometers, and preferably between 10 and 25 micrometers, is formed on the seed layer 4b of the metal layer 4 by a spin-on coating process, a lamination process, a screen-printing process or a spraying process. Next, the photoresist layer 29 is patterned with the processes of exposure and development to form multiple openings 29a in the photoresist layer 29 exposing the seed layer 4b of the metal layer 4, as shown in Fig. 25C. A 1X stepper or 1X contact aligner can be used to expose the photoresist layer 29 during the process of exposure.

[00561] For example, the photoresist layer 29 can be formed by a suitable process or processes, e.g., by spin-on coating a positive-type photosensitive polymer layer having a thickness between 5 and 30 micrometers, and preferably between 10 and 25 micrometers, on the seed layer 4a of the metal layer 4, then exposing the photosensitive polymer layer using a 1X stepper or a contact aligner with at least two of G-line, H-line and I-line, and G-line has a wavelength ranging from, e.g., about 434 to 438nm, H-line has a wavelength ranging from, e.g., about 403 to 407nm, and I-line has a wavelength ranging from, e.g., about 363 to 367nm, then developing the exposed polymer layer by spraying and puddling a developer on the photoresist layer 29 or by immersing the photoresist layer 29 into a developer, and then cleaning the semiconductor wafer using deionized wafer and drying the semiconductor wafer by spinning the semiconductor wafer. After development, a scum removal process of removing the residual polymeric material or other contaminants from the seed layer 4b of the metal layer 4 may be conducted by using an O_2 plasma or a plasma containing fluorine of below 200PPM and oxygen. By these processes, the photoresist layer 29 can be patterned with the openings 29a exposing the seed layer 4b of the metal layer 4.

[00562] Next, referring to Fig. 25D, a bulk metal layer 9 is formed in the openings 29a and on the seed layer 4b of the metal layer 4 exposed by the openings 29a by a process including an electroplating process. The bulk metal layer 9 may have a thickness larger than 1 micrometer, such as between 1 and 50 micrometers, between 2 and 20 micrometers or between 5 and 150 micrometers, and larger than that of the seed layer 4b, that of the adhesion/barrier layer 4a and that of each of the fine-line metal layers 60, respectively. The bulk metal layer 9 may include copper, gold, nickel, aluminum, silver, platinum, solder or a composite of the previously described materials.

[00563] For example, the bulk metal layer 9 can be composed of a single metal layer formed by a suitable process or processes, e.g., by electroplating a copper layer, to a thickness between 1 and 50 micrometers, between 2 and 20 micrometers or between 5 and 150 micrometers, in the openings 29a and on the seed layer 4b, preferably the previously described copper layer 4b, exposed by the openings 29a with an electroplating solution containing $CuSO_4$, $Cu(CN)_2$ or $CuHPO_4$.

[00564] Alternatively, the bulk metal layer 9 can be composed of a single metal layer formed by a suitable process or processes, e.g., by electroplating an aluminum layer, to a thickness between 1 and 50 micrometers, between 2 and 20 micrometers or between 5 and 150

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micrometers, in the openings 29a and on the seed layer 4b, preferably formed by a suitable process or processes, e.g., by the previously described aluminum layer or copper layer 4b, exposed by the openings 29a.

[00565] Alternatively, the bulk metal layer 9 can be composed of a single metal layer formed by a suitable process or processes, e.g., by electroplating a gold layer, to a thickness between 0.5 and 30 micrometers, between 1 and 10 micrometers or between 5 and 150 micrometers, in the openings 29a and on the seed layer 4b, preferably the previously described gold layer 4b, exposed by the openings 29a with an electroplating solution containing gold of between 1 and 20 grams per litter (g/l), and preferably between 5 and 15 g/l, and sulfite ion of 10 and 120 g/l, and preferably between 30 and 90 g/l. The electroplating solution may further include sodium ion, to be turned into a solution of gold sodium sulfite ($Na_3Au(SO_3)_2$), or may further include ammonium ion, to be turned into a solution of gold ammonium sulfite ($(NH_4)_3[Au(SO_3)_2]$). The operational parameters of electroplating the gold layer are described below:

1. The previously described electroplating solution can be at a temperature of between 30 and 70°C, and preferably between 45 and 65°C, to electroplate the gold layer on the seed layer 4b of the metal layer 4 exposed by the openings 29a.
2. The previously described electroplating solution can be used to electroplate the gold layer on the seed layer 4b of the metal layer 4 exposed by the openings 29a through an electric current with a current density at between 1 and 10 mA/cm^2, and preferably between 4 and 6 mA/cm^2.
3. The previously described electroplating solution may have a pH value of between 6 and 9, and preferably of between 7 and 8.5, to electroplate the gold layer on the seed layer 4b of the metal layer 4 exposed by the openings 29a.

[00566] Alternatively, the bulk metal layer 9 can be composed of double metal layers formed by a suitable process or processes, e.g., by electroplating a copper layer, to a thickness between 1 and 50 micrometers, between 2 and 20 micrometers or between 5 and 150 micrometers, in the openings 29a and on the seed layer 4b, preferably the previously described copper layer 4b, exposed by the openings 29a using the previously described electroplating solution for electroplating copper, and then electroplating a nickel layer, a top metal layer of the bulk metal layer 9, to a thickness between 1 and 15 micrometers, and preferably between 2

and 10 micrometers, in the openings 29a and on the electroplated copper layer in the openings 29a using an electroplating solution containing $NiSO_4$ or Ni sulfamate or $Ni(NH_2SO_3)_2$ or electroless plating a nickel layer, a top metal layer of the bulk metal layer 9, to a thickness between 1 and 15 micrometers, and preferably between 2 and 10 micrometers, in the openings 29a and on the electroplated copper layer in the openings 29a using an electroless plating solution containing Ni and $NaPO_2H_2$ (Sodium Hypophosphite).

[00567] Alternatively, the bulk metal layer 9 can be composed of a single metal layer formed by a suitable process or processes, e.g., by electroplating a nickel layer, to a thickness between 1 and 50 micrometers, between 2 and 20 micrometers or between 5 and 150 micrometers, in the openings 29a and on the seed layer 4b, preferably formed by a suitable process or processes, e.g., by the previously described copper layer or nickel layer 4b, exposed by the openings 29a using the previously described electroplating solution for electroplating nickel.

[00568] Alternatively, the bulk metal layer 9 can be composed of triple metal layers formed by a suitable process or processes, e.g., by electroplating a copper layer 126, to a thickness between 1 and 50 micrometers, between 2 and 20 micrometers or between 5 and 150 micrometers, in the openings 29a and on the seed layer 4b, preferably the previously described copper layer 4b, exposed by the openings 29a using the previously described electroplating solution for electroplating copper, next electroplating or electroless plating a nickel layer 127, to a thickness between 1 and 15 micrometers, and preferably between 2 and 10 micrometers, in the openings 29a and on the electroplated copper layer in the openings 29a using the previously described electroplating solution for electroplating or electroless plating nickel, and then electroplating a gold layer 128, a top metal layer of the bulk metal layer 9, to a thickness between 0.005 and 1 micrometers, and preferably between 0.05 and 0.1 micrometers, in the openings 29a and on the electroplated or electroless plated nickel layer in the openings 29a using the previously described electroplating solution for electroplating gold, or electroless plating a gold layer 128, to a thickness between 0.005 and 1 micrometers, and preferably between 0.05 and 0.1 micrometers, in the openings 29a and on the electroplated or electroless plated nickel layer in the openings 29a using an electroless plating solution containing gold salt, such as $AuNaSO_3$ or AuCN and a reduction agent, such as benzoic or phenyl.

[00569] Alternatively, the bulk metal layer 9 can be composed of triple metal layers formed by a suitable process or processes, e.g., by electroplating a copper layer 126, to a

thickness between 1 and 50 micrometers, between 2 and 20 micrometers or between 5 and 150 micrometers, in the openings 29a and on the seed layer 4b, preferably the previously described copper layer 4b, exposed by the openings 29a using the previously described electroplating solution for electroplating copper, next electroplating or electroless plating a nickel layer 127, to a thickness between 1 and 15 micrometers, and preferably between 2 and 10 micrometers, in the openings 29a and on the electroplated copper layer in the openings 29a using the previously described electroplating solution for electroplating or electroless plating nickel, and then electroplating a palladium layer 128, a top metal layer of the bulk metal layer 9, to a thickness between 0.005 and 5 micrometers, and preferably between 0.05 and 1 micrometers, in the openings 29a and on the electroplated or electroless plated nickel layer in the openings 29a using an electroplating solution containing palladium and ammonia, or electroless plating a palladium layer 128, a top metal layer of the bulk metal layer 9, to a thickness between 0.005 and 1 micrometers, and preferably between 0.05 and 0.1 micrometers, in the openings 29a and on the electroplated or electroless plated nickel layer in the openings 29a using an electroless plating solution containing palladium, ammonia and a reduction agent, such as hydrozine.

[00570] Alternatively, the bulk metal layer 9 can be composed of four metal layers formed by a suitable process or processes, e.g., by electroplating a copper layer, to a thickness between 1 and 50 micrometers, between 2 and 20 micrometers or between 5 and 150 micrometers, in the openings 29a and on the seed layer 4b, preferably the previously described copper layer 4b, exposed by the openings 29a using the previously described electroplating solution for electroplating copper, next electroplating or electroless plating a nickel layer, to a thickness between 1 and 15 micrometers, and preferably between 2 and 10 micrometers, in the openings 29a and on the electroplated copper layer in the openings 29a using the previously described electroplating solution for electroplating or electroless plating nickel, next electroplating or electroless plating a palladium layer, to a thickness between 0.005 and 5 micrometers, and preferably between 0.05 and 1 micrometers, in the openings 29a and on the electroplated or electroless plated nickel layer in the openings 29a using the previously described electroplating solution for electroplating or electroless plating palladium, and then electroplating or electroless plating a gold layer, a top metal layer of the bulk metal layer 9, to a thickness between 0.005 and 1 micrometers, and preferably between 0.05 and 0.1 micrometers, in the openings 29a and on the electroplated or electroless plated palladium layer in the openings 29a using the previously described electroplating solution for electroplating or electroless plating gold.

[00571] Referring to Fig. 25E, after forming the bulk metal layer 9, the photoresist layer 29 is removed using an inorganic solution or using an organic solution with amide. Some residuals from the photoresist layer 29 could remain on the metal layer 4 not under the bulk metal layer 9. Thereafter, the residuals can be removed from the metal layer 4 with a plasma, such as an O_2 plasma or a plasma containing fluorine of below 200PPM and oxygen.

[00572] Next, referring to Fig. 25F, the metal layer 4 not under the bulk metal layer 9 is removed by etching the seed layer 4b not under the bulk metal layer 9, and then etching the adhesion/barrier layer 4a not under the bulk metal layer 9.

[00573] In a case, the seed layer 4b and the adhesion/barrier layer 4a not under the bulk metal layer 9 can be subsequently removed by a dry etching method. As to the dry etching method, both the seed layer 4b and the adhesion/barrier layer 4a not under the bulk metal layer 9 can be subsequently removed by an Ar sputtering etching process; alternatively, both the seed layer 4b and the adhesion/barrier layer 4a not under the bulk metal layer 9 can be subsequently removed by a reactive ion etching (RIE) process; alternatively, the seed layer 4b not under the bulk metal layer 9 can be removed by an Ar sputtering etching process, and the adhesion/barrier layer 4a not under the bulk metal layer 9 can be removed by a reactive ion etching (RIE) process.

[00574] In another case, the seed layer 4b and the adhesion/barrier layer 4a not under the bulk metal layer 9 can be subsequently removed by a wet etching method. As to the wet etching method, when the seed layer 4b is a copper layer, it can be etched with a solution containing NH_4OH or with a solution containing H_2SO_4; when the seed layer 4b is a gold layer, it can be etched with an iodine-containing solution, such as a solution containing potassium iodide; when the adhesion/barrier layer 4a is a titanium-tungsten-alloy layer, it can be etched with a solution containing hydrogen peroxide or with a solution containing NH_4OH and hydrogen peroxide; when the adhesion/barrier layer 4a is a titanium layer, it can be etched with a solution containing hydrogen fluoride or with a solution containing NH_4OH and hydrogen peroxide; when the adhesion/barrier layer 4a is a chromium layer, it can be etched with a solution containing potassium ferricyanide.

[00575] In another case, the seed layer 4b, such as copper, not under the bulk metal layer 9 can be removed by a solution containing NH_4OH or a solution containing H_2SO_4, and the adhesion/barrier layer 210 not under the bulk metal layer 9 can be removed by a reactive ion etching (RIE) process or an Ar sputtering etching process.

[00576] In another case, the seed layer 4b, such as gold, not under the bulk metal layer 9 can be etched with an iodine-containing solution, such as a solution containing potassium iodide, and the adhesion/barrier layer 4a not under the bulk metal layer 9 can be removed by a reactive ion etching (RIE) process or an Ar sputtering etching process.

[00577] After etching the adhesion/barrier layer 4a not under the bulk metal layer 9, multiple interconnecting structures 88 provided by the metal layers 4 and 9 can be formed in the through-silicon vias 11a, 11b, 11c, 11d and 11e, on the insulating layer 3 and at the backside 1a of the thinned silicon substrate 1, and sidewalls of the bulk metal layer 9 are not covered by the metal layer 4.

[00578] Referring to Fig. 25G, after the step illustrated in Fig. 25F, a polymer layer 14 can be formed on the topmost layer of copper, gold, aluminum, nickel or palladium of the previously described various bulk metal layer 9 and on the insulating layer 3 using a process including a spin-on coating process, a lamination process, a screen-printing process or a spraying process and including a curing process, and an opening 14a in the polymer layer 14 is over a region of the topmost layer of copper, gold, aluminum, nickel or palladium of the previously described various bulk metal layer 9 and exposes it. The polymer layer 14 has a thickness larger than 2 micrometers, such as between 3 and 25 micrometers, and preferably between 5 and 15 micrometers. The material of the polymer layer 14 may include benzocyclobutane (BCB), polyimide (PI), polybenzoxazole (PBO) or epoxy resin.

[00579] In a case, the polymer layer 14 can be formed by a suitable process or processes, e.g., by spin-on coating a negative-type photosensitive polyimide layer having a thickness between 6 and 50 micrometers on the insulating layer 3 and on the topmost layer of copper, gold, aluminum, nickel or palladium of the previously described various bulk metal layer 9, then baking the spin-on coated polyimide layer, then exposing the baked polyimide layer using a 1X stepper or 1X contact aligner with at least two of G-line having a wavelength ranging from, e.g., about 434 to 438nm, H-line having a wavelength ranging from, e.g., about 403 to 407nm, and I-line having a wavelength ranging from, e.g., about 363 to 367nm, illuminating the baked polyimide layer, that is, G-line and H-line, G-line and I-line, H-line and I-line, or G-line, H-line and I-line illuminate the baked polyimide layer, then developing the exposed polyimide layer to form an opening exposing the bulk metal layer 9, then curing or heating the developed polyimide layer at a temperature between 180 and 400°C, between 180 and 250°C, between 250 and 290°C, between 290 and 400°C or between 200 and 390°C for a time

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between 20 and 150 minutes in a nitrogen ambient or in an oxygen-free ambient, the cured polyimide layer having a thickness between 3 and 25 micrometers, and then removing the residual polymeric material or other contaminants from the exposed bulk metal layer 9 with an O_2 plasma or a plasma containing fluorine of below 200PPM and oxygen. By the way, the polymer layer 14 can be formed on the insulating layer 3 and on the topmost layer of copper, gold, aluminum, nickel or palladium of the previously described various bulk metal layer 9, and the opening 14a formed in the polymer layer 14 exposes the region of the topmost layer of copper, gold, aluminum, nickel or palladium of the previously described various bulk metal layer 9.

[00580] In another case, the polymer layer 14 can be formed by a suitable process or processes, e.g., by spin-on coating a positive-type photosensitive polybenzoxazole layer having a thickness between 3 and 25 micrometers on the insulating layer 3 and on the topmost layer of copper, gold, aluminum, nickel or palladium of the previously described various bulk metal layer 9, then baking the spin-on coated polybenzoxazole layer, then exposing the baked polybenzoxazole layer using a 1X stepper or a 1X contact aligner with at least two of G-line having a wavelength ranging from, e.g., about 434 to 438nm, H-line having a wavelength ranging from, e.g., about 403 to 407nm, and I-line having a wavelength ranging from, e.g., about 363 to 367nm, illuminating the baked polybenzoxazole layer, that is, G-line and H-line, G-line and I-line, H-line and I-line, or G-line, H-line and I-line illuminate the baked polybenzoxazole layer, then developing the exposed polybenzoxazole layer to form an opening exposing the bulk metal layer 9, then curing or heating the developed polybenzoxazole layer at a temperature between 150 and 250°C, and preferably between 180 and 250°C, or between 200 and 400°C, and preferably between 250 and 350°C, for a time between 5 and 180 minutes, and preferably between 30 and 120 minutes, in a nitrogen ambient or in an oxygen-free ambient, the cured polybenzoxazole layer having a thickness between 3 and 25μm, and then removing the residual polymeric material or other contaminants from the exposed bulk metal layer 9 with an O_2 plasma or a plasma containing fluorine of below 200PPM and oxygen. By the way, the polymer layer 14 can be formed on the insulating layer 3 and on the topmost layer of copper, gold, aluminum, nickel or palladium of the previously described various bulk metal layer 9, and the opening 14a formed in the polymer layer 14 exposes the region of the topmost layer of copper, gold, aluminum, nickel or palladium of the previously described various bulk metal layer 9.

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[00581] Next, referring to Fig. 25H, an adhesion/barrier layer 16 having a thickness smaller than 1 micrometer, such as between 0.02 and 0.5 micrometers, and preferably between 0.1 and 0.2 micrometers, can be formed on the polymer layer 14 and on the region of the topmost layer of copper, gold, aluminum, nickel or palladium of the previously described various bulk metal layer 9 exposed by the opening 14a by using a physical vapor deposition (PVD) process, such as sputtering process or evaporation process, and then a seed layer 18 having a thickness smaller than 1 micrometer, such as between 0.05 and 0.5 micrometers, and preferably between 0.08 and 0.15 micrometers, can be formed on the adhesion/barrier layer 16 by using a physical vapor deposition (PVD) process, such as sputtering process or evaporation process. The material of the adhesion/barrier layer 16 may include titanium, a titanium-tungsten alloy, titanium nitride, chromium, tantalum, tantalum nitride or a composite of the previously described materials, and the material of the seed layer 18 may include copper, nickel, aluminum, gold, silver, platinum or palladium.

[00582] For example, when the adhesion/barrier layer 16 is formed by a suitable process or processes, e.g., by sputtering a titanium-containing layer, such as a single layer of titanium-tungsten alloy, titanium or titanium nitride, having a thickness smaller than 1 micrometer, such as between 0.005 and 0.8 micrometers, and preferably between 0.05 and 0.5 micrometers, on the polymer layer 14 and on the region of the topmost layer of copper, gold, aluminum, nickel or palladium of the previously described various bulk metal layer 9 exposed by the opening 14a, the seed layer 18 can be formed by a suitable process or processes, e.g., by sputtering a copper layer, a nickel layer, an aluminum layer, a gold layer, a silver layer, a platinum layer or a palladium layer with a thickness smaller than 1 micrometer, such as between 0.005 and 0.5 micrometers, and preferably between 0.05 and 0.2 micrometers, on the titanium-containing layer.

[00583] Alternatively, when the adhesion/barrier layer 16 is formed by a suitable process or processes, e.g., by sputtering a composite layer including a titanium layer having a thickness between 0.01 and 0.15 micrometers on the polymer layer 14 and on the region of the topmost layer of copper, gold, aluminum, nickel or palladium of the previously described various bulk metal layer 9 exposed by the opening 14a and a titanium-tungsten-alloy layer having a thickness between 0.1 and 0.35 micrometers on the titanium layer, the seed layer 18 can be formed by a suitable process or processes, e.g., by sputtering a copper layer, a nickel layer, an aluminum layer, a gold layer, a silver layer, a platinum layer or a palladium layer with a

thickness smaller than 1 micrometer, such as between 0.005 and 0.5 micrometers, and preferably between 0.05 and 0.2 micrometers, on the titanium-tungsten-alloy layer.

[00584] Alternatively, when the adhesion/barrier layer 16 is formed by a suitable process or processes, e.g., by sputtering a tantalum-containing layer, such as a single layer of tantalum or tantalum nitride, having a thickness smaller than 1 micrometer, such as between 0.005 and 0.8 micrometers, and preferably between 0.05 and 0.5 micrometers, on the polymer layer 14 and on the region of the topmost layer of copper, gold, aluminum, nickel or palladium of the previously described various bulk metal layer 9 exposed by the opening 14a, the seed layer 18 can be formed by a suitable process or processes, e.g., by sputtering a copper layer, a nickel layer, an aluminum layer, a gold layer, a silver layer, a platinum layer or a palladium layer with a thickness smaller than 1 micrometer, such as between 0.005 and 0.5 micrometers, and preferably between 0.05 and 0.2 micrometers, on the tantalum-containing layer.

[00585] Alternatively, when the adhesion/barrier layer 16 is formed by a suitable process or processes, e.g., by sputtering a chromium-containing layer, such as a single layer of chromium layer, having a thickness smaller than 1 micrometer, such as between 0.005 and 0.8 micrometers, and preferably between 0.05 and 0.5 micrometers, on the polymer layer 14 and on the region of the topmost layer of copper, gold, aluminum, nickel or palladium of the previously described various bulk metal layer 9 exposed by the opening 14a, the seed layer 18 can be formed by a suitable process or processes, e.g., by sputtering a copper layer, a nickel layer, an aluminum layer, a gold layer, a silver layer, a platinum layer or a palladium layer with a thickness smaller than 1 micrometer, such as between 0.005 and 0.5 micrometers, and preferably between 0.05 and 0.2 micrometers, on the chromium-containing layer.

[00586] Referring to Fig. 25I, after forming the seed layer 18, a photoresist layer 31, such as positive-type photoresist layer or negtive-type photoresist layer, having a thickness larger than 5 micrometers, such as between 10 and 150 micrometers, and preferably between 15 and 50 micrometers, is formed on the seed layer 18 of any previously described material by a spin-on coating process, a lamination process, a screen-printing process or a spraying process. Next, the photoresist layer 31 is patterned with the processes of exposure and development to form an opening 31a in the photoresist layer 31 exposing the seed layer 18 of any previously described material. A 1X stepper or 1X contact aligner can be used to expose the photoresist layer 31 during the process of exposure.

[00587] For example, the photoresist layer 31 can be formed by a suitable process or processes, e.g., by spin-on coating a positive-type photosensitive polymer layer having a thickness larger than 5 micrometers, such as between 10 and 150 micrometers, and preferably between 15 and 50 micrometers, on the seed layer 18 of any previously described material, then exposing the photosensitive polymer layer using a 1X stepper or a contact aligner with at least two of G-line, H-line and I-line, and G-line has a wavelength ranging from, e.g., about 434 to 438nm, H-line has a wavelength ranging from, e.g., about 403 to 407nm, and I-line has a wavelength ranging from, e.g., about 363 to 367nm, then developing the exposed polymer layer by spraying and puddling a developer on the photoresist layer 31 or by immersing the photoresist layer 31 into a developer, and then cleaning the semiconductor wafer using deionized wafer and drying the semiconductor wafer by spinning the semiconductor wafer. After development, a scum removal process of removing the residual polymeric material or other contaminants from the seed layer 18 may be conducted by using an O_2 plasma or a plasma containing fluorine of below 200PPM and oxygen. By these processes, the photoresist layer 31 can be patterned with the opening 31a exposing the seed layer 18.

[00588] Referring to Fig. 25J, after the step illustrated in Fig. 25I, a metal bump or pillar 27 can be formed on the seed layer 18 of any previously described material exposed by the opening 31a and in the opening 31a. The metal bump or pillar 27 may have a thickness larger than 5 micrometers, such as between 5 and 150 micrometers, and preferably between 10 and 100 micrometers, and larger than that of the seed layer 18, that of the adhesion/barrier layer 16 and that of each of the fine-line metal layers 60, respectively. The metal bump or pillar 27 may have a width larger than 1 micrometer, such as between 5 and 150 micrometers, and preferably between 5 and 50 micrometers, and larger than that of each of the fine-line metal layers 60. The material of the metal bump or pillar 27 may include copper, gold, nickel, aluminum, silver, solder, platinum or a composite of the previously described materials. The metal bump or pillar 27 can be used to be bonded with an external circuit, such as ball-grid-array (BGA) substrate, printed circuit board, semiconductor chip, metal substrate, glass substrate or ceramic substrate.

[00589] For example, the metal bump or pillar 27 can be composed of a single metal layer formed by a suitable process or processes, e.g., by electroplating a copper layer, to a thickness between 10 and 150 micrometers, and preferably between 20 and 100 micrometers, in the opening 31a and on the seed layer 18, preferably the previously described copper layer 18, exposed by the opening 31a using the previously described electroplating solution for electroplating copper of the bulk metal layer 9.

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[00590] Alternatively, the metal bump or pillar 27 can be composed of a single metal layer formed by a suitable process or processes, e.g., by electroplating a gold layer, to a thickness between 5 and 30 micrometers, and preferably between 10 and 25 micrometers, in the opening 31a and on the seed layer 18, preferably the previously described gold layer 18, exposed by the opening 31a using the previously described electroplating solution for electroplating gold of the bulk metal layer 9.

[00591] Alternatively, the metal bump or pillar 27 can be composed of a single metal layer formed by a suitable process or processes, e.g., by electroplating a nickel layer, to a thickness between 5 and 100 micrometers, and preferably between 10 and 50 micrometers, in the opening 31a and on the seed layer 18, preferably the previously described copper layer or nickel layer 18, exposed by the opening 31a using the previously described electroplating solution for electroplating nickel of the bulk metal layer 9.

[00592] Alternatively, the metal bump or pillar 27 can be composed of double metal layers formed by a suitable process or processes, e.g., by electroplating a copper layer, to a thickness between 10 and 150 micrometers, and preferably between 20 and 100 micrometers, in the opening 31a and on the seed layer 18, preferably the previously described copper layer 18, exposed by the opening 31a using the previously described electroplating solution for electroplating copper of the bulk metal layer 9, and then electroplating or electroless plating a gold layer, to a thickness between 0.005 and 10 micrometers, and preferably between 0.05 and 1 micrometers, in the opening 31a and on the electroplated copper layer in the opening 31a using the previously described electroplating or electroless plating solution for electroplating or electroless plating gold of the bulk metal layer 9.

[00593] Alternatively, the metal bump or pillar 27 can be composed of triple metal layers formed by a suitable process or processes, e.g., by electroplating a copper layer, to a thickness between 10 and 150 micrometers, and preferably between 20 and 100 micrometers, in the opening 31a and on the seed layer 18, preferably the previously described copper layer 18, exposed by the opening 31a using the previously described electroplating solution for electroplating copper of the bulk metal layer 9, next electroplating or electroless plating a nickel layer, to a thickness between 1 and 15 micrometers, and preferably between 2 and 10 micrometers, in the opening 31a and on the electroplated copper layer in the opening 31a using the previously described electroplating or electroless plating solution for electroplating or electroless plating nickel of the bulk metal layer 9, and then electroplating or electroless

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plating a gold layer, to a thickness between 0.005 and 1 micrometers, and preferably between 0.05 and 0.1 micrometers, in the opening 31a and on the electroplated or electroless plated nickel layer in the opening 31a using the previously described electroplating or electroless plating solution for electroplating or electroless plating gold of the bulk metal layer 9.

[00594] Alternatively, the metal bump or pillar 27 can be composed of triple metal layers formed by a suitable process or processes, e.g., by electroplating a copper layer, to a thickness between 10 and 150 micrometers, and preferably between 20 and 100 micrometers, in the opening 31a and on the seed layer 18, preferably the previously described copper layer 18, exposed by the opening 31a using the previously described electroplating solution for electroplating copper of the bulk metal layer 9, next electroplating or electroless plating a nickel layer, to a thickness between 1 and 15 micrometers, and preferably between 2 and 10 micrometers, in the opening 31a and on the electroplated copper layer in the opening 31a using the previously described electroplating or electroless plating solution for electroplating or electroless plating nickel of the bulk metal layer 9, and then electroplating or electroless plating a palladium layer, to a thickness between 0.005 and 1 micrometers, and preferably between 0.05 and 0.1 micrometers, in the opening 31a and on the electroplated or electroless plated nickel layer in the opening 31a using the previously described electroplating or electroless plating solution for electroplating or electroless plating palladium of the bulk metal layer 9.

[00595] Alternatively, the metal bump or pillar 27 can be composed of four metal layers formed by a suitable process or processes, e.g., by electroplating a copper layer, to a thickness between 10 and 150 micrometers, and preferably between 20 and 100 micrometers, in the opening 31a and on the seed layer 18, preferably the previously described copper layer 18, exposed by the opening 31a using the previously described electroplating solution for electroplating copper of the bulk metal layer 9, next electroplating or electroless plating a nickel layer, to a thickness between 1 and 15 micrometers, and preferably between 2 and 10 micrometers, in the opening 31a and on the electroplated copper layer in the opening 31a using the previously described electroplating or electroless plating solution for electroplating or electroless plating nickel of the bulk metal layer 9, next electroplating or electroless plating a palladium layer, to a thickness between 0.005 and 1 micrometers, and preferably between 0.05 and 0.1 micrometers, in the opening 31a and on the electroplated or electroless plated nickel layer in the opening 31a using the previously described electroplating or electroless plating solution for electroplating or electroless plating palladium of the bulk metal layer 9, and then

electroplating or electroless plating a gold layer, to a thickness between 0.005 and 1 micrometers, and preferably between 0.05 and 0.1 micrometers, in the opening 31a and on the electroplated or electroless plated palladium layer in the opening 31a using the previously described electroplating or electroless plating solution for electroplating or electroless plating gold of the bulk metal layer 9.

[00596] Alternatively, the metal bump or pillar 27 can be composed of double metal layers formed by a suitable process or processes, e.g., by electroplating a copper layer, to a thickness between 10 and 150 micrometers, and preferably between 20 and 100 micrometers, in the opening 31a and on the seed layer 18, preferably the previously described copper layer 18, exposed by the opening 31a using the previously described electroplating solution for electroplating copper of the bulk metal layer 9, and then electroplating or electroless plating a solder layer, such as a bismuth-containing layer, an indium-containing layer or a tin-containing layer of a tin-lead alloy, a tin-silver alloy or a tin-silver-copper alloy, to a thickness between 5 and 100 micrometers, and preferably between 10 and 50 micrometer, in the opening 31a and on the electroplated copper layer in the opening 31a.

[00597] Alternatively, the metal bump or pillar 27 can be composed of double metal layers formed by a suitable process or processes, e.g., by electroplating a nickel layer, to a thickness between 5 and 150 micrometers, and preferably between 10 and 60 micrometers, in the opening 31a and on the seed layer 18, preferably the previously described copper layer or nickel layer 18, exposed by the opening 31a using the previously described electroplating solution for electroplating nickel of the bulk metal layer 9, and then electroplating or electroless plating a solder layer, such as a bismuth-containing layer, an indium-containing layer or a tin-containing layer of a tin-lead alloy, a tin-silver alloy or a tin-silver-copper alloy, to a thickness between 5 and 100 micrometers, and preferably between 10 and 50 micrometer, in the opening 31a and on the electroplated nickel layer in the opening 31a.

[00598] Alternatively, the metal bump or pillar 27 can be composed of triple metal layers formed by a suitable process or processes, e.g., by electroplating a copper layer, to a thickness between 10 and 150 micrometers, and preferably between 20 and 100 micrometers, in the opening 31a and on the seed layer 18, preferably the previously described copper layer 18, exposed by the opening 31a using the previously described electroplating solution for electroplating copper of the bulk metal layer 9, next electroplating or electroless plating a nickel layer, to a thickness between 1 and 15 micrometers, and preferably between 2 and 10

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micrometers, in the opening 31a and on the electroplated copper layer in the opening 31a using the previously described electroplating or electroless plating solution for electroplating or electroless plating nickel of the bulk metal layer 9, and then electroplating or electroless plating a solder layer, such as a bismuth-containing layer, an indium-containing layer or a tin-containing layer of a tin-lead alloy, a tin-silver alloy or a tin-silver-copper alloy, to a thickness between 5 and 100 micrometers, and preferably between 10 and 50 micrometers, in the opening 31a and on the electroplated or electroless plated nickel layer in the opening 31a.

[00599] Alternatively, the metal bump or pillar 27 can be composed of triple metal layers formed by a suitable process or processes, e.g., by electroplating a copper layer, to a thickness between 1 and 10 micrometers, and preferably between 3 and 8 micrometers, in the opening 31a and on the seed layer 18, preferably the previously described copper layer 18, exposed by the opening 31a using the previously described electroplating solution for electroplating copper of the bulk metal layer 9, next electroplating or electroless plating a nickel layer, to a thickness between 1 and 15 micrometers, and preferably between 2 and 10 micrometers, in the opening 31a and on the electroplated copper layer in the opening 31a using the previously described electroplating or electroless plating solution for electroplating or electroless plating nickel of the bulk metal layer 9, and then electroplating or electroless plating a solder layer, such as a bismuth-containing layer, an indium-containing layer or a tin-containing layer of a tin-lead alloy, a tin-silver alloy or a tin-silver-copper alloy, to a thickness between 30 and 250 micrometers, and preferably between 50 and 150 micrometers, in the opening 31a and on the electroplated or electroless plated nickel layer in the opening 31a.

[00600] Next, referring to Fig. 25K, the photoresist layer 31 is removed using an inorganic solution or using an organic solution with amide. Some residuals from the photoresist layer 31 could remain on the seed layer 18 not under the metal bump or pillar 27. Thereafter, the residuals can be removed from the seed layer 18 with a plasma, such as an O_2 plasma or a plasma containing fluorine of below 200PPM and oxygen. Next, referring to Fig. 25L, the seed layer 18 not under the metal bump or pillar 27 is removed, and then the adhesion/barrier layer 16 not under the metal bump or pillar 27 is removed.

[00601] In a case, the seed layer 18 and the adhesion/barrier layer 16 not under the metal bump or pillar 27 can be subsequently removed by a dry etching method. As to the dry etching method, both the seed layer 18 and the adhesion/barrier layer 16 not under the metal bump or

pillar 27 can be subsequently removed by an Ar sputtering etching process; alternatively, both the seed layer 18 and the adhesion/barrier layer 16 not under the metal bump or pillar 27 can be subsequently removed by a reactive ion etching (RIE) process; alternatively, the seed layer 18 not under the metal bump or pillar 27 can be removed by an Ar sputtering etching process, and the adhesion/barrier layer 16 not under the metal bump or pillar 27 can be removed by a reactive ion etching (RIE) process.

[00602] In another case, the seed layer 18 and the adhesion/barrier layer 16 not under the metal bump or pillar 27 can be subsequently removed by a wet etching method. As to the wet etching method, when the seed layer 18 is a copper layer, it can be etched with a solution containing NH_4OH or with a solution containing H_2SO_4; when the seed layer 18 is a gold layer, it can be etched with an iodine-containing solution, such as a solution containing potassium iodide; when the adhesion/barrier layer 16 is a titanium-tungsten-alloy layer, it can be etched with a solution containing hydrogen peroxide or with a solution containing NH_4OH and hydrogen peroxide; when the adhesion/barrier layer 16 is a titanium layer, it can be etched with a solution containing hydrogen fluoride or with a solution containing NH_4OH and hydrogen peroxide; when the adhesion/barrier layer 16 is a chromium layer, it can be etched with a solution containing potassium ferricyanide.

[00603] In another case, the seed layer 18, such as copper, not under the metal bump or pillar 27 can be removed by a solution containing NH_4OH or a solution containing H_2SO_4, and the adhesion/barrier layer 16 not under the metal bump or pillar 27 can be removed by a reactive ion etching (RIE) process or an Ar sputtering etching process.

[00604] In another case, the seed layer 18, such as gold, not under the metal bump or pillar 27 can be etched with an iodine-containing solution, such as a solution containing potassium iodide, and the adhesion/barrier layer 16 not under the metal bump or pillar 27 can be removed by a reactive ion etching (RIE) process or an Ar sputtering etching process.

[00605] In case the adhesion/barrier layer 16 not under the metal bump or pillar 27 is removed using a wet etching process, an undercut is formed under the metal bump or pillar 27 overhanging the adhesion/barrier layer 16. The adhesion/barrier layer 16 under the metal bump or pillar 27 has a first sidewall recessed from a second sidewall of the metal bump or pillar 27, and a distance d1 between the first sidewall and the second sidewall is between 0.3 and 2 micrometers.

[00606] Accordingly, as shown in Fig. 25L, a bottom scheme 103 at the backside 1a of the thinned silicon substrate 1 is formed with the insulating layer 3, the interconnecting structures 88 provided by the metal layers 4 and 9, the polymer layer 14, the metal layers 16 and 18, and the metal bump or pillar 27, and the opening 14a in the polymer layer 14 is over the interconnecting structure 88. After the step illustrated in Fig. 25L, the semiconductor wafer 10 can be cut into a plurality of individual semiconductor chip by a die-sawing process.

[00607] Alternatively, after the step illustrated in Fig. 25L, with the following steps being illustrated with reverse figures for simple explanation, multiple openings 50 are formed in the passivation layer 5 to expose the metal traces or pads 600, and then each of the over-passivation schemes 102 illustrated in Figs. 15H, 15K-15M, 16L, 16M, 17J, 18I, 19H and 20 can be alternatively formed over the passivation layer 5 at the active side of the thinned silicon substrate 1. Thereafter, the semiconductor wafer 10 can be cut into a plurality of individual semiconductor chip by a die-sawing process.

[00608] Alternatively, a process of forming any one of the over-passivation schemes 102 illustrated in Figs. 15H, 15K-15M, 16L, 16M, 17J, 18I, 19H and 20 over the passivation layer 5 can be performed before the steps illustrated in Figs. 24B, 24C and 25A-25L. After the steps illustrated in Figs. 24B, 24C and 25A-25L, the semiconductor wafer 10 can be cut into a plurality of individual semiconductor chip by a die-sawing process.

[00609] After the die-sawing process, the semiconductor chip cut from the semiconductor wafer 10 can be packaged for a chip package. In the chip package, the semiconductor chip can be connected to an external circuit, such as ball-grid-array (BGA) substrate, printed circuit board, semiconductor chip, metal substrate, glass substrate or ceramic substrate, through the metal bump or pillar 27 of the bottom scheme 103. The semiconductor chip includes the bottom scheme 103, and the bottom scheme 103 includes the insulating layer 3 on the backside 1a of the thinned silicon substrate 1 and in the through-silicon vias 11a, 11b, 11c, 11d and 11e, the interconnecting structures 88 at the backside 1a of the thinned silicon substrate 1, in the through-silicon vias 11a, 11b, 11c, 11d and 11e and on the insulating layer 3, the polymer layer 14 at the backside 1a of the thinned silicon substrate 1, on the interconnecting structures 88 and on the insulating layer 3, the metal bump or pillar 27 at the backside 1a of the thinned silicon substrate 1, on the interconnecting structure 88 and on the polymer layer 14, the adhesion/barrier layer 16 between the bulk metal layer 9 and the metal bump or pillar 27, and the seed layer 18 between the adhesion/barrier layer 16 and the metal

bump or pillar 27. The interconnecting structures 88 connects the off-chip buffer 42 to the internal circuits 21, 22, 23 and 24, connects the off-chip buffer 42 to the metal bump or pillar 27, and connects the internal circuits 21, 22, 23 and 24 to the metal bumps or pillars 27. The off-chip ESD (electro static discharge) circuit 43 is connected to the off-chip buffer 42 through the fine-line metal trace 639, and to the interconnecting structure 88 through the fine-line metal trace 639.

[00610] Fig. 25M is a cross-sectional view showing a semiconductor wafer, which can be formed by a suitable process or processes, e.g., by the following steps. First, the semiconductor wafer 10 illustrated in Fig. 24A includes multiple openings 531, 532, 534, 539 and 539' in the passivation layer 5 to expose multiple regions 600a of the metal traces or pads 600. The openings 531, 532, 534, 539 and 539' are over the regions 600a of the metal traces or pads 600, and the regions 600a of the metal traces or pads 600 are at bottoms of the openings 531, 532, 534, 539 and 539'. Next, a flux 32 can be formed in the openings 531, 532, 534, 539 and 539' and on the regions 600a of the metal traces or pads 600 exposed by the openings 531, 532, 534, 539 and 539'. Next, the step illustrated in Fig. 24B can be performed. Next, the through silicon vias 11a, 11b, 11c, 11d and 11e can be formed in the thinned silicon substrate 1, and the insulating layer 3 can be formed on the backside 1a of the thinned silicon substrate 1 and on the sidewalls of the through silicon vias 11a, 11b, 11c, 11d and 11e, which can be referred to as the steps illustrated in Figs. 24C-24H or Figs. 24I-24N. Next, the structure including the interconnecting structures 88, the polymer layer 14 and the metal bump or pillar 27 can be formed in the through silicon vias 11a, 11b, 11c, 11d and 11e and at the backside 1a of the thinned silicon substrate 1, which can be referred to as the steps illustrated in Figs. 25A-25L. Accordingly, a bottom scheme 103 same as the bottom scheme 103 shown in Fig. 25L can be formed at the backside 1a of the thinned silicon substrate 1.

[00611] After forming the structure shown in Fig. 25M, the flux 32 is removed. Next, with the following steps being illustrated with reverse figures for simple explanation, each of the over-passivation schemes 102 illustrated in Figs. 15H, 15K-15M, 16L, 16M, 17J, 18I, 19H and 20 can be alternatively formed over the passivation layer 5 at the active side of the thinned silicon substrate 1. Thereafter, the semiconductor wafer 10 can be cut into a plurality of individual semiconductor chip by a die-sawing process. After the die-sawing process, the semiconductor chip cut from the semiconductor wafer 10 can be packaged for a chip package. In the chip package, the semiconductor chip can be connected to a first external circuit, such as ball-grid-array (BGA) substrate, printed circuit board, semiconductor chip, metal substrate,

glass substrate or ceramic substrate, through the metal bump or pillar 27 of the bottom scheme 103, and/or to a second external circuit, such as ball-grid-array (BGA) substrate, printed circuit board, semiconductor chip, metal substrate, glass substrate or ceramic substrate, through one of the over-passivation schemes 102 illustrated in Figs. 15H, 15K-15M, 16L, 16M, 17J, 18I, 19H and 20.

[00612] Fig. 25N is a cross-sectional view showing a semiconductor wafer, which can be formed by a suitable process or processes, e.g., by the following steps. First, the semiconductor wafer 10 illustrated in Fig. 24A includes multiple openings 531, 532, 534, 539 and 539' in the passivation layer 5 to expose multiple regions 600a of the metal traces or pads 600. The openings 531, 532, 534, 539 and 539' are over the regions 600a of the metal traces or pads 600, and the regions 600a of the metal traces or pads 600 are at bottoms of the openings 531, 532, 534, 539 and 539'. Next, multiple metal pads, bumps or traces 34a composed of two metal layers 32 and 34 can be formed on the passivation layer 5 and on the regions 600a of the metal traces or pads 600 exposed by the openings 531, 532, 534, 539 and 539'. The metal layer 32 is formed on the passivation layer 5 and on the regions 600a of the metal traces or pads 600 exposed by the openings 531, 532, 534, 539 and 539, and the metal layer 34 is formed on the metal layer 32, and the metal layer 34 is not covered by the metal layer 32.

[00613] The metal pad, bump or trace 34a has a thickness larger than 1 micrometer, such as between 1 and 20 micrometers or between 5 and 60 micrometers, and a width larger than that of the metal trace or pad 600 and larger than 3 micrometers, such as between 5 and 60 micrometers, and the metal trace or pad 600 may have a width smaller than 1 micrometer, such as between 0.05 and 0.95 micrometers. The metal pads, bumps or traces 34a can be used to be connected to a first external circuit, such as ball-grid-array (BGA) substrate, printed circuit board, semiconductor chip, metal substrate, glass substrate or ceramic substrate, by bonding the metal pads, bumps or traces 34a to the first external circuit or by wirebonding gold wires or copper wires to the metal pads, bumps or traces 34a and to the first external circuit.

[00614] For example, the metal pads, bumps or traces 34a can be formed by a suitable process or processes, e.g., by a process including sputtering an adhesion/barrier layer 32, such as titanium layer, titanium-tungsten-alloy layer, titanium-nitride layer, tantalum layer or tantalum-nitride layer, having a thickness smaller than 1 micrometer, such as between 0.005 and 0.8 micrometers, and preferably between 0.05 and 0.5 micrometers, on the passivation layer 5 and on the regions 600a of the metal traces or pads 600 exposed by the openings 531,

532, 534, 539 and 539', next sputtering an aluminum-containing layer 34, such as aluminum layer or aluminum-copper-alloy layer, having a thickness between 0.5 and 10 micrometers, and preferably between 1 and 5 micrometers, on the adhesion/barrier layer 32, next forming a patterned photoresist layer on the aluminum-containing layer 34, next etching the aluminum-containing layer 34 not under the patterned photoresist layer, next etching the adhesion/barrier layer 32 not under the patterned photoresist layer, and then removing the patterned photoresist layer. Accordingly, the metal pads, bumps or traces 34a provided by the adhesion/barrier layer 32 and the aluminum-containing layer 34 can be formed on the passivation layer 5 and on the regions 600a of the metal traces or pads 600 exposed by the openings 531, 532, 534, 539 and 539'. The aluminum-containing layer 34 of the metal pad, bump or trace 34a can be used to be connected to the first external circuit by wirebonding a gold wire or a copper wire to the aluminum-containing layer 34 and to the first external circuit or by bonding aluminum-containing layer 34 with a gold layer or a tin-alloy layer of the first external circuit.

[00615] Alternatively, the metal pads, bumps or traces 34a can be formed by a suitable process or processes, e.g., by a process including sputtering an adhesion/barrier layer 32, such as titanium layer, titanium-tungsten-alloy layer, titanium-nitride layer, tantalum layer or tantalum-nitride layer, having a thickness smaller than 1 micrometer, such as between 0.005 and 0.8 micrometers, and preferably between 0.05 and 0.5 micrometers, on the passivation layer 5 and on the regions 600a of the metal traces or pads 600 exposed by the openings 531, 532, 534, 539 and 539', next sputtering a seed layer of gold (not shown) having a thickness smaller than 1 micrometer, such as between 0.005 and 0.8 micrometers, and preferably between 0.05 and 0.5 micrometers, on the adhesion/barrier layer 32, next forming a patterned photoresist layer on the seed layer of gold, and multiple openings in the patterned photoresist layer expose multiple regions of the seed layer of gold, next electroplating a gold layer 34 having a thickness larger than 1 micrometer, such as between 1 and 25 micrometers, and preferably between 2 and 10 micrometers, on the regions of the seed layer of gold exposed by the openings in the patterned photoresist layer, next removing the photoresist layer, next etching the seed layer of gold not under the gold layer 34, and then etching the adhesion/barrier layer 32 not under the gold layer 34. Accordingly, the metal pads, bumps or traces 34a provided by the adhesion/barrier layer 32, the seed layer of gold and the gold layer 34 can be formed on the passivation layer 5 and on the regions 600a of the metal traces or pads 600 exposed by the openings 531, 532, 534, 539 and 539'. The gold layer 34 of the metal pad,

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bump or trace 34a can be used to be connected to the first external circuit by wirebonding a gold wire or a copper wire to the gold layer 34 and to the first external circuit or by bonding the gold layer 34 with a gold layer or a tin-alloy layer of the first external circuit.

[00616] Alternatively, the metal pads, bumps or traces 34a can be formed by a suitable process or processes, e.g., by a process including electroless plating a nickel layer 32 with a thickness between 1 and 10 micrometers, and preferably between 2 and 8 micrometers, on the passivation layer 5 and on the regions 600a of the metal traces or pads 600 exposed by the openings 531, 532, 534, 539 and 539', and then electroless plating the metal layer 34, such as gold layer or palladium layer, with a thickness between 200 angstroms and 2 micrometers, and preferably between 500 angstroms and 5,000 angstroms, on the nickel layer 32. Accordingly, the metal pads, bumps or traces 34a provided by the nickel layer 32 and the metal layer 34 can be formed on the passivation layer 5 and on the regions 600a of the metal traces or pads 600 exposed by the openings 531, 532, 534, 539 and 539'. The metal layer 34 of the metal pad, bump or trace 34a can be used to be connected to the first external circuit by wirebonding a gold wire or a copper wire to the metal layer 34 and to the first external circuit or by bonding the metal layer 34 with a gold layer or a tin-alloy layer of the first external circuit.

[00617] Alternatively, the metal pads, bumps or traces 34a can be formed by a suitable process or processes, e.g., by a process including sputtering an adhesion/barrier layer 32, such as titanium layer, titanium-tungsten-alloy layer, titanium-nitride layer, chromium layer, tantalum layer or tantalum-nitride layer, having a thickness smaller than 1 micrometer, such as between 0.005 and 0.8 micrometers, and preferably between 0.05 and 0.5 micrometers, on the passivation layer 5 and on the regions 600a of the metal traces or pads 600 exposed by the openings 531, 532, 534, 539 and 539', next sputtering a seed layer of copper (not shown) having a thickness smaller than 1 micrometer, such as between 0.005 and 0.8 micrometers, and preferably between 0.05 and 0.5 micrometers, on the adhesion/barrier layer 32, next forming a patterned photoresist layer on the seed layer of copper, and multiple openings in the patterned photoresist layer expose multiple regions of the seed layer of copper, next electroplating a copper layer 34 having a thickness larger than 1 micrometer, such as between 1 and 100 micrometers, and preferably between 5 and 60 micrometers, on the regions of the seed layer of copper exposed by the openings in the patterned photoresist layer, next removing the photoresist layer, next etching the seed layer of copper not under the copper layer 34, and then etching the adhesion/barrier layer 32 not under the copper layer 34. Accordingly, the metal pads, bumps or traces 34a provided by the adhesion/barrier layer 32, the seed layer of copper

and the copper layer 34 can be formed on the passivation layer 5 and on the regions 600a of the metal traces or pads 600 exposed by the openings 531, 532, 534, 539 and 539'. The copper layer 34 of the metal pad, bump or trace 34a can be used to be connected to the first external circuit by wirebonding a gold wire or a copper wire to the copper layer 34 and to the first external circuit or by bonding the copper layer 34 with a gold layer or a tin-alloy layer of the first external circuit.

[00618] Alternatively, the metal pads, bumps or traces 34a can be formed by a suitable process or processes, e.g., by a process including sputtering an adhesion/barrier layer 32, such as titanium layer, titanium-tungsten-alloy layer, titanium-nitride layer, chromium layer, tantalum layer or tantalum-nitride layer, having a thickness smaller than 1 micrometer, such as between 0.005 and 0.8 micrometers, and preferably between 0.05 and 0.5 micrometers, on the passivation layer 5 and on the regions 600a of the metal traces or pads 600 exposed by the openings 531, 532, 534, 539 and 539', next sputtering a seed layer of copper (not shown) having a thickness smaller than 1 micrometer, such as between 0.005 and 0.8 micrometers, and preferably between 0.05 and 0.5 micrometers, on the adhesion/barrier layer 32, next forming a patterned photoresist layer on the seed layer of copper, and multiple openings in the patterned photoresist layer expose multiple regions of the seed layer of copper, next electroplating a copper layer 34 having a thickness larger than 1 micrometer, such as between 1 and 100 micrometers, and preferably between 5 and 60 micrometers, on the regions of the seed layer of copper exposed by the openings in the patterned photoresist layer, next electroplating or electroless plating a nickel layer (not shown) having a thickness between 0.5 and 8 micrometers, and preferably between 1 and 5 micrometers, on the copper layer 34 in the openings in the patterned photoresist layer, next electroplating or electroless plating a gold layer (not shown) having a thickness between 0.1 and 10 micrometers, and preferably between 0.5 and 5 micrometers, on the electroplated or electroless plated nickel layer in the openings in the patterned photoresist layer, next removing the photoresist layer, next etching the seed layer of copper not under the copper layer 34, and then etching the adhesion/barrier layer 32 not under the copper layer 34. Accordingly, the metal pads, bumps or traces 34a provided by the adhesion/barrier layer 32, the seed layer of copper, the copper layer 34, the electroplated or electroless plated nickel layer and the electroplated or electroless plated gold layer can be formed on the passivation layer 5 and on the regions 600a of the metal traces or pads 600 exposed by the openings 531, 532, 534, 539 and 539'. The electroplated or electroless plated gold layer of the metal pad, bump or trace 34a can be used to be connected to the first external

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circuit by wirebonding a gold wire or a copper wire to the electroplated or electroless plated gold layer and to the first external circuit or by bonding the electroplated or electroless plated gold layer with a gold layer or a tin-alloy layer of the first external circuit.

[00619] Alternatively, the metal pads, bumps or traces 34a can be formed by a suitable process or processes, e.g., by a process including sputtering an adhesion/barrier layer 32, such as titanium layer, titanium-tungsten-alloy layer, titanium-nitride layer, chromium layer, tantalum layer or tantalum-nitride layer, having a thickness smaller than 1 micrometer, such as between 0.005 and 0.8 micrometers, and preferably between 0.05 and 0.5 micrometers, on the passivation layer 5 and on the regions 600a of the metal traces or pads 600 exposed by the openings 531, 532, 534, 539 and 539', next sputtering a seed layer of copper (not shown) having a thickness smaller than 1 micrometer, such as between 0.005 and 0.8 micrometers, and preferably between 0.05 and 0.5 micrometers, on the adhesion/barrier layer 32, next forming a patterned photoresist layer on the seed layer of copper, and multiple openings in the patterned photoresist layer expose multiple regions of the seed layer of copper, next electroplating a copper layer 34 having a thickness larger than 1 micrometer, such as between 1 and 100 micrometers, and preferably between 5 and 60 micrometers, on the regions of the seed layer of copper exposed by the openings in the patterned photoresist layer, next electroplating or electroless plating a nickel layer (not shown) having a thickness between 0.5 and 8 micrometers, and preferably between 1 and 5 micrometers, on the copper layer 34 in the openings in the patterned photoresist layer, next electroplating a tin-containing layer (not shown), such as a tin-lead-alloy layer, a tin-silver-alloy layer or a tin-silver-copper-alloy layer, having a thickness between 1 and 150 micrometers, and preferably between 5 and 60 micrometers, on the electroplated or electroless plated nickel layer in the openings in the patterned photoresist layer, next removing the photoresist layer, next etching the seed layer of copper not under the copper layer 34, and then etching the adhesion/barrier layer 32 not under the copper layer 34. Accordingly, the metal pads, bumps or traces 34a provided by the adhesion/barrier layer 32, the seed layer of copper, the copper layer 34, the electroplated or electroless plated nickel layer and the electroplated tin-containing layer can be formed on the passivation layer 5 and on the regions 600a of the metal traces or pads 600 exposed by the openings 531, 532, 534, 539 and 539'. The electroplated tin-containing layer of the metal pad, bump or trace 34a can be used to be connected to the first external circuit by bonding the electroplated tin-containing layer with a gold layer or a tin-alloy layer of the first external circuit.

[00620] After forming the metal pads, bumps or traces 34a, the step illustrated in Fig. 24B can be performed. Next, the through silicon vias 11a, 11b, 11c, 11d and 11e can be formed in the thinned silicon substrate 1, and the insulating layer 3 can be formed on the backside 1a of the thinned silicon substrate 1 and on the sidewalls of the through silicon vias 11a, 11b, 11c, 11d and 11e, which can be referred to as the steps illustrated in Figs. 24C-24H or Figs. 24I-24N. Next, the interconnecting structures 88 can be formed in the through silicon vias 11a, 11b, 11c, 11d and 11e, on the insulating layer 3 and at the backside 1a of the thinned silicon substrate 1, which can be referred to as the steps illustrated in Figs. 25A-25F. Next, the polymer layer 14, the adhesion/barrier layer 16, the seed layer 18 and the metal bump or pillar 27 can be formed at the backside 1a of the thinned silicon substrate 1, which can be referred to as the steps illustrated in Figs. 25G-25L. Accordingly, a bottom scheme 103 same as the bottom scheme 103 shown in Fig. 25L can be formed at the backside 1a of the thinned silicon substrate 1. Alternatively, the step of forming the metal pads, bumps or traces 34a on the passivation layer 5 and on the regions 600a of the metal traces or pads 600 exposed by the openings 531, 532, 534, 539 and 539' can be performed after forming the metal bump or pillar 27.

[00621] After forming the structure shown in Fig. 25N, the semiconductor wafer 10 can be cut into a plurality of individual semiconductor chip by a die-sawing process. After the die-sawing process, the semiconductor chip cut from the semiconductor wafer 10 can be packaged for a chip package. In the chip package, the semiconductor chip can be connected to the first external circuit through the metal pads, bumps or traces 34a, and to a second external circuit, such as printed circuit board, ball-grid-array (BGA) substrate, semiconductor chip, metal substrate, glass substrate or ceramic substrate, through the metal bump or pillar 27 of the bottom scheme 103.

[00622] Fig. 25O is a cross-sectional view showing a semiconductor wafer, which can be formed by a suitable process or processes, e.g., by the following steps. First, the semiconductor wafer 10 illustrated in Fig. 24A includes multiple openings 531, 532, 534, 539 and 539' in the passivation layer 5 to expose multiple regions 600a of the metal traces or pads 600. The openings 531, 532, 534, 539 and 539' are over the regions 600a of the metal traces or pads 600, and the regions 600a of the metal traces or pads 600 are at bottoms of the openings 531, 532, 534, 539 and 539'. Next, the patterned circuit layer 801 composed of the adhesion/barrier/seed layer 8011 and the metal layer 8012 can be formed on the passivation layer 5 and on the regions 600a of the metal traces or pads 600 exposed by the openings 531,

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532, 534, 539 and 539', which can be referred to as the steps illustrated in Figs. 15D-15H. Next, the polymer layer 98 is formed on the metal layer 8012 of the patterned circuit layer 801 and on the passivation layer 5, and the opening 980 in the polymer layer 98 is over a contact point 801a of the metal layer 8012 of the patterned circuit layer 801 and exposes it, which can be referred to as the process illustrated in Fig. 15I. Accordingly, an over-passivation scheme 102 can be formed with the patterned circuit layer 801 and the polymer layer 98, at the active side of the thinned silicon substrate 1. Next, a flux 32 is formed in the opening 980 and on the contact point 801a of the metal layer 8012 exposed by the opening 980. Next, the step illustrated in Fig. 24B can be performed. Next, the through silicon vias 11a, 11b, 11c, 11d and 11e can be formed in the thinned silicon substrate 1, and the insulating layer 3 can be formed on the backside 1a of the thinned silicon substrate 1 and on the sidewalls of the through silicon vias 11a, 11b, 11c, 11d and 11e, which can be referred to as the steps illustrated in Figs. 24C-24H or Figs. 24I-24N. Next, the interconnecting structures 88 can be formed in the through silicon vias 11a, 11b, 11c, 11d and 11e, on the insulating layer 3 and at the backside 1a of the thinned silicon substrate 1, which can be referred to as the steps illustrated in Figs. 25A-25F. Next, the polymer layer 14, the adhesion/barrier layer 16, the seed layer 18 and the metal bump or pillar 27 can be formed at the backside 1a of the thinned silicon substrate 1, which can be referred to as the steps illustrated in Figs. 25G-25L. Accordingly, a bottom scheme 103 same as the bottom scheme 103 shown in Fig. 25L can be formed at the backside 1a of the thinned silicon substrate 1. Alternatively, the steps of forming the patterned circuit layer 801, the polymer layer 98 and the flux 32 can be performed after the steps illustrated in Figs. 24B, 24C and 25A-25L.

[00623] After forming the structure shown in Fig. 25O, the flux 32 is removed. Thereafter, using a die-sawing process, the semiconductor wafer 10 can be cut into a plurality of individual semiconductor chip. The semiconductor chip cut from the semiconductor wafer 10 can be connected to a first external circuit, such as ball-grid-array (BGA) substrate, printed circuit board, semiconductor chip, metal substrate, glass substrate or ceramic substrate, by wirebonding a gold wire or a copper wire to the contact point 801a of gold, copper or aluminum of the patterned circuit layer 801 of the over-passivation scheme 102 and to the first external circuit or by solder bonding the contact point 801a of the patterned circuit layer 801 of the over-passivation scheme 102 with a gold layer or a tin-alloy layer of the first external circuit, and to a second external circuit, such as printed circuit board, ball-grid-array (BGA)

substrate, semiconductor chip, metal substrate, glass substrate or ceramic substrate, through the metal bump or pillar 27 of the bottom scheme 103.

[00624] Fig. 25P is a cross-sectional view showing a semiconductor wafer, which can be formed by a suitable process or processes, e.g., by the following steps. After the steps illustrated in Figs. 24B, 24C and 25A-25F are performed, the polymer layer 14 is formed on the bulk metal layer 9 and on the insulating layer 3, and multiple openings 14a in the polymer layer 14 are over multiple regions of the bulk metal layer 9 and expose them, which can be referred to as the step illustrated in Fig. 25G. Next, the adhesion/barrier layer 16 is formed on the polymer layer 14 and on the regions of the bulk metal layer 9 exposed by the openings 14a, and then the seed layer 18 is formed on the adhesion/barrier layer 16, which can be referred to as the step illustrated in Fig. 25H. Next, the photoresist layer 31 is formed on the seed layer 18, and multiple openings 31a in the photoresist layer 31 expose the seed layer 18, which can be referred to as the step illustrated in Fig. 25I. Next, multiple metal bumps or pillars 27 are formed in the openings 31a and on the seed layer 18 exposed by the openings 31a, which can be referred to as the step illustrated in Fig. 25J. Next, the photoresist layer 31 is removed, which can be referred to as the step illustrated in Fig. 25K. Next, the seed layer 18 not under the metal bumps or pillars 27 is removed, and then the adhesion/barrier layer 16 not under the metal bumps or pillars 27 is removed, which can be referred to as the step illustrated in Fig. 25L. Accordingly, the interconnecting structures 88 provided by the metal layers 4 and 9 can be formed in the through-silicon vias 11a, 11b, 11c, 11d and 11e and at the backside 1a of the thinned silicon substrate 1, and the metal bumps or pillars 27 can be formed over the interconnecting structures 88 and at the backside 1a of the thinned silicon substrate 1. The interconnecting structures 88 can connect the off-chip buffer 42 to the internal circuits 21, 22, 23 and 24, and can connect the metal bumps or pillars 27 to the off-chip buffer 42 and to the internal circuits 21, 22, 23 and 24. A bottom scheme 103, shown in Fig. 25P, at the backside 1a of the thinned silicon substrate 1 is formed with the insulating layer 3, the interconnecting structures 88 provided by the metal layers 4 and 9, the polymer layer 14, the metal layers 16 and 18, and the metal bumps or pillars 27, and the openings 14a in the polymer layer 14 are over the interconnecting structures 88. After forming the structure shown in Fig. 25P, the semiconductor wafer 10 can be cut into a plurality of individual semiconductor chip by a die-sawing process.

[00625] Alternatively, after forming the structure shown in Fig. 25P, with the following steps being illustrated with reverse figures for simple explanation, multiple openings

50 are formed in the passivation layer 5 to expose the metal traces or pads 600, and then each of the over-passivation schemes 102 illustrated in Figs. 15H, 15K-15M, 16L, 16M, 17J, 18I, 19H and 20 can be alternatively formed over the passivation layer 5 at the active side of the thinned silicon substrate 1. Thereafter, the semiconductor wafer 10 can be cut into a plurality of individual semiconductor chip by a die-sawing process.

[00626] Alternatively, a process of forming any one of the over-passivation schemes 102 illustrated in Figs. 15H, 15K-15M, 16L, 16M, 17J, 18I, 19H and 20 over the passivation layer 5 can be performed before the steps illustrated in Figs. 24B, 24C and 25A-25L. After the steps illustrated in Figs. 24B, 24C and 25A-25L, the steps illustrated in Fig. 25P is performed. Thereafter, the semiconductor wafer 10 can be cut into a plurality of individual semiconductor chip by a die-sawing process.

[00627] After the die-sawing process, the semiconductor chip cut from the semiconductor wafer 10 can be packaged for a chip package. In the chip package, the semiconductor chip can be connected to an external circuit, such as ball-grid-array (BGA) substrate, printed circuit board, semiconductor chip, metal substrate, glass substrate or ceramic substrate, through the metal bumps or pillars 27 of the bottom scheme 103, and the metal bumps or pillars 27 of the bottom scheme 103 of the semiconductor chip can be connected to the internal circuits 21, 22, 23 and 24 and the off-chip buffer 42 through the interconnecting structures 88 of the bottom scheme 103.

[00628] Fig. 25Q is a cross-sectional view showing a semiconductor wafer, which can be formed by a suitable process or processes, e.g., by the following steps. First, the semiconductor wafer 10 illustrated in Fig. 24A includes multiple openings 531, 532, 534, 539 and 539' in the passivation layer 5 to expose multiple regions 600a of the metal traces or pads 600. The openings 531, 532, 534, 539 and 539' are over the regions 600a of the metal traces or pads 600, and the regions 600a of the metal traces or pads 600 are at bottoms of the openings 531, 532, 534, 539 and 539'. Next, a flux 32 can be formed in the openings 531, 532, 534, 539 and 539' and on the regions 600a of the metal traces or pads 600 exposed by the openings 531, 532, 534, 539 and 539'. Next, the step illustrated in Fig. 24B can be performed. Next, the through silicon vias 11a, 11b, 11c, 11d and 11e can be formed in the thinned silicon substrate 1, and the insulating layer 3 can be formed on the backside 1a of the thinned silicon substrate 1 and on the sidewalls of the through silicon vias 11a, 11b, 11c, 11d and 11e, which can be referred to as the steps illustrated in Figs. 24C-24H or Figs. 24I-24N. Next, the interconnecting

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structures 88 can be formed in the through silicon vias 11a, 11b, 11c, 11d and 11e and at the backside 1a of the thinned silicon substrate 1, which can be referred to as the steps illustrated in Figs. 25A-25F. Next, the structure including the polymer layer 14 and the metal bumps or pillars 27 can be formed at the backside 1a of the thinned silicon substrate 1, which can be referred to as the steps illustrated in Fig. 25P. Accordingly, a bottom scheme 103 same as the bottom scheme 103 shown in Fig. 25P can be formed at the backside 1a of the thinned silicon substrate 1.

[00629] After forming the structure shown in Fig. 25Q, the flux 32 is removed. Next, with the following steps being illustrated with reverse figures for simple explanation, each of the over-passivation schemes 102 illustrated in Figs. 15H, 15K-15M, 16L, 16M, 17J, 18I, 19H and 20 can be alternatively formed over the passivation layer 5 at the active side of the thinned silicon substrate 1. Thereafter, the semiconductor wafer 10 can be cut into a plurality of individual semiconductor chip by a die-sawing process. After the die-sawing process, the semiconductor chip cut from the semiconductor wafer 10 can be packaged for a chip package. In the chip package, the semiconductor chip can be connected to a first external circuit, such as ball-grid-array (BGA) substrate, printed circuit board, semiconductor chip, metal substrate, glass substrate or ceramic substrate, through the metal bumps or pillars 27 of the bottom scheme 103, and/or to a second external circuit, such as ball-grid-array (BGA) substrate, printed circuit board, semiconductor chip, metal substrate, glass substrate or ceramic substrate, through one of the over-passivation schemes 102 illustrated in Figs. 15H, 15K-15M, 16L, 16M, 17J, 18I, 19H and 20. The interconnecting structures 88 connect the off-chip buffer 42 to the internal circuits 21, 22, 23 and 24, and connect the metal bumps or pillars 27 to the off-chip buffer 42, to the off-chip ESD circuit 43 and to the internal circuits 21, 22, 23 and 24.

[00630] Fig. 25R is a cross-sectional view showing a semiconductor wafer, which can be formed by a suitable process or processes, e.g., by the following steps. First, the semiconductor wafer 10 illustrated in Fig. 24A includes multiple openings 531, 532, 534, 539 and 539' in the passivation layer 5 to expose multiple regions 600a of the metal traces or pads 600. The openings 531, 532, 534, 539 and 539' are over the regions 600a of the metal traces or pads 600, and the regions 600a of the metal traces or pads 600 are at bottoms of the openings 531, 532, 534, 539 and 539'. Next, the metal pads, bumps or traces 34a can be formed on the passivation layer 5 and on the regions 600a of the metal traces or pads 600 exposed by the openings 531, 532, 534, 539 and 539', which can be referred to as the process illustrated in Fig. 25N. The specification of the metal pads, bumps or traces 34a shown in Fig. 25R can be

referred to as the specification of the metal pads, bumps or traces 34a as illustrated in Fig. 25N. After forming the metal pads, bumps or traces 34a, the step illustrated in Fig. 24B can be performed. Next, the through silicon vias 11a, 11b, 11c, 11d and 11e can be formed in the thinned silicon substrate 1, and the insulating layer 3 can be formed on the backside 1a of the thinned silicon substrate 1 and on the sidewalls of the through silicon vias 11a, 11b, 11c, 11d and 11e, which can be referred to as the steps illustrated in Figs. 24C-24H or Figs. 24I-24N. Next, the interconnecting structures 88 can be formed in the through silicon vias 11a, 11b, 11c, 11d and 11e and at the backside 1a of the thinned silicon substrate 1, which can be referred to as the steps illustrated in Figs. 25A-25F. Next, the structure including the polymer layer 14 and the metal bumps or pillars 27 can be formed at the backside 1a of the thinned silicon substrate 1, which can be referred to as the steps illustrated in Fig. 25P. Accordingly, a bottom scheme 103 same as the bottom scheme 103 shown in Fig. 25P can be formed at the backside 1a of the thinned silicon substrate 1. Alternatively, the step of forming the metal pads, bumps or traces 34a on the passivation layer 5 and on the regions 600a of the metal traces or pads 600 exposed by the openings 531, 532, 534, 539 and 539' can be performed after forming the metal bumps or pillars 27.

[00631] After forming the structure shown in Fig. 25R, the semiconductor wafer 10 can be cut into a plurality of individual semiconductor chip by a die-sawing process. After the die-sawing process, the semiconductor chip cut from the semiconductor wafer 10 can be packaged for a chip package. In the chip package, the semiconductor chip can be connected to a first external circuit, such as printed circuit board, semiconductor chip, ball-grid-array (BGA) substrate, metal substrate, glass substrate or ceramic substrate, through the metal pads, bumps or traces 34a, and to a second external circuit, such as printed circuit board, ball-grid-array (BGA) substrate, semiconductor chip, metal substrate, glass substrate or ceramic substrate, through the metal bumps or pillars 27 of the bottom scheme 103. The interconnecting structures 88 connect the off-chip buffer 42 to the internal circuits 21, 22, 23 and 24, and connect the metal bumps or pillars 27 to the off-chip buffer 42, to the off-chip ESD circuit 43 and to the internal circuits 21, 22, 23 and 24.

[00632] Fig. 25S is a cross-sectional view showing a semiconductor wafer, which can be formed by a suitable process or processes, e.g., by the following steps. First, the semiconductor wafer 10 illustrated in Fig. 24A includes multiple openings 531, 532, 534, 539 and 539' in the passivation layer 5 to expose multiple regions 600a of the metal traces or pads 600. The openings 531, 532, 534, 539 and 539' are over the regions 600a of the metal traces or pads 600,

and the regions 600a of the metal traces or pads 600 are at bottoms of the openings 531, 532, 534, 539 and 539'. Next, a patterned circuit layer 801 composed of an adhesion/barrier/seed layer 8011 and a metal layer 8012 can be formed on the passivation layer 5 and on the regions 600a of the metal traces or pads 600 exposed by the openings 531, 532, 534, 539 and 539', which can be referred to as the steps illustrated in Figs. 15D-15H. Next, a polymer layer 98 is formed on the metal layer 8012 of the patterned circuit layer 801 and on the passivation layer 5, and an opening 980 in the polymer layer 98 is over a contact point 801a of the metal layer 8012 of the patterned circuit layer 801 and exposes it, which can be referred to as the process illustrated in Fig. 15I. Accordingly, an over-passivation scheme 102 can be formed with the patterned circuit layer 801 and the polymer layer 98, at the active side of the thinned silicon substrate 1. Next, a flux 32 is formed in the opening 980 and on the contact point 801a of the metal layer 8012 exposed by the opening 980. Next, the step illustrated in Fig. 24B can be performed. Next, the through silicon vias 11a, 11b, 11c, 11d and 11e can be formed in the thinned silicon substrate 1, and the insulating layer 3 can be formed on the backside 1a of the thinned silicon substrate 1 and on the sidewalls of the through silicon vias 11a, 11b, 11c, 11d and 11e, which can be referred to as the steps illustrated in Figs. 24C-24H or Figs. 24I-24N. Next, the interconnecting structures 88 can be formed in the through silicon vias 11a, 11b, 11c, 11d and 11e and at the backside 1a of the thinned silicon substrate 1, which can be referred to as the steps illustrated in Figs. 25A-25F. Next, the structure including the polymer layer 14 and the metal bumps or pillars 27 can be formed at the backside 1a of the thinned silicon substrate 1, which can be referred to as the steps illustrated in Fig. 25P. Accordingly, a bottom scheme 103 same as the bottom scheme 103 shown in Fig. 25P can be formed at the backside 1a of the thinned silicon substrate 1. Alternatively, the steps of forming the patterned circuit layer 801 and the polymer layer 98 can be performed after forming the metal bumps or pillars 27.

[00633] After forming the structure shown in Fig. 25S, the flux 32 can be removed. Thereafter, the semiconductor wafer 10 can be cut into a plurality of individual semiconductor chip by a die-sawing process. After the die-sawing process, the semiconductor chip cut from the semiconductor wafer 10 can be packaged for a chip package. In the chip package, the semiconductor chip can be connected to a first external circuit, such as printed circuit board, semiconductor chip, ball-grid-array (BGA) substrate, metal substrate, glass substrate or ceramic substrate, by wirebonding a gold wire or a copper wire to the contact point 801a of gold, copper or aluminum of the patterned circuit layer 801 of the over-passivation scheme 102 and to the first external circuit or by solder bonding the contact point 801a of the patterned

circuit layer 801 of the over-passivation scheme 102 with a gold layer or a tin-alloy layer of the first external circuit, and can be connected to a second external circuit, such as printed circuit board, ball-grid-array (BGA) substrate, semiconductor chip, metal substrate, glass substrate or ceramic substrate, through the metal bumps or pillars 27 of the bottom scheme 103. The interconnecting structures 88 connect the off-chip buffer 42 to the internal circuits 21, 22, 23 and 24, and connect the metal bumps or pillars 27 to the off-chip buffer 42, to the off-chip ESD circuit 43 and to the internal circuits 21, 22, 23 and 24.

[00634] Fig. 25T is a cross-sectional view showing a semiconductor wafer, which can be formed by a suitable process or processes, e.g., by the following steps. First, the semiconductor wafer 10 illustrated in Fig. 24A includes multiple openings 531, 532, 534, 539 and 539' in the passivation layer 5 to expose multiple regions 600a of the metal traces or pads 600. The openings 531, 532, 534, 539 and 539' are over the regions 600a of the metal traces or pads 600, and the regions 600a of the metal traces or pads 600 are at bottoms of the openings 531, 532, 534, 539 and 539'. Next, a patterned circuit layer 801 composed of an adhesion/barrier/seed layer 8011 and a metal layer 8012 can be formed on the passivation layer 5 and on the regions 600a of the metal traces or pads 600 exposed by the openings 531, 532, 534, 539 and 539', which can be referred to as the steps illustrated in Figs. 15D-15H. Next, a polymer layer 98 is formed on the metal layer 8012 of the patterned circuit layer 801 and on the passivation layer 5, and multiple openings 980 in the polymer layer 98 are over multiple contact points 801a of the metal layer 8012 of the patterned circuit layer 801 and expose them, which can be referred to as the process illustrated in Fig. 15M. Next, multiple metal bumps 89 provided by the metal layers 89a, 89b and 89c can be formed on the polymer layer 98 and on the contact points 801a of the metal layer 8012 exposed by the openings 980, which can be referred to as the process illustrated in Fig. 15M. Accordingly, an over-passivation scheme 102 can be formed with the patterned circuit layer 801, the polymer layer 98 and the metal bumps 89, at the active side of the thinned silicon substrate 1. After forming the metal bumps 89, the step illustrated in Fig. 24B can be performed. Next, the through silicon vias 11a, 11b, 11c, 11d and 11e can be formed in the thinned silicon substrate 1, and the insulating layer 3 can be formed on the backside 1a of the thinned silicon substrate 1 and on the sidewalls of the through silicon vias 11a, 11b, 11c, 11d and 11e, which can be referred to as the steps illustrated in Figs. 24C-24H or Figs. 24I-24N. Next, the interconnecting structures 88 can be formed in the through silicon vias 11a, 11b, 11c, 11d and 11e and at the backside 1a of the thinned silicon substrate 1, which can be referred to as the steps illustrated in Figs. 25A-25F. Next, the structure including the polymer

layer 14 and the metal bumps or pillars 27 can be formed at the backside 1a of the thinned silicon substrate 1, which can be referred to as the steps illustrated in Fig. 25P. Accordingly, a bottom scheme 103 same as the bottom scheme 103 shown in Fig. 25P can be formed at the backside 1a of the thinned silicon substrate 1. Alternatively, the steps of forming the patterned circuit layer 801, the polymer layer 98, the metal layer 89a and the metal bumps 89 can be performed after forming the metal bumps or pillars 27.

[00635] After forming the structure shown in Fig. 25T, the semiconductor wafer 10 can be cut into a plurality of individual semiconductor chip by a die-sawing process. After the die-sawing process, the semiconductor chip cut from the semiconductor wafer 10 can be packaged for a chip package. In the chip package, the semiconductor chip can be connected to a first external circuit, such as printed circuit board, ball-grid-array (BGA) substrate, semiconductor chip, metal substrate, glass substrate or ceramic substrate, through the metal bumps 89 of the over-passivation scheme 102, and to a second external circuit, such as printed circuit board, ball-grid-array (BGA) substrate, semiconductor chip, metal substrate, glass substrate or ceramic substrate, through the metal bumps or pillars 27 of the bottom scheme 103. The interconnecting structures 88 connect the off-chip buffer 42 to the internal circuits 21, 22, 23 and 24, and connect the metal bumps or pillars 27 to the off-chip buffer 42, to the off-chip ESD circuit 43 and to the internal circuits 21, 22, 23 and 24. The patterned circuit layer 801 connects the off-chip buffer 42 to the internal circuits 21, 22, 23 and 24, and connects the metal bumps 89 to the off-chip buffer 42, to the off-chip ESD circuit 43 and to the internal circuits 21, 22, 23 and 24.

[00636] Fig. 25U is a cross-sectional view showing a package, which can be formed by a suitable process or processes, e.g., by the following steps. First, the semiconductor wafer 10 illustrated in Fig. 24A includes multiple openings 531, 532, 534, 539 and 539' in the passivation layer 5 to expose multiple regions 600a of the metal traces or pads 600. The openings 531, 532, 534, 539 and 539' are over the regions 600a of the metal traces or pads 600, and the regions 600a of the metal traces or pads 600 are at bottoms of the openings 531, 532, 534, 539 and 539'. Next, a patterned circuit layer 801 composed of an adhesion/barrier/seed layer 8011 and a metal layer 8012 can be formed on the passivation layer 5 and on the regions 600a of the metal traces or pads 600 exposed by the openings 531, 532, 534, 539 and 539', which can be referred to as the steps illustrated in Figs. 15D-15H. Next, a polymer layer 98 is formed on the metal layer 8012 of the patterned circuit layer 801 and on the passivation layer 5, and multiple openings 980 in the polymer layer 98 are over multiple contact points 801a of the

metal layer 8012 of the patterned circuit layer 801 and expose them, which can be referred to as the process illustrated in Fig. 15I. Accordingly, an over-passivation scheme 102 can be formed with the patterned circuit layer 801 and the polymer layer 98, at the active side of the thinned silicon substrate 1. Next, a flux can be formed in the openings 980 and on the contact points 801a of the metal layer 8012 exposed by the openings 980.

[00637] After forming the flux, the step illustrated in Fig. 24B can be performed. Next, the through silicon vias 11a, 11b, 11c, 11d and 11e can be formed in the thinned silicon substrate 1, and the insulating layer 3 can be formed on the backside 1a of the thinned silicon substrate 1 and on the sidewalls of the through silicon vias 11a, 11b, 11c, 11d and 11e, which can be referred to as the steps illustrated in Figs. 24C-24H or Figs. 24I-24N. Next, the interconnecting structures 88 can be formed in the through silicon vias 11a, 11b, 11c, 11d and 11e and at the backside 1a of the thinned silicon substrate 1, which can be referred to as the steps illustrated in Figs. 25A-25F. Next, the polymer layer 14 can be formed on the bulk metal layer 9 of the interconnecting structures 88 and on the insulating layer 3, and multiple openings 14a in the polymer layer 14 are over multiple regions of the bulk metal layer 9 and expose them, which can be referred to as the step illustrated in Fig. 25G. Accordingly, a bottom scheme 103 at the backside 1a of the thinned silicon substrate 1 can be formed with the insulating layer 3, the interconnecting structures 88 provided by the metal layers 4 and 9, and the polymer layer 14, and the openings 14a in the polymer layer 14 are over the interconnecting structures 88. Next, the flux is removed to expose the contact points 801a of the metal layer 8012 exposed by the openings 980.

[00638] Alternatively, the step illustrated in Fig. 24B can be performed before the steps of forming the patterned circuit layer 801 and the polymer layer 98. Next, the through silicon vias 11a, 11b, 11c, 11d and 11e can be formed in the thinned silicon substrate 1, and the insulating layer 3 can be formed on the backside 1a of the thinned silicon substrate 1 and on the sidewalls of the through silicon vias 11a, 11b, 11c, 11d and 11e, which can be referred to as the steps illustrated in Figs. 24C-24H or Figs. 24I-24N. Next, the structure including the interconnecting structures 88, the polymer layer 14 and the openings 14a in the polymer layer 14 can be formed at the backside 1a of the thinned silicon substrate 1, which can be referred to as the steps illustrated in Figs. 25A-25G. Next, the flux can be formed in the openings 14a and on the regions of the bulk metal layer 9 exposed by the openings 14a. Next, the patterned circuit layer 801, the polymer layer 98 and the openings 980 in the polymer layer 98 can be formed at the active side of the thinned silicon substrate 1, which can be referred to as the steps

illustrated in Figs. 15D-15I. Next, the flux is removed to expose the contact points 801a of the metal layer 8012 exposed by the openings 980.

[00639] After removing the flux, the semiconductor wafer 10 can be cut into a plurality of individual semiconductor chip by a die-sawing process. Thereafter, using a wire-bonding process, multiple wirebonded wires 129, such as wirebonded gold wires or wirebonded copper wires, can be bonded onto the schemes 102 and 103 of the semiconductor chip cut from the semiconductor wafer 10. For example, the wirebonded wires 129 can be wirebonded gold wires ball bonded with the regions of gold, copper, aluminum or palladium of the bulk metal layer 9 exposed by the openings 14a and with the regions 801a of gold, copper, aluminum or palladium of the metal layer 8012 exposed by the openings 980. Alternatively, the wirebonded wires 129 can be wirebonded copper wires ball bonded with the regions of gold, copper, aluminum or palladium of the bulk metal layer 9 exposed by the openings 14a and with the regions 801a of gold, copper, aluminum or palladium of the metal layer 8012 exposed by the openings 980.

[00640] Fig. 25V is a cross-sectional view showing a package, which can be formed by a suitable process or processes, e.g., by the following steps. First, the semiconductor wafer 10 illustrated in Fig. 24A includes multiple openings 531, 532, 534, 539 and 539' in the passivation layer 5 to expose multiple regions 600a of the metal traces or pads 600. The openings 531, 532, 534, 539 and 539' are over the regions 600a of the metal traces or pads 600, and the regions 600a of the metal traces or pads 600 are at bottoms of the openings 531, 532, 534, 539 and 539'. Next, the patterned circuit layer 801 composed of the adhesion/barrier/seed layer 8011 and the metal layer 8012 can be formed on the passivation layer 5 and on the regions 600a of the metal traces or pads 600 exposed by the openings 531, 532, 534, 539 and 539', which can be referred to as the steps illustrated in Figs. 15D-15H. Next, the polymer layer 98 is formed on the metal layer 8012 of the patterned circuit layer 801 and on the passivation layer 5, and multiple openings 980 in the polymer layer 98 are over multiple contact points 801a of the metal layer 8012 of the patterned circuit layer 801 and expose them, which can be referred to as the process illustrated in Fig. 15I. Accordingly, an over-passivation scheme 102 can be formed with the patterned circuit layer 801 and the polymer layer 98, at the active side of the thinned silicon substrate 1. Next, a flux can be formed in the openings 980 and on the contact points 801a of the metal layer 8012 exposed by the openings 980.

[00641] After forming the flux, the step illustrated in Fig. 24B can be performed. Next, the through silicon vias 11a, 11b, 11c, 11d and 11e can be formed in the thinned silicon substrate 1, and the insulating layer 3 can be formed on the backside 1a of the thinned silicon substrate 1 and on the sidewalls of the through silicon vias 11a, 11b, 11c, 11d and 11e, which can be referred to as the steps illustrated in Figs. 24C-24H or Figs. 24I-24N. Next, the interconnecting structures 88 can be formed in the through silicon vias 11a, 11b, 11c, 11d and 11e and at the backside 1a of the thinned silicon substrate 1, which can be referred to as the steps illustrated in Figs. 25A-25F. Next, the structure including the polymer layer 14 and the metal bumps or pillars 27 can be formed at the backside 1a of the thinned silicon substrate 1, which can be referred to as the steps illustrated in Fig. 25P. Accordingly, a bottom scheme 103 same as the bottom scheme 103 shown in Fig. 25P can be formed at the backside 1a of the thinned silicon substrate 1. Next, the flux is removed to expose the contact points 801a of the metal layer 8012 exposed by the openings 980.

[00642] After removing the flux, the semiconductor wafer 10 can be cut into a plurality of individual semiconductor chip by a die-sawing process. After the die-sawing process, the semiconductor chip cut from the semiconductor wafer 10 can be packaged for a chip package. In the chip package, the semiconductor chip can be connected to a first external circuit, such as printed circuit board, ball-grid-array (BGA) substrate, semiconductor chip, metal substrate, glass substrate or ceramic substrate, by wirebonding multiple wires 129, such as gold wires or copper wires, to the regions 801a of the metal layer 8012 of the over-passivation scheme 102 and to the first external circuit, and can be connected to a second external circuit, such as printed circuit board, ball-grid-array (BGA) substrate, semiconductor chip, metal substrate, glass substrate or ceramic substrate, by bonding the metal bumps or pillars 27 of the bottom scheme 103 with the second external circuit.

[00643] For example, using a wire-bonding process, the wirebonded wires 129 can be wirebonded gold wires ball bonded with the regions 801a of gold, copper, aluminum or palladium of the metal layer 8012 exposed by the openings 980. Alternatively, using a wire-bonding process, the wirebonded wires 129 can be wirebonded copper wires ball bonded with the regions 801a of gold, copper, aluminum or palladium of the metal layer 8012 exposed by the openings 980.

[00644] Alternatively, the step illustrated in Fig. 24B can be performed before the steps of forming the patterned circuit layer 801 and the polymer layer 98. Next, the through silicon

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vias 11a, 11b, 11c, 11d and 11e can be formed in the thinned silicon substrate 1, and the insulating layer 3 can be formed on the backside 1a of the thinned silicon substrate 1 and on the sidewalls of the through silicon vias 11a, 11b, 11c, 11d and 11e, which can be referred to as the steps illustrated in Figs. 24C-24H or Figs. 24I-24N. Next, the interconnecting structures 88 can be formed in the through silicon vias 11a, 11b, 11c, 11d and 11e and at the backside 1a of the thinned silicon substrate 1, which can be referred to as the steps illustrated in Figs. 25A-25F. Next, the structure including the polymer layer 14, the openings 14a and the metal bumps or pillars 27 can be formed at the backside 1a of the thinned silicon substrate 1, which can be referred to as the steps illustrated in Fig. 25P. Next, the patterned circuit layer 801, the polymer layer 98 and the openings 980 in the polymer layer 98 can be formed at the active side of the thinned silicon substrate 1, which can be referred to as the steps illustrated in Figs. 15D-15I. Next, the semiconductor wafer 10 can be cut into a plurality of individual semiconductor chip by a die-sawing process. Thereafter, using a wire-bonding process, the wirebonded wires 129, such as wirebonded gold wires or wirebonded copper wires, can be bonded onto the regions 801a of the metal layer 8012 exposed by the openings 980 of the semiconductor chip.

[00645] Fig. 25W is a cross-sectional view showing a package, which can be formed by a suitable process or processes, e.g., by the following steps. First, the semiconductor wafer 10 illustrated in Fig. 24A includes multiple openings 531, 532, 534, 539 and 539' in the passivation layer 5 to expose multiple regions 600a of the metal traces or pads 600. The openings 531, 532, 534, 539 and 539' are over the regions 600a of the metal traces or pads 600, and the regions 600a of the metal traces or pads 600 are at bottoms of the openings 531, 532, 534, 539 and 539'. Next, the patterned circuit layer 801 composed of the adhesion/barrier/seed layer 8011 and the metal layer 8012 can be formed on the passivation layer 5 and on the regions 600a of the metal traces or pads 600 exposed by the openings 531, 532, 534, 539 and 539', which can be referred to as the steps illustrated in Figs. 15D-15H. Next, the polymer layer 98 is formed on the metal layer 8012 of the patterned circuit layer 801 and on the passivation layer 5, and multiple openings 980 in the polymer layer 98 are over multiple contact points 801a of the metal layer 8012 of the patterned circuit layer 801 and expose them, which can be referred to as the process illustrated in Fig. 15M. Next, multiple metal bumps 89 provided by the metal layers 89a, 89b and 89c can be formed on the polymer layer 98 and on the contact points 801a of the metal layer 8012 exposed by the openings 980, which can be referred to as the step illustrated in Fig. 15M. Accordingly, an over-passivation scheme 102 can

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be formed with the patterned circuit layer 801, the polymer layer 98 and the metal bumps 89, at the active side of the thinned silicon substrate 1.

[00646] After forming the metal bumps 89, the step illustrated in Fig. 24B can be performed. Next, the through silicon vias 11a, 11b, 11c, 11d and 11e can be formed in the thinned silicon substrate 1, and the insulating layer 3 can be formed on the backside 1a of the thinned silicon substrate 1 and on the sidewalls of the through silicon vias 11a, 11b, 11c, 11d and 11e, which can be referred to as the steps illustrated in Figs. 24C-24H or Figs. 24I-24N. Next, the interconnecting structures 88 can be formed in the through silicon vias 11a, 11b, 11c, 11d and 11e and at the backside 1a of the thinned silicon substrate 1, which can be referred to as the steps illustrated in Figs. 25A-25F. Next, the polymer layer 14 can be formed on the bulk metal layer 9 of the interconnecting structures 88 and on the insulating layer 3, and multiple openings 14a in the polymer layer 14 are over multiple regions of the bulk metal layer 9 and expose them, which can be referred to as the step illustrated in Fig. 25G. Accordingly, a bottom scheme 103 at the backside 1a of the thinned silicon substrate 1 is formed with the insulating layer 3, the interconnecting structures 88 provided by the metal layers 4 and 9, and the polymer layer 14, and the openings 14a in the polymer layer 14 are over the interconnecting structures 88. After forming the bottom scheme 103, the semiconductor wafer 10 can be cut into a plurality of individual semiconductor chip by a die-sawing process.

[00647] After the die-sawing process, the semiconductor chip cut from the semiconductor wafer 10 can be packaged for a chip package. In the chip package, the semiconductor chip can be connected to a first external circuit, such as printed circuit board, ball-grid-array (BGA) substrate, semiconductor chip, metal substrate, glass substrate or ceramic substrate, by bonding the metal bumps 89 of the over-passivation scheme 102 with the first external circuit, and can be connected to a second external circuit, such as printed circuit board, ball-grid-array (BGA) substrate, semiconductor chip, metal substrate, glass substrate or ceramic substrate, by wirebonding multiple wires 129, such as gold wires or copper wires, to the bulk metal layer 9 of the bottom scheme 103 and to the second external circuit.

[00648] For example, using a wire-bonding process, the wirebonded wires 129 can be wirebonded gold wires ball bonded with the regions of gold, copper, aluminum or palladium of the bulk metal layer 9 exposed by the openings 14a. Alternatively, using a wire-bonding process, the wirebonded wires 129 can be wirebonded copper wires ball bonded with the

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regions of gold, copper, aluminum or palladium of the bulk metal layer 9 exposed by the openings 14a.

[00649] Alternatively, the step illustrated in Fig. 24B can be performed before the steps of forming the patterned circuit layer 801, the polymer layer 98 and the metal bumps 89. Next, the through silicon vias 11a, 11b, 11c, 11d and 11e can be formed in the thinned silicon substrate 1, and the insulating layer 3 can be formed on the backside 1a of the thinned silicon substrate 1 and on the sidewalls of the through silicon vias 11a, 11b, 11c, 11d and 11e, which can be referred to as the steps illustrated in Figs. 24C-24H or Figs. 24I-24N. Next, the interconnecting structures 88 can be formed in the through silicon vias 11a, 11b, 11c, 11d and 11e and at the backside 1a of the thinned silicon substrate 1, which can be referred to as the steps illustrated in Figs. 25A-25F. Next, the polymer layer 14 and the openings 14a in the polymer layer 14 can be formed at the backside 1a of the thinned silicon substrate 1, which can be referred to as the step illustrated in Fig. 25G. Next, a flux can be formed in the openings 14a and on the regions of the bulk metal layer 9 exposed by the openings 14a. Next, the structure including the patterned circuit layer 801, the polymer layer 98 and the metal bumps 89 can be formed at the active side of the thinned silicon substrate 1, which can be referred to as the steps illustrated in Figs. 15D-15H and 15M. Next, the flux is removed. Thereafter, the semiconductor wafer 10 can be cut into a plurality of individual semiconductor chip by a die-sawing process. After the die-sawing process, using a wire-bonding process, the wirebonded wires 129, such as wirebonded gold wires or wirebonded copper wires, can be bonded onto the regions of the bulk metal layer 9 exposed by the openings 14a in the polymer layer 14 of the semiconductor chip.

[00650] Figs. 26A-26G are cross-sectional views showing a process for forming a bottom scheme 103 of a bottom structure technology at a backside of a semiconductor wafer according to the present disclosure. Referring to Fig. 26A, after the steps illustrated in Figs. 24B, 24C and 25A-25D, a photoresist layer 51, such as positive-type photoresist layer or negative-type photoresist layer, having a thickness between 1 and 200 micrometers, and preferably between 2 and 150 micrometers, can be formed on the photoresist layer 29 and on the topmost layer of copper, gold, aluminum, nickel or palladium of the previously described various bulk metal layer 9 by a spin-on coating process, a screen-printing process, a lamination process or a spraying process. Next, the photoresist layer 51 is patterned with the processes of exposure and development to form multiple openings 51a in the photoresist layer 51 exposing multiple regions 9a of the topmost layer of copper, gold, aluminum, nickel or palladium of the

previously described various bulk metal layer 9. For example, a 1X stepper or 1X contact aligner can be used to expose the photoresist layer 51 during the process of exposure. Each of the openings 51a has a desired width W3, e.g., larger than 5 micrometers, such as between 10 and 30 micrometers, between 20 and 50 micrometers or between 50 and 150 micrometers.

[00651] For example, the photoresist layer 51 can be formed by a suitable process or processes, e.g., by spin-on coating a positive-type photosensitive polymer layer having a thickness between 1 and 200 micrometers, and preferably between 2 and 150 micrometers, on the topmost layer of copper, gold, aluminum, nickel or palladium of the previously described various bulk metal layer 9 and on the photoresist layer 29, then exposing the photosensitive polymer layer using a 1X stepper or a contact aligner with at least two of G-line, H-line and I-line, and G-line has a wavelength ranging from, e.g., about 434 to 438nm, H-line has a wavelength ranging from, e.g., about 403 to 407nm, and I-line has a wavelength ranging from, e.g., about 363 to 367nm, then developing the exposed polymer layer by spraying and puddling a developer on the semiconductor wafer 10 or by immersing the semiconductor wafer 10 into a developer, and then cleaning the semiconductor wafer 10 using deionized wafer and drying the semiconductor wafer 10 by spinning the semiconductor wafer 10. After development, a scum removal process of removing the residual polymeric material or other contaminants from the bulk metal layer 9 may be conducted by using an O_2 plasma or a plasma containing fluorine of below 200PPM and oxygen. By these processes, the photoresist layer 51 can be patterned with the openings 51a exposing the regions 9a of the topmost layer of copper, gold, aluminum, nickel or palladium of the previously described various bulk metal layer 9.

[00652] Referring to Fig. 26B, after the step illustrated in Fig. 26A, multiple metal bumps or pillars 27 having a thickness larger than 1 micrometer can be formed in the openings 51a and on the regions 9a of the topmost layer of copper, gold, aluminum, nickel or palladium of the previously described various bulk metal layer 9 exposed by the openings 51a. The material of the metal bumps or pillars 27 may include gold, nickel, tin, solder, palladium, copper, aluminum or a composite of the previously described materials.

[00653] For example, the metal bumps or pillars 27 can be composed of a single metal layer formed by a suitable process or processes, e.g., by electroplating a copper layer, to a thickness between 10 and 150 micrometers, and preferably between 20 and 100 micrometers, in the openings 51a and on the regions 9a of the topmost layer of copper, gold, aluminum, nickel or palladium of the previously described various bulk metal layer 9 exposed by the

openings 51a using the previously described electroplating solution for electroplating copper of the bulk metal layer 9.

[00654] Alternatively, the metal bumps or pillars 27 can be composed of a single metal layer formed by a suitable process or processes, e.g., by electroplating a gold layer, to a thickness between 1 and 30 micrometers, and preferably between 1 and 25 micrometers, in the openings 51a and on the regions 9a of the topmost layer of copper, gold, aluminum, nickel or palladium of the previously described various bulk metal layer 9 exposed by the openings 51a using the previously described electroplating solution for electroplating gold of the bulk metal layer 9.

[00655] Alternatively, the metal bumps or pillars 27 can be composed of a single metal layer formed by a suitable process or processes, e.g., by electroplating a palladium layer, to a thickness between 1 and 30 micrometers, and preferably between 1 and 25 micrometers, in the openings 51a and on the regions 9a of the topmost layer of copper, gold, aluminum, nickel or palladium of the previously described various bulk metal layer 9 exposed by the openings 51a using the previously described electroplating solution for electroplating palladium of the bulk metal layer 9.

[00656] Alternatively, the metal bumps or pillars 27 can be composed of a single metal layer formed by a suitable process or processes, e.g., by electroplating a nickel layer, to a thickness between 1 and 100 micrometers, and preferably between 5 and 60 micrometers, in the openings 51a and on the regions 9a of the topmost layer of copper, gold, aluminum, nickel or palladium of the previously described various bulk metal layer 9 exposed by the openings 51a using the previously described electroplating solution for electroplating nickel of the bulk metal layer 9.

[00657] Alternatively, the metal bumps or pillars 27 can be composed of double metal layers formed by a suitable process or processes, e.g., by electroplating a copper layer, to a thickness between 10 and 150 micrometers, and preferably between 20 and 100 micrometers, in the openings 51a and on the regions 9a of the topmost layer of copper, gold, aluminum, nickel or palladium of the previously described various bulk metal layer 9 exposed by the openings 51a using the previously described electroplating solution for electroplating copper of the bulk metal layer 9, and then electroplating or electroless plating a gold layer, to a thickness between 0.005 and 10 micrometers, and preferably between 0.05 and 1 micrometer, in the openings 51a and on the electroplated copper layer in the openings 51a using the previously

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described electroplating or electroless plating solution for electroplating or electroless plating gold of the bulk metal layer 9.

[00658] Alternatively, the metal bumps or pillars 27 can be composed of double metal layers formed by a suitable process or processes, e.g., by electroplating a copper layer, to a thickness between 10 and 150 micrometers, and preferably between 20 and 100 micrometers, in the openings 51a and on the regions 9a of the topmost layer of copper, gold, aluminum, nickel or palladium of the previously described various bulk metal layer 9 exposed by the openings 51a using the previously described electroplating solution for electroplating copper of the bulk metal layer 9, and then electroplating or electroless plating a palladium layer, to a thickness between 0.005 and 10 micrometers, and preferably between 0.05 and 1 micrometer, in the openings 51a and on the electroplated copper layer in the openings 51a using the previously described electroplating or electroless plating solution for electroplating or electroless plating palladium of the bulk metal layer 9.

[00659] Alternatively, the metal bumps or pillars 27 can be composed of double metal layers formed by a suitable process or processes, e.g., by electroplating or electroless plating a nickel layer, to a thickness between 1 and 15 micrometers, and preferably between 2 and 10 micrometers, in the openings 51a and on the regions 9a of the topmost layer of copper, gold, aluminum, nickel or palladium of the previously described various bulk metal layer 9 exposed by the openings 51a using the previously described electroplating or electroless plating solution for electroplating or electroless plating nickel of the bulk metal layer 9, and then electroplating or electroless plating a gold layer, to a thickness between 0.005 and 10 micrometers, and preferably between 0.05 and 1 micrometer, in the openings 51a and on the electroplated or electroless plated nickel layer in the openings 51a using the previously described electroplating or electroless plating solution for electroplating or electroless plating gold of the bulk metal layer 9.

[00660] Alternatively, the metal bumps or pillars 27 can be composed of double metal layers formed by a suitable process or processes, e.g., by electroplating or electroless plating a nickel layer, to a thickness between 1 and 15 micrometers, and preferably between 2 and 10 micrometers, in the openings 51a and on the regions 9a of the topmost layer of copper, gold, aluminum, nickel or palladium of the previously described various bulk metal layer 9 exposed by the openings 51a using the previously described electroplating or electroless plating solution for electroplating or electroless plating nickel of the bulk metal layer 9, and then

electroplating or electroless plating a palladium layer, to a thickness between 0.005 and 10 micrometers, and preferably between 0.05 and 1 micrometer, in the openings 51a and on the electroplated or electroless plated nickel layer in the openings 51a using the previously described electroplating or electroless plating solution for electroplating or electroless plating palladium of the bulk metal layer 9.

[00661] Alternatively, the metal bumps or pillars 27 can be composed of triple metal layers formed by a suitable process or processes, e.g., by electroplating a copper layer, to a thickness between 5 and 150 micrometers, and preferably between 10 and 100 micrometers, in the openings 51a and on the regions 9a of the topmost layer of copper, gold, aluminum, nickel or palladium of the previously described various bulk metal layer 9 exposed by the openings 51a using the previously described electroplating solution for electroplating copper of the bulk metal layer 9, next electroplating or electroless plating a nickel layer, to a thickness between 1 and 15 micrometers, and preferably between 2 and 10 micrometers, in the openings 51a and on the electroplated copper layer in the openings 51a using the previously described electroplating or electroless plating solution for electroplating or electroless plating nickel of the bulk metal layer 9, and then electroplating or electroless plating a gold layer, to a thickness between 0.005 and 1 micrometers, and preferably between 0.05 and 0.1 micrometers, in the openings 51a and on the electroplated or electroless plated nickel layer in the openings 51a using the previously described electroplating or electroless plating solution for electroplating or electroless plating gold of the bulk metal layer 9.

[00662] Alternatively, the metal bumps or pillars 27 can be composed of triple metal layers formed by a suitable process or processes, e.g., by electroplating a copper layer, to a thickness between 5 and 150 micrometers, and preferably between 10 and 100 micrometers, in the openings 51a and on the regions 9a of the topmost layer of copper, gold, aluminum, nickel or palladium of the previously described various bulk metal layer 9 exposed by the openings 51a using the previously described electroplating solution for electroplating copper of the bulk metal layer 9, next electroplating or electroless plating a nickel layer, to a thickness between 1 and 15 micrometers, and preferably between 2 and 10 micrometers, in the openings 51a and on the electroplated copper layer in the openings 51a using the previously described electroplating or electroless plating solution for electroplating or electroless plating nickel of the bulk metal layer 9, and then electroplating or electroless plating a palladium layer, to a thickness between 0.005 and 1 micrometers, and preferably between 0.05 and 0.1 micrometers, in the openings 51a and on the electroplated or electroless plated nickel layer in the openings 51a using the

previously described electroplating or electroless plating solution for electroplating or electroless plating palladium of the bulk metal layer 9.

[00663] Alternatively, the metal bumps or pillars 27 can be composed of four metal layers formed by a suitable process or processes, e.g., by electroplating a copper layer, to a thickness between 5 and 150 micrometers, and preferably between 10 and 100 micrometers, in the openings 51a and on the regions 9a of the topmost layer of copper, gold, aluminum, nickel or palladium of the previously described various bulk metal layer 9 exposed by the openings 51a using the previously described electroplating solution for electroplating copper of the bulk metal layer 9, next electroplating or electroless plating a nickel layer, to a thickness between 1 and 15 micrometers, and preferably between 2 and 10 micrometers, in the openings 51a and on the electroplated copper layer in the openings 51a using the previously described electroplating or electroless plating solution for electroplating or electroless plating nickel of the bulk metal layer 9, next electroplating or electroless plating a palladium layer, to a thickness between 0.005 and 1 micrometers, and preferably between 0.05 and 0.1 micrometers, in the openings 51a and on the electroplated or electroless plated nickel layer in the openings 51a using the previously described electroplating or electroless plating solution for electroplating or electroless plating palladium of the bulk metal layer 9, and then electroplating or electroless plating a gold layer, to a thickness between 0.005 and 1 micrometers, and preferably between 0.05 and 0.1 micrometers, in the openings 51a and on the electroplated or electroless plated palladium layer in the openings 51a using the previously described electroplating or electroless plating solution for electroplating or electroless plating gold of the bulk metal layer 9.

[00664] Alternatively, the metal bumps or pillars 27 can be composed of double metal layers formed by a suitable process or processes, e.g., by electroplating a copper layer, to a thickness between 5 and 150 micrometers, and preferably between 10 and 100 micrometers, in the openings 51a and on the regions 9a of the topmost layer of copper, gold, aluminum, nickel or palladium of the previously described various bulk metal layer 9 exposed by the openings 51a using the previously described electroplating solution for electroplating copper of the bulk metal layer 9, and then electroplating or electroless plating a solder layer, such as a bismuth-containing layer, an indium-containing layer or a tin-containing layer of a tin-lead alloy, a tin-silver alloy or a tin-silver-copper alloy, to a thickness between 5 and 250 micrometers, and preferably between 10 and 100 micrometer, in the openings 51a and on the electroplated copper layer in the openings 51a.

[00665] Alternatively, the metal bumps or pillars 27 can be composed of double metal layers formed by a suitable process or processes, e.g., by electroplating a nickel layer, to a thickness between 5 and 150 micrometers, and preferably between 10 and 60 micrometers, in the openings 51a and on the regions 9a of the topmost layer of copper, gold, aluminum, nickel or palladium of the previously described various bulk metal layer 9 exposed by the openings 51a using the previously described electroplating solution for electroplating nickel of the bulk metal layer 9, and then electroplating or electroless plating a solder layer, such as a bismuth-containing layer, an indium-containing layer or a tin-containing layer of a tin-lead alloy, a tin-silver alloy or a tin-silver-copper alloy, to a thickness between 5 and 250 micrometers, and preferably between 10 and 100 micrometer, in the openings 51a and on the electroplated nickel layer in the openings 51a.

[00666] Alternatively, the metal bumps or pillars 27 can be composed of triple metal layers formed by a suitable process or processes, e.g., by electroplating a copper layer, to a thickness between 5 and 150 micrometers, and preferably between 10 and 100 micrometers, in the openings 51a and on the regions 9a of the topmost layer of copper, gold, aluminum, nickel or palladium of the previously described various bulk metal layer 9 exposed by the openings 51a using the previously described electroplating solution for electroplating copper of the bulk metal layer 9, next electroplating or electroless plating a nickel layer, to a thickness between 1 and 15 micrometers, and preferably between 2 and 10 micrometers, in the openings 51a and on the electroplated copper layer in the openings 51a using the previously described electroplating or electroless plating solution for electroplating or electroless plating nickel of the bulk metal layer 9, and then electroplating or electroless plating a solder layer, such as a bismuth-containing layer, an indium-containing layer or a tin-containing layer of a tin-lead alloy, a tin-silver alloy or a tin-silver-copper alloy, to a thickness between 5 and 100 micrometers, and preferably between 10 and 50 micrometers, in the openings 51a and on the electroplated or electroless plated nickel layer in the openings 51a.

[00667] Alternatively, the metal bumps or pillars 27 can be composed of triple metal layers formed by a suitable process or processes, e.g., by electroplating a copper layer, to a thickness between 1 and 10 micrometers, and preferably between 3 and 8 micrometers, in the openings 51a and on the regions 9a of the topmost layer of copper, gold, aluminum, nickel or palladium of the previously described various bulk metal layer 9 exposed by the openings 51a using the previously described electroplating solution for electroplating copper of the bulk metal layer 9, next electroplating or electroless plating a nickel layer, to a thickness between 1

and 15 micrometers, and preferably between 2 and 10 micrometers, in the openings 51a and on the electroplated copper layer in the openings 51a using the previously described electroplating or electroless plating solution for electroplating or electroless plating nickel of the bulk metal layer 9, and then electroplating or electroless plating a solder layer, such as a bismuth-containing layer, an indium-containing layer or a tin-containing layer of a tin-lead alloy, a tin-silver alloy or a tin-silver-copper alloy, to a thickness between 30 and 250 micrometers, and preferably between 50 and 150 micrometers, in the openings 51a and on the electroplated or electroless plated nickel layer in the openings 51a.

[00668] Alternatively, the metal bumps or pillars 27 can be composed of double metal layers formed by a suitable process or processes, e.g., by electroplating a copper layer, to a thickness between 5 and 150 micrometers, and preferably between 10 and 100 micrometers, in the openings 51a and on the regions 9a of the topmost layer of copper, gold, aluminum, nickel or palladium of the previously described various bulk metal layer 9 exposed by the openings 51a using the previously described electroplating solution for electroplating copper of the bulk metal layer 9, and then electroplating or electroless plating a solder layer, such as a bismuth-containing layer, an indium-containing layer or a tin-containing layer of a tin-lead alloy, a tin-silver alloy or a tin-silver-copper alloy, to a thickness between 5 and 100 micrometers, and preferably between 10 and 50 micrometers, in the openings 51a and on the electroplated copper layer in the openings 51a.

[00669] Referring to Fig. 26C, after forming the metal bumps or pillars 27, the photoresist layers 29 and 51 are removed using an inorganic solution or using an organic solution with amide. Some residuals from the photoresist layers 29 and 51 could remain on the seed layer 4b of the metal layer 4, on the bulk metal layer 9 and on the metal bumps or pillars 27. Thereafter, the residuals can be removed from the seed layer 4b, from the bulk metal layer 9 and from the metal bumps or pillars 27 with a plasma, such as an O_2 plasma or a plasma containing fluorine of below 200PPM and oxygen.

[00670] Accordingly, the metal bumps or pillars 27 can be formed on the bulk metal layer 9 after the photoresist layers 29 and 51 are removed. Each of the metal bumps or pillars 27 has a width W3 larger than 5 micrometers, such as between 10 and 30 micrometers, between 20 and 50 micrometers or between 50 and 150 micrometers, and larger than that of each of the fine-line metal layers 60, and has a height H1 larger than 1 micrometer, such as between 1 and 300 micrometers, between 5 and 250 micrometers, between 10 and 100

micrometers or between 5 and 50 micrometers. A pitch P1 between neighboring two metal bumps or pillars 27 can be between 10 and 50 micrometers or between 50 and 200 micrometers. The metal bumps or pillars 27 can be used to be bonded with an external circuit, such as semiconductor chip, printed circuit board, ball-grid-array (BGA) substrate, flexible substrate, metal substrate, glass substrate or ceramic substrate.

[00671] Alternatively, another process for forming the metal bumps or pillars 27 on the bulk metal layer 9 can be performed by the following steps. Referring to Fig. 26D, after the steps illustrated in Figs. 24B, 24C and 25A-25D, the photoresist layer 29 can be removed using an inorganic solution or using an organic solution with amide. After removing the photoresist layer 29, the photoresist layer 51 illustrated in Fig. 26A can be formed on the topmost layer of copper, gold, aluminum, nickel or palladium of the previously described various bulk metal layer 9 and on the seed layer 4b of the metal layer 4 by a spin-on coating process, a lamination process, a screen-printing process or a spraying process. Next, the photoresist layer 51 is patterned with the processes of exposure and development to form the openings 51a in the photoresist layer 51 exposing the regions 9a of the topmost layer of copper, gold, aluminum, nickel or palladium of the previously described various bulk metal layer 9. Each of the openings 51a has a width W3 larger than 5 micrometers, such as between 10 and 30 micrometers, between 20 and 50 micrometers or between 50 and 150 micrometers. The process of forming the photoresist layer 51 and the openings 51a in the photoresist layer 51 as shown in Fig. 26D can be referred to as the process of forming the photoresist layer 51 and the openings 51a in the photoresist layer 51 as illustrated in Fig. 26A.

[00672] Referring to Fig. 26E, after the step illustrated in Fig. 26D, the metal bumps or pillars 27 illustrated in Fig. 26B are formed in the openings 51a and on the regions 9a of the topmost layer of copper, gold, aluminum, nickel or palladium of the previously described various bulk metal layer 9 exposed by the openings 51a, which can be referred to as the step illustrated in Fig. 26B. The specification of the metal bumps or pillars 27 shown in Fig. 26E can be referred to as the specification of the metal bumps or pillars 27 illustrated in Fig. 26B. After forming the metal bumps or pillars 27 as illustrated in Fig. 26E, the photoresist layer 51 is removed using an inorganic solution or using an organic solution with amide. Accordingly, the metal bumps or pillars 27 can be formed on the bulk metal layer 9 after removing the photoresist layer 51.

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[00673] Referring to Fig. 26F, after forming the metal bumps or pillars 27 on the bulk metal layer 9, the metal layer 4 not under the bulk metal layer 9 is removed by etching the seed layer 4b not under the bulk metal layer 9, and then etching the adhesion/barrier layer 4a not under the bulk metal layer 9. The process of removing the seed layer 4b not under the bulk metal layer 9 and the adhesion/barrier layer 4a not under the bulk metal layer 9 as shown in Fig. 26F can be referred to as the process of removing the seed layer 4b not under the bulk metal layer 9 and the adhesion/barrier layer 4a not under the bulk metal layer 9 as illustrated in Fig. 25F.

[00674] Accordingly, the interconnecting structures 88 provided by the metal layer 4 and the bulk metal layer 9 can be formed in the through-silicon vias 11a, 11b, 11c, 11d and 11e, on the insulating layer 3 and at the backside 1a of the thinned silicon substrate 1, and sidewalls of the bulk metal layer 9 are not covered by the adhesion/barrier layer 4a and the seed layer 4b of the metal layer 4. The interconnecting structures 88 connects the off-chip buffer 42 to the internal circuits 21, 22, 23 and 24, connects the off-chip buffer 42 to the metal bump or pillar 27, and connects the internal circuits 21, 22, 23 and 24 to the metal bumps or pillars 27. The off-chip ESD circuit 43 is connected to the off-chip buffer 42 through the fine-line metal trace 639, and to the metal bump or pillar 27 through the interconnecting structure 88.

[00675] Next, referring to Fig. 26G, a polymer layer 14 is formed on the topmost layer of copper, gold, aluminum, nickel or palladium of the previously described various bulk metal layer 9 of the interconnecting structures 88, on the insulating layer 3 and at the backside 1a of the thinned silicon substrate 1, and multiple openings 14a are formed in the polymer layer 14 to uncover the top surfaces and the sidewalls of the metal bumps or pillars 27. Accordingly, a bottom scheme 103 at the backside 1a of the thinned silicon substrate 1 is formed with the insulating layer 3, the interconnecting structures 88 provided by the metal layers 4 and 9, the metal bumps or pillars 27, and the polymer layer 14, and the openings 14a in the polymer layer 14 are over the interconnecting structures 88. After the step illustrated in Fig. 26G, the semiconductor wafer 10 can be cut into a plurality of individual semiconductor chip by a die-sawing process.

[00676] Alternatively, after the step illustrated in Fig. 26G, with the following steps being illustrated with reverse figures for simple explanation, multiple openings 50 are formed in the passivation layer 5 to expose the metal traces or pads 600, and then each of the over-passivation schemes 102 illustrated in Figs. 15H, 15K-15M, 16L, 16M, 17J, 18I,

19H and 20 can be alternatively formed over the passivation layer 5 at the active side of the thinned silicon substrate 1. Thereafter, the semiconductor wafer 10 can be cut into a plurality of individual semiconductor chip by a die-sawing process.

[00677] Alternatively, a process of forming any one of the over-passivation schemes 102 illustrated in Figs. 15H, 15K-15M, 16L, 16M, 17J, 18I, 19H and 20 over the passivation layer 5 can be performed before the steps illustrated in Figs. 24B, 24C, 25A-25D and 26A-26G. After the steps illustrated in Figs. 24B, 24C, 25A-25D and 26A-26G, the semiconductor wafer 10 can be cut into a plurality of individual semiconductor chip by a die-sawing process.

[00678] After the die-sawing process, the semiconductor chip cut from the semiconductor wafer 10 can be packaged for a chip package. In the chip package, the semiconductor chip can be connected to an external circuit, such as ball-grid-array (BGA) substrate, printed circuit board, semiconductor chip, metal substrate, glass substrate or ceramic substrate, through the metal bumps or pillars 27 of the bottom scheme 103. The semiconductor chip includes the bottom scheme 103, and the bottom scheme 103 includes the insulating layer 3 on the backside 1a of the thinned silicon substrate 1 and in the through-silicon vias 11a, 11b, 11c, 11d and 11e, the interconnecting structures 88 at the backside 1a of the thinned silicon substrate 1, in the through-silicon vias 11a, 11b, 11c, 11d and 11e and on the insulating layer 3, the polymer layer 14 at the backside 1a of the thinned silicon substrate 1, on the interconnecting structures 88 and on the insulating layer 3, and the metal bumps or pillars 27 at the backside 1a of the thinned silicon substrate 1 and on the interconnecting structures 88.

[00679] Fig. 26H is a cross-sectional view showing a semiconductor wafer, which can be formed by a suitable process or processes, e.g., by the following steps. First, the semiconductor wafer 10 illustrated in Fig. 24A includes multiple openings 531, 532, 534, 539 and 539' in the passivation layer 5 to expose multiple regions 600a of the metal traces or pads 600. The openings 531, 532, 534, 539 and 539' are over the regions 600a of the metal traces or pads 600, and the regions 600a of the metal traces or pads 600 are at bottoms of the openings 531, 532, 534, 539 and 539'. Next, a flux 32 can be formed in the openings 531, 532, 534, 539 and 539' and on the regions 600a of the metal traces or pads 600 exposed by the openings 531, 532, 534, 539 and 539'. Next, the step illustrated in Fig. 24B can be performed. Next, the through silicon vias 11a, 11b, 11c, 11d and 11e can be formed in the thinned silicon substrate 1, and the insulating layer 3 can be formed on the backside 1a of the thinned silicon substrate 1 and on the sidewalls of the through silicon vias 11a, 11b, 11c, 11d and 11e, which can be

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referred to as the steps illustrated in Figs. 24C-24H or Figs. 24I-24N. Next, the interconnecting structures 88 can be formed in the through silicon vias 11a, 11b, 11c, 11d and 11e, on the insulating layer 3 and at the backside 1a of the thinned silicon substrate 1, and the metal bumps or pillars 27 can be formed on the interconnecting structures 88, which can be referred to as the steps illustrated in Figs. 25A-25D and 26A-26F. Next, the polymer layer 14 is formed on the interconnecting structures 88, on the insulating layer 3 and at the backside 1a of the thinned silicon substrate 1, and the openings 14a are formed in the polymer layer 14 to uncover the top surfaces and the sidewalls of the metal bumps or pillars 27. Accordingly, a bottom scheme 103 same as the bottom scheme 103 shown in Fig. 26G can be formed at the backside 1a of the thinned silicon substrate 1.

[00680] After forming the structure shown in Fig. 26H, the flux 32 is removed. Next, with the following steps being illustrated with reverse figures for simple explanation, each of the over-passivation schemes 102 illustrated in Figs. 15H, 15K-15M, 16L, 16M, 17J, 18I, 19H and 20 can be alternatively formed over the passivation layer 5 at the active side of the thinned silicon substrate 1. Thereafter, the semiconductor wafer 10 can be cut into a plurality of individual semiconductor chip by a die-sawing process. After the die-sawing process, the semiconductor chip cut from the semiconductor wafer 10 can be packaged for a chip package. In the chip package, the semiconductor chip can be connected to a first external circuit, such as ball-grid-array (BGA) substrate, printed circuit board, semiconductor chip, metal substrate, glass substrate or ceramic substrate, through the metal bumps or pillars 27 of the bottom scheme 103, and/or to a second external circuit, such as ball-grid-array (BGA) substrate, printed circuit board, semiconductor chip, metal substrate, glass substrate or ceramic substrate, through one of the over-passivation schemes 102 illustrated in Figs. 15H, 15K-15M, 16L, 16M, 17J, 18I, 19H and 20. The interconnecting structures 88 connect the off-chip buffer 42 to the internal circuits 21, 22, 23 and 24, and connect the metal bumps or pillars 27 to the off-chip buffer 42, to the off-chip ESD circuit 43 and to the internal circuits 21, 22, 23 and 24.

[00681] Fig. 26I is a cross-sectional view showing a semiconductor wafer, which can be formed by a suitable process or processes, e.g., by the following steps. First, the semiconductor wafer 10 illustrated in Fig. 24A includes multiple openings 531, 532, 534, 539 and 539' in the passivation layer 5 to expose multiple regions 600a of the metal traces or pads 600. The openings 531, 532, 534, 539 and 539' are over the regions 600a of the metal traces or pads 600, and the regions 600a of the metal traces or pads 600 are at bottoms of the openings 531, 532, 534, 539 and 539'. Next, the metal pads, bumps or traces 34a can be formed on the passivation

layer 5 and on the regions 600a of the metal traces or pads 600 exposed by the openings 531, 532, 534, 539 and 539', which can be referred to as the process illustrated in Fig. 25N. The specification of the metal pads, bumps or traces 34a shown in Fig. 26I can be referred to as the specification of the metal pads, bumps or traces 34a as illustrated in Fig. 25N. After forming the metal pads, bumps or traces 34a, the step illustrated in Fig. 24B can be performed. Next, the through silicon vias 11a, 11b, 11c, 11d and 11e can be formed in the thinned silicon substrate 1, and the insulating layer 3 can be formed on the backside 1a of the thinned silicon substrate 1 and on the sidewalls of the through silicon vias 11a, 11b, 11c, 11d and 11e, which can be referred to as the steps illustrated in Figs. 24C-24H or Figs. 24I-24N. Next, the interconnecting structures 88 can be formed in the through silicon vias 11a, 11b, 11c, 11d and 11e, on the insulating layer 3 and at the backside 1a of the thinned silicon substrate 1, and the metal bumps or pillars 27 can be formed on the interconnecting structures 88, which can be referred to as the steps illustrated in Figs. 25A-25D and 26A-26F. Next, the polymer layer 14 is formed on the interconnecting structures 88, on the insulating layer 3 and at the backside 1a of the thinned silicon substrate 1, and the openings 14a are formed in the polymer layer 14 to uncover the top surfaces and the sidewalls of the metal bumps or pillars 27. Accordingly, a bottom scheme 103 same as the bottom scheme 103 shown in Fig. 26G can be formed at the backside 1a of the thinned silicon substrate 1. Alternatively, the step of forming the metal pads, bumps or traces 34a on the passivation layer 5 and on the regions 600a of the metal traces or pads 600 exposed by the openings 531, 532, 534, 539 and 539' can be performed after forming the polymer layer 14.

[00682] After forming the structure shown in Fig. 26I, the semiconductor wafer 10 can be cut into a plurality of individual semiconductor chip by a die-sawing process. After the die-sawing process, the semiconductor chip cut from the semiconductor wafer 10 can be packaged for a chip package. In the chip package, the semiconductor chip can be connected to a first external circuit, such as printed circuit board, semiconductor chip, ball-grid-array (BGA) substrate, metal substrate, glass substrate or ceramic substrate, through the metal pads, bumps or traces 34a, and to a second external circuit, such as printed circuit board, ball-grid-array (BGA) substrate, semiconductor chip, metal substrate, glass substrate or ceramic substrate, through the metal bumps or pillars 27 of the bottom scheme 103. The interconnecting structures 88 connect the off-chip buffer 42 to the internal circuits 21, 22, 23 and 24, and connect the metal bumps or pillars 27 to the off-chip buffer 42, to the off-chip ESD circuit 43 and to the internal circuits 21, 22, 23 and 24.

[00683] Fig. 26J is a cross-sectional view showing a semiconductor wafer, which can be formed by a suitable process or processes, e.g., by the following steps. First, the semiconductor wafer 10 illustrated in Fig. 24A includes multiple openings 531, 532, 534, 539 and 539' in the passivation layer 5 to expose multiple regions 600a of the metal traces or pads 600. The openings 531, 532, 534, 539 and 539' are over the regions 600a of the metal traces or pads 600, and the regions 600a of the metal traces or pads 600 are at bottoms of the openings 531, 532, 534, 539 and 539'. Next, a patterned circuit layer 801 composed of an adhesion/barrier/seed layer 8011 and a metal layer 8012 can be formed on the passivation layer 5 and on the regions 600a of the metal traces or pads 600 exposed by the openings 531, 532, 534, 539 and 539', which can be referred to as the steps illustrated in Figs. 15D-15H. Next, a polymer layer 98 is formed on the metal layer 8012 of the patterned circuit layer 801 and on the passivation layer 5, and an opening 980 in the polymer layer 98 is over a contact point 801a of the metal layer 8012 of the patterned circuit layer 801 and exposes it, which can be referred to as the process illustrated in Fig. 15I. Accordingly, an over-passivation scheme 102 can be formed with the patterned circuit layer 801 and the polymer layer 98, at the active side of the thinned silicon substrate 1. Next, a flux 32 is formed in the opening 980 and on the contact point 801a of the metal layer 8012 exposed by the opening 980. Next, the step illustrated in Fig. 24B can be performed. Next, the through silicon vias 11a, 11b, 11c, 11d and 11e can be formed in the thinned silicon substrate 1, and the insulating layer 3 can be formed on the backside 1a of the thinned silicon substrate 1 and on the sidewalls of the through silicon vias 11a, 11b, 11c, 11d and 11e, which can be referred to as the steps illustrated in Figs. 24C-24H or Figs. 24I-24N. Next, the interconnecting structures 88 can be formed in the through silicon vias 11a, 11b, 11c, 11d and 11e, on the insulating layer 3 and at the backside 1a of the thinned silicon substrate 1, and the metal bumps or pillars 27 can be formed on the interconnecting structures 88, which can be referred to as the steps illustrated in Figs. 25A-25D and 26A-26F. Next, the polymer layer 14 is formed on the interconnecting structures 88, on the insulating layer 3 and at the backside 1a of the thinned silicon substrate 1, and the openings 14a are formed in the polymer layer 14 to uncover the top surfaces and the sidewalls of the metal bumps or pillars 27. Accordingly, a bottom scheme 103 same as the bottom scheme 103 shown in Fig. 26G can be formed at the backside 1a of the thinned silicon substrate 1. Alternatively, the steps of forming the patterned circuit layer 801 and the polymer layer 98 can be performed after forming the polymer layer 14.

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[00684] After forming the structure shown in Fig. 26J, the flux 32 is removed. Thereafter, the semiconductor wafer 10 can be cut into a plurality of individual semiconductor chip by a die-sawing process. After the die-sawing process, the semiconductor chip cut from the semiconductor wafer 10 can be packaged for a chip package. In the chip package, the semiconductor chip can be connected to a first external circuit, such as printed circuit board, semiconductor chip, ball-grid-array (BGA) substrate, metal substrate, glass substrate or ceramic substrate, by wirebonding a gold wire or a copper wire to the contact point 801a of gold, copper or aluminum of the patterned circuit layer 801 and to the first external circuit or by solder bonding the contact point 801a of the patterned circuit layer 801 with a gold layer or a tin-alloy layer of the first external circuit, and can be connected to a second external circuit, such as printed circuit board, ball-grid-array (BGA) substrate, semiconductor chip, metal substrate, glass substrate or ceramic substrate, through the metal bumps or pillars 27 of the bottom scheme 103. The interconnecting structures 88 connect the off-chip buffer 42 to the internal circuits 21, 22, 23 and 24, and connect the metal bumps or pillars 27 to the off-chip buffer 42, to the off-chip ESD circuit 43 and to the internal circuits 21, 22, 23 and 24.

[00685] Fig. 26K is a cross-sectional view showing a semiconductor wafer, which can be formed by a suitable process or processes, e.g., by the following steps. First, the semiconductor wafer 10 illustrated in Fig. 24A includes multiple openings 531, 532, 534, 539 and 539' in the passivation layer 5 to expose multiple regions 600a of the metal traces or pads 600. The openings 531, 532, 534, 539 and 539' are over the regions 600a of the metal traces or pads 600, and the regions 600a of the metal traces or pads 600 are at bottoms of the openings 531, 532, 534, 539 and 539'. Next, a patterned circuit layer 801 composed of an adhesion/barrier/seed layer 8011 and a metal layer 8012 can be formed on the passivation layer 5 and on the regions 600a of the metal traces or pads 600 exposed by the openings 531, 532, 534, 539 and 539', and multiple metal bumps or pillars 141 can be formed on multiple regions of gold, copper, nickel, aluminum or palladium of the metal layer 8012 of the patterned circuit layer 801. The adhesion/barrier/seed layer 8011 is formed on the passivation layer 5 and on the regions 600a of the metal traces or pads 600 exposed by the openings 531, 532, 534, 539 and 539', and the metal layer 8012 is formed on the adhesion/barrier/seed layer 8011. After forming the metal bumps or pillars 141, a polymer layer 98 can be formed on the metal layer 8012 of the patterned circuit layer 801 and on the passivation layer 5, and multiple openings 980 are formed in the polymer layer 98 to uncover top surfaces and sidewalls of the metal bumps or pillars 141. Accordingly, an over-passivation scheme 102 can be formed with the

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patterned circuit layer 801, the metal bumps or pillars 141 and the polymer layer 98, at the active side of the thinned silicon substrate 1. Next, the step illustrated in Fig. 24B can be performed. Next, the through silicon vias 11a, 11b, 11c, 11d and 11e can be formed in the thinned silicon substrate 1, and the insulating layer 3 can be formed on the backside 1a of the thinned silicon substrate 1 and on the sidewalls of the through silicon vias 11a, 11b, 11c, 11d and 11e, which can be referred to as the steps illustrated in Figs. 24C-24H or Figs. 24I-24N. Next, the interconnecting structures 88 can be formed in the through silicon vias 11a, 11b, 11c, 11d and 11e, on the insulating layer 3 and at the backside 1a of the thinned silicon substrate 1, and the metal bumps or pillars 27 can be formed on the interconnecting structures 88, which can be referred to as the steps illustrated in Figs. 25A-25D and 26A-26F. Next, the polymer layer 14 is formed on the interconnecting structures 88, on the insulating layer 3 and at the backside 1a of the thinned silicon substrate 1, and the openings 14a are formed in the polymer layer 14 to uncover the top surfaces and the sidewalls of the metal bumps or pillars 27. Accordingly, a bottom scheme 103 same as the bottom scheme 103 shown in Fig. 26G can be formed at the backside 1a of the thinned silicon substrate 1. Alternatively, the steps of forming the patterned circuit layer 801, the metal bumps or pillars 141 and the polymer layer 98 can be performed after forming the polymer layer 14.

[00686] The metal bumps or pillars 141 have a width larger than 3 micrometers, such as between 5 and 100 micrometers, and a height grater than 1 micrometer, such as between 5 and 150 micrometers or between 10 and 100 micrometers. The material of the metal bumps or pillars 141 may include gold, copper, nickel, aluminum, palladium, solder or a composite of the previously described materials. The metal bumps or pillars 141 can be used to be bonded with an external circuit, such as printed circuit board, flexible substrate, ball-grid-array (BGA) substrate, semiconductor chip, metal substrate, glass substrate or ceramic substrate.

[00687] The metal bumps or pillars 141, for example, can be composed of a single metal layer formed by a suitable process or processes, e.g., by electroplating a copper layer, to a thickness between 5 and 100 micrometers, between 10 and 150 micrometers or between 20 and 100 micrometers, on the regions of gold, copper, nickel, aluminum or palladium of the metal layer 8012.

[00688] Alternatively, the metal bumps or pillars 141 can be composed of a single metal layer formed by a suitable process or processes, e.g., by electroplating a gold layer, to a thickness between 1 and 30 micrometers, between 10 and 25 micrometers or between 3 and 50

micrometers, on the regions of gold, copper, nickel, aluminum or palladium of the metal layer 8012.

[00689] Alternatively, the metal bumps or pillars 141 can be composed of a single metal layer formed by a suitable process or processes, e.g., by electroplating a palladium layer, to a thickness between 1 and 30 micrometers, between 10 and 25 micrometers or between 3 and 50 micrometers, on the regions of gold, copper, nickel, aluminum or palladium of the metal layer 8012.

[00690] Alternatively, the metal bumps or pillars 141 can be composed of a single metal layer formed by a suitable process or processes, e.g., by electroplating a nickel layer, to a thickness between 5 and 100 micrometers, and preferably between 10 and 60 micrometers, on the regions of gold, copper, nickel, aluminum or palladium of the metal layer 8012.

[00691] Alternatively, the metal bumps or pillars 141 can be composed of double metal layers formed by a suitable process or processes, e.g., by electroplating a copper layer, to a thickness between 5 and 100 micrometers, between 10 and 150 micrometers or between 20 and 100 micrometers, on the regions of gold, copper, nickel, aluminum or palladium of the metal layer 8012, and then electroplating or electroless plating a gold layer or a palladium layer, to a thickness between 0.005 and 10 micrometers, and preferably between 0.05 and 1 micrometers, on the electroplated copper layer.

[00692] Alternatively, the metal bumps or pillars 141 can be composed of double metal layers formed by a suitable process or processes, e.g., by electroplating or electroless plating a nickel layer, to a thickness between 1 and 15 micrometers, and preferably between 2 and 10 micrometers, on the regions of gold, copper, nickel, aluminum or palladium of the metal layer 8012, and then electroplating or electroless plating a gold layer or a palladium layer, to a thickness between 0.005 and 10 micrometers, and preferably between 0.05 and 1 micrometers, on the electroplated or electroless plated nickel layer.

[00693] Alternatively, the metal bumps or pillars 141 can be composed of triple metal layers formed by a suitable process or processes, e.g., by electroplating a copper layer, to a thickness between 5 and 150 micrometers, and preferably between 10 and 100 micrometers, on the regions of gold, copper, nickel, aluminum or palladium of the metal layer 8012, next electroplating or electroless plating a nickel layer, to a thickness between 1 and 15 micrometers, and preferably between 2 and 10 micrometers, on the electroplated copper layer, and then electroplating or electroless plating a gold layer or a palladium layer, to a thickness between

0.005 and 1 micrometers, and preferably between 0.05 and 0.1 micrometers, on the electroplated or electroless plated nickel layer.

[00694] Alternatively, the metal bumps or pillars 141 can be composed of four metal layers formed by a suitable process or processes, e.g., by electroplating a copper layer, to a thickness between 5 and 150 micrometers, and preferably between 10 and 100 micrometers, on the regions of gold, copper, nickel, aluminum or palladium of the metal layer 8012, next electroplating or electroless plating a nickel layer, to a thickness between 1 and 15 micrometers, and preferably between 2 and 10 micrometers, on the electroplated copper layer, next electroplating or electroless plating a palladium layer, to a thickness between 0.005 and 1 micrometers, and preferably between 0.05 and 0.1 micrometers, on the electroplated or electroless plated nickel layer, and then electroplating or electroless plating a gold layer, to a thickness between 0.005 and 1 micrometers, and preferably between 0.05 and 0.1 micrometers, on the electroplated or electroless plated palladium layer.

[00695] Alternatively, the metal bumps or pillars 141 can be composed of double metal layers formed by a suitable process or processes, e.g., by electroplating a copper layer, to a thickness between 5 and 150 micrometers, and preferably between 10 and 100 micrometers, on the regions of gold, copper, nickel, aluminum or palladium of the metal layer 8012, and then electroplating or electroless plating a solder layer, such as a bismuth-containing layer, an indium-containing layer or a tin-containing layer of a tin-lead alloy, a tin-silver alloy or a tin-silver-copper alloy, to a thickness between 5 and 100 micrometers, and preferably between 10 and 50 micrometer, on the electroplated copper layer.

[00696] Alternatively, the metal bumps or pillars 141 can be composed of double metal layers formed by a suitable process or processes, e.g., by electroplating a nickel layer, to a thickness between 5 and 150 micrometers, and preferably between 10 and 100 micrometers, on the regions of gold, copper, nickel, aluminum or palladium of the metal layer 8012, and then electroplating or electroless plating a solder layer, such as a bismuth-containing layer, an indium-containing layer or a tin-containing layer of a tin-lead alloy, a tin-silver alloy or a tin-silver-copper alloy, to a thickness between 5 and 250 micrometers, and preferably between 10 and 100 micrometer, on the electroplated nickel layer.

[00697] Alternatively, the metal bumps or pillars 141 can be composed of triple metal layers formed by a suitable process or processes, e.g., by electroplating a copper layer, to a thickness between 5 and 150 micrometers, and preferably between 10 and 100 micrometers, on

the regions of gold, copper, nickel, aluminum or palladium of the metal layer 8012, next electroplating or electroless plating a nickel layer, to a thickness between 1 and 15 micrometers, and preferably between 2 and 10 micrometers, on the electroplated copper layer, and then electroplating or electroless plating a solder layer, such as a bismuth-containing layer, an indium-containing layer or a tin-containing layer of a tin-lead alloy, a tin-silver alloy or a tin-silver-copper alloy, to a thickness between 5 and 100 micrometers, and preferably between 10 and 50 micrometers, on the electroplated or electroless plated nickel layer.

[00698] Alternatively, the metal bumps or pillars 141 can be composed of triple metal layers formed by a suitable process or processes, e.g., by electroplating a copper layer, to a thickness between 1 and 10 micrometers, and preferably between 3 and 8 micrometers, on the regions of gold, copper, nickel, aluminum or palladium of the metal layer 8012, next electroplating or electroless plating a nickel layer, to a thickness between 1 and 15 micrometers, and preferably between 2 and 10 micrometers, on the electroplated copper layer, and then electroplating or electroless plating a solder layer, such as a bismuth-containing layer, an indium-containing layer or a tin-containing layer of a tin-lead alloy, a tin-silver alloy or a tin-silver-copper alloy, to a thickness between 30 and 250 micrometers, and preferably between 50 and 150 micrometers, on the electroplated or electroless plated nickel layer.

[00699] Alternatively, the metal bumps or pillars 141 can be composed of double metal layers formed by a suitable process or processes, e.g., by electroplating a copper layer, to a thickness between 5 and 150 micrometers, and preferably between 10 and 100 micrometers, on the regions of gold, copper, nickel, aluminum or palladium of the metal layer 8012, and then electroplating or electroless plating a solder layer, such as a bismuth-containing layer, an indium-containing layer or a tin-containing layer of a tin-lead alloy, a tin-silver alloy or a tin-silver-copper alloy, to a thickness between 5 and 100 micrometers, and preferably between 10 and 50 micrometers, on the electroplated copper layer.

[00700] After forming the structure shown in Fig. 26K, the semiconductor wafer 10 can be cut into a plurality of individual semiconductor chip by a die-sawing process. After the die-sawing process, the semiconductor chip cut from the semiconductor wafer 10 can be packaged for a chip package. In the chip package, the semiconductor chip can be connected to a first external circuit, such as ball-grid-array (BGA) substrate, printed circuit board, semiconductor chip, metal substrate, glass substrate or ceramic substrate, through the metal bumps or pillars 141 of the over-passivation scheme 102, and can be connected to a second

external circuit, such as ball-grid-array (BGA) substrate, printed circuit board, semiconductor chip, metal substrate, glass substrate or ceramic substrate, through the metal bumps or pillars 27 of the bottom scheme 103. The patterned circuit layer 801 composed of the metal layers 8011 and 8012 at the active side of the thinned silicon substrate 1 connects the off-chip buffer 42 to the internal circuits 21, 22, 23 and 24, and connects the off-chip buffer 42 and the internal circuits 21, 22, 23 and 24 to the first external circuit through the metal bumps or pillars 141. The interconnecting structures 88 provided by the metal layers 4 and 9 at the backside 1a of the thinned silicon substrate 1 connect the off-chip buffer 42 to the internal circuits 21, 22, 23 and 24, and connect the off-chip buffer 42 and the internal circuits 21, 22, 23 and 24 to the second external circuit through the metal bumps or pillars 27. The off-chip ESD circuit 43 can be connected to the patterned circuit layer 801 through the fine-line metal trace 639, and to the interconnecting structure 88 through the fine-line metal trace 639.

[00701] Figs. 27A-27Q are cross-sectional views showing a process for forming a bottom scheme 103 of a bottom structure technology at a backside of a semiconductor wafer according to the present disclosure. Referring to Fig. 27A, after the steps illustrated in Figs. 24B, 24C and 25A-25D, a photoresist layer 51, such as positive-type photoresist layer or negative-type photoresist layer, having a thickness larger than 1 micrometer, such as between 1 and 120 micrometers, and preferably between 5 and 50 micrometers, can be formed on the photoresist layer 29 and on the topmost layer of copper, gold, aluminum, nickel or palladium of the previously described various bulk metal layer 9 by a spin-on coating process, a lamination process, a screen-printing process or a spraying process. Next, the photoresist layer 51 is patterned with the processes of exposure and development to form multiple openings 51b in the photoresist layer 51 exposing multiple regions 9a of the topmost layer of copper, gold, aluminum, nickel or palladium of the previously described various bulk metal layer 9. A 1X stepper or 1X contact aligner can be used to expose the photoresist layer 51 during the process of exposure. Each of the openings 51b has a width W4 between 3 and 10 micrometers or between 10 and 30 micrometers. The process of forming the photoresist layer 51 and the openings 51b in the photoresist layer 51 as shown in Fig. 27A can be referred to as the process of forming the photoresist layer 51 and the openings 51a in the photoresist layer 51 as illustrated in Fig. 26A.

[00702] Next, referring to Fig. 27B, multiple via plugs 58 can be formed in the openings 51b and on the regions 9a of the topmost layer of copper, gold, aluminum, nickel or palladium of the previously described various bulk metal layer 9 exposed by the openings 51b. The

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material of the via plugs 58 may include gold, nickel, tin, palladium, silver, aluminum, copper or a composite of the previously described materials.

[00703] For example, the via plugs 58 can be composed of a single metal layer formed by a suitable process or processes, e.g., by electroplating a copper layer, to a thickness between 1 and 100 micrometers, and preferably between 2 and 30 micrometers, in the openings 51b and on the regions 9a of the topmost layer of copper, gold, aluminum, nickel or palladium of the previously described various bulk metal layer 9 exposed by the openings 51b using the previously described electroplating solution for electroplating copper of the bulk metal layer 9.

[00704] Alternatively, the via plugs 58 can be composed of a single metal layer formed by a suitable process or processes, e.g., by electroplating or electroless plating a gold layer, to a thickness between 1 and 100 micrometers, and preferably between 2 and 30 micrometers, in the openings 51b and on the regions 9a of the topmost layer of copper, gold, aluminum, nickel or palladium of the previously described various bulk metal layer 9 exposed by the openings 51b using the previously described electroplating or electroless plating solution for electroplating or electroless plating gold of the bulk metal layer 9.

[00705] Alternatively, the via plugs 58 can be composed of a single metal layer formed by a suitable process or processes, e.g., by electroplating or electroless plating a palladium layer, to a thickness between 1 and 100 micrometers, and preferably between 2 and 30 micrometers, in the openings 51b and on the regions 9a of the topmost layer of copper, gold, aluminum, nickel or palladium of the previously described various bulk metal layer 9 exposed by the openings 51b using the previously described electroplating or electroless plating solution for electroplating or electroless plating palladium of the bulk metal layer 9.

[00706] Alternatively, the via plugs 58 can be composed of a single metal layer formed by a suitable process or processes, e.g., by electroplating or electroless plating a nickel layer, to a thickness between 1 and 100 micrometers, and preferably between 2 and 30 micrometers, in the openings 51b and on the regions 9a of the topmost layer of copper, gold, aluminum, nickel or palladium of the previously described various bulk metal layer 9 exposed by the openings 51b using the previously described electroplating or electroless plating solution for electroplating or electroless plating nickel of the bulk metal layer 9.

[00707] Alternatively, the via plugs 58 can be composed of double metal layers formed by a suitable process or processes, e.g., by electroplating a copper layer, to a thickness between 1 and 100 micrometers, and preferably between 2 and 30 micrometers, in the openings 51b and

on the regions 9a of the topmost layer of copper, gold, aluminum, nickel or palladium of the previously described various bulk metal layer 9 exposed by the openings 51b using the previously described electroplating solution for electroplating copper of the bulk metal layer 9, and then electroplating or electroless plating a gold layer or a palladium layer, to a thickness between 0.005 and 10 micrometers, and preferably between 0.05 and 1 micrometer, in the openings 51b and on the electroplated copper layer in the openings 51b.

[00708] Alternatively, the via plugs 58 can be composed of double metal layers formed by a suitable process or processes, e.g., by electroplating or electroless plating a nickel layer, to a thickness between 1 and 15 micrometers, and preferably between 2 and 10 micrometers, in the openings 51b and on the regions 9a of the topmost layer of copper, gold, aluminum, nickel or palladium of the previously described various bulk metal layer 9 exposed by the openings 51b using the previously described electroplating or electroless plating solution for electroplating or electroless plating nickel of the bulk metal layer 9, and then electroplating or electroless plating a gold layer or a palladium layer, to a thickness between 0.005 and 10 micrometers, and preferably between 0.05 and 1 micrometer, in the openings 51b and on the electroplated or electroless plated nickel layer in the openings 51b.

[00709] Referring to Fig. 27C, after forming the via plugs 58, the photoresist layers 29 and 51 are removed using an inorganic solution or using an organic solution with amide. Some residuals from the photoresist layers 29 and 51 could remain on the bulk metal layer 9 and on the via plugs 58. Thereafter, the residuals can be removed from the bulk metal layer 9 and from the via plugs 58 with a plasma, such as an O_2 plasma or a plasma containing fluorine of below 200PPM and oxygen. Accordingly, the via plugs 58 can be formed on the bulk metal layer 9 after the photoresist layers 29 and 51 are removed. Each of the via plugs 58 has a width W4 between 3 and 10 micrometers or between 10 and 30 micrometers, and a height between 1 and 100 micrometers, and preferably between 2 and 30 micrometers.

[00710] Alternatively, another process for forming the via plugs 58 on the bulk metal layer 9 can be performed by the following steps. Referring to Fig. 27D, after the steps illustrated in Figs. 24B, 24C and 25A-25D, the photoresist layer 29 can be removed using an inorganic solution or using an organic solution with amide. After the photoresist layer 29 is removed, the previously described photoresist layer 51 having a thickness between 1 and 120 micrometers, and preferably between 5 and 50 micrometers, can be formed on the seed layer 4b of the metal layer 4 and on the topmost layer of copper, gold, aluminum, nickel or

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palladium of the previously described various bulk metal layer 9 by a spin-on coating process, a lamination process, a screen-printing process or a spraying process. Next, the photoresist layer 51 is patterned with the processes of exposure and development to form the openings 51b in the photoresist layer 51 exposing the regions 9a of the topmost layer of copper, gold, aluminum, nickel or palladium of the previously described various bulk metal layer 9. The process of forming the photoresist layer 51 and the openings 51b in the photoresist layer 51 as shown in Fig. 27D can be referred to as the process of forming the photoresist layer 51 and the openings 51a in the photoresist layer 51 as illustrated in Fig. 26A.

[00711] Referring to Fig. 27E, after the step illustrated in Fig. 27D, the via plugs 58 illustrated in Fig. 27B are formed in the openings 51b and on the regions 9a of the topmost layer of copper, gold, aluminum, nickel or palladium of the previously described various bulk metal layer 9 exposed by the openings 51b. The process of forming the via plugs 58 in the openings 51b and on the regions 9a of the topmost layer of copper, gold, aluminum, nickel or palladium of the previously described various bulk metal layer 9 as shown in Fig. 27E can be referred to as the process of forming the via plugs 58 in the openings 51b and on the regions 9a of the topmost layer of copper, gold, aluminum, nickel or palladium of the previously described various bulk metal layer 9 exposed by the openings 51b as illustrated in Fig. 27B. The specification of the via plugs 58 shown in Fig. 27E can be referred to as the specification of the via plugs 58 illustrated in Fig. 27B. After forming the via plugs 58, the photoresist layer 51 is removed using an inorganic solution or using an organic solution with amide. Accordingly, the via plugs 58 can be formed on the bulk metal layer 9 after the photoresist layer 51 is removed.

[00712] Referring to Fig. 27F, after forming the via plugs 58 on the bulk metal layer 9, the metal layer 4 not under the bulk metal layer 9 is removed with an etching method. The process of removing the metal layer 4 not under the bulk metal layer 9 shown in Fig. 27F can be referred to as the process of removing the metal layer 4 not under the bulk metal layer 9 as illustrated in Fig. 25F. Accordingly, multiple interconnecting structures 88 provided by the metal layer 4 and the bulk metal layer 9 can be formed in the thinned silicon substrate 1 and at the backside 1a of the thinned silicon substrate 1, and sidewalls of the bulk metal layer 9 are not covered by the metal layer 4. The interconnecting structures 88 can connect the off-chip buffer 42 to the internal circuits 21, 22, 23 and 24 and connect the off-chip buffer 42 to the via plug 58.

[00713] Next, referring to Fig. 27G, a polymer layer 142 can be formed on the insulating layer 3, on the via plugs 58 and on the bulk metal layer 9, enclosing the via plugs 58 and the bulk metal layer 9, by a spin-on coating process, a lamination process or a screen-printing process. The polymer layer 142 has a thickness t6 between 10 and 200 micrometers, and preferably between 15 and 50 micrometers. The material of the polymer layer 142 may include benzocyclobutane (BCB), polyimide (PI), polybenzoxazole (PBO) or epoxy resin.

[00714] For example, the polymer layer 142 can be formed by a suitable process or processes, e.g., by spin-on coating a negative-type photosensitive polyimide layer, containing ester-type precursor, having a thickness between 20 and 400 micrometers, and preferably between 30 and 100 micrometers on the insulating layer 3, on the via plugs 58 and on the bulk metal layer 9, then baking the spin-on coated polyimide layer, and then curing or heating the baked polyimide layer at a temperature between 180 and 400°C, between 180 and 250°C, between 250 and 290°C, between 290 and 400°C or between 200 and 390°C for a time between 20 and 150 minutes in a nitrogen ambient or in an oxygen-free ambient, the cured polyimide layer having a thickness between 10 and 200 micrometers, and preferably between 15 and 50 micrometers. By the way, the polymer layer 142 can be formed on the insulating layer 3, on the via plugs 58 and on the bulk metal layer 9, and encloses the via plugs 58 and the bulk metal layer 9.

[00715] Referring to Fig. 27H, after forming the polymer layer 142, a polishing or mechanical polishing process, and preferably a chemical-mechanical polishing (CMP) process, is used to planarize the surface of the polymer layer 142, exposing the via plugs 58. The polymer layer 142, after being planarized, may have a thickness t7 between 7 and 80 micrometers, and preferably between 10 and 30 micrometers. The top surfaces 58a of the via plugs 58 can be substantially coplanar with the top surface 142a of the polymer layer 142.

[00716] Next, referring to Fig. 27I, an adhesion/barrier layer 64 having a thickness smaller than 1 micrometer, such as between 0.02 and 0.5 micrometers, and preferably between 0.1 and 0.2 micrometers, can be formed on the top surface 142a of the polymer layer 142 and on the top surfaces 58a of the via plugs 58 by a physical vapor deposition (PVD) process, such as sputtering process or evaporation process, and then a seed layer 65 having a thickness smaller than 1 micrometer, such as between 0.05 and 0.5 micrometers, and preferably between 0.08 and 0.15 micrometers, can be formed on the adhesion/barrier layer 64 by a physical vapor deposition (PVD) process, such as sputtering process or evaporation process. The material of

the adhesion/barrier layer 64 may include titanium, a titanium-tungsten alloy, titanium nitride, chromium, tantalum, tantalum nitride or a composite of the previously described materials, and the material of the seed layer 65 may include copper, nickel, aluminum, gold, silver, platinum or palladium.

[00717] For example, when the adhesion/barrier layer 64 is formed by a suitable process or processes, e.g., by sputtering a titanium-containing layer, such as a single layer of titanium-tungsten alloy, titanium or titanium nitride, having a thickness smaller than 1 micrometer, such as between 0.02 and 0.5 micrometers, and preferably between 0.1 and 0.2 micrometers, on the top surface 142a of the polymer layer 142 and on the top surfaces 58a of the via plugs 58, the seed layer 65 can be formed by a suitable process or processes, e.g., by sputtering a copper layer, a nickel layer, an aluminum layer, a gold layer, a silver layer, a platinum layer or a palladium layer with a thickness smaller than 1 micrometer, such as between 0.05 and 0.5 micrometers, between 0.08 and 0.15 micrometers, between 0.1 and 1 micrometers or between 0.2 and 0.5 micrometers, on the titanium-containing layer.

[00718] Alternatively, when the adhesion/barrier layer 64 is formed by a suitable process or processes, e.g., by sputtering a composite layer including a titanium layer having a thickness between 0.01 and 0.15 micrometers on the top surface 142a of the polymer layer 142 and on the top surfaces 58a of the via plugs 58 and a titanium-tungsten-alloy layer having a thickness between 0.1 and 0.35 micrometers on the titanium layer, the seed layer 65 can be formed by a suitable process or processes, e.g., by sputtering a copper layer, a nickel layer, an aluminum layer, a gold layer, a silver layer, a platinum layer or a palladium layer with a thickness smaller than 1 micrometer, such as between 0.05 and 0.5 micrometers, between 0.08 and 0.15 micrometers, between 0.1 and 1 micrometers or between 0.2 and 0.5 micrometers, on the titanium-tungsten-alloy layer.

[00719] Alternatively, when the adhesion/barrier layer 64 is formed by a suitable process or processes, e.g., by sputtering a tantalum-containing layer, such as a single layer of tantalum or tantalum nitride, having a thickness smaller than 1 micrometer, such as between 0.02 and 0.5 micrometers, and preferably between 0.1 and 0.2 micrometers, on the top surface 142a of the polymer layer 142 and on the top surfaces 58a of the via plugs 58, the seed layer 65 can be formed by a suitable process or processes, e.g., by sputtering a copper layer, a nickel layer, an aluminum layer, a gold layer, a silver layer, a platinum layer or a palladium layer with a thickness smaller than 1 micrometer, such as between 0.05 and 0.5 micrometers, between 0.08

and 0.15 micrometers, between 0.1 and 1 micrometers or between 0.2 and 0.5 micrometers, on the tantalum-containing layer.

[00720] Alternatively, when the adhesion/barrier layer 64 is formed by a suitable process or processes, e.g., by sputtering a chromium-containing layer, such as a single layer of chromium layer, having a thickness smaller than 1 micrometer, such as between 0.02 and 0.5 micrometers, and preferably between 0.1 and 0.2 micrometers, on the top surface 142a of the polymer layer 142 and on the top surfaces 58a of the via plugs 58, the seed layer 65 can be formed by a suitable process or processes, e.g., by sputtering a copper layer, a nickel layer, an aluminum layer, a gold layer, a silver layer, a platinum layer or a palladium layer with a thickness smaller than 1 micrometer, such as between 0.05 and 0.5 micrometers, between 0.08 and 0.15 micrometers, between 0.1 and 1 micrometers or between 0.2 and 0.5 micrometers, on the chromium-containing layer.

[00721] Referring to Fig. 27J, after forming the seed layer 65, a photoresist layer 67, such as positive-type photoresist layer or negtive-type photoresist layer, having a thickness larger than 1 micrometer, such as between 5 and 50 micrometers, and preferably between 10 and 25 micrometers, is formed on the seed layer 65 of any previously described material by a spin-on coating process, a lamination process, a screen-printing process or a spraying process. Next, the photoresist layer 67 is patterned with the processes of exposure and development to form multiple openings 67a in the photoresist layer 67 exposing the seed layer 65 of any previously described material. A 1X stepper or 1X contact aligner can be used to expose the photoresist layer 67 during the process of exposure.

[00722] For example, the photoresist layer 67 can be formed by a suitable process or processes, e.g., by spin-on coating a positive-type photosensitive polymer layer having a thickness between 5 and 50 micrometers, and preferably between 10 and 25 micrometers, on the seed layer 65, then exposing the photosensitive polymer layer using a 1X stepper or a contact aligner with at least two of G-line, H-line and I-line, and G-line has a wavelength ranging from, e.g., about 434 to 438nm, H-line has a wavelength ranging from, e.g., about 403 to 407nm, and I-line has a wavelength ranging from, e.g., about 363 to 367nm, then developing the exposed polymer layer by spraying and puddling a developer on the semiconductor wafer 10 or by immersing the semiconductor wafer 10 into a developer, and then cleaning the semiconductor wafer 10 using deionized wafer and drying the semiconductor wafer 10 by spinning the semiconductor wafer 10. After development, a scum removal process of removing

the residual polymeric material or other contaminants from the seed layer 65 may be conducted by using an O_2 plasma or a plasma containing fluorine of below 200PPM and oxygen. By these processes, the photoresist layer 67 can be patterned with the openings 67a exposing the seed layer 65.

[00723] Next, referring to Fig. 27K, a metal layer 68 having a thickness larger than 1 micrometer, such as between 1 and 50 micrometers, and preferably between 2 and 20 micrometers, can be electroplated in the openings 67a and on the seed layer 65 of any previously described material exposed by the openings 67a. The metal layer 68 may be a single layer of gold, copper, silver, palladium, platinum, rhodium, ruthenium, rhenium or nickel, or a composite layer made of the previously described metals.

[00724] For example, the metal layer 68 can be composed of a single metal layer formed by a suitable process or processes, e.g., by electroplating a gold layer, to a thickness between 1 and 50 micrometers, and preferably between 2 and 20 micrometers, in the openings 67a and on the seed layer 65, preferably the previously described gold layer 65, exposed by the openings 67a using the previously described electroplating solution for electroplating gold of the bulk metal layer 9.

[00725] Alternatively, the metal layer 68 can be composed of a single metal layer formed by a suitable process or processes, e.g., by electroplating a copper layer, to a thickness between 1 and 50 micrometers, and preferably between 2 and 20 micrometers, in the openings 67a and on the seed layer 65, preferably the previously described copper layer 65, exposed by the openings 67a using the previously described electroplating solution for electroplating copper of the bulk metal layer 9.

[00726] Alternatively, the metal layer 68 can be composed of a single metal layer formed by a suitable process or processes, e.g., by electroplating a palladium layer, to a thickness between 1 and 50 micrometers, and preferably between 2 and 20 micrometers, in the openings 67a and on the seed layer 65, preferably the previously described palladium layer 65, exposed by the openings 67a using the previously described electroplating solution for electroplating palladium of the bulk metal layer 9.

[00727] Alternatively, the metal layer 68 can be composed of a single metal layer formed by a suitable process or processes, e.g., by electroplating a nickel layer, to a thickness between 1 and 50 micrometers, and preferably between 2 and 20 micrometers, in the openings 67a and on the seed layer 65, preferably the previously described copper layer or nickel layer

65, exposed by the openings 67a using the previously described electroplating solution for electroplating nickel of the bulk metal layer 9.

[00728] Alternatively, the metal layer 68 can be composed of double metal layers formed by a suitable process or processes, e.g., by electroplating a copper layer, to a thickness between 1 and 50 micrometers, and preferably between 2 and 15 micrometers, in the openings 67a and on the seed layer 65, preferably the previously described copper layer 65, exposed by the openings 67a using the previously described electroplating solution for electroplating copper of the bulk metal layer 9, and then electroplating or electroless plating a gold layer, to a thickness between 0.005 and 10 micrometers, and preferably between 0.05 and 1 micrometers, in the openings 67a and on the electroplated copper layer in the openings 67a using the previously described electroplating or electroless plating solution for electroplating or electroless plating gold of the bulk metal layer 9.

[00729] Alternatively, the metal layer 68 can be composed of double metal layers formed by a suitable process or processes, e.g., by electroplating a copper layer, to a thickness between 1 and 50 micrometers, and preferably between 2 and 15 micrometers, in the openings 67a and on the seed layer 65, preferably the previously described copper layer 65, exposed by the openings 67a using the previously described electroplating solution for electroplating copper of the bulk metal layer 9, and then electroplating or electroless plating a palladium layer, to a thickness between 0.005 and 10 micrometers, and preferably between 0.05 and 1 micrometers, in the openings 67a and on the electroplated copper layer in the openings 67a using the previously described electroplating or electroless plating solution for electroplating or electroless plating palladium of the bulk metal layer 9.

[00730] Alternatively, the metal layer 68 can be composed of double metal layers formed by a suitable process or processes, e.g., by electroplating a copper layer, to a thickness between 1 and 50 micrometers, and preferably between 2 and 15 micrometers, on the seed layer 65, preferably the previously described copper layer 65, exposed by the openings 67a using the previously described electroplating solution for electroplating copper of the bulk metal layer 9, and then electroplating or electroless plating a nickel layer, to a thickness between 1 and 15 micrometers, and preferably between 2 and 5 micrometers, in the openings 67a and on the electroplated copper layer in the openings 67a using the previously described electroplating or electroless plating solution for electroplating or electroless plating nickel of the bulk metal layer 9.

[00731] Alternatively, the metal layer 68 can be composed of double metal layers formed by a suitable process or processes, e.g., by electroplating a nickel layer, to a thickness between 1 and 50 micrometers, and preferably between 2 and 15 micrometers, in the openings 67a and on the seed layer 65, preferably the previously described copper layer or nickel layer 65, exposed by the openings 67a using the previously described electroplating solution for electroplating nickel of the bulk metal layer 9, and then electroplating or electroless plating a gold layer or a palladium layer, to a thickness between 0.005 and 10 micrometers, and preferably between 0.05 and 1 micrometers, in the openings 67a and on the electroplated nickel layer in the openings 67a.

[00732] Alternatively, the metal layer 68 can be composed of triple metal layers formed by a suitable process or processes, e.g., by electroplating a copper layer, to a thickness between 1 and 50 micrometers, and preferably between 2 and 15 micrometers, on the seed layer 65, preferably the previously described copper layer 65, exposed by the openings 67a using the previously described electroplating solution for electroplating copper of the bulk metal layer 9, next electroplating or electroless plating a nickel layer, to a thickness between 1 and 15 micrometers, and preferably between 2 and 5 micrometers, in the openings 67a and on the electroplated copper layer in the openings 67a using the previously described electroplating or electroless plating solution for electroplating or electroless plating nickel of the bulk metal layer 9, and then electroplating or electroless plating a gold layer, to a thickness between 0.005 and 1 micrometers, and preferably between 0.05 and 0.1 micrometers, in the openings 67a and on the electroplated or electroless plated nickel layer in the openings 67a using the previously described electroplating or electroless plating solution for electroplating or electroless plating gold of the bulk metal layer 9.

[00733] Alternatively, the metal layer 68 can be composed of triple metal layers formed by a suitable process or processes, e.g., by electroplating a copper layer, to a thickness between 1 and 50 micrometers, and preferably between 2 and 15 micrometers, on the seed layer 65, preferably the previously described copper layer 65, exposed by the openings 67a using the previously described electroplating solution for electroplating copper of the bulk metal layer 9, next electroplating or electroless plating a nickel layer, to a thickness between 1 and 15 micrometers, and preferably between 2 and 5 micrometers, in the openings 67a and on the electroplated copper layer in the openings 67a using the previously described electroplating or electroless plating solution for electroplating or electroless plating nickel of the bulk metal layer 9, and then electroplating or electroless plating a palladium layer, to a thickness between

0.005 and 1 micrometers, and preferably between 0.05 and 0.1 micrometers, in the openings 67a and on the electroplated or electroless plated nickel layer in the openings 67a using the previously described electroplating or electroless plating solution for electroplating or electroless plating palladium of the bulk metal layer 9.

[00734] Referring to Fig. 27L, after forming the metal layer 68, the photoresist layer 67 can be removed using an inorganic solution or using an organic solution with amide. Some residuals from the photoresist layer 67 could remain on the metal layer 68 and on the seed layer 65 not under the metal layer 68. Thereafter, the residuals can be removed from the metal layer 68 and from the seed layer 65 with a plasma, such as an O_2 plasma or a plasma containing fluorine of below 200PPM and oxygen.

[00735] Next, referring to Fig. 27M, the seed layer 65 and the adhesion/barrier layer 64 not under the metal layer 68 are subsequently removed with an etching method. In a case, the seed layer 65 and the adhesion/barrier layer 65 not under the metal layer 68 can be subsequently removed by a dry etching method. As to the dry etching method, both the seed layer 65 and the adhesion/barrier layer 64 not under the metal layer 68 can be subsequently removed by an Ar sputtering etching process; alternatively, both the seed layer 65 and the adhesion/barrier layer 64 not under the metal layer 68 can be subsequently removed by a reactive ion etching (RIE) process; alternatively, the seed layer 65 not under the metal layer 68 can be removed by an Ar sputtering etching process, and then the adhesion/barrier layer 64 not under the metal layer 68 can be removed by a reactive ion etching (RIE) process. In another case, the seed layer 65 and the adhesion/barrier layer 64 not under the metal layer 68 can be subsequently removed by a wet etching method. As to the wet etching method, when the seed layer 65 is a copper layer, it can be etched with a solution containing NH_4OH or with a solution containing H_2SO_4; when the adhesion/barrier layer 64 is a titanium-tungsten-alloy layer, it can be etched with a solution containing hydrogen peroxide or with a solution containing NH_4OH and hydrogen peroxide; when the adhesion/barrier layer 64 is a titanium layer, it can be etched with a solution containing hydrogen fluoride or with a solution containing NH_4OH and hydrogen peroxide; when the adhesion/barrier layer 64 is a chromium layer, it can be etched with a solution containing potassium ferricyanide. In another case, the seed layer 65, such as copper, not under the metal layer 68 can be removed by a solution containing NH_4OH or a solution containing H_2SO_4, and then the adhesion/barrier layer 64 not under the metal layer 68 can be removed by a reactive ion etching (RIE) process. In another case, the seed layer 65, such as copper, not under the metal layer 68 can be removed by a solution containing NH_4OH

or a solution containing H_2SO_4, and then the adhesion/barrier layer 64 not under the metal layer 68 can be removed by an Ar sputtering etching process.

[00736] Next, referring to Fig. 27N, a polymer layer 14 can be formed on the top surface 142a of the polymer layer 142 and on the topmost layer of gold, copper, nickel or palladium of the previously described various metal layer 68 by a process including a spin-on coating process, a lamination process, a screen-printing process or a spraying process and including a curing process, and multiple openings 14a in the polymer layer 14 are over multiple regions of the topmost layer of gold, copper, nickel or palladium of the previously described various metal layer 68 and expose them. The polymer layer 14 has a thickness larger than 2 micrometers, such as between 3 and 50 micrometers, and preferably between 5 and 25 micrometers. The material of the polymer layer 14 may include benzocyclobutane (BCB), polyimide (PI), polybenzoxazole (PBO) or epoxy resin.

[00737] In a case, the polymer layer 14 can be formed by a suitable process or processes, e.g., by spin-on coating a negative-type photosensitive polyimide layer having a thickness between 6 and 100 micrometers on the top surface 142a of the polymer layer 142 and on the topmost layer of gold, copper, nickel or palladium of the previously described various metal layer 68, then baking the spin-on coated polyimide layer, then exposing the baked polyimide layer using a 1X stepper or a 1X contact aligner with at least two of G-line having a wavelength ranging from, e.g., about 434 to 438nm, H-line having a wavelength ranging from, e.g., about 403 to 407nm, and I-line having a wavelength ranging from, e.g., about 363 to 367nm, illuminating the baked polyimide layer, that is, G-line and H-line, G-line and I-line, H-line and I-line, or G-line, H-line and I-line illuminate the baked polyimide layer, then developing the exposed polyimide layer to form multiple openings exposing the metal layer 68, then curing or heating the developed polyimide layer at a temperature between 180 and 400°C, between 180 and 250°C, between 250 and 290°C, between 290 and 400°C or between 200 and 390°C for a time between 20 and 150 minutes in a nitrogen ambient or in an oxygen-free ambient, the cured polyimide layer having a thickness between 3 and 50 micrometers, and then removing the residual polymeric material or other contaminants from the metal layer 68 exposed by the openings 14a with an O_2 plasma or a plasma containing fluorine of below 200PPM and oxygen. By the way, the polymer layer 14 can be formed on the top surface 142a of the polymer layer 142 and on the topmost layer of gold, copper, nickel or palladium of the previously described various metal layer 68, and the openings 14a formed in the polymer layer

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14 expose the regions of the topmost layer of gold, copper, nickel or palladium of the previously described various metal layer 68.

[00738] In another case, the polymer layer 14 can be formed by a suitable process or processes, e.g., by spin-on coating a positive-type photosensitive polybenzoxazole layer having a thickness between 3 and 50 micrometers on the top surface 142a of the polymer layer 142 and on the topmost layer of gold, copper, nickel or palladium of the previously described various metal layer 68, then baking the spin-on coated polybenzoxazole layer, then exposing the baked polybenzoxazole layer using a 1X stepper or a 1X contact aligner with at least two of G-line having a wavelength ranging from, e.g., about 434 to 438nm, H-line having a wavelength ranging from, e.g., about 403 to 407nm, and I-line having a wavelength ranging from, e.g., about 363 to 367nm, illuminating the baked polybenzoxazole layer, that is, G-line and H-line, G-line and I-line, H-line and I-line, or G-line, H-line and I-line illuminate the baked polybenzoxazole layer, then developing the exposed polybenzoxazole layer to multiple openings exposing the metal layer 68, then curing or heating the developed polybenzoxazole layer at a temperature between 150 and 250°C, and preferably between 180 and 250°C, or between 200 and 400°C, and preferably between 250 and 350°C, for a time between 5 and 180 minutes, and preferably between 30 and 120 minutes, in a nitrogen ambient or in an oxygen-free ambient, the cured polybenzoxazole layer having a thickness between 3 and 50 micrometers, and then removing the residual polymeric material or other contaminants from the metal layer 68 exposed by the openings 14a with an O_2 plasma or a plasma containing fluorine of below 200PPM and oxygen. By the way, the polymer layer 14 can be formed on the top surface 142a of the polymer layer 142 and on the topmost layer of gold, copper, nickel or palladium of the previously described various metal layer 68, and the openings 14a formed in the polymer layer 14 expose the regions of the topmost layer of gold, copper, nickel or palladium of the previously described various metal layer 68.

[00739] Next, referring to Fig. 27O, an adhesion/barrier layer 16 having a thickness smaller than 1 micrometer, such as between 0.02 and 0.5 micrometers, and preferably between 0.1 and 0.2 micrometers, can be formed on the polymer layer 14 and on the regions of the topmost layer of gold, copper, nickel or palladium of the previously described various metal layer 68 exposed by the openings 14a by using a physical vapor deposition (PVD) process, such as sputtering process or evaporation process, and then a seed layer 18 having a thickness smaller than 1 micrometer, such as between 0.05 and 0.5 micrometers, and preferably between 0.08 and 0.15 micrometers, can be formed on the adhesion/barrier layer 16 by using a physical