Fast Acquisition Scheme and Implementation of PRACH in WCDMA System

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Abstract: The performance and implementation of PRACH(physical random access channel) acquisition in WCDMA system is investigated in this paper. The analysis shows that the conventional methods are not satisfying. Thus we proposed the quasi-matched filter acquisition scheme of PRACH preamble which based on fast Hadamard transform. And we implement this method by hard ware in the practical WCDMA field try system. The simulation and test results show that the proposed scheme achieves the following performance: the detection probability with E_b/N_0 =7db does not less than 95%, and the mean acquisition time is less than 1.33ms.

I. INTRODUCTION

Pesudo-noise(PN) code acquisition is the first action of any direct-sequence code division multiple access(DS-CDMA) system. Acquisition refers to the coarse synchronization of the received PN sequence and the locally generated PN sequence within a fraction of the chip duration of the code sequence. Fast and effective acquisition is one of the key techniques in CDMA communication system. And the acquisition performance can even be a limitation of the capacity of a system (acquisition-based capacity)[1].

Acquisition can be performed and classified in several ways[2-3]. One way to separate acquisition methods is based on correlation measurement principle, which is used, active or passive measurement or a combination of the two[4]. In the passive method, a filter matched to the spreading code is used. But in the active method, the received signal is multiplied with the locally generated replica of the spreading code, and the result is integrated over some observation interval. The multiplication and integration is performed step-by-step for each code phases to be tested. Usually, serial、complete parallel、store parallel and hybrid parallel search[5-7] approach can be used for the detection of the code phases to be tested. However, serial search with correlation integration method seldom used for fast acquisition.

In WCDMA systems, the physical random access channel (PRACH) has one or more preambles and each preamble is only 4096 chips. The single acquisition time is limited in 5120chips. Thus, there is high requirement for fast acquisition of RACH preamble. At the same time, there are a total of 16 signatures of RACH preamble part. This further increases the difficulty of the acquisition scheme. In addition, there need two sets of identical acquisition device for I/Q branches. Thus, the acquisition efficiency must be compare to the match filter.

Based on above discussion and aiming at to achieve good performance and reduce the hardware resource at the same time, we propose a novel acquisition scheme. The simulation and test results show that the proposed scheme can be easy implement in practical WCDMA field try system and achieve high performance.

II. WCDMA PRACH DESCRIPTION

In WCDMA system, the random-access transmission is based on a Slotted ALOHA approach with fast acquisition indication. There are 15 access slots per two physical frames and they are spaced 5120 chips apart. See reference[8]. The structure of the random-access transmission is also shown in reference[8]. The random-access transmission consists of one or several *preambles* of length 4096 chips and a *message* of length 10 ms or 20 ms. Each preamble is of length 4096 chips and consists of 256 repetitions of a signature of length 16 chips. There are maximum 16 available signatures. The baseband modulator for RACH is illustrated as figure 1. The binary preamble $a(k)$ is modulated to get the complex valued preamble $b(k)$.

$$b(k) = a(k)e^{j\left(\frac{\pi}{4}+\frac{\pi}{2}k\right)}, k = 0,1,2,...,4095 \qquad (1)$$

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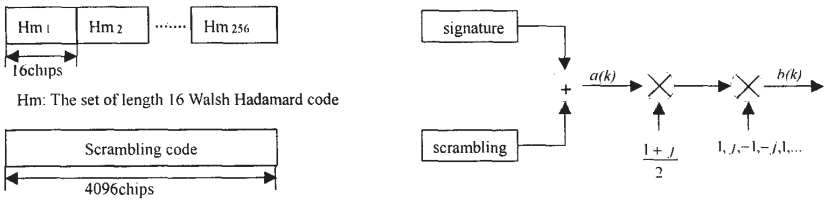


Fig.1 Structure of preamble & scrambling code and baseband modulator for RACH preamble

III. Quasi-Matched Filter Scheme Based on Fast Hadamard Transform

At the bsae station, the code phase of the preamble is retarded by a roundtrip delay compared with that of the pilot signal[8]. Hera we assume that the code phase which need to be tested equals 400(200chips). We also assume that the correlation period is 1024 chips. In this case, the serial search method is not suitable distinctly. If the hybrid parallel[7] acquisition approach is adopted here. To limit the acquisition time within 5120chips, we appoximately assume that the 400 phase to be tested is divided into 14 sub-phase intervals. Thus, it should finish the search of $400/30 \approx 14$ unknown phase within each sub-phase interval. For 16 signatures and I/Q branches, the total parallel correlators needed to detect the unknown phase are $16 \times 2 \times 30 = 960$. It is impractical for implementation of such huge correlator arrays. If conventional match filters method[9] is used for PRACH, there need two sets of 16 match filters for I/Q branches of 16 signatures. As we know, a digital match filter actually is a multi-stage parallel accumulator. And the number of accumulators relate to correlation length. At the correlation period is 1024chips, it needs 1023 accumulators to implement such a match filter. It is disastrous for system resource to implement this method (total $16 \times 2 \times 1023 = 32700$ accumlators).

Based on the above discussion and the property of PRACH, we propose the following new acquisition detector structure.

From figure 1, we can find that the preamble is generated by a signature consists of 256 repetitions of a length 16 signature and scrambling code. The signature is from the set of 16 Hadamard codes of length 16. For the same cell, the scrambling code of all mobile terminals used is the same. Thus, fast Hadamard transform (FHT) can be used to do the correlation of the preamble. The acquisition time when using FHT can be shortened. Furthermore, FHT can be implemented by original position operation and this cannot expend too much hardware resource. FHT is only change the modality of correlation operation, the conventional structure of the acquisition system can still be used.

Here we propose the acquisition system of quasi-matched filter scheme based on the FHT. It is shown as figure 2. According to the figure 1, a non-coherent QPSK detector is used for for each FHT branch. The acquisition system consists of two sets of L(16) FHT which corresponding to the 16 signatures for each I/Q branches and a maximum selection unit and a threshold comparing part. If the maximum correlation value $Z_{\max}$ is larger than the threshold, then the corresponding phase is considered as correct phase and the system turns into tracking state. Otherwise, it goes back to the state of searching another unknown phase. The threshold setting principles we used here is Neyman-Pearson criterion. That is at the condition of constant false alarm rate(CFAR), to maximize the detection probability[5,9].

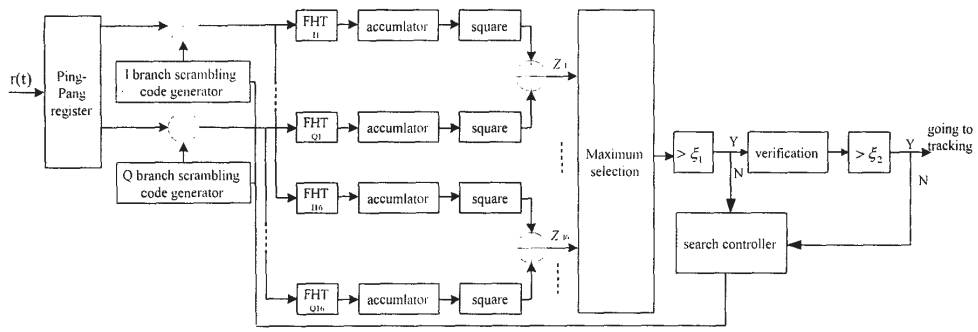


Fig. 2 a non-coherent QPSK acquisition system based on the FHT

In figure 2, r(t) is the received baseband signal in base station. ξ_1 is the threshold set for the search mode and ξ_2 is the threshold set for the verification mode.

In practical system, the scrambling code is put into memory. The input data stream is first put into the register and the size of the register is chosen as two times as the correlation length. Thus, the ping-pang operation can be done. Every time 16chips data is read out and scrambling code is de-spreaded. Then the results will be fed into FHT and accumulator. Finally the corresponding results of I/Q branches are squared and summed. The decision variable can be obtained.

For one FHT, 4 accumlators are needed. To complte the detection of 400 phase to be tested, the hybrid parallel[7] acquisition approach is also adopted here and the 400 phase to be tested is divided into 200 sub-phase intervals. Thus, it should finish the search of 400/200=2 unknown phase within each sub-phase interval. Thus, for this system, there are total $(16\times4+16)\times2\times2=320$ accumlators. This is much less than that used in MF method and conventional hybird parallel method. Hadamard sequence used here is only 16 chips, the original position operation doesn't need. We can use streamline structure to do this operation and the acquisition time can be further shortened. This streamline structure just is a match filter for the Hadamard sequence with length of 16 chips. In practical implementation, To increase the process gain, the correlation length should greater than 16chips. It can select as N times of 16chips and N is an integer. The desired correlation result is the accumulation of N consecutive output value of the match filter. Here we choose N as 64 and such selection can guarantee the required performance.

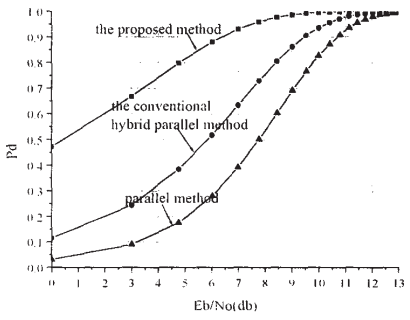
IV. Performance analysis and simulation results

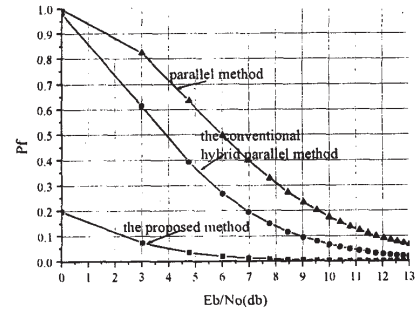
Based on the above discription, we do the simulation on mean acquisition time and detection probability. The simulation parameters are listed in table1. The correlation length is set as 1024 chips. The penalty factor for the false alarm is selected as two, i.e., the penalty time is 2T s. The threshold parameters ξ_1 and ξ_2 are adjust to meet the detection probability and minimum mean acquisition time requirements. The another two parameters of the verification mode are quoted from [10]. In the conventional hybrid parallel method, the parallel branch is set as 100. And in each parallel branch, there are 4 phase to be tested.

Table 1 parameters used for simulation

Chip rate	3.84Mcps
Threshold set method	CFAR
Multipath model	ETSI vehicular A[11]
Multipath fading	Rayleigh

The simulation results are as follows.





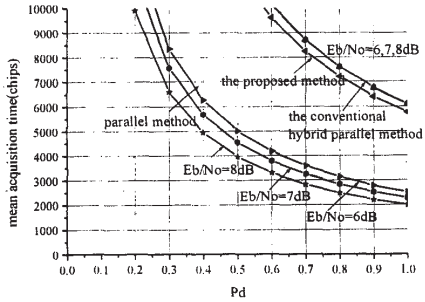
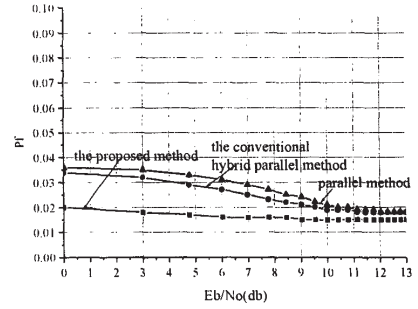


Fig.3 performance of single dwell mode



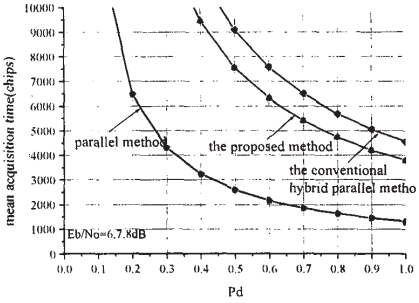
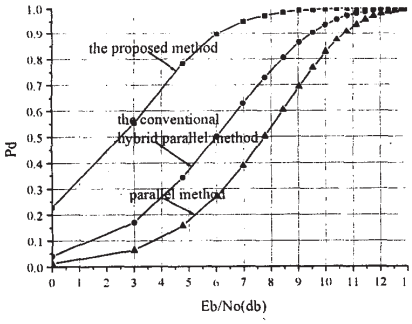


Fig.4 performance of double dwell mode

We can see from fig.1 that the detection probability(Pd) will increase and the false-alarm probability(Pf) decrease with the inceraseing of signal to noise ratio.

We can see from fig.3 and fig.4 that when the double dwell search method is used, a relatively low threshold ξ_1 can be used to increase the detection probability, and the verification mode operation can reduce the probability of a false-alarm event; therefore, the mean acquisition time can be greatly reduced.



V. Hard ware implementation and performance results

We use Alter FPGA 20K200EFC-3 to evaluate the hardware scale of the PRACH acquisition system. Total 11740 logic cells and 142336ESB are used. The diagram for the FPGA implementation is shown in figure 5.

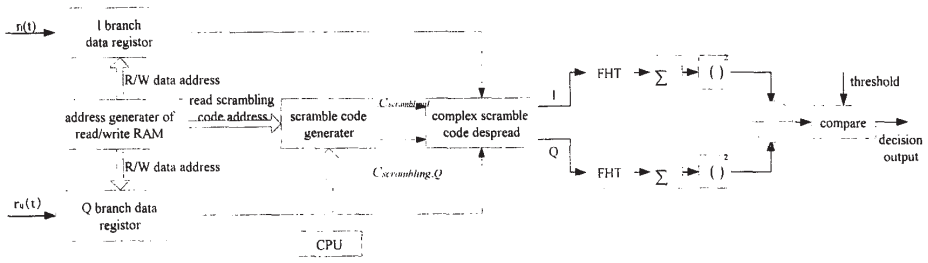


Fig.5 the hardware structure of PRACH acquisition scheme

One of the branches of the process of PRACH acquisition is described above. It's hardware implementation structure mainly contains the following modules.

1. DATA_REGISTER

This module receives signal from A/D, and put the data into register. The size of the register is two times as correlation length. This unit is the main limitation for FPGA resource.

2. ADDRESS_GENERATOR

This module generates the R/W(read/write) address for both I and Q branches data registers. It also generates the read address of scrambling code generator.

3. SCRAMBING _CODE GENERATER

This module generates the scramble code that is used for current cell according to initial state that CPU informs.

4. COMPLEX SCRAMBLE _CODE DESPRADING

The complex scramble code is de-spread in this module. The scramble code multiples the input data step-by-step and the results are output.

5. FHT

The multiple results of I/Q branches come from COMPLEX SCRAMBING_CODE DESPRADING module are separate fed into FHT modules. 16 parallel chips are needed for FHT. Each FHT unit has four accumulators with the bit width 10, 11,12 and 13. The streamline operation is used here.

6. ACCUMULATOR

To obtain the high process gain, we accumulate the FHT output 32 time in ACCUMULATOR module.

7. SQUARE

Then accumulator values from I/Q branches are summed in this module.

8. COMPARE

The last module is COMPARE. The correlation results of 16 signature are compared with the threshold that is set by higher layer successively. And the decision variable is obtained finally.

VI. Conclusion

In this paper, we have investigated the PRACH acquisition of WCDMA. Considering both acquisition performance and hardware scale, we proposed the novel fast acquisition scheme that based on FHT. The simulation ant test results are that the correct detection probability with E_b/N_0 =7dB doesn't less than 95% and the single acquisition time is less than 5120chips.

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