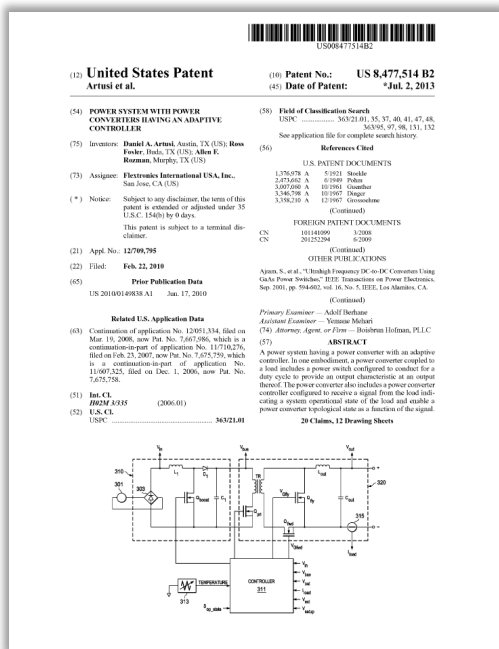


U.S. Patent No. 8,477,514 – Dell LA90PM170



Title: POWER SYSTEM WITH POWER CONVERTERS HAVING AN ADAPTIVE CONTROLLER

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Inventors: Daniel A. Artusi; Ross Fosler; Allen F. Rozman

Claims: 6, 7, 8, 10



- All the claim elements identified herein are literally and equivalently present in the Accused Instrumentalities.
- For clarity, the portion of a cited reference that is relied upon for support may also be reproduced in the chart. Also, earlier, later or otherwise different versions of the reference may be available but not specifically cited.
- The portion of the Accused Instrumentality covered by a claim element is typically identified by an arrow and/or outlined in color. Such identification is exemplary, not exclusive or exhaustive. The Asserted Claims are open ended, close ended or improperly restricted. Additional portions of the Accused Instrumentality might also be covered by the claim element but might not be identified in the chart.
- All quantitative figures, qualitative figures and data cited in the chart are subject to measurement and/or computational variation.

Claim 6

A **(SYS) power system**, comprising:

a **(PSC) power system controller** configured to provide a **(COM) signal** characterizing a **(PREQ) power requirement** of a **(PRO) processor system**; and

a **(PC) power converter** coupled to said **(PRO) processor system**, comprising:

a **(PS) power switch** configured to conduct for a **(DC) duty cycle** to provide an **(OC) output characteristic** and an **(OUT) output** thereof, and

a **(CON) power converter controller** configured to receive a **(COM) signal** from said **(PSC) power system controller** to control an **(IOC) internal operating characteristic** of said **(PC) power converter** as a function of said **(COM) signal**.

Claim 7

The **(SYS) power system** as recited in claim 6 wherein

said **(CON) power converter controller** is further configured to provide another **(OS) signal** to control said **(DC) duty cycle** of said **(PS) power switch** as a function of said **(OC) output characteristic** and in accordance with said **(COM) signal**.

Claim 8

The **(SYS) power system** as recited in claim 6 wherein said **(CON) power converter controller** is configured to adjust said **(IOC) internal operating characteristic** over a **(TTIM) period of time**.

Claim 10

The **(SYS) power system** as recited in claim 6 wherein said **(IOC) internal operating characteristic** is selected from the group consisting of:

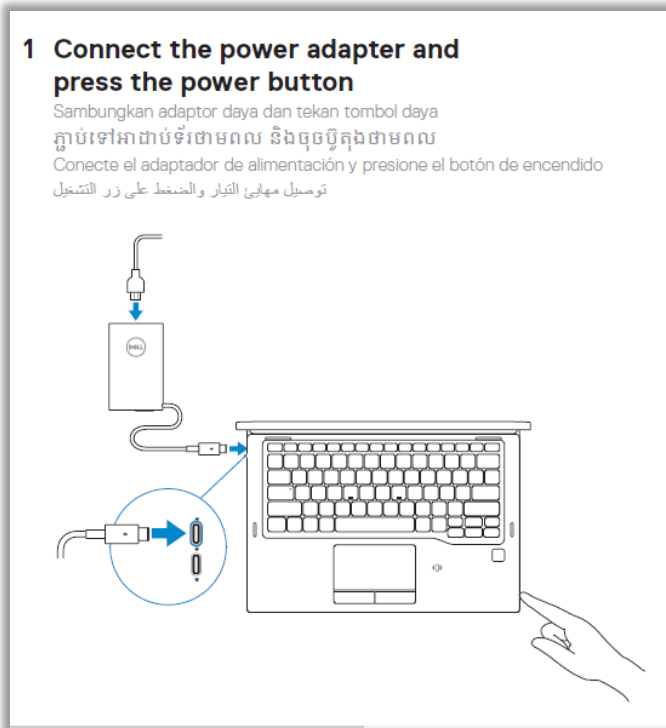
a **(GDV) gate drive voltage level** of said **(PS) power switch** of said **(PC) power converter**,

a switching frequency of said **(PC) power converter**, and

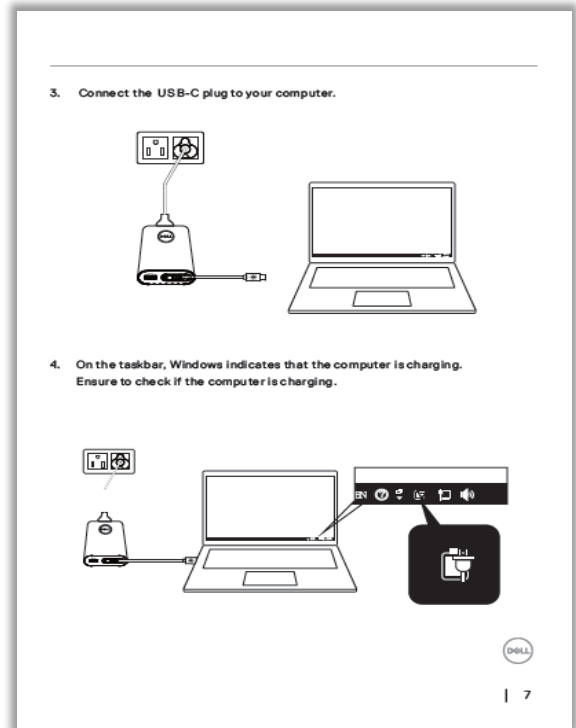
an **(DCBV) internal direct current bus voltage** of said **(PC) power converter**.

Claim 6

A (SYS) power system, comprising:



Dell Inc., Quick Start Guide for Latitude 5289 2-in-1 at p. 1 (2016)

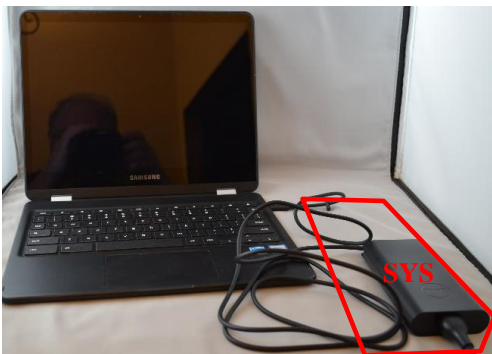
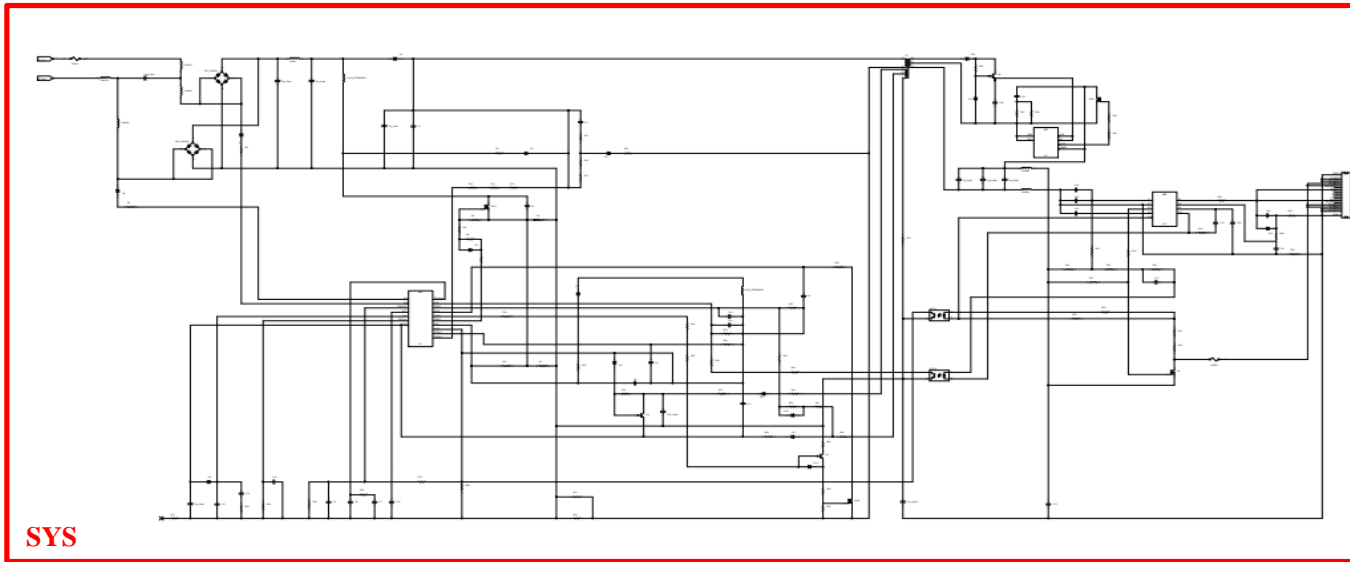


Dell Inc., User's Guide for Dell USB-C Power Adapter Plus-90W PA901C at p. 7 (2020)

These are typical examples of Dell generally instructing users of its power converters to couple them to loads.

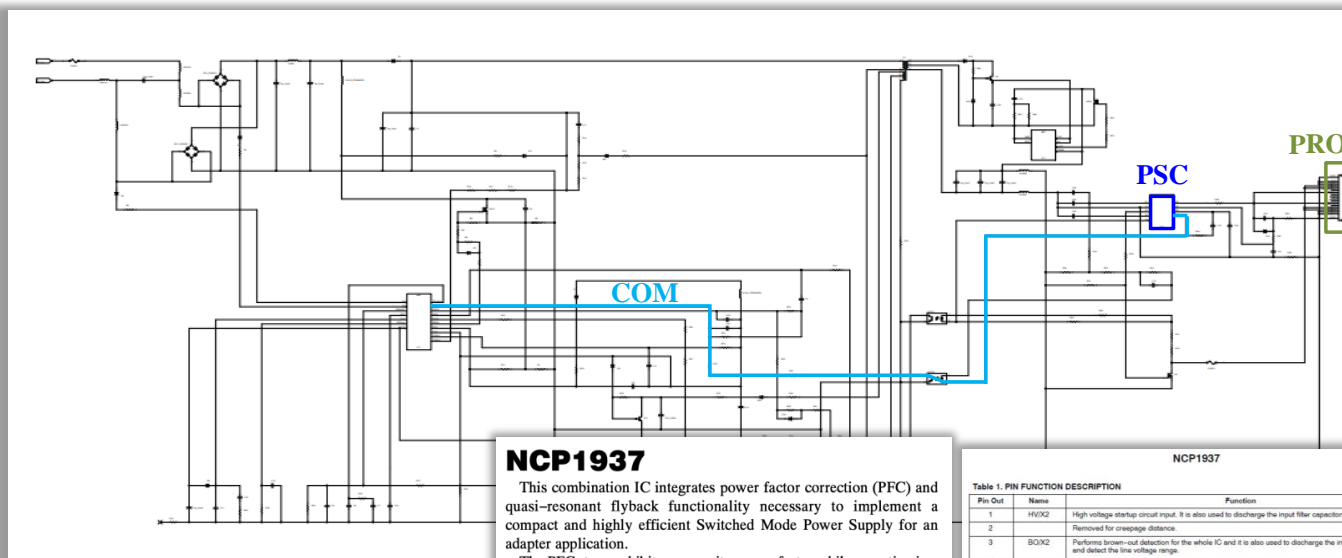
Claim 6

A (SYS) power system, comprising:



Claim 6

a (PSC) power system controller configured to provide a (COM) signal characterizing a (PREQ) power requirement of a (P) processor system; and



NCP1937

This combination IC integrates power factor correction (PFC) and quasi-resonant flyback functionality necessary to implement a compact and highly efficient Switched Mode Power Supply for an adapter application.

The PFC stage exhibits near-unity power factor while operating in a Critical Conduction Mode (CrM) with a maximum frequency clamp. The circuit incorporates all the features necessary for building a robust and compact PFC stage while minimizing the number of external components.

The quasi-resonant current-mode flyback stage features a proprietary valley-lockout circuitry, ensuring stable valley switching. This system works down to the 4th valley and toggles to a frequency foldback mode with a minimum frequency clamp beyond the 4th valley to eliminate audible noise. Skip mode operation allows excellent efficiency in light load conditions while consuming very low standby power consumption.

The supply capacitor provides power to the controller during power up. The capacitor must be sized such that a V_{CC} voltage greater than V_{CC(off)} is maintained while the auxiliary supply voltage is building up. Otherwise, V_{CC} will collapse and the controller will turn off. The operating IC bias current, I_{CC4}, and gate charge load at the drive outputs must be considered to correctly size C_{CC}. The increase in current consumption due to external gate charge is calculated using Equation 1.

Referring to Figure 4-7, a port that behaves as a Source has the following functional characteristics:

1. The Source uses a FET to enable/disable power delivery across V_{BUS} and initially the Source has V_{BUS} disabled.
2. The Source supplies pull-up resistors (R_p) on CC1 and CC2 and monitors both to detect a Sink. The presence of an R_d pull-down resistor on either pin indicates that a Sink is being attached. The value of R_p indicates the initial USB Type-C Current level supported by the host.
3. The Source uses the CC pin pull-down characteristic to detect and establish the correct routing for the SuperSpeed USB data path and determine which CC pin is intended for supplying V_{CONN}.
4. Once a Sink is detected, the Source enables V_{BUS} and V_{CONN}.
5. The Source can dynamically adjust the value of R_p to indicate a change in available USB Type-C Current to a Sink.

PREQ

Source(s): [1], [2]

Table 1. PIN FUNCTION DESCRIPTION

Pin Out	Name	Function
1	HVX2	High voltage startup circuit input. It is also used to discharge the input filter capacitors.
2		Removed for coverage distance.
3	BOX2	Performs brown-out detection for the whole IC and it is also used to discharge the input filter capacitors.
4		Removed for coverage distance.
5	PCntrol	Output of the PFC transconductance error amplifier. A compensation network is connected to this pin and ground to set the loop bandwidth.
6	PONOFF	A resistor between this pin and ground sets the PFC turn-off threshold. The voltage on this pin is pulled up to an internal voltage signal proportional to the output power. The PFC is disabled when the voltage on this pin falls below the threshold.
7	QCT	An external capacitor sets the frequency in VCO mode for the QR flyback controller.
8	Fault	The controller enters fault mode if the voltage of this pin is pulled above or below the precise pull-up current source allows direct interface with an NTC thermistor. Fault detection or auto-recovery depending on device option.
9	PSTmer	Power savings mode (PSM) control and timer adjust. Compatible with an optocoupler for PFC feedback. The device enters PSM if the voltage on this pin exceeds the PSM threshold. The device enters PSM if the voltage on this pin exceeds the PSM threshold. Once the controller enters power savings mode the IC is disabled and the current consumption is a maximum of 20µA. The input filter capacitor discharge function is available in power savings mode. The controller is enabled once V _{FB} drops below V _{FB,up} .
10	QFB	Feedback input for the QR Flyback controller. Allows direct connection to an optocoupler.
11	QZCD	Input to the demagnetization detection comparator for the QR Flyback controller. Also used for demagnetization.
12	VCC	Supply input.
13	QCS	Input to the cycle-by-cycle current limit comparator for the QR Flyback section.
14	QDRV	QR Flyback controller switch driver.
15	PDRV	PFC controller switch driver.
16	PCSPZCD	Input to the cycle-by-cycle current limit comparator for the PFC section. Also used for demagnetization detection for the PFC controller.
17	GND	Ground reference.
18	PFBV	Low voltage PFC feedback input. An external resistor divider is used to sense the PFC feedback. A high side resistor connects to this pin. This voltage is compared to an internal reference voltage of 2.5 V at low line and 4 V at high line. An internal high-voltage switch side resistor from the high side resistor chain when the PFC is disabled in order to reduce input power.
19		Removed for coverage distance.
20	PFBVH	High voltage PFC feedback input. An external resistor divider is used to sense the PFC feedback. A high side resistor connects to this pin. This voltage is compared to an internal reference voltage of 2.5 V at low line and 4 V at high line. An internal high-voltage switch side resistor from the high side resistor chain when the PFC is disabled in order to reduce input power.

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