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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/709,795	07/02/2013	8477514	CDW-011CP1CP1C1	7439

112093 7590 06/12/2013

Boisbrun Hofman, PLLC
12900 Preston Road
Suite 204
Dallas, TX 75230

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Daniel A. Artusi, Austin, TX;
Ross Fosler, Buda, TX;
Allen F. Rozman, Murphy, TX;

PTO/SB/08a (03-09)
Approved for use through 04/30/2009. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 2

Complete if Known	
Application Number	12/709,795
Filing Date	2/22/2010
First Named Inventor	Artusi et al.
Art Unit	2838
Examiner Name	Yemane Mehari
Attorney Docket Number	CDW-011CP1CP1C1

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number - Kind Code[2] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1.	US-3,602,795	08-31-1971	Gunn	
	2.	US-5,539,630	07-23-1996	Pietkiewicz et al.	
	3.	US-5,929,665	07-27-1999	Ichikawa et al.	
	4.	US-6,345,364 B1	02-05-2002	Lee	
	5.	US-6,548,992 B2	04-15-2003	Alcantar et al.	
	6.	US-6,580,627 B2	06-17-2003	~~Takahashi~~ Toshio	
	7.	US-6,614,206 B1	09-02-2003	Wong et al.	
	8.	US-6,668,296 B1	12-23-2003	Dougherty et al.	
	9.	US-2004-0200631 A1	10-14-2004	Chen	
	10.	US-6,813,170 B2	11-02-2004	Yang	
	11.	US-7,098,640 B2	08-29-2006	Brown	
	12.	US-2008-0205104 A1	08-28-2008	Lev et al.	
	13.	US-7,558,037 B1	07-07-2009	Gong et al.	
	14.	US-2009-0273957 A1	11-05-2009	Feldtkeller	
	15.	US-7,715,217 B2	05-11-2010	Manabe et al.	
	16.	US-7,733,679 B2	06-08-2010	Luger et al.	
	17.	US-7,746,041 B2	06-29-2010	Xu et al.	
	18.	US-7,940,035 B2	05-10-2011	Yang	
	19.	US-2012-0243271 A1	09-27-2012	Berghegger	

Change(s) applied to document, /C.H./ 6/6/2013

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] - Number[4] - Kind Code[5] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
	20.	CN201252294	06-03-2009	Jinfu Huang		

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1]Applicant's unique citation designation number (optional). [2]See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3]Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6]Applicant is to place a check mark here if English language Translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /Y.M./

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NOTICE OF ALLOWANCE AND FEE(S) DUE

25962 7590 03/05/2013

SLATER & MATSIL, L.L.P.
17950 PRESTON RD, SUITE 1000
DALLAS, TX 75252-5793

EXAMINER	
MEHARI, YEMANE	
ART UNIT	PAPER NUMBER
2838	

DATE MAILED: 03/05/2013

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/709,795	02/22/2010	Daniel A. Artusi	CDW-011CP1CP1C1	7439

TITLE OF INVENTION: POWER SYSTEM WITH POWER CONVERTERS HAVING AN ADAPTIVE CONTROLLER

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1770	$300	$0	$2070	06/05/2013

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 02/11)

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

25962 7590 03/05/2013
SLATER & MATSIL, L.L.P.
17950 PRESTON RD, SUITE 1000
DALLAS, TX 75252-5793

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/709,795	02/22/2010	Daniel A. Artusi	CDW-011CP1CP1C1	7439

TITLE OF INVENTION: POWER SYSTEM WITH POWER CONVERTERS HAVING AN ADAPTIVE CONTROLLER

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1770	$300	$0	$2070	06/05/2013

EXAMINER	ART UNIT	CLASS-SUBCLASS
MEHARI, YEMANE	2838	363-021010

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): (**Please first reapply any previously paid issue fee shown above**)

❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/709,795	02/22/2010	Daniel A. Artusi	CDW-011CP1CP1C1	7439

25962 7590 03/05/2013

SLATER & MATSIL, L.L.P.
17950 PRESTON RD, SUITE 1000
DALLAS, TX 75252-5793

EXAMINER	
MEHARI, YEMANE	

ART UNIT	PAPER NUMBER
2838	

DATE MAILED: 03/05/2013

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No.	Applicant(s)	
	12/709,795	ARTUSI ET AL.	
	Examiner	Art Unit	
	YEMANE MEHARI	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *12/26/2012*.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are *1-20*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 12/26/2012
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/Adolf Berhane/
Primary Examiner, Art Unit 2838

DETAILED ACTION

Summary

1. This is in response to the RCE filed on 12/26/2012.

2. Receipt is acknowledged of the information disclosure statements filed on 12/26/2012, which information has been considered and entered into the application.

3. Claims 1-20 are pending and have been examined.

Continued Examination Under 37 CFR 1.114

4. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 12/26/2012 has been entered.

Allowable Subject Matter

5. The independent claims 1-20 are allowed over the cited prior arts.

In re to claims 1, 6, 11 & 16: The following is an examiner's statement of reasons for allowance: None of the cited prior art disclose or teach the claimed inventions in which a power converter controller configured to receive a signal from a load indicating a system operational state of the load as recited in claim 1, and a power converter controller configured to receive a signal characterizing a power requirement of a processor system from a power system controller

as recited in claim 6 of the present application. In addition, none of the cited prior art disclose or teach a power converter controller configured to receive a signal to identify an operation of a processor system in a state of power drain from a power system controller as recited in claim 11, and providing a signal to identify an operation of a processor system in a state of power drain, sensing a power level of the state of power drain in response to the signal, and controlling a power converter topological state of a power converter as a function of the power level as recited in claim 16 of the present application.

6. The dependent claims 2-5 are allowed due to their dependency on claim 1.

7. The dependent claims 7-10 are allowed due to their dependency on claim 6.

8. The dependent claims 12-15 are allowed due to their dependency on claim 11.

9. The dependent claims 17-20 are allowed due to their dependency on claim 16.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Contact Information

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to YEMANE MEHARI whose telephone number is (571)270-7603. The examiner can normally be reached on Monday, Wednesday & Friday between 9-AM to 6-PM and on Tuesday and Thursday between 8-AM to 3-PM EST. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Dole can be reached on (571)272-2229. The fax phone number for the organization where this application or

proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Y. M./
Examiner, Art Unit 2838

/Adolf Berhane/

Primary Examiner, Art Unit 2838

PTO/SB/08a (03-09)
Approved for use through 04/30/2009. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 2

Complete if Known	
Application Number	12/709,795
Filing Date	2/22/2010
First Named Inventor	Artusi et al.
Art Unit	2838
Examiner Name	Yemane Mehari
Attorney Docket Number	CDW-011CP1CP1C1

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number - Kind Code[2] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1.	US-3,602,795	08-31-1971	Gunn	
	2.	US-5,539,630	07-23-1996	Pietkiewicz et al.	
	3.	US-5,929,665	07-27-1999	Ichikawa et al.	
	4.	US-6,345,364 B1	02-05-2002	Lee	
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	15.	US-7,715,217 B2	05-11-2010	Manabe et al.	
	16.	US-7,733,679 B2	06-08-2010	Luger et al.	
	17.	US-7,746,041 B2	06-29-2010	Xu et al.	
	18.	US-7,940,035 B2	05-10-2011	Yang	
	19.	US-2012-0243271 A1	09-27-2012	Berghegger	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] - Number[4] - Kind Code[5] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
	20.	CN201252294	06-03-2009	Jinfu Huang		

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1]Applicant's unique citation designation number (optional). [2]See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3]Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6]Applicant is to place a check mark here if English language Translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /Y.M./

PTO/SB/08b (03-09)
Approved for use through 04/30/2009. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Substitute for form 1449B/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 2 of 2

Complete if Known	
Application Number	12/709,795
Filing Date	2/22/2010
First Named Inventor	Artusi et al.
Art Unit	2838
Examiner Name	Yemane Mehari
Attorney Docket Number	CDW-011CP1CP1C1

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	21.	Power Integrations, Inc., "TOP200-4-14 TOPSwitch® Family Three-terminal Off-line PWM Switch," Internet Citation http:--www.datasheet4u.com-.download.php?id=311769, July 1996, XP002524650, pp. 1-16.	

Examiner Signature	/Yemane Mehari/	Date Considered	02/21/2013

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.
[1]Applicant's unique citation designation number (optional). [2]Applicant is to place a check mark here if English language Translation is attached.
This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /Y.M./

PTO/SB/08a (03-09)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 2

Complete if Known	
Application Number	12/709,795
Filing Date	2/22/2010
First Named Inventor	Artusi et al.
Art Unit	2838
Examiner Name	Yemane Mehari
Attorney Docket Number	CDW-011CP1CP1C1

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number - Kind Code[2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1.	US-3,602,795	08-31-1971	Gunn	
	2.	US-5,539,630	07-23-1996	Pietkiewicz et al.	
	3.	US-5,929,665	07-27-1999	Ichikawa et al.	
	4.	US-6,345,364 B1	02-05-2002	Lee	
	5.	US-6,548,992 B2	04-15-2003	Alcantar et al.	
	6.	US-6,580,627 B2	06-17-2003	Takahashi	
	7.	US-6,614,206 B1	09-02-2003	Wong et al.	
	8.	US-6,668,296 B1	12-23-2003	Dougherty et al.	
	9.	US-2004-0200631 A1	10-14-2004	Chen	
	10.	US-6,813,170 B2	11-02-2004	Yang	
	11.	US-7,098,640 B2	08-29-2006	Brown	
	12.	US-2008-0205104 A1	08-28-2008	Lev et al.	
	13.	US-7,558,037 B1	07-07-2009	Gong et al.	
	14.	US-2009-0273957 A1	11-05-2009	Feldtkeller	
	15.	US-7,715,217 B2	05-11-2010	Manabe et al.	
	16.	US-7,733,679 B2	06-08-2010	Luger et al.	
	17.	US-7,746,041 B2	06-29-2010	Xu et al.	
	18.	US-7,940,035 B2	05-10-2011	Yang	
	19.	US-2012-0243271 A1	09-27-2012	Berghegger	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] - Number[4] - Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
	20.	CN201252294	06-03-2009	Jinfu Huang		

Examiner Signature		Date Considered	

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PTO/SB/08b (03-09)
Approved for use through 04/30/2009. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Substitute for form 1449B/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 2 of 2

Complete if Known	
Application Number	12/709,795
Filing Date	2/22/2010
First Named Inventor	Artusi et al.
Art Unit	2838
Examiner Name	Yemane Mehari
Attorney Docket Number	CDW-011CP1CP1C1

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	21.	Power Integrations, Inc., "TOP200-4-14 TOPSwitch® Family Three-terminal Off-line PWM Switch," Internet Citation http:--www.datasheet4u.com-.download.php?id=311769, July 1996, XP002524650, pp. 1-16.	

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.
[1]Applicant's unique citation designation number (optional). [2]Applicant is to place a check mark here if English language Translation is attached.
This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

25962 7590 10/03/2012

SLATER & MATSIL, L.L.P.
17950 PRESTON RD, SUITE 1000
DALLAS, TX 75252-5793

EXAMINER	
MEHARI, YEMANE	
ART UNIT	PAPER NUMBER
2838	

DATE MAILED: 10/03/2012

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/709,795	02/22/2010	Daniel A. Artusi	CDW-011CP1CP1C1	7439

TITLE OF INVENTION: POWER SYSTEM WITH POWER CONVERTERS HAVING AN ADAPTIVE CONTROLLER

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1740	$300	$0	$2040	01/03/2013

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 02/11)

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

25962 7590 10/03/2012
SLATER & MATSIL, L.L.P.
17950 PRESTON RD, SUITE 1000
DALLAS, TX 75252-5793

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/709,795	02/22/2010	Daniel A. Artusi	CDW-011CP1CP1C1	7439

TITLE OF INVENTION: POWER SYSTEM WITH POWER CONVERTERS HAVING AN ADAPTIVE CONTROLLER

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1740	$300	$0	$2040	01/03/2013

EXAMINER	ART UNIT	CLASS-SUBCLASS
MEHARI, YEMANE	2838	363-021010

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): (**Please first reapply any previously paid issue fee shown above**)

❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/709,795	02/22/2010	Daniel A. Artusi	CDW-011CP1CP1C1	7439

25962 7590 10/03/2012

SLATER & MATSIL, L.L.P.
17950 PRESTON RD, SUITE 1000
DALLAS, TX 75252-5793

EXAMINER	
MEHARI, YEMANE	
ART UNIT	PAPER NUMBER
2838	

DATE MAILED: 10/03/2012

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No.	Applicant(s)	
	12/709,795	ARTUSI ET AL.	
	Examiner	Art Unit	
	YEMANE MEHARI	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the RCE filed on 08/23/2012*.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-20*.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 08/23/2012
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/Y. M./ Examiner, Art Unit 2838	/Adolf Berhane/ Adolf Berhane Primary Examiner Art Unit 2838

DETAILED ACTION

Summary

1. This is in response to the RCE filed on 08/23/2012.

2. Receipt is acknowledged of the information disclosure statements filed on 08/23/2012, which information has been considered and entered into the application.

3. Claims 1-20 are pending and have been examined.

Continued Examination Under 37 CFR 1.114

4. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 08/23/2012 has been entered.

Allowable Subject Matter

5. The independent claims 1-20 are allowed over the cited prior arts.

In re to claims 1, 6, 11 & 16: The following is an examiner's statement of reasons for allowance: None of the cited prior art disclose or teach the claimed inventions in which a power converter controller configured to receive a signal from a load indicating a system operational state of the load as recited in claim 1, and a power converter controller configured to receive a signal characterizing a power requirement of a processor system from a power system controller

as recited in claim 6 of the present application. In addition, none of the cited prior art disclose or teach a power converter controller configured to receive a signal to identify an operation of a processor system in a state of power drain from a power system controller as recited in claim 11, and providing a signal to identify an operation of a processor system in a state of power drain, sensing a power level of the state of power drain in response to the signal, and controlling a power converter topological state of a power converter as a function of the power level as recited in claim 16 of the present application.

6. The dependent claims 2-5 are allowed due to their dependency on claim 1.

7. The dependent claims 7-10 are allowed due to their dependency on claim 6.

8. The dependent claims 12-15 are allowed due to their dependency on claim 11.

9. The dependent claims 17-20 are allowed due to their dependency on claim 16.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to YEMANE MEHARI whose telephone number is (571)270-7603. The examiner can normally be reached on Monday to Thursday, 8 AM to 5 PM, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Monica N. Lewis can be reached on (571)272-1838. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Y. M./

Examiner, Art Unit 2838

/Adolf Berhane/
Adolf Berhane
Primary Examiner
Art Unit 2838

PTO/SB/08a (01-08)
Approved for use through 06/30/2008. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 2

Complete if Known	
Application Number	12/709,795
Filing Date	02-22-2010
First Named Inventor	Artusi
Art Unit	2838
Examiner Name	Yemane Mehari
Attorney Docket Number	CDW-011CP1CP1C1

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number - Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1	US-2,473,662	06-21-1949	Pohm	
	2	US-4,202,031	05-06-1980	Hesler, et al.	
	3	US-4,613,841	09-23-1986	Roberts	
	4	US-5,523,673	06-04-1996	Ratliff, et al.	
	5	US-5,946,207	08-31-1999	Schoofs	
	6	US-6,046,664	04-04-2000	Weller, et al.	
	7	US-6,288,501 B1	09-11-2001	Nakamura, et al.	
	8	US-6,317,021 B1	11-13-2001	Jansen	
	9	US-2002/0057080 A1	05-16-2002	Telefus et al.	
	10	US-6,611,132 B2	08-26-2003	Nakagawa et al.	
	11	US-2004/0217794 A1	11-04-2004	Strysko	
	12	US-6,867,986 B2	03-15-2005	Amei	
	13	US-7,099,163 B1	08-29-2006	Ying	
	14	US-7,269,038 B2	09-11-2007	Shekhawat et al.	
	15	US-7,386,404 B1	06-10-2008	Cargonja, et al.	
	16	US-7,348,612 B2	03-25-2008	Sriram et al.	
	17	US-2008/0298106 A1	12-04-2008	Tataeishi	
	18	US-2009/0284994 A1	11-19-2009	Lin et al.	
	19	US-7,778,050 B2	08-17-2010	Yamashita	
	20	US-7,778,051 B2	08-17-2010	Yang	
	21	US-8,179,699 B2	05-15-2012	Tumminaro et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] - Number[4] - Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
	22	JP 57097361 A	06-17-1982	Miyazaki Takaharu		
	23	WO8700991	02-12-1987	Pham-Dang Tam		
	24	CN101141099	03-12-2008	Zheng GE		

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1]Applicant's unique citation designation number (optional). [2]See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3]Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6]Applicant is to place a check mark here if English language Translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /Y.M./

PTO/SB/08b (10-07)
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Substitute for form 1449B/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 2 of 2

Complete if Known	
Application Number	12/709,795
Filing Date	02-22-2010
First Named Inventor	Artusi
Art Unit	2838
Examiner Name	Yemane Mehari
Attorney Docket Number	CDW-011CP1CP1C1

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	25	XU, P., et al., "Design and Performance Evaluation of Multi-Channel Interleaved Quasi-Square-Wave Buck Voltage Regulator Module," HFPC 2000 Proceedings, October 2000, pp. 82–88.	

Examiner Signature	/Yemane Mehari/	Date Considered	08/31/2012

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.
[1]Applicant's unique citation designation number (optional). [2]Applicant is to place a check mark here if English language Translation is attached.
This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /Y.M./

PTO/SB/30 (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Request for Continued Examination (RCE) Transmittal

Address to:
Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Application Number	12/709,795
Filing Date	2/22/2010
First Named Inventor	Artusi, *et al.*
Art Unit	2838
Examiner Name	Yemane Mehari
Attorney Docket Number	CDW-011CP1CP1C1

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. See Instruction Sheet for RCEs (not to be submitted to the USPTO) on page 2.

1. Submission required under 37 CFR 1.114 Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).
   - a. ☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.
     - i. ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
     - ii. ☐ Other _____
   - b. ☒ Enclosed
     - i. ☐ Amendment/Reply
     - ii. ☐ Affidavit(s)/Declaration(s)
     - iii. ☒ Information Disclosure Statement (IDS)
     - iv. ☐ Other _____

2. Miscellaneous
   - a. ☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of _____ months. (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)
   - b. ☐ Other _____

3. Fees The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.
   - a. ☒ The Director is hereby authorized to charge the following fees, any underpayment of fees, or credit any overpayments, to Deposit Account No. 50-1065.
     - i. ☒ RCE fee required under 37 CFR 1.17(e)
     - ii. ☐ Extension of time fee (37 CFR 1.136 and 1.17)
     - iii. ☐ Other _____
   - b. ☐ Check in the amount of $ _____ enclosed
   - c. ☐ Payment by credit card (Form PTO-2038 enclosed)

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

Signature	/Glenn W. Boisbrun/	Date	August 23, 2012
Name (Print/Type)	Glenn W. Boisbrun	Registration No.	39,615

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop RCE, Commissioner For Patents, P.O. Box 1450, Alexandria, VA 22313-1450 or facsimile transmitted to the U.S. Patent and Trademark Office on the date shown below.

Signature			
Name (Print/Type)		Date	

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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 2

Complete if Known	
Application Number	12/709,795
Filing Date	02-22-2010
First Named Inventor	Artusi
Art Unit	2838
Examiner Name	Yemane Mehari
Attorney Docket Number	CDW-011CP1CP1C1

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number - Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1	US-2,473,662	06-21-1949	Pohm	
	2	US-4,202,031	05-06-1980	Hesler, et al.	
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	23	WO8700991	02-12-1987	Pham-Dang Tam		
	24	CN101141099	03-12-2008	Zheng GE		

Examiner Signature		Date Considered	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 2 of 2

Complete if Known	
Application Number	12/709,795
Filing Date	02-22-2010
First Named Inventor	Artusi
Art Unit	2838
Examiner Name	Yemane Mehari
Attorney Docket Number	CDW-011CP1CP1C1

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	25	XU, P., et al., "Design and Performance Evaluation of Multi-Channel Interleaved Quasi-Square-Wave Buck Voltage Regulator Module," HFPC 2000 Proceedings, October 2000, pp. 82–88.	

Examiner Signature		Date Considered	

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This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
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NOTICE OF ALLOWANCE AND FEE(S) DUE

25962 7590 05/23/2012

SLATER & MATSIL, L.L.P.
Ira Matsil
17950 PRESTON RD, SUITE 1000
DALLAS, TX 75252-5793

EXAMINER	
MEHARI, YEMANE	
ART UNIT	PAPER NUMBER
2838	

DATE MAILED: 05/23/2012

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/709,795	02/22/2010	Daniel A. Artusi	CDW-011CP2C1	7439

TITLE OF INVENTION: POWER SYSTEM WITH POWER CONVERTERS HAVING AN ADAPTIVE CONTROLLER

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1740	$300	$0	$2040	08/23/2012

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 02/11)

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

25962 7590 05/23/2012
SLATER & MATSIL, L.L.P.
Ira Matsil
17950 PRESTON RD, SUITE 1000
DALLAS, TX 75252-5793

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/709,795	02/22/2010	Daniel A. Artusi	CDW-011CP2C1	7439

TITLE OF INVENTION: POWER SYSTEM WITH POWER CONVERTERS HAVING AN ADAPTIVE CONTROLLER

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1740	$300	$0	$2040	08/23/2012

EXAMINER	ART UNIT	CLASS-SUBCLASS
MEHARI, YEMANE	2838	363-021010

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): (**Please first reapply any previously paid issue fee shown above**)

❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/709,795	02/22/2010	Daniel A. Artusi	CDW-011CP2C1	7439

25962 7590 05/23/2012

SLATER & MATSIL, L.L.P.
Ira Matsil
17950 PRESTON RD, SUITE 1000
DALLAS, TX 75252-5793

EXAMINER	
MEHARI, YEMANE	
ART UNIT	**PAPER NUMBER**
2838	

DATE MAILED: 05/23/2012

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 12/709,795	Applicant(s) ARTUSI ET AL.	
	Examiner YEMANE MEHARI	Art Unit 2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the RCE filed on 04/19/2012* .
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-20*.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 04/19/2012
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/Y. M./ Examiner, Art Unit 2838	/Adolf Berhane/ Adolf Berhane Primary Examiner Art Unit 2838

DETAILED ACTION

Summary

1. This is in response to the RCE filed on 04/19/2012.

2. Receipt is acknowledged of the information disclosure statements filed on 04/19/2012, which information has been considered and entered into the application.

3. Claims 1-20 are pending and have been examined.

Continued Examination Under 37 CFR 1.114

4. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 04/19/2012 has been entered.

Allowable Subject Matter

5. The independent claims 1-20 are allowed over the cited prior arts.

In re to claims 1, 6, 11 & 16: The following is an examiner's statement of reasons for allowance: None of the cited prior art disclose or teach the claimed inventions in which a power converter controller configured to receive a signal from a load indicating a system operational state of the load as recited in claim 1, and a power converter controller configured to receive a signal characterizing a power requirement of a processor system from a power system controller

as recited in claim 6 of the present application. In addition, none of the cited prior art disclose or teach a power converter controller configured to receive a signal to identify an operation of a processor system in a state of power drain from a power system controller as recited in claim 11, and providing a signal to identify an operation of a processor system in a state of power drain, sensing a power level of the state of power drain in response to the signal, and controlling a power converter topological state of a power converter as a function of the power level as recited in claim 16 of the present application.

6. The dependent claims 2-5 are allowed due to their dependency on claim 1.

7. The dependent claims 7-10 are allowed due to their dependency on claim 6.

8. The dependent claims 12-15 are allowed due to their dependency on claim 11.

9. The dependent claims 17-20 are allowed due to their dependency on claim 16.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to YEMANE MEHARI whose telephone number is (571)270-7603. The examiner can normally be reached on Monday to Thursday, 8 AM to 5 PM, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Monica N. Lewis can be reached on (571)272-1838. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Y. M./

Examiner, Art Unit 2838

/Adolf Berhane/
Adolf Berhane
Primary Examiner
Art Unit 2838

PTO/SB/08a (03-09)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 2

Complete if Known	
Application Number	12/709,795
Filing Date	2/22/2010
First Named Inventor	Artusi et al.
Art Unit	2838
Examiner Name	Yemane Mehari
Attorney Docket Number	CDW-011CP1CP1C1

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number - Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1.	US-3,007,060	10-31-1961	Guenther	
	2.	US-3,708,742	01-02-1973	Gunn	
	3.	US-4,274,071	06-16-1981	Pfarre	
	4.	US-5,225,971	07-06-1993	Spreen	
	5.	US-6,160,721	12-12-2000	Kossives et al.	
	6.	US-6,304,460 B1	10-16-2001	Cuk	
	7.	US-6,317,337 B1	11-13-2001	Yasumura	
	8.	US-6,438,009 B2	08-20-2002	Assow	
	9.	US-6,466,461 B2	10-15-2002	Mao et al.	
	10.	US-2003/0026115 A1	02-06-2003	Miyazaki	
	11.	US-6,552,917 B2	04-22-2003	Bourdillon	
	12.	US-6,608,768 B2	08-19-2003	Sula	
	13.	US-6,687,137 B1	02-03-2004	Yasumura	
	14.	US-20040217794 A1	11-04-2004	Strysko	
	15.	US-6,856,149 B2	02-15-2005	Yang	
	16.	US-6,882,548 B1	04-19-2005	Jacobs et al.	
	17.	US-7,301,785 B2	11-27-2007	Yasumura	
	18.	US-7,339,801 B2	03-04-2008	Yasumura	

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Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1]Applicant's unique citation designation number (optional). [2]See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3]Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6]Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /Y.M./

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Sheet 2 of 2

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Examiner Name	Yemane Mehari
Attorney Docket Number	CDW-011CP1CP1C1

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	19.	US-2008/0137381 A1	06-12-2008	Beasley	
	20.	US-7,446,512 B2	11-04-2008	Nishihara et al.	
	21.	US-7,447,049 B2	11-04-2008	Garner et al.	
	22.	US-7,471,523 B2	12-30-2008	Yang	
	23.	US-7,499,295 B2	03-03-2009	Indika de Silva et al.	
	24.	US-7,567,445 B2	07-28-2009	Coulson et al.	
	25.	US-2009/0257250 A1	10-15-2009	Liu	
	26.	US-2010/0123486 A1	05-20-2010	Berghegger	
	27.	US-7,847,535 B2	12-07-2010	Meynard et al.	
	28.	US-7,965,528 B2	06-21-2011	Yang et al.	
	29.	US-2011/0305047 A1	12-15-2011	Jungreis et al.	

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	30.	JP57097361	06-17-1982	Takaharu		

Examiner Signature	/Yemane Mehari/	Date Considered	05/17/2012

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	23.	US-7,499,295 B2	03-03-2009	Indika de Silva et al.	
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PTO/SB/30 (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Request for Continued Examination (RCE) Transmittal

Address to:
Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Application Number	12/709,795
Filing Date	2/22/2010
First Named Inventor	Artusi, *et al.*
Art Unit	2838
Examiner Name	Yemane Mehari
Attorney Docket Number	CDW-011CP1CP1C1

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. See Instruction Sheet for RCEs (not to be submitted to the USPTO) on page 2.

1. Submission required under 37 CFR 1.114 Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).
   - a. ☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.
     - i. ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
     - ii. ☐ Other _____
   - b. ☒ Enclosed
     - i. ☐ Amendment/Reply
     - ii. ☐ Affidavit(s)/Declaration(s)
     - iii. ☒ Information Disclosure Statement (IDS)
     - iv. ☐ Other _____

2. Miscellaneous
   - a. ☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of _____ months. (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)
   - b. ☐ Other _____

3. Fees The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.
   - a. ☒ The Director is hereby authorized to charge the following fees, any underpayment of fees, or credit any overpayments, to Deposit Account No. 50-1065.
     - i. ☒ RCE fee required under 37 CFR 1.17(e)
     - ii. ☐ Extension of time fee (37 CFR 1.136 and 1.17)
     - iii. ☐ Other _____
   - b. ☐ Check in the amount of $ _____ enclosed
   - c. ☐ Payment by credit card (Form PTO-2038 enclosed)

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

Signature	/Glenn W. Boisbrun/	Date	April 19, 2012
Name (Print/Type)	Glenn W. Boisbrun	Registration No.	39,615

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop RCE, Commissioner For Patents, P.O. Box 1450, Alexandria, VA 22313-1450 or facsimile transmitted to the U.S. Patent and Trademark Office on the date shown below.

Signature			
Name (Print/Type)		Date	

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

25962 7590 01/19/2012

SLATER & MATSIL, L.L.P.
17950 PRESTON RD, SUITE 1000
DALLAS, TX 75252-5793

EXAMINER	
MEHARI, YEMANE	
ART UNIT	PAPER NUMBER
2838	

DATE MAILED: 01/19/2012

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/709,795	02/22/2010	Daniel A. Artusi	CDW-011CP1CP1C1	7439

TITLE OF INVENTION: POWER SYSTEM WITH POWER CONVERTERS HAVING AN ADAPTIVE CONTROLLER

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1740	$300	$0	$2040	04/19/2012

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 02/11)

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

25962 7590 01/19/2012
SLATER & MATSIL, L.L.P.
17950 PRESTON RD, SUITE 1000
DALLAS, TX 75252-5793

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/709,795	02/22/2010	Daniel A. Artusi	CDW-011CP1CP1C1	7439

TITLE OF INVENTION: POWER SYSTEM WITH POWER CONVERTERS HAVING AN ADAPTIVE CONTROLLER

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1740	$300	$0	$2040	04/19/2012

EXAMINER	ART UNIT	CLASS-SUBCLASS
MEHARI, YEMANE	2838	363-021010

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): (**Please first reapply any previously paid issue fee shown above**)

❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/709,795	02/22/2010	Daniel A. Artusi	CDW-011CP1CP1C1	7439

25962 7590 01/19/2012

SLATER & MATSIL, L.L.P.
17950 PRESTON RD, SUITE 1000
DALLAS, TX 75252-5793

EXAMINER	
MEHARI, YEMANE	

ART UNIT	PAPER NUMBER
2838	

DATE MAILED: 01/19/2012

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Supplemental Notice of Allowability	Application No. 12/709,795	Applicant(s) ARTUSI ET AL.	
	Examiner YEMANE MEHARI	Art Unit 2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *12/16/2011*.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are *1-20*.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 12/16/2011
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/Y. M./ Examiner, Art Unit 2838	/Adolf Berhane/ Adolf Berhane Primary Examiner Art Unit 2838

DETAILED ACTION

Summary

1. This is in response to the response filed on 12/16/2011.

2. Receipt is acknowledged of the information disclosure statements filed on 12/16/2011, which information has been considered and entered into the application.

3. Claims 1-20 are pending and have been examined.

Continued Examination Under 37 CFR 1.114

4. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 12/16/2011 has been entered.

Allowable Subject Matter

5. The independent claims 1-20 are allowed over the cited prior arts.

In re to claims 1, 6, 11 & 16: The following is an examiner's statement of reasons for allowance: None of the cited prior art disclose or teach the claimed inventions in which a power converter controller configured to receive a signal from a load indicating a system operational state of the load as recited in claim 1, and a power converter controller configured to receive a signal characterizing a power requirement of a processor system from a power system controller

as recited in claim 6 of the present application. In addition, none of the cited prior art disclose or teach a power converter controller configured to receive a signal to identify an operation of a processor system in a state of power drain from a power system controller as recited in claim 11, and providing a signal to identify an operation of a processor system in a state of power drain, sensing a power level of the state of power drain in response to the signal, and controlling a power converter topological state of a power converter as a function of the power level as recited in claim 16 of the present application.

6. The dependent claims 2-5 are allowed due to their dependency on claim 1.

7. The dependent claims 7-10 are allowed due to their dependency on claim 6.

8. The dependent claims 12-15 are allowed due to their dependency on claim 11.

9. The dependent claims 17-20 are allowed due to their dependency on claim 16.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to YEMANE MEHARI whose telephone number is (571)270-7603. The examiner can normally be reached on Monday to Thursday, 8 AM to 5 PM, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Monica N. Lewis can be reached on (571)272-1838. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Y. M./

Examiner, Art Unit 2838

/Adolf Berhane/
Adolf Berhane
Primary Examiner
Art Unit 2838

PTO/SB/08a (03-09)
Approved for use through 04/30/2009. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	12/709,795
Filing Date	2/22/2010
First Named Inventor	Artusi et al.
Art Unit	2838
Examiner Name	Yemane Mehari
Attorney Docket Number	CDW-011CP1CP1C1

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number - Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1.	US-5,907,481	05-25-1999	Svardsjo	
	2.	US-5,999,429	12-07-1999	Brown	
	3.	US-6,674,658 B2	01-06-2004	Mao et al.	
	4.	US-6,804,125 B2	10-12-2004	Brkovic	
	5.	US-7,095,638 B2	08-22-2006	Uusitalo	
	6.	US-7,558,082 B2	07-07-2009	Jitaru	
	7.	US-7,795,849 B2	09-14-2010	Sohma	
	8.	US-2011/0149607 A1	06-23-2011	Jungreis et al.	
	9.	US-2011/0182089 A1	07-28-2011	Berghegger	
	10.	US-2011/0239008 A1	09-29-2011	Lam et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] - Number[4] - Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
	11.	WO 2011/116225 A1	09-22-2011	Power Systems Technologies, Ltd.		

Examiner Signature	/Yemane Mehari/	Date Considered	01/03/2012

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1]Applicant's unique citation designation number (optional). [2]See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3]Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6]Applicant is to place a check mark here if English language Translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /Y.M./

PTO/SB/30 (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Request for Continued Examination (RCE) Transmittal

Address to:
Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Application Number	12/709,795
Filing Date	2/22/2010
First Named Inventor	Artusi, *et al.*
Art Unit	2838
Examiner Name	Yemane Mehari
Attorney Docket Number	CDW-011CP1CP1C1

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. See Instruction Sheet for RCEs (not to be submitted to the USPTO) on page 2.

1. Submission required under 37 CFR 1.114 Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).
   - a. ☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.
     - i. ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
     - ii. ☐ Other _____
   - b. ☒ Enclosed
     - i. ☐ Amendment/Reply
     - ii. ☐ Affidavit(s)/Declaration(s)
     - iii. ☒ Information Disclosure Statement (IDS)
     - iv. ☐ Other _____

2. Miscellaneous
   - a. ☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of _____ months. (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)
   - b. ☐ Other _____

3. Fees The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.
   - a. ☒ The Director is hereby authorized to charge the following fees, any underpayment of fees, or credit any overpayments, to Deposit Account No. 50-1065.
     - i. ☒ RCE fee required under 37 CFR 1.17(e)
     - ii. ☐ Extension of time fee (37 CFR 1.136 and 1.17)
     - iii. ☐ Other _____
   - b. ☐ Check in the amount of $ _____ enclosed
   - c. ☐ Payment by credit card (Form PTO-2038 enclosed)

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

Signature	/Glenn W. Boisbrun/	Date	December 16, 2011
Name (Print/Type)	Glenn W. Boisbrun	Registration No.	39615

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop RCE, Commissioner For Patents, P.O. Box 1450, Alexandria, VA 22313-1450 or facsimile transmitted to the U.S. Patent and Trademark Office on the date shown below.

Signature			
Name (Print/Type)		Date	

PTO/SB/08a (03-09)
Approved for use through 04/30/2009. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	12/709,795
Filing Date	2/22/2010
First Named Inventor	Artusi et al.
Art Unit	2838
Examiner Name	Yemane Mehari
Attorney Docket Number	CDW-011CP1CP1C1

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number - Kind Code[2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1.	US-5,907,481	05-25-1999	Svardsjo	
	2.	US-5,999,429	12-07-1999	Brown	
	3.	US-6,674,658 B2	01-06-2004	Mao et al.	
	4.	US-6,804,125 B2	10-12-2004	Brkovic	
	5.	US-7,095,638 B2	08-22-2006	Uusitalo	
	6.	US-7,558,082 B2	07-07-2009	Jitaru	
	7.	US-7,795,849 B2	09-14-2010	Sohma	
	8.	US-2011/0149607 A1	06-23-2011	Jungreis et al.	
	9.	US-2011/0182089 A1	07-28-2011	Berghegger	
	10.	US-2011/0239008 A1	09-29-2011	Lam et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] - Number[4] - Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
	11.	WO 2011/116225 A1	09-22-2011	Power Systems Technologies, Ltd.		

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1]Applicant's unique citation designation number (optional). [2]See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3]Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6]Applicant is to place a check mark here if English language Translation is attached.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

25962 7590 09/21/2011

SLATER & MATSIL, L.L.P.
17950 PRESTON RD, SUITE 1000
DALLAS, TX 75252-5793

EXAMINER
MEHARI, YEMANE

ART UNIT	PAPER NUMBER
2838	

DATE MAILED: 09/21/2011

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/709,795	02/22/2010	Daniel A. Artusi	CDW-011CP1CP1C1	7439

TITLE OF INVENTION: POWER SYSTEM WITH POWER CONVERTERS HAVING AN ADAPTIVE CONTROLLER

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	12/21/2011

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 02/11)

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

25962 7590 09/21/2011
SLATER & MATSIL, L.L.P.
17950 PRESTON RD, SUITE 1000
DALLAS, TX 75252-5793

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/709,795	02/22/2010	Daniel A. Artusi	CDW-011CP1CP1C1	7439

TITLE OF INVENTION: POWER SYSTEM WITH POWER CONVERTERS HAVING AN ADAPTIVE CONTROLLER

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	12/21/2011

EXAMINER	ART UNIT	CLASS-SUBCLASS
MEHARI, YEMANE	2838	363-021010

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): (**Please first reapply any previously paid issue fee shown above**)

❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/709,795	02/22/2010	Daniel A. Artusi	CDW-011CP1CP1C1	7439

25962 7590 09/21/2011

SLATER & MATSIL, L.L.P.
17950 PRESTON RD, SUITE 1000
DALLAS, TX 75252-5793

EXAMINER	
MEHARI, YEMANE	
ART UNIT	PAPER NUMBER
2838	

DATE MAILED: 09/21/2011

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No.	Applicant(s)	
	12/709,795	ARTUSI ET AL.	
	Examiner	Art Unit	
	YEMANE MEHARI	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the argument filed on 06/20/2011*.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are *1-20*.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 06/20/2011
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/Adolf Berhane/
Adolf Berhane
Primary Examiner
Art Unit 2838

DETAILED ACTION

Summary

1. This is in response to the response filed on 06/20/2011.

2. Claims 1-20 are pending and have been examined.

Allowable Subject Matter

3. The independent claims 1, 6, 11 & 16 are allowed over the cited prior arts. The following is an examiner's statement of reasons for allowance: None of the cited prior art disclose or teach the claimed inventions in which a power converter controller configured to receive a signal from a load indicating a system operational state of the load as recited in claim 1, and a power converter controller configured to receive a signal characterizing a power requirement of a processor system from a power system controller as recited in claim 6 of the present application. In addition, none of the cited prior art disclose or teach a power converter controller configured to receive a signal to identify an operation of a processor system in a state of power drain from a power system controller as recited in claim 11, and providing a signal to identify an operation of a processor system in a state of power drain, sensing a power level of the state of power drain in response to the signal, and controlling a power converter topological state of a power converter as a function of the power level as recited in claim 16 of the present application.

4. The dependent claims 2-5 are allowed due to their dependency on claim 1.

5. The dependent claims 7-10 are allowed due to their dependency on claim 6.

6. The dependent claims 12-15 are allowed due to their dependency on claim 11.

7. The dependent claims 17-20 are allowed due to their dependency on claim 16.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to YEMANE MEHARI whose telephone number is (571)270-7603. The examiner can normally be reached on Monday to Thursday, 8 AM to 5 PM, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Monica N. Lewis can be reached on (571)272-1838. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Adolf Berhane/
Adolf Berhane
Primary Examiner
Art Unit 2838

/Y. M./Examiner, Art Unit 2838

PTO/SB/08a (01-08)
Approved for use through 06/30/2008. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 3

Complete if Known	
Application Number	12/709,795
Filing Date	02-22-2010
First Named Inventor	Artusi
Art Unit	2838
Examiner Name	Yemane Mehari
Attorney Docket Number	CDW-011CP1CP1C1

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number - Kind Code[2] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1	US-4,962,354	10-09-1990	Visser, et al.	
	2	US-5,959,850	09-28-1999	Lim	
	3	US-6,069,798	05-30-2000	Liu	
	4	US-6,325,035 B1	12-04-2001	Codina, et al.	
	5	US-6,373,727 B1	04-16-2002	Hedenskog, et al.	
	6	US-2003/0026115 A1	02-06-2003	Miyazaki	
	7	US-6,552,917	04-22-2003	Bourdillon	
	8	US-6,654,259 B2	11-25-2003	Koshita, et al.	
	9	US-7,209,024 B2	04-24-2007	Nakahori	
	10	US-2007/0120953 A1	05-31-2007	Koga, et al.	
	11	US-2007/0121351 A1	05-31-2007	Zhang, et al.	
	12	US-2007/0241721 A1	10-18-2007	Weinstein, et al.	
	13	US-7,375,607 B2	05-20-2008	Lee, et al.	
	14	US-2009/0027926 A1	01-29-2009	Yang, et al.	
	15	US-2009/0046486 A1	02-19-2009	Lu, et al.	
	16	US-2009/0109711 A1	04-30-2009	Hsu	
	17	US-2009/0257250 A1	10-15-2009	Liu	
	18	US-2010/0123486	05-20-2010	Berghegger	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] - Number[4] - Kind Code[5] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1]Applicant's unique citation designation number (optional). [2]See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3]Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6]Applicant is to place a check mark here if English language Translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /Y.M./

PTO/SB/08a (01-08)
Approved for use through 06/30/2008. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 2 of 3

Complete if Known	
Application Number	12/709,795
Filing Date	02-22-2010
First Named Inventor	Artusi
Art Unit	2838
Examiner Name	Yemane Mehari
Attorney Docket Number	CDW-011CP1CP1C1

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number - Kind Code[2] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	19	US-2010/0149838	06-17-2010	Artusi et al.	
	20	US-2010/0254168 A1	10-07-2010	Chandrasekaran	
	21	US-2010/0321958 A1	12-23-2010	Brinlee, et al.	
	22	US-2010/0321964 A1	12-23-2010	Brinlee, et al.	
	23	US-7,889,517 B2	02-15-2011	Artusi, et al.	
	24	US-2011/0038179 A1	02-17-2011	Zhang	
	25	US-7,906,941 B2	03-15-2011	Jayaraman, et al.	
	26	US-2011/0134664 A1	06-09-2011	Berghegger	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] - Number[4] - Kind Code[5] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

Examiner Signature		Date Considered	

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /Y.M./

PTO/SB/08b (01-08)
Approved for use through 06/30/2008. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Substitute for form 1449B/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 3 of 3

	Complete if Known
Application Number	12/709,795
Filing Date	02-22-2010
First Named Inventor	Artusi
Art Unit	2838
Examiner Name	Yemane Mehari
Attorney Docket Number	CDW-011CP1CP1C1

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	27	Freescale Semiconductor, "Design of a Digital AC/DC SMPS using the 56F8323 Device, Designer Reference Manual, 56800E 16-bit Digital Signal Controllers", DRM074, Rev. 0, August 2005 (108 pages).	
	28	Freescale Semiconductor, "56F8323 Evaluation Module User Manual, 56F8300 16-bit Digital Signal Controllers", MC56F8323EVMUM, Rev. 2, July 2005 (72 pages).	
	29	Freescale Semiconductor, "56F8323/56F8123 Data Sheet Preliminary Technical Data, 56F8300 16-bit Digital Signal Controllers," MC56F8323 Rev. 17, April 2007 (140 pages).	

Examiner Signature	/Yemane Mehari/	Date Considered	09/10/2011

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.
[1]Applicant's unique citation designation number (optional). [2]Applicant is to place a check mark here if English language Translation is attached.
This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Artusi, *et al.*	Docket No.:	CDW-011CP1CP1C1
Serial No.:	12/709,795	Art Unit:	2838
Filed:	February 22, 2010	Examiner:	Mehari, Yemane
For:	POWER SYSTEM WITH POWER CONVERTERS HAVING AN ADAPTIVE CONTROLLER		

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT UNDER 37 CFR §1.111

Dear Sir:

The following remarks are presented in response to the Examiner's Office Action mailed March 18, 2011. Please amend the above-referenced application as follows. No new matter has been added.

IN THE CLAIMS:

1. (Original) A power converter coupled to a load, comprising:

a power switch configured to conduct for a duty cycle to provide an output characteristic at an output thereof; and

a power converter controller configured to receive a signal from said load indicating a system operational state of said load and control an internal operating characteristic of said power converter as a function of said signal.

2. (Original) The power converter as recited in Claim 1 wherein said power converter controller is further configured to provide another signal to control said duty cycle of said power switch as a function of said output characteristic and in accordance with said signal.

3. (Original) The power converter as recited in Claim 1 wherein said power converter controller is configured to adjust said internal operating characteristic over a period of time.

4. (Original) The power converter as recited in Claim 1 wherein said load is a processor and said system operational state is dependent on one of a core state and a performance state of said processor.

5. (Original) The power converter as recited in Claim 1 wherein said internal operating characteristic is selected from the group consisting of:

a gate drive voltage level of said power switch of said power converter,

a switching frequency of said power converter, and

an internal direct current bus voltage of said power converter.

6. (Original) A power system, comprising:

a power system controller configured to provide a signal characterizing a power

requirement of a processor system; and

a power converter coupled to said processor system, comprising:

a power switch configured to conduct for a duty cycle to provide an output characteristic at an output thereof, and

a power converter controller configured to receive a signal from said power system controller to control an internal operating characteristic of said power converter as a function of said signal.

7. (Original) The power system as recited in Claim 6 wherein said power converter controller is further configured to provide another signal to control said duty cycle of said power switch as a function of said output characteristic and in accordance with said signal.

8. (Original) The power system as recited in Claim 6 wherein said power converter controller is configured to adjust said internal operating characteristic over a period of time.

9. (Original) The power system as recited in Claim 6 wherein said power requirement of a processor system is dependent on one of a core state and a performance state of said processor system.

10. (Original) The power system as recited in Claim 6 wherein said internal operating characteristic is selected from the group consisting of:

a gate drive voltage level of said power switch of said power converter,

a switching frequency of said power converter, and

an internal direct current bus voltage of said power converter.

11. (Original) A power system, comprising:

a power system controller configured to enable operation of components of a processor system to establish a state of power drain thereof, said power system controller configured to

provide a signal to identify operation of said processor system in said state of power drain; and

a power converter, coupled to said processor system, comprising a power converter controller configured to receive said signal from said power system controller, to sense a power level of said state of power drain in response to said signal, and to control an internal operating characteristic of said power converter as a function of said power level.

12. (Original) The power system as recited in Claim 11 wherein said power converter further comprises a power switch configured to conduct for a duty cycle to provide an output characteristic at an output thereof, said power converter controller further configured to control said duty cycle of said power switch dependent on said output characteristic and in accordance with said power level.

13. (Original) The power system as recited in Claim 11 wherein said signal is provided upon startup of said processor system.

14. (Original) The power system as recited in Claim 11 wherein said power converter controller is configured to adjust said internal operating characteristic over a period of time.

15. (Original) The power system as recited in Claim 11 wherein said internal operating characteristic is selected from the group consisting of:

a gate drive voltage level of a power switch of said power converter,

a switching frequency of said power converter, and

an internal direct current bus voltage of said power converter.

16. (Original) A method of operating a power system, comprising:

enabling operation of components of a processor system to establish a state of power drain thereof;

providing a signal to identify operation of said processor system in said state of power

drain;

sensing a power level of said state of power drain in response to said signal; and

controlling an internal operating characteristic of a power converter as a function of said power level.

17. (Original) The method as recited in Claim 16, further comprising:

inducing a power switch of said power converter to conduct for a duty cycle to provide an output characteristic at an output thereof; and

controlling said duty cycle of said power switch dependent on said output characteristic and in accordance with said power level.

18. (Original) The method as recited in Claim 16 wherein said signal is provided upon startup of said processor system.

19. (Original) The method as recited in Claim 16 wherein said controlling said internal operating characteristic comprises occurs over a period of time.

20. (Original) The method as recited in Claim 16 wherein said internal operating characteristic is selected from the group consisting of:

a gate drive voltage level of a power switch of said power converter,

a switching frequency of said power converter, and

an internal direct current bus voltage of said power converter.

REMARKS

The Applicants have carefully considered this application in connection with the Examiner's Office Action and respectfully request reconsideration of this application in view of the following remarks.

The Applicants originally submitted Claims 1-20 in the application. No claims have been amended, added or cancelled herein. Accordingly, Claims 1-20 are currently pending in the application.

I. Rejections under 35 U.S.C. §102

A. The Examiner has rejected Claims 1-3 and 5 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,344,986 to Jain, *et al.* ("Jain"). The Examiner believes that Jain discloses all of the limitations of independent Claim 1 of the present application including a power converter controller (*i.e.*, 68) configured to receive a signal (*i.e.*, 64) from a load indicating a system operational state of said load and control an internal operating characteristic of the power converter as a function of the signal (*i.e.*, such as input and output voltage are examples of internal operating characteristics, column 6, lines 11-59). (Examiner's Office Action, p. 2.) The Applicants respectfully disagree.

Referring to FIGURE 1, Jain provides that a flyback converter 22 receives a first DC voltage V_{DC} from a boost converter 20 across a node 24 and ground 16. The flyback converter 22 converts the first DC voltage V_{DC} to an output voltage V_o across a node 62 and an output ground 63. The output voltage V_o is a regulated DC voltage of lower value than the first DC voltage V_{DC} and within the desired voltage range for the particular specification of the power supply. Regulation of the output voltage V_o is accomplished in a conventional way. Preferably,

feedback of the output voltage V_o from a node 62 is provided on a signal line 64, which is coupled to an input terminal 66 of a controller 68. An output terminal 70 of the controller 68 is coupled to a signal line 72, which in turn is coupled to a control node 56 of a FET switch 48. (Column 6, lines 4-17.) It appears to the Applicants that Jain is monitoring the output voltage of the power converter to control the same via a conventional feedback loop configuration.

In stark contrast, the power converter as recited in independent Claim 1 of the present application includes a power converter controller configured to receive a signal from a load indicating a system operational state of the load and control an internal operating characteristic of the power converter as a function of the signal. A system operational state of the load is more than just an output voltage of the power converter.

In an embodiment, the present application provides examples of environmental parameters including, without limitation, a signal indicating the existence of a paralleled power converter, the operational state of the paralleled power converter, that the powered system is operating from a backup power source, a request for a particular load voltage, an indication that a particular portion of the load has failed, or has been disabled, or is operating at a reduced power level. Further examples indicating a system operational state include, without limitation, a signal providing a performance state or a core state of a processor such as a P-state or C-state, indicating, for example, that the system is operating from emergency power or battery reserve, that redundant hardware such as a redundant power converter may have been disabled, that the system is not providing a critical function such as during an off-hours timeframe, that the system is sustaining substantial thermal margins allowing selected fans to be disabled and/or the fan speed to be substantially reduced, that the system is about to transition to a higher level of system

performance, or that a requirement for a specified holdover time can be relaxed. An example of a signal indicating a change in a system operational state is a signal indicating that a load current will change from a first current level to a second current level at or around a particular time. (Paragraph 0044 of the present application.)

In accordance with FIGURE 11, the present application continues that the servers SVR communicate with the power system controller PSC over respective server communication buses (designated "SVRBUS_1…SVRBUS_n" and also referred to as "SVRBUS") to communicate data to establish a system operational state with respect to the servers SVR. The data may include a processor P-state or C-state, a signal indicative of a level of system or power system functionality, and/or a signal anticipating a change in power system functionality. In a preferred embodiment, the various communication buses are serial data buses such as I2C buses (or any other suitable communication protocol). In an alternative embodiment, parallel buses can be used. (Paragraph 0093 of the present application.)

In accordance with FIGURE 3, the present application provides that a controller 311 may also respond to a signal indicating a system operational state S_{op_state}, which may be provided by a power system controller. (Paragraph 0058 of the present application.) The signal indicating a system operational state S_{op_state} is clearly different than an output voltage Vout supplied to the controller 311. (Paragraph 0055 of the present application.) In view of the foregoing, it appears that Jain fails to disclose a power converter controller configured to receive a signal from a load indicating a system operational state of the load and control an internal operating characteristic of the power converter as a function of the signal as recited in independent Claim 1 of the present application.

The Applicants, therefore, respectfully submit that independent Claim 1 of the present application, and the claims dependent thereon (including Claims 2, 3 and 5), are not anticipated by Jain and request that the Examiner remove the rejections thereto under 35 U.S.C. §102(b).

B. The Examiner has also rejected Claims 11-20 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent Publication No. 2007/0222463 to Qahouq, *et al.* ("Qahouq"). The Examiner believes that Qahouq discloses all of the limitations of independent Claims 11 and 16 of the present application including a power system controller configured to provide a signal (*i.e.*, Ve, FIGURE 1) to identify operation of a processor system in a state of power drain (*i.e.*, paragraph 0007-0009), and a power converter controller (*i.e.*, FIGURE 1, 124) configured to receive the signal from the power system controller (*i.e.*, paragraph 0007-0009), to sense a power level of the state of power drain in response to the signal (*i.e.*, Ve provides an indication of a power level at the output of the power converter), and to control an internal operating characteristic of the power converter as a function of the power level (*i.e.*, Vo, Ve and C1, C2, …CN are types of internal operating characteristics, 0008-0010). (Examiner's Office Action, pp. 4, 5.) The Applicants respectfully disagree.

FIGURE 1 of Qahouq illustrates a block diagram of an apparatus 100 and system 110 for power conversion efficiency management. The apparatus 100 includes measurement logic 114 to measure a feedback error signal change ΔFSe (*e.g.*, comprising an output voltage error change ΔVe) as an indication of efficiency in one or more power stages 118. The apparatus 100 also includes performance governor logic 122 coupled to the power stages 118, such that the performance governor logic 122 is used to select one or more determined power stage control parameter values C1, C2, . . . , CN to increase efficiency responsive to the feedback error signal

change ΔFSe. Examples of determined power stage control parameter values C1, C2, . . . , CN include selecting a particular switching frequency or switching dead time, selecting an input voltage or an output voltage, or selecting a number of active switches, or active power stages, among others. The measurement logic 114 and the performance governor logic 122 may form a portion of an adaptive controller 124. (Paragraph 0009.)

According to Qahouq, a control technique is disclosed that can be used to dynamically reduce power consumption by adaptively tracking the change in a feedback error signal. Here, the change in a feedback error signal is used as an indicator of efficiency (*i.e.*, as an increase or decrease in power loss when power is provided in various applications). By monitoring the feedback error signal change and using it as an indication of efficiency, the trend of power consumption and efficiency for the power stages 118 can be predicted. It is then possible to use the trend information to dynamically select proper control parameters or modify the existing mode of operation in order to reduce power loss, even in the face of adverse conditions, such as a non-constant input voltage, variable loading, and component parameter instability. (Paragraph 0010.)

The apparatus 100 of FIGURE 1 of Qahouq includes one or more gain compensators 130 to couple to the measurement logic 114, and to receive a reference voltage Vref. The apparatus 100 also includes one or more switching frequency controllers 134 coupled to the performance governor logic 122, and/or one or more input filters 138 coupled to the power stages 118. (Paragraph 0012.)

While it should be understood according to Qahouq that the feedback error signal change ΔFSe may comprise an error voltage change or an error current change, the example of an error

voltage change will be used for the balance of Qahouq to maintain simplicity. Thus, the reader should understand that the terms "voltage" and "current" can be used interchangeably throughout Qahouq. (Paragraph 0013.) Qahouq continues that monitoring the change in the error signal FSe, such as the output voltage error change ΔVe, may reveal additional information that indicates the conversion power loss in addition to the required duty cycle/conversion ratio (gain). This indication of efficiency, or power loss, can therefore be used to adaptively reduce power losses and increase efficiency. (Paragraph 0016.)

From the aforementioned description in accordance with FIGURE 1 of the reference, it is clear that Qahouq fails to disclose a power system, or method of operating the same, configured to provide a signal to identify operation of a processor system in a state of power drain, sense a power level of the state of power drain in response to the signal and control an internal operating characteristic of a power converter as a function of the power level as recited in ones of independent Claims 11 and 16 of the present application. Again, the controller 124 of Qahouq monitors the change in the error signal FSe, such as the output voltage error change ΔVe, of the power stages 118, and does not sense a power level of a state of power drain in response to a signal to identify operation of a processor system in the state of power drain.

As an example in the environment of the present application, a power converter controller (*e.g.*, a controller 311 of FIGURE 3) senses and is responsive to, among other things, an external signal V_{ext} indicating an environmental parameter from an external source such as a server powered by the power converter. (Paragraph 0056 of the present application.) In accordance therewith, the controller 311 is configured to augment the operating efficiency of the power converter in response to a sensed or signaled internal operating characteristic and/or an output

characteristic, a power converter parameter measured after a manufacturing step, and a signal from an external source representing an environmental parameter obtained from an external source such as a signal from a server being powered. (Paragraph 0057 of the present application.)

The controller 311 may also respond to a signal indicating a system operational state S_{op_state}, which may be provided by a power system controller, which may be constructed as a component of the load (for example and without restriction, as a power system controller described with reference to FIGURE 11 of the present application). (Paragraph 0058 of the present application.) Additionally, the power system controller can be configured to provide a signal to the power system to identify operation of the system in such a state of a maximum power drain. A power converter controller, such as the controller 311, can be configured to receive the signal from the power system controller, and to sense a power level of the system operating in such a state of maximum power drain. The power converter controller can then control a power converter topological state as a function of the sensed maximum power level, including an appropriate margin as necessary. (Paragraph 0059 of the present application.)

From the aforementioned description, it is clear that the power system, or method of operating the same, of one of independent Claims 11 and 16 of the present application is configured to receive different parameters to perform the intended functions as opposed to the controller 124 of Qahouq. While the controller 124 of Qahouq operates on an internally generated error signal, the power system, or method of operating the same, of one of independent Claims 11 and 16 of the present application is configured to be responsive to an externally generated signal from the power converter. The Applicants, therefore, respectfully submit that Claims 11 and 16 of the present application, and the claims dependent thereon (namely, Claims

12-15, and 16-20, respectively), are not anticipated by Qahouq and request that the Examiner remove the rejections thereto under 35 U.S.C. §102(b).

II. Rejections under 35 U.S.C. §103(a)

The Examiner has rejected Claims 4 and 6-10 under 35 U.S.C. 103(a) as being unpatentable over Jain in view of Qahouq. Beginning with Claim 4, for the reasons as set forth herein, Jain fails to teach or suggest all of the elements of independent Claim 1 of the present application. Thus, since Jain fails to teach or suggest all of the elements of independent Claim 1, and Qahouq fails to cure the deficiencies thereof, the Examiner cannot establish a *prima facie* case of obviousness of Claim 4, which depends from Claim 1. In view of the foregoing remarks, the cited references do not support the Examiner's rejection of Claim 4 under 35 U.S.C. §103(a). In accordance therewith, the Applicants respectfully request the Examiner withdraw the rejection.

Turning now to Claims 6-10, the Examiner believes that Jain discloses all of the limitations of the power system of independent Claim 6 of the present application with the exception of a power converter coupled to a processor system. The Examiner then cites Qahouq for the admitted deficiencies of Jain. (Examiner's Office Action, pp. 7-8.) The Applicants respectfully disagree.

For analogous reasons as provided above, the Applicants believe that Jain fails to disclose a power system controller configured to provide a signal characterizing a power requirement of a processor system and a power converter controller configured to receive a signal from the power system controller to control an internal operating characteristic of a power converter as a function of the signal as recited in independent Claim 6 of the present application. Again, the output

voltage V_o of Jain is a regulated DC voltage of lower value than the first DC voltage V_{DC} and within the desired voltage range for the particular specification of the power supply. Regulation of the output voltage V_o is accomplished in a conventional way. Preferably, feedback of the output voltage V_o from a node 62 is provided on a signal line 64, which is coupled to an input terminal 66 of a controller 68. An output terminal 70 of the controller 68 is coupled to a signal line 72, which in turn is coupled to a control node 56 of a FET switch 48. (Column 6, lines 4-17.) It appears to the Applicants that Jain is monitoring the output voltage of the power converter to control the same via a conventional feedback loop configuration. Thus, Jain operates on an internally generated feedback signal, whereas the power converter controller as recited in independent Claim 6 of the present application is configured to be responsive to an externally generated signal from the power converter.

For the reasons as set forth herein, the combination of Jain and Qahouq fail to teach or suggest the power system as recited in independent Claim 6 of the present application. Thus, since Jain and Qahouq fail to teach or suggest all of the elements of Claim 6, the Examiner cannot establish a *prima facie* case of obviousness of Claims 7-10, which depend from Claim 6. In view of the foregoing remarks, the cited references do not support the Examiner's rejection of Claims 6-10 under 35 U.S.C. §103(a). In accordance therewith, the Applicants respectfully request the Examiner withdraw the rejection.

III. Conclusion

In view of the foregoing remarks, the Applicants now see all of the claims currently pending in this application to be in condition for allowance and therefore earnestly solicit a Notice of Allowance therefor.

The Applicants request that the Examiner telephone the undersigned attorney of record at (972) 732-1001 if such would further expedite the prosecution of the present application. In the event the enclosed fees are insufficient, the Commissioner is hereby authorized to charge any additional fees, or credit any overpayments, to Deposit Account No. 50-1065.

Respectfully submitted,

June 20, 2011
Date

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 1 of 3

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Application Number	12/709,795
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Art Unit	2838
Examiner Name	Yemane Mehari
Attorney Docket Number	CDW-011CP1CP1C1

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	1	US-4,962,354	10-09-1990	Visser, et al.	
	2	US-5,959,850	09-28-1999	Lim	
	3	US-6,069,798	05-30-2000	Liu	
	4	US-6,325,035 B1	12-04-2001	Codina, et al.	
	5	US-6,373,727 B1	04-16-2002	Hedenskog, et al.	
	6	US-2003/0026115 A1	02-06-2003	Miyazaki	
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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Examiner Name	Yemane Mehari
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	19	US-2010/0149838	06-17-2010	Artusi et al.	
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	26	US-2011/0134664 A1	06-09-2011	Berghegger	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] - Number[4] - Kind Code[5] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1]Applicant's unique citation designation number (optional). [2]See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3]Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6]Applicant is to place a check mark here if English language Translation is attached.

PTO/SB/08b (01-08)
Approved for use through 06/30/2008. OMB 0651-0031
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Substitute for form 1449B/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 3 of 3

	Complete if Known
Application Number	12/709,795
Filing Date	02-22-2010
First Named Inventor	Artusi
Art Unit	2838
Examiner Name	Yemane Mehari
Attorney Docket Number	CDW-011CP1CP1C1

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	27	Freescale Semiconductor, "Design of a Digital AC/DC SMPS using the 56F8323 Device, Designer Reference Manual, 56800E 16-bit Digital Signal Controllers", DRM074, Rev. 0, August 2005 (108 pages).	
	28	Freescale Semiconductor, "56F8323 Evaluation Module User Manual, 56F8300 16-bit Digital Signal Controllers", MC56F8323EVMUM, Rev. 2, July 2005 (72 pages).	
	29	Freescale Semiconductor, "56F8323/56F8123 Data Sheet Preliminary Technical Data, 56F8300 16-bit Digital Signal Controllers," MC56F8323 Rev. 17, April 2007 (140 pages).	

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.
[1]Applicant's unique citation designation number (optional). [2]Applicant is to place a check mark here if English language Translation is attached.
This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/709,795	02/22/2010	Daniel A. Artusi	CDW-011CP1CP1C1	7439

25962 7590 03/18/2011

SLATER & MATSIL, L.L.P.
17950 PRESTON RD, SUITE 1000
DALLAS, TX 75252-5793

EXAMINER	
MEHARI, YEMANE	
ART UNIT	PAPER NUMBER
2838	

NOTIFICATION DATE	DELIVERY MODE
03/18/2011	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docketing@slater-matsil.com

Office Action Summary	Application No.	Applicant(s)	
	12/709,795	ARTUSI ET AL.	
	Examiner	Art Unit	
	YEMANE MEHARI	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 February 2011*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 February 2010* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/21/2010*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Summary

1. This office action is in response to the response filed on 12/20/2010.

2. Claims 1-20 are pending and have been examined.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-3 & 5 are rejected under 35 U.S.C. 102(b) as being anticipated by Jain et al. (US 6,344,986 B1).

In re to claim 1, Jain et al. disclose a power converter (i.e. 22, fig. 1, col. 5, lines 5-10) coupled to a load (i.e. 54), comprising: a power switch (i.e. 48) configured to conduct for a duty cycle to provide an output characteristic at an output thereof (i.e. col. 6, lines 11-24); and a power converter controller (i.e. 68) configured to receive a signal (i.e. 64) from said load indicating a system operational state of said load and control an internal operating characteristic of said power converter as a function of said signal (i.e. such as input and output voltage are examples of internal operating characteristics, col. 6, lines 11-59).

In re to claim 2, Jain et al. disclose the power converter (i.e. 22, fig. 1, col. 5, lines 5-10) as recited in claim 1, wherein said power converter controller (i.e. 68) is further configured to provide another signal (i.e. 72) to control said duty cycle of said power switch (i.e. 48) as a

function of said output characteristic and in accordance with said signal (i.e. such as input and output voltage are examples of internal operating characteristics, col. 5, lines 48-52 and col. 6, lines 11-24).

In re to claim 3, Jain et al. disclose the power converter (i.e. 22, fig. 1, col. 5, lines 5-10) as recited in claim 1, wherein said power converter controller (i.e. 68) is configured to adjust said internal operating characteristic (i.e. such as signals 72 and voltage across node 24, fig. 1) over a period of time (i.e. col. 6, lines 11-59).

In re to claim 5, Jain et al. disclose the power converter (i.e. 22, fig. 1, col. 5, lines 5-10) as recited in claim 1, wherein said internal operating characteristic is selected from the group consisting of: a gate drive voltage level (i.e. 72, fig. 1) of said power switch (i.e. 48, fig. 1) of said power converter (i.e. 22, fig. 1), a switching frequency of said power converter (i.e. see col. 3, lines 57-61 and col. 7, lines 12-23), and an internal direct current bus voltage of said power converter (i.e. see col. 7, lines 36-43).

5. Claims 11-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Qahouq et al. (US 2007/0222463 A1).

In re to claim 11, Qahouq et al. disclose a power system (i.e. 100, fig. 1, [0009]), comprising: a power system controller (i.e. 124, fig. 1) configured to enable operation of components of a processor system (i.e. 154, fig. 1) to establish a state of power drain thereof (i.e. Vo supply to 154, fig. 1), said power system controller configured to provide a signal (i.e. Ve, fig. 1) to identify operation of said processor system in said state of power drain (i.e. see [0007-0009]);

and a power converter (i.e. 118), coupled to said processor system, comprising a power converter controller (i.e. 124, fig. 1) configured to receive said signal from said power system controller (i.e. see [0009]), to sense a power level of said state of power drain in response to said signal (i.e. Ve provides indication of power level at the output of the power converter, [0009]), and to control an internal operating characteristic of said power converter as a function of said power level (i.e. Vo, Ve and C1, C2…CN are types of internal operating characteristics [0008-0010]).

In re to claim 12, Qahouq et al. disclose the power system (i.e. 100, fig. 1, [0009]) as recited in claim 11, wherein said power converter (i.e. 22) further comprises a power switch (i.e. 146) configured to conduct for a duty cycle to provide an output characteristic at an output thereof (i.e. [0016]), said power converter controller further configured to control said duty cycle of said power switch dependent on said output characteristic and in accordance with said power level (i.e. see [0016]).

In re to claim 13, Qahouq et al. disclose the power system (i.e. 100, fig. 1, [0009]) as recited in claim 11, wherein said signal is provided upon startup of said processor system (i.e. [0022]).

In re to claim 14, Qahouq et al. disclose the power system (i.e. 100, fig. 1, [0009]) as recited in claim 11 wherein said power converter controller (i.e. 124, fig. 1) is configured to adjust said internal operating characteristic over a period of time (i.e. see [0029]).

In re to claim 15, Qahouq et al. disclose the power system (i.e. 100, fig. 1, [0009]) as recited in claim 11, wherein said internal operating characteristic is selected from the group consisting of: a gate drive voltage level (i.e. 142, fig. 1) of a power switch (i.e. 146, fig. 1) of said power converter (i.e. 118, fig. 1), a switching frequency of said power converter (i.e. see [0009]), and an internal direct current bus voltage of said power converter (i.e. see [0013 & 0032]).

In re to claim 16, Qahouq et al. disclose a method of operating a power system (i.e. 100, fig. 1, [0009]), comprising: enabling operation of components of a processor system (i.e. 154, fig. 1) to establish a state of power drain thereof (i.e. Vo supply to 154, fig. 1); providing a signal (i.e. Ve, fig. 1) to identify operation of said processor system in said state of power drain (i.e. see [0007-0009]); sensing a power level of said state of power drain in response to said signal (i.e. Ve provides indication of power level at the output of the power converter, [0009]); and controlling an internal operating characteristic of a power converter as a function of said power level (i.e. Vo, Ve and C1, C2…CN are types of internal operating characteristics [0008-0010].

In re to claim 17, Qahouq et al. disclose a method of operating a power system (i.e. 100, fig. 1, [0009]) as recited in claim 16, further comprising: inducing a power switch (i.e. 146, fig. 1) of said power converter (i.e. 118, fig. 1) to conduct for a duty cycle to provide an output characteristic at an output thereof and controlling said duty cycle of said power switch dependent on said output characteristic and in accordance with said power level (i.e. see Abstract and [0016]);.

In re to claim 18, Qahouq et al. disclose a method of operating a power system (i.e. 100, fig. 1, [0009]) as recited in claim 16 wherein said signal is provided upon startup of said processor system (i.e. [0022]).

In re to claim 19, Qahouq et al. disclose a method of operating a power system (i.e. 100, fig. 1, [0009]) as recited in claim 16, wherein said controlling said internal operating characteristic comprises occurs over a period of time (i.e. see [0029]).

In re to claim 20, Qahouq et al. disclose a method of operating a power system (i.e. 100, fig. 1, [0009]) as recited in claim 16, wherein said internal operating characteristic is selected from the

group consisting of (i.e. Vo, Ve and C1, C2…CN are types of internal operating characteristics [0008-0010]): a gate drive voltage level of a power switch of said power converter (i.e. 118, fig. 1), a switching frequency of said power converter (i.e. see [0009]),, and an internal direct current bus voltage of said power converter (i.e. Refer to paragraph 0007-0010).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 4 & 6-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jain et al. (US 6,344,986 B1) in view of Qahouq et al. (US 2007/0222463 A1).

In re to claim 4, Jain et al. disclose the power converter (i.e. 22, fig. 1, col. 5, lines 5-10) as recited in claim 1. Except, Jain et al. fail to disclose wherein said load is a processor and said system operational state is dependent on one of a core state and a performance state of said processor.

However, Qahouq et al. disclose a load is a processor (i.e. 154, fig. 1) and said system operational state is dependent on one of a core state and a performance state of said processor (i.e. core state and performance state are processor state indicators, 154 comprises a processor 148, fig. 1 [0021-0022]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the power converter of Jain et al. to include a load is a processor as taught by Qahouq et al., because it help in enhancing the efficiency of the power converter.

Additionally, since Jain et al. and Qahouq et al., are both from the same field of endeavor, the purpose disclosed by Qahouq et al. would have been recognized in the pertinent art of Jain et al.

In re to claim 6, Jain et al. disclose a power system (i.e. fig. 1, col. 4, lines 18-20), comprising: a power system controller (i.e. 68) configured to provide a signal (i.e. 72) characterizing a power requirement (i.e. col. 6, lines 11-24): a power switch (i.e. 48) configured to conduct for a duty cycle to provide an output characteristic at an output thereof (i.e. col. 6, lines 11-24), and a power converter controller (i.e. 68 is also a controller for converter 22, fig. 1) configured to receive a signal (i.e. 72) from said power system controller to control an internal operating characteristic of said power converter as a function of said signal (i.e. col. 6, lines 11-59). Except, Jain et al. fail to disclose a processor system; and a power converter coupled to said processor system.

However, Qahouq et al. disclose a processor system (i.e. 154, fig. 1) and a power converter (i.e. 118) coupled to said processor system processor (i.e. [0021-0022]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the power converter of Jain et al. to include a processor system as taught by Qahouq et al., because it help in enhancing the efficiency of the power converter.

Additionally, since Jain et al. and Qahouq et al., are both from the same field of endeavor, the purpose disclosed by Qahouq et al. would have been recognized in the pertinent art of Jain et al.

In re to claim 7, Jain et al. disclose a power system (i.e. fig. 1, col. 4, lines 18-20) as recited in claim 6, wherein said power converter controller (i.e. 68) is further configured to provide another signal (i.e. the controller 68 supplies varying signals through he signaling medium 72 to switch 48) to control said duty cycle of said power switch as a function of said output characteristic (i.e. 64) and in accordance with said signal (i.e. col. 6, lines 11-59).

In re to claim 8, Jain et al. disclose a power system (i.e. fig. 1, col. 4, lines 18-20) as recited in claim 6, wherein said power converter controller (i.e. 68) is configured to adjust said internal operating characteristic (i.e. such as signals 72 and voltage across node 24, fig. 1) over a period of time (i.e. col. 6, lines 11-59).

In re to claim 9, Jain et al. disclose a power system (i.e. fig. 1, col. 4, lines 18-20) as recited in claim 6. Except, Jain et al. fail to disclose wherein said power requirement of a processor system is dependent on one of a core state and a performance state of said processor system.

However, Qahouq et al. disclose power requirement of a processor system (i.e. 154, fig. 1) is dependent on one of a core state and a performance state of said processor system (i.e., core state and performance state are processor state indicators, 154 comprises a processor 148, fig. 1 [0021-0022]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the power converter of Jain et al. to include a processor system as taught by Qahouq et al., because it help in enhancing the efficiency of the power converter.

Additionally, since Jain et al. and Qahouq et al., are both from the same field of endeavor, the purpose disclosed by Qahouq et al. would have been recognized in the pertinent art of Jain et al.

In re to claim 10, Jain et al. disclose a power system (i.e. fig. 1, col. 4, lines 18-20) as recited in claim 6 wherein said internal operating characteristic is selected from the group consisting of:a gate drive voltage level (i.e. level of 72, fig. 1) of said power switch (i.e. 48, fig. 1) of said power converter (i.e. 22, fig. 1), a switching frequency of said power converter (i.e. see col. 3, lines 57-61 and col. 7, lines 12-23), and an internal direct current bus voltage of said power converter (i.e. voltage across node 24, fig. 1, col. 7, lines 36-43).

Examiner Notes

39. Examiner cites particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings in the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested that, in preparing responses, the applicant fully consider the references in its entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the examiner.

Contact Information

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to YEMANE MEHARI whose telephone number is (571)270-7603. The examiner can normally be reached on Monday to Thursday, 8-AM to 5-PM, EST. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Monica

Lewis can be reached on (571)272-1838. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Monica Lewis/
Supervisory Patent Examiner, Art Unit 2838

/YM/

Notice of References Cited	Application/Control No. 12/709,795	Applicant(s)/Patent Under Reexamination ARTUSI ET AL.	
	Examiner YEMANE MEHARI	Art Unit 2838	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,344,986 B1	02-2002	Jain et al.	363/89
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

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	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
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	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

PTO/SB/08a (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 5

Complete if Known	
Application Number	12/709,795
Filing Date	2/22/2010
First Named Inventor	Artusi et al.
Art Unit	2838
Examiner Name	Mehari, Yemane
Attorney Docket Number	CDW-011CP1CP1C1

U.S. PATENT DOCUMENTS

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	1	US-2006/0006976 Al	01-12-2006	Bruno	
	2	US-2006/0109698 A1	05-25-2006	Qu	
	3	US-2007/0007945 A1	01-11-2007	King, et al.	
	4	US-2007/0159857 A1	07-12-2007	Lee	
	5	US-2008/0111657 A1	05-15-2008	Mehrotra, et al.	
	6	US-2008/0150666 A1	06-26-2008	Chandrasekaran, et al.	
	7	US-2008/0224812 A1	09-18-2008	Chandrasekaran	
	8	US-2008/0232141 A1	09-25-2008	Artusi, et al.	
	9	US-2008/0310190 A1	12-18-2008	Chandrasekaran, et al.	
	10	US-2009/0097290 A1	04-16-2009	Chandrasekaran	
	11	US-2010/0091522 A1	04-15-2010	Chandrasekaran, et al.	
	12	US-2010/0182806 A1	07-22-2010	Garrity, et al.	
	13	US-2010/0188876 A1	07-29-2010	Garrity, et al.	
	14	US-3,346,798	10-10-1967	Dinger	
	15	US-3,484,562	12-16-1969	Kronfeld	
	16	US-4,257,087	03-17-1981	Cuk	
	17	US-4,770,667	09-13-1988	Evans, et al.	
	18	US-4,770,668	09-13-1988	Skoultchi, et al.	

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	19	EP 0 665 634 A1	01-31-1994	Siemens AG		
	20	WO 2010/083514 A1	07-22-2010	Flextronics International USA, Inc., et al.		
	21	WO 2010/114914 A1	10-07-2010	Chandrasekaran		
	22	WO 2010/083511 A1	07-22-2010	Flextronics International USA, Inc., et al.		

Examiner Signature	/Yemane Mehari/	Date Considered	03/03/2011

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /Y.M./

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Sheet 2 of 5

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Examiner Name	Mehari, Yemane
Attorney Docket Number	CDW-011CP1CP1C1

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Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1]Applicant's unique citation designation number (optional). [2]See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3]Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6]Applicant is to place a check mark here if English language Translation is attached.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 5 of 5

Complete if Known	
Application Number	12/709,795
Filing Date	2/22/2010
First Named Inventor	Artusi et al.
Art Unit	2838
Examiner Name	Mehari, Yemane
Attorney Docket Number	CDW-011CP1CP1C1

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	73	CHHAWCHHARIA, P., et al., "On the Reduction of Component Count in Switched Capacitor DC/DC Convertors," Hong Kong Polytechnic University, IEEE, 1997, Hung Hom, Kowloon, Hong King, pages 1395-1401.	
	74	KUWABARA, K., et al., "Switched-Capacitor DC – DC Converters," Fujitsu Limited, IEEE, 1988, Kawasaki, Japan, pages 213-218.	
	75	MAXIM, Application Note 725, www.maxim-ic.com/an725, Maxim Integrated Products, November 29, 2001, 8 pages.	
	76	NATIONAL SEMICONDUCTOR CORPORATION, "LMC7660 Switched Capacitor Voltage Converter," www.national.com, April 1997, 12 pages.	
	77	NATIONAL SEMICONDUCTOR CORPORATION, "LM2665 Switched Capacitor Voltage Converter," www.national.com, September 2005, 9 pages.	
	78	TEXAS INSTRUMENTS INCORPORATED, "LT1054, LT1054Y Switched-Capacitor Voltage Converters With Regulators," SLVS033C, February 1990 – Revised July 1998, 25 pages.	
	79	VALLAMKONDA, S., "Limitations of Switching Voltage Regulators," A Thesis in Electrical Engineering, Texas Tech University, May 2004, 89 pages.	
	80	XU, M., et al., "Voltage Divider and its Application in the Two-stage Power Architecture," Center for Power Electronics Systems, Virginia Polytechnic Institute and State University, IEEE, 2006, Blacksburg, Virginia, pages 499-505.	
	81	Freescale Semiconductor, "Implementing a Digital AC/DC Switched-Mode Power Supply using a 56F8300 Digital Signal Controller," Application Note AN3115, August 2005, 24 pp., Chandler, AZ.	

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.
[1]Applicant's unique citation designation number (optional). [2]Applicant is to place a check mark here if English language Translation is attached.
This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Artusi, *et al.*	Docket No.:	CDW-011CP1CP1C1
Serial No.:	12/709,795	Art Unit:	2838
Filed:	February 22, 2010	Examiner:	Mehari, Yemane
For:	Power System with Power Converter Having an Adaptive Controller		

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT UNDER 37 CFR §1.111

Dear Sir:

The following amendments and remarks are presented in response to the Examiner's Office Action mailed September 20, 2010. Please amend the above-referenced application as follows. No new matter has been added.

IN THE SPECIFICATION:

Please amend paragraph 80 as set forth below.

[0080] The number of different relationships that could be measured and data points collected is limited only by the ingenuity of the test engineer, time, and data memory resources. Over many such projects, an engineer may learn that certain relationship data has more of an impact on efficiency than others, and may learn how to intelligently limit the number of tests performed and data points collected to only those relationships having the greatest ~~affect~~effect on efficiency.

IN THE CLAIMS:

1. (Original) A power converter coupled to a load, comprising:

a power switch configured to conduct for a duty cycle to provide an output characteristic at an output thereof; and

a power converter controller configured to receive a signal from said load indicating a system operational state of said load and control an internal operating characteristic of said power converter as a function of said signal.

2. (Original) The power converter as recited in Claim 1 wherein said power converter controller is further configured to provide another signal to control said duty cycle of said power switch as a function of said output characteristic and in accordance with said signal.

3. (Original) The power converter as recited in Claim 1 wherein said power converter controller is configured to adjust said internal operating characteristic over a period of time.

4. (Original) The power converter as recited in Claim 1 wherein said load is a processor and said system operational state is dependent on one of a core state and a performance state of said processor.

5. (Original) The power converter as recited in Claim 1 wherein said internal operating characteristic is selected from the group consisting of:

a gate drive voltage level of said power switch of said power converter,

a switching frequency of said power converter, and

an internal direct current bus voltage of said power converter.

6. (Original) A power system, comprising:

a power system controller configured to provide a signal characterizing a power

requirement of a processor system; and

a power converter coupled to said processor system, comprising:

a power switch configured to conduct for a duty cycle to provide an output characteristic at an output thereof, and

a power converter controller configured to receive a signal from said power system controller to control an internal operating characteristic of said power converter as a function of said signal.

7. (Original) The power system as recited in Claim 6 wherein said power converter controller is further configured to provide another signal to control said duty cycle of said power switch as a function of said output characteristic and in accordance with said signal.

8. (Original) The power system as recited in Claim 6 wherein said power converter controller is configured to adjust said internal operating characteristic over a period of time.

9. (Original) The power system as recited in Claim 6 wherein said power requirement of a processor system is dependent on one of a core state and a performance state of said processor system.

10. (Original) The power system as recited in Claim 6 wherein said internal operating characteristic is selected from the group consisting of:

a gate drive voltage level of said power switch of said power converter,

a switching frequency of said power converter, and

an internal direct current bus voltage of said power converter.

11. (Original) A power system, comprising:

a power system controller configured to enable operation of components of a processor system to establish a state of power drain thereof, said power system controller configured to

provide a signal to identify operation of said processor system in said state of power drain; and

a power converter, coupled to said processor system, comprising a power converter controller configured to receive said signal from said power system controller, to sense a power level of said state of power drain in response to said signal, and to control an internal operating characteristic of said power converter as a function of said power level.

12. (Original) The power system as recited in Claim 11 wherein said power converter further comprises a power switch configured to conduct for a duty cycle to provide an output characteristic at an output thereof, said power converter controller further configured to control said duty cycle of said power switch dependent on said output characteristic and in accordance with said power level.

13. (Original) The power system as recited in Claim 11 wherein said signal is provided upon startup of said processor system.

14. (Original) The power system as recited in Claim 11 wherein said power converter controller is configured to adjust said internal operating characteristic over a period of time.

15. (Original) The power system as recited in Claim 11 wherein said internal operating characteristic is selected from the group consisting of:

a gate drive voltage level of a power switch of said power converter,

a switching frequency of said power converter, and

an internal direct current bus voltage of said power converter.

16. (Original) A method of operating a power system, comprising:

enabling operation of components of a processor system to establish a state of power drain thereof;

providing a signal to identify operation of said processor system in said state of power

drain;

sensing a power level of said state of power drain in response to said signal; and

controlling an internal operating characteristic of a power converter as a function of said power level.

17. (Original) The method as recited in Claim 16, further comprising:

inducing a power switch of said power converter to conduct for a duty cycle to provide an output characteristic at an output thereof; and

controlling said duty cycle of said power switch dependent on said output characteristic and in accordance with said power level.

18. (Original) The method as recited in Claim 16 wherein said signal is provided upon startup of said processor system.

19. (Original) The method as recited in Claim 16 wherein said controlling said internal operating characteristic comprises occurs over a period of time.

20. (Original) The method as recited in Claim 16 wherein said internal operating characteristic is selected from the group consisting of:

a gate drive voltage level of a power switch of said power converter,

a switching frequency of said power converter, and

an internal direct current bus voltage of said power converter.

REMARKS

The Applicants have carefully considered this application in connection with the Examiner's Office Action and respectfully request reconsideration of this application in view of the following remarks.

The Applicants originally submitted Claims 1-20 in the application, and no claims have been amended, added or cancelled herein. Accordingly, Claims 1-20 are currently pending in the application.

I. Double Patenting

The Examiner has rejected Claims 1, 2, 4, 6, 7, 9, 11-13 and 16-18 on the ground of nonstatutory obviousness-type double patenting as being unpatentable over Claims 1, 6, 11 and 16 of U.S. Patent No. 7,667,986 to Artusi, *et al.* ("Artusi"). The Examiner has also rejected Claims 3, 5, 8, 10, 14, 15, 19 and 20 on the ground of nonstatutory obviousness-type double patenting as being unpatentable over Claims 3, 5, 8, 10, 14, 15, 19 and 20 of Artusi in view of U.S. Patent Publication No. 2007/0222463 to Qahouq, *et al.* ("Qahouq"). Although the Applicants do not necessarily agree with the Examiner's position, the Applicants have filed a Terminal Disclaimer herewith directed to U.S. Patent No. 7,667,986 in compliance with 37 CFR §1.321 to overcome the Examiner's rejection thereto.

II. Conclusion

In view of the foregoing amendments and remarks, the Applicants now see all of the claims currently pending in this application to be in condition for allowance and therefore earnestly solicit a Notice of Allowance therefor.

The Applicants request that the Examiner telephone the undersigned attorney of record at (972) 732-1001 if such would further expedite the prosecution of the present application. In the event the enclosed fees are insufficient, the Commissioner is hereby authorized to charge any additional fees, or credit any overpayments, to Deposit Account No. 50-1065.

Respectfully submitted,

December 20, 2010
Date

/Glenn W. Boisbrun/
Glenn W. Boisbrun
Attorney for Applicants
Reg. No. 39,615

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Tel. 972-732-1001
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PTO/SB/26 (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT	Docket Number (Optional) CDW-011CP1CP1C1

In re Application of: Artusi, et al.

Application No.: 12/709,795

Filed: 2/22/2010

For: Power System with Power Converters Having an Adaptive Controller

The owner*, Flextronic International USA, Inc., of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term **prior patent** No. 7,667,986 as the term of said prior patent is defined in 35 U.S.C. 154 and 173, and as the term of said **prior patent** is presently shortened by any terminal disclaimer. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the **prior patent** are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the owner does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term as defined in 35 U.S.C. 154 and 173 of the **prior patent**, "as the term of said **prior patent** is presently shortened by any terminal disclaimer," in the event that said **prior patent** later:

expires for failure to pay a maintenance fee;
is held unenforceable;
is found invalid by a court of competent jurisdiction;
is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
has all claims canceled by a reexamination certificate;
is reissued; or
is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

Check either box 1 or 2 below, if appropriate.

1. ☐ For submissions on behalf of a business/organization (e.g., corporation, partnership, university, government agency, etc.), the undersigned is empowered to act on behalf of the business/organization.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

2. ☒ The undersigned is an attorney or agent of record. Reg. No. 39,615

/Glenn W. Boisbrun/ — Signature
December 20, 2010 — Date

Glenn W. Boisbrun — Typed or printed name

972-732-1001 — Telephone Number

☒ Terminal disclaimer fee under 37 CFR 1.20(d) included.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

*Statement under 37 CFR 3.73(b) is required if terminal disclaimer is signed by the assignee (owner).
Form PTO/SB/96 may be used for making this certification. See MPEP § 324.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/709,795	02/22/2010	Daniel A. Artusi	CDW-011CP1CP1C1	7439

25962 7590 09/20/2010

SLATER & MATSIL, L.L.P.
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DALLAS, TX 75252-5793

EXAMINER	
MEHARI, YEMANE	
ART UNIT	PAPER NUMBER
2838	

NOTIFICATION DATE	DELIVERY MODE
09/20/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docketing@slater-matsil.com

Office Action Summary	Application No.	Applicant(s)	
	12/709,795	ARTUSI ET AL.	
	Examiner	Art Unit	
	YEMANE MEHARI	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 February 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 February 2010* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *04/16/2010*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Summary

1. This office action is in response to the continuation of application 12/051,334 filed on 02/22/2010.

2. Claims 1-20 are pending and have been examined.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In *re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 1, 2, 4, 6, 7, 9, 11, 12, 13, 16, 17 & 18 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1, 6, 11 & 16 of U.S. 7,667,986.

In re to claim 1, claim 1 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 7,667,986. Although the conflicting claims are not identical, they are not patentably distinct from each other because replacing the term or limitation "enable a power converter topological state as a function of said

signal." of US patent number 7,667,986 with the term or limitation "control an internal operating characteristic of said power converter as a function of said signal" on the current application 12/709,795, does not change the content of the claim. Although, application 12/709,795 does not specifically disclose "enable a power converter topological state as a function of said signal", the internal operating characteristic of the power converter is the same as the topological state of the power converter. Both phrases are referring to the internal make up or mechanism of the power converter. Therefore, a mare wording change is not sufficient to patently distinguish claim 1 of application No. 12/709,795 over claim 1 of the parent patent No. US 7,667,986. Below is the comparison of claim 1 of the application No. 12/709,795 and the parent patent (US 7,667.986):-

Claim No.	App. No. 12/709,795	App. No. 12/051,334 (US 7,667.986)
1	A power converter coupled to a load, comprising: a power switch configured to conduct for a duty cycle to provide an output characteristic at an output thereof; and a power converter controller configured to receive a signal from said load indicating a system operational state of said load and **control an internal operating characteristic of said power converter** as a function of said signal.	A power converter coupled to a load, comprising: a power switch configured to conduct for a duty cycle to provide an output characteristic at an output thereof; and a power converter controller configured to receive a signal from said load indicating a system operational state of said load and **enable a power converter topological state** as a function of said signal.

In re to claim 2, claim 2 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 2 of US patent No. 7,667,986.

In re to claim 4, claim 4 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 4 of US patent No. 7,667,986.

In re to claim 6, claim 6 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 6 of U.S. Patent No. 7,667,986. Although the conflicting claims are not identical, they are not patentably distinct from each other because replacing the term or limitation "enter a power converter topological state dependent on said signal." of US patent number 7,667,986 with the term or limitation "control an internal operating characteristic of said power converter as a function of said signal." on the current application 12/709,795, does not change the content of the claim. Although, application 12/709,795 does not specifically disclose "enable a power converter topological state as a function of said signal", the internal operating characteristic of the power converter is inherently the same as the topological state of the power converter. Both phrases are referring to the internal make up or mechanism of the power converter. Therefore, a mare wording change is not sufficient to patently distinguish claim 6 of application No. 12/709,795 over claim 6 of the parent patent No. US 7,667,986. Below is the comparison of claim 1 of the application No. 12/709,795 and the parent patent (US 7,667.986):-

Claim NO.	12/709,795	12/051,334 (US 7,667.986)
6	A power system, comprising: a power system controller configured to provide a signal characterizing a power requirement of a processor system; and a power converter coupled to said processor system, comprising: a power switch configured to conduct for a duty cycle to provide an output characteristic at an output thereof, and a power converter controller configured to receive a signal from said power system controller to **control an internal operating characteristic of said power converter as a function of** said signal.	A power system, comprising: a power system controller configured to provide a signal characterizing a power requirement of a processor system; and a power converter coupled to said processor system, comprising: a power switch configured to conduct for a duty cycle to provide an output characteristic at an output thereof, and a power converter controller configured to receive said signal from said power system controller to **enter a power converter topological state dependent on** said signal.

In re to claim 7, claim 7 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 7 of US patent No. 7,667,986.

In re to claim 9, claim 9 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 9 of US patent No. 7,667,986.

In re to claim 11, claim 11 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 11 of U.S. Patent No. 7,667,986. Although the conflicting claims are not identical, they are not patentably distinct from each other because replacing the term or limitation "and to control a power converter topological state as a function of said power level." of US patent number 7,667,986 with the term or limitation "and to control an internal operating characteristic of said power converter as a function of said power level." on the current application 12/709,795, does not change the content of the claim. Although, application 12/709,795 does not specifically disclose "enable a power converter topological state as a function of said signal", the internal operating characteristic of the power converter is inherently the same as the topological state of the power converter. Both phrases are referring to the internal make up or mechanism of the power converter. Therefore, a mare wording change is not sufficient to patently distinguish claim 11 of application No. 12/709,795 over claim 11 of the parent patent No. US 7,667,986. Below is the comparison of claim 1 of the application No. 12/709,795 and the parent patent (US 7,667.986):-

Claim NO.	12/709,795	12/051,334 (US 7,667.986)

11	A power system, comprising: a power system controller configured to enable operation of components of a processor system to establish a state of power drain thereof, said power system controller configured to provide a signal to identify operation of said processor system in said state of power drain; and a power converter, coupled to said processor system, comprising a power converter controller configured to receive said signal from said power system controller, to sense a power level of said state of power drain in response to said signal, and to control **an internal operating characteristic of said power converter** as a function of said power level.	A power system, comprising: a power system controller configured to enable operation of components of a processor system to establish a state of power drain thereof, said power system controller configured to provide a signal to identify an operation of said processor system in said state of power drain; and a power converter, coupled to said processor system, comprising a power converter controller configured to receive said signal from said power system controller, to sense a power level of said state of power drain in response to said signal, and to control **a power converter topological state** as a function of said power level.

In re to claim 12, claim 12 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 12 of US patent No. 7,667,986.

In re to claim 13, claim 13 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 13 of US patent No. 7,667,986.

In re to claim 16, claim 16 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 16 of U.S. Patent No. 7,667,986. Although the conflicting claims are not identical, they are not patentably distinct from each other because replacing the term or limitation "controlling a power converter topological state of a power converter as a function of said power level." of US patent number 7,667,986 with the term or limitation "and to control an internal operating characteristic of said power converter as a function of said power level." on the current application 12/709,795, does not change the content of the claim. Although, application 12/709,795 does not specifically disclose "controlling a power converter topological state of a power converter as a function of said power level", the

internal operating characteristic of the power converter is inherently the same as the topological state of the power converter. Both phrases are referring to the internal make up or mechanism of the power converter. Therefore, a mare wording change is not sufficient to patently distinguish claim 16 of application No. 12/709,795 over claim 16 of the parent patent No. US 7,667,986.

Claim NO.	12/709,795	12/051,334 (US 7,667.986)
16	A method of operating a power system, comprising: enabling operation of components of a processor system to establish a state of power drain thereof; providing a signal to identify operation of said processor system in said state of power drain; sensing a power level of said state of power drain in response to said signal; and controlling **an internal operating characteristic of a power converter** as a function of said power level.	A method of operating a power system, comprising: enabling operation of components of a processor system to establish a state of power drain thereof; providing a signal to identify an operation of said processor system in said state of power drain; sensing a power level of said state of power drain in response to said signal; and controlling **a power converter topological state of a power converter** as a function of said power level.

In re to claim 17, claim 17 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 17 of US patent No. 7,667,986.

In re to claim 18, claim 18 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 18 of US patent No. 7,667,986.

5. Claims 3, 5, 8, 10, 14, 15, 19 & 20 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 3, 5, 8, 10, 14, 15, 19 & 20 of Artusi et al. (U.S. 7,667,986 B2) in view of Qahouq et al. (US 2007/0222463 A1).

In re to claim 3, Artusi et al. disclose the power converter (i.e. 100, fig 1) as recited in claim 1. Except, Artusi et al. fails to disclose wherein said power converter controller is further configured to adjust internal operating characteristic over a period of time.

However, Qahouq et al. disclose, wherein said power converter controller (i.e. 124, fig 1, [0009]) is further configured to adjust internal operating characteristic over a period of time. (Refer to paragraphs [0007 & 0009])

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the power converter of Artusi et al. to include method of adjusting internal operating characteristic as taught by Qahouq et al., because it help in enhancing the efficiency of the power converter.

Additionally, since Artusi et al. and Qahouq et al., are both from the same field of endeavor, the purpose disclosed by Qahouq et al. would have been recognized in the pertinent art of Artusi et al.

In re to claim 5, Artusi et al. disclose, the power converter (i.e. 118, fig 1) as recited in claim 1 Except, Artusi et al. fails to disclose, wherein said internal operating characteristic is selected from the group consisting of: a gate drive voltage level of said power switch of said power converter, a switching frequency of said power converter, and an internal direct current bus voltage of said power converter. (i.e. Refer to paragraph 0007-0010).

However, Qahouq et al. disclose, wherein said internal operating characteristic is selected from the group consisting of: a gate drive voltage level of said power switch of said power converter, a switching frequency of said power converter, and an internal direct current bus voltage of said power converter. (i.e. Refer to paragraph 0007-0010).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the power converter of Artusi et al. to include method of adjusting internal operating characteristic as taught by Qahouq et al., because it help in enhancing the efficiency of the power converter.

Additionally, since Artusi et al. and Qahouq et al., are both from the same field of endeavor, the purpose disclosed by Qahouq et al. would have been recognized in the pertinent art of Artusi et al.

In re to claim 8, Artusi et al. disclose, the power system (i.e. 100, fig 1) as recited in claim 6. Except, Artusi et al. fails to disclose wherein said power converter controller is further configured to adjust internal operating characteristic over a period of time.

However, Qahouq et al. disclose, wherein said power converter controller (i.e. 124, fig 1, [0009]) is further configured to adjust internal operating characteristic over a period of time. (Refer to paragraphs [0007 & 0009]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the power converter of Artusi et al. to include method of adjusting internal operating characteristic as taught by Qahouq et al., because it help in enhancing the efficiency of the power converter.

Additionally, since Artusi et al. and Qahouq et al., are both from the same field of endeavor, the purpose disclosed by Qahouq et al. would have been recognized in the pertinent art of Artusi et al.

In re to claim 10, Artusi et al. disclose, the power converter (i.e. 118, fig 1, [0009]) as recited in claim 6. Except, Artusi et al. fails to disclose, wherein said internal operating characteristic is

selected from the group consisting of: a gate drive voltage level of said power switch of said power converter, a switching frequency of said power converter, and an internal direct current bus voltage of said power converter.

However, Qahouq et al. disclose, wherein said internal operating characteristic is selected from the group consisting of: a gate drive voltage level of said power switch of said power converter, a switching frequency of said power converter, and an internal direct current bus voltage of said power converter (i.e. Refer to paragraph 0007-0010).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the power converter of Artusi et al. to include method of adjusting internal operating characteristic as taught by Qahouq et al., because it help in enhancing the efficiency of the power converter.

Additionally, since Artusi et al. and Qahouq et al., are both from the same field of endeavor, the purpose disclosed by Qahouq et al. would have been recognized in the pertinent art of Artusi et al.

In re to claim 14, Artusi et al. disclose, the power system (i.e. 100, fig 1) as recited in claim 11. Except, Artusi et al. fails to disclose, wherein said power converter controller is further configured to adjust internal operating characteristic over a period of time.

However, Qahouq et al. disclose, wherein said power converter controller (i.e. 124, fig 1, [0009]) is further configured to adjust internal operating characteristic over a period of time. (Refer to paragraphs [0007 & 0009]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the power converter of Artusi et al. to include method of adjusting internal

operating characteristic as taught by Qahouq et al., because it help in enhancing the efficiency of the power converter.

Additionally, since Artusi et al. and Qahouq et al., are both from the same field of endeavor, the purpose disclosed by Qahouq et al. would have been recognized in the pertinent art of Artusi et al.

In re to claim 15, Artusi et al. disclose, the power converter (i.e. 118, fig 1, [0009]) as recited in claim 11. Except, Artusi et al. fails to disclose, wherein said internal operating characteristic is selected from the group consisting of: a gate drive voltage level of said power switch of said power converter, a switching frequency of said power converter, and an internal direct current bus voltage of said power converter.

However, Qahouq et al. disclose, wherein said internal operating characteristic is selected from the group consisting of: a gate drive voltage level of said power switch of said power converter, a switching frequency of said power converter, and an internal direct current bus voltage of said power converter (i.e. Refer to paragraph 0007-0010).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the power converter of Artusi et al. to include method of adjusting internal operating characteristic as taught by Qahouq et al., because it help in enhancing the efficiency of the power converter.

Additionally, since Artusi et al. and Qahouq et al., are both from the same field of endeavor, the purpose disclosed by Qahouq et al. would have been recognized in the pertinent art of Artusi et al.

In re to claim 18, Artusi et al. disclose, the power system (i.e. 100, fig 1, [0009]) as recited in claim 16. Except, Artusi et al. fails to disclose, wherein said power converter controller is further configured to adjust internal operating characteristic over a period of time.

However, Qahouq et al. disclose, wherein said power converter controller (i.e. 124, fig 1, [0009]) is further configured to adjust internal operating characteristic over a period of time. (Refer to paragraphs [0007 & 0009]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the power converter of Artusi et al. to include method of adjusting internal operating characteristic as taught by Qahouq et al., because it help in enhancing the efficiency of the power converter.

Additionally, since Artusi et al. and Qahouq et al., are both from the same field of endeavor, the purpose disclosed by Qahouq et al. would have been recognized in the pertinent art of Artusi et al.

In re to claim 20, Artusi et al. disclose, the power converter (i.e. 118, fig 1, [0009]) as recited in claim 16. Except, Artusi et al. fails to disclose, wherein said internal operating characteristic is selected from the group consisting of: a gate drive voltage level of said power switch of said power converter, a switching frequency of said power converter, and an internal direct current bus voltage of said power converter.

However, Qahouq et al. disclose, wherein said internal operating characteristic is selected from the group consisting of: a gate drive voltage level of said power switch of said power converter, a switching frequency of said power converter, and an internal direct current bus voltage of said power converter (i.e. Refer to paragraph 0007-0010).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the power converter of Artusi et al. to include method of adjusting internal operating characteristic as taught by Qahouq et al., because it help in enhancing the efficiency of the power converter.

Additionally, since Artusi et al. and Qahouq et al., are both from the same field of endeavor, the purpose disclosed by Qahouq et al. would have been recognized in the pertinent art of Artusi et al.

Examiner Notes

39. Examiner cites particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings in the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested that, in preparing responses, the applicant fully consider the references in its entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the examiner.

The prior art made of record and not relied upon is cited to establish the level of skill in the applicant art and those arts considered reasonably pertinent to applicant disclosure.

Contact Information

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to YEMANE MEHARI whose telephone number is (571)270-7603. The examiner can normally be reached on Monday to Thursday, 8-AM to 5-PM, EST. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Monica

Lewis can be reached on (571)272-1838. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Monica Lewis/
Supervisory Patent Examiner, Art Unit 2838

/YM/

Notice of References Cited	Application/Control No. 12/709,795	Applicant(s)/Patent Under Reexamination ARTUSI ET AL.	
	Examiner YEMANE MEHARI	Art Unit 2838	Page 1 of 1

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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Complete if Known	
Application Number	12/709,795
Filing Date	2/22/2010
First Named Inventor	Artusi et al.
Art Unit	2838
Examiner Name	TBD
Attorney Docket Number	CDW-011CP1CP1C1

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First Named Inventor	Artusi et al.
Art Unit	2838
Examiner Name	TBD
Attorney Docket Number	CDW-011CP1CP1C1

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Sheet 13 of 15

Complete if Known	
Application Number	12/709,795
Filing Date	2/22/2010
First Named Inventor	Artusi et al.
Art Unit	2838
Examiner Name	TBD
Attorney Docket Number	CDW-011CP1CP1C1

NON PATENT LITERATURE DOCUMENTS

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Art Unit	2838
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Sheet 15 of 15

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First Named Inventor	Artusi et al.
Art Unit	2838
Examiner Name	TBD
Attorney Docket Number	CDW-011CP1CP1C1

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Examiner Signature	/Yemane Mehari/	Date Considered	09/09/2010

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Sheet 1 of 15

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Application Number	12/709,795
Filing Date	2/22/2010
First Named Inventor	Artusi et al.
Art Unit	2838
Examiner Name	TBD
Attorney Docket Number	CDW-011CP1CP1C1

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	19.	JP 3-215911	09-20-1991	Matsushita Electric Ind.		
	20.	JP 2000-68132	03-03-2000	Toko Inc.		

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Sheet 2 of 15

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First Named Inventor	Artusi et al.
Art Unit	2838
Examiner Name	TBD
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Examiner Name	TBD
Attorney Docket Number	CDW-011CP1CP1C1

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT				**Application Number**	12/709,795
				Filing Date	2/22/2010
				First Named Inventor	Artusi et al.
				Art Unit	2838
(Use as many sheets as necessary)				Examiner Name	TBD
Sheet	12	of	15	Attorney Docket Number	CDW-011CP1CP1C1

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	193.	GAYE, M., *et al.*, "A 50-100MHz 5V to -5V, 1W Cuk Converter Using Gallium Arsenide Power Switches," ISCAS 2000 - IEEE International Symposium on Circuits and Systems, May 28-31, 2000, pp. I-264 – I-267, Vol. 1, IEEE, Geneva, Switzerland.	
	194.	GOLDBERG, A.F., *et al.*, "Issues Related to 1–10-MHz Transformer Design," IEEE Transactions on Power Electronics, January 1989, pp. 113–123, Vol. 4, No. 1, IEEE, Los Alamitos, CA.	
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				Filing Date	2/22/2010
				First Named Inventor	Artusi et al.
				Art Unit	2838
(Use as many sheets as necessary)				Examiner Name	TBD
Sheet	13	of	15	Attorney Docket Number	CDW-011CP1CP1C1

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	203.	MIWA, B.A., *et al.*, "High Efficiency Power Factor Correction Using Interleaving Techniques," IEEE Proceedings of APEC, 1992, pp. 557–568, IEEE, Los Alamitos, CA.	
	204.	NGUYEN, L.D., *et al.*, "Ultra-High-Speed Modulation-Doped Field-Effect Transistors: A Tutorial Review," Proceedings of the IEEE, April 1992, pp. 494–518, Vol. 80, No. 4, IEEE.	
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Sheet	14	of	15	Attorney Docket Number	CDW-011CP1CP1C1

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	213.	SEVERNS, R., "Circuit Reinvention in Power Electronics and Identification of Prior Work," Proceedings of 1997 IEEE Applied Power Electronics Conference (APEC '97), 1997, pp. 3–9, IEEE, Los Alamitos, CA.	
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	222.	XU, P., *et al.*, "Design and Performance Evaluation of Multi-Channel Interleaved Quasi-Square-Wave Buck Voltage Regulator Module," HFPC 2000 Proceedings, October 2000, pp. 82–88.	

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Sheet 15 of 15

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	223.	XU, P., *et al.*, "Design of 48 V Voltage Regulator Modules with a Novel Integrated Magnetics," IEEE Transactions on Power Electronics, November 2002, pp. 990–998, Vol. 17, No. 6, IEEE, Los Alamitos, CA.	
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	229.	ZHOU, X., *et al.*, "Investigation of Candidate VRM Topologies for Future Microprocessors," IEEE Applied Power Electronics Conference, March 1998, pp. 145–150, IEEE, Los Alamitos, CA.	

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
12/709,795	02/22/2010	2838	1310	CDW-011CP1CP1C1	20	4

CONFIRMATION NO. 7439

25962
SLATER & MATSIL, L.L.P.
17950 PRESTON RD, SUITE 1000
DALLAS, TX 75252-5793

FILING RECEIPT

OC000000040435474

Date Mailed: 03/05/2010

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Applicant(s)

Daniel A. Artusi, Austin, TX;
Ross Fosler, Buda, TX;
Allen F. Rozman, Murphy, TX;

Power of Attorney: The patent practitioners associated with Customer Number 25962

Domestic Priority data as claimed by applicant

This application is a CON of 12/051,334 03/19/2008 PAT 7,667,986
which is a CIP of 11/710,276 02/23/2007 PAT 7,675,759
which is a CIP of 11/607,325 12/01/2006 PAT 7,675,758

Foreign Applications

If Required, Foreign Filing License Granted: 03/04/2010

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/709,795**

Projected Publication Date: 06/17/2010

Non-Publication Request: No

Early Publication Request: No

Title

Power System with Power Converters Having an Adaptive Controller

Preliminary Class

363

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POWER SYSTEM WITH POWER CONVERTERS HAVING AN ADAPTIVE CONTROLLER

[0001] This application is a continuation of U.S. Patent Application Serial Number 12/051,334, entitled "Power System with Power Converters having an Adaptive Controller," filed on March 19, 2008 (now, U.S. Patent No. 7,667,986), which is a continuation in part of, and claims priority to, U.S. Patent Application Serial Number 11/710,276, entitled "Power System with Power Converters having an Adaptive Controller," filed on February 23, 2007 (now, U.S. Patent No. 7,675,759), which is a continuation in part of, and claims priority to, U.S. Patent Application Serial Number 11/607,325, entitled "Power Converter with an Adaptive Controller and Method of Operating the Same," filed on December 1, 2006 (now, U.S. Patent No. 7,675,758). The aforementioned applications are incorporated herein by reference.

CROSS-REFERENCE TO RELATED APPLICATIONS

[0002] This application relates to the following co-pending and commonly assigned patent applications, which applications are incorporated herein by reference:

Serial Number	**Patent Numbers or Publication Numbers**	**Title**
11/349,637	7,417,875	Power Converter Employing Integrated Magnetics with a Current Multiplier Rectifier and Method of Operating the Same
11/361,742	7,176,662	Power Converter Employing a Tapped Inductor and Integrated Magnetics and Method of Operating the Same
11/655,334	7,298,118	Power Converter Employing a Tapped Inductor and Integrated Magnetics and Method of Operating the Same

11/942,632	2008/0150666	Power Converter Employing a Tapped Inductor and Integrated Magnetics and Method of Operating the Same
11/361,914	7,385,375	Control Circuit for a Depletion Mode Switch and Method of Operating the Same
11/093,592	7,439,556	Substrate Driven Field-Effect Transistor
11/094,632	7,439,557	Semiconductor Device Having a Lateral Channel and Contacts on Opposing Surfaces Thereof
11/711,340	2007/0145417	High Voltage Semiconductor Device Having a Lateral Channel and Enhanced Gate-to-Drain Separation
11/128,623	7,339,208	Semiconductor Device Having Multiple Lateral Channels and Method of Forming the Same
11/211,964	7,285,807	Semiconductor Device Having Substrate-Driven Field-Effect Transistor and Schottky Diode and Method of Forming the Same
11/236,376	7,462,891	Semiconductor Device Having an Interconnect with Sloped Walls and Method of Forming the Same
11/765,252	2007/0298559	Vertical Field-Effect Transistor and Method of Forming the Same
11/765,323	7,663,183	Vertical Field-Effect Transistor and Method of Forming the Same
11/765,324	7,541,640	Vertical Field-Effect Transistor and Method of Forming the Same
11/847,450	2008/0054874	Power Converter Employing Regulators with a Coupled Inductor
11/607,325	7,675,758	Power Converter with an Adaptive Controller and Method of Controlling the Same

11/710,276	7,675,759	Power System with Power Converters Having an Adaptive Controller
11/955,627	2008/0316779	System and Method for Estimating Input Power for a Power Processing Circuit
11/955,642	2008/0315852	System and Method for Estimating Input Power for a Power Processing Circuit
10/922,062	7,012,414	Vertically Packaged Switched-Mode Power Converter
10/922,064	7,427,910	Winding Structure for Efficient Switch-Mode Power Converters
10/126,477	6,873,237	Core Structure
10/837,552	7,431,862	Synthesis of Magnetic, Dielectric or Phosphorescent Nano Composites
10/302,095	7,046,523	Core Structure and Interleaved DC-DC Converter Topology
10/080,142	6,549,436	Integrated Magnetic Converter Circuit and Method with Improved Filtering
10/080,026	6,775,159	Switching Power Converter Circuits Providing Main and Auxiliary Output Voltages
10/922,066	7,321,283	Vertical Winding Structures for Planar Magnetic Switched-Mode Power Converters
10/922,068	6,980,077	Composite Magnetic Core for Switch-Mode Power Converters
10/922,067	7,280,026	Extended E Matrix Integrated Magnetics (MIM) Core

TECHNICAL FIELD

[0003] The present invention is directed, in general, to electronic power conversion and, more specifically, to a power system having power converters including a controller adapted to improve power conversion efficiency and method of operating the same.

BACKGROUND

[0004] A switch-mode power converter (also referred to as a "power converter") is a power supply or power processing circuit that converts an input voltage waveform into a specified output voltage waveform. Controllers associated with the power converters manage an operation thereof by controlling the conduction periods of power switches employed therein. Generally, the controllers are coupled between an input and output of the power converter in a feedback loop configuration.

[0005] Typically, the controller measures an internal operating characteristic (*e.g.*, an internal bus voltage) or an output characteristic, (*e.g.*, an output voltage or an output current) representing an operating condition of the power converter, and based thereon modifies a duty cycle of a power switch or power switches of the power converter to regulate the internal operating characteristic or the output characteristic. The duty cycle is a ratio represented by a conduction period of a power switch to a switching period thereof. Thus, if a power switch conducts for half of the switching period, the duty cycle for the power switch would be 0.5 (or 50 percent). Additionally, as the needs for systems such as a microprocessor powered by the power converter dynamically change (*e.g.*, as a computational load on the microprocessor changes), the controller should be configured to dynamically increase or decrease the duty cycle of the power switches therein to regulate the internal or the output characteristic at a desired value. In an

exemplary application, the power converters have the capability to convert an unregulated dc input voltage such as five volts to a lower, regulated, dc output voltage such as 2.5 volts to power a load. In another exemplary application, the power converters have the capability to convert an unregulated ac input voltage such as 120 volts to a regulated internal dc bus voltage, such as 300 volts dc, and to further convert the regulated internal dc bus voltage into a dc output voltage such as 2.5 volts to power a load.

[0006] An important consideration for the design of a power converter and its controller is the efficiency (also referred to as "operating efficiency") in a particular application, and under particular operating conditions. The efficiency of a power converter is the ratio of its output power to its input power. The practical efficiency of a power converter that delivers at least half its rated output power to a load is typically 80 to 90%. As load current is reduced, the operating efficiency correspondingly goes down. In the limiting case wherein the load current approaches a small percentage of the maximum rated current of the power converter, the operating efficiency approaches zero due to the need to provide power for fixed internal loads such as the controller itself, for drivers, for internal high-frequency power switches, and for inherently dissipative circuit elements such as the magnetic core of a high-frequency transformer. Power converter efficiency is accordingly dependent on an internal operating characteristic of the power converter or an output characteristic thereof. Examples of an internal operating characteristic include a temperature of a component part, an internal bus voltage, the voltage level of a drive signal for a power switch, the number of paralleled power switches selectively enabled to conduct, the number of phases enabled on a power converter, or even the basic switching frequency of the power converter. Examples of an output characteristic include a load current drawn from the power converter and an output voltage. Power converter efficiency is also dependent on a

parameter that may be measured after a manufacturing step, which may reflect a dependency of efficiency on particular parts used to manufacture the power converter in question.

[0007] Operating efficiency is an important quality indicator for a power converter because of the broad impact efficiency has on equipment reliability and size, operating expense, and corresponding effects on the load equipment that it powers. Thus, system considerations of achieving high operating efficiency have immediate effects on the applicability of a particular power converter design, and the associated price thereof in the marketplace.

[0008] Numerous prior art attempts have been made to improve the operating efficiency of a power converter. Most attempts have focused on selection of proper components to provide the maximum operating efficiency for average operating conditions at a chosen operating point, such as a load current at three quarters of a maximum rated value, the environmental temperature at a typical expected value, and for a typical mix of actual components employed to manufacture a particular power converter. Recognizing the wide range of possible values for any of these parameters, there is substantial opportunity to improve the efficiency of a power converter for a particular operating condition.

[0009] An example of the prior art to provide high power converter efficiency at a particular operating condition is provided in U.S. Patent No. 6,351,396, entitled "Method and Apparatus for Dynamically Altering Operation of a Converter Device to Improve Conversion Efficiency," to Jacobs, issued February 26, 2002 which is incorporated herein by reference. Jacobs is directed to a search process that varies parameters accessible to the controller during power converter operation, such as a timing delay between conduction intervals of the power switches, and observes the resulting effect on the duty cycle. The duty cycle is employed as an indicator of operating efficiency, and parameters accessible to the controller are adjusted to produce an

extremum in the duty cycle for a particular operating condition, thereby increasing the operating efficiency of the power converter. While Jacobs performs efficiency optimization under actual operating conditions, the reference nonetheless fails to consider constraints of the actual application (such as described in a requirements document or operating specification document) or the environment during execution of the process of efficiency optimization, or a signal from an external source to enable, limit, or alter the optimization process. For example, no attempt is made to measure a parameter of a particular power converter after a manufacturing step (or to measure a parameter of a representative power converter), or to control, program, or otherwise alter a response of the controller to reflect such measurement, such as by controlling an internal operating characteristic or an output characteristic.

[0010] Another attempt to adaptively operate a power converter to improve efficiency is described in U.S. Patent No. 5,742, 491, entitled "Power Converter Adaptively Driven," to Bowman, *et al.* ("Bowman"), issued April 21, 1998, which is incorporated herein by reference. Bowman is directed to a drive circuit for a power converter wherein the timing of conduction intervals for the power switches is programmed to increase the efficiency of the power converter while keeping stresses on individual components within acceptable limits. A predetermined delay between drive waveforms supplied to the power switches and to the synchronous rectifiers of the power converter is altered with a predetermined program that is a function of an operating condition of the power converter to allow the power converter to operate efficiently in an anticipated operating environment and with anticipated component realizations. A design objective is to desensitize the operating efficiency to an expected range of changes in the operating environment and with an anticipated range of component realizations, which results in a compromise in a static program to optimize efficiency that might otherwise be achievable with

the design of an improved controller not so limited. Bowman relies on a limited set of *a priori* conditions, and does not adjust controller parameters in response to a measured power converter parameter for the particular power converter after a manufacturing step, or to a measured parameter of a representative power converter (*e.g.*, from a group of manufactured units), or in response to a signal from an external source representing an environmental parameter.

[0011] A further attempt to optimize power conversion efficiency is described in U.S. Patent No. 5,734,564, entitled "High-Efficiency Switching Power Converter," to Brkovic, issued March 31, 1998, which is incorporated herein by reference. Brkovic describes measuring an internal operating characteristic of a power train of the power converter (*i.e.*, a voltage across a power switch) and adjusting a timing of a duty cycle for the power switch in response to the measured power switch voltage to improve power conversion efficiency. Brkovic provides a preconditioned response to a measured parameter of the particular power converter after a manufacturing step. Brkovic does not consider adapting or constraining the response to a signal from an external source representing an environmental parameter.

[0012] It is well known in the art to couple an input control signal to a power converter to control the setpoint of an output characteristic thereof. For example, the output voltage of a power converter adapted to supply power to a microprocessor load (wherein the operating voltage thereof is not known at the time of manufacture, or that is changed during normal operation such as when a microprocessor enters a sleep mode) can be statically or dynamically altered by an input control signal. However, this control mechanism merely changes a setpoint for an output characteristic of the power converter, and is not adapted to optimize the efficiency of the power converter at the signaled setpoint.

[0013] It should also be taken into account that there are loads with different operating states. For example, a server configured to process financial data may operate at a higher level of criticality during normal business hours, and revert to a lower processing state at another time of day. The aforementioned system may require a higher level of performance from the power converter during such periods of high criticality, which may compromise operating efficiency, but which may admit higher operating efficiency during substantial periods of time in the lower processing state.

[0014] Power conversion systems of the prior art have only partially responded to such system operational state considerations in the optimization of operating efficiency, particularly at a system level. For example, the Advanced Configuration and Power Interface ("ACPI") specification is an open industry standard initially produced in December 1996 that describes "P-states" and "C-states" of a processor employed in a digital system, and which is incorporated herein by reference. The P-state, typically designated as P-states P0, P1, and P2, describes the "performance" state (or, alternatively, the "power" state) of the processor as high, medium, or low, respectively, for example, as described by Alon Naveh, *et al.*, in the article entitled "Power and Thermal Management in the Intel® Core Duo™ Processor, Intel Technology Journal, May 15, 2006, pp. 109-121, which is incorporated herein by reference. The P-state is selected by the software operating system to meet the execution needs of the software load as observed over a period of time. A particular P-state is affected by setting, from a set of predetermined values from a list, the core input voltage of the processor and its clock rate. The processor core input voltage is adjusted by sending a digital signal such as a "VID" code to the processor's point-of-load voltage source. A processor operating at a lower core voltage and with a slower clock operates at a substantially lower power level.

[0015] Another processor state indicator, the core state ("C-state"), also under software operating system control, affects its level of power consumption from another perspective. The highest processor C-state, C0, describes a processor at its full operational level. Lower C-state levels, C1, C2,…, C4, describe various levels of a processor sleep state. The C-state level C1 provides the minimum level of power saving, but provides the fastest response time back to the full operational level C-state level C0. The C-state level C4 provides a "deep sleep" level, but requires substantial time for the processor to return to normal operation. The various sleep levels are achieved by halting instruction execution, gating internal clocks, disabling internal phase-locked loops, and disabling ports that respond to certain levels of interrupts. The minimum core voltage necessary to retain certain volatile memory elements is applied.

[0016] Although these state indicators have been used to substantially reduce the energy requirement of a digital system at the system level, particularly the power level during an idling state, corresponding states have not been described for elements of the power system as it responds to the various operational levels of the load, such as a request for a particular load voltage, or a particular level of system readiness, or the response time for changes in a system operational level. Accordingly, opportunities for further improvement in power converter operational efficiency have not been realized.

[0017] Thus, attempts have been made in the prior art to configure power converter controllers to statically optimize power conversion efficiency of a power train. The static responses have included varying an internal operating characteristic of the power converter with a fixed program in response to a measured characteristic such as a load current to improve power conversion efficiency, or in response to observed changes in power converter duty cycle. The aforementioned attempts to improve efficiency have been facilitated by inclusion of

programmable digital devices such as microprocessors, digital signal processors, application specific integrated circuits, and field-programmable gate arrays in the controller. Nonetheless, the responses of a controller have not included consideration of a measured parameter after a manufacturing step for the particular power converter that is being controlled such as a measurement of an actual delay of a particular power switch or an internal circuit after completion of a stage of manufacture, or a signal indicating a system operational state.

[0018] Considering limitations as described above, a controller for a power converter is presently not available for the more severe applications that lie ahead that depend on achieving higher operating efficiency for a particular operating characteristic constrained or controlled by an environmental parameter. In addition, a controller for a power converter is presently not available that responds to a parameter measured after a manufacturing step for the particular power converter, or to a parameter measured after a manufacturing step on a representative power converter, or on power converters in a representative run, to improve the operating efficiency thereof. A controller for a power converter is also presently not available that responds to a signal indicating a system operational state to improve operating efficiency at a system level.

[0019] Accordingly, what is needed in the art is a controller for a power converter and power system that adaptively improves power conversion efficiency of a power converter in response to a measured parameter of the power converter after a manufacturing step, or to a parameter measured on a representative power converter, and includes consideration of operating conditions, a signal from an external source representing an environmental parameter or system operational state of a load coupled to the power system. In accordance therewith, a controller for

a power converter and power system is provided that adaptively improves power conversion efficiency, including considerations as provided herein.

SUMMARY OF THE INVENTION

[0020] These and other problems are generally solved or circumvented, and technical advantages are generally achieved, by advantageous embodiments of the present invention, which include a power system having a power converter with an adaptive controller and method of operating the same. In one embodiment, a power converter coupled to a load includes a power switch configured to conduct for a duty cycle to provide an output characteristic at an output thereof. The power converter also includes a power converter controller configured to receive a signal from the load indicating a system operational state of the load and enable a power converter topological state as a function of the signal.

[0021] In another embodiment, a power system includes a power system controller configured to provide a signal characterizing a power requirement of a processor system and a power converter coupled to the processor system. The power converter includes a power switch configured to conduct for a duty cycle to provide an output characteristic at an output thereof and a power converter controller configured to receive the signal from the power system controller to enter a power converter topological state dependent on the signal.

[0022] In another embodiment, a power system includes a power system controller configured to enable operation of components of a processor system to establish a state of power drain thereof and provide a signal to identify operation of the processor system in the state of power drain. The power system also includes a power converter, coupled to the processor system, including a power converter controller configured to receive the signal from the power system controller, to sense a power level of the state of power drain in response to the signal, and to control a power converter topological state as a function of the power level.

[0023] The foregoing has outlined rather broadly the features and technical advantages of the present invention in order that the detailed description of the invention that follows may be better understood. Additional features and advantages of the invention will be described hereinafter which form the subject of the claims of the invention. It should be appreciated by those skilled in the art that the conception and specific embodiment disclosed may be readily utilized as a basis for modifying or designing other structures or processes for carrying out the same purposes of the present invention. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the spirit and scope of the invention as set forth in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0024] For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

[0025] FIGURE 1 illustrates a block diagram of a power converter controlled by a conventional controller;

[0026] FIGURE 2 illustrates a schematic diagram of an exemplary power train of a buck power converter;

[0027] FIGURE 3 illustrates a schematic diagram of an embodiment of a power converter including a controller constructed according to the principles of the present invention;

[0028] FIGURE 4 illustrates exemplary waveform diagrams to control the conduction intervals of selected power switches of the power converter of FIGURE 3 with an intervening delay therebetween;

[0029] FIGUREs 5A and 5B illustrate diagrams of exemplary multidimensional tables for the time delays for the control signals to control the conduction intervals of synchronous rectifier switches in accordance with a representative operating parameter of the power converter of FIGURE 3;

[0030] FIGURE 6 illustrates an embodiment of a functional representation to improve power conversion efficiency constructed according to the principles of the present invention;

[0031] FIGURE 7 illustrates a block diagram of an embodiment of a power converter constructed according to the principles of the present invention;

[0032] FIGURE 8 illustrates a block diagram of an embodiment of a power converter constructed according to the principles of the present invention;

[0033] FIGUREs 9A to 9F illustrate the dependence of power converter efficiency on various operating parameters and the operating environment in accordance with the principles of the present invention;

[0034] FIGURE 10 illustrates an ac input voltage waveform including an exemplary input line voltage dropout transient, showing time histories of possible internal bus voltages in accordance with the principles of the present invention;

[0035] FIGURE 11 illustrates a block diagram of an embodiment of a power system coupled to loads and including power converters controlled by a power system controller constructed according to the principles of the present invention;

[0036] FIGURE 12 illustrates a diagram of an embodiment of processor core states in accordance with the principles of the present invention;

[0037] FIGURE 13 illustrates a state transition diagram for power converter operational states for a power converter constructed according to the principles of the present invention;

[0038] FIGURE 14 illustrates a graphical representation of efficiency improvement as a function of power converter operational state for a representative power converter constructed according to the principles of the present invention;

[0039] FIGURE 15 illustrates a graphical representation of power converter dissipation corresponding to the efficiency data illustrated in FIGURE 14;

[0040] FIGURE 16 illustrates a graphical representation of efficiency improvement as a function of power converter operational state for a representative power system including two

power converters operating in parallel to provide a high level of power system reliability constructed according to the principles of the present invention; and

[0041] FIGURE 17 illustrates a graphical representation of power converter dissipation corresponding to the efficiency data illustrated in FIGURE 16.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

[0042] The making and using of the presently preferred embodiments are discussed in detail below. It should be appreciated, however, that the present invention provides many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative of specific ways to make and use the invention, and do not limit the scope of the invention.

[0043] The present invention will be described with respect to exemplary embodiments in a specific context, namely, a power system including power converters with a controller and, more particularly, a controller for a power converter that regulates an output characteristic of the power converter at an output thereof that adaptively controls an internal operating characteristic of the power converter to increase power conversion efficiency in response to a parameter of the power converter measured after a manufacturing step and/or an environmental parameter of the power converter. The parameters mentioned above are typically measured after the power converter(s) are implemented and/or after a signal is received from an external source representing an environmental parameter or a signal indicating a system operational state or a change in a system operational state. In addition, the controller may change a topological state of a power converter in response to a signal received from an external source. Examples of a topological state or changes thereto include, without limitation, a fully operational power converter, a number of paralleled synchronous rectifiers that are actively driven, a power factor-corrected front end for which active control is disabled but remains operational to maintain an internal bus voltage without active power factor control, disabling (or setting in a standby mode) one or more of a plurality of paralleled power converters when a high level of operational reliability is not required by the system, a power converter with reduced power factor control,

and a power converter with at least one phase of power factor control disabled. The changes to the topological state of the power converter may improve an operating efficiency thereof as a function of a system operational state.

[0044] Regarding the environmental parameters, examples thereof include, without limitation, a signal indicating the existence of a paralleled power converter, the operational state of the paralleled power converter, that the powered system is operating from a backup power source, a request for a particular load voltage, an indication that a particular portion of the load has failed, or has been disabled, or is operating at a reduced power level. Further examples indicating a system operational state include, without limitation, a signal providing a performance state or a core state of a processor such as a P-state or C-state, indicating, for example, that the system is operating from emergency power or battery reserve, that redundant hardware such as a redundant power converter may have been disabled, that the system is not providing a critical function such as during an off-hours timeframe, that the system is sustaining substantial thermal margins allowing selected fans to be disabled and/or the fan speed to be substantially reduced, that the system is about to transition to a higher level of system performance, or that a requirement for a specified holdover time can be relaxed. An example of a signal indicating a change in a system operational state is a signal indicating that a load current will change from a first current level to a second current level at or around a particular time.

[0045] Additionally, the controller for a power converter according to the principles of the present invention can control, alter, relax, or differently constrain an internal operating characteristic (such as a gate drive voltage level, a switching frequency, an internal voltage or current, *etc.*) or an output characteristic (such as a regulated voltage setpoint of the power converter) to improve an efficiency thereof in response to signals from an external source

representing an environmental parameter (such as the existence of a parallel-coupled power converter powering a common load) or in response to a signal indicating a system operational state. For example, the internal dc bus voltage of a power converter might be adaptively reduced to improve the power conversion efficiency of a front-end boost power converter, recognizing that such voltage reduction would directly affect the holdover capability of the power converter during periods of loss of ac input voltage (often referred to as line dropout, for example, as illustrated and described hereinbelow with reference to FIGURE 10), which might be a required internal operating characteristic. Holdover capability is generally inversely proportional to the load on the power converter and would depend on the presence and operational state of a paralleled power converter.

[0046] The data from an external source representing an environmental parameter can be employed by an adaptive controller, for example, to reduce the internal dc bus voltage to a particular level above a lower voltage limit dependent on the measured power converter load and the external data, and thereby improve operating efficiency in view of an internal characteristic or an output characteristic, but constrained by a signal from an external source. Examples of a response to a signal indicating a system operational state include, without limitation, selectively disabling paralleled synchronous rectifiers during a sustained light load operating condition, disabling a power factor correction function in a boost power converter and relying on a peak-charging mechanism to sustain an internal bus voltage, configuring a power factor correction function in a boost power converter to operate at reduced power factor thereby improving efficiency, selectively disabling one or more phases of a multi-phase power converter such as a multi-phase boost power factor correction ("PFC") power converter, or a multi phase implementation of a DC/DC power converter, disabling (or setting in a standby mode) a

redundant power converter when such redundancy is not required for system operation, and selectively disabling and/or reducing the speed of power converter fans that may not be needed from a system operational consideration.

[0047] Referring initially to FIGURE 1, illustrated is a block diagram of a power converter controlled by a conventional controller. The power converter includes a power train 105 coupled to a source of electrical power (represented by a battery, but may be other sources of power, such as ac power) for providing an input voltage V_{in} for the power converter. The power converter also includes a controller 110, and provides power to a system (not shown) such as a microprocessor coupled to an output thereof. The power train 105 may employ a buck topology as illustrated and described with respect to FIGURE 2 below.

[0048] The power train 105 receives an input voltage V_{in} at an input thereof and provides a regulated output characteristic (*e.g.*, an output voltage V_{out}) to power a microprocessor or other load coupled to an output of the power converter. The controller 110 is typically coupled to a voltage reference representing a desired characteristic such as a desired system voltage from an internal or external source associated with the microprocessor, and to the output voltage V_{out} of the power converter. In accordance with the aforementioned characteristics, the controller 110 provides a signal to control a duty cycle and a frequency of at least one power switch of the power train 105 to regulate the output voltage V_{out} or another characteristic thereof. Thus, the controller 110 for the power train 105 of a power converter, particularly a switch-mode power converter, generally measures an internal operating characteristic or an output characteristic of the power converter and controls a duty cycle of a power switch therein in response to the measured characteristic to regulate the internal operating characteristic or the output characteristic thereof.

[0049] A driver (not shown) may be interposed between the controller 110 and the power train 105 to provide a drive signal(s) for the power switch(es) with sufficient amplitude and with waveform characteristics to efficiently enable or disable conductivity of the power switch(es). In accordance with the aforementioned characteristics, a drive signal is provided by a driver to control a duty cycle and a frequency of one or more power switches of the power converter, preferably to regulate the output voltage V_{out} thereof. For a P-channel metal-oxide semiconductor power switch, a gate drive signal is typically driven negative (with respect to the source terminal) to turn on the power switch, and for an N-channel metal-oxide semiconductor power switch, a gate drive signal is typically driven positive (with respect to the source terminal) to turn on the power switch. A driver may employ techniques to provide sufficient signal delays to prevent shoot-through currents when controlling multiple power switches in a power converter.

[0050] Turning now to FIGURE 2, illustrated is a schematic diagram of an exemplary power train of a buck power converter. The power train of the power converter receives an input voltage V_{in} (*e.g.*, an unregulated input voltage) from a source of electrical power (represented by a battery) at an input thereof and provides a regulated output voltage V_{out} to power, for instance, a microprocessor at an output of the power converter. In keeping with the principles of a buck topology, the output voltage V_{out} is generally less than the input voltage V_{in} such that a switching operation of the power converter can regulate the output voltage V_{out}. A main power switch Q_{main} is enabled to conduct by a gate drive signal D for a primary interval and couples the input voltage V_{in} to an output filter inductor L_{out}. During the primary interval, an inductor current I_{Lout} flowing through the output filter inductor L_{out} increases as a current flows from the input to the

output of the power train. An ac component of the inductor current I_{Lout} is filtered by an output capacitor C_{out}.

[0051] During a complementary interval, the main power switch Q_{main} is transitioned to a non-conducting state and an auxiliary power switch Q_{aux} is enabled to conduct by a complementary gate drive signal 1-D. The auxiliary power switch Q_{aux} provides a path to maintain a continuity of the inductor current I_{Lout} flowing through the output filter inductor L_{out}. During the complementary interval 1-D, the inductor current I_{Lout} through the output filter inductor L_{out} decreases. In general, the duty cycle of the main and auxiliary power switches Q_{main}, Q_{aux} may be adjusted to maintain a regulation of the output voltage V_{out} of the power converter. Those skilled in the art understand that the conduction periods for the main and auxiliary power switches $Q_{main,}$, Q_{aux} may be separated by a small time interval to avoid cross conduction current therebetween and beneficially to reduce the switching losses associated with the power converter, where such time interval is ideally selected based on load, operating, and environmental conditions. Similarly, conduction periods for power switches that may be diodes may also be separated by a small time interval to avoid cross conduction current therebetween. Thus, the power train of a switch-mode power converter generally includes a plurality of power switches coupled to reactive circuit elements to provide the power conversion function therefore.

[0052] Turning now to FIGURE 3, illustrated is a schematic diagram of an embodiment of a power converter including a controller 311 constructed according to the principles of the present invention. The power converter includes two exemplary power stages, namely, a first power stage 310 (*e.g.*, a boost power stage possibly employed to perform power factor correction) and a second power stage (*e.g.*, an isolating dc-to-dc power stage) 320. The input power source 301 to the first power stage 310 is an ac power source, which is coupled to a diode bridge rectifier 303.

The first power stage 310, controlled by controller 311, produces an internal regulated bus voltage V_{bus} across a capacitor C_1, which provides the input voltage to the second power stage 320. The first power stage 310 includes boost power switch Q_{boost} and diode D_1, which alternately conduct to transfer charge from the input power source 301 through an inductor L_1 to the capacitor C_1. The controller 311 senses the rectified input voltage V_{in} and the internal bus voltage V_{bus} to control a duty cycle of the boost power switch Q_{boost}, to regulate the bus voltage V_{bus} and to control the power factor of power drawn from the input power source 301.

[0053] The second power stage 320 includes isolation transformer TR and a power switch Q_{pri} in series with the primary winding thereof. Synchronous rectifier switches Q_{fwd}, Q_{fly} are power switches coupled in series across a secondary winding of the isolation transformer TR to rectify the voltage therefrom, which winding voltage is coupled to an output filter including an output inductor L_{out} and an output capacitor C_{out}. The controller 311 provides control signals (*e.g.*, gate control signals) V_{Gfwd}, V_{Gfly} to control the synchronous rectifier switches Q_{fwd}, Q_{fly}, respectively. A brief time delay ΔT between conduction intervals of the synchronous rectifier switches Q_{fwd}, Q_{fly} is provided by the controller 311 to prevent cross conduction therebetween. In a preferred embodiment, the controller 311 selects the time delay ΔT dependent on operating conditions of the power converter as described hereinbelow to provide improved power conversion efficiency.

[0054] Turning now to FIGURE 4, illustrated are exemplary waveform diagrams to control the conduction intervals of selected power switches of the power converter of FIGURE 3 with an intervening delay therebetween. More specifically, FIGURE 4 illustrates an example of a time delay ΔT between the gate control signals V_{Gfwd}, V_{Gfly} to control the conduction intervals of the synchronous rectifier switches Q_{fwd}, Q_{fly}, respectively.

[0055] Returning now to the description of the power converter of FIGURE 3, the output filter attenuates ac components present across the secondary winding of transformer TR to provide a substantially constant dc output voltage V_{out}. The output voltage V_{out}, as well as the load current I_{load} sensed by a sensor (*e.g.*, a current sensing circuit element 315), is sensed by controller 311. Various circuit elements capable of sensing a load current, including a low resistance current-sensing resistor or a current-sensing transformer, are well known in the art and will not be described herein. Although the controller 311 is shown directly coupled to both sides of the isolation transformer TR, circuit elements to provide the necessary level of isolation for a controller 311 for a particular application are also well known in the art and will not be described herein. A thermistor (or other suitable thermal sensor) 313 provides a temperature measurement to the controller 311 at a selected point(s) in or about the power converter. Typical points for temperature sensing include a location adjacent to a power switch or to an isolation transformer, and may include the ambient temperature outside the power converter itself. Although one thermistor 313 is illustrated in FIGURE 3, a plurality of thermistors may also be included within the scope of the invention to provide multiple temperature measurements to the controller 311. The detailed operation and characteristics of the first and second power stages 310, 320 are well known in the art, and will not be further described herein.

[0056] The controller 311 in the exemplary power converter illustrated in FIGURE 3 senses and is responsive to the rectified input voltage V_{in}, the internal bus voltage V_{bus}, the power converter output voltage V_{out}, the load current I_{load}, as well as a signal "Temp" representing a temperature using the thermistor 313. In addition, the controller 311 senses and is responsive to an external signal V_{ext} indicating an environmental parameter from an external source such as a server powered by the power converter, and to a setup signal V_{setup} that may provide the result of

a parameter measured in a test fixture after a manufacturing step to set or otherwise tailor parameters for the operation of the controller 311. In a preferred embodiment, the controller 311 includes digital processing capability at least comparable to that of a low-end microprocessor (or other digital implementations, such as a microcontroller, digital signal controller, digital signal processor, a field-programmable gate array, complex programmable logic device, or combinations thereof), and is operative to adaptively improve (*e.g.*, optimize) the efficiency of the power converter from a variety of data and signal sources.

[0057] The controller 311 is configured to augment the operating efficiency of the power converter in response to a sensed or signaled internal operating characteristic and/or an output characteristic, a power converter parameter measured after a manufacturing step, and a signal from an external source representing an environmental parameter obtained from an external source such as a signal from a server being powered. Exemplary environmental parameters obtained from an external source, which reflect how the power converter is being used in an application, include a signal indicating parallel operation with a second power converter, an indication that a paralleled power converter has failed, an indication that the power converter is supporting a critical application requiring a modified trade-off between power conversion efficiency and reliability, and an indication that the system is operating from a back-up power source, and may signal, for example, a lower limit for a dc bus voltage, reflecting a modified need for power converter holdover to accommodate altered statistics for a transient power outage condition.

[0058] The controller 311 may also respond to a signal indicating a system operational state S_{op_state}, which may be provided by a power system controller, which may be constructed as a component of the load (for example and without restriction, as a power system controller

described hereinbelow with reference to FIGURE 11). The responses may include altering a power converter topological state such as disabling a power factor correction function for the boost power switch Q_{boost} (*e.g.*, a disable signal from the controller 311 to disable the boost power switch Q_{boost}), disabling a drive signal for synchronous rectifier switches Q_{fly}, Q_{fwd}, or disabling (or setting in a standby mode) a particular power converter because sufficient redundant or nonredundant operation can be sustained presently by the system. Further responses may include operating at a lower switching frequency because the system can tolerate a higher ripple voltage in view of a present system operational state or operating at a higher switching frequency, *etc.*, because the system is about to enter a system state with a higher required level of system performance.

[0059] A system such as a personal computer, processor system or a server is often constructed with a number of system components such as memory, hard drives, and specialized circuit cards that are specified and installed when the system is assembled for a particular application. Thus, power system drains are generally unknown until such a system is specified and assembled. The rated power drain of installed power converters will generally be substantially greater than actual power drains of a system in a particular application, which provides an opportunity to optimize power conversion efficiency. Upon power-up of such a system, or during its continued operation, a power system controller can enable operation of its principal components to establish a state of maximum power drain (*e.g.*, substantially a maximum level of power drain that must be supported by the power system). The power system controller can be configured to provide a signal to the power system to identify operation of the system in such a state of a maximum power drain. A power converter controller, such as controller 311, can be configured to receive the signal from the power system controller, and to

sense a power level of the system operating in such a state of maximum power drain. The power converter controller can then control a power converter topological state as a function of the sensed maximum power level, including an appropriate margin as necessary. The power converter controller can be configured to control a duty cycle of a power switch, adjust a bus voltage, *etc.*, in accordance with the sensed maximum power level. The power converter controller can also transmit a signal back to the power system controller identifying the sensed maximum power level so that the power system controller can select a system operational state dependent on the sensed maximum power level. Of course, a power level of a system can be sensed and signaled at other times during system operation, such as at a time when power drains are at a normal or reduced operating level. A signal from a power system controller signaling to a power converter controller an expected level of power drains can also be produced by the power system controller based on an inventory of installed components, rather than on an actual drain measurement.

[0060] The power converter controller, such as controller 311, may include a multidimensional table or other functional representation of a value to control an internal operating characteristic or an output characteristic of the power converter. Multidimensional inputs to such a table or other functional representation include signals representing an internal operating characteristic, an output operating characteristic, a power converter parameter measured after a manufacturing stage, a parameter measured on a representative power converter, and/or a signal representing an environmental parameter or a system operational state. There are references utilizing lookup tables and other multidimensional functional representations directed to automotive engine map and lookup table systems such as U.S. Patent No. 5,925,088, entitled "Air-fuel Ratio Detecting Device and Method," to Nasu, issued July 20,

1999, U.S. Patent No. 7,076,360, entitled "Auto-Ignition Timing Control and Calibration Method," to Ma, issued July 11, 2006, and U.S. Patent No. 6,539,299, entitled "Apparatus and Method for Calibrating an Engine Management System," to Chatfield, *et al.*, issued March 25, 2003, which are incorporated herein by reference.

[0061] Turning now to FIGUREs 5A and 5B, illustrated are diagrams of exemplary multidimensional tables for the time delays ΔT (in nanoseconds) for the gate control signals V_{Gfwd}, V_{Gfly} to control the conduction intervals of the synchronous rectifier switches Q_{fwd}, Q_{fly}, respectively, in accordance with a representative operating parameter of the power converter of FIGURE 3. More specifically, FIGURE 5A demonstrates the time delay ΔT with the input voltage V_{in} being below about 48 volts and FIGURE 5B demonstrates the time delay ΔT with the input voltage V_{in} being above about 48 volts. The tables, listing delay in nanoseconds between opening a first power switch and closing a second power switch (*e.g.*, the synchronous rectifier switches Q_{fwd}, Q_{fly}) is accessed along a row with suitably quantized load current I_{load}, and along a column with suitably quantized temperature. The entries in the table are obtained by experimentally varying switch delay in a test set after manufacture of the power converter, and observing the effect of various delays on power conversion efficiency. The tables reflect a range of different values of input voltage V_{in} measured for the particular power converter after a manufacturing stage. Of course, tables can be constructed with additional dimensions, accommodating additional parameters such as an output voltage V_{out}, and internal bus voltage V_{bus}, an input signal from an external source indicating an environmental parameter, *etc.*, and finer levels of granularity. Various methods of interpolation between entries in the tables are well known in the art, and will not be described in the interest of brevity.

[0062] Such multidimensional tables can be used, for example, to control the switching frequency of a power converter. Switching frequency in the prior art is generally set as a design parameter, and is selected and fixed during a stage of design. The selected switching frequency is generally the result of a trade-off that considers, for example, the loss characteristics of the core material of the isolation transformer which depend on, without limitation, transformer core temperature, the primary-to-secondary turns ratio of the transformer, the expected thermal environment of the application, the heat transfer characteristics of the resulting power converter design, and the particular batch of core material from which the magnetic core thereof was formed. The resulting core loss for a particular power converter can also be substantially dependent on core characteristics such as a flux gap and core area of the particular core that was installed, all of which are substantially unknown before the power converter is manufactured.

[0063] In addition, the selected switching frequency is a result of consideration of other frequency dependent losses within the power converter. For example, gate drive losses are generally proportional to switching frequency and depend on the particular manufacturing run of power switches employed therein. Thus, altering the switching frequency for a particular application using a table constructed according to the principles of the present invention, considering manufacturing data, actual load current, and other measured or sensed variables can result in improved power conversion efficiency within a predetermined set of operating constraints that may be signaled from an external source. A test set can be readily constructed, as is well known in the art, to vary switching frequency and observe the effect on power conversion efficiency. Entries are then made in the table to represent preferable switching frequencies. Static efficiency optimization approaches of the prior art that use a predetermined

curve or other fixed approach do not advantageously achieve the benefits of improved efficiency with greater flexibility to respond to additional data as described herein.

[0064] A lookup table-based optimization procedure may be the most economical and effective method for many practical applications. Optimization would be limited to discrete ranges using preprogrammed values. A power converter would only enter an optimization state after sufficient time at a given operating point. A few discrete power states can be fully characterized during design to ensure reliability. The alternative of a continuous search algorithm would be eliminated by a table-based procedure. A continuous search algorithm can lead to a continuing state of "hunting." The complex, nonlinear nature of the optimization problem may make such continuous search algorithms non-deterministic and unreliable in a practical application.

[0065] Turning now to FIGURE 6, illustrated is an embodiment of a functional representation to improve power conversion efficiency constructed according to the principles of the present invention by determining a controllable parameter such as an internal bus voltage setpoint $V_{bus\_setpoint}$ of the power converter. An exemplary function is represented dependent on load current $I_{load,}$ operating temperature, data acquired after a manufacturing step, and data from an external source. The exemplary functional dependence illustrated in FIGURE 6 for the internal bus voltage setpoint $V_{bus\_setpoint}$ for an internal bus voltage is:

$$V_{bus\_setpoint} = 380 + 0.1 \cdot I_{load} - 0.2 \cdot Temp + V_{setup} + 10 \cdot V_{ext},$$

where "I_{load}" represents a sensed power converter load current, "Temp" represents a sensed temperature using a thermistor or other temperature sensing element for a location in or about the power converter, "V_{setup}" represents a correction constant obtained from a test set after a manufacturing step, and "V_{ext}" represents a signal from an external source that might assume the

values 0 and 1 to indicate the presence or absence of a paralleled power converter (see, *e.g.*, FIGURE 3 and the related description therefor). A constant "380" is a nominal number to describe the internal bus voltage setpoint $V_{bus\_setpoint}$. Other functional relationships including combinations of curve fits or other algorithmic relationships can be used within the broad scope of the present invention to meet the needs of a particular application. The controller 311 illustrated in FIGURE 3 may use the internal bus voltage setpoint $V_{bus\_setpoint}$ as a reference voltage to control the internal bus voltage V_{bus} illustrated and described with reference to FIGURE 3.

[0066] The functional representation for the internal bus voltage setpoint $V_{bus\_setpoint}$ to improve power conversion efficiency illustrated in FIGURE 6 may be further enhanced by a power converter operational state PC_{op_state} based on a command from a power system controller (see FIGURE 11 and the related description). An alternative functional representation for the internal bus voltage setpoint $V_{bus\_setpoint}$ may be used depending on the value of the power converter operational state PC_{op_state} indicating, for example, a command to reduce holdover time. An alternative functional representation may also be used for the internal bus voltage setpoint $V_{bus\_setpoint}$ if a power system employing the power converter anticipates a changing system operational state.

[0067] The use of tables, functional relationships, and curve fits to control an operating parameter for a controller of a power converter, constructed according to the principles of the present invention, can advantageously use the extensive data ordinarily acquired by test fixtures at various stages of the manufacturing process. The test fixtures are generally configured to sweep a broad range of operating conditions from a particular power converter, or from a representative power converter, or from power converters produced during a run of

representative power converters, and can even operate the power converter over a range of temperatures and for an extended period of time (*e.g.*, during "burn in"). A test fixture can be arranged to operate a power converter over a range of trial values for a controllable parameter and to select a value that provides a preferable operating efficiency for the particular power converter under test. Thus, the efficiency program for a particular power converter can be tailored to represent the particular characteristics of the individual components from which the power converter is built. In a preferred arrangement, the test fixture is programmed to automatically search for the best value for the controllable parameter.

[0068] Recognizing that automatic test equipment ("ATE") programs can be configured to perform thousands of tests on a representative unit, every reasonable combination of parameters can generally be practically searched for optimal efficiency over a given operating range. Reasonable combinations of parameters would be those that allow the power converter to maintain transient specifications for that operating range. These parameters can be determined, for example, using design equations and spreadsheets employing techniques well known in the art. The ATE data can then be reduced to a small lookup table containing the proper optimization parameters for the given operating range. Small variations in power converter test data would be expected over a production run. Optimizing every production power supply would be costly in certain production environments, providing diminishing returns for the effort. Nonetheless, it could be done if the resulting efficiency improvement would justify the effort. A practical option would be to sample power converters from all or selected production runs based on operating experience.

[0069] It is recognized that the timescale for the response of a controller to different internal and external stimuli can preferably be different. For example, the voltage level of an internal

bus, which generally depends on charging and discharging a capacitor, might be practically changed over a period of hundreds of milliseconds, or even seconds, whereas the switching frequency of a power conversion stage or the timing delay between power switch conduction intervals can be readily changed on a much faster time scale, ultimately on a cycle-by-cycle basis. It may even be inappropriate to substantially change operating parameters such as an internal bus voltage level over intervals of time shorter than several seconds. Some internal operating characteristics or parameters would inherently change or would be inherently varied over a relatively long period, such as the input current of an ac front end, compared to other time scales within a power converter, and require a period of time to sense or alter an average or peak value. The internal parameters may be monitored over a longer time interval before the controller responds to a change in an internal operating characteristic or an output characteristic to augment power conversion efficiency.

[0070] Thus, for example, a controller may control an internal operating characteristic of a power converter in a step-by-step manner during an efficiency enhancement (*e.g.*, optimization) process on a time scale substantially different from a time scale for controlling the duty cycle of the power converter. A parameter can be controlled on a slow timescale by using a digital representation of a low pass filter to retard changes in a parameter. An exemplary equation representing a low pass filter implemented over discrete time steps is:

$$V_{bus,n} = (1-\tau)\cdot V_{bus,n-1} + \tau \cdot V_{bus,desired}$$

where "$V_{bus,n}$" represents a filtered bus reference voltage at time step "n" to control an internal bus voltage on a slow time scale, "τ" represents a parameter that sets the time scale for the filtering process, "$V_{bus,n-1}$" represents the filtered bus reference voltage at the previous time step

"n-1," and "$V_{bus,desired}$" represents a desired, optimized bus voltage produced by a functional relationship or a table as described hereinabove.

[0071] In a related embodiment, a controller for a power converter may enhance (*e.g.*, optimize) the operating efficiency (or other desirable parameter) of the power converter in response to a sensed or signaled internal operating characteristic and/or an output characteristic, using parameters measured on a representative power converter. For example, a multidimensional table or other functional representation of a value to control an internal operating characteristic or an output characteristic of the power converter could be derived from testing one or more representative power converters, as opposed to testing the actual power converter to be controlled. Multidimensional inputs to such a table or other functional representation may include, without limitation, signals representing an internal operating characteristic, an output operating characteristic, a power converter parameter measured during a test or characterization phase, and/or a signal representing an environmental parameter.

[0072] During a typical power converter product development process, a product design may proceed through several stages, for example, prototyping, pilot (or small volume) production, characterization and/or qualification testing, safety agency and electromagnetic interference ("EMI") compliance testing, highly accelerated life testing, highly accelerated stress screening, and final release to production. During the characterization and/or qualification testing phase, one or more representative power supplies may be subjected to extensive testing to ensure compliance with the end specification. This testing may be automated by one or more racks of automated test equipment, enabling possibly many thousands of individual tests to be performed.

[0073] During an exemplary characterization testing stage, a representative power converter may be extensively tested over a wide variety of operating conditions. The characterization test may measure and collect thousands, or tens of thousands, of individual data points. These data may then be compiled into one or more multidimensional tables or other functional representation(s) and used by the control circuit to adjust an internal operating characteristic or an output characteristic of the power converter in order to operate the power converter at or near an optimal efficiency for a given set of conditions, while still enabling the power converter to meet its required specification. The characterization testing may also be repeated after a new manufacturing run to characterize the currently manufactured product.

[0074] Turning now to FIGURE 7, illustrated is a block diagram of an embodiment of a power converter constructed according to the principles of the present invention. In the exemplary embodiment illustrated in FIGURE 7, a block diagram of an ac input, power factor correction, and dc output power converter is depicted. The power converter operates from a power source providing 85 to 264 V ac input, and provides outputs of +12V and 3.3VSB (a standby voltage). The power converter also provides output signals PS_ON and POK indicating, respectively, that the power converter is turned on and power is "OK," as well as other "communications" signals typically provided between a power converter and a host system. It is readily understood by those skilled in the art that there are many ways to design an ac-to-dc power converter, and correspondingly there are many possible block diagrams that could suitably depict an exemplary power converter. It is also understood that the spirit and scope of the present invention is not limited to ac-to-dc power converters, but may encompass any type of power converter, including ac and/or dc input, as well as ac and/or dc output. Multiple input

and/or multiple output power converters are also within the spirit and scope of the present invention.

[0075] FIGURE 7 illustrates many of the constituent blocks of a power converter that may be controlled, as well as many of the internal nodes that may be measured and/or controlled, to improve operating efficiency. For example, a switching frequency of the boost field-effect transistors ("FETs"), and/or the bridge, may be adjusted based on operating conditions and/or on a system operational state to improve efficiency. Additionally, the voltage on the 400V bus may be adjusted, or the timing between bridge switches and a synchronous rectifier device ("sync rect") may be adjusted.

[0076] Turning now to FIGURE 8, illustrated is a block diagram of an embodiment of a power converter (*e.g.*, an ac-to-dc power converter) constructed according to the principles of the present invention and demonstrating in more detail possible control and alarm circuit connections. These control and alarm circuits may be realized using dedicated firmware-driven microcontrollers, digital control integrated circuits, application specific integrated circuits, field-programmable gate arrays, or any suitable electronic circuitry. The power factor correction ("PFC") control and primary alarm blocks (part of the primary control) of FIGURE 8 illustrate some of the many internal nodes and circuits that may be measured and controlled. For example, the primary controller may monitor the input line voltage, frequency, and current, *etc*. It may also monitor the PFC output bus voltage (shown here as the 400V bus, although the bus voltage may be controlled to other voltage levels). The primary controller may control the PFC boost power switches using a variety of control techniques, including fixed and variable frequency, continuous current mode, discontinuous current mode, or critically continuous inductor current, to name but a few. The power converter could also employ additional components to achieve,

for example, soft switching, with the controller capable of measuring and/or altering operating parameters affecting these additional components. The primary controller may also be capable of communicating with a secondary controller, and this communication may be bidirectional.

[0077] The secondary controller, including the pulse-width modulation ("PWM") control and alarm circuits, may monitor and control the parameters shown in FIGURE 8, as well as others not shown. The secondary control can thus be used to control, among other things, switching frequency, operating mode, output voltage, timing relationships, *etc*. The secondary control may advantageously also enable or disable the operation of individual power switches (or banks of power switches) to improve power conversion efficiency. The illustrated embodiment of FIGURE 8 also shows a means of communication allowing the power converter to communicate with a wide variety of devices including, but not limited to, a host processor, one or more pieces of automated test equipment, or another power converter. The communication protocol in the illustrated embodiment is a wired I^2C bus, but could be realized with any suitable communication means or protocol, including wired and wireless, optical, radio frequency, *etc*. Additionally, the communications means need not be restricted to the secondary side, but may be located on the primary side, or may be on both primary and secondary sides.

[0078] Turning now to FIGUREs 9A thru 9F, illustrated are examples of how power converter efficiency can vary as a function of operating conditions and operating environment in accordance with the principles of the present invention. The curves in FIGUREs 9A thru 9F are merely illustrative of a few of the parameters or environmental conditions affecting power conversion efficiency, and are by no means meant to be exhaustive. In addition, the curve shapes and variations illustrated in FIGUREs 9A thru 9F are meant for illustrative purposes only.

The efficiency of different power converter designs may vary in a manner different from the exemplary curves.

[0079] In FIGURE 9A, the efficiency of the PFC section is illustrated as a function of both output power and input line voltage. In FIGUREs 9A thru 9F, the arrows point in the direction of an increasing parameter. In FIGURE 9B, the efficiency of the dc-to-dc section is illustrated as a function of both output power and bus voltage. In FIGURE 9C, the efficiency of the PFC section is illustrated as a function of both output power and switching frequency at a single line voltage. A family of such curves could be generated at different ac line voltages. In FIGURE 9D, the efficiency of the dc-to-dc section is illustrated as a function of both output power and switching frequency at a single bus voltage. A family of such curves could be generated at different dc bus voltages. In FIGURE 9E, the efficiency of the power converter (PFC plus dc-to-dc sections) is illustrated as a function of both output power and bus voltage at a single line voltage. A family of such curves could be generated at different ac line voltages. Lastly, in FIGURE 9F, the efficiency of the power converter (PFC plus dc-to-dc sections) is illustrated as a function of both output power and the timing delay between the bridge and synchronous rectifier switches, at a single line voltage. A family of such curves could be generated at different ac line voltages. Clearly, many other relationships could be measured for their effect on power converter efficiency including, but not limited to, temperature (internal and/or external), altitude, fan speed, number of power switching devices enabled, *etc*.

[0080] The number of different relationships that could be measured and data points collected is limited only by the ingenuity of the test engineer, time, and data memory resources. Over many such projects, an engineer may learn that certain relationship data has more of an impact on efficiency than others, and may learn how to intelligently limit the number of tests

performed and data points collected to only those relationships having the greatest affect on efficiency.

[0081] Once the data is collected on one or more representative power converters, multidimensional data table(s) or other functional representation(s) may be stored into the internal control memory of the power converter for use during operation. This stored data could include, for example, a look-up table, an algorithm, or any other suitable method of converting test data into an actionable control parameter. For example, assume an exemplary power converter constructed according to the principles of the present invention was operating in a server, perhaps in a data center. The exemplary power converter may sense one or more environmental and operating conditions including a system operational state. The power converter may determine that it is operating at 20% load, at 120V ac input at 59.9Hz, with an inlet ambient temperature of 35°C (other parameters could also be measured), and that the power system is operating at full operational performance. The primary and/or secondary controller(s) may then access a stored look-up table that specifies, for example, the proper switching frequency, bus voltage operating conditions, the number of interleaved phases to enable, and switch timing relationships in order to improve or optimize efficiency. The controllers may be programmed to wait for a predetermined amount of time at a given operating condition before making any adjustment. This type of delay could allow the power converter to avoid making an unnecessarily large number of adjustments.

[0082] It may be advantageous to limit the range of possible adjustments to only those values that allow the power converter to remain within specified operating requirements during any operating condition specified in a requirements document. It may also be advantageous to limit the range of possible adjustments to only those values that ensure that the components of

the power converter do not exceed maximum stress levels, thereby improving reliability and reducing component or power converter failures. For example, a requirements document for a power converter may specify operation under a number of transient conditions, such as output load transients, input transients, brown-out conditions, line drop-out conditions, temperature transients, *etc*.

[0083] Turning now to FIGURE 10, illustrated is an ac input voltage waveform including an exemplary input line voltage dropout transient, showing time histories of possible internal bus voltages in accordance with the principles of the present invention. The FIGURE shows time histories of possible internal bus voltages, and an ac input voltage waveform with a drop-out period 1003 during which no ac input voltage is present. Illustrated for the internal bus voltages is a portion in which the slope 1001 of the internal bus voltage is load dependent. Also illustrated in the FIGURE is a bus undervoltage limit 1002. Power converters are often required to continue to provide output power for a period of time with the ac input voltage at or near zero. This time is typically referred to as the holdup time. When the input line voltage drops out, the dc-to-dc power converter section (see, *e.g.*, FIGURE 3) will continue to operate, pulling energy from the holdup capacitors, thereby reducing the voltage on the bus (designated V_{bus} in FIGURE 3). The bus voltage will continue to fall until the line voltage is restored. Note that the slope of the bus voltage will be steeper at a higher output load current. If the bus voltage is allowed to reduce below an under voltage limit, the dc-to-dc power converter will not be able to support the load and maintain regulation, thereby resulting in an out-of-specification condition (*e.g.*, for a particular system operational state). If the exemplary power converter of FIGURE 10 is operating at Bus Voltage 1, the power converter can operate within specification, but may be operating at a lower efficiency than desired. If, however, the power converter adjusted its bus

voltage to Bus Voltage 2 in an effort to improve efficiency, the bus voltage will dip below the undervoltage limit before the end of the drop-out period. Thus, Bus Voltage 1 has more than adequate margin for the load, but efficiency may not be optimized. Bus Voltage 2 may provide higher efficiency, but cannot meet the dropout specification. Bus Voltage 3 may be the most efficient operating point for which operating specifications can be maintained. The power supply system would be crafted to select Bus Voltage 3.

[0084] It should ordinarily be assumed that a maximum specification power transient can occur at any time during power supply operation without warning. This assumption clearly limits opportunities for optimization. A given server with a particular configuration of memory, disk drives, *etc*., will have a maximum load capability, which is typically less than the power supply's maximum load specification. This maximum load could be characterized at system boot up and communicated to the power supply, then stored, for example, in a flash memory. The power supply control system could add margin to the maximum load number and thus know the maximum possible load for the server to which it is coupled. This information can then be used to compute the optimization parameters such that specification conformance is maintained.

[0085] Thus, a power converter constructed according to the principles of the present invention may sense a variety of input/output operating parameters and calculate, for example, the minimum (or a safe) bus voltage that could both improve efficiency and ensure that the power converter can maintain the proper holdup time through a line dropout event. This is illustrated by Bus Voltage 3 in FIGURE 10. For a given output load condition, adjusting the bus voltage to Bus Voltage 3 both improves efficiency and ensures compliance with the specification. Thus, the exemplary power converter is capable of using a multidimensional data table(s) or other functional representation(s), in conjunction with sensed operating parameters, to

determine an operating point with improved efficiency that also allows the power converter to maintain compliance with a specification.

[0086] There are many examples where adjustments to improve efficiency while maintaining compliance with a specification will require a power converter to make intelligent adjustments, possibly combining data stored in a multidimensional data table(s) or other functional representation(s) with sensed operating parameters in the adjustment computation. One such example concerns switching frequency adjustments. It may be advantageous to reduce a switching frequency under, for example, lighter output load conditions. However, if the load were to suddenly increase, the power converter controller should ensure that the magnetic components will not be detrimentally affected (by possibly saturating) at the combination of a higher load condition and a lower frequency operating condition, prior to the controller adjusting the switching frequency to a level more appropriate with the new load condition. Thus, a power system controller may consider a system operational state when altering a power converter switching frequency.

[0087] Another example can be found in switch timing adjustments, illustrated in FIGURE 9F. The improved switch timing is often dependent on input or output current levels. For example, switch timing to improve efficiency at a lighter load may result in cross conduction at heavier loads (or vice versa), thereby causing a detrimental operation and possible failure of the power converter.

[0088] Turning now to FIGURE 11, illustrated is a block diagram of an embodiment of a power system coupled to loads and including power converters controlled by a power system controller constructed according to the principles of the present invention. The loads are represented by a plurality of servers (designated "SVR_1…SVR_n" and also referred to as

"SVR") powered by respective power converters (designated "PU_1…PU_n" and also referred to as "PU") over respective power buses (designated "PB_1…PB_n" and also referred to as "PB"). Each server SVR may be individually coupled to a respective power converter PU for its power source as illustrated herein, or may be coupled to more than one power converter PU and powered in a redundant manner to form multiple redundant power converters PU. The power system controller (designated "PSC") may also be powered by one of the illustrated power converters PU, or by another power converter not shown.

[0089] The power converters PU are coupled to the power system controller PSC over respective power converter communication buses (designated "PCBUS_1…PCBUS_n" and also referred to as "PCBUS") that conduct signals therebetween to communicate requests for a power converter operational state PC_{op_state} from the power system controller PSC to a power converter PU. The power system controller PSC may also be coupled over a bus (designated "BUS_env") to a circuit element (not shown) signaling an environmental parameter such as a component temperature. In addition, the power system controller PSC may be coupled over a bus (designated "BUS_test") to a signal source such as a manufacturing test set that provides a power converter parameter measured after a manufacturing step. The power system controller PSC receives signals representing a power converter status PC_{status} from the power converters PU over the respective power converter communication buses PCBUS and transmits commands thereover for the power converter operational states PC_{op_state} to the power converters PU. The commands for the power converter PU to enter the power converter operational states PC_{op_state} can be used to enhance (*e.g.*, optimize) an operational efficiency or reliability of the power converter PU and at a power system level.

[0090] An exemplary set of power converter operational states PC_{op_state} and an associated description thereof is illustrated in TABLE I below. A power converter operational state PC_{op_state} introduces an opportunity, which may be based on a signal received from a server SVR, to control an internal operating characteristic of a power converter PU, such as an internal bus voltage, a switching frequency, or altering a power conversion topological operation such as disabling (or reducing the effectiveness of) active power factor correction or altering the number of actively driven synchronous rectifiers. The power converter operational states PC_{op_state} indicate an operational condition beyond controlling an external characteristic such as an output voltage set point controlled by a VID signal. An example of a response to a signal indicating a power converter operational state PC_{op_state} from the power system controller PSC includes disabling (or setting in a standby mode) one of a plurality of redundant power converters PU during a low power condition, such as during a reduced software load sensed at a power system level, with or without changing an output characteristic such as an output voltage of the remaining power converters PU. A power converter operational state PC_{op_state} may be determined from a signal from a server SVR indicating a processor core state, a software load on the power system, or a level of power system criticality.

TABLE I

PC_{op_state}	Power Converter Operational State	Power Converter Operational State Description
0	Fully operational	Full power capability. All power converter components operational at full performance level
1	Reduced load	Reduced internal bus voltage (possibly reducing holdover time). Switching frequency reduced. Switch timing optimized for lighter load.
2	Light load	Elements of $PC_{op\text{-}state1}$ plus active power factor correction control

		off or diminished, at least one synchronous rectifier switch disabled, and/or an interleaved phase disabled. Bus voltage reduction.
3	Very light load	Elements of $PC_{op\text{-}state2}$ plus substantial bus voltage reduction. Disable phases in PFC.
4	Reduced Redundancy	Elements of $PC_{op\text{-}state3}$ plus temporarily disabling a power converter in a redundant set, but power converter remaining in a standby condition. PFC disabled at high line.
5	Further capability reduction	Redundant supply shut down. PFC disabled at high line.

[0091] The C-states corresponding to the PC_{op_states} are illustrated in TABLE II below for a representative system design. Resulting estimated power converter dissipation for a representative power converter design at 10% load is illustrated in the right column of TABLE II to illustrate the potential for dissipation reduction in a system constructed according to the principles of the present invention.

TABLE II

PC_{op_state}	**Corresponding C-State**	**Comments**	**Power converter dissipation at 10% load**
0	C0	Limited efficiency optimization.	75 W
1	C1	Moderate efficiency optimization. Transition back to $PC_{op\_state} = 0$ in tens of microseconds.	73W
2	C2	Moderate efficiency optimization. Transition back to $PC_{op\_state} = 0$ in several ms.	71 W
3	C3	Good efficiency optimization. Transition back to $PC_{op\_state} = 0$ in tens of ms.	58 W

4	C4	Maximum power savings with redundancy. Transition back to $PC_{op\_state} = 0$ in 50 ms.	38 W
5	Deep C4	Maximum possible power savings. Transition back to $PC_{op\_state} = 0$ in 100 ms.	19 W

[0092] Each power converter PU responds to a command for a power converter operational state PC_{op_state} by enhancing (*e.g.*, optimizing) its operating efficiency under the requested power converter operational state PC_{op_state}. The power system controller PSC may command different power converter operational states PC_{op_state} to different power converters PU in the power system. Thus, one power converter PU may be disabled, while the other power converters PU continue to operate under a light system load, preferably with a consideration of measured operating efficiencies of the particular power converters PU installed. In such manner, a higher operating efficiency can be achieved on a system-level basis than can be achieved in an environment without such system-level communication. Alternatively, the power system controller PCS may sequentially operate different power converters PU at different times to reduce the overall power system failure rate by reducing the operating time of individual power converters PU.

[0093] The servers SVR communicate with the power system controller PSC over respective server communication buses (designated "SVRBUS_1…SVRBUS_n" and also referred to as "SVRBUS") to communicate data to establish a system operational state with respect to the servers SVR. The data may include a processor P-state or C-state, a signal indicative of a level of system or power system functionality, and/or a signal anticipating a change in power system functionality. In a preferred embodiment, the various communication

buses are serial data buses such as I^2C buses (or any other suitable communication protocol). In an alternative embodiment, parallel buses can be used.

[0094] As mentioned above, the power system controller PSC receives signals representing a power converter status PC_{status} from the power converters PU over a respective power converter communication bus PCBUS. An exemplary set of power converter statuses PC_{status} is shown below in TABLE III with an associated description thereof. Additional (or fewer) status conditions could be used based on the needs of each system. For example, a power converter status flag setting of "1" may indicate an overheated condition for a power converter component, or a high level of ripple voltage on an internal circuit node, either event representing an out-of-specification or unanticipated operating condition for the power converter PU. A power converter status flag setting of "3" may indicate a load failure, wherein a load (*e.g.*, server SVR) component draws a current beyond a rated value. The power system controller PSC may signal, as a consequence thereof, the need to replace a power converter PU, temporarily operate a power converter PU at a lower level of performance, or indicate a generally lower level of power system reliability. The power system controller PSC may employ power converter status data to enhance (*e.g.*, optimize) power system operating efficiency on a power system-level basis.

TABLE III

PC_{status}	Power Converter Status	Power Converter Status Description
0	Fully Operational	All power converter components operational at a full performance level
1	Failure Likely	Power converter operating with reduced operational capability
2	Failed	Power converter failed
3	Overloaded	Power converter unable to sustain an output voltage or current

[0095] In FIGURE 11, the power system controller PSC is illustrated as a block separate from the servers SVR. In an alternative embodiment, the power system controller PSC may be constructed as an element of one or more servers SVR, or as an element of one or more of the power converters PU.

[0096] Turning now to FIGURE 12, illustrated is a diagram of an embodiment of processor core states ("C-states") in accordance with the principles of the present invention illustrated. In particular, the diagram illustrates ACPI C-states including an active state C0, idle states C1, C2, C3, C4 and a Deep state C4 including transition times between idle states. The processor idle states are generally scheduled at a system level, and it may be possible to signal the power supply prior to transitions into and out of the idle states. With as little as several milliseconds' notice, a power supply could prepare itself for a state transition. Such notification could allow a much deeper optimization of efficiency than would otherwise be possible. Switch timing, frequency, bus voltage, *etc.*, could be changed prior to the idle state change to prepare for the transition in operating conditions. These parameter changes would be accomplished in a predictable, controlled fashion, thereby augmenting (*e.g.*, maximizing) power supply and system reliability. Adjustment of power converter operating characteristics would generally be done slowly, waiting seconds or even minutes in a given operating state before enhancing (*e.g.*, optimizing) parameters for efficiency.

[0097] Turning now to FIGURE 13, illustrated is an exemplary state transition diagram for a power converter constructed according to the principles of the present invention. The diagram illustrates power converter operational states PC_{op_state} based on commands from a power system controller and the allowable transition times therebetween. For example, the transition from the

first power converter operational state PC_{op_state1} to the fourth power converter operational state PC_{op_state4} is 5 milliseconds ("ms") or less, wherein the reverse transition is 15 ms or less.

[0098] Transitions among the power converter operational states PC_{op_state} illustrated in FIGURE 13 advantageously can be conditioned by the power system controller to control individual power converters to meet power system-level performance metrics. For example, a transition from the power converter operational state PC_{op_state0}, a "fully operational" state, to the first power converter operational state PC_{op_state1}, a "reduced load" state, may be performed in response to a system operational state requirement related to a processor core state signal indicating a transition of a processor core state from core state C0 to core state C1 or higher. The transitions may also be temporally conditioned. For example, persistent residence in the first power converter operational state PC_{op_state1} (*e.g.*, for a time period greater than 0.5 seconds) may enable a transition to the fourth power converter operational state PC_{op_state4} ("reduced redundancy"). A transition to the fifth power converter operational state PC_{op_state5} ("idle") may be enabled upon receipt of a power converter status of two $PC_{status2}$ ("failed power converter") and receipt of a system operational state such as a processor core state with a value greater than or equal to one. Logic enabling particular state transitions in an embodiment of the present invention based on a power converter status PC_{status} and on a system operational state can be readily constructed for a particular application.

[0099] Turning now to FIGURE 14, illustrated is a graphical representation of efficiency improvement as a function of power converter operational state PC_{op_state} for a representative power converter (*e.g.*, 1000 W power converter) constructed according to the principles of the present invention. The graphs illustrate power converter efficiency as a function of percent of load for the four states $PC_{op\_state} = 0$, 2, 3, and 4. As illustrated in the FIGURE, substantial

efficiency improvement can be attained at light levels of power converter loading, particularly in the deeper idle states of the system. Power converter dissipation corresponding to the efficiency data illustrated in FIGURE 14 is illustrated in FIGURE 15.

[0100] Turning now to FIGURE 16, illustrated is a graphical representation of efficiency improvement as a function of power converter operational state PC_{op_state} for a representative power system (*e.g.*, 1000 W power converter system) including two power converters (*e.g.*, 1000 W power converters) operating in parallel ("1 + 1") to provide a high level of power system reliability constructed according to the principles of the present invention. The graphs illustrate power converter efficiency as a function of percent of load for the five states $PC_{op\_state} = 0$, 2, 3, 4, and 5. As illustrated in the FIGURE, substantial efficiency improvement again can be attained at light levels of power converter loading, particularly in the deeper idle states of the system. In normal system operation, wherein both power converters are fully operational, each power converter necessarily operates at less than 50% of its rated load capacity. Thus, in such system arrangements, substantial opportunities exist and can be accommodated in an advantageous embodiment for improvement in system power conversion efficiency during an idle state. Power converter dissipation corresponding to the efficiency data illustrated in FIGURE 16 is illustrated in FIGURE 17.

[0101] Thus, a controller for a power converter advantageously providing improved power conversion efficiency and improved power system reliability both at a unit and a system level has been introduced. A load is configured to provide a signal representing a system operational state to a power system controller coupled thereto. The power system controller in turn provides a command to the power converter to transition to or enter into a power converter operational state in accordance with the system operational state and a power converter status. The power

system controller, therefore, induces the power converter to enter a power converter operational state. The power system controller may advantageously provide a command to the power converter to transition to or enter into a power converter topological state. The power converter includes a controller and a power switch configured to conduct for a duty cycle and to provide a regulated output characteristic at an output thereof. The power converter controller is configured to provide a signal to control the duty cycle of the power switch as a function of the output characteristic. The controller thereby regulates an internal operating characteristic of the power converter to improve an operating efficiency of the power converter depending on a value of a system operational state. Thus, by communicating operational data among the power converters of the power system in accordance with a power system controller, the operational efficiency of the power system and its reliability can be enhanced (*e.g.*, optimized) at a level beyond that which can be achieved with more limited powering arrangements. The systems introduced herein may be implemented as hardware (including an integrated circuit such as an application specific integrated circuit), or may be implemented as software or firmware for execution by a computer processor. In particular, in the case of firmware or software, the exemplary embodiment can be provided as a computer program product including a computer readable storage structure embodying computer program code (*i.e.*, software or firmware) thereon for execution by the computer processor.

[0102] Those skilled in the art should understand that the previously described embodiments of a controller for a power converter and related methods are submitted for illustrative purposes only. Those skilled in the art understand further that various changes, substitutions, and alterations can be made to the controller without departing from the spirit and scope of the invention in its broadest form. In addition, other embodiments capable of providing the

advantages as described hereinabove are well within the broad scope of the present invention. While the controller and method have been described as providing advantages in the environment of a power converter, other applications therefor such as a controller for a motor or other electromechanical device are well within the broad scope of the present invention.

[0103] For a better understanding of power electronics, see "Principles of Power Electronics," by J. G. Kassakian, M. F. Schlecht and G. C. Verghese, Addison-Wesley (1991). For a better understanding of semiconductor devices and processes, see "Fundamentals of III-V Devices," by William Liu, John Wiley and Sons, (1999). For a better understanding of gallium arsenide processing, see "Modern GaAs Processing Methods," by Ralph Williams, Artech House, Second Ed. (1990). The aforementioned references are incorporated herein by reference.

[0104] Also, although the present invention and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the invention as defined by the appended claims. For example, many of the controllers discussed hereinabove can be implemented in different methodologies and replaced by other processes, or a combination thereof, to form the devices providing improved efficiency for a power converter as described herein.

[0105] Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure of the present invention, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the present invention.

Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.

WHAT IS CLAIMED IS:

1. A power converter coupled to a load, comprising:

a power switch configured to conduct for a duty cycle to provide an output characteristic at an output thereof; and

a power converter controller configured to receive a signal from said load indicating a system operational state of said load and control an internal operating characteristic of said power converter as a function of said signal.

2. The power converter as recited in Claim 1 wherein said power converter controller is further configured to provide another signal to control said duty cycle of said power switch as a function of said output characteristic and in accordance with said signal.

3. The power converter as recited in Claim 1 wherein said power converter controller is configured to adjust said internal operating characteristic over a period of time.

4. The power converter as recited in Claim 1 wherein said load is a processor and said system operational state is dependent on one of a core state and a performance state of said processor.

5. The power converter as recited in Claim 1 wherein said internal operating characteristic is selected from the group consisting of:

a gate drive voltage level of said power switch of said power converter,

a switching frequency of said power converter, and

an internal direct current bus voltage of said power converter.

6. A power system, comprising:

a power system controller configured to provide a signal characterizing a power requirement of a processor system; and

a power converter coupled to said processor system, comprising:

a power switch configured to conduct for a duty cycle to provide an output characteristic at an output thereof, and

a power converter controller configured to receive a signal from said power system controller to control an internal operating characteristic of said power converter as a function of said signal.

7. The power system as recited in Claim 6 wherein said power converter controller is further configured to provide another signal to control said duty cycle of said power switch as a function of said output characteristic and in accordance with said signal.

8. The power system as recited in Claim 6 wherein said power converter controller is configured to adjust said internal operating characteristic over a period of time.

9. The power system as recited in Claim 6 wherein said power requirement of a processor system is dependent on one of a core state and a performance state of said processor system.

10. The power system as recited in Claim 6 wherein said internal operating characteristic is selected from the group consisting of:

a gate drive voltage level of said power switch of said power converter,

a switching frequency of said power converter, and

an internal direct current bus voltage of said power converter.

11. A power system, comprising:

a power system controller configured to enable operation of components of a processor system to establish a state of power drain thereof, said power system controller configured to provide a signal to identify operation of said processor system in said state of power drain; and

a power converter, coupled to said processor system, comprising a power converter controller configured to receive said signal from said power system controller, to sense a power level of said state of power drain in response to said signal, and to control an internal operating characteristic of said power converter as a function of said power level.

12. The power system as recited in Claim 11 wherein said power converter further comprises a power switch configured to conduct for a duty cycle to provide an output characteristic at an output thereof, said power converter controller further configured to control said duty cycle of said power switch dependent on said output characteristic and in accordance with said power level.

13. The power system as recited in Claim 11 wherein said signal is provided upon startup of said processor system.

14. The power system as recited in Claim 11 wherein said power converter controller is configured to adjust said internal operating characteristic over a period of time.

15. The power system as recited in Claim 11 wherein said internal operating characteristic is selected from the group consisting of:

a gate drive voltage level of a power switch of said power converter,

a switching frequency of said power converter, and

an internal direct current bus voltage of said power converter.

16. A method of operating a power system, comprising:

enabling operation of components of a processor system to establish a state of power drain thereof;

providing a signal to identify operation of said processor system in said state of power drain;

sensing a power level of said state of power drain in response to said signal; and

controlling an internal operating characteristic of a power converter as a function of said power level.

17. The method as recited in Claim 16, further comprising:

inducing a power switch of said power converter to conduct for a duty cycle to provide an output characteristic at an output thereof; and

controlling said duty cycle of said power switch dependent on said output characteristic and in accordance with said power level.

18. The method as recited in Claim 16 wherein said signal is provided upon startup of said processor system.

19. The method as recited in Claim 16 wherein said controlling said internal operating characteristic comprises occurs over a period of time.

20. The method as recited in Claim 16 wherein said internal operating characteristic is selected from the group consisting of:

a gate drive voltage level of a power switch of said power converter,

a switching frequency of said power converter, and

an internal direct current bus voltage of said power converter.

POWER SYSTEM WITH POWER CONVERTERS HAVING AN ADAPTIVE CONTROLLER

ABSTRACT OF THE DISCLOSURE

A power system having a power converter with an adaptive controller. In one embodiment, a power converter coupled to a load includes a power switch configured to conduct for a duty cycle to provide an output characteristic at an output thereof. The power converter also includes a power converter controller configured to receive a signal from the load indicating a system operational state of the load and enable a power converter topological state as a function of the signal.

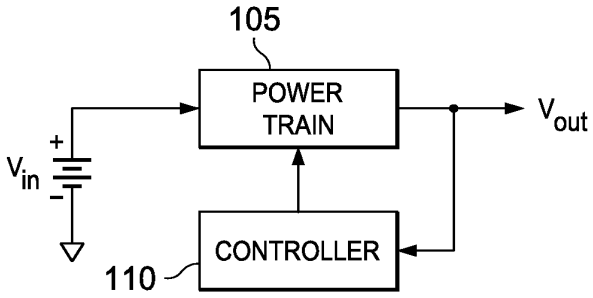


FIG. 1
(PRIOR ART)

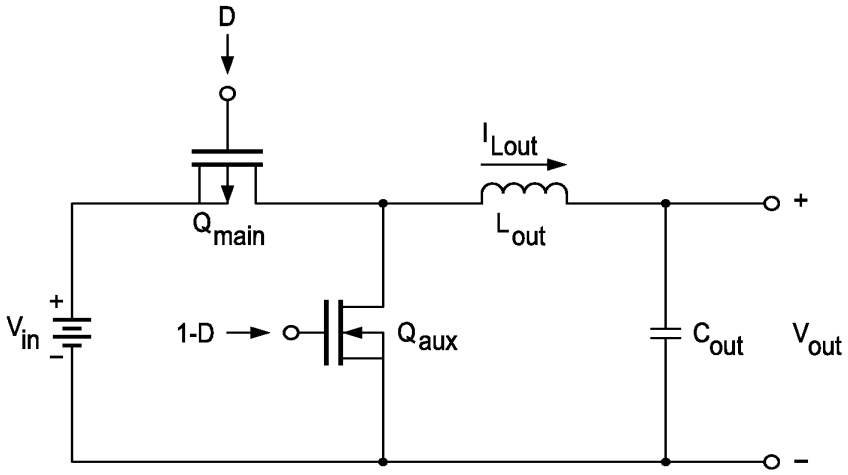


FIG. 2
(PRIOR ART)

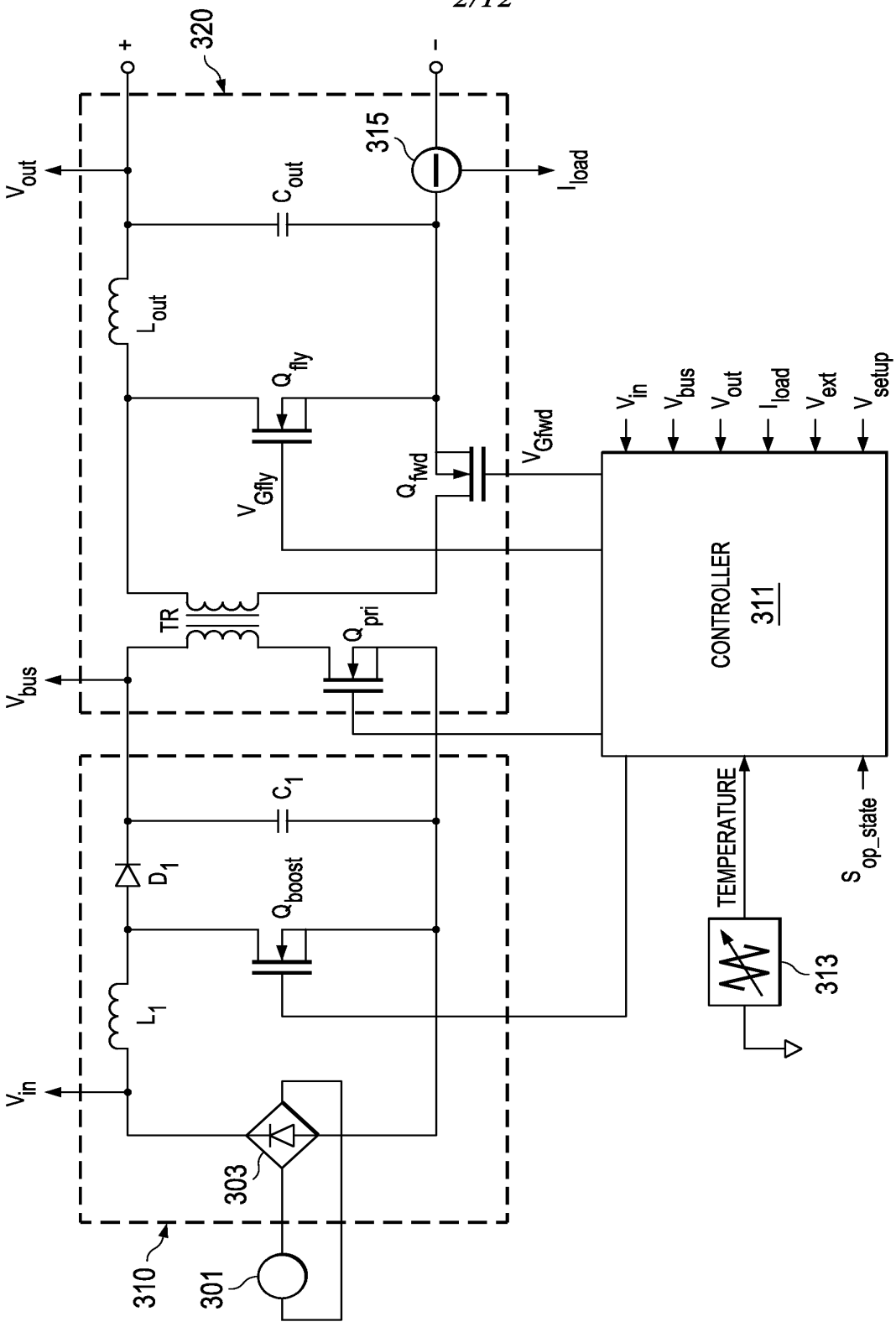

320
+
-
315
V_{out}
C_{out}
I_{load}
L_{out}
Q_{fly}
V_{Gfly}
Q_{fwd}
V_{Gfwd}
V_{in}
V_{bus}
V_{out}
I_{load}
V_{ext}
V_{setup}
CONTROLLER
311
TR
Q_{pri}
V_{bus}
C_1
D_1
Q_{boost}
L_1
V_{in}
TEMPERATURE
313
S_{op_state}
303
310
301

FIG. 3

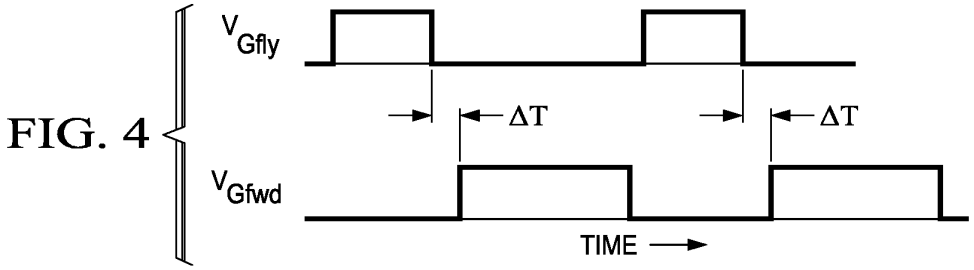


FIG. 4

LOAD CURRENT, A →

TEMPERATURE	0	10	20	30	40
< 30 C	20	22	24	26.5	29
> 30 C	21	23	25	27.5	30

V_{in} < 48 V

FIG. 5A

LOAD CURRENT, A →

TEMPERATURE	0	10	20	30	40
< 30 C	20.4	22.6	24.8	27.3	30
> 30 C	22	24	26	28.5	32

V_{in} > 48 V

FIG. 5B

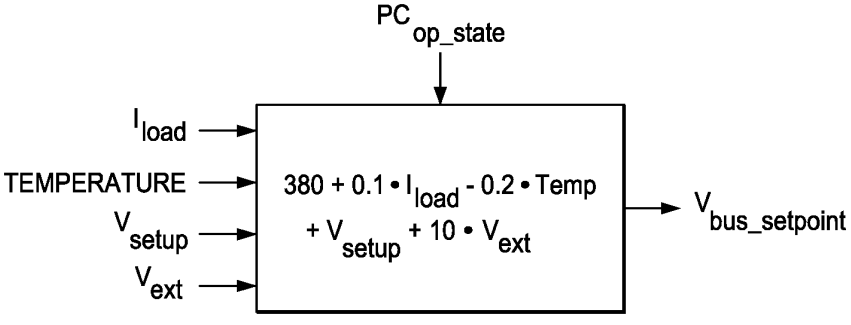


FIG. 6

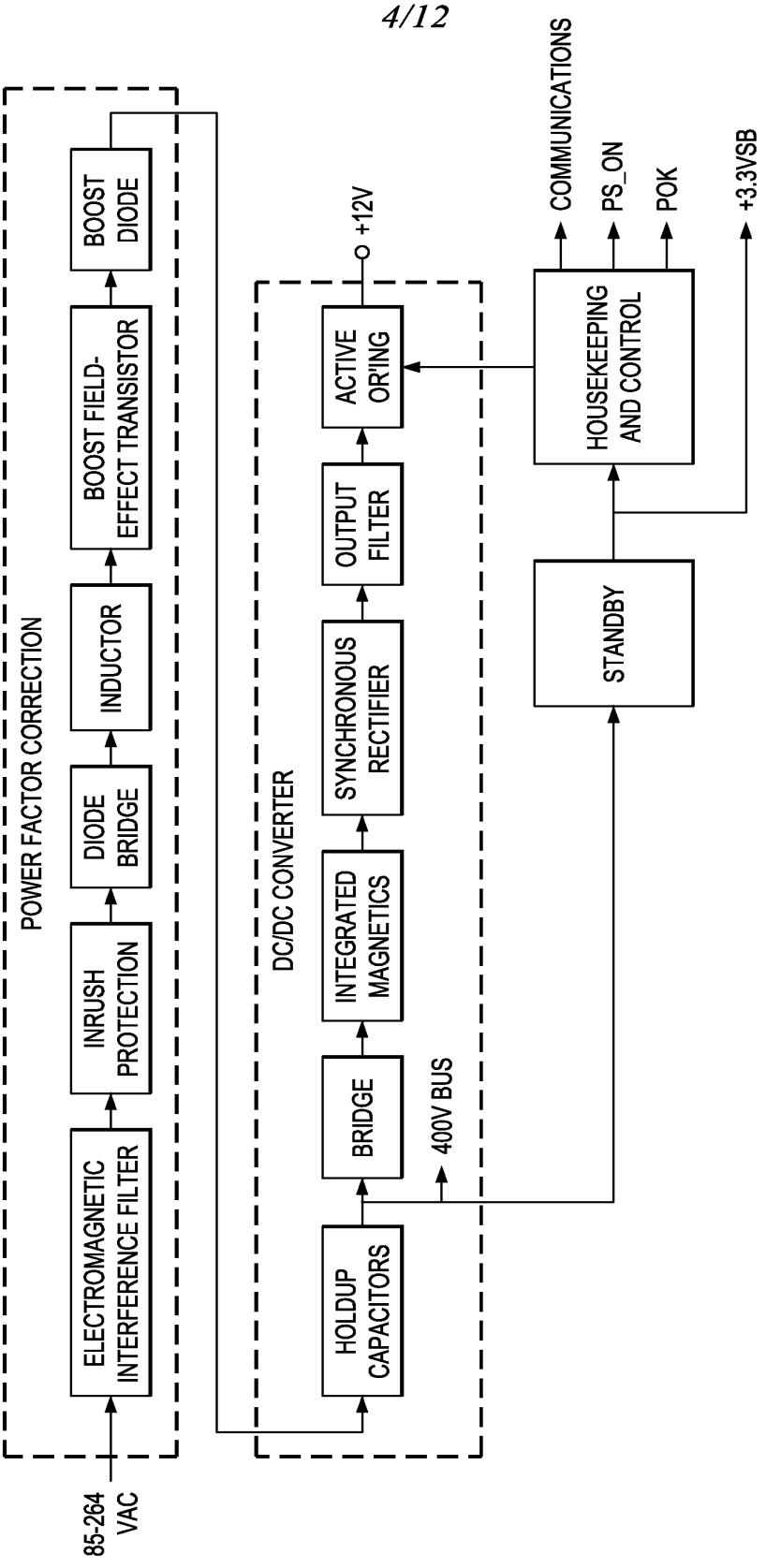

85-264 VAC
POWER FACTOR CORRECTION
ELECTROMAGNETIC INTERFERENCE FILTER
INRUSH PROTECTION
DIODE BRIDGE
INDUCTOR
BOOST FIELD-EFFECT TRANSISTOR
BOOST DIODE
DC/DC CONVERTER
HOLDUP CAPACITORS
BRIDGE
400V BUS
INTEGRATED MAGNETICS
SYNCHRONOUS RECTIFIER
OUTPUT FILTER
ACTIVE OR'ING
+12V
HOUSEKEEPING AND CONTROL
STANDBY
COMMUNICATIONS
PS_ON
POK
+3.3VSB

FIG. 7

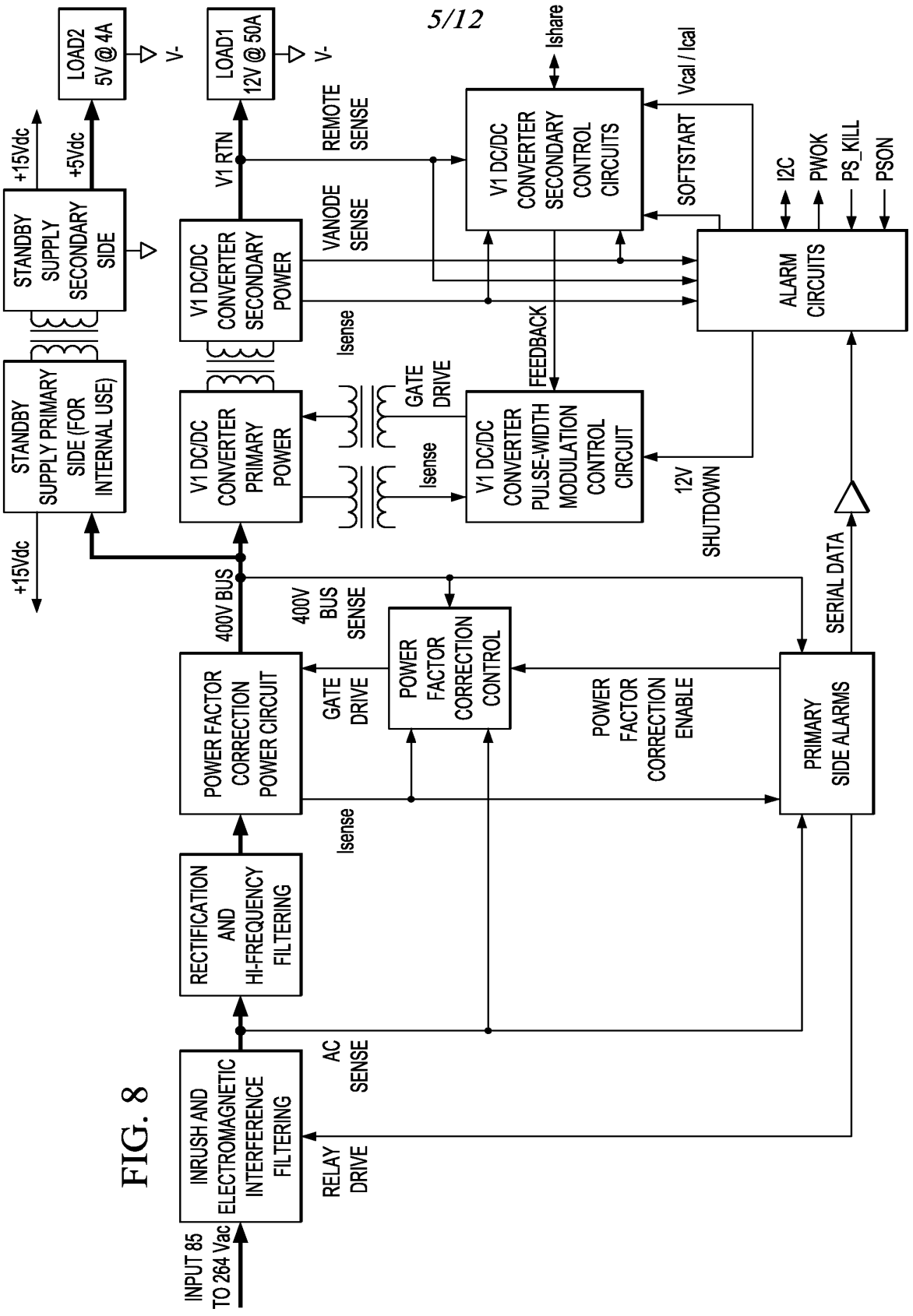

INPUT 85 TO 264 Vac
INRUSH AND ELECTROMAGNETIC INTERFERENCE FILTERING
RELAY DRIVE
AC SENSE
RECTIFICATION AND HI-FREQUENCY FILTERING
POWER FACTOR CORRECTION POWER CIRCUIT
Isense
GATE DRIVE
400V BUS
400V BUS SENSE
POWER FACTOR CORRECTION CONTROL
POWER FACTOR CORRECTION ENABLE
PRIMARY SIDE ALARMS
SERIAL DATA
V1 DC/DC CONVERTER PRIMARY POWER
Isense
GATE DRIVE
V1 DC/DC CONVERTER PULSE-WIDTH MODULATION CONTROL CIRCUIT
FEEDBACK
12V SHUTDOWN
V1 DC/DC CONVERTER SECONDARY POWER
VANODE SENSE
V1 RTN
REMOTE SENSE
V1 DC/DC CONVERTER SECONDARY CONTROL CIRCUITS
Ishare
Vcal / Ical
SOFTSTART
ALARM CIRCUITS
I2C
PWOK
PS_KILL
PSON
STANDBY SUPPLY PRIMARY SIDE (FOR INTERNAL USE)
+15Vdc
STANDBY SUPPLY SECONDARY SIDE
+15Vdc
+5Vdc
LOAD2 5V @ 4A
V-
LOAD1 12V @ 50A
V-

FIG. 8

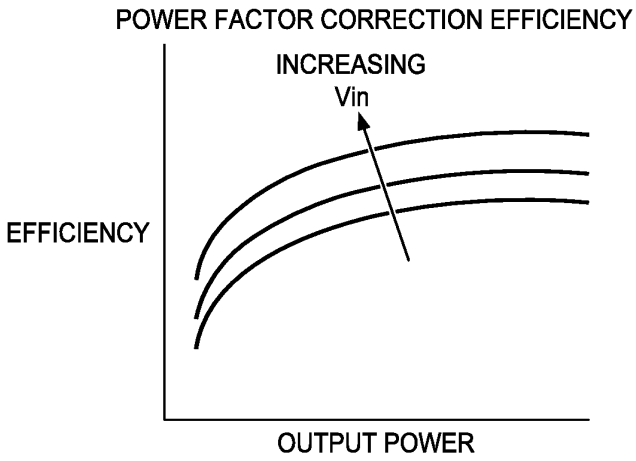


FIG. 9A

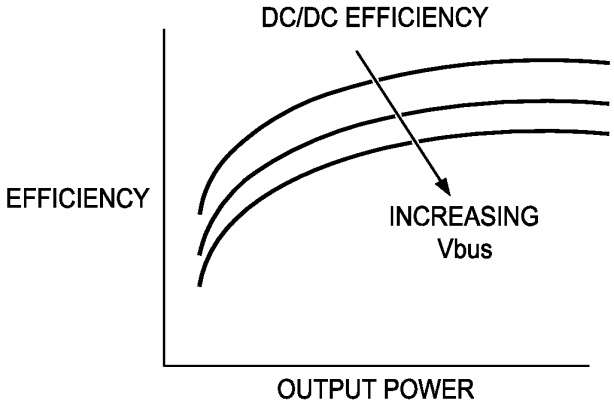


FIG. 9B

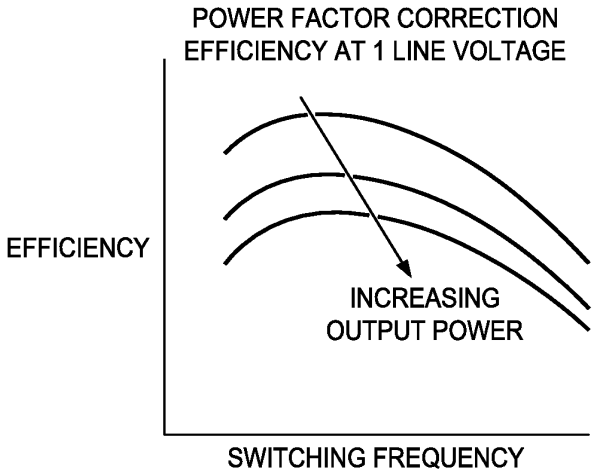


FIG. 9C

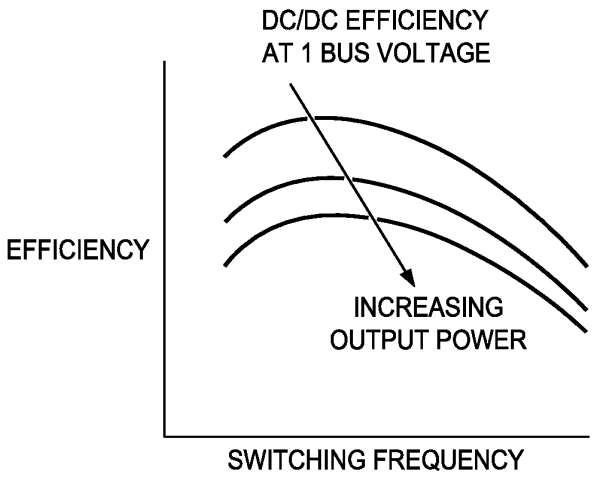


FIG. 9D

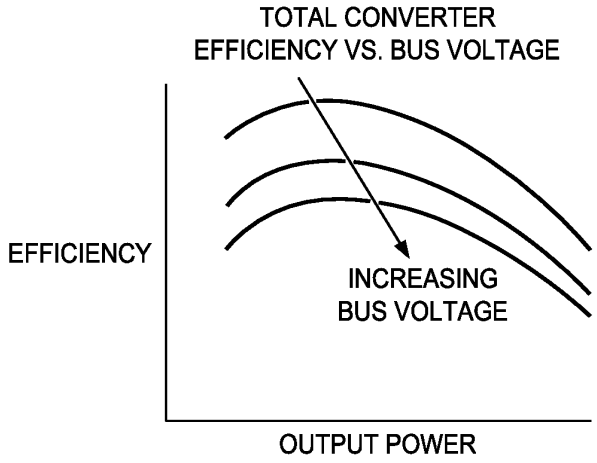


FIG. 9E

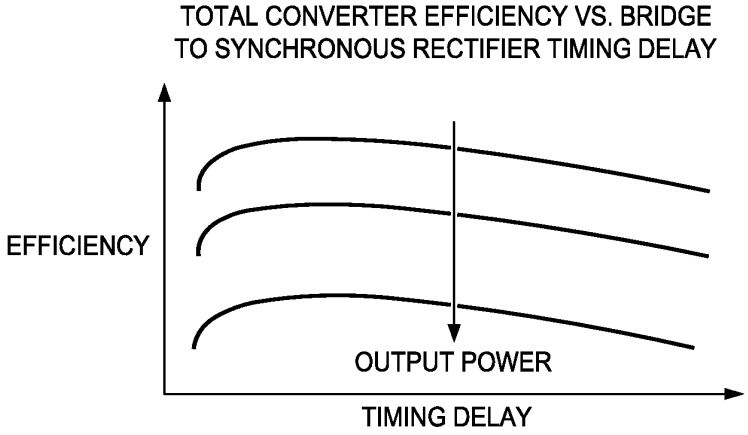


FIG. 9F

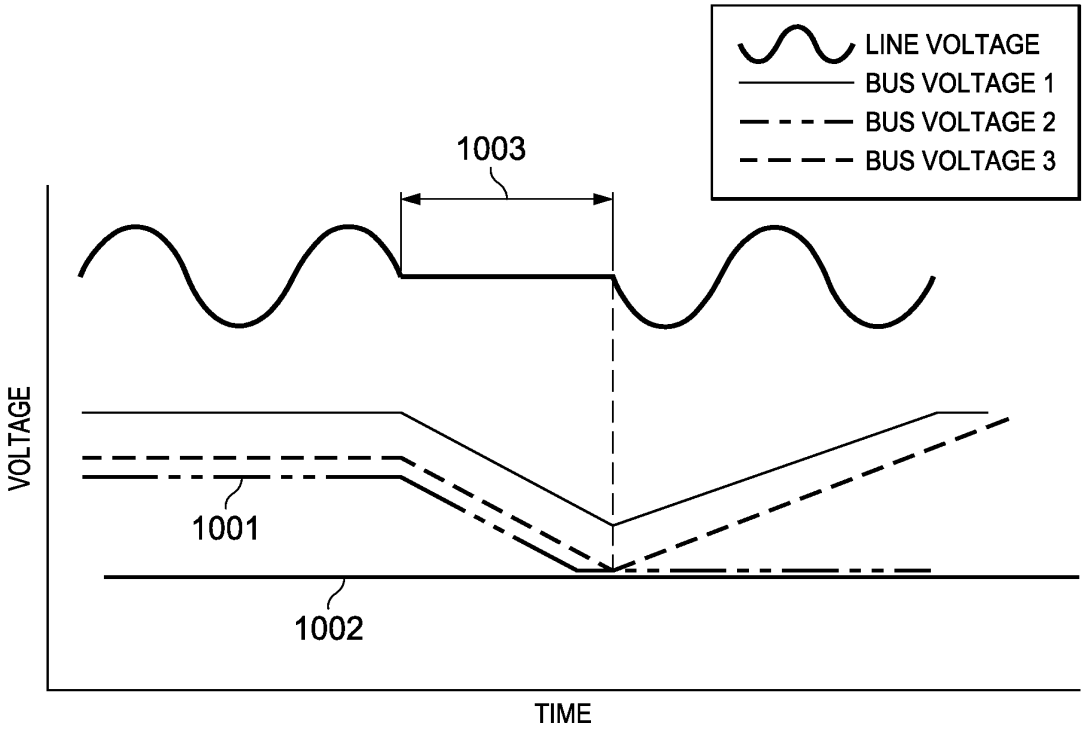

LINE VOLTAGE
BUS VOLTAGE 1
BUS VOLTAGE 2
BUS VOLTAGE 3
1003
VOLTAGE
1001
1002
TIME

FIG. 10

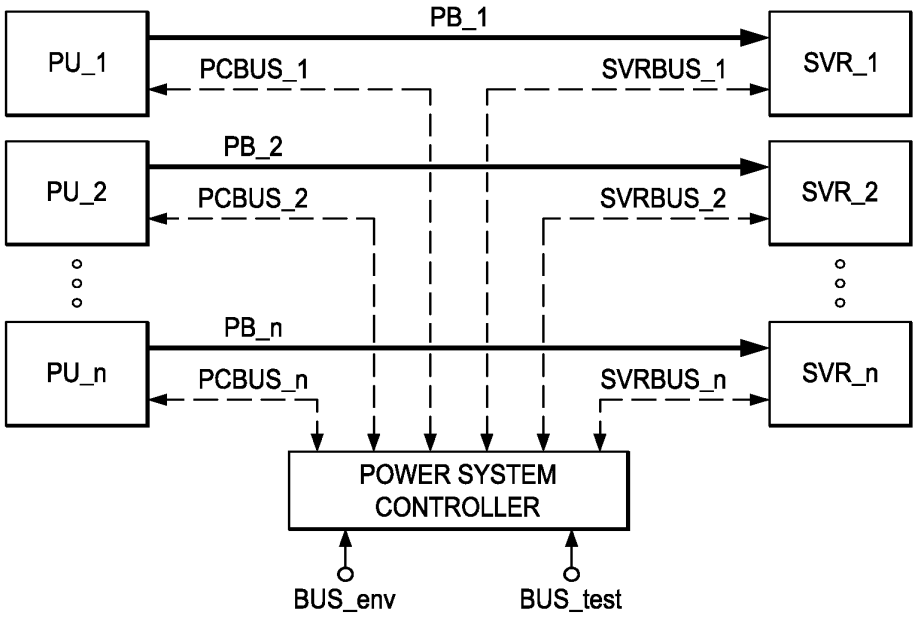

PB_1
PU_1
PCBUS_1
SVRBUS_1
SVR_1
PB_2
PU_2
PCBUS_2
SVRBUS_2
SVR_2
PB_n
PU_n
PCBUS_n
SVRBUS_n
SVR_n
POWER SYSTEM CONTROLLER
BUS_env
BUS_test

FIG. 11

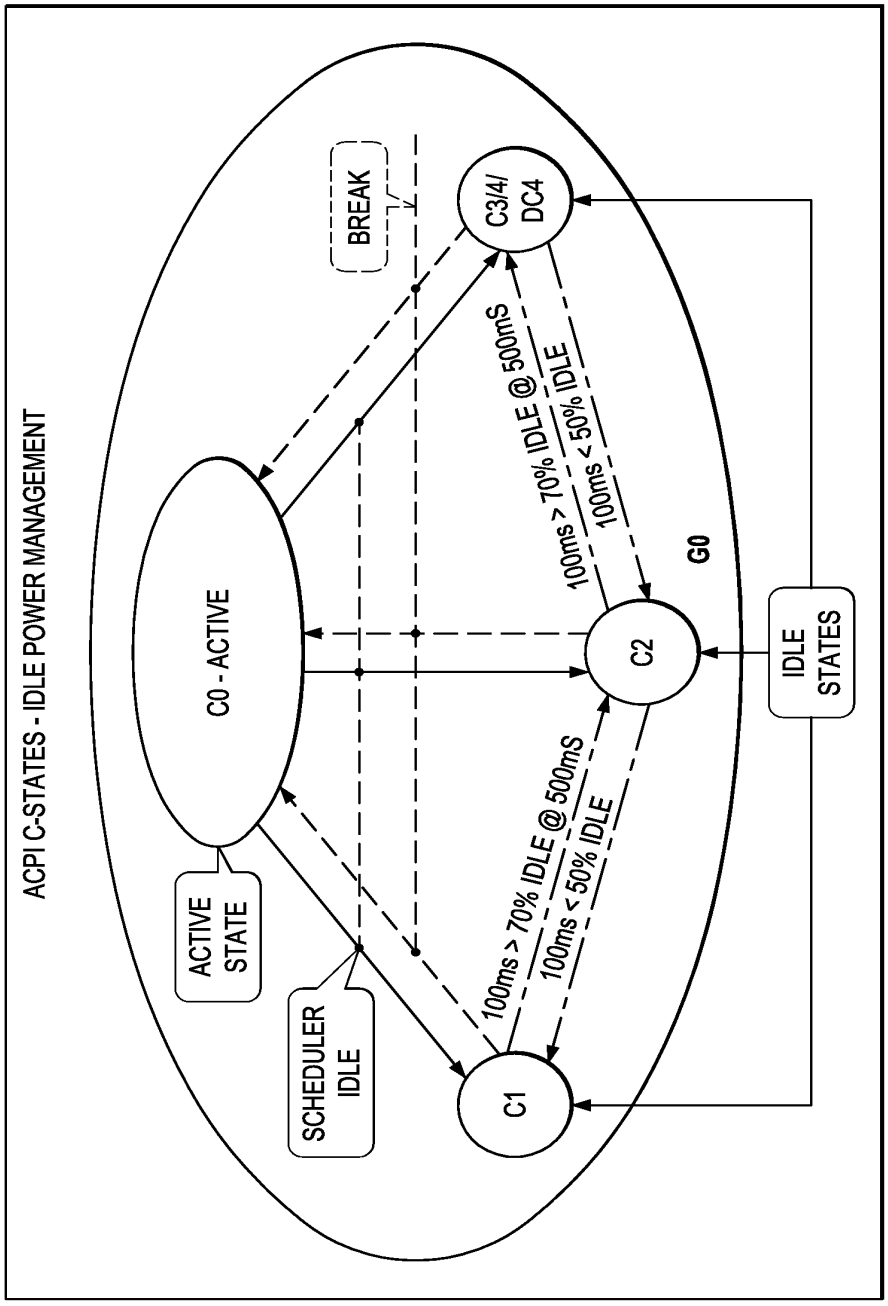

ACPI C-STATES - IDLE POWER MANAGEMENT
BREAK
C3/4/ DC4
C0 - ACTIVE
C2
C1
G0
IDLE STATES
ACTIVE STATE
SCHEDULER IDLE
100ms > 70% IDLE @ 500mS
100ms < 50% IDLE
100ms > 70% IDLE @ 500mS
100ms < 50% IDLE

FIG. 12

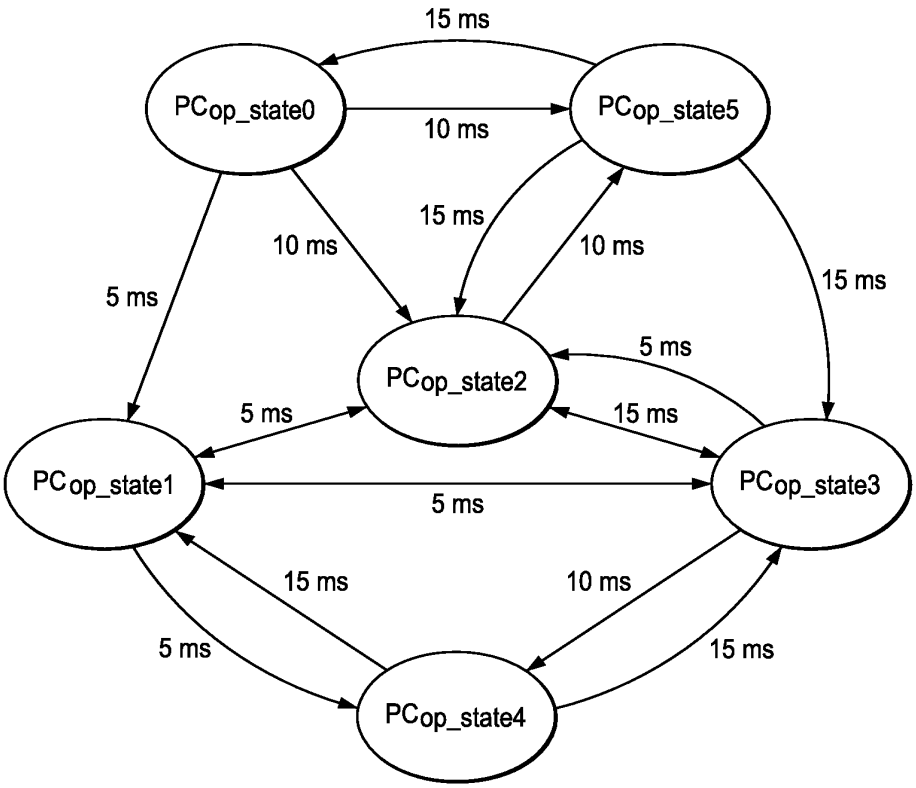

15 ms
PCop_state0
PCop_state5
10 ms
15 ms
10 ms
10 ms
15 ms
5 ms
5 ms
PCop_state2
5 ms
15 ms
PCop_state1
PCop_state3
5 ms
15 ms
10 ms
5 ms
15 ms
PCop_state4

FIG. 13

FIG. 14

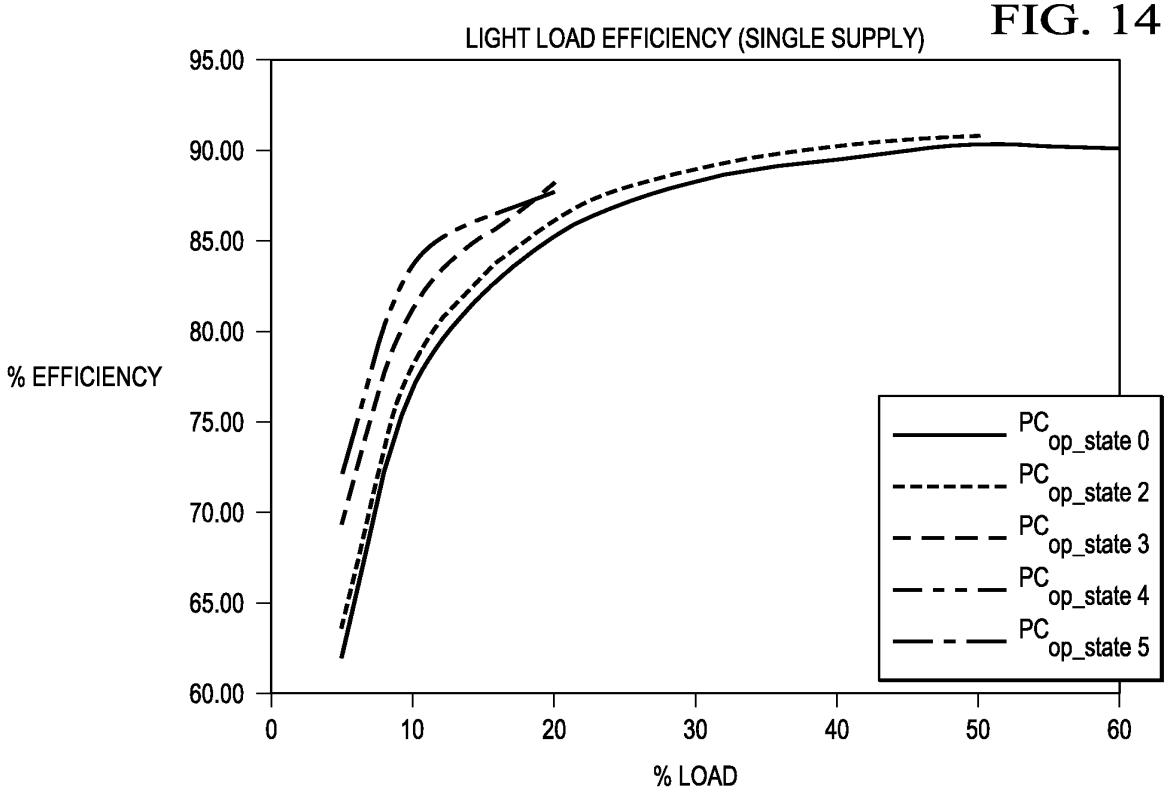

LIGHT LOAD EFFICIENCY (SINGLE SUPPLY)
% EFFICIENCY
95.00
90.00
85.00
80.00
75.00
70.00
65.00
60.00
0
10
20
30
40
50
60
% LOAD
PC op_state 0
PC op_state 2
PC op_state 3
PC op_state 4
PC op_state 5

FIG. 15

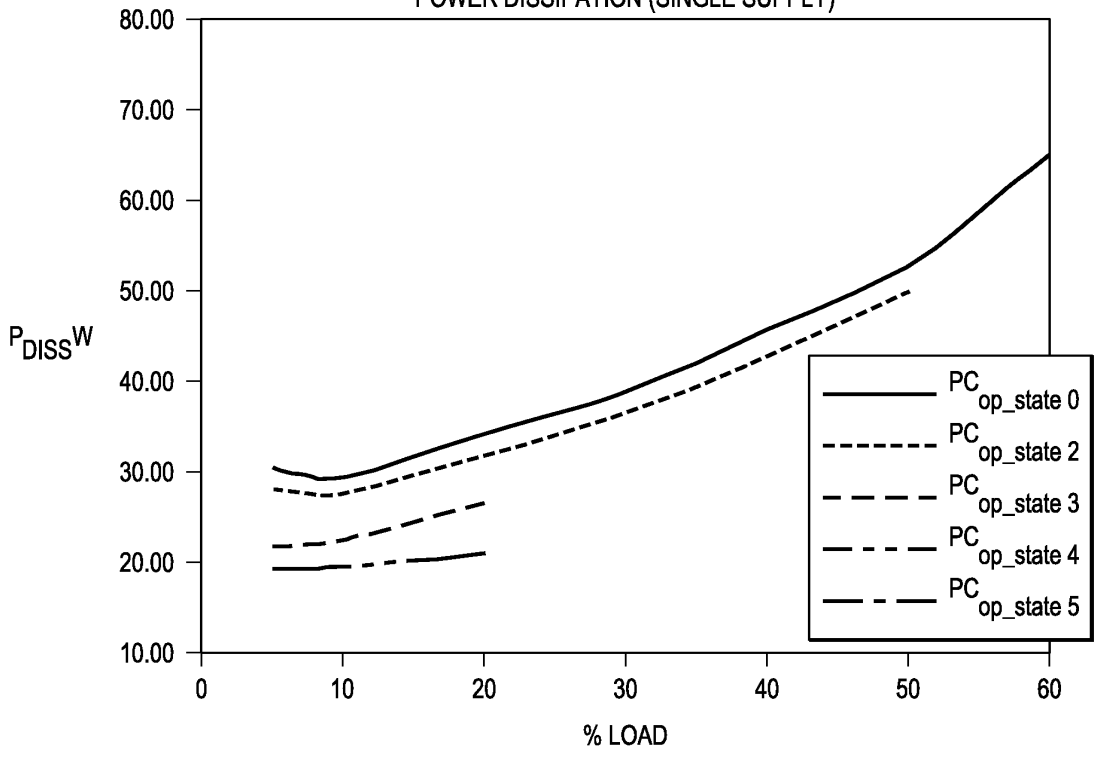

POWER DISSIPATION (SINGLE SUPPLY)
P DISS W
80.00
70.00
60.00
50.00
40.00
30.00
20.00
10.00
0
10
20
30
40
50
60
% LOAD
PC op_state 0
PC op_state 2
PC op_state 3
PC op_state 4
PC op_state 5

FIG. 16

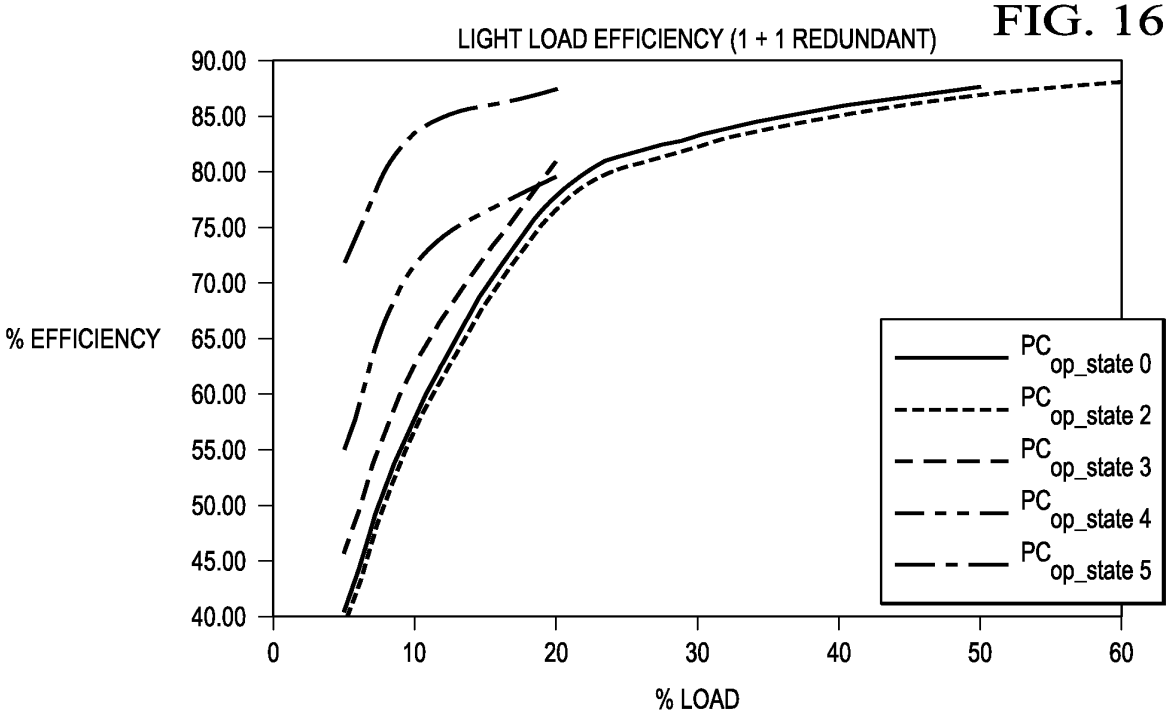
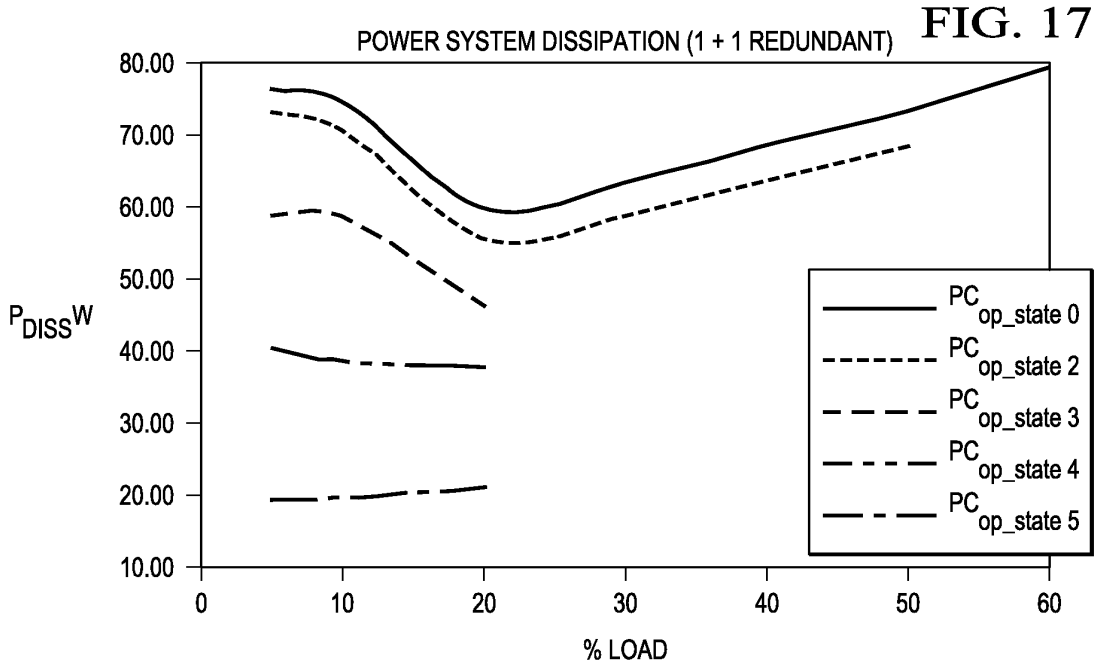

LIGHT LOAD EFFICIENCY (1 + 1 REDUNDANT)
% EFFICIENCY
90.00
85.00
80.00
75.00
70.00
65.00
60.00
55.00
50.00
45.00
40.00
0
10
20
30
40
50
60
% LOAD
PC op_state 0
PC op_state 2
PC op_state 3
PC op_state 4
PC op_state 5

FIG. 17


POWER SYSTEM DISSIPATION (1 + 1 REDUNDANT)
P DISS W
80.00
70.00
60.00
50.00
40.00
30.00
20.00
10.00
0
10
20
30
40
50
60
% LOAD
PC op_state 0
PC op_state 2
PC op_state 3
PC op_state 4
PC op_state 5