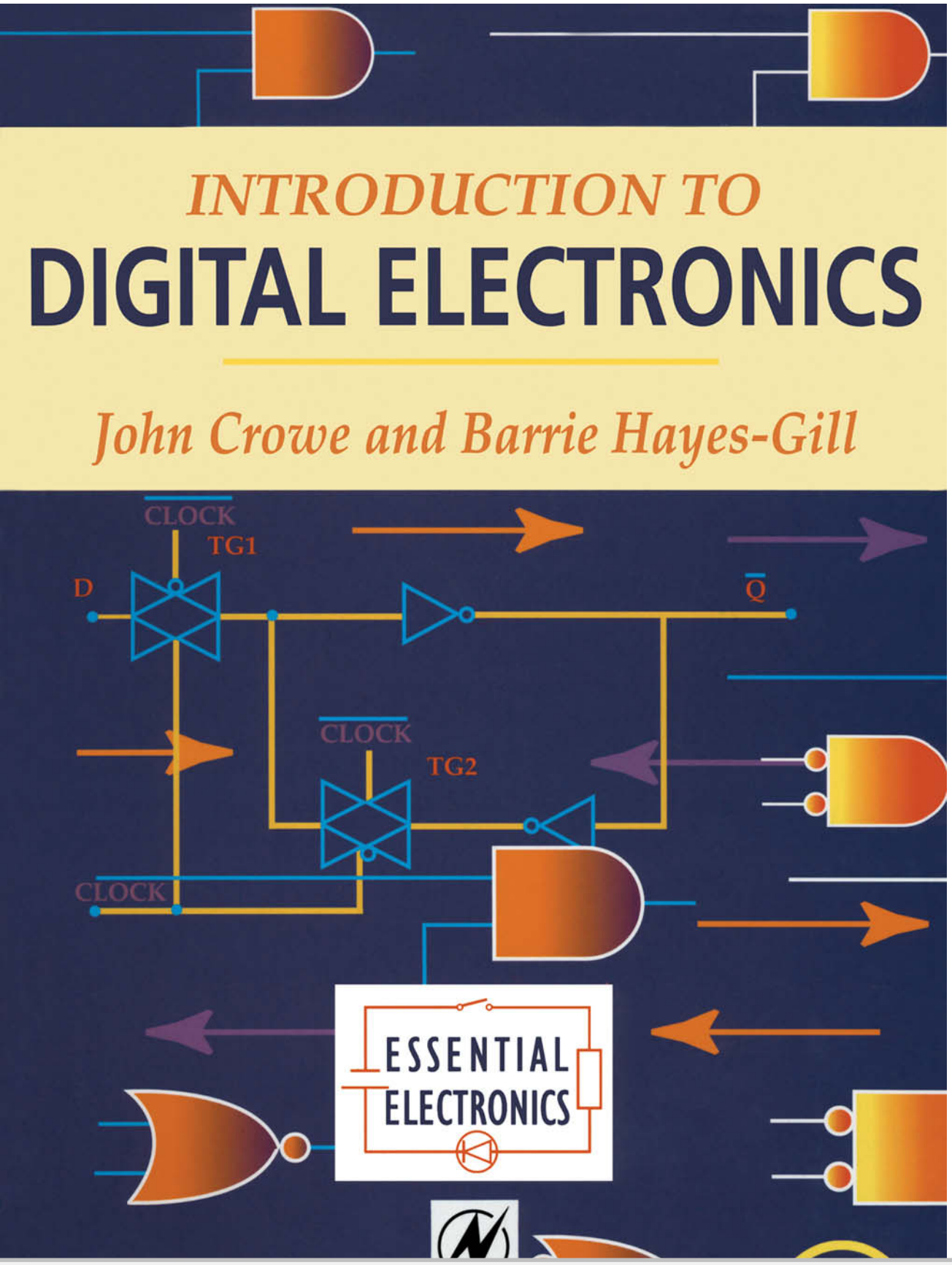

Introduction to Digital Electronics

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larger current to be passed within the same size transistor. In addition the higher the mobility, the faster the switching speed. In fact N-channel mobility is 2–3 times that of P-channel carriers and hence the NMOS logic operates at 2–3 times the speed of PMOS.

One problem of the NMOS gates (and for that matter PMOS) is that the upper transistor load is just acting as a resistor. When the lower transistor is on then current will flow from V_{dd} to V_{ss} and hence these types of devices consume a moderate amount of power. Consequently in 1978 both PMOS and NMOS devices were combined on to the same chip to produce the Complementary Metal Oxide Semiconductor family or CMOS as it is more commonly known.

9.3.3 CMOS inverter

A CMOS inverter is shown in Fig. 9.11. It consists of one NMOS and one PMOS transistor. The PMOS device is indicated by the negation sign (i.e. a bubble) on its gate and has a negative threshold voltage of typically –1 V. To turn on a PMOS device we require a voltage, V_{GS}, more negative than –1 V. Notice that the two drains of the two MOS transistors are connected together and form the output whilst the two gates form the single input. Due to the difference in the mobilities of the two devices the PMOS device is made with its W/L ratio 2–3 times larger than the NMOS device. This results in the two transistors having the same value of K so that both will have the same electrical performance.

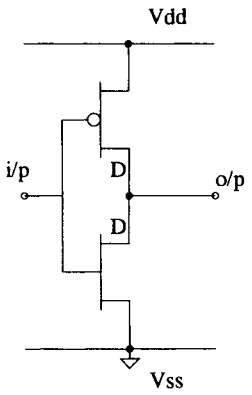

Fig. 9.11 CMOS inverter

The circuit operation depends upon the individual gate-source voltages. When the input voltage is 5 V then the NMOS V_{GS} is 5 V and hence this device is on. However, the PMOS V_{GS} is 0 V and so this device is turned off. The output voltage is thus pulled down to 0 V. Now with the input at 0 V the NMOS V_{GS} is 0 V and hence is turned off. However, the PMOS V_{GS} is –5 V and is thus turned on (remember a voltage more negative than the threshold voltage is needed to turn on a PMOS device). With the PMOS device on, the output voltage is pulled up to

CMOS inverter power dissipation

You should notice that when the input is steady at either a high or a low voltage (static condition) then one transistor is always off between V_{dd} and V_{ss}. Hence the current flowing is extremely small – equal to the leakage current of the off transistor which is typically 100 nA. As a result of this the static power dissipation is extremely low and it is this reason that has made CMOS such a popular choice of technology.

For input voltages between V_T and $V_{dd} - V_T$ then the individual MOS transistors will be switched on by an amount dictated by Equations 9.1 and 9.2 and thus current will flow from V_{dd} to V_{ss}. When the input voltage is $V_{dd}/2$ both transistors will be turned on by the same amount and hence the current will rise to a maximum and power will be dissipated. On many integrated circuits, several thousand gates exist and hence this power dissipation can be large. It is for this reason that the input voltage to a CMOS circuit must not be held at $V_{dd}/2$. When the inputs are switching the power dissipated is called dynamic power dissipation. However, as long as the input signals have a fast rise and fall time then this form of dynamic power dissipation is small. The main cause of dynamic power dissipation, however, in a CMOS circuit is due to the charge and discharge of capacitance at each gate output. The dynamic power dissipation of a CMOS gate is therefore dependent upon the number of times a capacitor is charged and discharged. Hence as the frequency of switching increases so the dynamic power dissipation increases. The dynamic power dissipation for a CMOS gate is equal to

$$P_{dynamic} = C_L \times V_{dd}^2 \times f \tag{9.3}$$

where f is the switching frequency and C_L is the load capacitance.

The total power dissipated in a CMOS inverter is thus the sum of the static and dynamic components.

Example 9.9

Compare the power dissipated by a CMOS inverter driving a 50 pF load at (a) 10 kHz and (b) 10 MHz. What average current flows in each case. Assume a 5 V power supply.

Solution

(a) 10 kHz:

$$P_{dynamic} = C_L \times V_{dd}^2 \times f = 50 \times 10^{-12} \times 25 \times 10 \times 10^3 = 12.5\,\mu W$$

Also:

$$P_{dynamic} = V_{dd} \times I_{average} \Rightarrow I_{average} = 12.5 \times 10^{-6}/5 = 2.5\,\mu A$$

(b) 10 MHz:

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