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Hulkko et al.

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[45] **Date of Patent: Mar. 31, 1998**

[54] **DEMODULATION OF AN INTERMEDIATE FREQUENCY SIGNAL BY A SIGMA-DELTA CONVERTER**

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[21] Appl. No.: **624,113**

[22] Filed: **Mar. 29, 1996**

Related U.S. Application Data

[63] Continuation of Ser. No. 303,613, Sep. 9, 1994, abandoned.

[30] **Foreign Application Priority Data**

Sep. 10, 1993 [FI] Finland 933989

[51] **Int. Cl.**[6] **H04B 14/06**; H04L 27/22

[52] **U.S. Cl.** **375/316**; 375/247; 375/328; 375/329

[58] **Field of Search** 375/240, 244, 375/247, 316, 328–329, 332; 341/143

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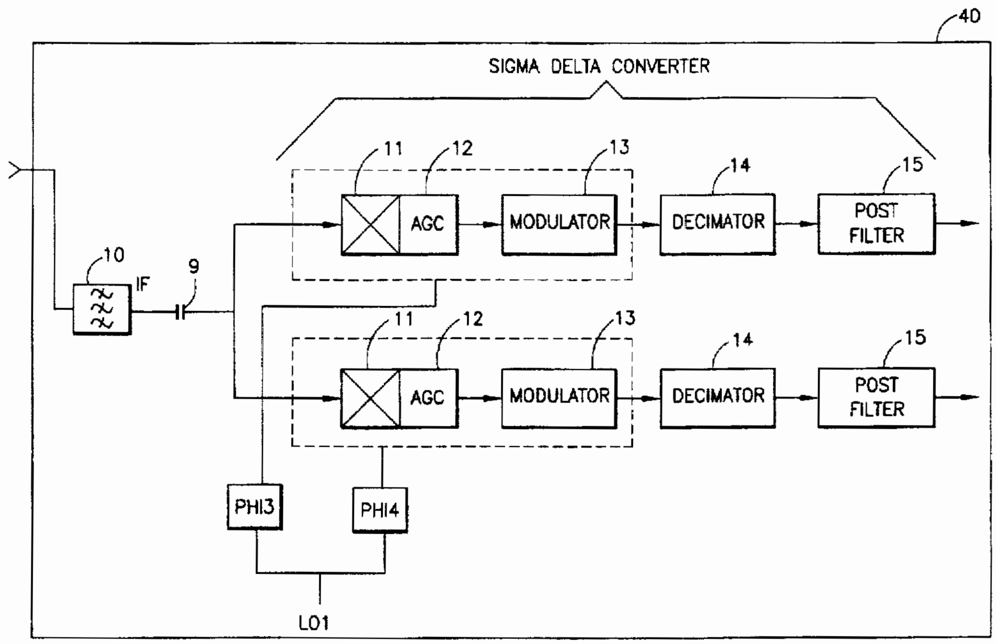
Attorney, Agent, or Firm—Perman & Green, LLP

[57] **ABSTRACT**

A sigma-delta signal converter is implemented using switched capacitor switching elements in which a first switch (**31**) serves as a mixer (**11**). The output of the mixer is directed to the second input of an adder (**16**), and its second input is the feedback signal (f1) of the sigma-delta signal converter, which is also directed into a base-frequency output signal through a decimator (**14**) and low-pass filtering (**15**).

16 Claims, 3 Drawing Sheets



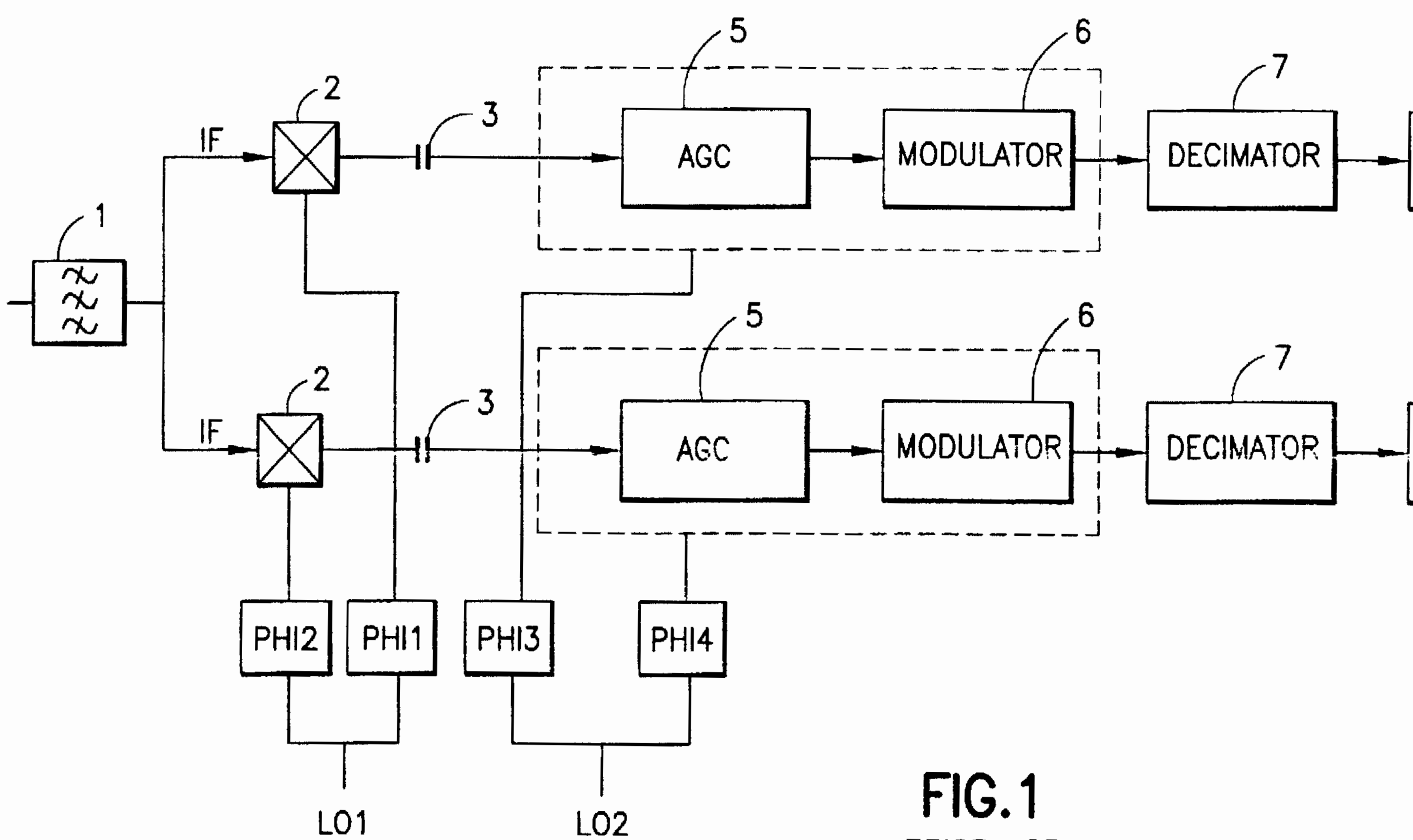


FIG. 1
PRIOR ART

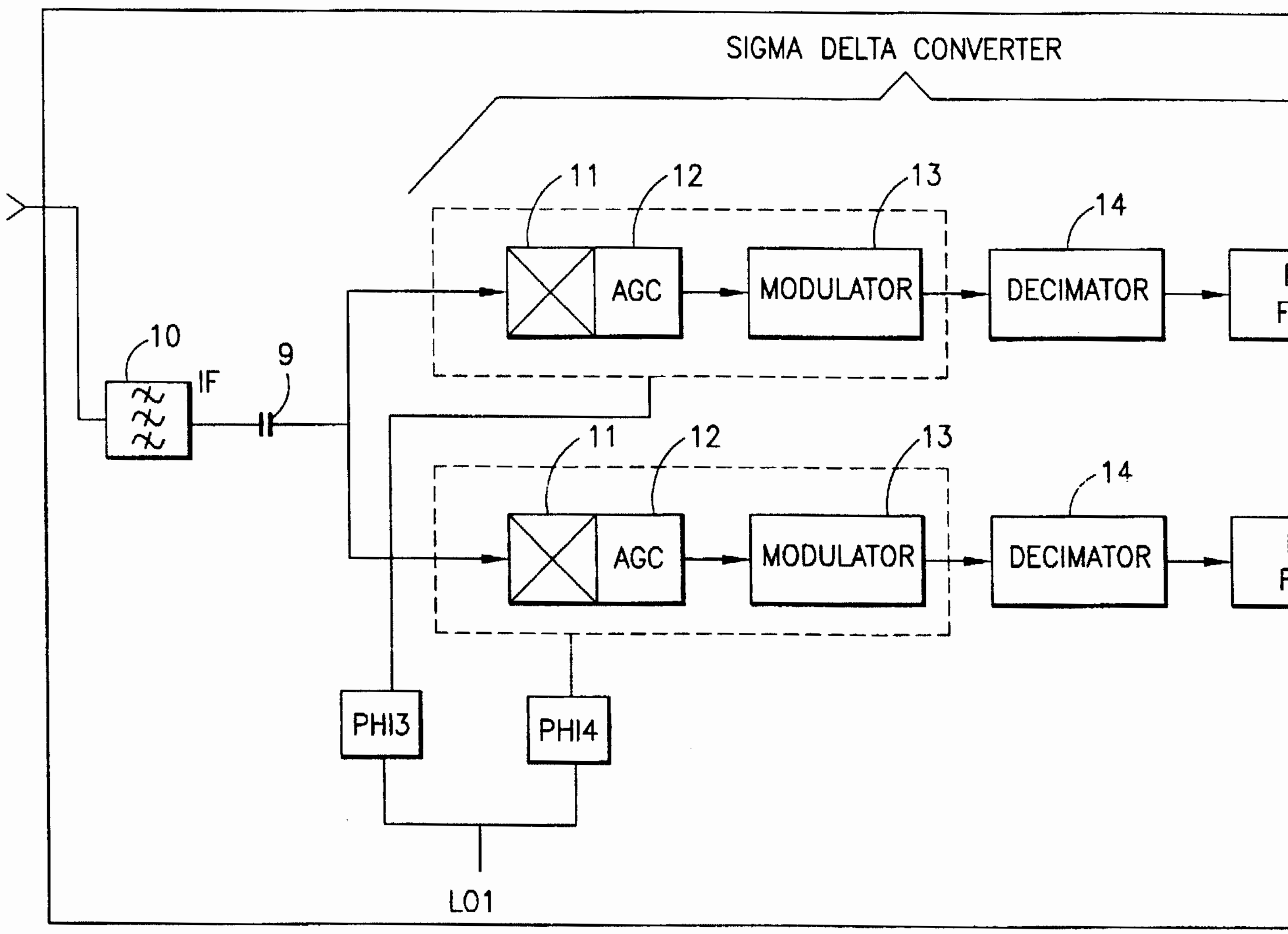

SIGMA DELTA CONVERTER
11
12
13
14
AGC
MODULATOR
DECIMATOR
10
IF
9
PHI3
PHI4
LO1

FIG.2

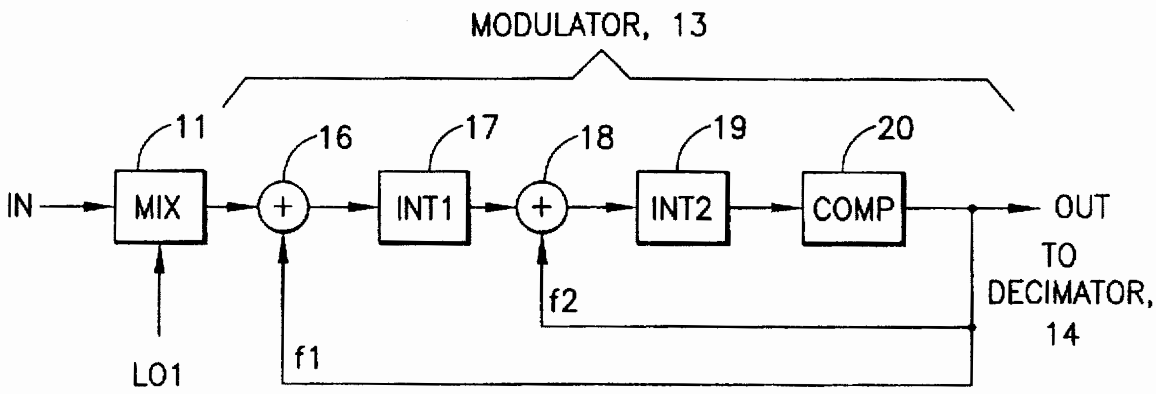

MODULATOR, 13
11
16
17
18
19
20
IN
MIX
+
INT1
+
INT2
COMP
OUT
TO
DECIMATOR,
14
f2
f1
LO1

FIG.3

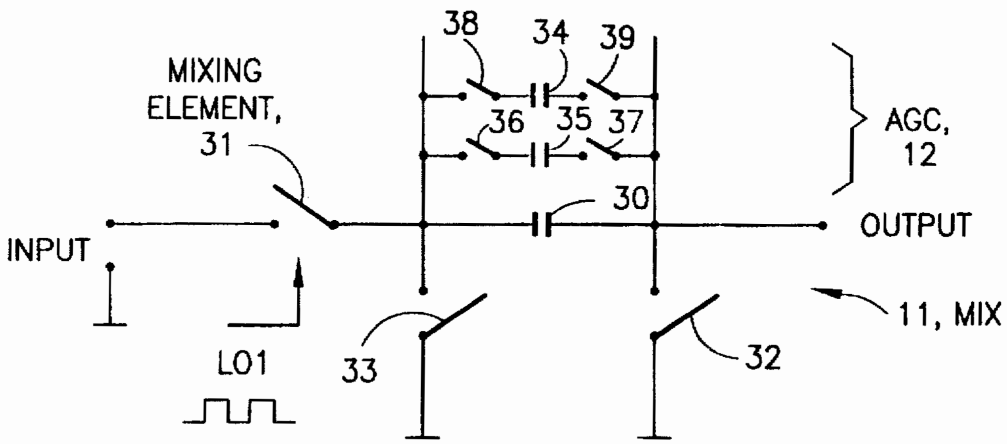

38
34
39
MIXING
ELEMENT,
31
36
35
37
AGC,
12
30
INPUT
OUTPUT
11, MIX
LO1
33
32

FIG.4

DEMODULATION OF AN INTERMEDIATE FREQUENCY SIGNAL BY A SIGMA-DELTA CONVERTER

This is a continuation of application Ser. No. 08/303,613 filed on Sep. 9, 1994, now abandoned.

BACKGROUND OF THE INVENTION

The invention relates to a receive arrangement for receiving a modulated carrier signal.

EP 0 461 720-A1 describes a known receive arrangement for receiving a modulated carrier signal, comprising a mixer/demodulator driven with a sinusoidal oscillator of carrier frequency fc, at least one adder, a low-pass filter, a pulse shaper constituting a one-bit sigma-delta signal converter, all included in a closed signal loop, the pulse shaper being driven with sampling frequency fs, and further comprising a digital decimation filter. In this type of receive arrangement the modulated carrier signal is demodulated in the closed signal loop by the mixer/demodulator, the output signal of which is converted after passing through the low-pass filter into a digital signal by the sigma-delta converter.

A typical prior art sigma-delta converter arrangement is described in greater detail with reference to FIG. **1** of the drawings.

An incoming intermediate frequency IF carrier signal is provided to each branch of the receive arrangement. In each branch the incoming signal is filtered through bandpass filter **1** and mixed to a baseband signal in a linear mixer **2** using a sinusoidal local oscillator signal LO1 at the IF frequency. A high time constant capacitor **3** is provided on each of the incoming signal branches to remove direct currents from the baseband signal. The gain of the circuit is controlled through Automatic Gain Controllers (AGC) **5** and the baseband signals are converted to digital signals in modulators **6**. After modulation the signals pass through respective decimators **7** and post filters **8** to remove spurious signals created by the decimators. The specific details of the local oscillator frequency and phase shifts of the particular arrangement illustrated in FIG. **1** are as follows:

PHI1=+45°

PHI2=−45°

PHI3=PHI4=0°

LO1=IF

LO2=oversampling frequency

The demodulation, i.e., the mixing of the intermediate frequency (bandpass-filtered) int-signal down to the base frequency is traditionally based on the use of a multiplier. Thus the modulated IF-signal is multiplied by the sinusoidal oscillator signal (LO1). In the synchronous demodulation the frequency and the phase of the oscillator are locked to the carrier wave with the aid of a phase-locked loop (PLL), for instance. The frequency spectrum of the mixed product consists of the desired base-frequency component and the component spectrums which are removed by low-pass filtering prior to entering the sigma-delta converter. Such a mixing process may be described by the following trigonometric equation:

$$\cos(a) * \cos(b) = ½ * \cos(a-b) + ½ * \cos(a+b) \quad (1)$$

Equation (1) holds only if both products are pure cosine signals.

If cos(a) now represents the modulated int-carrier wave then:

where ω0 is the angle frequency of the carrier wave and PHI is a momentary phase modulation (QAM, MSK, QPSK, GMSK . . . .).

Ideally the term cos(b) represents a clean, mixing oscillator frequency (LO):

$$b = n * \omega 1 * t \; (n=1, 2, 3, \ldots) \quad (3)$$

where n*ω1 is the angular frequency of the oscillator of the mixer.

In the ideal case the frequency and the phase of the oscillator are locked to the frequency and the phase of the carrier wave of the input signal (in). in these conditions ω0=n*ω1, and the term ½*cos(a−b) is reduced to ½*cos (PHI). This base-frequency phase difference signal conveys the data symbols. Term ½*cos(a+b) represents the component of the frequency spectrum on frequency 2*ω0.

When prior art receive arrangements such as those described above are implemented by discrete components they require a very large area on the printed circuit board. In addition, as the signal entering the sigma-delta converter is a baseband signal the ac-coupled branches need very low high-pass corner frequencies with high time constants in order to accomplish dc blocking. This means that it is not efficient for the arrangement to be powered down as often as would be ideal, as powering up again is slow and as a result the circuit cannot be powered down for short periods, the circuit therefore, consumes a large amount of power.

SUMMARY OF THE INVENTION

In accordance with the present invention there is provided a receiver for receiving a modulated carrier signal comprising, a sigma-delta signal converter having at least one adder included in a feedback loop, characterised in that the arrangement comprises a time discrete sampling means for down converting the modulated carrier signal prior to the feedback loop.

By down convening the carrier frequency signal using a time discrete sampling means a number of advantages are provided. Firstly, an expensive sinusoidal oscillator is no longer required with space and cost benefits. Secondly, although use of time discrete sampling means, rather than a pure sinusoidal local oscillator for down converting the IF signal means that mixing occurs at the frequency of sampling and also at harmonics of the sampling frequency this perceived disadvantage can be used to the system's advantage enabling samples to be taken using a local oscillator sampling at a subharmonic frequency of the carrier signal. Thus can also give important power savings.

One way in which the invention can be implemented is by using the input stage of a sigma-delta signal Converter having switched capacitor switching elements to implement the time discrete sampling means that acts as a mixer. The sigma-delta converter with the desired switched capacitor switching elements provided at the input stage may be implemented as an ASIC. The output of this mixer can then be directed to the first input of an adder included in the closed feedback signal loop of the sigma-delta converter. This adder comprises, as the second input, the feedback signal of the sigma-delta signal converter, which is also directed through a decimator and low-pass filter to provide an output signal which is provided to the second input of the adder.

In circuits of embodiments of the invention the incoming modulated signal may be mixed into a base-band frequency signal or a frequency approaching the base-band frequency

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