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**Manohararajah et al.**

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(54) **METHODS FOR CALIBRATING MEMORY INTERFACE CIRCUITRY**

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(73) Assignee: **Altera Corporation**, San Jose, CA (US)

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(\* ) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 224 days.

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(21) Appl. No.: **13/149,562**

*Primary Examiner* — Fernando Hidalgo

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(74) *Attorney, Agent, or Firm* — Treyz Law Group; Jason Tsai

(51) **Int. Cl.**  
**G11C 7/00** (2006.01)

(52) **U.S. Cl.**  
USPC .... **365/193**; 365/129; 365/149; 365/189.011;  
365/189.14; 365/189.05; 365/230.06; 365/233.1;  
365/233.13; 365/233.16; 365/233.17

(57) **ABSTRACT**

(58) **Field of Classification Search**  
USPC ..... 365/129, 149, 189.011, 189.14, 189.05,  
365/193, 230.06, 233.1, 233.13, 233.16,  
365/233.17  
See application file for complete search history.

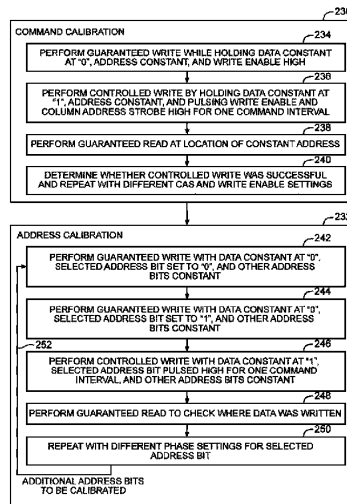
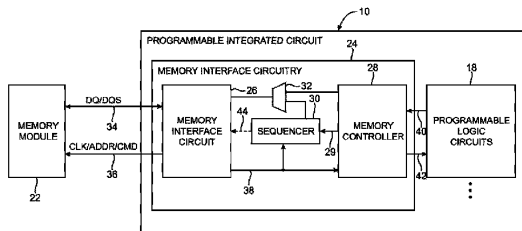
Integrated circuits may communicate with off-chip memory. Such types of integrated circuits may include memory interface circuitry that is used to interface with the off-chip memory. The memory interface circuitry may be calibrated using a procedure that includes read calibration, write leveling, read latency tuning, and write calibration. Read calibration may serve to ensure proper gating of data strobe signals and to center the data strobe signals with respect to read data signals. Write leveling ensures that the data strobe signals are aligned to system clock signals. Read latency tuning serves to adjust read latency to ensure optimum read performance. Write calibration may serve to center the data strobe signals with respect to write data signals. These calibration operations may be used to calibrate memory systems supporting a variety of memory communications protocols.

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**20 Claims, 16 Drawing Sheets**



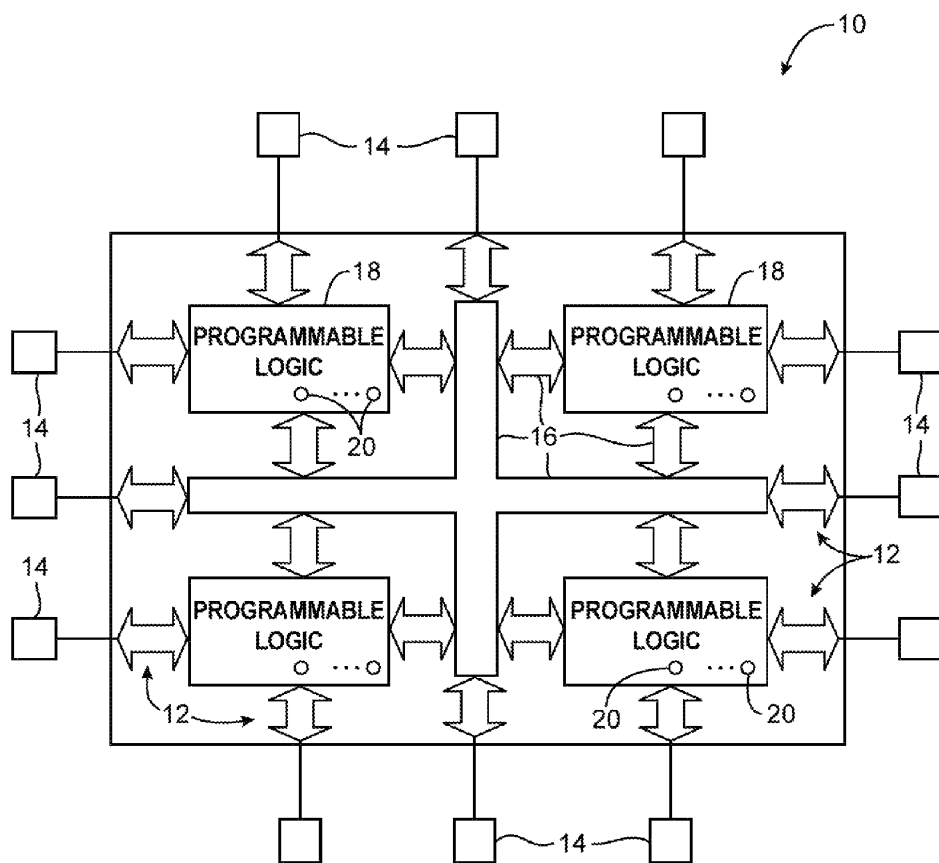


FIG. 1

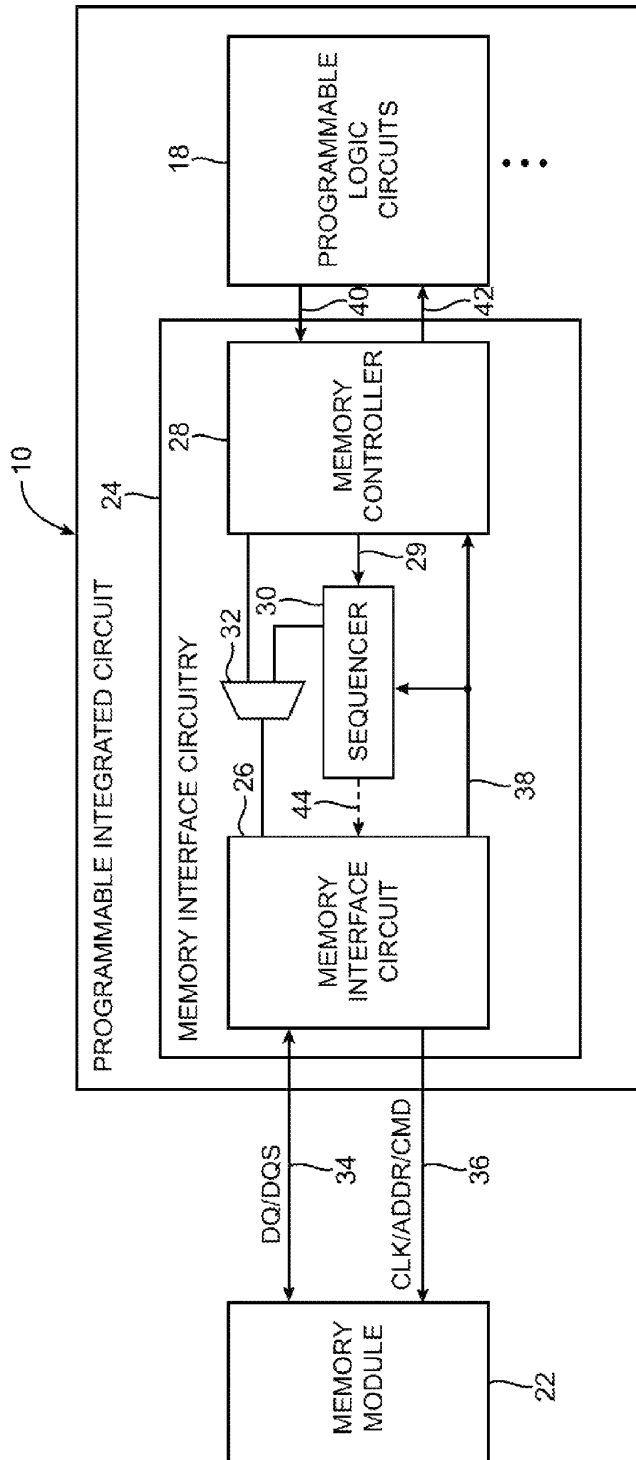


FIG. 2

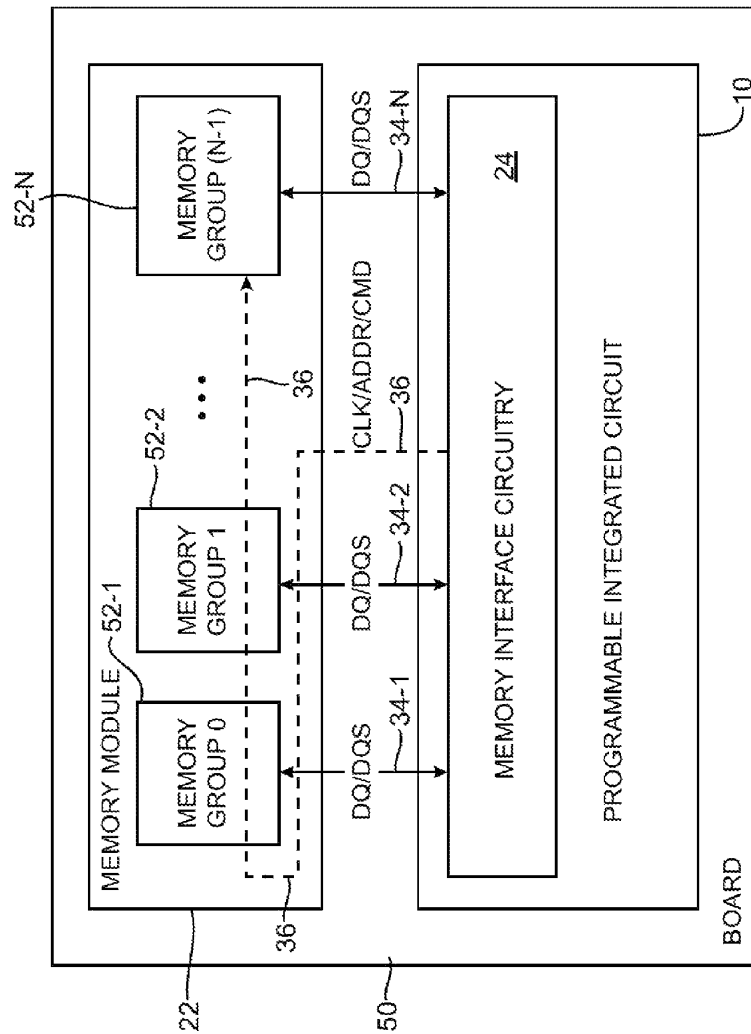


FIG. 3

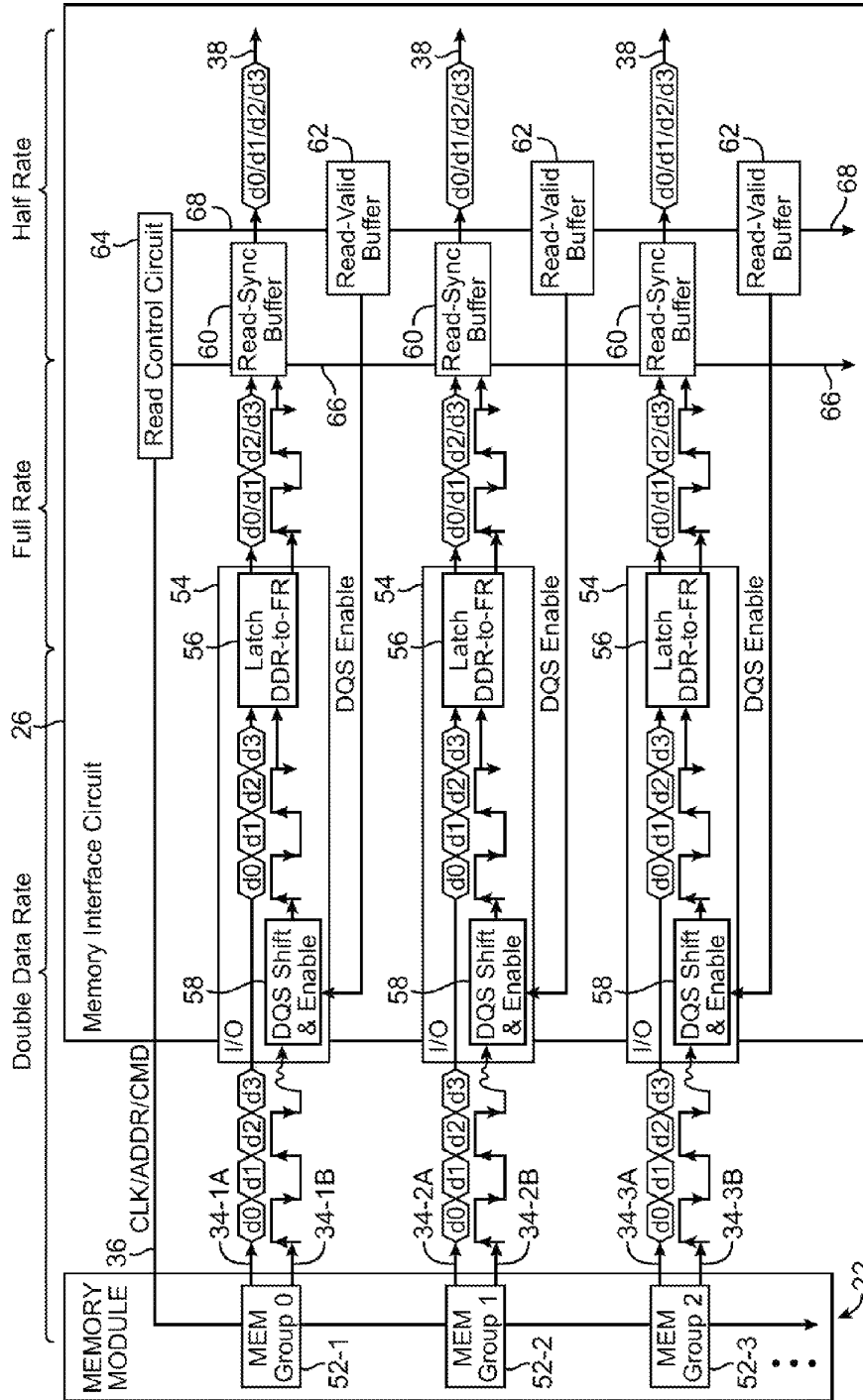


FIG. 4

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