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(12) **United States Patent**
Tokuhiro

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(54) **DELAY TIME CONTROL OF MEMORY CONTROLLER**

(56) **References Cited**

(75) Inventor: **Noriyuki Tokuhiro**, Kawasaki (JP)

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(73) Assignee: **Fujitsu Limited**, Kawasaki (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 334 days.

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(21) Appl. No.: **12/209,740**

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Primary Examiner — Raymond Phan

(65) **Prior Publication Data**

(74) *Attorney, Agent, or Firm* — Staas & Halsey LLP

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(30) **Foreign Application Priority Data**

(57) **ABSTRACT**

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A memory control circuit has a write leveling function and controls read/write operations by supplying a clock signal to a plurality of memories through a clock signal line which is wired to the plurality of memories through daisy chain connection. For each of the plurality of memories, a first variable delay unit delays, in a write operation, a data strobe signal output to the memory by a first delay time that is set by utilizing the write leveling function and a second variable delay unit delays, in a read operation, a data signal input from the memory by a second delay time that is set based on the first delay time.

(51) **Int. Cl.**

G06F 13/42 (2006.01)

(52) **U.S. Cl.** **713/401**; 713/601

(58) **Field of Classification Search** 713/400-401, 713/500-501, 600-601

See application file for complete search history.

16 Claims, 20 Drawing Sheets

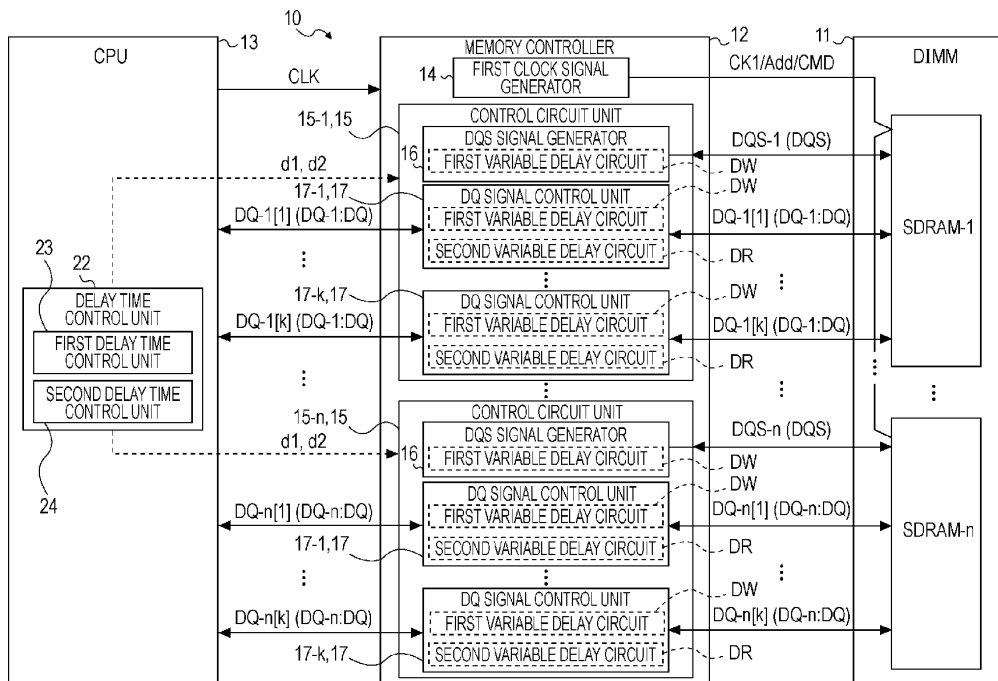


FIG. 1
RELATED ART

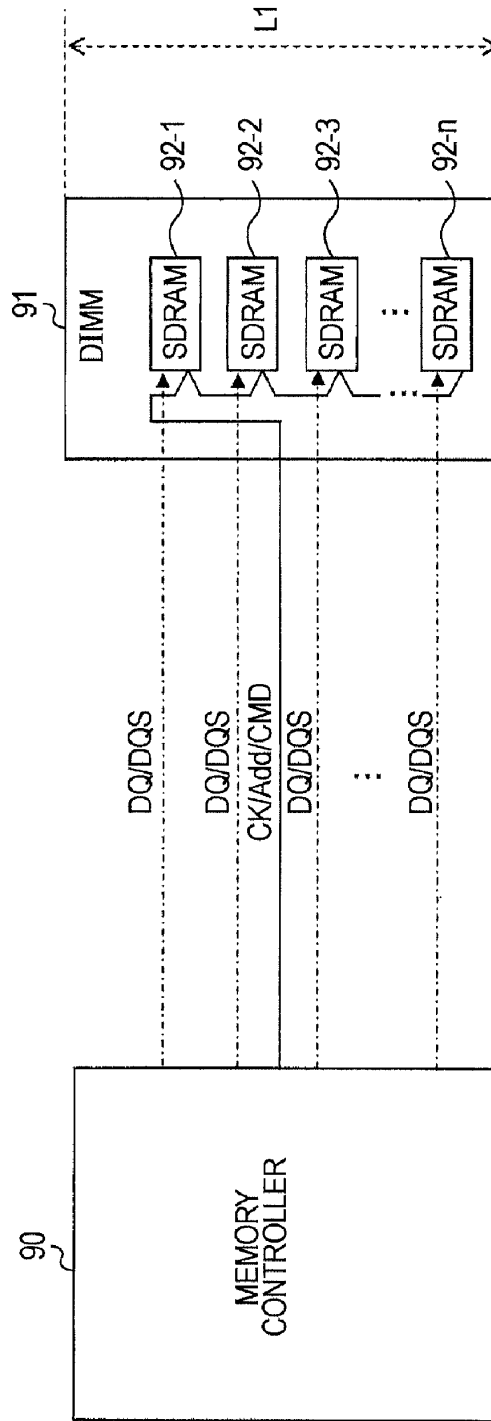


FIG. 2
RELATED ART

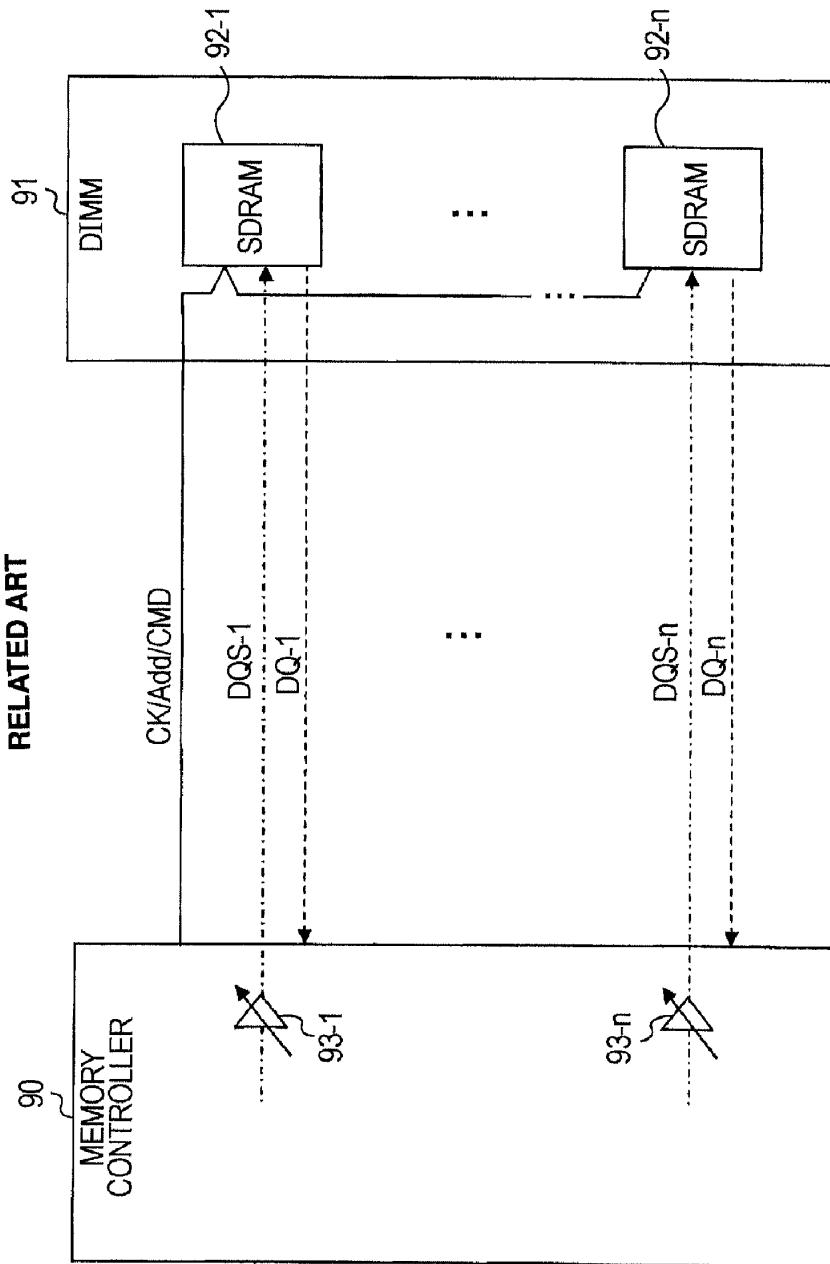
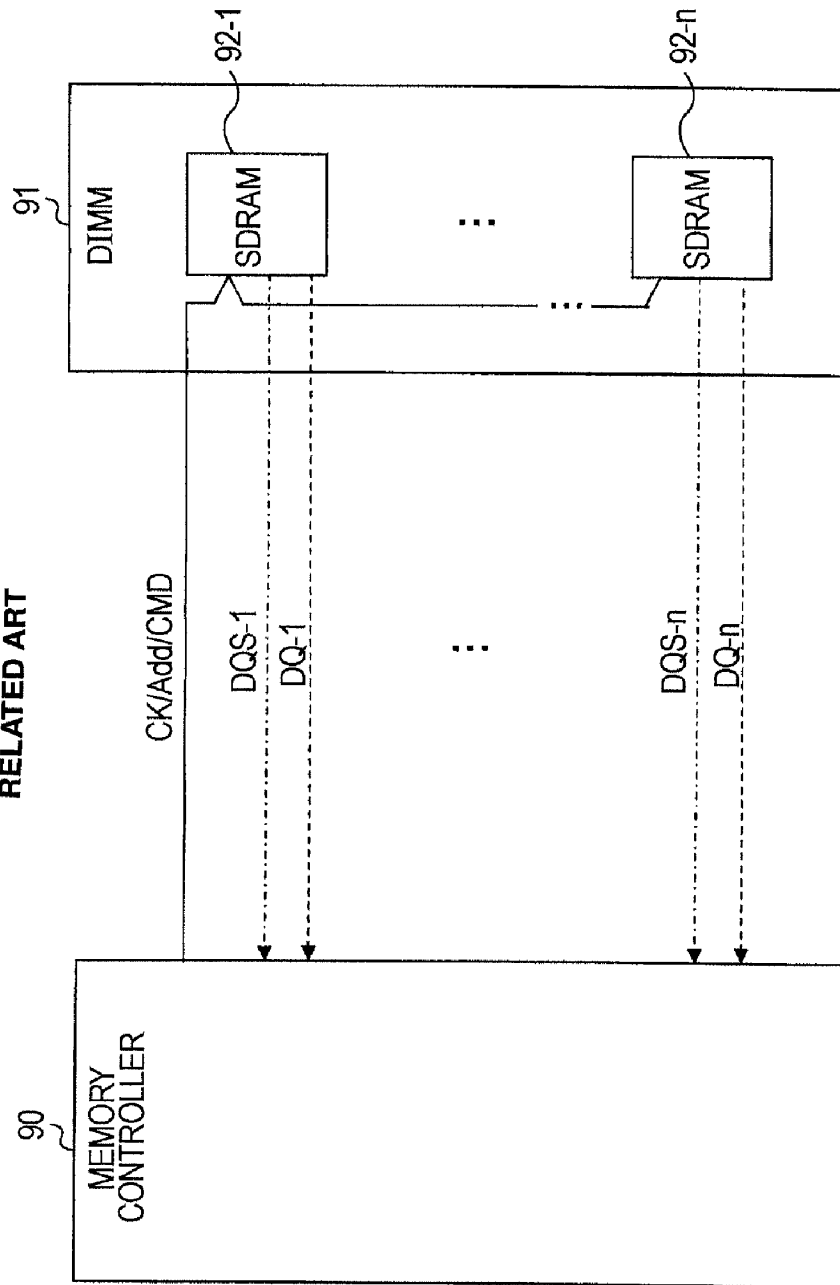
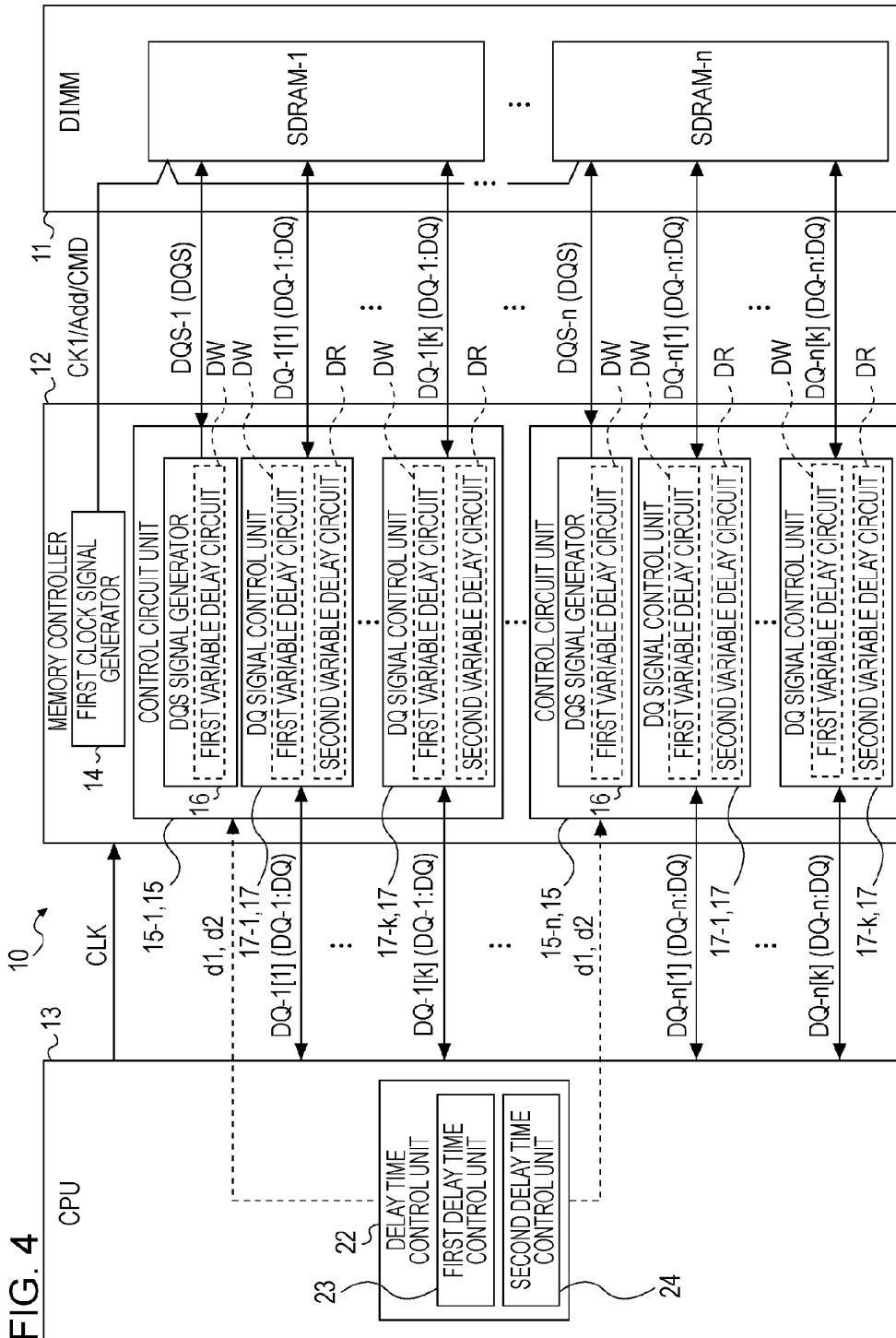


FIG. 3
RELATED ART





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