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Lee et al.

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(54) **MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

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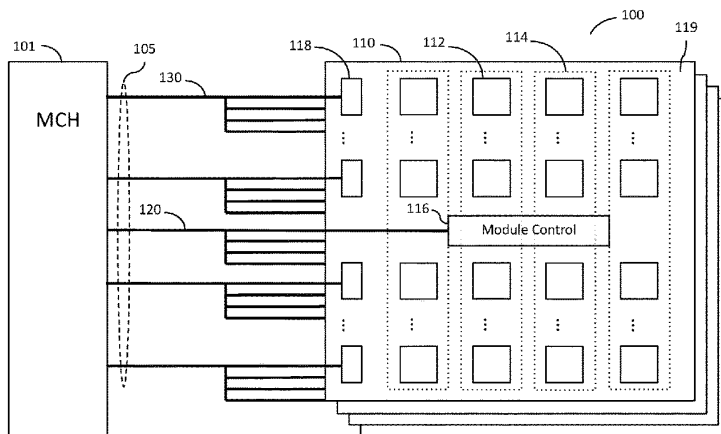US 2017/0147514 A1 May 25, 2017

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G06F 3/00 (2006.01)
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G06F 3/06 (2006.01)
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CPC *G06F 13/1673* (2013.01); *G06F 3/0613* (2013.01); *G06F 3/0656* (2013.01); *G06F*
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(58) **Field of Classification Search**
None
See application file for complete search history.

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(57) **ABSTRACT**

A memory module is operable in a memory system with a memory controller. The memory module comprises a module control device mounted on the module board to receive command signals from the memory controller and to output module command signals and module control signals, and memory devices mounted on the module board to perform a first memory operation in response to the module command signals. The memory module further comprises a plurality of buffer circuits distributed across a surface of the module board. Each respective buffer circuit is associated with a respective set of the memory devices and includes logic that is configured to obtain timing information based on signals received by the each respective buffer circuit during a second memory operation prior to the first memory operation and to control timing of the data and strobe signals through the each respective buffer circuit in accordance with the timing information.

22 Claims, 26 Drawing Sheets

Related U.S. Application Data

continuation of application No. 13/952,599, filed on Jul. 27, 2013, now Pat. No. 9,128,632.

(60) Provisional application No. 61/676,883, filed on Jul. 27, 2012.

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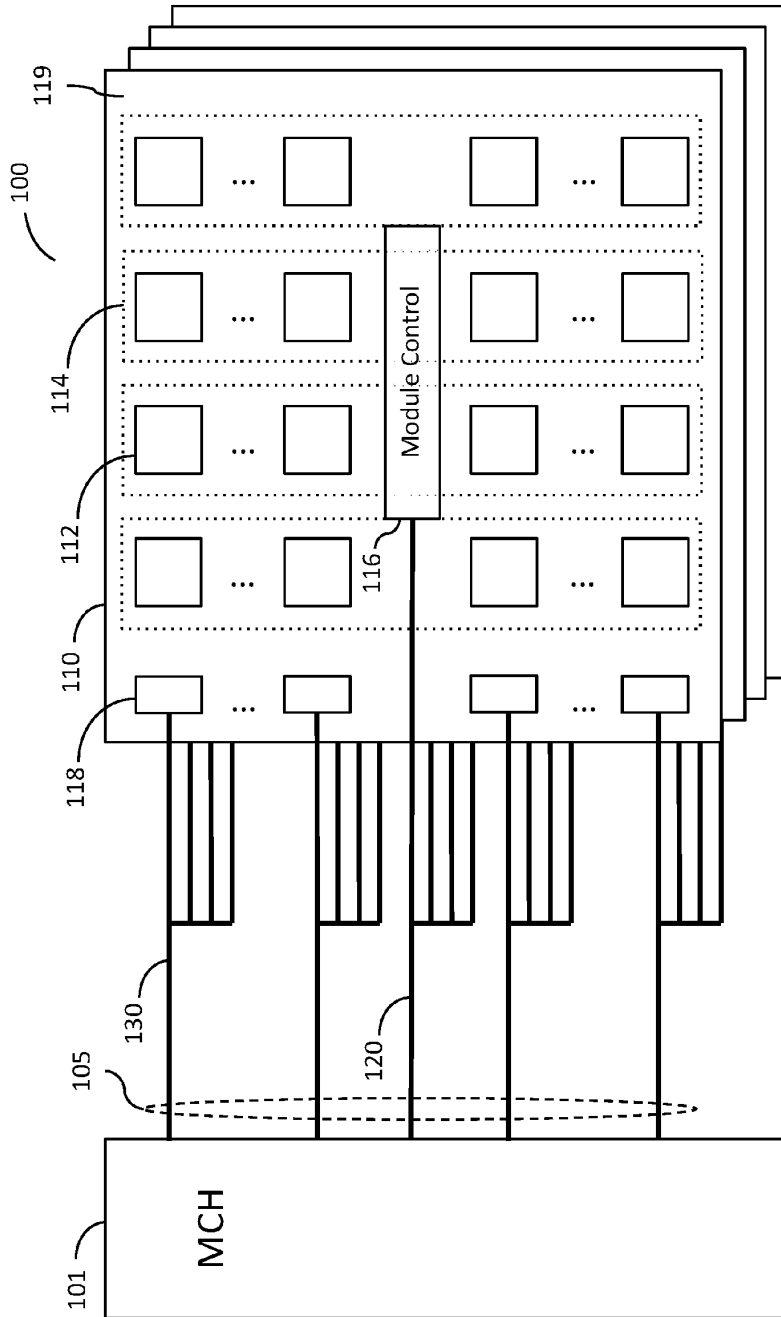|				
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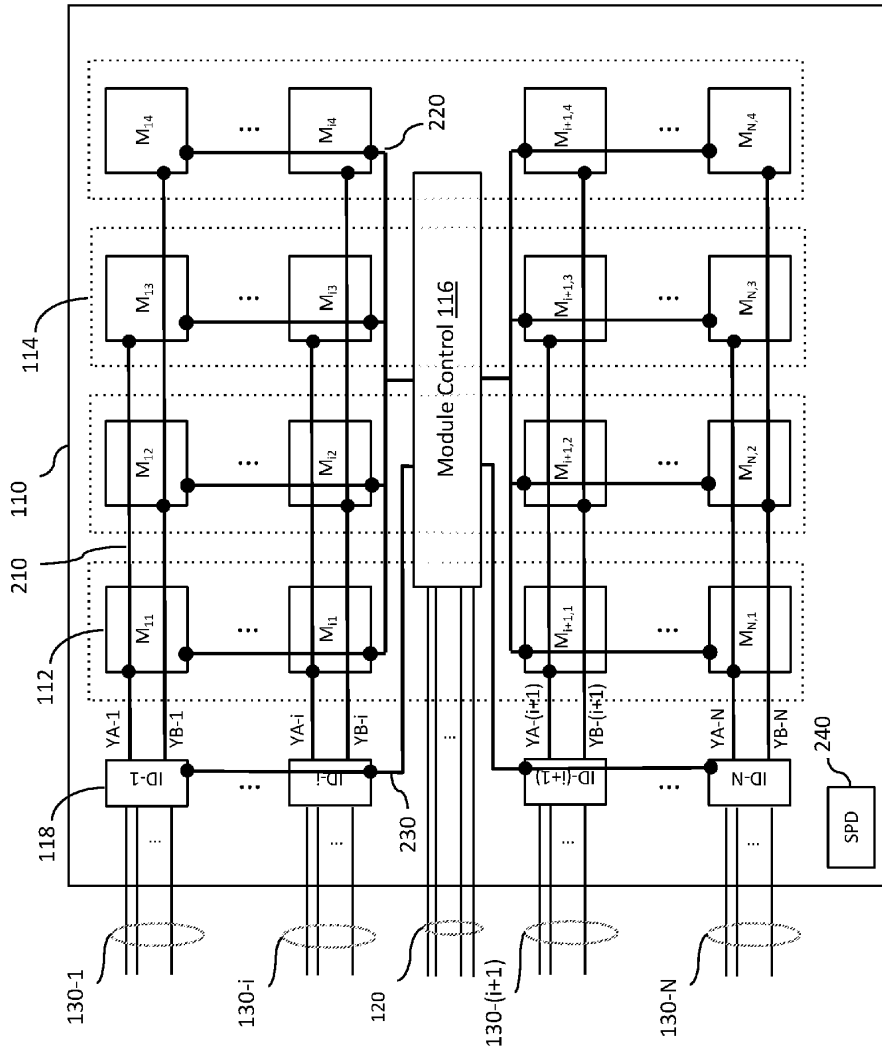* cited by examiner

FIG. 1

FIG. 2A

FIG. 2B

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