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(54) **MAINTAINING LINE VOLTAGE DURING RESET**

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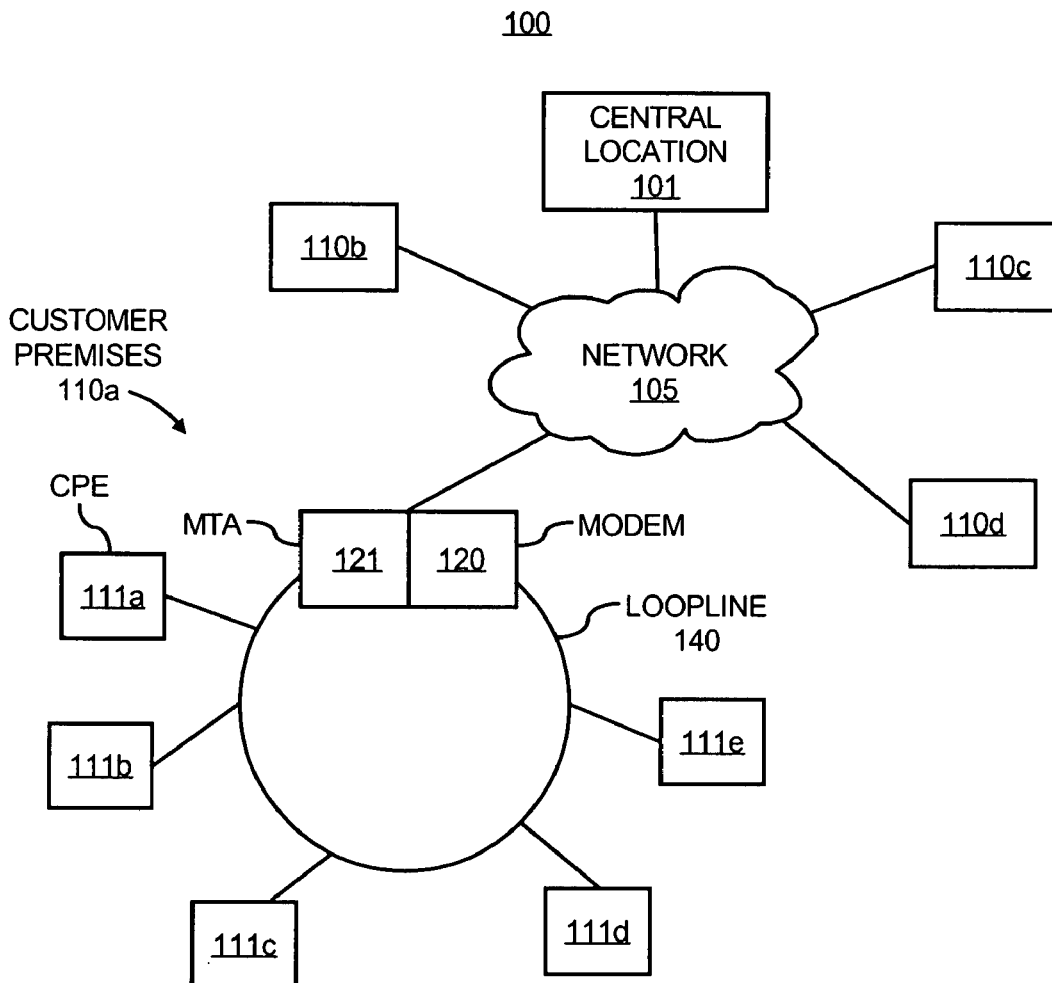
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(52) **U.S. Cl.** **379/399.01**

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(57) **ABSTRACT**

A first clock signal is generated by a first circuit and a second clock signal is generated by an auxiliary clock circuit. A switch controls whether the first clock signal or the second clock signal is provided to a subscriber line integrated circuit (SLIC). The SLIC is operable to generate a line voltage within predetermined tolerances on a loop line at a customer premises if the SLIC is receiving the first clock signal or the second clock signal.

(21) Appl. No.: **11/411,696**
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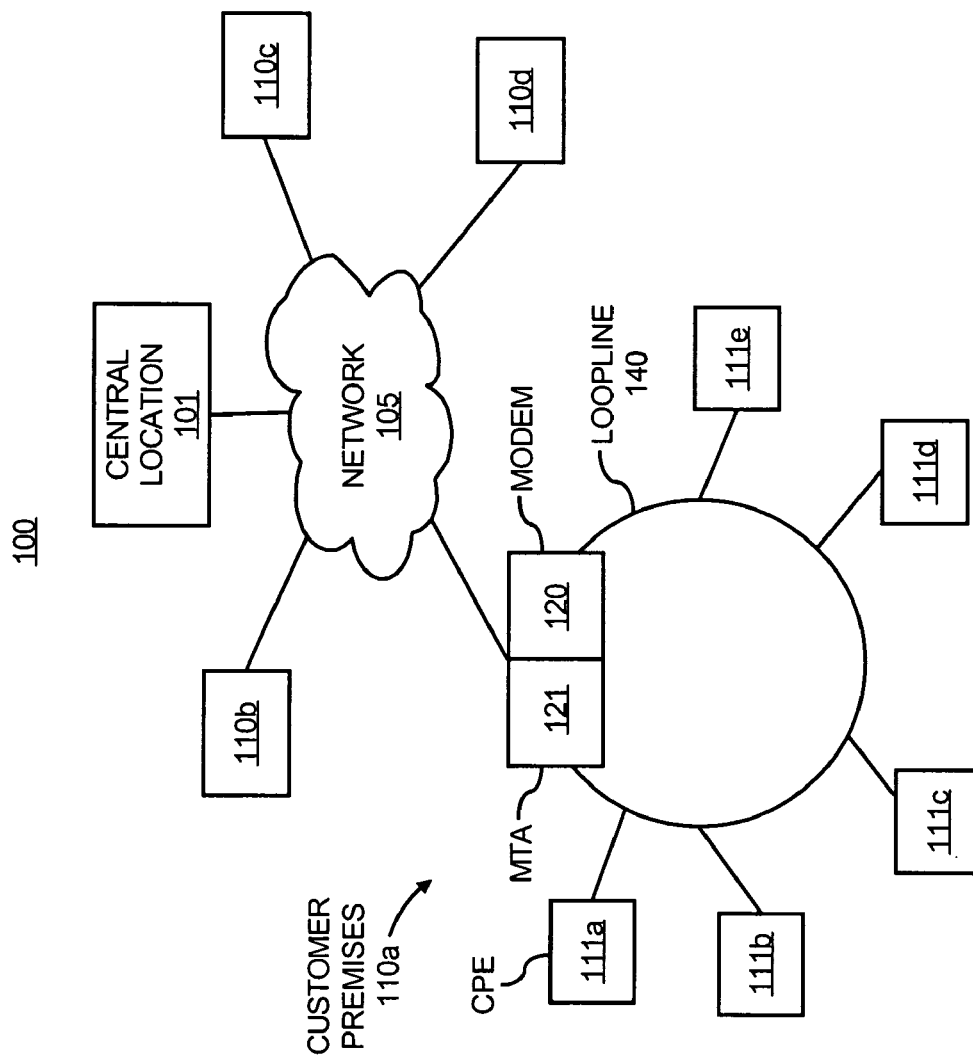


FIG. 1

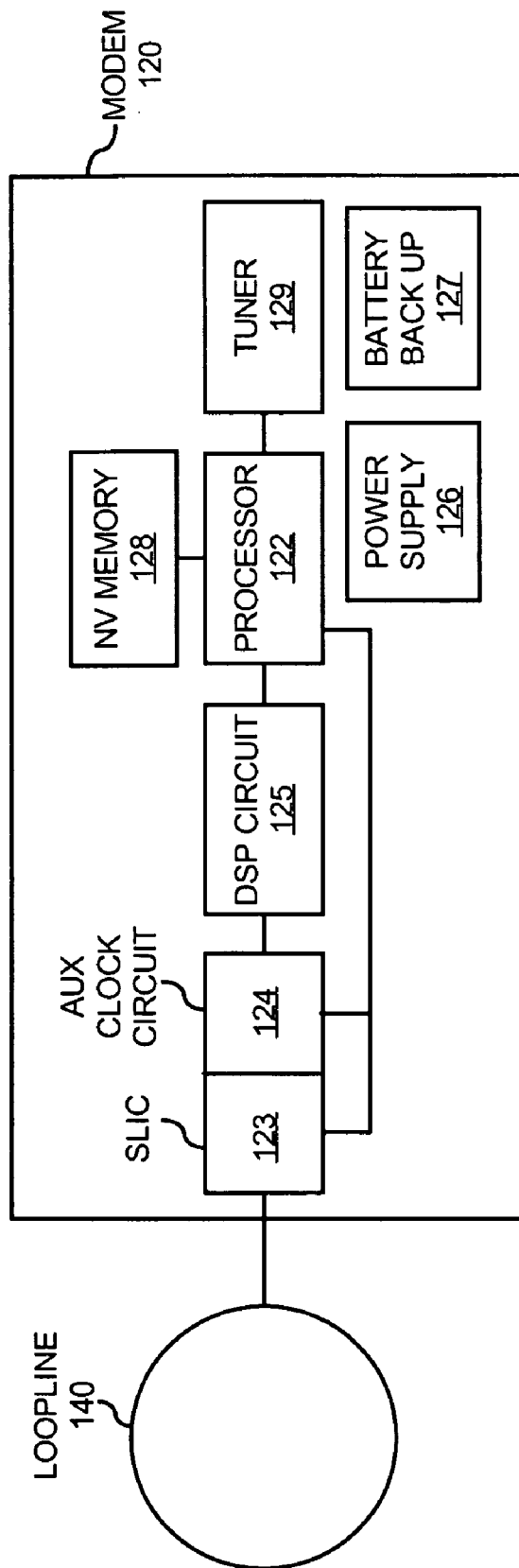


FIG. 2A

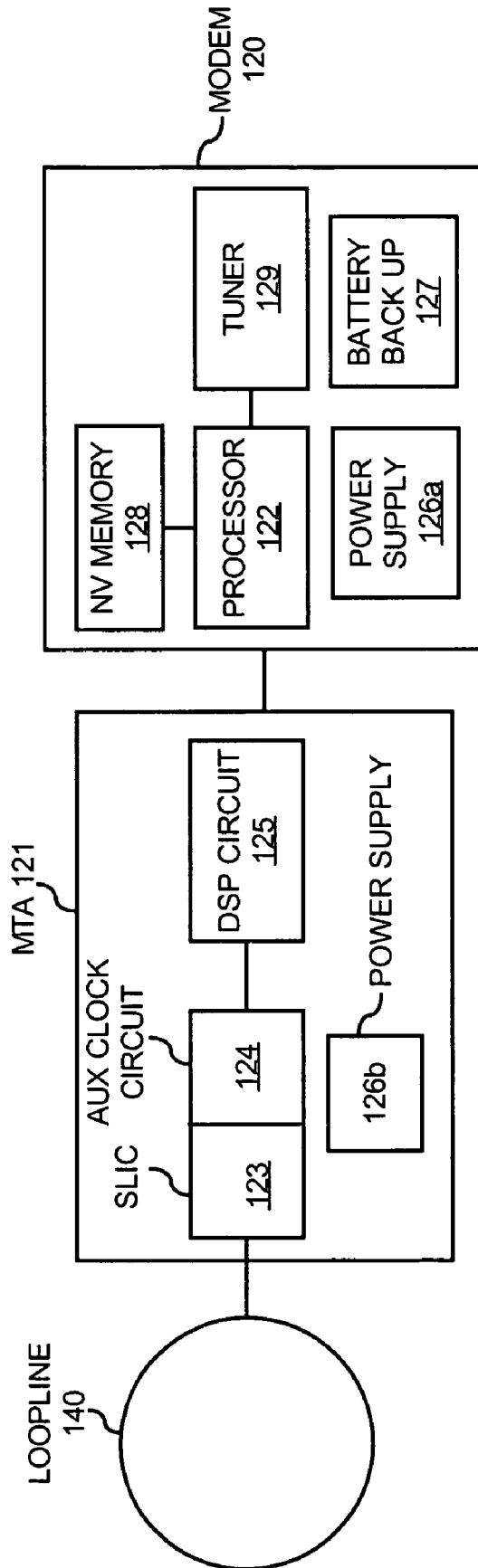


FIG. 2B

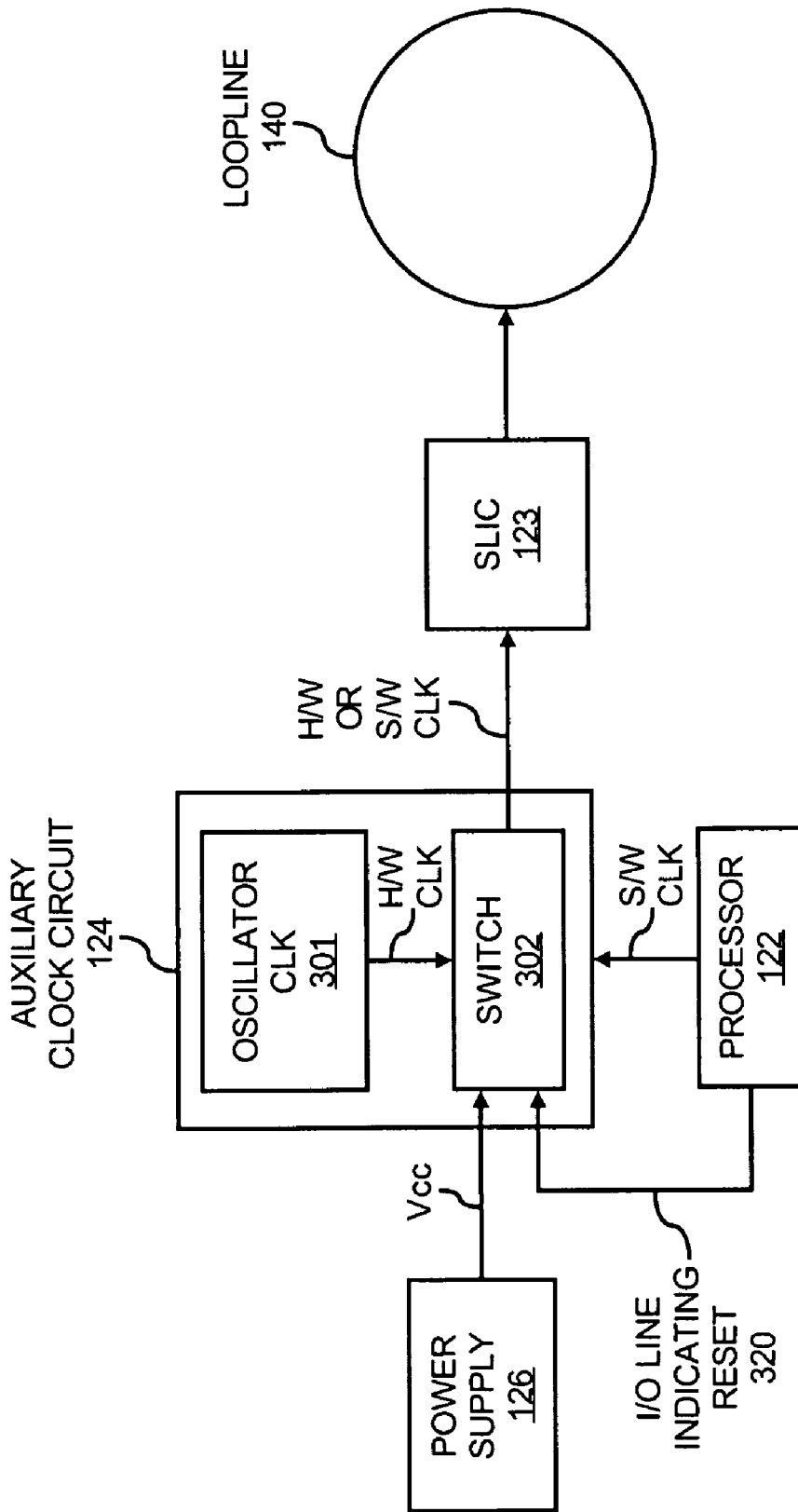


FIG. 3

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