



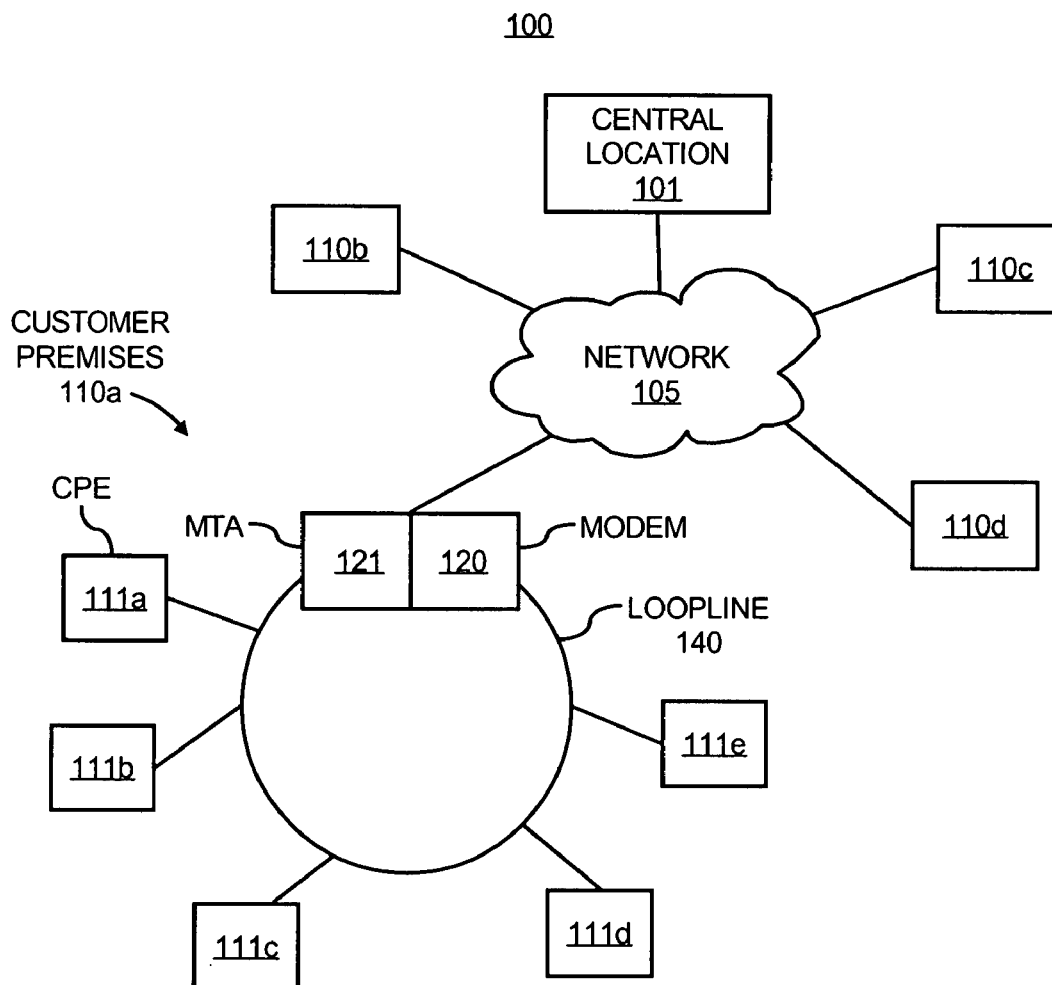
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(43) **Pub. Date: Sep. 6, 2007**(54) **MAINTAINING LINE VOLTAGE DURING
RESET****Related U.S. Application Data**(60) Provisional application No. 60/779,517, filed on Mar.
6, 2006.(76) Inventors: **Dipak R. Patel**, Hatboro, PA (US);
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Brook, PA (US)**Publication Classification**(51) **Int. Cl.**
H04M 1/00 (2006.01)
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HORSHAM, PA 19044 (US)**(57) **ABSTRACT**

A first clock signal is generated by a first circuit and a second clock signal is generated by an auxiliary clock circuit. A switch controls whether the first clock signal or the second clock signal is provided to a subscriber line integrated circuit (SLIC). The SLIC is operable to generate a line voltage within predetermined tolerances on a loop line at a customer premises if the SLIC is receiving the first clock signal or the second clock signal.

(21) Appl. No.: **11/411,696**(22) Filed: **Apr. 26, 2006**

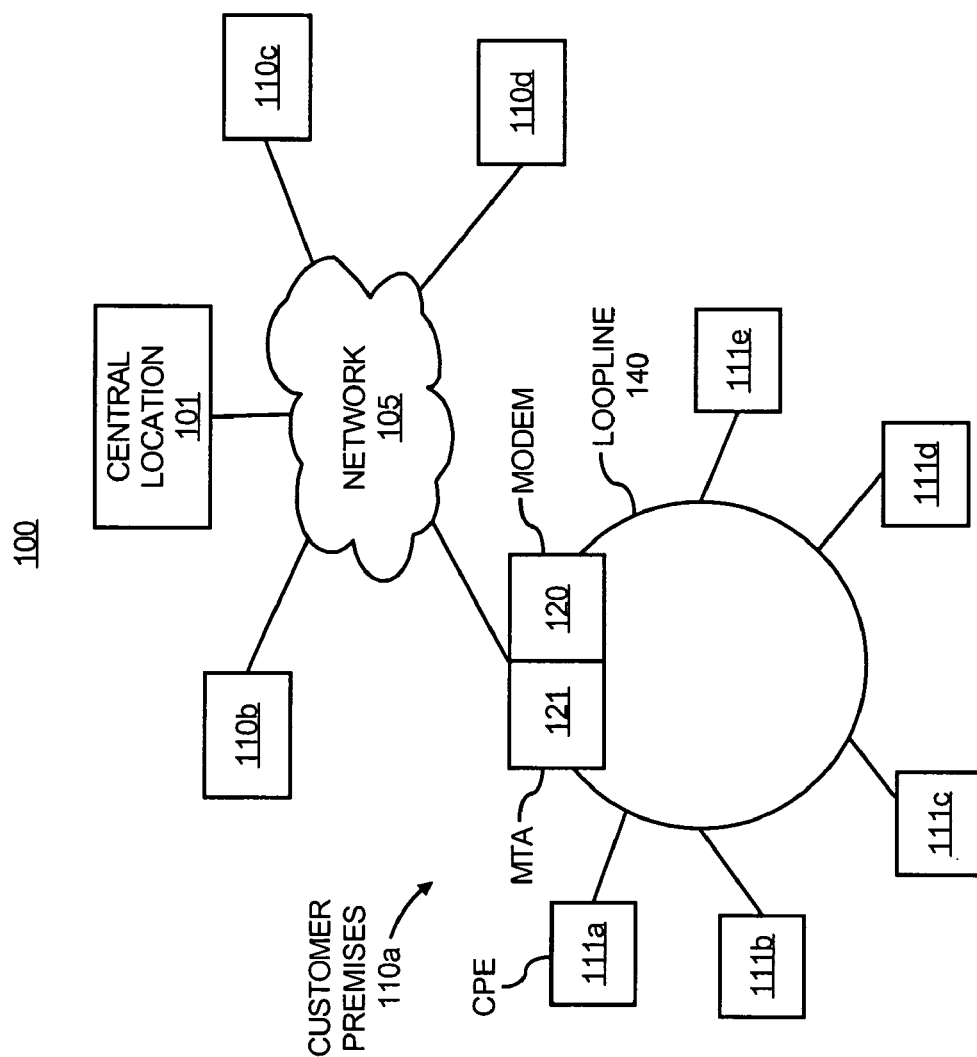


FIG. 1

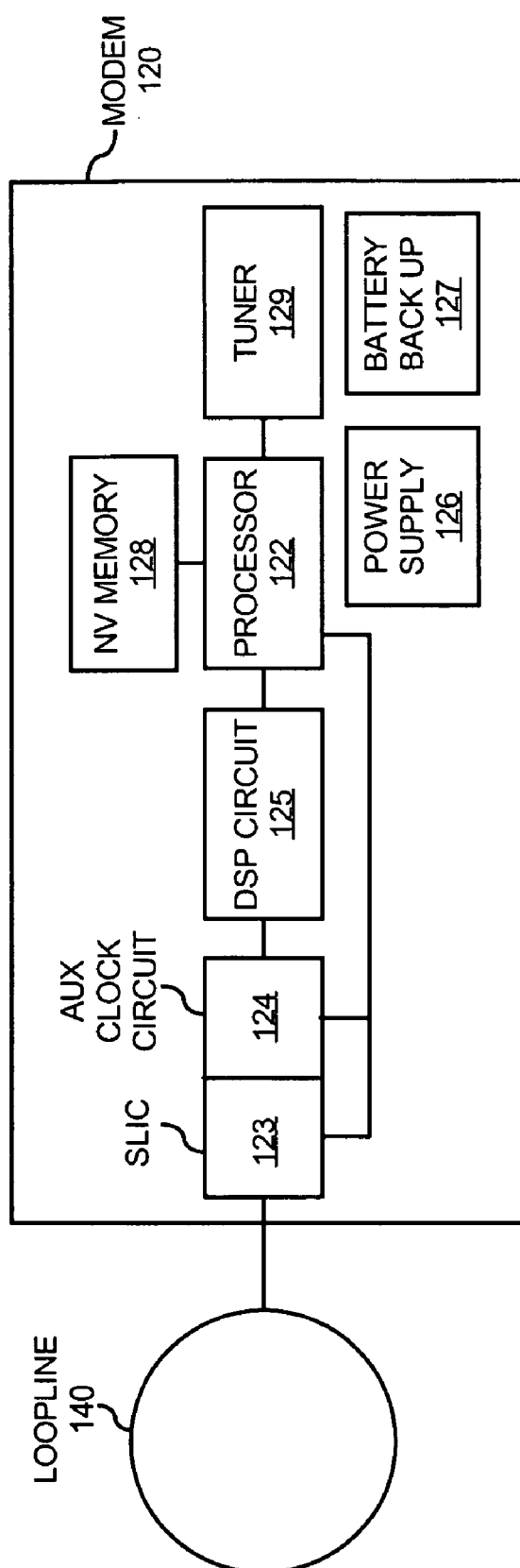


FIG. 2A

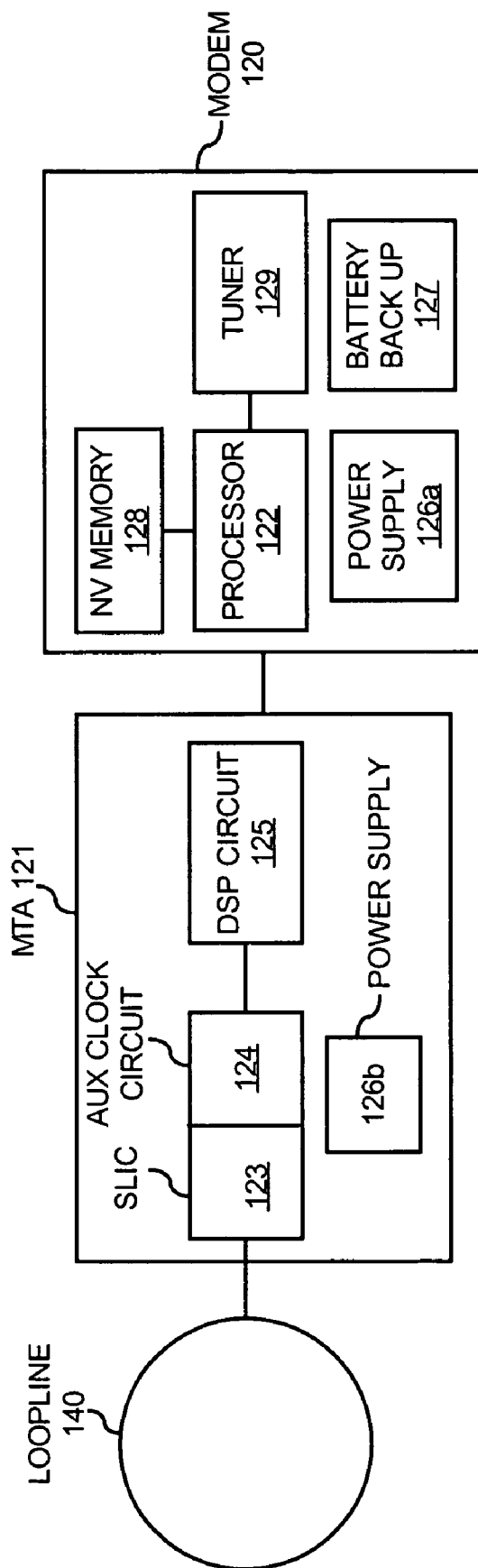


FIG. 2B

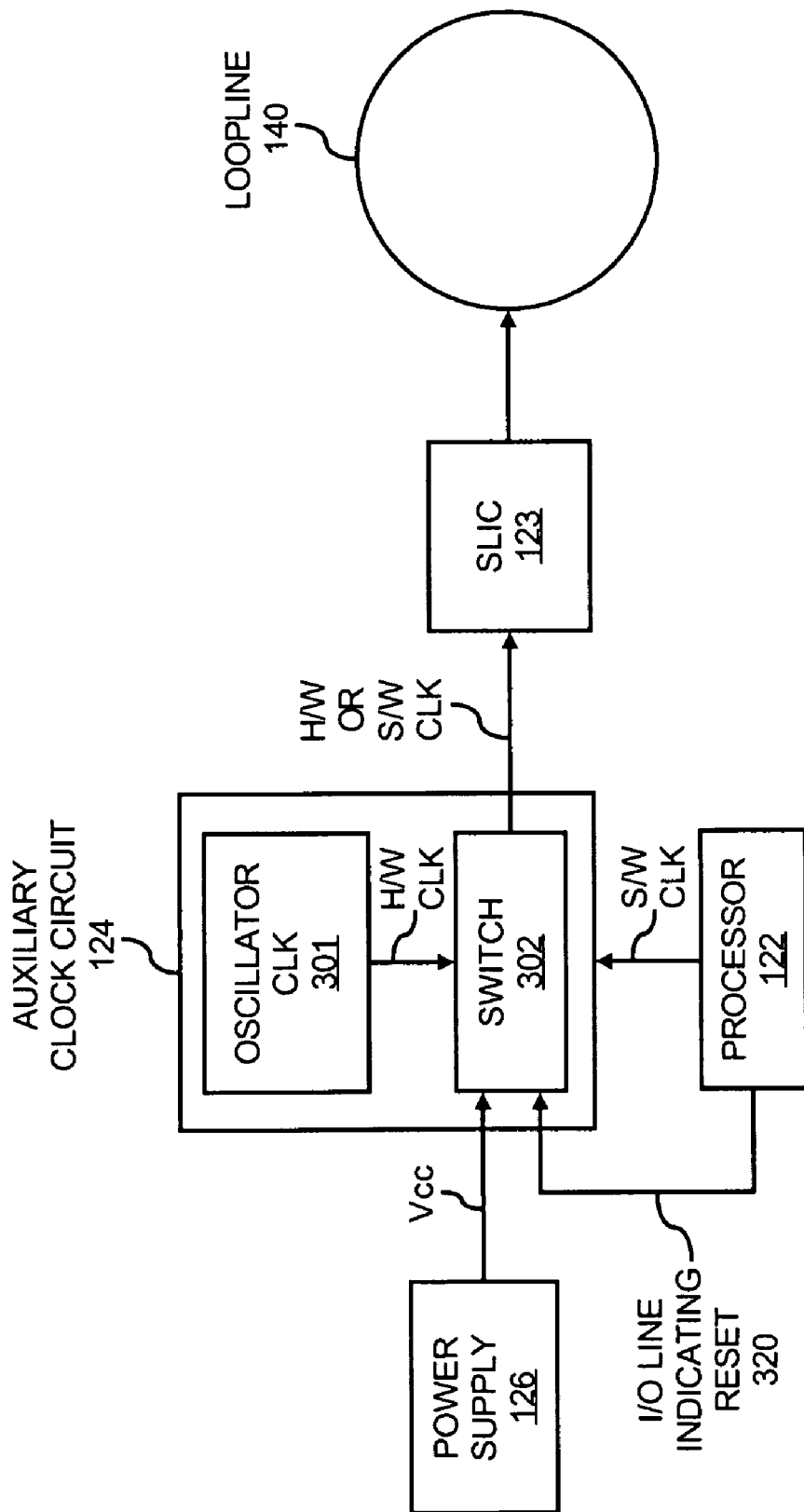


FIG. 3

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