PTO/AIA/15 (03-13)
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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	A0863.70051US04
First Named Inventor	Donald W. Milbrand, Jr.
Title	HIGH PERFORMANCE CABLE CONNECTOR
Express Mail Label No.	

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. [X] **Fee Transmittal Form** (PTO/SB/17 or equivalent)
2. [ ] **Applicant asserts small entity status.** See 37 CFR 1.27
3. [ ] **Applicant certifies micro entity status.** See 37 CFR 1.29. Applicant must attach form PTO/SB/15A or B or equivalent.
4. [X] **Specification** [*Total Pages* 51]
   Both the claims and abstract must start on a new page.
   (See MPEP § 608.01(a) for information on the preferred arrangement)
5. [X] **Drawing(s)** (35 U.S.C. 113) [*Total Sheets* 12]
6. **Inventor's Oath or Declaration** [*Total Pages* 1]
   (including substitute statements under 37 CFR 1.64 and assignments serving as an oath or declaration under 37 CFR 1.63(e))
   a. [ ] Newly executed (original or copy)
   b. [X] A copy from a prior application (37 CFR 1.63(d))
7. [X] **Application Data Sheet** * *See note below.*
   See 37 CFR 1.76 (PTO/AIA/14 or equivalent)
8. **CD-ROM or CD-R** in duplicate, large table, or Computer Program (*Appendix*)
   [ ] Landscape Table on CD
9. **Nucleotide and/or Amino Acid Sequence Submission** (*if applicable, items a. – c. are required*)
   a. [ ] Computer Readable Form (CRF)
   b. [ ] Specification Sequence Listing on:
      i. [ ] CD-ROM or CD-R (2 copies); or
      ii. [ ] Paper
   c. [ ] Statements verifying identity of above copies

ADDRESS TO:
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

ACCOMPANYING APPLICATION PAPERS

10. [ ] **Assignment Papers** (cover sheet & document(s))
    Name of Assignee
11. [ ] **37 CFR 3.73(c) Statement** (*when there is an assignee*) [ ] **Power of Attorney**
12. [ ] **English Translation Document** (*if applicable*)
13. [ ] **Information Disclosure Statement** (PTO/SB/08 or PTO-1449)
    [ ] Copies of citations attached
14. [ ] **Preliminary Amendment**
15. [ ] **Return Receipt Postcard** (*MPEP § 503*) (*Should be specifically itemized*)
16. [ ] **Certified Copy of Priority Document(s)** (*if foreign priority is claimed*)
17. [X] **Nonpublication Request** Under 35 U.S.C. 122(b)(2)(B)(i). Applicant must attach form PTO/SB/35 or equivalent.
18. [ ] **Other:**

***Note:** (1) Benefit claims under 37 CFR 1.78 and foreign priority claims under 1.55 **must** be included in an Application Data Sheet (ADS).
(2) For applications filed under 35 U.S.C. 111, the application must contain an ADS specifying the applicant if the applicant is an assignee, person to whom the inventor is under an obligation to assign, or person who otherwise shows sufficient proprietary interest in the matter. See 37 CFR 1.46(b).

19. CORRESPONDENCE ADDRESS

[X] The address associated with Customer Number: 23628 **OR** [ ] Correspondence address below

Name					
Address					
City		State		Zip Code	
Country		Telephone		Email	

Signature	William R. McClellan	Date	March 9, 2016
Name (Print/Type)	William R. McClellan	Registration No. (Attorney/Agent)	29,409

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PTO/SB/17 (03-13)
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FEE TRANSMITTAL

Complete if known	
Application Number	Not Yet Assigned
Filing Date	Concurrently Herewith
First Named Inventor	Donald W. Milbrand, Jr.
Examiner Name	Not Yet Assigned
Art Unit	N/A
Practitioner Docket No.	A0863.70051US04

☐ Applicant asserts small entity status. See 37 CFR 1.27.

☐ Applicant certifies micro entity status. See 37 CFR 1.29. Form PTO/SB/15A or B or equivalent must either be enclosed or have been submitted previously.

TOTAL AMOUNT OF PAYMENT ($) 1,760.00

METHOD OF PAYMENT (check all that apply)

☐ Check ☒ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☐ Deposit Account Deposit Account Number: 23/2825 Deposit Account Name: Wolf, Greenfield & Sacks, P.C.

For the above-identified deposit account, the Director is hereby authorized to (check all that apply):

☐ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, **except for the filing fee**

☒ Charge any additional fee(s) or underpayment of fee(s) under 37 CFR 1.16 and 1.17 ☒ Credit any overpayment of fee(s)

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES (U = undiscounted fee; S = small entity fee; M = micro entity fee)

	FILING FEES			SEARCH FEES			EXAMINATION FEES			
Application Type	U ($)	S ($)	M ($)	U ($)	S ($)	M ($)	U ($)	S ($)	M ($)	Fees Paid ($)
Utility	280	140*	70	600	300	150	720	360	180	1,600.00
Design	180	90	45	120	60	30	460	230	115	
Plant	180	90	45	380	190	95	580	290	145	
Reissue	280	140	70	600	300	150	2,160	1,080	540	
Provisional	260	130	65	0	0	0	0	0	0	

* The $140 small entity status filing fee for a utility application is further reduced to $70 for a small entity status applicant who files the application via EFS-Web.

2. EXCESS CLAIM FEES

Fee Description	Undiscounted Fee ($)	Small Entity Fee ($)	Micro Entity Fee ($)
Each claim over 20 (including Reissues)	80	40	20
Each independent claim over 3 (including Reissues)	420	210	105
Multiple dependent claims	780	390	195

Total Claims	Extra Claims	Fee ($)	Fee Paid ($)
22 - 20 or HP =	2 x	80.00 =	160.00

HP = highest number of total claims paid for, if greater than 20.

Multiple Dependent Claims	
Fee ($)	Fee Paid ($)

Indep. Claims	Extra Claims	Fee ($)	Fee Paid ($)
1 - 3 or HP =	x	=	

HP = highest number of independent claims paid for, if greater than 3.

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $400 ($200 for small entity) ($100 for micro entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee ($)	Fee Paid ($)
48 - 100 =		/50 = (round **up** to a whole number) x		=

4. OTHER FEE(S)

	Fees Paid ($)
Non-English specification, $130 fee (no small or micro entity discount)	
Non-electronic filing fee under 37 CFR 1.16(t) for a utility application, $400 fee ($200 small or micro entity)	
Other (e.g., late filing surcharge):	

SUBMITTED BY

Signature	William R. McClellan	Registration No. (Attorney/Agent)	29,409	Telephone	617.646.8000
Name (Print/Type)	William R. McClellan			Date	March 9, 2016

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PTO/SB/35 (07-09)
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NONPUBLICATION REQUEST UNDER 35 U.S.C. 122(b)(2)(B)(i)	First Named Inventor	Donald W. Milbrand, Jr.
	Title	HIGH PERFORMANCE CABLE CONNECTOR
	Attorney Docket Number	A0863.70051US04

I hereby certify that the invention disclosed in the attached application **has not and will not be** the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

I hereby request that the attached application not be published under 35 U.S.C. 122(b).

William R. McClellan
Signature

March 9, 2016
Date

William R. McClellan
Typed or printed name

29,409
Registration Number, if applicable

617.646.8000
Telephone Number

This request must be signed in compliance with 37 CFR 1.33(b) and submitted with the application **upon filing.**

Applicant may rescind this nonpublication request at any time. If applicant rescinds a request that an application not be published under 35 U.S.C. 122(b), the application will be scheduled for publication at eighteen months from the earliest claimed filing date for which a benefit is claimed.

If applicant subsequently files an application directed to the invention disclosed in the attached application in another country, or under a multilateral international agreement, that requires publication of applications eighteen months after filing, the applicant **must** notify the United States Patent and Trademark Office of such filing within forty-five (45) days after the date of the filing of such foreign or international application. **Failure to do so will result in abandonment of this application (35 U.S.C. 122(b)(2)(B)(iii)).**

Application Data Sheet

Inventor Information

Inventor Number::	1
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Correspondence Information

Correspondence Customer Number::	23628

Application Information

Application Type::	Regular
Subject Matter::	Utility
CD-ROM or CD-R?::	None
Sequence submission?::	None

Computer Readable Form (CRF)?::	No
Title::	HIGH PERFORMANCE CABLE CONNECTOR
Attorney Docket Number::	A0863.70051US04
Request for Early Publication?::	No
Request for Non-Publication?::	Yes
Total Drawing Sheets::	12
Small Entity?::	No
Petition included?::	No
Authorization to Permit Access to the Instant Application by the Participating Offices::	Yes
This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013::	No

Representative Information

Representative Customer Number::	23628

Domestic Priority Information

Application::	Continuity Type::	Parent Application::	Parent Filing Date::
This Application	Continuation of	13/683295	11/21/12
13/683295	Continuation of	13/671096	11/07/12
13/671096	Continuation of	PCT/US2011/035515	05/06/11
PCT/US2011/035515	An application claiming the benefit under 35 USC 119(e)	61/332366	05/07/10

Foreign Priority Information

Applicant Information

Applicant Number::	1
Applicant Type::	Assignee
Organization Name::	Amphenol Corporation
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City of mailing address::	Wallingford Center
State or Province of mailing address::	CT
Postal or Zip Code of mailing address::	06492-3574

Assignee Information Including Non-Applicant Assignee Information

Assignee Number::	1
Organization Name::	Amphenol Corporation
Street of mailing address::	358 Hall Avenue
City of mailing address::	Wallingford Center

State or Province of mailing address::	CT
Postal or Zip Code of mailing address::	06492-3574

Authorization or Opt-Out of Authorization to Permit Access

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

Signature:

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	William R. McClellan	Date (YYYY-MM-DD)	2016-03-09
Name	William R. McClellan	Registration Number	29,409

DECLARATION (37 C.F.R. § 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 C.F.R. § 1.76)

Title of Invention	HIGH PERFORMANCE CABLE CONNECTOR

As the below named inventor, I declare that:

This declaration is directed to:

☐ The attached application, or

☒ United States application or PCT international application number 13/683,295 filed on November 21, 2012

☐ As amended on _____ (if applicable);

The above-identified application was made or authorized to be made by me.

I believe the inventor(s) named below to be the original and first inventor(s) of the subject matter which is claimed and for which a patent is sought.

I believe I am the original inventor or an original joint inventor of a claimed invention in the application.

I have reviewed and understand the contents of the above-identified application, including the claims, as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in 37 C.F.R. § 1.56.

All statements made herein of my own knowledge are true, and all statements made herein on information and belief are believed to be true.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. § 1001 by fine or imprisonment of not more than five (5) years, or both.

LEGAL NAME OF SOLE OR FIRST INVENTOR

Inventor one: Donald Milbrand, Jr. Date: 9/4/13

Signature: _____ Citizen of: US

LEGAL NAME OF ADDITIONAL JOINT INVENTOR, if any

Inventor two: Brian Kirk Date: 9/4/13

Signature: _____ Citizen of: US

LEGAL NAME OF ADDITIONAL JOINT INVENTOR, if any

Inventor three: Prescott B. Atkinson Date: 9/4/13

Signature: _____ Citizen of: US

☐ Additional inventors are being named on _____ additional form(s) attached hereto.

2920460.1

HIGH PERFORMANCE CABLE CONNECTOR

RELATED APPLICATIONS

[001] This application is a continuation of U.S. Application Serial No. 13/683,295, filed on November 21, 2012, and titled "HIGH PERFORMANCE CABLE CONNECTOR", which application is a continuation of U.S. Patent Application Serial No. 13/671,096, filed on November 7, 2012, and titled "HIGH PERFORMANCE CABLE CONNECTOR," which application is a continuation of and claims the benefit under 35 U.S.C. §§120 and 365(c) of International Application PCT/US2011/035515, with an international filing date of May 6, 2011, and titled "HIGH PERFORMANCE CABLE CONNECTOR," which applications are herein incorporated by reference in their entirety. This application also claims the benefit under 35 U.S.C. §119(e) of U.S. Provisional Patent Application Serial No. 61/332,366, filed on May 7, 2010, and titled, "HIGH PERFORMANCE CABLE CONNECTOR," which application is hereby incorporated herein by reference in its entirety.

FIELD OF THE INVENTION

[002] This invention application relates generally to electrical interconnection systems and more specifically to interconnections between cables and circuit assemblies.

RELATED TECHNOLOGY

[003] Electronic systems are frequently manufactured from multiple interconnected assemblies. Electronic devices, such as computers, frequently contain electronic components attached to printed circuit boards. One or more printed circuit boards may be positioned within a rack or other support structure and interconnected so that data or other signals may be processed by the components on different printed circuit boards.

[004] Frequently, interconnections between printed circuit boards are made using electrical connectors. To make such an interconnection, one electrical connector is attached to each printed circuit board to be connected, and those boards are positioned such that the connectors mate, creating signal paths between the boards. Signals can pass from board to board through the connectors, allowing electronic components on different

printed circuit boards to work together. Use of connectors in this fashion facilitates assembly of complex devices because portions of the device can be manufactured on separate boards and then assembled. Use of connectors also facilitates maintenance of electronic devices because a board can be added to a system after it is assembled to add functionality or to replace a defective board.

[005] In some instances, an electronic system is more complex or needs to span a wider area than can practically be achieved by assembling boards into a rack. It is known, though, to interconnect devices, which may be widely separated, using cables. In this scenario, cable connectors, designed to make connections between conductors of cables and conductors of printed circuit boards within the devices may be used. The cable connectors may be separable, with a cable end terminated with a cable connector, sometimes called a "plug." A printed circuit board within the electronic device may contain a board-mounted connector, sometimes called a "receptacle," that receives the plug. Rather than being mounted to align with a connector on another board, the receptacle is positioned near an opening in an exterior surface, sometimes referred to as a "panel," of the device. The plug may be inserted through the opening in the panel, to mate with the receptacle, completing a connection between the cable and electronic components within the device.

[006] An example of a board-mounted connector is the small form factor pluggable, or SFP, connector. SFP connectors have been standardized by an SFF working group and are documented in standard SFF 8431. Though, cable connectors in other form factors are known, including connectors made according to the QSFP standard.

SUMMARY

[007] Improved electrical performance and ease of use of a cable connector may be provided through incorporation of one or more design features. These features may be used alone or in combination.

[008] According to an aspect of the present application, there is provided a receptacle assembly comprising: a housing having a mating face; a plug-receiving port within the mating face; a plurality of conductive elements disposed within the housing, each of the conductive elements comprising a mating contact portion within the port; a

hole in the mating face, the hole being bounded by at least one wall; and a compliant member within the hole, the compliant member comprising a segment, the segment being adjacent the wall at a first location and extending toward a centerline of the hole at a second location, the first location being closer to the mating face than the second location.

[009] In some embodiments, the segment of the compliant member is a first segment; and the compliant member comprises a second segment.

[010] In some embodiments, the compliant member comprises a metal strip bent to form the first segment and the second segment.

[011] In some embodiments, the compliant member comprises a metal strip.

[012] In some embodiments, the compliant member is a J-shaped member.

[013] In some embodiments, the receptacle comprises at least two ports in the mating face.

[014] According to an aspect of the present application, there is provided a receptacle assembly, in combination with a plug, the plug comprising: a shell; a planar member disposed within the shell, the planar member comprising plurality of conductive elements, each conductive element having a mating contact portion, a screw comprising a thread, wherein: the planar member of the plug is positioned within the plug-receiving port to align the mating contact portions of the conductive elements within the plug with the mating contact portion of the conductive elements within the receptacle assembly; the segment of the complaint member has a distal end; and the screw is inserted in the hole with the distal end of the segment engaging the thread of the screw.

[015] In some embodiments, the combination further comprises a cable and the plug is attached to the cable.

[016] In some embodiments, the combination further comprises a printed circuit board mounted adjacent a panel of an electronic device, the panel comprising an opening and the plug-receiving port being positioned in the opening.

[017] According to an aspect of the present application, there is provided a method of operating an interconnection system comprising a receptacle and a plug, the method comprising: inserting the plug into a port in the receptacle; securing the plug to the

receptacle by pressing a screw coupled to the plug into a hole in the receptacle; and releasing the plug from the receptacle by rotating the screw.

[018] In some embodiments, the receptacle comprises a retaining member and pressing the screw into the hole comprises deflecting the retaining member.

[019] In some embodiments, the screw comprises a thread; the retaining member comprises a distal end; and deflecting the retaining member comprises deflecting the retaining member such that the thread of the screw passes the distal end of the retaining member.

[020] In some embodiments, rotating the screw comprises sliding the thread of the screw along the distal end of the retaining member.

[021] In some embodiments, inserting the plug into the port comprises making a plurality of electrical connections between a cable attached to the plug and a printed circuit board attached to the receptacle.

[022] In some embodiments, the screw comprises a shaft with the thread extending from the shaft; and pressing the screw into the hole further comprises releasing compressive force on the distal end such that the distal end presses against the shaft.

[023] According to an aspect of the present application, there is provided a receptacle assembly comprising: a housing having a mating face; a plug-receiving port within the mating face; a hole in the mating face; and a metal member within the hole, the metal member comprising a segment, the segment being ramped toward a centerline of the hole.

[024] In some embodiments, the metal member is springy.

[025] In some embodiments, the hole is bounded by at least one wall; the segment is a first segment; and the metal member comprises a second segment, the second segment being parallel to a wall of the at least one wall and the first segment joined to the second segment at an acute angle.

[026] According to an aspect of the present application, there is provided a receptacle assembly, in combination with a plug, the plug comprising: a shell; and a screw comprising a thread, wherein: at least a portion of the plug is positioned within the plug-receiving port; the segment of the metal member has a distal end; and the screw is inserted in the hole with the distal end of the segment engaging the thread of the screw.

[027] In some embodiments, the combination further comprises a printed circuit board mounted adjacent a panel of an electronic device, the panel comprising an opening and the plug-receiving port and the hole being positioned in the opening.

[028] The foregoing is a non-limiting summary of the invention, which is defined by the attached claims.

BRIEF DESCRIPTION OF DRAWINGS

[029] The accompanying drawings are not intended to be drawn to scale. In the drawings, each identical or nearly identical component that is illustrated in various figures is represented by a like numeral. For purposes of clarity, not every component may be labeled in every drawing. In the drawings:

[030] FIG. 1 is a perspective view of an electronic assembly incorporating an interconnection system according to some embodiments of the invention;

[031] FIG. 2 is a partially exploded view of a receptacle assembly according to some embodiments of the invention;

[032] FIG. 3 is a view from below of a receptacle assembly according to some embodiments of the invention;

[033] FIG. 4 is a partially exploded view of a front housing portion of a receptacle assembly according to some embodiments of the invention;

[034] FIG. 5 is a partially exploded view of a receptacle according to some embodiments of the invention;

[035] FIG. 6 is an exploded view of a portion of a receptacle according to some embodiments of the invention;

[036] FIGs. 7A and 7B are schematic illustrations of profiles of the mating faces of a receptacle and a plug according to some embodiments of the invention;

[037] FIG. 8 is a sketch of a lead frame of a plug according to some embodiments of the invention;

[038] FIG. 9 is a partially exploded view of a plug sub-assembly according to some embodiments of the invention;

[039] FIG. 10 is a sketch, partially exploded, of a portion of a wafer according to some embodiments of the invention;

[040] FIG. 11 is a sketch of a wafer sub-assembly according to some embodiments of the invention;

[041] FIG. 12A is a perspective view of a plug from below, according to some embodiments of the invention;

[042] FIG. 12B is a sketch, partially exploded, of the plug of FIG. 12A;

[043] FIG. 13A is a schematic illustration of features for mounting a plug to a cable bundle according to some embodiments of the invention;

[044] FIG. 13B is a cross-section through a portion of a plug attached to a cable bundle according to some embodiments of the invention;

[045] FIG. 14 is a sketch showing a plug mated with a receptacle assembly according to some embodiments of the invention; and

[046] FIG. 15 is a cross-section through a portion of a plug secured to a receptacle assembly according some embodiments of the invention.

DETAILED DESCRIPTION

[047] A cable connector according to embodiments of the invention may be used to interconnect electronic devices as is known in the art. However, the cable connector may include features that provide desirable electrical performance, such as reduced crosstalk between signals propagating through interconnection system less attenuation or more uniform attenuation at frequencies of signals to be conveyed through the interconnection system. In some embodiments, the interconnection system may provide acceptable attenuation over a frequency range up to 16 GHz or beyond.

[048] Features to provide this electrical performance may be incorporated in connectors that are easy to use. Such connectors may facilitate quickly and reliably making multiple connections to an electronic device, such as a router or a telecommunications switch, to which multiple other devices may be connected through cables.

[049] In one aspect, a receptacle may have mating contact portions of conductive elements forming multiple ports positioned such that the ports are staggered. This

arrangement of the mating contact portions may reduce crosstalk through the cable connector. This arrangement also facilitates a housing for the receptacle that has an L-shaped profile on its mating face. A plug adapted for mating with such a receptacle may have a complementary profile on its mating face, allowing the plug to be inserted into the receptacle in only one orientation.

[050] In another aspect, the plug may contain subassemblies, each of which provides mating contact portions for a port. The plug may be adapted to mate with staggered ports by mounting the subassemblies in a shell in a staggered arrangement.

[051] Each sub-assembly may comprise at least two insulative housings, each holding a plurality of conductive elements. Two such subassemblies may be mounted with mating contact portions of the respective conductive elements facing outwards and an electrically lossy member between the insulative housings.

[052] In some embodiments, the conductive elements of each sub-assembly may contain conductive elements sized and positioned to act as a differential pair. The differential pairs may be separated by conductive elements adapted to act as ground conductors. The lossy member may have projections extending through the insulative housings towards the ground conductors, coupling the ground conductors to the lossy member.

[053] In another aspect, each of the subassemblies may have a conductive segment, embedded in the insulative housings. The conductive segment may connect the distal ends of the mating contact portions of the ground conductors, thereby improving electrical performance. In some embodiments, such a conductive segment may be stamped as part of a lead frame from which the plurality of conductive elements are formed. When the lead frame is formed, the conductive segment may be positioned out of the plane of the mating contact portions of the conductive elements. When an insulative housing is molded over the lead frame, the conductive segment is mechanically and electrically isolated from mating contact portions in a mating connector.

[054] In another aspect, a plug may be designed for quick, yet secure, connection to a receptacle assembly. The plug may contain a screw that may slide within the shell. A receptacle assembly may have an opening adapted to receive a threaded end of the screw

when the plug and receptacle are mated. The receptacle assembly may include a compliant member adjacent such a hole. Once the plug is mated with the receptacle, a user may press on the screw. The compliant member may deflect, allowing threads of the screw to slide past an end of the compliant member as the screw enters the hole. The compliant member may be shaped to engage a thread on the screw if the screw is pulled in a direction to remove the screw from the hole. Consequently, the plug is quickly and securely attached to the receptacle assembly, though the screw may be removed by rotation of the screw to slide the thread over the compliant member.

[055] In yet another aspect, a plug may be designed for simple, yet robust, connection to a cable bundle in a fashion that preserves desirable electrical properties in the cable attachment region. A ferrule may be used at an end of a cable to be attached to plug. The ferrule may have two or more pieces that can be easily inserted under a jacket of the cable. Though, the pieces, collectively, may form a tubular surface resistant to deformation by radial forces on the cable. A braid from within the cable may be exposed exterior to the cable jacket. Attachment of a shell may generate a radial force pinching the jacket and braid between the shell and ferrule, securing the shell to the cable bundle. The radial force may also press the shell and braid together, making an electrical connection between the shell and braid in embodiments in which the shell is formed of a conductive material. Interior portions of the cable bundle, holding signal conductors are not deformed by this force because the presence of the ferrule.

[056] FIG. 1 is a sketch of an interconnection system 100 in which embodiments of the invention may be practiced. FIG. 1 provides a simplified view of portions of an electronic device that may be connected to other electronic devices through cable bundle 160. The electronic device includes a printed circuit board 120 contained within an enclosure that includes a panel 190, a portion of which is shown in phantom in FIG. 1.

[057] Electronic components may be mounted to printed circuit board 120, and printed circuit board 120 may contain other connectors to connect printed circuit board 120 to other printed circuit boards within the device. These components may be as known in the art and are not shown for simplicity.

[058] The simplified example of FIG. 1, shows only a portion of the electronic device where cable bundle 160 is connected to the device. Though one such cable

bundle is shown, it should be appreciated that electronic devices may connect to multiple cable bundle. To facilitate more such connections, additional components could be included, effectively duplicating interconnection system 100 for each cable bundle to make connections to components within the electronic device. Therefore, embodiments are possible in which panel 190 includes multiple openings, each adapted to receive a cable connector. These openings may be arrayed in rows or disposed in any suitable way, but are not expressly illustrated for simplicity of illustration.

[059] In the embodiment illustrated, receptacle assembly 110 is attached, along a lower face, to printed circuit board 120. To facilitate attachment to printed circuit board 120, receptacle assembly 110 includes mounting features 118. In the example of FIG. 1, mounting features 118 are in the shape of posts extending from receptacle assembly 110 towards printed circuit board 120. Attachment is made by inserting each of the mounting features 118 into a respective mounting hole 124 on printed circuit board 120. In this example, mounting features 118 and mounting holes 124 provide a mechanical coupling between receptacle assembly 110 and printed circuit board 120.

[060] In addition, electrical connections may be made between printed circuit board 120 and conductive elements of receptacle assembly 110. Mounting features 118 may additionally, or alternatively, provide such electrical connection. In some embodiments, portions of receptacle assembly 110 may be connected to an electrical ground. For example, cage 112 that provides an outer casing for receptacle assembly 110 may be formed of conductive material that may be connected to ground, to reduce interference with other components of the electronic device caused by electromagnetic radiation emanating from receptacle assembly 110. In these embodiments, mounting features 118 may be conductive and interior walls of mounting hole 124 may be connected to ground within printed circuit board 120.

[061] Other electrical connections between printed circuit board 120 and receptacle assembly 110 may be used to couple electrical signals some or all of these signal may be high speed differential signals, such as digital data signals communicating digital data at a rate between 1 Gbps and 8 Gbps. In the embodiment illustrated, electrical connections for signals are formed between receptacle assembly 110 and printed circuit board 120 by inserting projections (not shown in FIG. 1) from receptacle assembly 110 into holes in

printed circuit board 120. In the example of FIG. 1, the holes form a connector footprint 122. Each of the holes within connector footprint 122 may be electrically connected within printed circuit board 120 to a trace, a ground plane or other conductive structure. Projections inserted into the holes 122 make electrical connection, via the holes, to the conducting structures within printed circuit board 120. In this way, signals and reference potentials may be coupled between components on printed circuit board or otherwise within the electronic device to conductive elements (not shown in FIG. 1) within receptacle assembly 110.

[062] Though, it should be recognized that projections inserted into via holes on the printed circuit board are only one example of a mechanism that may be used to make electrical connections between conductive elements within receptacle assembly 110 and conductive elements within printed circuit board 120. More generally, the conductive elements within receptacle assembly 110 may include tails extending from receptacle assembly 110 that may be attached to conductive structures on printed circuit board 120 in any suitable way. The tails may be soldered within the holes, may have compliant segments that form press fit connections when inserted in the holes or the tails may be attached to conductive pads on the service of printed circuit board 120, without being inserted into the holes. Accordingly, the specific structure of the tails extending from conductive elements within receptacle assembly 110 and the specific mechanism by which the tails are attached to printed circuit board 120 are not critical to the invention.

[063] In addition to making electrical connections, the projections from receptacle assembly 110 that are attached to footprint 122 may also provide mechanical attachment of receptacle assembly 110 to printed circuit board 120. Though, any suitable combination of features may be used for making electrical and/or mechanical connections between receptacle assembly 110 and printed circuit board 120.

[064] The projections from receptacle assembly 110 may serve as tails for conductive elements that propagate signals through receptacle assembly 110 to one or more ports (not visible in FIG. 1) where those conductive elements may mate with conductive elements (not visible in FIG. 1) within plug 150. As shown in FIG. 1, receptacle assembly 110 is positioned within an opening in panel 190 such that plug 150 may be inserted into an opening of receptacle assembly 110. In this configuration, a

mating face of plug 150 engages a mating face of a receptacle within receptacle assembly 110.

[065] Once plug 150 is inserted into receptacle assembly 110, it may be secured with an attachment mechanism. In this example, the attachment mechanism includes lock screw 152. Once plug 150 is inserted into receptacle assembly 110, lock screw 152 aligns with hole 116 in receptacle assembly 110. Interior portions (not visible in FIG. 1) of receptacle assembly 110 adjacent hole 116 may be adapted to engage a threaded end (not visible in FIG. 1) of lock screw 152. In this way, plug 150 may be secured to receptacle assembly 110 and therefore to the electronic device incorporating receptacle assembly 110, by engaging lock screw 152. Conversely, plug 150 may be separated from the electronic device by unscrewing lock screw 152 and removing plug 150.

[066] Other features of interconnection system 110 are also visible in FIG. 1. Receptacle assembly 110 is shown with an EMI gasket 114. EMI gasket 114 provides a seal between receptacle assembly 110 and panel 190 and reduces the amount of electromagnetic radiation emanating from receptacle assembly 110 or from entering receptacle assembly 110.

[067] FIG. 2 is a partially exploded view of receptacle assembly 110. FIG. 2 reveals that receptacle assembly 110 may be constructed such that cage 112 (FIG. 1) encloses a receptacle 220. Further, FIG. 2 shows that cage 112 may be constructed from multiple components. In this example, cage 112 is constructed from cage body 112A and front member 112B. Though cage 112 may be assembled from any suitable number of components.

[068] In the embodiment illustrated in FIG. 2, the components of cage 112 may be partially or totally conductive. In some embodiments, cage body 112A may be formed by bending a sheet of metal to have generally U-shaped cross section such that cage body 112A fits over receptacle 220. Though, any suitable construction technique may be used to form cage body 112A.

[069] Front member 112B may also be formed from conductive materials according to any suitable techniques. With front member 112B attached to cage body 112A, receptacle 220 may be enclosed within cage 112, preventing electromagnetic radiation

from emanating from receptacle 220 and interfering with electronic circuitry in the vicinity of receptacle 220.

[070] Cage 112 may also guide a plug 150 (FIG. 1) into engagement with receptacle 220. A plug inserted into an opening in panel 190 surrounded by cage 112 will be positioned by cage body 112A to align with receptacle 220. In the example of FIG. 2, receptacle 220 is formed with two ports, port 210A and 210B. Each of the ports 210A and 210B is shaped to receive a generally planar member from plug 150. Each of the ports 210A and 210B may contain mating contact portions of conductive elements (not visible in FIG. 2) within receptacle 220. The mating contact portions may be positioned within the ports 210A and 210B to make electrical connection with complimentary mating contact portions on the planar members from the plug.

[071] FIG. 3 shows an alternative view receptacle assembly 110, revealing a lower surface 350 of receptacle 220. Contact tails (of which contact tail 310 is numbered) of conductive elements within receptacle 220 extend through lower surface 350. In this embodiment, the conductive elements are positioned in four columns such that four columns, 312A, 312B, 312C and 312D of contact tails are visible in the view of FIG. 3.

[072] In the embodiment illustrated, conductive elements in each of two columns extend into one of the ports 210A or 210B. In the specific example of FIG. 3, columns 312A and 312B contain contact tails for conductive elements that extend into port 210B. Columns 312C and 312D contain contact tails for conductive elements that extend into port 210A. Accordingly, when the contact tails in columns 312A and 312B are secured to holes within footprint 122, they provide an electrical connection between conductive elements within printed circuit board 120 (FIG. 1) and conductive elements within port 210B. Likewise, when the contact tails in columns 312C and 312D are attached to holes within footprint 122, they complete an electrical connection between conductive elements within printed circuit board 120 and mating contact portions within port 210A.

[073] Turning to FIG. 4, additional details of front member 112B are illustrated. In the embodiment illustrated in FIG. 4, front member 112B is formed from a front housing portion 412 to which EMI gasket members 114A, 114B, 114C and 114D are attached. Front housing portion 412 may be formed of a conductive material. For example, front

housing portion 412 may be formed of metal using a die casting process. Though, any suitable construction techniques or materials may be used.

[074] Gasket elements 114A, 114B, 114C and 114D may be formed in any suitable way. In the embodiment illustrated, the gasket elements are each formed from a sheet of metal that is stamped and bent into the shapes shown. Each of the gasket elements may be U-shaped to fit around wall of front housing portion 412. Each of the gasket elements also may be formed with multiple flexible fingers extending from a common base portion (of which common base portion 414A is numbered). The common base portion of each of the gasket elements 114A…114D may be attached to a wall surrounding an opening in front housing portion 412 through which plug 150 (FIG. 1) may pass. The common base portion (of which common base portion 414 on gasket element 114A is numbered) may be attached to a wall, such as wall 432 surrounding an opening in front housing portion 412 using any suitable attachment technique. As an example, common base portion 414 may be welded to wall 432. With this attachment, a subset of the fingers (of which finger 416 is numbered) may extend outwardly from the opening in front housing portion 410. Another subset of the fingers (of which finger 418 is numbered) may extend into the opening of front housing portion 412.

[075] In the example of FIG. 4, both the outwardly extending and inwardly extending fingers are formed of a springy metal such that each finger is compliant. Accordingly, inwardly extending fingers (of which finger 418 is numbered) may press against a shell of plug 150 inserted into the opening in front housing portion 412. Outwardly extending fingers (of which finger 416 is numbered) may press against an opening in panel 190 (FIG. 1) when receptacle assembly 110 is inserted into the opening of the panel. In this way, gasket elements 114A…114D may block openings between a plug inserted into front housing portion 412 and panel 190, thereby forming a seal blocking the passage of electromagnetic radiation.

[076] In addition, front housing portion 412 is shaped to provide a hole 116 into which lock screw 152 may be inserted. In the embodiment illustrated, hole 116 may be formed to provide a quick connect feature for lock screw 152. The quick connection features allow lock screw 152 to engage front housing portion 412 without requiring lock screw 152 to be rotated.

[077] To support this quick connect feature, hole 116 may have a generally smooth inner diameter equal to or greater than the maximum diameter of a thread on a threaded end of lock screw 152. A retention element 420 also may be included. Here, retention element 420 is J-shaped and is held within format housing portion 114. To hold lock screw 152 within hole 116, a compliant member 422 projects into hole 116 on retention element 420 and forms an acute angle with respect to a base portion 426. Insertion of lock screw 152 may deflect compliant member 422 such that lock screw 152 may enter hole 116. Compliant member 422 may be positioned such that once a portion of the thread is pushed passed the distal end 424 of compliant member 422, the distal end 424 will engage the thread, thereby preventing lock screw 152 from being withdrawn from hole 116 without rotating the screw.

[078] In the embodiment illustrated in FIG. 4, compliant member 422 is a portion of retention element 420. Retention element 420 includes a base 426 that may be fixed within an opening in front housing portion 412. That opening may be adjacent hole 116 such that when base 426 is secured to front housing portion 412, compliant member 422 projects into hole 116. Further detail of this locking arrangement is illustrated in conjunction with FIG. 15, below.

[079] Turning to FIG. 5, additional detail of receptacle 220 is illustrated. In the example of FIG. 5, receptacle 220 is formed from an insulative housing 510 and a lead sub-assembly 550.

[080] Insulative housing 510 may be formed in any suitable way, including molding of a thermal plastic material. Housing 510 may be formed of an insulative material. For example, it may be molded from a dielectric material such as plastic or nylon. Examples of suitable materials are liquid crystal polymer (LCP), polyphenyline sulfide (PPS), high temperature nylon or polypropylene (PPO). Other suitable materials may be employed, as the present invention is not limited in this regard. All of these are suitable for use as binder materials in manufacturing connectors according to the invention. One or more fillers may be included in some or all of the binder material used to form housing 510 to control the electrical or mechanical properties of housing 510. For example, thermoplastic PPS filled to 30% by volume with glass fiber may be used.

[081] In the example embodiment of FIG. 5, housing 510 is formed with two cavities, 520A and 520B. Cavity 520A has a lower surface 522 and an upper surface 524. Cavity 520B has a lower surface 526 and an upper surface 528. Each of the surface 522, 524, 526 and 528 is shaped to receive a column of mating contacts portions of conductive elements within receptacle 220. When lead sub-assembly 550 is inserted into housing 510, a column of mating contact portions is positioned along each of the surfaces. Column 512A of mating contact portions is positioned along surface 528. Column 512B of mating contact portions is positioned along surface 526. Column 512C of mating contact portions is positioned along surface 525 and column 512D of mating contact portions is positioned along surface 522. In this example, the mating contact portions form linear arrays of contacts along the surfaces of the cavities. Though, any suitable pattern of contact portions may be used.

[082] In this example, the mating contact portions of receptacle 220 are shaped as compliant beams. As can be see in FIG. 5, each of the surfaces 522, 524, 526 and 528 includes slots into which individual mating contact portions may fit, allowing compliant motion of the mating contact portions when a member is inserted into cavity 520A or 520B. Consequently, cavity 520A in combination with columns 512C and 512D of mating contact portions forms port 210A (FIG. 2) into which a member from plug 150 (FIG. 1) may be inserted. Likewise, cavity 520B in combination with columns 512A and 512B of mating contact portions forms port 210B, into which a second member of plug 150 may be inserted when receptacle 220 is mated with plug 150.

[083] Turning to FIG. 6, additional details of lead sub-assembly 550 are illustrated. In the illustrated embodiment, each of the columns of conductive elements is held within a separate assembly. In the example of FIG. 6, lead assemblies 610A, 610B, 610C and 610D are shown. In this example, each of the lead assemblies 610A…610D includes a column of conductive elements held within an insulative housing portion. Lead assembly 610A includes a column of conductive elements for which column 312A of contact tails and column 512A of mating contact portions can be seen.

[084] Intermediate portions (not numbered) of the conductive elements are also visible in the illustration of FIG. 6. The intermediate portions are held within housing member 612A. Housing member 612A may be an insulative material, including a

material of the type used to form housing 510. Lead assembly 610A may be formed in any suitable way, including molding housing member 612A over a portion of the conductive elements in lead assembly 610A. Though, other construction techniques may be employed, including inserting the conductive elements into housing member 612A.

[085] Lead assembly 610B may be similarly formed, with a housing member 612B holding intermediate portions of a column of conductive elements with a column 312B of contact tails and column 512B of mating portions extending from housing member 612B. Lead assembly 610C may likewise be formed in similar way to secure a column of conductive elements with a column 312C of contact tails and a column 512C of mating contact portions.

[086] Lead assembly 610D may be similarly formed, with a housing member 612D securing a column of conductive elements such that a column 312D of contact tails and a column 512D of mating contact portions are exposed. Additionally, housing member 612D may also act as an organizer for the components of lead sub-assembly 550. Housing member 612D may be formed with a lower surface 350 (FIG. 3) containing multiple columns of holes (not numbered) through which columns 312A, 312B and 312C of contact tails may be inserted. Housing member 612D may therefore act as a support member for other components of lead sub-assembly 550.

[087] Improved electrical performance may be provided by inserts separating adjacent ones of the lead assemblies 610A…610D. In the embodiment illustrated in FIG. 6, insert 650 separates lead assemblies 610C and 610D. Insert 652 separates lead assemblies 610A and 610B. In this example, an insert is provided between lead assemblies containing mating contact portions positioned on opposing surfaces of the same port. Though, in other embodiments, inserts may be included between lead assemblies containing conductive elements of different ports. In some embodiments, inserts 650 and 652 may be of insulative material and may serve a mechanical support function. In other embodiments, inserts, such as inserts 650 and 652, may instead of or in addition to providing mechanical support alter the electrical performance of interconnection system 110. In the embodiment illustrated, each of inserts 650 and 652 may be at least partially conductive. In some embodiments, the inserts may be formed of

metal or other material that may be regarded as a conductor. In other embodiments, the inserts may be formed of a lossy material.

[088] Materials that conduct, but with some loss, over the frequency range of interest are referred to herein generally as "lossy" materials. Electrically lossy materials can be formed from lossy dielectric and/or lossy conductive materials. The frequency range of interest depends on the operating parameters of the system in which such a connector is used, but will generally be between about 1 GHz and 25 GHz, though higher frequencies or lower frequencies may be of interest in some applications. Some connector designs may have frequency ranges of interest that span only a portion of this range, such as 1 to 10 GHz or 3 to 15 GHz or 3 to 6 GHz.

[089] Electrically lossy material can be formed from material traditionally regarded as dielectric materials, such as those that have an electric loss tangent greater than approximately 0.003 in the frequency range of interest. The "electric loss tangent" is the ratio of the imaginary part to the real part of the complex electrical permittivity of the material.

[090] Electrically lossy materials can also be formed from materials that are generally thought of as conductors, but are either relatively poor conductors over the frequency range of interest, contain particles or regions that are sufficiently dispersed that they do not provide high conductivity or otherwise are prepared with properties that lead to a relatively weak bulk conductivity over the frequency range of interest. Electrically lossy materials typically have a conductivity of about 1 siemans/meter to about 6.1 x 10^7 siemans/meter, preferably about 1 siemans/meter to about 1 x 10^7 siemans/meter and most preferably about 1 siemans/meter to about 30,000 siemans/meter.

[091] Electrically lossy materials may be partially conductive materials, such as those that have a surface resistivity between 1 Ω/square and 10^6 Ω/square. In some embodiments, the electrically lossy material has a surface resistivity between 1 Ω/square and 10^3 Ω/square. In some embodiments, the electrically lossy material has a surface resistivity between 10 Ω/square and 100 Ω/square. As a specific example, the material may have a surface resistivity of between about 20 Ω/square and 40 Ω/square.

[092] In other embodiments, the lossy materials maybe electromagnetic absorptive material, include ferrule magnetic materials.

[093] In some embodiments, electrically lossy material is formed by adding to a binder a filler that contains conductive particles. Examples of conductive particles that may be used as a filler to form an electrically lossy material include carbon or graphite formed as fibers, flakes or other particles. Metal in the form of powder, flakes, fibers or other particles may also be used to provide suitable electrically lossy properties. Alternatively, combinations of fillers may be used. For example, metal plated carbon particles may be used. Silver and nickel are suitable metal plating for fibers. Coated particles may be used alone or in combination with other fillers, such as carbon flake. In some embodiments, the conductive particles disposed in inserts 650 and 652 may be disposed generally evenly throughout, rendering a conductivity of the lossy portion generally constant. In other embodiments, a first region of inserts 650 and 652 may be more conductive than a second region of insert 650 and 652 so that the conductivity, and therefore amount of loss within inserts 650 and 652 may vary. In embodiments in which the lossy material is magnetically lossy material, the filler may include ferrous materials.

[094] The binder or matrix may be any material that will set, cure or can otherwise be used to position the filler material. In some embodiments, the binder may be a thermoplastic material such as is traditionally used in the manufacture of electrical connectors to facilitate the molding of the electrically lossy material into the desired shapes and locations as part of the manufacture of the electrical connector. However, many alternative forms of binder materials may be used. Curable materials, such as epoxies, can serve as a binder. Alternatively, materials such as thermosetting resins or adhesives may be used. Also, while the above described binder materials may be used to create an electrically lossy material by forming a binder around conducting particle fillers, the invention is not so limited. For example, conducting particles may be impregnated into a formed matrix material or may be coated onto a formed matrix material, such as by applying a conductive coating to a plastic housing. As used herein, the term "binder" encompasses a material that encapsulates the filler, is impregnated with the filler or otherwise serves as a substrate to hold the filler.

[095] Preferably, the fillers will be present in a sufficient volume percentage to allow conducting paths to be created from particle to particle. For example, when metal fiber is used, the fiber may be present in about 3% to 40% by volume. The amount of filler may impact the conducting properties of the material.

[096] Filled materials may be purchased commercially, such as materials sold under the trade name Celestran® by Ticona. A lossy material, such as lossy conductive carbon filled adhesive perform, such as those sold by Techfilm of Billerica, Massachusetts, US may also be used. This preform can include an epoxy binder filled with carbon particles. The binder surrounds carbon particles, which acts as a reinforcement for the preform. Such a preform may be shaped to form all or part of inserts 650 and 652 and may be positioned to adhere to ground conductors in the connector. In some embodiments, the preform may adhere through the adhesive in the preform, which may be cured in a heat treating process. Various forms of reinforcing fiber, in woven or non-woven form, coated or non-coated may be used. Non-woven carbon fiber is one suitable material. Other suitable materials, such as custom blends as sold by RTP Company, can be employed, as the present invention is not limited in this respect.

[097] Regardless of the specific material used, inserts 650 and 652 may be formed in any suitable way. In the embodiment illustrated, inserts 650 and 652 are formed by molding a lossy material into a suitable shape, such as the shape illustrated in FIG. 6. In the embodiment illustrated in FIG. 6, inserts 650 and 652 are shaped to selectively couple electrically to one or more of the conductive elements within the columns of conductive elements. To support selective coupling, each of the inserts may have projections on outwardly facing surfaces. For example, insert 652 has projections (of which projection 670 is numbered) on an upward facing surface and projections (of which 672 is numbered) on a lower surface. Each of the projections is positioned to couple to a conductive element in a column of conductive elements in an adjacent lead assembly. In this example, projections on the upper surface of insert 652 are positioned to couple to selective ones of the conductive elements within lead assembly 610A. Projections from the lower surface of insert 652 are positioned to make contact with selected ones of the conductive elements within lead assembly 610B.

[098] Similarly, projections from an upper surface of insert 650 are positioned to make contact with selected ones of the conductive elements in lead assembly 610C. Projections from a lower surface of insert 650 are positioned to make contact with selected ones of the conductive elements in lead assembly 610D. The conductive elements to which the inserts are coupled may be selected based on an intended function of the conductive elements within interconnection system 110. In the specific embodiment illustrated, interconnection system 110 is adapted to carry differential signals. Accordingly, certain ones of the conductive elements in a column will be arranged in pairs, with each conductive element in the pair having similar electrical properties. Taking lead assembly 610D as illustrative, a first differential pair is formed by conductive elements 662A and 662B. A second differential pair is formed by conductive elements 664A and 664B.

[099] Each column of conductive elements may include in addition to signal pairs, multiple conductive elements designed to be ground conductors. In this example, the column of conductive elements includes ground conductors 660A, 660B and 660C. Here, the conductive elements are positioned in the column to create a pattern of ground, signal pair, ground, signal pair, ground. Projections (not numbered) from a lower surface of insert 650 may be positioned to make contact with the ground conductors, 660A, 660B and 660C. A similar pattern of conductive elements, with similar contact between the lossy insert and the grand conductors, may be used in each of the lead assemblies 610A…610D.

[0100] To facilitate contact between inserts 650 and 652 and the ground conductors, the housing members 612A…612D may be shaped with slots that expose portions of the conductive elements acting as ground conductors. For example, housing member 612B is shown with slots (of which slot 682 is numbered) exposing ground conductors. Projection 672 from the lower surface of insert 652 may fit within slot 682, thereby either contacting a conductive element acting as a ground conductor in lead assembly 610B or being positioned enough close to the ground conductor that electrical coupling between the ground conductor and the projection 672 occurs. Other projections from the lower surface of insert 652 may similarly contact the other ground conductors in lead assembly 610B. Projections (of which projection 670 is numbered) from the upper

surface of insert 652 may similar extend into slots in housing member 612A to couple to ground conductors in lead assembly 610A. Projections from the upper the lower surface of insert 650 may likewise extend into slots in housing members 612C and 612D respectively, to couple to the ground conductors in lead assemblies 610C and 610D, respectively.

[0101] In this way, when the elements of lead sub-assembly 550 are assembled, ground conductors for each of the ports may be joined through a common lossy member, which has been found to improve the integrity of high speed signals passing through interconnection system 100.

[0102] FIG. 5 illustrates a further feature that may be used to improve the integrity of high speed signals passing through interconnection system 100. FIG. 5 shows columns 512A and 512B of mating contact portions are vertically aligned such that when lead sub-assembly 550 is inserted into housing 510 columns 512A and 512B will each be positioned along a surface, 528 and 526, respectively of cavity 520B. Similarly, columns 512C and 512D are vertically aligned such that when lead sub-assembly 550 is inserted into housing 510, columns 512C and 512D will line surfaces 524 and 522, respectively, of cavity 520A. With this positioning, the mating contact portions in columns 512A and 512B form mating contacts within port 210B (FIG. 2) and the mating contact portions in columns 512C and 512D form mating contact portions in port 210A. Each of these ports is accessible through mating face 540 of receptacle 220.

[0103] However, as can be seen in FIGs. 2 and 5, ports 210A and 210B are staggered in a horizontal dimension. With this configuration, ports 210A and 210B are offset in a direction parallel to lower surface 350, which in use may be mounted against printed circuit board 120 (FIG. 1). This mounting configuration provides horizontal separation between the mating contact portions of the conductive elements in forming port 210A and 210B. This separation is illustrated by the dimension S in FIG. 5. This offset provides both horizontal and vertical separation between the mating contact portions of the conductive elements within ports 210A and 210B. This separation reduces the extent to which from the mating contact portions of the conductive elements in one port will impact the integrity of signals in the other port.

[0104] Further, offsetting the ports in a right angle connector reduces the length of conductive elements in upper port 210B relative to lengths that may exist in a conventional connector in which ports are vertically aligned. Reducing the length of the conductive elements in upper port 210B may reduce the effect of electromagnetic radiation on those conductive elements, which may be reflected as noise in signals propagating along the conductive elements. Additionally, the conductive elements in port 210B is more nearly equal to the length of the conductive elements in port 210A, which may also contribute to desirable signal properties where differences in propagation delay among signals passing through an interconnection system is undesirable.

[0105] The off-set configuration of ports 210A and 210B also facilitates incorporation of mechanical features contributing to ease of use of interconnection system 100. Staggering the ports facilitates incorporation of an irregular contour in the forward face of receptacle 220. A plug adapted to mate with receptacle 220 may have an irregular contour that is complimentary to the contour of receptacle 220 when the plug is positioned in the intended orientation for mating with receptacle 220. In the example of FIG. 5, an irregular contour is provided in mating face 540 through the positioning of portions 536 and 538 of housing 510. Portion 536 contains port 210A and portion 538 contains port 210B.

[0106] A plug adapted to mate with receptacle 534 may have a forward face that similarly has an irregular profile. The plug may include planar members designed to fit within cavities 520A and 520B when the plug has an intended orientation with respect to receptacle 220 such that the irregular contour of the plug conforms to the irregular contour of the receptacle. However, the plug may have a mating face with portions that will contact one or more of the portions of the mating face 540 if the plug is inserted into receptacle assembly 110 with any other orientation. The plug, for example, may have a portion that contacts portion 536 of receptacle 220, blocking any portion of the plug from entering cavities 520A or 520B. Though, when property inserted, a shell of the plug may contact wall 532 while following the contour of shoulder 534.

[0107] FIGs. 7A and 7B illustrate the manner in which an irregular profile of mating face 540 may allow mating between a plug and receptacle 220 in some orientations, but block mating between receptacle 220 and a plug when the plug is in other orientations.

FIG. 7A illustrates that in profile, receptacle 220 has a generally L-shape, with portion 536 forming a lower horizontal portion of the L. Plug 150 has a similarly L-shaped profile formed by segments 712A and 712B. Though, when positioned for mating with receptacle 220, the L-shaped profile of plug 150 is inverted with respect to that of receptacle 220. As a result, mating end 1232 of plug 150 may slide over housing portion 538 until it abuts wall 532. In this configuration, planar member 710B may enter cavity 520B. Likewise, planar member 710A may enter cavity 520A.

[0108] In plug 150, planar members 710A and 710B have mating contact portions of conductive elements that carry signals through plug 150. The mating contact portions on planar members 710A and 710B may be positioned to align with the mating contact portions of the conductive elements carrying signals through receptacle 220. Accordingly, if planar members 710A and 710B enter cavities 520A and 520B, respectively, the conductive elements in plug 150 made with respective conductive elements in receptacle 220.

[0109] FIG. 7B shows that if plug 150 is positioned with an alternative orientation, plug 150 will not mate with receptacle 220. Specifically, mating end 1232 will abut portion 536, stopping motion of plug 150 towards receptacle 220. As a result, planar member 710B does not enter cavity 520A. Likewise, planar member 710A does not enter cavity 520B. By blocking planar members 710A and 710B from entering cavities 520A and 520B, improper connections between the conductive elements within plug 150 and receptacle 220 are prevented.

[0110] FIGs. 8, 9, 10 and 11 illustrate a technique for forming the planar members, such as 710A and 710B within plug 150. Each of the planar members 710A and 710B may be constructed in the same way. In the example embodiment of FIGs. 8-11, each of the planar members is a wafer sub-assembly 1100 (FIG. 11). Though, any suitable construction techniques may be used.

[0111] In the embodiment illustrated, each wafer sub-assembly is formed from two wafers, each of which includes a lead frame held within an insulative housing. FIG. 8 illustrates a lead frame suitable for use in forming a wafer of a wafer sub-assembly 1100. In the example of FIG. 8, each wafer includes conductive elements configured to form two differential signal pairs. Conductive elements forming ground conductors may be

interspersed with the signal pairs. As a specific example, FIG. 8 shows a lead frame 810 including conductive elements 870A and 870B, forming a first differential signal pair. Conductive elements 872A and 872B form a second differential signal pair. In lead frame 810, conductive elements 860A, 860B and 860C may be designated as ground conductors. With this configuration, each of the differential signal pairs is positioned along a column between two adjacent ground conductors.

[0112] In this example of FIG. 8, lead frame 810 includes a conductive segment 830 interconnecting conductive elements 860A, 860B and 860C. In this configuration, conductive segment 830 electrically interconnects the ground conductors in a wafer that may be used in forming a wafer sub-assembly. The inventors have recognized and appreciated that connecting the distal ends of the ground conductors may improve the integrity with which signals propagate through interconnection system 100.

[0113] Lead frame 810 may be formed from materials of the type known in the art for forming conductive elements within an electrical connector. For example, lead frame 810 may be formed of a copper alloy. All or portions of the conductive elements may be coated. For example, the portions of the conductive elements in region 840 form tails for the conductive elements. The portions of the conductive elements in region 840 may be coated with nickel, tin or other solder wettable material to facilitate attachment of other conductors in region 840 as part of attaching a wafer sub-assembly to a cable. Portions of conductive elements in region 842, forming the mating contact portions of the conductive elements, may be coated with gold or other malleable conductive material resistant to oxidation. Such coatings may be applied using techniques as are known in the art.

[0114] In forming lead frame 810, a blanking operation may be used to provide conductive elements having a desired outline. As part of the blanking operation, a carrier strip 820 may be retained to facilitate handling of lead frame 810. Once the conductive elements are embedded within insulative housing, carrier strip 820 may be separated from the conductive elements. Once conductive elements are blanked from a sheet of metal, the conductive elements may be shaped in a forming operation. In the embodiment illustrated in FIG. 8, the conductive elements are generally planar. However, the forward mating ends of the conductive elements are tapered in the

downward direction in the orientation illustrated in FIG. 8. Conductive segment 830 is formed to extend below these tapered portions of the conductive elements. This positioning embeds conductive segment 830 and the distal ends of the conductive elements 860A, 870A, 870B, 860B, 872A, 872B and 860C in an insulative housing 910 (FIG. 9) when lead frame 810 is incorporated into a wafer 900.

[0115] FIG. 9 illustrates an example of a wafer 900 formed by embedding lead frame 810 in an insulative housing 910. Any suitable technique may be used to embed lead frame 810 within housing 910. For example, an over molding process as is known in the art may be used to form wafer 900. The over molding may be performed using an insulative material of type described above for forming receptacle housing 510, or any other suitable material.

[0116] In the configuration illustrated in FIG. 9, though the distal tips of the conductive elements of lead frame 810 are embedded within insulative housing 910, surfaces of the conductive elements within region 842 (FIG. 8) are exposed FIG. in a surface of housing 910. The exposed portions form mating contact portions of the conductive elements in plug 150. Here, the mating contact portions are shaped as conductive pads. Housing 910 may be formed with one or more cavities. For example, such as cavity 912 may be formed between portions of conductive elements that form a differential pair. As shown, cavity 912 separates conductive elements 870A and 870B.

[0117] Contact tails in region 840 of lead frame 810 are also exposed. In the configuration illustrated in FIG. 9, the contact tails extend from a rearward portion of housing 910. In this configuration, the contact tails are positioned for attachment to cables. In this example, two cables, cables 920A and 920B are attached to conductive elements within wafer 900. Each of the cables 920A and 920B contains a pair of signal wires, of which signal wires 970A and 970B numbered in FIG. 9. Each of the signal wires may be attached to a contact tail of a signal conductor in lead frame 810. In the embodiment illustrated in FIG. 9 signal wire 970A may be attached to a tail of conductive element 870A. Likewise, wire 970B may be attached to a tail of conductive element 870B. Wires associated with cable 920B may similarly be attached to tails of conductive elements 872A and 872B. The wires may be attached to the tails in any

suitable way. The wires, for example, may be welded, brazed or soldered to the contact tails. Though any suitable attachment technique may be used.

[0118] Each of the cables 920A and 920B may also include a drain wire, of which drain wire 972 is numbered. Drain wire 972 may be electrically coupled to one or more of the tails of the ground conductors. In the embodiment illustrated, drain wire 972 is indirectly coupled to tails of conductive elements 860A, 860B and 860C through corrugated plate 930.

[0119] Corrugated plate 930 is shaped to make contact with tails of ground conductors in wafer 900. The corrugations, though, prevent contact with signal wires or signal tails. Corrugated plate 930 may be welded to tails of conductive elements 860A, 860B and 860C and may have a portion adjacent drain wire 972. Placing plate 930 in proximity to drain wire 972 may provide electrical coupling through capacitive means between drain wire 972 and plate 930 such that an adequate electrical connection is formed between drain wire 972 and one or more of the tails of the ground conductors to which plate 930 is attached. Alternatively, drain wire 972 may be connected to plate 930, such as by brazing or soldering. Though, in other embodiments, a direct connection may be formed between a drain wire, such as drain wire 972, and a ground conductor. Such a direct connection may be formed, for example, by welding.

[0120] In addition to providing electrical coupling for drain wires, such as drain wire 972, and a corresponding drain wire (not numbered) in cable 920B, corrugated plate 930 may provide shielding in the vicinity of the contact tails for the conductive elements within wafer 900. Corrugated plate 930 provides such shielding for radiation emanating from or incident on signal wires, such as 970A and 970B, from an upper direction in the orientation illustrated in FIG. 9. A similar corrugated plate may be attached from below, effectively providing shielding on both sides of signal wires and contact tails. FIG. 10 shows two such wafers, wafers 1050A and 1050B, each with two corrugated plates welded to tails of ground conductors to encircle the signal conductors by the plates.

[0121] Corrugated plate 930 may be formed of a metal or any other suitable conductive material, which may be stamped and formed into a suitable shape.

[0122] In the example of FIG. 10, wafer 1050 includes corrugated plates 930A and 930B. Wafer 1050B includes corrugated plates 930C and 930D.

[0123] FIG. 10 is a partially exploded view of wafer assembly 1100. In the example of FIG. 10, wafer assembly 1100 is formed from two wafers 1050A and 1050B. In this example, each of the wafers 1050A and 1050B has the same shape. However, wafer 1050B has an opposite orientation from wafer 1050A. As can be seen in FIG. 10, the mating contact portions of the conductive elements in wafer 1050A are exposed in an outwardly facing surface 1010. Outwardly facing surface 1010 of wafer 1050A has an upward orientation in the example of FIG. 10. Wafer 1050B has a similar outwardly facing surface, but it has a downwardly facing direction in the configuration of FIG. 10 and therefore is not visible. Rather, an inwardly facing surface 1012, of wafer 105B, which has an upward orientation in FIG. 10, is visible. Wafer 1050A has a corresponding inwardly facing surface, which has a downwardly facing direction in FIG. 10 and therefore is not visible.

[0124] In assembling wafer sub-assembly 1100, wafers 1050A and 1050B are aligned with their inwardly facing surfaces, facing each other. Between the inwardly facing surfaces, a lossy member 1020 may be included. Lossy member 1020 may be formed of a suitable lossy material, including lossy material having properties as described above in connection with the inserts of the receptacle 220. In the embodiment illustrated, lossy member 1020 is formed of a material that is partially conductive. In this embodiment, lossy member 1020 may be electrically isolated from signal conductors within wafers 1050A and 1050B by the insulative housings of those wafers.

[0125] In the embodiment illustrated, however, lossy member 1020 may be electrically coupled to ground conductors within wafers 1050A and 1050B. This coupling may be provided through projections from surfaces of lossy member 1020. In FIG. 10, upwardly facing surface 1022 of lossy member 1020 is visible. Projections 1024, 1026 and 1028 are formed in surface 1022. Projections 1024, 1026 and 1028 are aligned with the ground conductors in wafer 1050A. Similar projections may extend from a lower surface (not visible in FIG. 10) of lossy member 1020. Those projections may be positioned to align with ground conductors in wafer 1050B. To facilitate electrical connection between the projections of lossy member 1010 and the ground conductors, the insulative housings of wafers 1050A and 1050B may be formed with openings aligned with the ground conductors. In FIG. 10, openings 1032, 1034 and 1036

are visible in inwardly facing surface 1012 of wafer 1050B. The inwardly facing surface of wafer 1050A may have similar openings to receive projections 1024, 1026 and 1028.

[0126] In some embodiments, the openings, such as openings 1032, 1034 and 1036 may expose a subset of the conductive elements in wafer 1050B through inwardly facing surface 1012. That subset may include some or all of the ground conductors in wafers 1050B. As a result, lossy member 1020 may provide access to the ground conductors in wafer 1050B. Similar openings in the inwardly facing surface of wafer 1050A may provide lossy coupling between the ground conductors in wafer 1050A to provide lossy coupling between that subset of the conductive elements in wafer 1050A. Such a coupling may improve signal integrity, particularly of high frequency signals propagating through the signal conductors of wafers 1050A and 1050B.

[0127] In some embodiments, projections, such as projections 1024, 1026 and 1028 may be electrically coupled to ground conductors by making direct contact to those conductive elements. However, in other embodiments, coupling between lossy member 1020 and the ground conductors may be capacitive such that merely positioning the projections in close proximity to the ground conductors may achieve sufficient electrical coupling.

[0128] A wafer assembly 1100 may be formed by aligning wafers 1050A and 1050B with their inwardly facing surfaces facing towards each other and with lossy member 1020 between wafers 1050A and 1050B. Wafers 1050A and 1050B may then be secured together, holding lossy member 1020 in place. In this example, each of the wafers 1050A and 1050B is shown with attachment features that may be used to secure wafers 1050A and 1050B together. As illustrated, each of the wafers includes a post, such as post 1014 which is aligned with a hole, such as hole 1016. Post 1014 may be retained in hole 1016 such as through welding, through the use of adhesives, through an interference fit or in any other suitable way.

[0129] Regardless of the manner in which wafers 1050A and 1050B are secured, the resulting wafer sub-assembly 1100 may have the form illustrated in FIG. 11. In this view, FIG. projection 1024 contacting conductive element 860C is visible. Conductive segment 830, embedded in the housing of wafer 1050A is also visible.

[0130] With wafers 1050A and 1050B secured together, wafer sub-assembly 1100 forms a planar member 1120. As can be seen, planar member 1120 includes the conductive elements of wafer 1050A on an outwardly facing surface of wafer 1050A, facing in an upward direction in the orientation of FIG. 11. In this example, mating contact portions of the conductive elements are held in a plane defined by the upper surface. Though not visible in FIG. 11, the outwardly facing surface of wafer 1050B, which is facing in a downward direction in FIG. 11, contains contact portions of the conductive elements of wafer 1050B. Accordingly, planar member 1120 includes mating contact portions of conductive elements on both outwardly facing surfaces. Accordingly, planar member 1120 may serve the purpose of planar members 710 (FIG. 7) for insertion into a port in receptacle 220 (FIG. 2).

[0131] Wafer sub-assembly 1100 includes attachment features that allow it to be held within a shell of a plug. In the example of FIG. 11, those attachment features include attachment features 1112 and 1114. In this example, the attachment features are in the form of slots that may engage corresponding projections in a shell. Though, any suitable attachment feature may be used.

[0132] FIG. 12A illustrates two wafer subassemblies, wafer subassemblies 1100A and 1100B, in a shell 1210 that acts as a housing for plug 150. As can be seen in the view of plug 150 presented in FIG. 12A, the planar numbers of wafer subassemblies 1100A and 1100B are aligned in parallel. Wafer subassemblies 1100A and 1100B are held within shell 1210 as such that wafer sub-assembly 1100B is closer to mating face 1200 then wafer sub-assembly 1100A. Though, wafer sub-assembly 1100B is set back from mating end 1232 such that the mating contact portions are within shell 1210.

[0133] FIG. 12A reveals the L-shaped profile of shell 1210 along mating face 1200. Here, a portion of the L-shaped profile is formed by sidewall 1234. Sidewall 1234 is set back from mating end 1232. When plug 150 is mated with a receptacle in the form of receptacle 220 (FIG. 2), sidewall 1234 may abut shoulder 534 (FIG. 5). With mating end 1232 abutting wall 532 and sidewall 1234 abutting shoulder 534, wafer sub-assembly 1100B will be positioned to enter cavity 520B and wafer sub-assembly 1100A will be positioned to enter cavity 520A. In this way, the conductive elements along the upper and lower outwardly facing surfaces of wafer 1100B may mate with columns of

conductive elements 512A and 512B, respectively within port 210B of receptacle 220. Similarly, the conductive elements positioned along the upper and lower outwardly facing surfaces of wafer sub-assembly 1100A will mate with conductive elements in columns 512C and 512D, respectively, within port 210A of receptacle 220. Though, as illustrated in connection with FIG. 7, if plug 150 is inverted, mating between plug 150 and receptacle 220 will be blocked when mating end 1232 of plug 150 contacts portion 536 of the receptacle housing.

[0134] FIG. 12B illustrates an exemplary construction of shell 1210 to hold wafer subassemblies 1100A and 1100B in the desired orientation. In the example illustrated, shell 1210 is formed from two pieces, upper shell portion 1210A and lower shell portion 1210B. Shell portions 1210A and 1210B may be made of any suitable material. However, in the embodiment illustrated, shell 1210 is conductive and upper shell portion 1210A and lower shell portion 1210B are formed of a conductive material. As one example, shell portion 1210A and 1210B may be formed of metal using die casting techniques.

[0135] In the embodiment illustrated, lower shell portion 1210B is shaped to receive wafer subassemblies 1100A and 1100B in positions that will orient the planar members of the wafer subassemblies adjacent mating face 1200. Upper shell portion 1210A is shaped to be secured to lower shell portion 1210B to hold wafer subassemblies 1100A and 1100B in position. In the example of FIG. 12B, screws 1220A and 1220B may be used to hold upper shell portion 1210A to lower shell portion 1210B. Though, any suitable fastening mechanism may be used, such as rivets, instead of or in addition to screws.

[0136] Any suitable features may be used to retain wafer subassemblies 1100A and 1100B within shell 1210. As one example, FIG. 12B shows that lower shell portion 1210B contains a region 1260 shaped to receive a rear housing portion of wafer sub-assembly 1100A.

[0137] Attachment features may also be included to position wafer sub-assembly 1100B. FIG. 12B illustrates attachment features 1214, which in this example are shaped as projections that may engage complimentary attachment features, such as attachment features 1112 and 1114 of wafer sub-assembly 1100B. Though, the specific attachment

features used is not critical to the invention and any suitable mechanism may be used to retain wafer subassemblies 1100A and 1100B within shell 1210.

[0138] Shell 1210 may serve other functions in addition to providing a housing for wafer subassemblies 1100A and 1100B. Shell 1200 may retain a fastening mechanism, such as screw 152, such that plug 150 may be secured to a receptacle assembly. Accordingly, lower shell portion 1210B may include a hole 1252 to receive screw 152. Lower shell portion 1210B may be shaped such that when screw 152 is inserted fully into hole 1252, thread 1254 may extend through hole 1252 such that it may engage a receptacle assembly. Screw 152 may be held within hole 1252 using a clip or other mechanism that allows screw 152 to rotate and slide within hole 1252, but prevents screw 152 from being fully withdrawn from hole 1252.

[0139] Shell 1210 may additionally be constructed to make electrical and mechanical connection to cable bundle 160. As illustrated in FIG. 12B, upper shell portion 1210A includes a region 1272 and lower shell portion 1210B includes a region 1274. Regions 1272 and 1274 are generally circular and are sized to receive cable bundle 160. However, the sizing is such that when upper shell portion 1210A is secured to lower shell portion 1210B, portions of cable bundle 160 will be squeezed against regions 1272 and 1274, making a desired electrical and mechanical connection between cable bundle 160 and shell 1210.

[0140] FIGs. 13A and 13B illustrate electrical and mechanical attachment between shell 1210 and cable bundle 160. Cable bundle 160 may contain multiple cables of which cables 1322A and 1322B are numbered in FIG. 13A. As illustrated in FIG. 10, conductors from two cables are attached to the conductive elements within each wafer, such as wafers 1050A and 1050B. Accordingly, as illustrated in FIG. 11, the conductors within four cables are attached to the conductive elements within each wafer sub-assembly, such as wafer sub-assembly 1100. In a plug in the form illustrated in FIG. 12B containing two wafer subassemblies, there may be eight cables within cable bundle 160. Though, it should be appreciated that the number of cables within a cable bundle is not critical to the invention.

[0141] FIG. 13B illustrates cables 1322A… 1322H within cable bundle 160. Each of the cables may be held in interior portion 1332 of cable bundle 160. Further, though not

shown in Figs. 13A and 13B, each of the cables 1322A… 1233H may contain two signal wires, such as signal wires 970A and 970B (FIG. 9), and a drain wire, such as drain wire 972. These wires within each cable may be held within a core of a dielectric material within the cable. The cores of the cables position the wires within the cables to provide desired impedance for conveying differential signals. FIG. 13B illustrates an attachment mechanism that makes a secure electrical and mechanical connection between cable bundle 160 and shell 1200, without crushing cable bundle 160 in a way that would alter the spacing between wires in the cables 1322A…. 1322H. In this way, the electrical properties of cables 1322A…, 1322H are not degraded when cable bundle 160 is attached to shell 1200.

[0142] The attachment mechanism includes a multipart ferrule attached at an end of cable bundle 160. In the example illustrated in Figs. 13A and 13B, the multipart ferrule includes two parts, ferrule parts 1310A and 1310B. Though, it should be appreciated that a multipart ferrule may have more than two parts.

[0143] Each of the ferrule parts 1310A and 1310B may be inserted under jacket 1330 of cable bundle 160. In this example, each of the ferrule parts 1310A and 1310B is inserted under braid 1320. A portion of braid 1320 extending beyond jacket 1330 may be folded back on top of jacket 1330. The portion of cable bundle 160 containing ferrule 1310 may be positioned between shell portions 1210A and 1210B in regions 1272 and 1274. When shell portions 1210A and 1210B are secured together, cable bundle 160 will be secured between shell portions 1210A and 1210B.

[0144] To increase the force asserted by shell portions 1210A and 1210B against cable bundle 160, projections may be included in shell portions 1210A. FIG. 13B illustrates projections 1340A, 1340B and 1340C. In the illustrated embodiment in projections 1340A and 1340B are semicircular ribs lining an interior surface of shell portion 1210A in region 1272. The semicircular ribs extend in a direction perpendicular to the elongated axis of cable bundle 160. Similarly, projection 1340C may be formed as a semicircular rib in lower shell portion 1210B.

[0145] When shell portions 1210A and 1210B are secured together, braid 1320 and jacket 1330 will be pinched between ferrule 1310 and projections 1340A, 1340B, and 1340C. Though ferrule 1310 is in multiple pieces, the pieces collectively define a closed

path encircling cables 1322A…, 1322H. As a result, even though shell portions 1210A and 1210B press against ferrule halves 1310A and 1310B, the cores within cables 1322A…, 1322H are not appreciably compressed. As a result, a strong mechanical attachment is formed without altering the electrical properties of cables 1322A…, 1322H.

[0146] Additionally, because projections 1340A, 1340B, and 1340C directly contact braid 1320, a good electrical connection is formed between braid 1320 and shell 1210.

[0147] Such strong electrical and mechanical connections may be formed using simple assembly techniques. The multiple piece nature of ferrule 1310 allows the ferrule to be attached to cable bundle 160 after wafer subassemblies 1100A and 1100B have been attached to the cables within cable bundle 160. For example, as illustrated in FIG. 13A, the end of cable bundle 160 may be prepared for a plug 150 to be attached by stripping portions of jacket 1330 to expose lengths of cables 1310 (FIG. 12B). Each of the cables may then be stripped to reveal wires, such as 970A and 970B (FIG. 9). These wires may then be brazed or otherwise attached tails extending from a wafer. The wafers may then be attached to form wafer subassemblies. With the wafer subassemblies attached to the ends of cables 1322A…, 1322H, jacket 1330 and braid 1320 may be trimmed to appropriate lengths to fit within regions 1272 and 1274. Once the elements of cable bundle 160 are cut to the appropriate length, ferrule halves 1310A and 1310B may be inserted in cable bundle 160.

[0148] With plug 150 attached to cable bundle 160, plug 150 may be inserted into receptacle assembly 110. In this way, electrical connections may be formed between signal wires within cable bundle 160 and conductive traces within a printed circuit board, such as printed circuit board 120 to which receptacle assembly 110 is attached. To secure plug 150 in place, screw 150 may be engaged.

[0149] FIG. 15 shows in cross section plug 150 secured to receptacle assembly 110 via screw 152. In the configuration illustrated, screw 152 had been pressed into hole 116 (FIG. 1). Thread 1510 at a distal end of screw 152 has slid past compliant member 422 such that compliant member 422 engages thread 1510. In this state, screw 152 is prevented by the locking action of compliant member 422 against thread 1510 from

being pulled out of hole 116. However, screw 152 may be removed by rotating screw 152 such that thread 1510 slides along compliant member 422.

[0150] Having thus described several aspects of at least one embodiment of this invention, it is to be appreciated various alterations, modifications, and improvements will readily occur to those skilled in the art.

[0151] For example, the techniques described herein need not all be used together. These techniques may be used in any suitable combination to provide desired connector performance.

[0152] As another example of possible variations, although inventive aspects are shown and described with reference to cable connectors, some or all of these techniques may be applied to connectors of other types, such as backplane connectors.

[0153] Also, though embodiments of connectors assembled from wafers are described above, in other embodiments connectors may be assembled from wafers without first forming wafers. As one example connectors may be assembled by inserting multiple columns of conductive members into a housing.

[0154] In the embodiments illustrated, some conductive elements are designated as forming differential pairs of conductors and some conductive elements are designated as ground conductors. These designations refer to the intended use of the conductive elements in an interconnection system as they would be understood by one of skill in the art. For example, though other uses of the conductive elements may be possible, differential pairs may be identified based on preferential coupling between the conductive elements that make up the pair. Electrical characteristics of the pair, such as its impedance, that make it suitable for carrying a differential signal may provide an alternative or additional method of identifying a differential pair. For example, a pair of signal conductors may have a differential mode impedance of between 75 Ohms and 100 Ohms. As a specific example, a signal pair may have an impedance of 85 Ohms +/- 10% or 100 Ohms +/- 10%. A ground conductor may have a higher inductance than a signal conductor, which may lead to an impedance outside this range. As yet another example, a connector in which a column containing pairs of high speed signal conductors and adjacent ground conductors was described. It is not a requirement that every signal conductor in a column be part of a pair or that every signal conductor be a high speed

signal conductor. In some embodiments, columns may contain lower speed signal conductors intermixed with high speed signal conductors.

[0155] As another example, certain features of connectors were described relative to a "front" face. The front face of a connector may be regarded as surfaces of the connector facing in the direction from which a mating connector is inserted. However, it should be recognized that terms such as "front" and "rear" are intended to differentiate surfaces from one another and may have different meanings in electronic assemblies in different forms. Likewise, terms such as "upper" and "lower" are intended to differentiate features based on their position relative to a printed circuit board or to portions of a connector adapted for attachment to a printed circuit board. Such terms as "upper" and "lower" do not imply an absolute orientation relative to an inertial reference system or other fixed frame of reference.

[0156] As a further example, hole 116, which receives a fastening member attached to plug 150, is shown to be formed as part of front housing portion 114 of the receptacle assembly. Such a hole may be incorporated into the receptacle assembly in any suitable way, including being formed in a panel incorporating the receptacle assembly.

[0157] In accordance with the foregoing, some novel aspects of the present application are summarized below.

[0158] According to an aspect of the present application, there is provided a receptacle adapted for mounting to a printed circuit board, the receptacle comprising: a housing, the housing comprising a first portion with a first cavity and a second portion with a second cavity, the first cavity being bounded by a first surface and an opposing second surface, and the second cavity being bounded by a third surface and an opposing fourth surface; a first plurality of conductive elements, a second plurality of conductive elements, a third plurality of conductive elements, and a fourth plurality of conductive elements, each conductive element of the first, second, third and fourth pluralities of conductive elements comprising a tail adapted for attachment to a printed circuit board, a mating contact portion and an intermediate portion coupling the tail to the mating contact portion, wherein: the mating contact portions of the first plurality of conductive elements are disposed along the first surface of the first cavity; the mating contact portions of the second plurality of conductive elements are disposed along the second surface of the first

cavity; the mating contact portions of the third plurality of conductive elements are disposed along the third surface of the second cavity; the mating contact portions of the fourth plurality of conductive elements are disposed along the fourth surface of the second cavity; and the first portion extends, in a direction perpendicular to the first surface, beyond the second portion.

[0159] In some embodiments, the first surface, the second surface, the third surface and the fourth surface are parallel.

[0160] In some embodiments, the housing has a lower surface; and the tails of the first, second, third and fourth pluralities of conductive elements extend through the lower surface.

[0161] In some embodiments, the housing further comprises a projection extending from the lower surface.

[0162] In some embodiments, the housing is insulative; and the receptacle is in a combination with a conductive cage, the conductive cage comprising a rectangular opening, wherein the first portion is closer to the rectangular opening than the second portion.

[0163] In some embodiments, the cage comprises a body portion and a front portion, the end portion comprising a radio frequency seal.

[0164] In some embodiments, the first cavity comprises a first port and the second cavity comprises a second port.

[0165] In some embodiments, the receptacle is in combination with a plug and a printed circuit board, the receptacle being mounted to the printed circuit board and the plug comprising: a first member having a first side and a second, opposing, side; a second member having a third side and a fourth, opposing, side; a fifth plurality of conductive elements, an sixth plurality of conductive elements, a seventh plurality of conductive elements, a eighth plurality of conductive elements, each conductive element of the fifth, sixth, seventh and eighth plurality of conductive elements comprising a tail adapted for attachment to a cable, a mating contact portion and an intermediate portion coupling the tail to the mating contact portion, wherein: the mating contact portions of the fifth plurality of conductive elements are disposed on the first side of the first member; the mating contact portions of the sixth plurality of conductive elements are

disposed on the second side; the mating contact portions of the seventh plurality of conductive elements are disposed on the third side; the mating contact portions of the eighth plurality of conductive elements are disposed along the fourth side; the first member is inserted in the first cavity; the second member is inserted in the second cavity; the second member extends, in a direction perpendicular to the first surface, beyond the first member.

[0166] According to an aspect of the present application, there is provided a plug adapted for engaging a receptacle, the plug comprising: a first sub-assembly comprising: a first insulative housing; a first plurality of conductive elements held by the first insulative housing, each of the first plurality of conductive elements comprising a mating contact portion; a second sub-assembly comprising: a second insulative housing; a second plurality of conductive elements held by the second insulative housing, each of the second plurality of conductive elements comprising a mating contact portion; and a shell having a mating end adapted to engage the receptacle, wherein the first sub-assembly is attached to the shell at a first distance from the mating end and the second sub-assembly is attached to the shell at a second distance, greater than the first distance, from the mating end.

[0167] In some embodiments, the shell comprises a first shell segment and a second shell segment arranged to provide an L-shaped profile; and the first sub-assembly is mounted in the first segment and the second sub-assembly is mounted in the second segment.

[0168] In some embodiments, the mating contact portions of the first plurality of conductive elements are disposed in a first plane; and the mating contact portions of the second plurality of conductive elements are disposed in a second plane, the second plane being parallel to the first plane.

[0169] In some embodiments, the mating contact portion of each of the first plurality of conductive elements comprises a conductive pad exposed in a surface of the first insulative housing; and the mating contact portion of each of the second plurality of conductive elements comprises a conductive pad exposed in a surface of the second insulative housing.

[0170] In some embodiments, the plug is in combination with a receptacle, wherein: the receptacle comprises a housing with a first housing portion and a second housing portion arranged to provide an L-shaped profile, the receptacle comprising a first port adapted to receive the first wafer and a second port adapted to receive the second wafer, the first port being formed in the first housing portion and the second port being formed in the second housing portion.

[0171] According to an aspect of the present application, there is provided a receptacle, the receptacle comprising: a housing comprising: a lower surface adapted for attachment to a printed circuit board; a first port and a second port in a mating face , the first port being offset from the second port in a direction parallel to the lower surface; a first plurality of conductive elements and a second plurality of conductive elements held within the housing, each conductive element of the first and second pluralities comprising a mating contact portion, the mating contact portions of the first plurality of conductive elements being disposed in a first linear array within the first port and the mating contact portions of the second plurality of conductive elements being disposed in a second linear array within the second port.

[0172] In some embodiments, the first port comprises a first cavity; the second port comprises a second cavity; the mating contact portion of each of the first plurality of conductive elements comprises a compliant beam extending into the first cavity; and the mating contact portion of each of the second plurality of conductive elements comprises a compliant beam extending into the second cavity.

[0173] In some embodiments, the first port and the second port are positioned within the housing such that the first cavity and second cavity open in a forward face of the receptacle housing, the forward face having an irregular contour.

[0174] In some embodiments, the receptacle is in combination with a plug, the plug comprising a forward face, the forward face of the plug comprising a contour conforming to the irregular contour of the forward face of the receptacle in one orientation of the plug, whereby the plug is adapted for mating with the receptacle in a single orientation.

[0175] According to an aspect of the present application, there is provided a plug adapted for engaging a receptacle having a plurality of ports, the plug comprising: a shell having a mating end and a cable attachment end; a first planar insulative member and a

second planar insulative member, the second planar insulative member being offset relative to the second planar insulative member from the mating end; a first plurality of conductive elements, each of the first plurality of conductive elements comprising a tail disposed adjacent the cable attachment end and a mating contact portion disposed in a first array though a surface of the first planar insulative member; a second plurality of conductive elements, each of the second plurality of conductive elements comprising a tail disposed adjacent the cable attachment end and a mating contact portion disposed in a second array in a second plane adjacent the mating end.

[0176] In some embodiments, the first planar insulative member and the second planar insulative member are exposed through an opening of the shell.

[0177] In some embodiments, the surface of the first planar insulative member is a first surface of the first planar insulative member and the first planar insulative member comprises a second surface; the surface of the second planar insulative member is a first surface of the second planar insulative member and the second planar insulative member comprises a second surface; the plug further comprises: a third plurality of conductive elements and a fourth plurality of conductive elements, each of the third plurality of conductive elements comprising a tail disposed adjacent the cable attachment end and a mating contact portion disposed in a third array though the second surface of the first planar insulative member, each of the fourth plurality of conductive elements comprising a tail end disposed adjacent the cable attachment end and a mating contact portion disposed in a fourth array though the second surface of the second planar insulative member.

[0178] According to an aspect of the present application, there is provided a connector comprising: a shell; and at least one sub-assembly held within the shell, each of the at least one sub-assemblies comprising: a first housing having a first outer surface and a first inner surface; a first plurality of conductive elements held by the first housing, each of the conductive elements of the first plurality comprising a mating contact portion adjacent a first end of the conductive element and a tail adjacent a second end of the conductive element; a second housing having a second outer surface and a second inner surface; a second plurality of conductive elements held by the second housing, each of the conductive elements of the second plurality comprising a mating contact portion

adjacent a first end of the conductive element and a tail adjacent a second end of the conductive element; and a lossy member disposed between the first housing and the second housing, the planar member comprising an electrically lossy material; wherein the first housing and the second housing are held within the shell with the first inner surface facing the second inner surface.

[0179] In some embodiments, mating contact portions of the conductive elements of the first plurality of conductive elements are exposed in the first outer surface; and mating contact portions of the conductive elements of the second plurality of conductive elements are exposed in the second outer surface.

[0180] In some embodiments, for each conductive element of a first subset of the first plurality of conductive elements, a portion of the conductive element is exposed through the first inner surface; and for each conductive element of a second subset of the second plurality of conductive elements, a portion of the conductive element is exposed through the second inner surface.

[0181] In some embodiments, the lossy member comprises a first surface and a second surface, the first surface being positioned adjacent the first inner surface and the second surface being positioned adjacent the second inner surface; the first surface of the lossy member comprises a first plurality of projections, each projection of the first plurality of projections being coupled to a conductive element of the first subset; and the second surface of the lossy member comprises a second plurality of projections, each projection of the second plurality of projections being coupled to a conductive element of the second subset.

[0182] In some embodiments, the first plurality of conductive elements comprises conductive elements disposed in a plurality of pairs of conductive elements; and the first subset of the first plurality of conductive elements comprises conductive elements each of which is disposed adjacent a pair of the plurality of pairs.

[0183] In some embodiments, conductive elements disposed in the plurality of pairs have a first width; and conductive elements within the first subset of the plurality of conductive elements have a width greater than the first width.

[0184] In some embodiments, the plurality of pairs is a first plurality of pairs; the second plurality of conductive elements comprises conductive elements disposed in a

second plurality of pairs of conductive elements; and the second subset of the second plurality of conductive elements comprises conductive elements each of which is disposed adjacent a pair of the second plurality of pairs.

[0185] In some embodiments, conductive elements disposed in the second plurality of pairs have the first width; and conductive elements within the second subset of the plurality of conductive elements are wider than the first width.

[0186] In some embodiments, the connector further comprises: a fastening mechanism holding the first housing to the second housing.

[0187] In some embodiments, the fastening mechanism comprises a post on the first housing sized to engage an opening within the second housing.

[0188] In some embodiments, the shell comprises a mating end; and the at least one sub-assembly comprises a first sub-assembly and a second assembly, the first sub-assembly and the second sub-assembly being positioned in parallel planes with the first sub-assembly closer to the mating end than the second sub-assembly.

[0189] In some embodiments, the connector further comprises: a first conductive segment interconnecting a plurality of conductive elements in the first subset; and a second conductive segment interconnecting a plurality of conductive elements in the second subset.

[0190] In some embodiments, the first conductive segment is embedded within the first housing adjacent mating contact portions of the conductive elements of the first plurality of conductive elements; and the second conductive segment is embedded within the second housing adjacent mating contact portions of the conductive elements of the second plurality of conductive elements.

[0191] According to an aspect of the present application, there is provided a connector configured as a plug adapted for engaging a receptacle, the plug comprising: a shell; and a plurality of sub-assemblies held within the shell, each of the plurality of sub-assemblies comprising: a first insulative housing having a first outer surface and a first inner surface, the first insulative housing having a plurality of first openings therein; a first plurality of conductive elements held by the first insulative housing, each conductive element of a first subset of the first plurality of conductive elements having a portion positioned in a respective first opening; a second housing having a second outer

surface and a second inner surface, the second insulative housing having a plurality of second openings therein; a second plurality of conductive elements held by the second insulative housing, each conductive element of a second subset of the second plurality of conductive elements having a portion positioned in a respective second opening; and a lossy member disposed between the first housing and the second housing, the lossy member being comprised of an electrically lossy material, and the lossy member comprising: a first plurality of projections, each of the first plurality of projections extending into a respective first opening and being electrically coupled within the first opening to a respective conductive element of the first subset; and a second plurality of projections, each of the second plurality of projections extending into a respective second opening and being electrically coupled within the second opening to a respective conductive element of the second subset.

[0192] In some embodiments, the lossy member comprises a unitary planar member.

[0193] In some embodiments, the plug further comprises: a first conductive segment interconnecting a plurality of conductive elements in the first subset, the first conductive segment being embedded in the first housing; and a second conductive segment interconnecting a plurality of conductive elements in the second subset, the second conductive segment being embedded in the second housing.

[0194] According to an aspect of the present application, there is provided a method of manufacturing a plug, the method comprising: attaching each of a first plurality of conductors of a cable to a respective cable attachment end of a conductive element held in a first insulative housing; attaching each of a second plurality of conductors of a cable to a respective cable attachment end of a conductive element held in a second insulative housing; placing a lossy member between the first housing and the second housing; securing the first housing to the second housing to form a sub-assembly; and inserting the sub-assembly into a shell.

[0195] In some embodiments, the method further comprises: molding the first insulative housing over a first lead frame, the first lead frame being comprised of the first plurality of conductive elements; wherein: the first lead frame comprises a first conductive segment interconnecting a first subset of the first plurality of conductive

elements; and the molding the first insulative housing comprises encasing the first conductive segment within the first insulative housing.

[0196] In some embodiments, the method further comprises: molding the second insulative housing over a second lead frame, the second lead frame being comprised of the second plurality of conductive elements, wherein: the second lead frame comprises a second conductive segment interconnecting a second subset of the second plurality of conductive elements; and the molding the second insulative housing comprises encasing the second conductive segment within the second insulative housing.

[0197] According to an aspect of the present application, there is provided a plug adapted for engaging a receptacle, the plug comprising: a shell having an opening therein; and a plurality of sub-assemblies held within the shell, each of the plurality of sub-assemblies comprising: an insulative housing; a plurality of conductive elements held by the housing, each conductive element of the plurality of conductive elements comprising an exposed mating contact portion adjacent a first end of the conductive element; and a conductive segment interconnecting first ends of a first subset of conductive elements of the plurality of conductive elements, the first conductive segment being embedded within the insulative housing adjacent mating contact portions of the conductive elements of the first plurality of conductive elements.

[0198] In some embodiments, the plurality of conductive elements is comprised of a second subset of conductive elements, the conductive elements in the second sub-set being disposed in a plurality of pairs with a conductive element in the first subset being between adjacent pairs of the plurality of pairs.

[0199] In some embodiments, the conductive elements in the second subset are of equal width and at least one of the conductive elements in the first subset is wider than conductive elements in the second subset.

[0200] In some embodiments, the second subset consists of a first pair and a second pair and a conductive element of the first subset of conductive elements disposed between the first pair and the second pair is wider than the conductive elements of the second subset.

[0201] In some embodiments, the plurality of conductive elements are disposed in a column, with a conductive element of the first subset disposed on each end of the

column being narrower than the conductive element between the first pair and the second pair.

[0202] According to an aspect of the present application, there is provided a plug, in combination with a cable bundle, wherein: the shell comprises a first portion and a second portion; the cable comprises an interior portion, an outer jacket and a conductive braid between the interior and the outer jacket; the combination comprises a ferrule between the braid and the interior portion adjacent an end of the cable; and the first portion and the second portion of the shell are held together such that the outer jacket is secured between the shell and the ferrule.

[0203] In some embodiments, a portion of the braid extends beyond the outer jacket at the end of the cable and folds over the outer jacket such that the portion of the braid is secured between the shell and the ferrule.

[0204] In some embodiments, the shell is comprised of a conductive material and the shell is electrically connected to the braid.

[0205] In some embodiments, the shell comprises a plurality of projections, each of the projections deforming the braid and outer jacket.

[0206] In some embodiments, the plurality of projections are offset with respect to each other along an axis of the cable.

[0207] In some embodiments, the ferrule comprises two pieces.

[0208] According to an aspect of the present application, there is provided a plug adapted for engaging a receptacle, the plug comprising: a shell; and at least one sub-assembly held within the shell, each of the at least one sub-assemblies comprising: a first housing; a first plurality of conductive elements held by the first housing, each of the conductive elements of the first plurality comprising a mating contact portion adjacent a first end of the conductive element and a cable attachment portion adjacent a second end of the conductive element; a second housing; a second plurality of conductive elements held by the second housing, each of the conductive elements of the second plurality comprising a mating contact portion adjacent a first end of the conductive element and a cable attachment portion adjacent a second end of the conductive element; a first conductive segment interconnecting a plurality of conductive elements of the first plurality of conductive elements, the first conductive segment is embedded within the

first housing adjacent mating contact portions of the conductive elements of the first plurality of conductive elements; and a second conductive segment interconnecting a plurality of conductive elements of the second plurality of conductive elements, the second conductive segment is embedded within the second housing adjacent mating contact portions of the conductive elements of the second plurality of conductive elements.

[0209] In some embodiments, the first housing has a first outer surface and a first inner surface; mating contact portions of conductive elements of the first plurality of conductive elements are exposed in the first outer surface; the second housing has a second outer surface and a second inner surface; mating contact portions of conductive elements of the second plurality of conductive elements are exposed in the second outer surface; and the first housing and the second housing are held within the shell with the first inner surface facing the second inner surface.

[0210] In some embodiments, the plug further comprises a lossy member between the first housing and the second housing.

[0211] In some embodiments, the sub-assembly comprises a forward mating edge; the first conductive segment is embedded in the first housing along the forward mating edge; the second conductive segment is embedded in the second housing along the forward mating edge.

[0212] According to an aspect of the present application, there is provided a plug, in combination with a cable bundle, wherein: the shell comprises a first portion and a second portion; the cable comprises an interior portion, an outer jacket and a conductive braid between the interior portion and the outer jacket, and a plurality of conductors, each of the conductors being attached to a cable attachment portion of a conductive element of the first plurality of conductive elements or the second plurality of conductive elements; the combination comprises a ferrule between the braid and the interior portion adjacent an end of the cable bundle; and the first portion and the second portion of the shell are held together, whereby the outer jacket is secured in the shell by a force between the shell and the ferrule.

[0213] In some embodiments, the shell comprises a plurality of projections adjacent the end of the cable, each of the projections deforming the braid and outer jacket.

[0214] In some embodiments, the ferrule comprises a plurality of segments that form a tubular ferrule.

[0215] According to an aspect of the present application, there is provided a sub-assembly adapted for use in a plug, the sub-assembly comprising: a housing having a first outer surface and a second outer surface; a first plurality of conductive elements held by the housing, each of the conductive elements of the first plurality comprising a mating contact portion adjacent a first end of the conductive element and a cable attachment portion adjacent a second end of the conductive element, the mating contact portion being exposed in the first outer surface; a second plurality of conductive elements held by the housing, each of the conductive elements of the second plurality comprising a mating contact portion adjacent a first end of the conductive element and a cable attachment portion adjacent a second end of the conductive element, the mating contact portion being exposed in the second outer surface; a first conductive segment interconnecting the first ends of a plurality of conductive elements of the first plurality of conductive elements, the first conductive segment being embedded within the first housing; and a second conductive segment interconnecting the first ends of a plurality of conductive elements of the second plurality of conductive elements, the second conductive segment being embedded within the second housing.

[0216] In some embodiments, the first plurality of conductive elements is disposed in a repeating pattern of a conductive element interconnected with the first conductive segment and a pair of conductive elements separate from the first conductive segment; and the second plurality of conductive elements is disposed in a repeating pattern of a conductive element interconnected with the second conductive segment and a pair of conductive elements separate from the second conductive segment.

[0217] Accordingly, the invention should be limited only by the attached claims.

What is claimed is:

CLAIMS

1. A receptacle adapted for mounting to a printed circuit board, comprising:

a housing having a cavity bounded by a first surface and an opposing second surface;

a first lead assembly including a first plurality of conductive elements disposed in a first housing member;

a second lead assembly including a second plurality of conductive elements disposed in a second housing member, each conductive element of the first and second pluralities of conductive elements comprising a contact tail adapted for attachment to the printed circuit board, a mating contact portion and an intermediate portion coupling the contact tail to the mating contact portion, wherein the mating contact portions of the first plurality of conductive elements are disposed along the first surface of the cavity and the mating contact portions of the second plurality of conductive elements are disposed along the second surface of the cavity; and

an insert disposed between the first and second lead assemblies.

2. The receptacle as defined in claim 1, wherein the insert includes an electrically lossy material.

3. The receptacle as defined in claim 1, wherein the insert contacts selected ones of the conductive elements.

4. The receptacle as defined in claim 1, wherein the insert includes projections towards selected ones of the conductive elements.

5. The receptacle as defined in claim 4, wherein at least one of the first and second housing members includes one or more slots for receiving the projections of the insert.

6. The receptacle as defined in claim 1, wherein the contact tails and the mating contact portions are disposed at right angles.

7. The receptacle as defined in claim 1, wherein the first plurality of conductive elements and the second plurality of conductive elements form rows of contacts on the first and second surfaces, respectively, of the cavity.

8. The receptacle as defined in claim 1, wherein the first and second surfaces of the cavity include slots configured to receive the conductive elements of the first plurality of conductive elements and the second plurality of conductive elements, respectively.

9. The receptacle as defined in claim 1, wherein the first and second surfaces of the cavity are parallel.

10. The receptacle as defined in claim 1, wherein the first plurality of conductive elements is molded in the first housing member, and the second plurality of conductive elements is molded in the second housing member.

11. The receptacle as defined in claim 1, wherein the housing, the first housing member and the second housing member are made of an insulative material.

12. The receptacle as defined in claim 1, wherein the housing includes at least one projection from a lower surface thereof.

13. The receptacle as defined in claim 1, further comprising a shell adapted for attachment of the housing to the printed circuit board.

14. The receptacle as defined in claim 1, wherein the housing further comprises a second cavity bounded by a third surface and an opposing fourth surface, further comprising a third lead assembly including a third plurality of conductive elements disposed in a third housing member and a fourth lead assembly including a fourth plurality of conductive elements disposed in a fourth housing member, each conductive element of the third and fourth pluralities of conductive elements comprising a contact tail adapted for attachment to the printed circuit board, a mating contact portion and an

intermediate portion coupling the contact tail to the mating contact portion, wherein the mating contact portions of the third plurality of conductive elements are disposed along the third surface of the second cavity and the mating contact portions of the fourth plurality of conductive elements are disposed along the fourth surface of the second cavity.

15. The receptacle of claim 1, wherein:

for each conductive element of a first subset of the first plurality of conductive elements, a portion of the conductive element is exposed through the first housing member, and

for each conductive element of a second subset of the second plurality of conductive elements, a portion of the conductive element is exposed through the second housing member.

16. The receptacle of claim 15, wherein:

a first surface of the insert comprises a first plurality of projections, each projection of the first plurality of projections being coupled to a conductive element of the first subset; and

a second surface of the insert comprises a second plurality of projections, each projection of the second plurality of projections being coupled to a conductive element of the second subset.

17. The receptacle of claim 16, wherein:

the first plurality of conductive elements comprises conductive elements disposed in a plurality of pairs of conductive elements; and

the first subset of the first plurality of conductive elements comprises conductive elements each of which is disposed adjacent a pair of the plurality of pairs.

18. The receptacle of claim 1, wherein the insert includes a conductive material.

19. The receptacle of claim 1, wherein the insert is at least partially conductive.

20. The receptacle as defined in claim 1, wherein:

the insert includes an electrically lossy material; and

the electrically lossy material is electrically coupled to selected ones of the first plurality of conductive elements and the second plurality of conductive elements.

21. The receptacle as defined in claim 20, wherein:

the first plurality of conductive elements are positioned in a first row, the first row comprising pairs of the first plurality of conductive elements separated by single conductive elements of the first plurality of conductive elements;

the second plurality of conductive elements are positioned in a second row, the second row comprising pairs of the second plurality of conductive elements separated by single conductive elements of the second plurality of conductive elements; and

the electrically lossy material is selectively electrically coupled to the single conductive elements of the first plurality of conductive elements and second plurality of conductive elements.

22. The receptacle as defined in claim 21, wherein:

the insert includes projections towards the selected ones of the conductive elements.

ABSTRACT

A cable connector with improved performance and ease of use. The connector has staggered ports to reduce crosstalk and to prevent incorrect insertion of a plug into a receptacle. The plug may be constructed with subassemblies, each of which has a lossy central portion. Conductive members embedded within an insulative housing of the subassemblies may be used to electrically connect ground conductors within the subassemblies. Further, the connector may have a quick connect locking screw that can be engaged by pressing on the screw, but requires rotation of the screw to remove. Additionally, a ferrule may be used in making a mechanical connection between a cable bundle and a plug and making an electrical connection between a braid of the cable bundle and a conductive shell of the plug. The ferrule may be in multiple pieces for easy attachment while precluding deformation of the cable, which disrupts electrical performance.

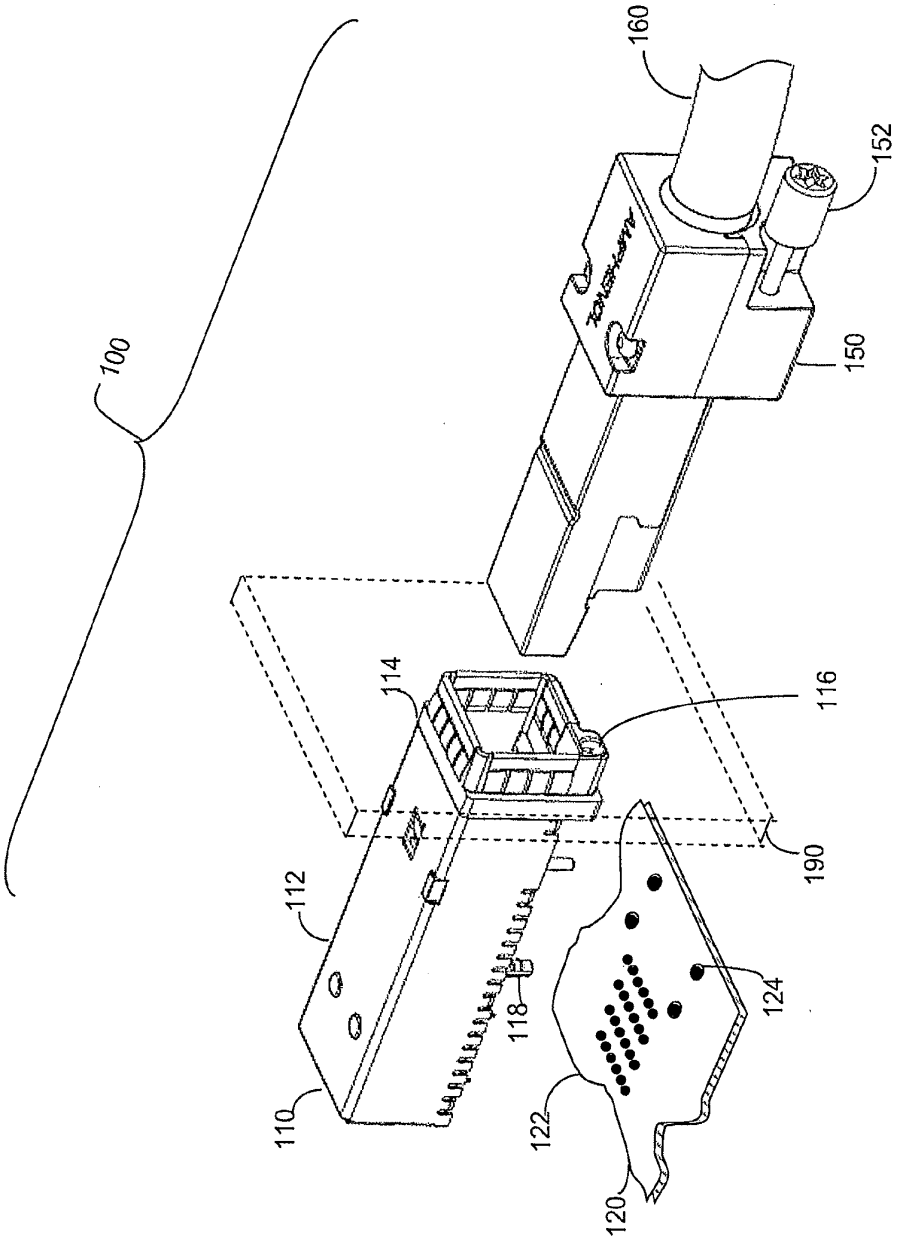

FIG. 1

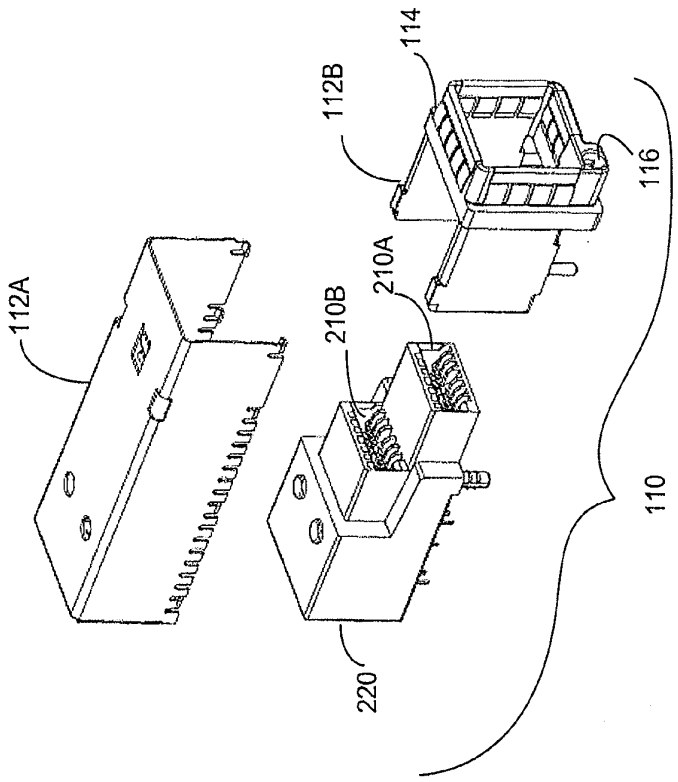

FIG. 2

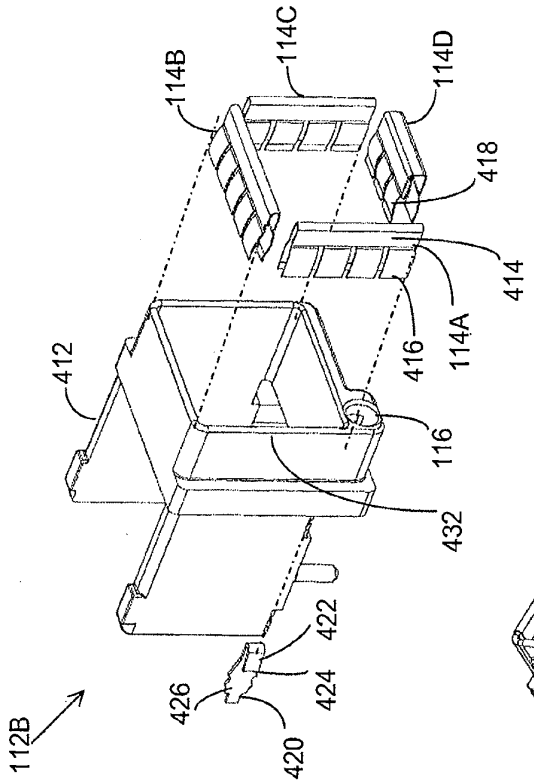
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FIG. 4

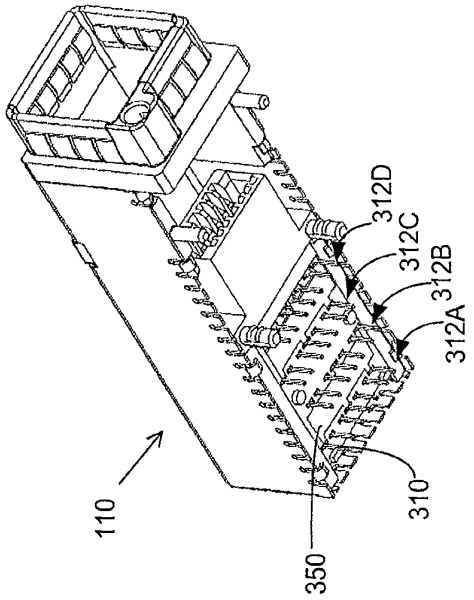
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FIG. 3

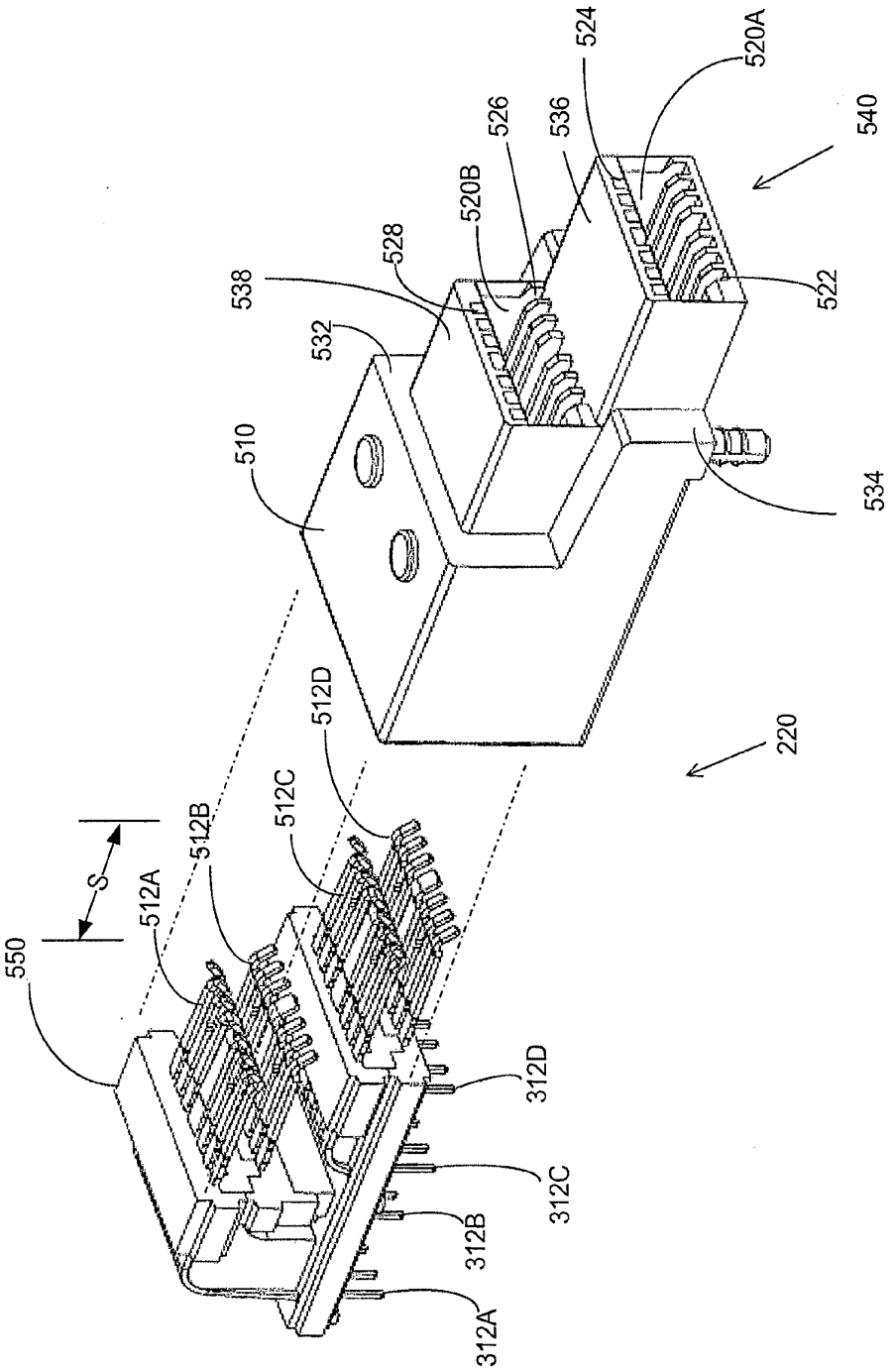
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FIG. 5

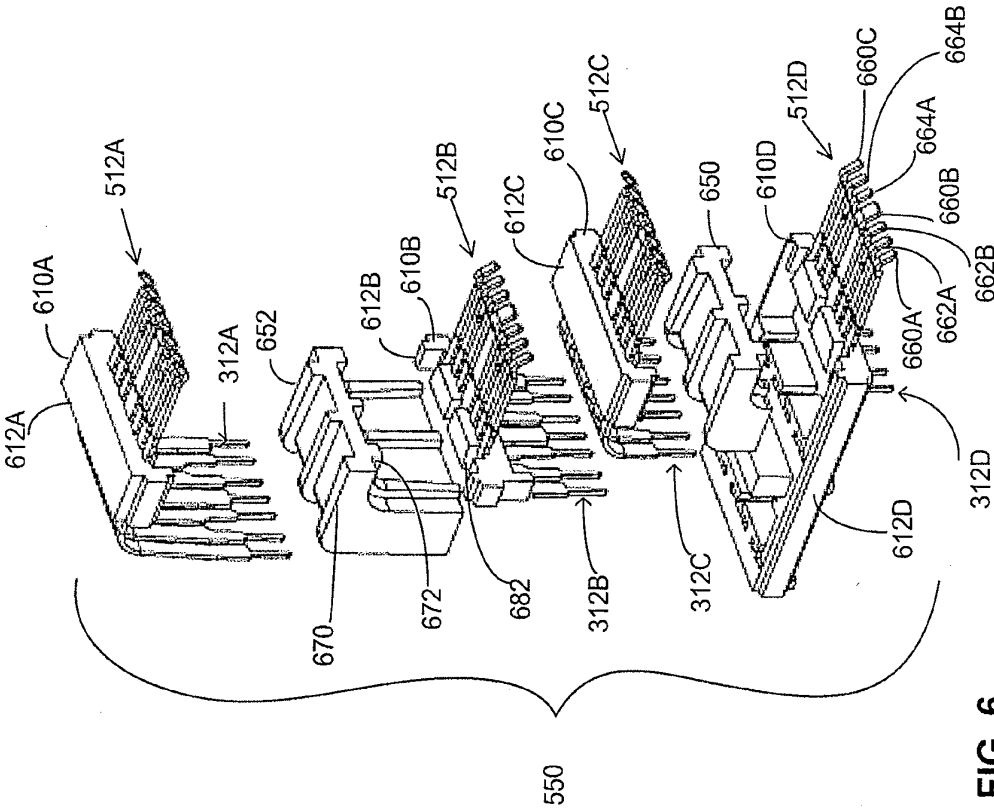
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FIG. 6

FIG. 7A

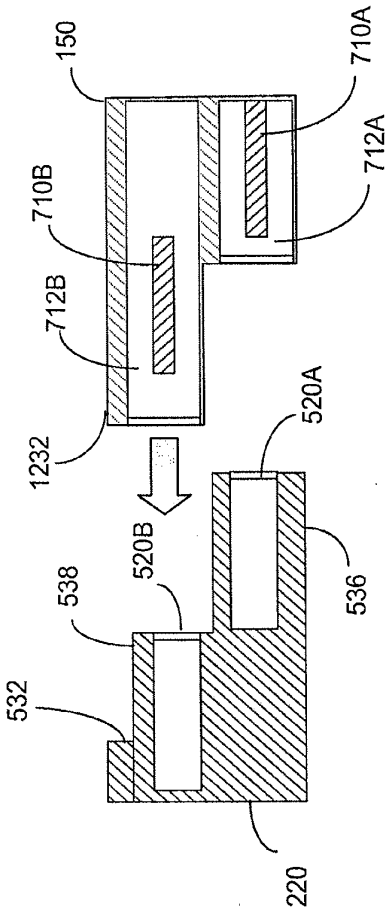
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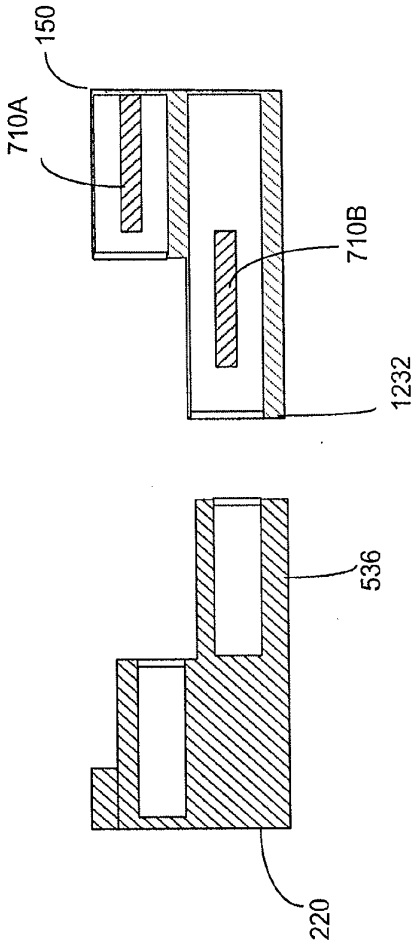
FIG. 7B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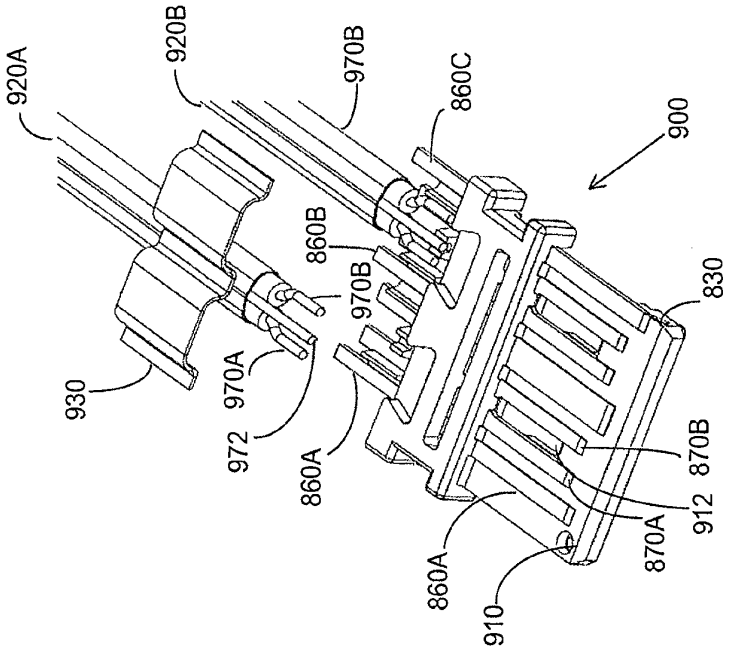
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FIG. 9

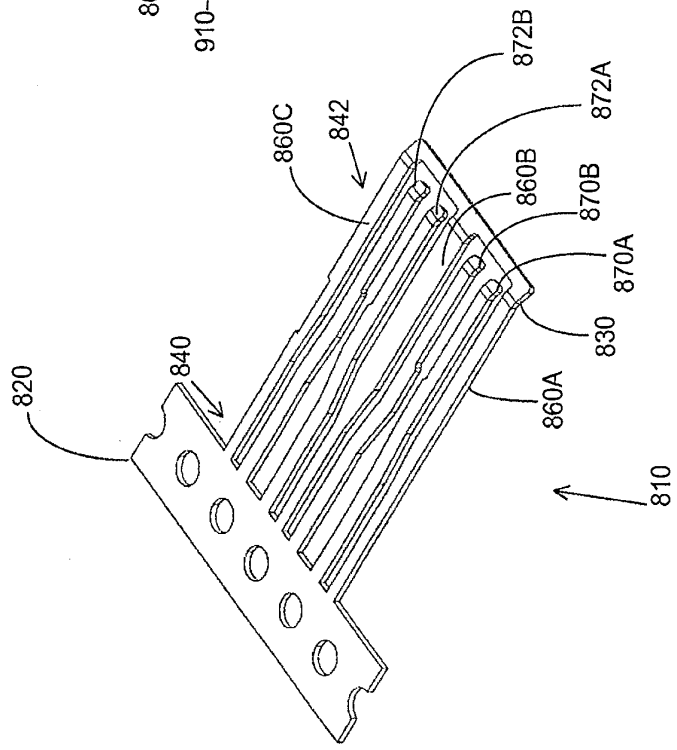
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FIG. 8

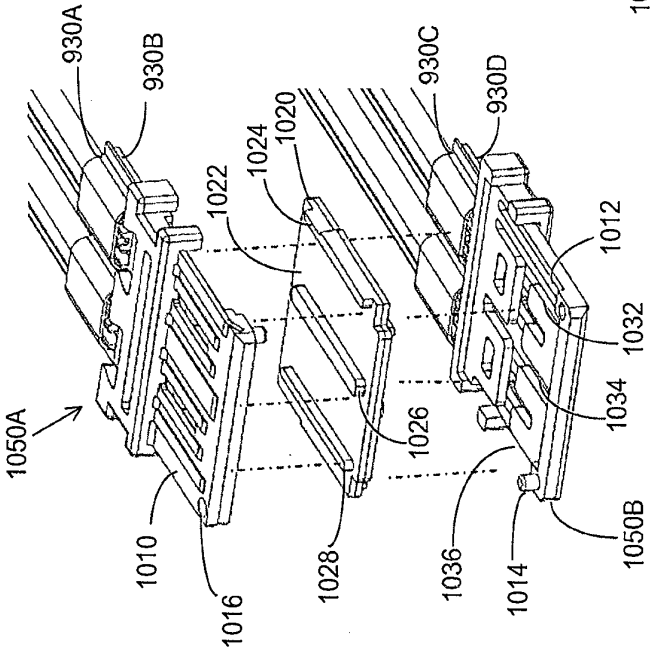
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FIG. 10

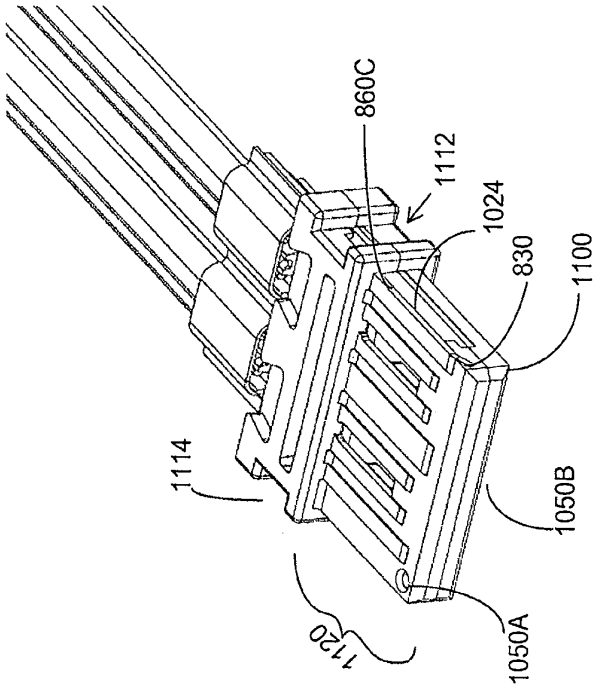
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FIG. 11

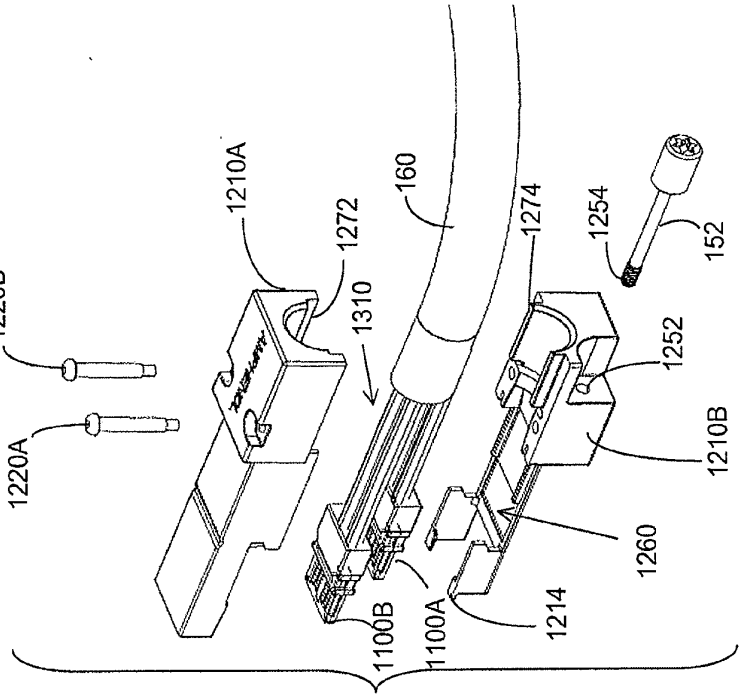

FIG.12B

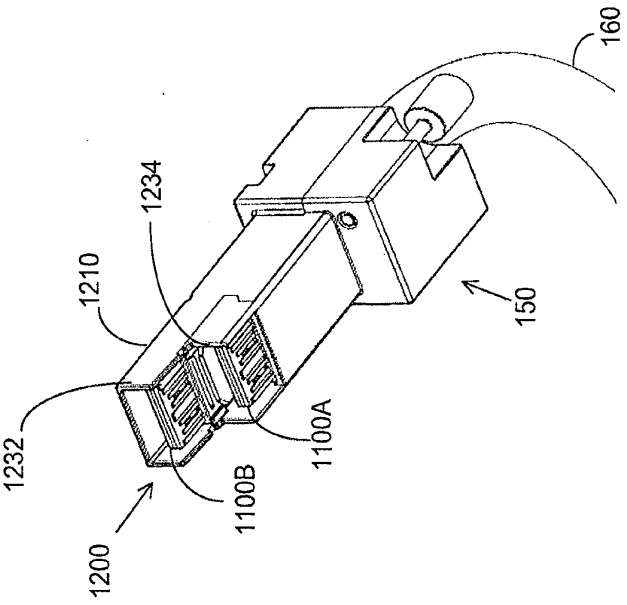

FIG. 12A

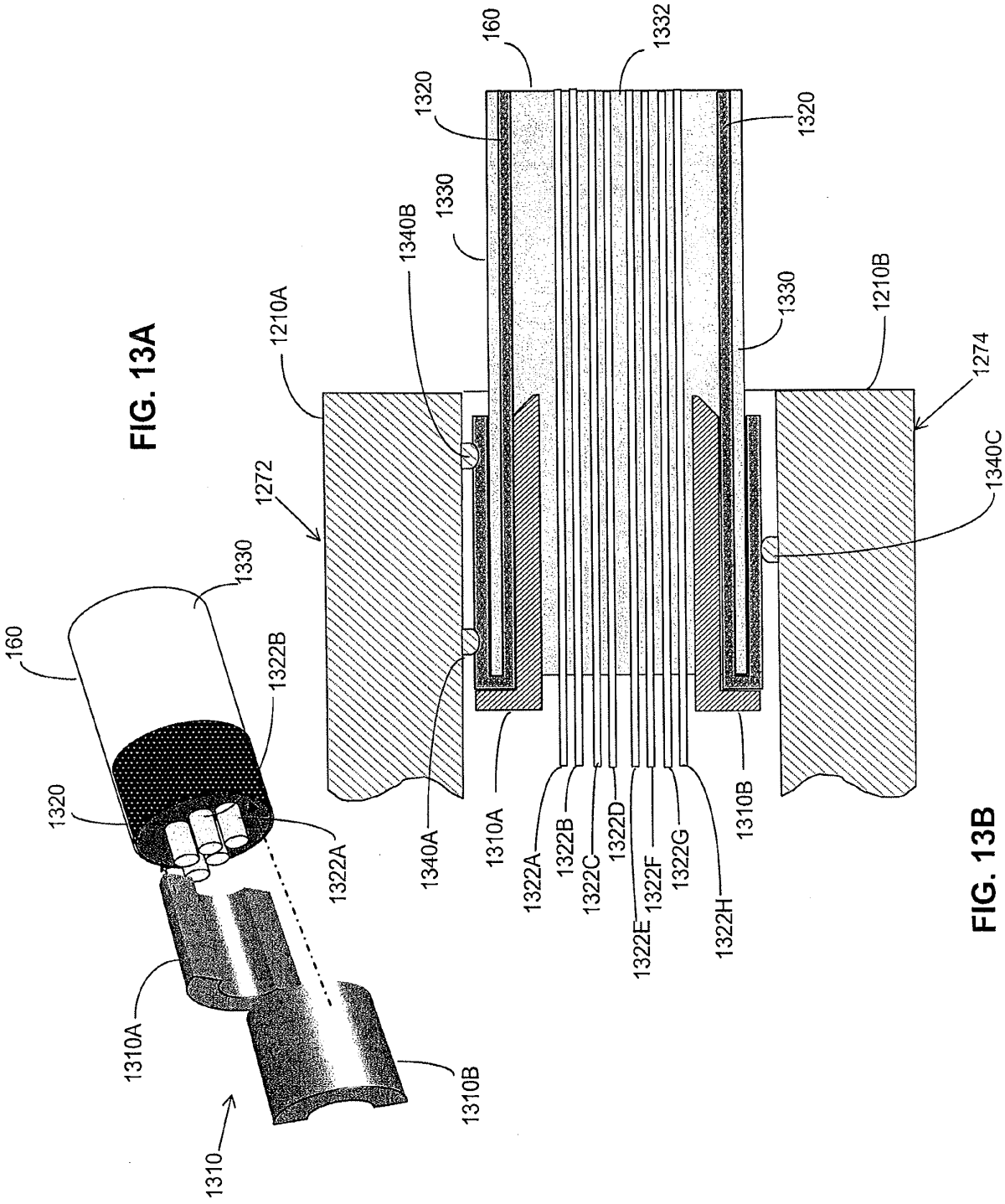

FIG. 13A

FIG. 13B

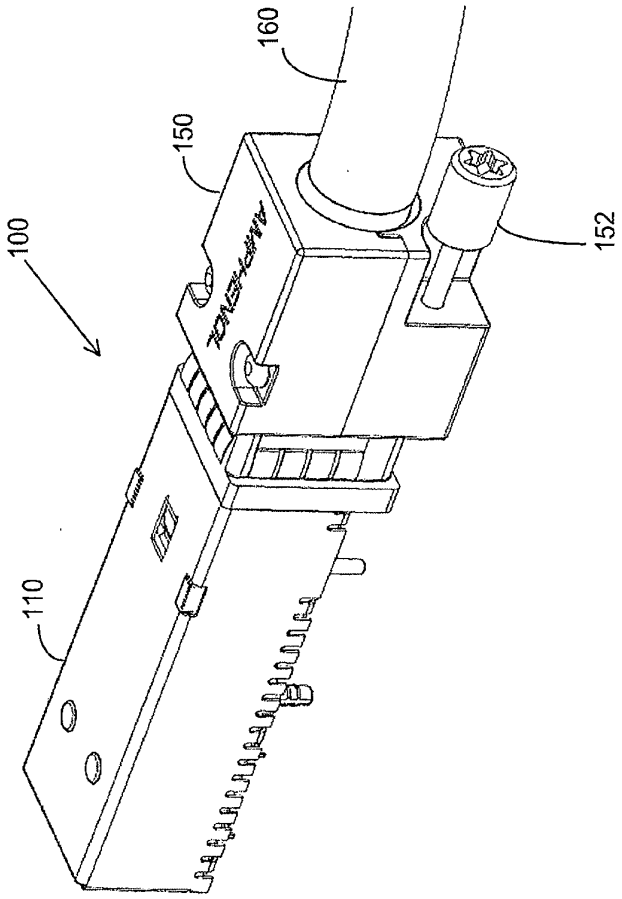

FIG. 14

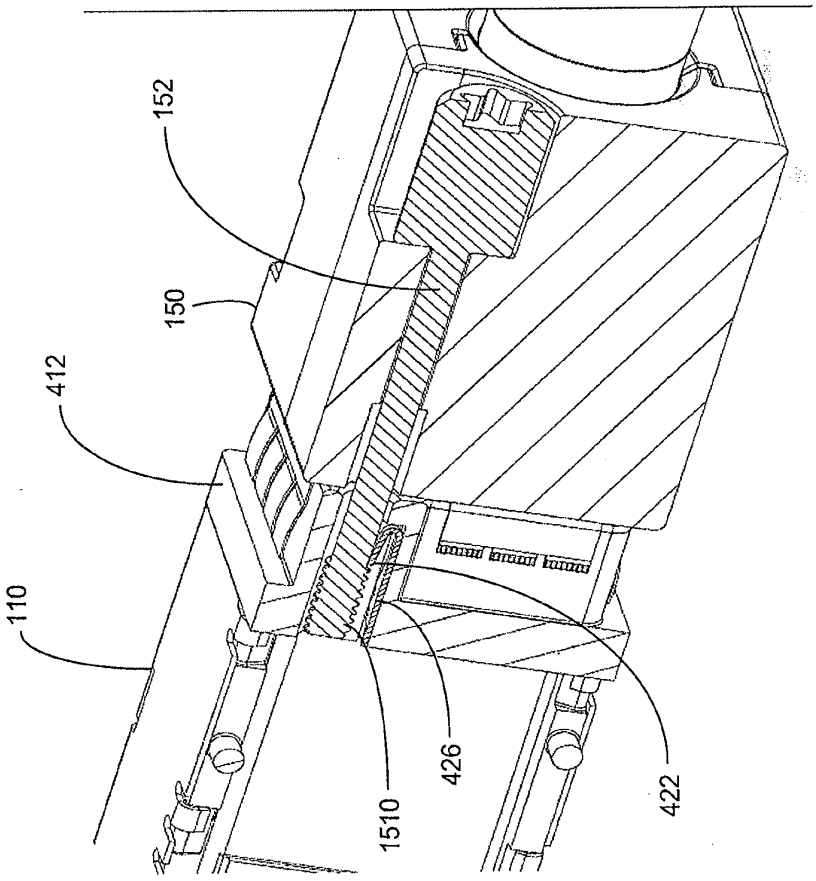

FIG. 15

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	HIGH PERFORMANCE CABLE CONNECTOR
First Named Inventor/Applicant Name:	Donald W. Milbrand, Jr.
Filer:	William R. McClellan/Eileen MacKenzie
Attorney Docket Number:	A0863.70051US04

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Utility application filing	1011	1	280	280
Utility Search Fee	1111	1	600	600
Utility Examination Fee	1311	1	720	720
Pages:				
Claims:				
Claims in Excess of 20	1202	2	80	160
Miscellaneous-Filing:				
Petition:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	1760

Electronic Acknowledgement Receipt	
EFS ID:	25153300
Application Number:	15065683
International Application Number:	
Confirmation Number:	5112
Title of Invention:	HIGH PERFORMANCE CABLE CONNECTOR
First Named Inventor/Applicant Name:	Donald W. Milbrand, Jr.
Customer Number:	23628
Filer:	William R. McClellan/Eileen MacKenzie
Filer Authorized By:	William R. McClellan
Attorney Docket Number:	A0863.70051US04
Receipt Date:	09-MAR-2016
Filing Date:	
Time Stamp:	19:03:14
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$1760
RAM confirmation Number	5619
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal of New Application	A086370051US04-TRN-WRM.PDF	72223 6ad5fec068645e626328effb516f006bd8aef23e	no	1
Warnings:					
Information:					
2	Fee Worksheet (SB06)	A086370051US04-FEE-WRM.PDF	77923 d1ba02830723c577717437445O3bbbe538e62c04	no	1
Warnings:					
Information:					
3	Nonpublication request from applicant	A086370051US04-NONPUB-WRM.PDF	52939 fd68f7de028ed93484d9d483d3ac5015cca19011	no	1
Warnings:					
Information:					
4	Application Data Sheet	A086370051US04-ADS-WRM.PDF	195073 1138f7aaf26dd8ff0ba1bce925b90e527e0f5ba6	no	7
Warnings:					
Information:					
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5	Oath or Declaration filed	A086370051US04-INVDEC-WRM.PDF	53527 cf30dcc46c45a169c3caa05e7bd684b7b195cd4d	no	1
Warnings:					
Information:					
6		A086370051US04-UTLAPL-WRM.pdf	162908 e74ed4001d3427efbeaeb8e88510db17741ffc78	yes	51

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Specification	1	46
	Claims	47	50

	Abstract		51	51	
Warnings:					
Information:					
7	Drawings-other than black and white line drawings	A086370051US04-DRW-WRM.PDF	349804 dee85c6e3f443787068a489db104454e9ab0bd8a	no	12
Warnings:					
Information:					
8	Fee Worksheet (SB06)	fee-info.pdf	37135 fd136ef021f7f75772c3834467c670699217c204	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	1001532		

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

DocCode – SCORE

SCORE Placeholder Sheet for IFW Content

Application Number: 15065683 Document Date: 03/09/2016

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Form Revision Date: August 26, 2013

FORM PTO-1449/A and B (modified PTO/SB/08)				APPLICATION NO.: 15/065,683	ATTY. DOCKET NO.: A0863.70051US04
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				FILING DATE: March 9, 2016	CONFIRMATION NO.: 5112
				FIRST NAMED INVENTOR: Donald W. Milbrand, Jr.	
Sheet	1	of	7	GROUP ART UNIT: 2833	EXAMINER: Not Yet Assigned

U.S. PATENT DOCUMENTS

Examiner's Initials #	Cite No.	U.S. Patent Document Number	U.S. Patent Document Kind Code	Name of Patentee or Applicant of Cited Document	Date of Publication or Issue of Cited Document MM-DD-YYYY
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				FIRST NAMED INVENTOR: Donald W. Milbrand, Jr.	
Sheet	2	of	7	GROUP ART UNIT: 2833	EXAMINER: Not Yet Assigned

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT				FILING DATE: March 9, 2016	CONFIRMATION NO.: 5112
				FIRST NAMED INVENTOR: Donald W. Milbrand, Jr.	
Sheet	3	of	7	GROUP ART UNIT: 2833	EXAMINER: Not Yet Assigned

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Sheet	4	of	7	GROUP ART UNIT: 2833	EXAMINER: Not Yet Assigned

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Sheet	5	of	7	GROUP ART UNIT: 2833	EXAMINER: Not Yet Assigned

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Sheet	6	of	7	GROUP ART UNIT: 2833	EXAMINER: Not Yet Assigned

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		2015-0056856	A1	Atkinson et al.	02-26-2015
		2015-0236451	A1	Cartier, Jr. et al.	08-20-2015
		2015-0236452	A1	Cartier, Jr. et al.	08-20-2015
		2015-0255926	A1	Paniagua	09-10-2015

FOREIGN PATENT DOCUMENTS

Examiner's Initials #	Cite No.	Foreign Patent Document			Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Translation (Y/N)
		Office/ Country	Number	Kind Code			
	*	EP	1 779 472	A1	Amphenol Corp.	05-02-2007	
	*	EP	2 169 770	A2	Amphenol Corporation	03-31-2010	
	*	GB	1272347	A	Amp Inc.	04-26-1972	
	*	JP	07302649	A	Framatome Connectors Int	11-14-1995	Y – Abstract Only
	*	WO	88/05218	A1	Amp Inc.	07-14-1988	
	*	WO	2004/059794	A2	Teradyne, Inc.	07-15-2004	
	*	WO	2004/059801	A1	Teradyne, Inc.	07-15-2004	
	*	WO	2006/039277	A1	Teradyne, Inc.	04-13-2006	
	*	WO	2007/005597	A2	Amphenol Corporation	01-11-2007	
	*	WO	2007/005599	A1	Amphenol Corporation	01-11-2007	
	*	WO	2008/124057	A1	Amphenol Corporation	10-16-2008	
	*	WO	2010/039188	A1	Amphenol Corporation	04-08-2010	

EXAMINER:	DATE CONSIDERED:

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

*a copy of this reference is not provided as it was previously cited by or submitted to the office in a prior application, Serial No. 13/683,295, filed November 21, 2012, and relied upon for an earlier filing date under 35 U.S.C. 120 (continuation, continuation-in-part, and divisional applications).

FORM PTO-1449/A and B (modified PTO/SB/08)				APPLICATION NO.: 15/065,683	ATTY. DOCKET NO.: A0863.70051US04
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				FILING DATE: March 9, 2016	CONFIRMATION NO.: 5112
				FIRST NAMED INVENTOR: Donald W. Milbrand, Jr.	
Sheet	7	of	7	GROUP ART UNIT: 2833	EXAMINER: Not Yet Assigned

OTHER ART – NON PATENT LITERATURE DOCUMENTS

Examiner's Initials #	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	Translation (Y/N)
	*	Extended European Search Report mailed January 24, 2012 for Application No. EP 11166820.8.	
	*	International Search Report and Written Opinion mailed January 26, 2006 for Application No. PCT/US2005/034605.	
	*	International Search Report with Written Opinion mailed October 31, 2007 for Application No. PCT/US2006/025562.	
	*	International Search Report and Written Opinion mailed March 14, 2011 for Application No. PCT/US2010/056482 (A0863.70049WO00).	
	*	International Preliminary Report on Patentability mailed May 24, 2012 for Application No. PCT/US2010/056482 (A0863.70049WO00).	
	*	International Search Report and Written Opinion mailed November 22, 2011 for Application No. PCT/US2011/026139 (A0863.70055WO00).	
	*	International Preliminary Report on Patentability mailed September 7, 2012 for Application No. PCT/US2011/026139 (A0863.70055WO00).	
	*	International Search Report and Written Opinion mailed July 28, 2011 for Application No. PCT/US2011/034747 .	
	*	International Search Report and Written Opinion mailed September 12, 2012 for Application No. PCT/US2012/023689 (A0863.70061WO00).	
	*	International Preliminary Report on Patentability mailed August 15, 2013 for Application No. PCT/US2012/023689 (A0863.70061WO00).	
	*	International Search Report and Written Opinion mailed March 29, 2013 for Application No. PCT/US2012/060610 (A0863.70066WO00).	
		International Search Report and Written Opinion mailed May 13, 2015 for Application No. PCT/US2015/012463 (A0863.70078WO00).	
	*	[NO AUTHOR LISTED], Carbon Nanotubes For Electromagnetic Interference Shielding. SBIR/STTR. Award Information. Program Year 2001. Fiscal Year 2001. Materials Research Institute, LLC. Chu et al. Available at http://sbir.gov/sbirsearch/detail/225895. Last accessed 9/19/13.	
	*	BEAMAN, High Performance Mainframe Computer Cables. 1997 Electronic Components and Technology Conference. 1997;911-7.	
	*	SHI et al, Improving Signal Integrity In Circuit Boards By Incorporating Absorbing Materials. 2001 Proceedings. 51st Electronic Components and Technology Conference, Orlando FL. 2001:1451-56.	

[NOTE – No copies of U.S. patents, published U.S. patent applications, or pending, unpublished patent applications stored in the USPTO's Image File Wrapper (IFW) system, are included. See 37 CFR § 1.98 and 1287OG163. Copies of all other patent(s), publication(s), unpublished, pending U.S. patent applications, or other information listed are provided as required by 37 CFR § 1.98 unless 1) such copies were provided in an IDS in an earlier application that complies with 37 CFR § 1.98, and 2) the earlier application is relied upon for an earlier filing date under 35 U.S.C. § 120.]

EXAMINER:	DATE CONSIDERED:

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

*a copy of this reference is not provided as it was previously cited by or submitted to the office in a prior application, Serial No. 13/683,295, filed November 21, 2012, and relied upon for an earlier filing date under 35 U.S.C. 120 (continuation, continuation-in-part, and divisional applications).

1 FD

PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

To:
CHEUNG HUGHES, LING

WOLF, GREENFIELD & SACKS, P.C. 600 ATLANTIC AVENUE BOSTON MA 02210-2206 US

PCT

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL SEARCH REPORT AND THE WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY, OR THE DECLARATION

(PCT Rule 44.1)

Applicant's or agent's file reference A0863.70078	Date of mailing *(day/month/year)* 13 May 2015 (13.05.2015) **FOR FURTHER ACTION** See paragraphs 1 and 4 below
International application No. **PCT/US2015/012463**	International filing date *(day/month/year)* **22 January 2015 (22.01.2015)**

Applicant
AMPHENOL CORPORATION

1. ☒ The applicant is hereby notified that the international search report and the written opinion of the International Searching Authority have been established and are transmitted herewith.

Filing of amendments and statement under Article 19:

The applicant is entitled, if he so wishes, to amend the claims of the international application (see Rule 46):

When? The time limit for filing such amendments is normally two months from the date of transmittal of the international search report.

How? Directly to the International Bureau of WIPO preferably through ePCT or on paper to, 34 chemin des Colombettes 1211 Geneva 20, Switzerland, Facsimile No.: 141 22 338 82 70

For more detailed instructions, see *PCT Applicant's Guide*, International Phase, paragraphs 9.004 . 9-011.

2. ☐ The applicant is hereby notified that no international search report will be established and that the declaration under Article 17(2)(a) to that effect and the written opinion of the International Searching Authority are transmitted herewith.

3. ☐ **With regard to any protest** against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:

☐ the protest together with the decision thereon has been transmitted to the International Bureau together with any request to forward the texts of both the protest and the decision thereon to the designated Offices.

☐ no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.

4. **Reminders**

The applicant may submit comments on an informal basis on the written opinion of the International Searching Authority to the International Bureau. The International Bureau will send a copy of such comments to all designated Offices unless an international preliminary examination report has been or is to be established. Following the expiration of 30 months from the priority date, these comments will also be made available to the public.

Shortly after the expiration of **18 months** from the priority date, the international application will be published by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau before the completion of the technical preparations for international publication (Rules 90*bis*.1 and 90*bis*.3).

Within **19 months** from the priority date, but only in respect of some designated Offices, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase **until 30 months** from the priority date (in some Offices even later); otherwise, the applicant must, **within 20 months** from the priority date, perform the prescribed acts for entry into the national phase before those designated Offices. In respect of other designated Offices, the time limit of **30 months** (or later) will apply even if no demand is filed within 19 months. For details about the applicable time limits, Office by Office, see www.wipo.int/pct/en/texts/time_limits.html and the *PCT Applicant's Guide*, National Chapters.

Within **19 months** from the priority date, the applicant may request that a supplementary international search be carried out by an International Searching Authority, that offers this service (Rule 45*bis*.1). The procedure for requesting supplementary international search is described in the *PCT Applicant's Guide*, International Phase, paragraphs 8.006-8.032.

Name and mailing address of the ISA/KR International Application Division Korean Intellectual Property Office 189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City, 302-701, Republic of Korea Facsimile No. +82 42 472 7140	Authorized officer COMMISSIONER Telephone No. 82-42-481-8751

Form PCT/ISA/220 (July 2014)

* Attention

Copies of the documents cited in the international search report can be searched in the following Korean Intellectual Property Office English website for six months(expire date : **2015.11.13**) from the date of mailing of the international search report.

http://www.kipo.go.kr/en/ => PCT Services => PCT Services

ID : PCT international application number
PW : **VY92UVAD**

Inquiries related to PCT International Search Report or Written Opinion prepared by KIPO as an International Searching Authority can be answered not only by KIPO but also through IPKC (Intellectual Property Korea Center), located in Vienna, VA, which functions as a PCT Help Desk for PCT applicants.

Homepage: http://www.ipkcenter.com

Email: ipkc@ipkcenter.com

Notes to Form PCT/ISA/220 (July 2014)

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference A0863.70078	FOR FURTHER ACTION	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
International application No. **PCT/US2015/012463**	International filing date *(day/month/year)* **22 January 2015 (22.01.2015)**	(Earliest) Priority Date *(day/month/year)* 22 January 2014 (22.01.2014)
Applicant **AMPHENOL CORPORATION**		

This International search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 4 sheets.

☐ It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**
   a. With regard to the **language**, the international search was carried out on the basis of :
      ☒ the international application in the language in which it was filed
      ☐ a translation of the international application into _____ , which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))
   b. ☐ This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6*bis*(a)).
   c. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.
2. ☐ **Certain claims were found unsearchable** (See Box No. II)
3. ☐ **Unity of invention is lacking** (See Box No. III)
4. With regard to the **title,**
   ☒ the text is approved as submitted by the applicant.
   ☐ the text has been established by this Authority to read as follows:
5. With regard to the **abstract,**
   ☒ the text is approved as submitted by the applicant.
   ☐ the text has been established, according to Rule 38.2, by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.
6. With regard to the drawings,
   a. the figure of the **drawings** to be published with the abstract is Figure No. **6B**
      ☒ as suggested by the applicant.
      ☐ as selected by this Authority, because the applicant failed to suggest a figure.
      ☐ as selected by this Authority, because this figure better characterizes the invention.
   b. ☐ none of the figures is to be published with the abstract.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/012463

A. CLASSIFICATION OF SUBJECT MATTER

H01R 12/71(2011.01)i, H01R 12/55(2011.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01R 12/71; H01R 13/648; H01R 4/66; H01R 17/04; H01R 12/00; H01R 12/55

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: electrical connector, electromagnetic shielding material, conductive element, compliant member

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5334050 A (DEREK ANDREWS) 02 August 1994 See abstract, column 4, line 25 - column 6, line 5, claim 1, and figures 1-5.	1-35,39-45
Y		36-38
Y	US 2009-0305533 A1 (STEVEN FELDMAN et al.) 10 December 2009 See paragraphs [0034]-[0036], [0061]-[0064], claims 1, 3-4, and figures 1, 13.	36-38
Y	US 2005-0233610 A1 (CHRISTOPHER ALAN TUTT et al.) 20 October 2005 See paragraphs [0113]-[0117], claim 1, and figure 10.	37
A	US 5176538 A (GEORGE A. HANSELL, III et al.) 05 January 1993 See column 3, line 16 - column 4, line 47, claim 1, and figures 1-3, 11.	1-45
A	US 2004-0005815 A1 (AKINORI MIZUMURA et al.) 08 January 2004 See paragraphs [0045]-[0066], claim 1, and figures 1, 3, 8.	1-45

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
12 May 2015 (12.05.2015)	**13 May 2015 (13.05.2015)**

Name and mailing address of the ISA/KR	Authorized officer
International Application Division Korean Intellectual Property Office 189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City, 302-701, Republic of Korea Facsimile No. ++82 42 472 7140	KIM, Sung Gon Telephone No. +82-42-481-8746

Form PCT/ISA/210 (second sheet) (January 2015)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2015/012463

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5334050 A	02/08/1994	EP 0555933 A1	18/08/1993
		EP 0555933 B1	08/05/1996
		JP 06-013136 A	21/01/1994
		JP 3300450 B2	08/07/2002
		KR 10-0270419 B1	01/11/2000
US 2009-0305533 A1	10/12/2009	CN 102106041 A	22/06/2011
		EP 2304849 A2	06/04/2011
		EP 2304849 A4	18/07/2012
		JP 2011-523196 A	04/08/2011
		KR 10-2011-0027757 A	16/03/2011
		US 7651374 B2	26/01/2010
		WO 2009-152081 A2	17/12/2009
		WO 2009-152081 A3	04/03/2010
US 2005-0233610 A1	20/10/2005	CA 2544851 A1	19/05/2005
		CA 2544851 C	14/08/2012
		CA 2608509 A1	30/11/2006
		CA 2608509 C	07/05/2013
		CN 101208837 A	25/06/2008
		CN 101208837 B	27/03/2013
		CN 1902786 A	24/01/2007
		CN 1902786 B	04/01/2012
		EP 1687870 A1	09/08/2006
		EP 1894278 A1	05/03/2008
		JP 2007-511051 A	26/04/2007
		JP 2008-541409 A	20/11/2008
		JP 4943157 B2	30/05/2012
		JP 4949386 B2	06/06/2012
		KR 10-1166953 B1	19/07/2012
		KR 10-2008-0019203 A	03/03/2008
		US 2005-0095896 A1	05/05/2005
		US 2006-0194477 A1	31/08/2006
		US 2007-0184681 A1	09/08/2007
		US 2009-0176410 A1	09/07/2009
		US 2010-0273350 A1	28/10/2010
		US 7074047 B2	11/07/2006
		US 7249953 B2	31/07/2007
		US 7404718 B2	29/07/2008
		US 7503768 B2	17/03/2009
		US 7748990 B2	06/07/2010
		US 7997907 B2	16/08/2011
		WO 2005-046005 A1	19/05/2005
		WO 2006-127521 A1	30/11/2006
US 5176538 A	05/01/1993	GB 2267787 A	15/12/1993
		WO 93-12564 A1	24/06/1993
US 2004-0005815 A1	08/01/2004	CN 1204655 C	01/06/2005

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2015/012463

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
		CN 1446391 A	01/10/2003
		EP 1327288 A1	16/07/2003
		JP 2002-151207 A	24/05/2002
		JP 4451978 B2	14/04/2010
		US 6780058 B2	24/08/2004
		WO 02-33789 A1	25/04/2002

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:
CHEUNG HUGHES, LING

WOLF, GREENFIELD & SACKS, P.C. 600 ATLANTIC AVENUE BOSTON MA 02210-2206 USA

PCT

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43bis.1)

Date of mailing *(day/month/year)*	**13 May 2015 (13.05.2015)**
Applicant's or agent's file reference A0863.70078	**FOR FURTHER ACTION** See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US2015/012463	**22 January 2015 (22.01.2015)**	22 January 2014 (22.01.2014)

International Patent Classification (IPC) or both national classification and IPC

H01R 12/71(2011.01)i, H01R 12/55(2011.01)i

Applicant
AMPHENOL CORPORATION

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step and industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☒ Box No. VII Certain defects in the international application
- ☒ Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1bis(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.
For further options, see Form PCT/ISA/220.

Name and mailing address of the ISA/KR	Date of completion of this opinion	Authorized officer
International Application Division Korean Intellectual Property Office 189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City, 302-701, Republic of Korea Facsimile No. ++82 42 472 7140	12 May 2015 (12.05.2015)	KIM, Sung Gon Telephone No. +82-42-481-8746

Form PCT/ISA/237 (cover sheet) (January 2015)

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2015/012463

Box No. I Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of:

   ☒ the international application in the language in which it was filed

   ☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(a))

3. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of a sequence listing:

   a. ☐ forming part of the international application as filed:
      ☐ in the form of an Annex C/ST.25 text file.
      ☐ on paper or in the form of an image file.

   b. ☐ furnished together with the international application under PCT Rule 13*ter*.1(a) for the purposes of international search only in the form of an Annex C/ST.25 text file.

   c. ☐ furnished subsequent to the international filing date for the purposes of international search only:
      ☐ in the form of an Annex C/ST.25 text file (Rule 13*ter*.1(a)).
      ☐ on paper or in the form of an image file (Rule 13*ter*.1(b) and Administrative Instructions, Section 713).

4. ☐ In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that forming part of the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2015/012463

Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Claims	1-45	YES
	Claims	NONE	NO
Inventive step (IS)	Claims	NONE	YES
	Claims	1-45	NO
Industrial applicability (IA)	Claims	1-45	YES
	Claims	NONE	NO

2. Citations and explanations :

Reference is made to the following documents:

D1: US 5334050 A (DEREK ANDREWS) 02 August 1994
D2: US 2009-0305533 A1 (STEVEN FELDMAN et al.) 10 December 2009
D3: US 2005-0233610 A1 (CHRISTOPHER ALAN TUTT et al.) 20 October 2005

1. Novelty and Inventive Step

1.1. Claims [1-26]

D1, which is considered to be the closest prior art to the subject matter of independent claim [1], discloses a coaxial connector module (1) comprising: coaxial contact elements (4), each coaxial contact element (4) including plastic support elements (31, 32) and electrical conductors (25); and casings (14, 15) of electrically conducting sheet material, wherein the plastic support elements (31, 32) can be made of any other suitable insulation material, while the electrical conductors (25) themselves can be provided with an electrically insulating sheath, wherein the coaxial contact elements (4) are arranged in two rows each with three in columns, and wherein the casings (14, 15) surround and electrically insulate the electrical conductors (25) (see column 4, line 25 - column 5, line 66, claim 1, and figures 1-3, 5 in D1).

The present invention slightly differs from D1 in that claim [1] comprises electromagnetic shielding material, whereas D1 discloses the casings (14, 15) of the electrically conducting sheet material. However, such a slight design change comes within the scope of customary practice followed by a person skilled in the art. Accordingly, claim [1] would have been obvious over D1. Therefore, claim [1] lacks an inventive step under PCT Article 33(3).

The additional features of claims [2-5] are merely variations of the disclosure of D1 considering the casings (14, 15) of the electrically conducting sheet material (see column 4, lines 50-52 in D1), and a person skilled in the art would arrive at the claimed invention by general experimentation alone without exercising any ingenuity.

Continued on Supplemental Box

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2015/012463

Box No. VII Certain defects in the international application

The following defects in the form or contents of the international application have been noted:

Claims [25-26] do not comply with PCT Rule 6.4(a) because the claims [25-26] have referred to themselves, not to other claims.
(NOTE: This written opinion has been established on the assumption that claims [25-26] refer to claim 24.)

Box No. VIII Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

Claim [20] is worded in reference to "the first and second shield members" of claim 1. However, said "first and second shield members" has not been worded in claim 1 (PCT Article 6).
(NOTE: This written opinion has been established on the assumption that claim [20] refers to claim 19.)

Claim [21] is worded in reference to "the at least one lossy portion" of claim 1. However, said "at least one lossy portion" has not been worded in claim 1 (PCT Article 6).
(NOTE: This written opinion has been established on the assumption that claim [21] refers to claim 20.)

Supplemental Box

In case **the space in any of the preceding boxes is not sufficient.**
Continuation of : Box No. V

The additional features of claims [6-7] are merely variations of the disclosure of D1 considering that the coaxial connector module (1) includes an assembly or unit of the two coaxial contact elements (4) situated in a column such that one is above the other, and the above one is longer than the other (see column 4, lines 59-61 and figure 3 in D1), and a person skilled in the art would arrive at the claimed invention by general experimentation alone without exercising any ingenuity.

The additional feature of claim [8] is merely a variation of the disclosure of D1 considering that the coaxial contact elements (4) are arranged in the two rows each with three in columns and each assembly or unit of the two coaxial contact elements (4) is situated in a column such that one is above the other, and the above one is longer than the other (see column 4, lines 25-30, 59-61 and figures 1-3 in D1), and a person skilled in the art would arrive at the claimed invention by general experimentation alone without exercising any ingenuity.

The additional feature of claim [9] is merely a variation of the disclosure of D1 considering that the casings (14, 15) of the coaxial contact elements (4) are arranged in three columns (see column 4, lines 25-30, 50-61 and figures 1-3 in D1), and a person skilled in the art would arrive at the claimed invention by general experimentation alone without exercising any ingenuity.

The additional feature of claim [10] is merely a variation of the disclosure of D1 considering that the casings (14, 15) surround the electrical conductors (25) (see column 5, lines 19-24 and figure 3 in D1), and a person skilled in the art would arrive at the claimed invention by general experimentation alone without exercising any ingenuity.

The additional features of claims [11-12] are merely variations of the disclosure of D1 considering the electrical conductors (25) (see column 5, lines 19-22 and figure 3 in D1), and a person skilled in the art would arrive at the claimed invention by general experimentation alone without exercising any ingenuity.

The additional feature of claim [13] is merely a variation of the disclosure of D1 considering the casings (14, 15) of the electrically conducting sheet material (see column 4, lines 50-52 in D1), and a person skilled in the art would arrive at the claimed invention by general experimentation alone without exercising any ingenuity.

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The additional features of claims [14-16] are merely variations of the disclosure of D1 considering that the plastic support elements (31, 32) are disposed between side-pieces (19, 22) of the casings (14, 15) (see column 5, lines 60-62 and figure 5 in D1), and a person skilled in the art would arrive at the claimed invention by general experimentation alone without exercising any ingenuity.

Claim [17] further specifies at least one conductive element which comprises a conductive wire, an insulative portion which comprises a passageway, and the wire which is routed through the passageway. However, the feature is regarded as a normal design option within the coverage of the prior art by a person skilled in the art.

Claim [18] further specifies the insulative portion which is formed by molding and the wire which is threaded through the passageway after the insulative portion has been molded. However, the feature is regarded as a normal design option within the coverage of the prior art by a person skilled in the art.

Claim [19] further specifies a shielding material comprising a first shield member and a second shield member disposed on opposing sides of a module. However, the feature is regarded as a normal design option within the coverage of the prior art by a person skilled in the art.

Claims [20-21] further comprise at least one lossy portion and further specify the at least one lossy portion which is elongated and runs along an entire length of the first shield member. However, the features are regarded as normal design options within the coverage of the prior art by a person skilled in the art.

The additional feature of claim [22] is merely a variation of the disclosure of D1 considering that soldering pins (44, 45) are attached to a connection end of the conductor (25), and an outer contact part (33) and a pin-shaped inner contact part (34) are attached to a contact side of the coaxial contact element (4) (see column 5, lines 55-59, column 6, lines 1-5 and figures 1-3, 5 in D1), and a person skilled in the art would arrive at the claimed invention by general experimentation alone without exercising any ingenuity.

The additional feature of claim [23] is virtually suggested by the feature of D1, considering that the casings (14, 15) have a cross-section similar to U-shape (see figure 4 in D1).

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The additional feature of claim [24] is merely a variation of the disclosure of D1 considering that each coaxial contact element (4) has the soldering pins (44, 45) to mount on a printed circuit board (see column 6, lines 1-5 and figures 1-3, 5 in D1), and a person skilled in the art would arrive at the claimed invention by general experimentation alone without exercising any ingenuity.

Claims [25-26] further specify an organizer adapted to occupy space between an electrical connector and a surface of a printed circuit board and comprising a flat surface and an opposing surface. However, the features are regarded as normal design options within the coverage of the prior art by a person skilled in the art.

Therefore, claims [2-26] lack an inventive step under PCT Article 33(3).

1.2. Claims [27-35]

D1, which is considered to be the closest prior art to the subject matter of independent claim [27], discloses a coaxial connector module (1) comprising: coaxial contact elements (4) arranged in two rows each with three in columns, each coaxial contact element (4) including a socket-type inner contact part (6) having a connection end and a contact side, the inner contact part (6) having an electrical conductor (25) extending from the connection end to the contact side and a casing (14, 15) surrounding the conductor (25), soldering pins (44, 45) attached to the connection end of the conductor (25), and an outer contact part (33) and a pin-shaped inner contact part (34) attached to the contact side of the coaxial contact element (4) (see column 4, line 25 - column 6, line 5, claim 1, and figures 1-3, 5 in D1).

The present invention slightly differs from D1 in that claim [27] comprises a cable, whereas D1 discloses the inner contact part (6). However, such a slight design change comes within the scope of customary practice followed by a person skilled in the art. Accordingly, claim [27] would have been obvious over D1. Therefore, claim [27] lacks an inventive step under PCT Article 33(3).

Claim [28] further comprises an insulative portion at a first end of the cable and specifies contact tails of a pair of conductive elements which are attached to the insulative portion. However, the feature is regarded as a normal design option within the coverage of the prior art by a person skilled in the art.

The additional feature of claim [29] is merely a variation of the disclosure of D1

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considering that the soldering pins (44, 45) of each coaxial contact element (4) are formed to mount on a printed circuit board (see column 6, lines 1-5 and figures 1-3, 5 in D1), and a person skilled in the art would arrive at the claimed invention by general experimentation alone without exercising any ingenuity.

The additional feature of claim [30] is merely a variation of the disclosure of D1 considering that the casing (14, 15) surrounds the conductor (25) (see column 5, lines 19-24 and figure 3 in D1), and a person skilled in the art would arrive at the claimed invention by general experimentation alone without exercising any ingenuity.

Claim [31] further comprises a lossy member attached to a conductive structure. However, the feature is regarded as a normal design option within the coverage of the prior art by a person skilled in the art.

The additional feature of claim [32] can be easily derived from the feature of D1 in that a housing (2) of plastic has the coaxial contact elements (4) therein (see column 4, lines 27-30 and figure 1 in D1).

The additional feature of claim [33] can be easily derived from the feature of D1 in that the outer contact part (33) and the pin-shaped inner contact part (34) are attached to the contact side of the coaxial contact element (4) (see column 5, lines 55-59 and figure 5 in D1).

Claim [34] further comprises a conductive structure at a second end of the cable and specifies the conductive structure which surrounds the insulative portion. However, the feature is regarded as a normal design option within the coverage of the prior art by a person skilled in the art.

The additional feature of claim [35] can be easily derived from the feature of D1 in that the housing (2) has lobes (7) for engaging in corresponding grooves of a further connector to be contacted with a connector and hook-shaped projections (8) serving to lock the coaxial connector module (1) to the further connector (see column 4, lines 34-41 and figure 1 in D1).

Therefore, claims [28-35] lack an inventive step under PCT Article 33(3).

1.3. Claims [36-38]

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D1, which is considered to be the closest prior art to the subject matter of independent claim [36], discloses a coaxial connector module (1) comprising: electrical conductors (25), each electrical conductor (25) including a circular cylindrical outer contact part (5) surrounding a socket-type inner contact part (6) that is disposed to define a mating interface of the coaxial connector module (1); and a housing (2) adjacent the outer and inner contact parts (5, 6), the housing (2) having two rows each with three channels (3) arranged in columns (see column 4, line 25 - column 6, line 5, claim 1, and figures 1-3, 5 in D1).

The present invention differs from D1 in a plurality of compliant members attached to a plurality of conductive walls, the plurality of compliant members being positioned adjacent a forward edge, wherein the walls bounding each of a plurality of regions comprise at least two of the plurality of compliant members, and at least two contact surfaces, the at least two contact surfaces being set back from the forward edge and adapted for making electrical contact with a compliant member from a mating electrical connector. However, the feature is merely a variation of the disclosure of D2 considering a shielded connector (226) comprising: a shield body (240) including any suitable shape such as a cylindrical hull, or a hull having a square or rectangular cross-sectional shape and disposed around an insulator (35) that is disposed around a contact (32); and a first ground wiper (242) and a second ground wiper (244), which are resilient and flexible grounding beams, disposed on the shield body (240) and adjacent a forward edge, wherein the ground wiper (244) is configured to have a sufficient range of resilient flexibility to ensure that the ground wiper (244) will extend fully away from the shield body (240) and make connection with a plate (254) on a printed circuit board (225) (see paragraphs [0034]-[0036], [0061]-[0064], claims 1, 3-4, and figures 1, 13 in D2), and a person skilled in the art would arrive at the claimed invention by general experimentation alone without exercising any ingenuity. Accordingly, claim [36] would have been obvious over a combination of D1 and D2. Therefore, claim [36] lacks an inventive step under PCT Article 33(3).

The additional feature of claim [37] is merely a variation of the disclosure of D3 considering that a connector assembly (200) includes connector assemblies (200a, 200b) that couple together signal arrays (202a, 202b) and utilize alignment pins (222) and corresponding alignment openings (224) (see paragraphs [0113], [0117] and figure 10 in D3), and a person skilled in the art would arrive at the claimed invention by general experimentation alone without exercising any ingenuity.

The additional feature of claim [38] is merely a variation of the disclosure of D2 considering that the first ground wiper (242) and the second ground wiper (244), which

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are the resilient and flexible grounding beams, are disposed on the shield body (240) and adjacent the forward edge (see paragraphs [0063]-[0064] and figure 13 in D2), and a person skilled in the art would arrive at the claimed invention by general experimentation alone without exercising any ingenuity.

Therefore, claims [37-38] lack an inventive step under PCT Article 33(3).

1.4. Claims [39-45]

D1, which is considered to be the closest prior art to the subject matter of independent claim [39], discloses a method comprising: providing coaxial contact elements (4), each coaxial contact element (4) including plastic support elements (31, 32) and electrical conductors (25); and arranging the coaxial contact elements (4) in two rows each with three in columns, and using electrically conducting sheet material to electrically insulate the electrical conductors (25), wherein the elements (31, 32) can be made of any other suitable insulation material, while the electrical conductors (25) themselves can be provided with an electrically insulating sheath (see column 4, line 25 - column 5, line 66, claim 1, and figures 1-3, 5 in D1).

The present invention slightly differs from D1 in that claim [39] comprises using electromagnetic shielding material to separate adjacent modules of a plurality of modules, whereas D1 discloses using the electrically conducting sheet material to electrically insulate the electrical conductors (25). However, such a slight design change comes within the scope of customary practice followed by a person skilled in the art. Accordingly, claim [39] would have been obvious over D1. Therefore, claim [39] lacks an inventive step under PCT Article 33(3).

Claim [40] further specifies the shielding material which comprises lossy material, and a method which comprises an act of overmolding the lossy material on at least a portion of the modules. However, the feature is regarded as a normal design option within the coverage of the prior art by a person skilled in the art.

The additional features of claims [41-42] are merely variations of the disclosure of D1 considering that a coaxial connector module (1) includes an assembly or unit of two coaxial contact elements (4) situated in a column such that one is above the other, and the above one is longer than the other (see column 4, lines 59-61 and figure 3 in D1), and a person skilled in the art would arrive at the claimed invention by general experimentation alone without exercising any ingenuity.

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The additional feature of claim [43] is merely a variation of the disclosure of D1 considering that the coaxial contact elements (4) are arranged in two rows each with three in columns and each assembly or unit of the two coaxial contact elements (4) is situated in a column such that one is above the other, and the above one is longer than the other (see column 4, lines 25-30, 59-61 and figures 1-3 in D1), and a person skilled in the art would arrive at the claimed invention by general experimentation alone without exercising any ingenuity.

Claim [44] further specifies at least one conductive element which comprises a conductive wire, an insulative portion which comprises a passageway, and the method which comprises threading the conductive wire through the passageway. However, the feature is regarded as a normal design option within the coverage of the prior art by a person skilled in the art.

Claim [45] further comprises an act of prior to threading the conductive wire through the passageway, forming the insulative portion by molding. However, the feature is regarded as a normal design option within the coverage of the prior art by a person skilled in the art.

Therefore, claims [40-45] lack an inventive step under PCT Article 33(3).

2. Industrial Applicability
Claims [1-45] are industrially applicable under PCT Article 33(4).

Electronic Acknowledgement Receipt

EFS ID:	25248716
Application Number:	15065683
International Application Number:	
Confirmation Number:	5112
Title of Invention:	HIGH PERFORMANCE CABLE CONNECTOR
First Named Inventor/Applicant Name:	Donald W. Milbrand, Jr.
Customer Number:	23628
Filer:	Edmund J. Walsh/Yehoshua Zehavi
Filer Authorized By:	Edmund J. Walsh
Attorney Docket Number:	A0863.70051US04
Receipt Date:	20-MAR-2016
Filing Date:	
Time Stamp:	10:49:08
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	A086370051US04-TRN-EJW.pdf	24603 3e32445d24e0ac9f9115933bab6fbd2e27d26522	no	1

Warnings:	
Information:	

2		A086370051US04-IDS-EJW.pdf	85767 c54246ea6d4d68f2500dfe64e72c22060d5f7998	yes	11
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Transmittal Letter		1	4	
	Information Disclosure Statement (IDS) Form (SB08)		5	11	
Warnings:					
Information:					
3	Other Reference-Patent/App/Search documents	A086370078WO00_ISR_WO_mailed_5-13-2015_QC.pdf	1974946 05ecab039663732a6441f109fdd52936ee19deac	no	18
Warnings:					
Information:					
		Total Files Size (in bytes):	2085316		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc Code: TRAN.LET
Document Description: Transmittal Letter

USED IN LIEU OF PTO/SB/21 (07-09)

TRANSMITTAL FORM (to be used for all correspondence after initial filing)			
		Application Number	15/065,683-Conf. #5112
		Filing Date	March 9, 2016
		First Named Inventor	Donald W. Milbrand, Jr.
		Art Unit	2833
		Examiner Name	Not Yet Assigned
Total Number of Pages in This Submission		Attorney Docket Number	A0863.70051US04

ENCLOSURES (*Check all that apply*)

☐ Fee Transmittal Form	☐ Drawing(s)	☐ After Allowance Communication to TC
☐ Fee Attached	☐ Licensing-related Papers	☐ Appeal Communication to Board of Appeals and Interferences
☐ Amendment/Reply	☐ Petition	☐ Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
☐ After Final	☐ Petition to Convert to a Provisional Application	☐ Proprietary Information
☐ Affidavits/declaration(s)	☐ Power of Attorney, Revocation Change of Correspondence Address	☐ Status Letter
☐ Extension of Time Request	☐ Terminal Disclaimer	☒ Other Enclosure(s) (please Identify below):
☐ Express Abandonment Request	☐ Request for Refund	Form PTO-1449 Copy of cited reference
☒ Information Disclosure Statement	☐ CD, Number of CD(s) _____	
☐ Certified Copy of Priority Document(s)	☐ Landscape Table on CD	
☐ Reply to Missing Parts/ Incomplete Application	Remarks	
☐ Reply to Missing Parts under 37 CFR 1.52 or 1.53		

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	WOLF, GREENFIELD & SACKS, P.C.		
Signature	/Edmund J. Walsh/		
Printed name	Edmund J. Walsh		
Date	March 20, 2016	Reg. No.	32,950

Certificate of Electronic Filing Under 37 CFR 1.8

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being transmitted via the Office electronic filing system in accordance with 37 CFR § 1.6(a)(4).

Dated: March 20, 2016 Electronic Signature for Yehoshua E. Zehavi: /Yehoshua E. Zehavi/

4657436.1

DOCKET NO.: A0863.70051US04

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor:	Donald W. Milbrand, Jr.
Application No.:	15/065,683
Confirmation No.:	5112
Filed:	March 9, 2016
For:	HIGH PERFORMANCE CABLE CONNECTOR
Examiner:	Not Yet Assigned
Art Unit:	2833

CERTIFICATE OF ELECTRONIC FILING UNDER 37 C.F.R. § 1.8

The undersigned hereby certifies that this paper, along with any paper referred to as being attached or enclosed, is being transmitted via the Office electronic filing system in accordance with § 1.6(a)(4), on the 20th day of March, 2016.

/Yehoshua E. Zehavi/
Yehoshua E. Zehavi

MAIL STOP AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

STATEMENT FILED PURSUANT TO THE DUTY OF DISCLOSURE UNDER 37 C.F.R. §§ 1.56, 1.97 AND 1.98

Sir:

Pursuant to the duty of disclosure under 37 C.F.R. §§ 1.56, 1.97 and 1.98, the undersigned requests consideration of this Information Disclosure Statement.

PART I: Compliance with 37 C.F.R. § 1.97

This Information Disclosure Statement has been filed within three months of the filing date of a national application other than a continued prosecution application under 37 C.F.R. § 1.53(d).

No fee or certification is required.

PART II: Information Cited

The undersigned hereby makes of record in the above-identified application the information listed on the attached form PTO-1449 (modified PTO/SB/08). The order of

presentation of the references should not be construed as an indication of the importance of the references.

The undersigned hereby makes the following additional information of record in the above-identified application.

The undersigned would like to bring to the Examiner's attention the following co-pending applications that may contain subject matter related to this application:

Serial No.	Filing Date	Inventor(s)	Docket No.
*13/752,534	January 29, 2013	Gailus et al.	N/A
*13/775,808	February 25, 2013	Khilchenko et al.	N/A
*14/948,171	November 20, 2015	Atkinson et al.	A0863.70041US04
*13/683,295	November 21, 2012	Milbrand, Jr. et al.	A0863.70051US02
*13/973,921	August 22, 2013	Cohen	A0863.70063US01
*13/930,447	June 28, 2013	Cartier, Jr. et al.	A0863.70065US02
*14/640,114	March 6, 2015	Paniagua	A0863.70066US02
*14/209,240	March 13, 2014	Cartier, Jr. et al.	A0863.70068US01
*14/209,079	March 13, 2014	Cartier, Jr. et al.	A0863.70069US01
*14/603,300	January 22, 2015	Cartier, Jr. et al.	A0863.70078US01
*14/603,294	January 22, 2015	Cartier, Jr. et al.	A0863.70078US02

*A copy of this reference is not provided as the Office has waived the requirement under 37 C.F.R. § 1.98(a)(2)(iii) for submitting a copy of a cited U.S. patent application if it is scanned to the Image File Wrapper system and is available on Private PAIR.

The undersigned would like to bring to the Examiner's attention the enclosed search report or other communication from a corresponding or related International or Foreign National Application:

Serial No.	Date of Mailing	Type(s) of Communication	Docket No.
***EP 11166820.8**	**January 24, 2012**	**Extended European Search Report**	**N/A**

***PCT/US2005/034605**	**January 26, 2006**	**International Search Report and Written Opinion**	**N/A**
***PCT/US2006/025562**	**October 31, 2007**	**International Search Report with Written Opinion**	**N/A**
***PCT/US2010/056482**	**March 14, 2011**	**International Search Report and Written Opinion**	**A0863.70049WO00**
***PCT/US2010/056482**	**May 24, 2012**	**International Preliminary Report on Patentability**	**A0863.70049WO00**
***PCT/US2011/026139**	**November 22, 2011**	**International Search Report and Written Opinion**	**A0863.70055WO00**
***PCT/US2011/026139**	**September 7, 2012**	**International Preliminary Report on Patentability**	**A0863.70055WO00**
***PCT/US2011/034747**	**July 28, 2011**	**International Search Report and Written Opinion**	**N/A**
***PCT/US2012/023689**	**September 12, 2012**	**International Search Report and Written Opinion**	**A0863.70061WO00**
***PCT/US2012/023689**	**August 15, 2013**	**International Preliminary Report on Patentability**	**A0863.70061WO00**
***PCT/US2012/060610**	**March 29, 2013**	**International Search Report and Written Opinion**	**A0863.70066WO00**
PCT/US2015/012463	**May 13, 2015**	**International Search Report and Written Opinion**	**A0863.70078WO00**

*a copy of this reference is not provided as it was previously cited by or submitted to the office in a prior application, Serial No. 13/683,295, filed November 21, 2012, and relied upon for an earlier filing date under 35 U.S.C. 120 (continuation, continuation-in-part, and divisional applications).

PART III: Remarks

Documents cited anywhere in the Information Disclosure Statement are enclosed unless otherwise indicated. It is respectfully requested that:

1. The Examiner consider completely the cited information, along with any other information, in reaching a determination concerning the patentability of the present claims;

2. The enclosed form PTO-1449 (modified PTO/SB/08) be signed by the Examiner to evidence that the cited information has been fully considered by the United States Patent and Trademark Office during the examination of this application;

3. The citations for the information be printed on any patent which issues from this application.

By submitting this Information Disclosure Statement, the undersigned makes no representation that a search has been performed, of the extent of any search performed, or that more relevant information does not exist.

By submitting this Information Disclosure Statement, the undersigned makes no representation that the information cited in the Statement is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b).

By submitting this Information Disclosure Statement, the undersigned makes no representation that the information cited in the Statement is, or is considered to be, in fact, prior art as defined by 35 U.S.C. § 102.

Notwithstanding any statements by the undersigned, the Examiner is urged to form his or her own conclusion regarding the relevance of the cited information.

An early and favorable action is hereby requested.

The Director is hereby authorized to charge any deficiency or credit any overpayment in the fees occasioned by the filing of this Information Disclosure Statement to our Deposit Account No. 23/2825 under Docket No. A0863.70051US04 from which the undersigned is authorized to draw.

Respectfully submitted,

By: /Edmund J. Walsh/
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Docket No.: A0863.70051US04
Date: March 20, 2016
xNDDx

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
15/065,683	03/09/2016	2833	1760	A0863.70051US04	22	1

CONFIRMATION NO. 5112

23628
WOLF GREENFIELD & SACKS, P.C.
600 ATLANTIC AVENUE
BOSTON, MA 02210-2206

FILING RECEIPT

OC000000081632040

Date Mailed: 03/25/2016

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Donald W. Milbrand JR., Bristol, NH;
Prescott B. Atkinson, Nottingham, NH;
Brian Kirk, Amherst, NH;

Applicant(s)

Amphenol Corporation, Wallingford Center, CT;

Assignment For Published Patent Application

Amphenol Corporation, Wallingford Center, CT

Power of Attorney: None

Domestic Priority data as claimed by applicant

This application is a CON of 13/683,295 11/21/2012
which is a CON of 13/671,096 11/07/2012
which is a CON of PCT/US2011/035515 05/06/2011
which claims benefit of 61/332,366 05/07/2010

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 03/23/2016

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 15/065,683**

Projected Publication Date: Request for Non-Publication Acknowledged

Non-Publication Request: Yes

Early Publication Request: No

Title

HIGH PERFORMANCE CABLE CONNECTOR

Preliminary Class

439

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific

countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop

technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 15/065,683

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	600
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720
TOTAL CLAIMS (37 CFR 1.16(i))	22 minus 20 =	* 2			OR	x 80 =	160
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1 minus 3 =	*				x 420 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1760

APPLICATION AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)	OR	RATE($)	ADDITIONAL FEE($)
Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

PTO/AIA/80 (07-12)
Approved for use through 11/30/2014. OMB 0651-0035
U.S. Patent and Trademark Office; U.S DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(c).

I hereby appoint:

[X] Practitioners associated with Customer Number: 23628

OR

[ ] Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

As attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignments documents attached to this form in accordance with 37 CFR 3.73(c).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(c) to:

[ ] The address associated with Customer Number:

OR

[ ] Firm or Individual Name			
Address			
City		State	Zip
Country			
Telephone		Email	

Assignee Name and Address:

Amphenol Corporation
358 Hall Avenue
Wallingford Center, Connecticut 06492-3574

A copy of this form, together with a statement under 37 CFR 3.73(c) (Form PTO/AIA/96 or equivalent) is required to be filed in each application in which this form is used. The statement under 37 CFR 3.73(c) may be completed by one of the practitioners appointed in this form, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature	[signature]	Date	1/15/2016
Name	Thomas S Pitten	Telephone	(203) 320-4204
Title	VP Engineering		

4037495

PTO/AIA/96 (08-12)
Approved for use through 01/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: Amphenol Corporation

Application No./Patent No.: 15/065,683 Filed/Issue Date: March 9, 2016

Titled: HIGH PERFORMANCE CABLE CONNECTOR

Amphenol Corporation (Name of Assignee) , a Corporation (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. [X] The assignee of the entire right, title, and interest.

2. [ ] An assignee of less than the entire right, title, and interest (check applicable box):

   [ ] (The extent (by percentage) of its ownership interest is _____ %). Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

   [ ] There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. [ ] The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. [ ] The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2, or 3 above (not option 4) is evidence by either (choose **one** of options A or B below):

A. [X] An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 031170 , Frame 0638 , or for which a copy thereof is attached.

B. [ ] A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

   1. From: _____ To: _____
      The document was recorded in the United States Patent and Trademark Office at
      Reel _____ , Frame _____ , or for which a copy thereof is attached.

   2. From: _____ To: _____
      The document was recorded in the United States Patent and Trademark Office at
      Reel _____ , Frame _____ , or for which a copy thereof is attached.

PTO/AIA/96 (08-12)
Approved for use through 01/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____
The document was recorded in the United States Patent and Trademark Office at
Reel _____ , Frame _____ , or for which a copy thereof is attached.

4. From: _____ To: _____
The document was recorded in the United States Patent and Trademark Office at
Reel _____ , Frame _____ , or for which a copy thereof is attached.

5. From: _____ To: _____
The document was recorded in the United States Patent and Trademark Office at
Reel _____ , Frame _____ , or for which a copy thereof is attached.

6. From: _____ To: _____
The document was recorded in the United States Patent and Trademark Office at
Reel _____ , Frame _____ , or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☐ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

William R. McClellan	May 10, 2016
Signature	Date
William R. McClellan	29,409
Printed or Typed Name	Title or Registration Number

Certificate of Electronic Filing Under 37 CFR 1.8

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being transmitted via the Office electronic filing system in accordance with 37 CFR § 1.6(a)(4).

Dated: May 10, 2016 Signature: Doris A. Champagne (Doris A. Champagne)

Electronic Acknowledgement Receipt

EFS ID:	25733557
Application Number:	15065683
International Application Number:	
Confirmation Number:	5112
Title of Invention:	HIGH PERFORMANCE CABLE CONNECTOR
First Named Inventor/Applicant Name:	Donald W. Milbrand
Customer Number:	23628
Filer:	William R. McClellan/Doris Champagne
Filer Authorized By:	William R. McClellan
Attorney Docket Number:	A0863.70051US04
Receipt Date:	10-MAY-2016
Filing Date:	09-MAR-2016
Time Stamp:	14:18:22
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	A086370051US04-TRN-WRM.PDF	56251 d5d546fa87ec0729e313b491d79bcd0235b75b40	no	1

Warnings:	
Information:	

2	Power of Attorney	A086370051US04-POA-WRM.PDF	63799 7527391f9c9e636e38e86f9283e2df47694a73d3	no	1
Warnings:					
Information:					
3	Assignee showing of ownership per 37 CFR 3.73	A086370051US04-373-WRM.PDF	110187 2b8abc08b699dfac91681c5d8c91600d0922e59a	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	230237		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc Code: TRAN.LET
Document Description: Transmittal Letter

USED IN LIEU OF PTO/SB/21 (07-09)

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission	4

Application Number	15/065,683-Conf. #5112
Filing Date	March 9, 2016
First Named Inventor	Donald W. Milbrand, Jr.
Art Unit	2833
Examiner Name	Figueroa, F.O.
Attorney Docket Number	A0863.70051US04

ENCLOSURES (*Check all that apply*)

- [ ] Fee Transmittal Form
  - [ ] Fee Attached
- [ ] Amendment/Reply
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Reply to Missing Parts/ Incomplete Application
  - [ ] Reply to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [x] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s) _____
  - [ ] Landscape Table on CD
- [ ] After Allowance Communication to TC
- [ ] Appeal Communication to Board of Appeals and Interferences
- [ ] Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- [ ] Proprietary Information
- [ ] Status Letter
- [x] Other Enclosure(s) (please Identify below):

3.73(c) Statement

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	WOLF, GREENFIELD & SACKS, P.C.		
Signature	William R. McClellan		
Printed name	William R. McClellan		
Date	May 10, 2016	Reg. No.	29,409

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Dated: May 10, 2016 Signature: Doris A. Champagne (Doris A. Champagne)

4748409.1

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/065,683	03/09/2016	Donald W. Milbrand JR.	A0863.70051US04

CONFIRMATION NO. 5112

23628
WOLF GREENFIELD & SACKS, P.C.
600 ATLANTIC AVENUE
BOSTON, MA 02210-2206

POA ACCEPTANCE LETTER

OC000000083027012

Date Mailed: 05/20/2016

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 05/10/2016.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/fstephanos/

FORM PTO-1449/A and B (modified PTO/SB/08)	APPLICATION NO.: 15/065,683	ATTY. DOCKET NO.: A0863.70051US04
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	FILING DATE: March 9, 2016	CONFIRMATION NO.: 5112
	FIRST NAMED INVENTOR: Donald W. Milbrand	
Sheet 1 of 1	GROUP ART UNIT: 2833	EXAMINER: Felix O. Figueroa

U.S. PATENT DOCUMENTS

Examiner's Initials #	Cite No.	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication or Issue of Cited Document MM-DD-YYYY
		Number	Kind Code		
		6,565,387	B2	Cohen	05-20-2003
		9,300,074	B2	Gailus	03-29-2016
		9,450,344	B2	Cartier, Jr. et al.	09-20-2016
		2010-0099299	A1	Moriyama et al.	04-22-2010
		2012-0077380	A1	Minich et al.	03-29-2012
		2013-0217263	A1	Pan	08-22-2013
		2013-0273781	A1	Buck et al.	10-17-2013
		2016-0149343	A1	Atkinson et al.	05-26-2016

FOREIGN PATENT DOCUMENTS

Examiner's Initials #	Cite No.	Foreign Patent Document			Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Translation (Y/N)
		Office/ Country	Number	Kind Code			

OTHER ART – NON PATENT LITERATURE DOCUMENTS

Examiner's Initials #	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	Translation (Y/N)

EXAMINER:	DATE CONSIDERED:

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

[NOTE – No copies of U.S. patents, published U.S. patent applications, or pending, unpublished patent applications stored in the USPTO's Image File Wrapper (IFW) system, are included. See 37 CFR § 1.98 and 1287OG163. Copies of all other patent(s), publication(s), unpublished, pending U.S. patent applications, or other information listed are provided as required by 37 CFR § 1.98 unless 1) such copies were provided in an IDS in an earlier application that complies with 37 CFR § 1.98, and 2) the earlier application is relied upon for an earlier filing date under 35 U.S.C. § 120.]

Electronic Acknowledgement Receipt

EFS ID:	27140876
Application Number:	15065683
International Application Number:	
Confirmation Number:	5112
Title of Invention:	HIGH PERFORMANCE CABLE CONNECTOR
First Named Inventor/Applicant Name:	Donald W. Milbrand
Customer Number:	23628
Filer:	Edmund J. Walsh/Yehoshua Zehavi
Filer Authorized By:	Edmund J. Walsh
Attorney Docket Number:	A0863.70051US04
Receipt Date:	06-OCT-2016
Filing Date:	09-MAR-2016
Time Stamp:	13:39:38
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	A086370051US04-TRN-EJW.pdf	24695 72e1bd6ae74c0e6331fc8a24911c25eb44de664d	no	1

Warnings:

Information:					
2		A086370051US04-IDS-EJW.pdf	33869 c260bb243a498b9f7af90325ed9c048f1727e12b	yes	5
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Transmittal Letter		1	4	
	Information Disclosure Statement (IDS) Form (SB08)		5	5	
Warnings:					
Information:					
		Total Files Size (in bytes):	58564		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
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New International Application Filed with the USPTO as a Receiving Office
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Doc Code: TRAN.LET
Document Description: Transmittal Letter

USED IN LIEU OF PTO/SB/21 (07-09)

TRANSMITTAL FORM (to be used for all correspondence after initial filing)			
		Application Number	15/065,683-Conf. #5112
		Filing Date	March 9, 2016
		First Named Inventor	Donald W. Milbrand, Jr.
		Art Unit	2833
		Examiner Name	Felix O. Figueroa
Total Number of Pages in This Submission		Attorney Docket Number	A0863.70051US04

ENCLOSURES (*Check all that apply*)

☐ Fee Transmittal Form	☐ Drawing(s)	☐ After Allowance Communication to TC
☐ Fee Attached	☐ Licensing-related Papers	☐ Appeal Communication to Board of Appeals and Interferences
☐ Amendment/Reply	☐ Petition	☐ Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
☐ After Final	☐ Petition to Convert to a Provisional Application	☐ Proprietary Information
☐ Affidavits/declaration(s)	☐ Power of Attorney, Revocation Change of Correspondence Address	☐ Status Letter
☐ Extension of Time Request	☐ Terminal Disclaimer	☒ Other Enclosure(s) (please Identify below):
☐ Express Abandonment Request	☐ Request for Refund	Form PTO-1449
☒ Information Disclosure Statement	☐ CD, Number of CD(s) _____	
☐ Certified Copy of Priority Document(s)	☐ Landscape Table on CD	
☐ Reply to Missing Parts/ Incomplete Application	Remarks	
☐ Reply to Missing Parts under 37 CFR 1.52 or 1.53		

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	WOLF, GREENFIELD & SACKS, P.C.		
Signature	/Edmund J. Walsh/		
Printed name	Edmund J. Walsh		
Date	October 5, 2016	Reg. No.	32,950

Certificate of Electronic Filing Under 37 CFR 1.8

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being transmitted via the Office electronic filing system in accordance with 37 CFR § 1.6(a)(4).

Dated: October 6, 2016 Electronic Signature for Yehoshua E. Zehavi: /Yehoshua E. Zehavi/

5010261.1

DOCKET NO.: A0863.70051US04

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor:	Donald W. Milbrand
Application No.:	15/065,683
Confirmation No.:	5112
Filed:	March 9, 2016
For:	HIGH PERFORMANCE CABLE CONNECTOR
Examiner:	Felix O. Figueroa
Art Unit:	2833

CERTIFICATE OF ELECTRONIC FILING UNDER 37 C.F.R. § 1.8

The undersigned hereby certifies that this paper, along with any paper referred to as being attached or enclosed, is being transmitted via the Office electronic filing system in accordance with § 1.6(a)(4), on the 6th day of October, 2016.

/Yehoshua E. Zehavi/
Yehoshua E. Zehavi

MAIL STOP AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

STATEMENT FILED PURSUANT TO THE DUTY OF DISCLOSURE UNDER 37 C.F.R. §§ 1.56, 1.97 AND 1.98

Sir:

Pursuant to the duty of disclosure under 37 C.F.R. §§ 1.56, 1.97 and 1.98, the undersigned requests consideration of this Information Disclosure Statement.

PART I: Compliance with 37 C.F.R. § 1.97

This Information Disclosure Statement has been filed before the mailing of a first Office Action on the merits in the above-identified case.

No fee or certification is required.

PART II: Information Cited

The undersigned hereby makes of record in the above-identified application the information listed on the attached form PTO-1449 (modified PTO/SB/08). The order of presentation of the references should not be construed as an indication of the importance of the references.

The undersigned hereby makes the following additional information of record in the above-identified application.

The undersigned would like to bring to the Examiner's attention the following co-pending applications that may contain subject matter related to this application:

Serial No.	Filing Date	Inventor(s)	Docket No.
*13/752,534	January 29, 2013	Gailus et al.	N/A
*13/775,808	February 25, 2013	Khilchenko et al.	N/A
*14/948,171	November 20, 2015	Atkinson et al.	A0863.70041US04
*13/683,295	November 21, 2012	Milbrand, Jr. et al.	A0863.70051US02
*13/973,921	August 22, 2013	Cohen	A0863.70063US01
*13/930,447	June 28, 2013	Cartier, Jr. et al.	A0863.70065US02
*14/640,114	March 6, 2015	Paniagua	A0863.70066US02
*14/209,240	March 13, 2014	Cartier, Jr. et al.	A0863.70068US01
*14/209,079	March 13, 2014	Cartier, Jr. et al.	A0863.70069US01
*14/603,294	January 22, 2015	Cartier, Jr. et al.	A0863.70078US02

*A copy of this reference is not provided as the Office has waived the requirement under 37 C.F.R. § 1.98(a)(2)(iii) for submitting a copy of a cited U.S. patent application if it is scanned to the Image File Wrapper system and is available on Private PAIR.

The above-identified co-pending applications may include subject matter that is technically-related to subject matter of the present application and may contain claims that recite elements similar to those recited in claims of the present application. In handling prosecution of the above-identified applications, the Examiners for these other applications presumably will search for relevant prior art and, in some circumstances, may take positions about the prior art and/or the interpretation of the claims that may be material to the examination of the present application.

Accordingly, the Examiner in the present application is requested to review the file histories of the above-identified co-pending applications to see whether there is any information that the Examiner believes may be relevant to the prosecution of the present application. It is assumed that the Examiner has access to the file histories of the above-identified applications. However, if the Examiner would like copies of any or all of the information included in the file

histories of the above-identified applications, the Examiner is asked to contact the undersigned representative.

PART III: Remarks

Documents cited anywhere in the Information Disclosure Statement are enclosed unless otherwise indicated. It is respectfully requested that:

1. The Examiner consider completely the cited information, along with any other information, in reaching a determination concerning the patentability of the present claims;

2. The enclosed form PTO-1449 (modified PTO/SB/08) be signed by the Examiner to evidence that the cited information has been fully considered by the United States Patent and Trademark Office during the examination of this application;

3. The citations for the information be printed on any patent which issues from this application.

By submitting this Information Disclosure Statement, the undersigned makes no representation that a search has been performed, of the extent of any search performed, or that more relevant information does not exist.

By submitting this Information Disclosure Statement, the undersigned makes no representation that the information cited in the Statement is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b).

By submitting this Information Disclosure Statement, the undersigned makes no representation that the information cited in the Statement is, or is considered to be, in fact, prior art as defined by 35 U.S.C. § 102.

Notwithstanding any statements by the undersigned, the Examiner is urged to form his or her own conclusion regarding the relevance of the cited information.

An early and favorable action is hereby requested.

The Director is hereby authorized to charge any deficiency or credit any overpayment in the fees occasioned by the filing of this Information Disclosure Statement to our Deposit Account No. 23/2825 under Docket No. A0863.70051US04 from which the undersigned is authorized to draw.

Respectfully submitted,

By: /Edmund J. Walsh/
Edmund J. Walsh, Reg. No. 32,950
Wolf, Greenfield & Sacks, P.C.
600 Atlantic Avenue
Boston, Massachusetts 02210-2206
Telephone: (617) 646-8000

Docket No.: A0863.70051US04
Date: October 5, 2016
xNDDx

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/065,683	03/09/2016	Donald W. Milbrand JR.	A0863.70051US04	5112

23628 7590 06/05/2017
WOLF GREENFIELD & SACKS, P.C.
600 ATLANTIC AVENUE
BOSTON, MA 02210-2206

EXAMINER
FIGUEROA, FELIX O

ART UNIT	PAPER NUMBER
2833	

NOTIFICATION DATE	DELIVERY MODE
06/05/2017	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

Patents_eOfficeAction@WolfGreenfield.com
WGS_eOfficeAction@WolfGreenfield.com

Office Action Summary	Application No. 15/065,683	Applicant(s) MILBRAND ET AL.	
	Examiner FELIX O. FIGUEROA	Art Unit 2833	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-22* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-22* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

DETAILED ACTION

Notice of Pre-AIA or AIA Status

The present application is being examined under the pre-AIA first to invent provisions.

Information Disclosure Statement

The information disclosure statement filed 3/20/2016 fails to comply with 37 CFR 1.98(a)(1), which requires the following: (1) a list of all patents, publications, applications, or other information submitted for consideration by the Office; (2) U.S. patents and U.S. patent application publications listed in a section separately from citations of other documents; (3) the application number of the application in which the information disclosure statement is being submitted on each page of the list; (4) a column that provides a blank space next to each document to be considered, for the examiner's initials; and (5) a heading that clearly indicates that the list is an information disclosure statement. The information disclosure statement has been placed in the application file, but the information referred to therein has not been considered.

Claim Rejections - 35 USC § 103

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject

matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-22 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Fogg et al. (US 6,582,244) in view of Cohen et al. (US 7,753,731).

Fogg discloses a receptacle adapted for mounting to a printed circuit board, comprising: a housing (150) having a cavity (202) bounded by a first surface (206) and an opposing second surface (208); a first lead assembly including a first plurality of conductive elements (302) disposed in a first housing member; a second lead assembly including a second plurality of conductive elements (304) disposed in a second housing member, each conductive element of the first and second pluralities of conductive elements comprising a contact tail (312, 314) adapted for attachment to the printed circuit board, a mating contact portion (at 302, 304) and an intermediate portion (not shown, inside 300, Fig. 9) coupling the contact tail to the mating contact portion, wherein the mating contact portions of the first plurality of conductive elements are disposed along the first surface of the cavity and the mating contact portions of the second plurality of conductive elements are disposed along the second surface of the cavity (Fig. 13). Fogg discloses substantially the claimed invention except for an insert disposed between the first and second lead assemblies.

Cohen teaches (in Fig. 4) the use of an insert (160) disposed between the first and second lead assemblies. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use an insert, as taught by Cohen, in order to provide the desired shielding and reduce crosstalk between the lead assemblies/rows.

Regarding claim 2, Cohen teaches the insert including an electrically lossy material.

Regarding claim 3, Cohen teaches the insert contacting selected ones of the conductive elements.

Regarding claim 4, Cohen teaches the insert including projections towards selected ones of the conductive elements.

Regarding claim 5, Cohen teaches at least one of the first and second housing members including one or more slots for receiving the projections of the insert.

Regarding claim 6, Fogg discloses the contact tails and the mating contact portions disposed at right angles.

Regarding claim 7, Fogg discloses the first plurality of conductive elements and the second plurality of conductive elements forming rows of contacts on the first and second surfaces, respectively, of the cavity.

Regarding claim 8, Fogg discloses the first and second surfaces of the cavity include slots configured to receive the conductive elements of the first plurality of conductive elements and the second plurality of conductive elements, respectively.

Regarding claim 9, Fogg discloses the first and second surfaces of the cavity are parallel.

Regarding claim 10, Fogg, as modified by Cohen, discloses the first plurality of conductive elements is molded in the first housing member, and the second plurality of conductive elements is molded in the second housing member.

Regarding claim 11, Fogg, as modified by Cohen, discloses the housing, the first housing member and the second housing member made of an insulative material.

Regarding claim 12, Fogg discloses the housing includes at least one projection from a lower surface thereof.

Regarding claim 13, Fogg discloses a shell (10) adapted for attachment of the housing to the printed circuit board.

Regarding claim 14, Fogg discloses the housing further comprises a second cavity (204) bounded by a third surface (210) and an opposing fourth surface (212), further comprising a third lead assembly including a third plurality of conductive elements (306) disposed in a third housing member and a fourth lead assembly including a fourth plurality of conductive elements (308) disposed in a fourth housing member, each conductive element of the third and fourth pluralities of conductive elements comprising a contact tail adapted for attachment to the printed circuit board, a mating contact portion and an intermediate portion coupling the contact tail to the mating contact portion, wherein the mating contact portions of the third plurality of conductive elements are disposed along the third surface of the second cavity and the mating contact portions of the fourth plurality of conductive elements are disposed along the fourth surface of the second cavity.

Regarding claim 15, Fogg, as modified by Cohen, discloses that for each conductive element of a first subset of the first plurality of conductive elements, a portion of the conductive element is exposed through the first housing member, and for each conductive element of a second subset of the second plurality of conductive

elements, a portion of the conductive element is exposed through the second housing member.

Regarding claim 16, Cohen discloses a first surface of the insert comprising a first plurality of projections, each projection of the first plurality of projections being coupled to a conductive element of the first subset; and a second surface of the insert comprises a second plurality of projections, each projection of the second plurality of projections being coupled to a conductive element of the second subset.

Regarding claim 17, Cohen discloses the first plurality of conductive elements comprising conductive elements disposed in a plurality of pairs of conductive elements; and the first subset of the first plurality of conductive elements comprises conductive elements each of which is disposed adjacent a pair of the plurality of pairs.

Regarding claim 18, Cohen teaches the insert including a conductive material.

Regarding claim 19, Cohen teaches the insert being at least partially conductive.

Regarding claim 20, Cohen teaches the insert including an electrically lossy material; and the electrically lossy material is electrically coupled to selected ones of the first plurality of conductive elements and the second plurality of conductive elements.

Regarding claim 21, Fogg, as modified by Cohen, discloses the first plurality of conductive elements positioned in a first row, the first row comprising pairs of the first plurality of conductive elements separated by single conductive elements of the first plurality of conductive elements; the second plurality of conductive elements positioned in a second row, the second row comprising pairs of the second plurality of conductive elements separated by single conductive elements of the second plurality of conductive

elements; and the electrically lossy material is selectively electrically coupled to the single conductive elements of the first plurality of conductive elements and second plurality of conductive elements.

Regarding claim 22, Cohen discloses the insert includes projections towards the selected ones of the conductive elements.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to FELIX O. FIGUEROA whose telephone number is (571)272-2003. The examiner can normally be reached on Mon.-Fri., 10:00am-6:00pm.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Renee Luebke can be reached on (571) 272-2009. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/FELIX O. FIGUEROA/
Primary Examiner
Art Unit 2833

FORM PTO-1449/A and B (modified PTO/SB/08)				APPLICATION NO.: 15/065,683	ATTY. DOCKET NO.: A0863.70051US04
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				FILING DATE: March 9, 2016	CONFIRMATION NO.: 5112
				FIRST NAMED INVENTOR: Donald W. Milbrand, Jr.	
Sheet	1	of	7	GROUP ART UNIT: 2833	EXAMINER: Not Yet Assigned

U.S. PATENT DOCUMENTS

Examiner's Initials #	Cite No.	U.S. Patent Document Number	U.S. Patent Document Kind Code	Name of Patentee or Applicant of Cited Document	Date of Publication or Issue of Cited Document MM-DD-YYYY
		2,996,710		Pratt	08-15-1961
		3,002,162		Garstang	09-26-1961
		3,134,950		Cook	05-26-1964
		3,322,885		May et al.	05-30-1967
		3,786,372		Epis et al.	01-15-1974
		3,825,874		Peverill	07-23-1974
		3,863,181		Glance et al.	01-28-1975
		4,155,613		Brandeau	05-22-1979
		4,195,272		Boutros	03-25-1980
		4,276,523		Boutros et al.	06-30-1981
		4,371,742		Manly	02-01-1983
		4,408,255		Adkins	10-04-1983
		4,447,105		Ruehl	05-08-1984
		4,471,015		Ebneth et al.	09-11-1984
		4,484,159		Whitley	11-20-1984
		4,490,283		Kleiner	12-25-1984
		4,518,651		Wolfe, Jr.	05-21-1985
		4,519,664		Tillotson	05-28-1985
		4,519,665		Althouse et al.	05-28-1985
		4,636,752		Saito	01-13-1987
		4,682,129		Bakermans et al.	07-21-1987
		4,751,479		Parr	06-14-1988
		4,761,147		Gauthier	08-02-1988
		4,846,724		Sasaki et al.	07-11-1989
		4,878,155		Conley	10-31-1989
		4,948,922		Varadan et al.	08-14-1990
		4,970,354		Iwasa et al.	11-13-1990
		4,992,060		Meyer	02-12-1991
		5,000,700		Masubuchi et al.	03-19-1991
		5,141,454		Garrett et al.	08-25-1992
		5,150,086		Ito	09-22-1992
		5,168,252		Naito	12-01-1992
		5,168,432		Murphy et al.	12-01-1992

EXAMINER:	DATE CONSIDERED:

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

*a copy of this reference is not provided as it was previously cited by or submitted to the office in a prior application, Serial No. 13/683,295, filed November 21, 2012, and relied upon for an earlier filing date under 35 U.S.C. 120 (continuation, continuation-in-part, and divisional applications).

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /F.O.F/

FORM PTO-1449/A and B (modified PTO/SB/08)	APPLICATION NO.: 15/065,683	ATTY. DOCKET NO.: A0863.70051US04
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	FILING DATE: March 9, 2016	CONFIRMATION NO.: 5112
	FIRST NAMED INVENTOR: Donald W. Milbrand, Jr.	
Sheet 2 of 7	GROUP ART UNIT: 2833	EXAMINER: Not Yet Assigned

		5,266,055		Naito et al.	11-30-1993
		5,280,257		Cravens et al.	01-18-1994
		5,287,076		Johnescu et al.	02-15-1994
		5,340,334		Nguyen	08-23-1994
		5,346,410		Moore, Jr.	09-13-1994
		5,456,619		Belopolsky et al.	10-10-1995
		5,461,392		Mott et al.	10-24-1995
		5,499,935		Powell	03-19-1996
		5,551,893		Johnson	09-03-1996
		5,562,497		Yagi et al.	10-08-1996
		5,597,328		Mouissie	01-28-1997
		5,651,702		Hanning et al.	07-29-1997
		5,669,789		Law	09-23-1997
		5,796,323		Uchikoba et al.	08-18-1998
		5,831,491		Buer et al.	11-03-1998
		5,924,899		Paagman	07-20-1999
		5,981,869		Kroger	11-09-1999
		5,982,253		Perrin et al.	11-09-1999
		6,019,616		Yagi et al.	02-01-2000
		6,152,747		McNamara	11-28-2000
		6,168,469		Lu	01-02-2001
		6,174,203		Asao	01-16-2001
		6,174,944		Chiba et al.	01-16-2001
		6,217,372	B1	Reed	04-17-2001
		6,299,483	B1	Cohen et al.	10-09-2001
		6,328,601	B1	Yip et al.	12-11-2001
		6,347,962	B1	Kline	02-19-2002
		6,350,134	B1	Fogg et al.	02-26-2002
		6,364,711	B1	Berg et al.	04-02-2002
		6,375,510	B2	Asao	04-23-2002
		6,379,188	B1	Cohen et al.	04-30-2002
		6,398,588	B1	Bickford	06-04-2002
		6,409,543	B1	Astbury, Jr. et al.	06-25-2002
		6,482,017	B1	Van Doorn	11-19-2002
		6,503,103	B1	Cohen et al.	01-07-2003
		6,506,076	B2	Cohen et al.	01-14-2003

EXAMINER:	DATE CONSIDERED:

[#] EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

*a copy of this reference is not provided as it was previously cited by or submitted to the office in a prior application, Serial No. 13/683,295, filed November 21, 2012, and relied upon for an earlier filing date under 35 U.S.C. 120 (continuation, continuation-in-part, and divisional applications).

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /F.O.F/

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT				FILING DATE: March 9, 2016	CONFIRMATION NO.: 5112
				FIRST NAMED INVENTOR: Donald W. Milbrand, Jr.	
Sheet	3	of	7	GROUP ART UNIT: 2833	EXAMINER: Not Yet Assigned

		6,517,360	B1	Cohen	02-11-2003
		6,530,790	B1	McNamara et al.	03-11-2003
		6,537,087	B2	McNamara et al.	03-25-2003
		6,554,647	B1	Cohen et al.	04-29-2003
		6,565,387	B2	Cohen	05-20-2003
		6,579,116	B2	Brennan et al.	06-17-2003
		6,582,244	B2	Fogg et al.	06-24-2003
		6,595,802	B1	Watanabe et al.	07-22-2003
		6,602,095	B2	Astbury, Jr. et al.	08-05-2003
		6,616,864	B1	Jiang et al.	09-09-2003
		6,652,318	B1	Winings et al.	11-25-2003
		6,655,966	B2	Rothermel et al.	12-02-2003
		6,709,294	B1	Cohen et al.	03-23-2004
		6,713,672	B1	Stickney	03-30-2004
		6,743,057	B2	Davis et al.	06-01-2004
		6,776,659	B1	Stokoe et al.	08-17-2004
		6,786,771	B2	Gailus	09-07-2004
		6,814,619	B1	Stokoe et al.	11-09-2004
		6,830,489	B2	Aoyama	12-14-2004
		6,872,085	B1	Cohen et al.	03-29-2005
		6,979,226	B2	Otsu et al.	12-27-2005
		7,044,794	B2	Consoli et al.	05-16-2006
		7,057,570	B2	Irion, II et al.	06-06-2006
		7,074,086	B2	Cohen et al.	07-11-2006
		7,094,102	B2	Cohen et al.	08-22-2006
		7,108,556	B2	Cohen et al.	09-19-2006
		7,163,421	B1	Cohen et al.	01-16-2007
		7,285,018	B2	Kenny et al.	10-23-2007
		7,335,063	B2	Cohen et al.	02-26-2008
		7,371,117	B2	Gailus	05-13-2008
		7,494,383	B2	Cohen et al.	02-24-2009
		7,540,781	B2	Kenny et al.	06-02-2009
		7,581,990	B2	Kirk et al.	09-01-2009
		7,588,464	B2	Kim	09-15-2009
		7,722,401	B2	Kirk et al.	05-25-2010
		7,731,537	B2	Amleshi et al.	06-08-2010

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /F.O.F/

FORM PTO-1449/A and B (modified PTO/SB/08)	APPLICATION NO.: 15/065,683	ATTY. DOCKET NO.: A0863.70051US04
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	FILING DATE: March 9, 2016	CONFIRMATION NO.: 5112
	FIRST NAMED INVENTOR: Donald W. Milbrand, Jr.	
Sheet 4 of 7	GROUP ART UNIT: 2833	EXAMINER: Not Yet Assigned

		7,753,731	B2	Cohen et al.	07-13-2010
		7,771,233	B2	Gailus	08-10-2010
		7,794,240	B2	Cohen et al.	09-14-2010
		7,874,873	B2	Do et al.	01-25-2011
		7,887,371	B2	Kenny et al.	02-15-2011
		7,906,730	B2	Atkinson et al.	03-15-2011
		7,914,304	B2	Cartier et al.	03-29-2011
		8,083,553	B2	Manter et al.	12-27-2011
		8,182,289	B2	Stokoe et al.	05-22-2012
		8,215,968	B2	Cartier et al.	07-10-2012
		8,272,877	B2	Stokoe et al.	09-25-2012
		8,371,875	B2	Gailus	02-12-2013
		8,382,524	B2	Khilchenko et al.	02-26-2013
		8,657,627	B2	McNamara et al.	02-25-2014
		8,715,003	B2	Buck et al.	05-06-2014
		8,771,016	B2	Atkinson et al.	07-08-2014
		8,864,521	B2	Atkinson et al.	10-21-2014
		8,926,377	B2	Kirk et al.	01-06-2015
		8,944,831	B2	Stoner et al.	02-03-2015
		8,998,642	B2	Manter et al.	04-07-2015
		9,004,942	B2	Paniauqa	04-14-2015
		9,022,806	B2	Cartier, Jr. et al.	05-05-2015
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		9,219,335	B2	Atkinson et al.	12-22-2015
		9,225,085	B2	Cartier, Jr. et al.	12-29-2015
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		2002-0089464	A1	Joshi	07-11-2002
		2002-0098738	A1	Astbury et al.	07-25-2002
		2002-0111068	A1	Cohen et al.	08-15-2002
		2002-0111069	A1	Astbury et al.	08-15-2002
		2004-0020674	A1	McFadden et al.	02-05-2004
		2004-0115968	A1	Cohen	06-17-2004
		2004-0121652	A1	Gailus	06-24-2004
		2004-0196112	A1	Welbon et al.	10-07-2004

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	FIRST NAMED INVENTOR: Donald W. Milbrand, Jr.	
Sheet 5 of 7	GROUP ART UNIT: 2833	EXAMINER: Not Yet Assigned

		2004-0259419	A1	Payne et al.	12-23-2004
		2005-0070160	A1	Cohen et al.	03-31-2005
		2005-0133245	A1	Katsuyama et al.	06-23-2005
		2005-0176835	A1	Kobayashi et al.	08-11-2005
		2005-0283974	A1	Richard et al.	12-29-2005
		2005-0287869	A1	Kenny et al.	12-29-2005
		2006-0068640	A1	Gailus	03-30-2006
		2007-0004282	A1	Cohen et al.	01-04-2007
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		2007-0042639	A1	Manter et al.	02-22-2007
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		2008-0194146	A1	Gailus	08-14-2008
		2008-0246555	A1	Kirk et al.	10-09-2008
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		2010-0081302	A1	Atkinson et al.	04-01-2010
		2010-0273359	A1	Walker et al.	10-28-2010
		2010-0294530	A1	Atkinson et al.	11-25-2010
		2011-0003509	A1	Gailus	01-06-2011
		2011-0104948	A1	Girard, Jr. et al.	05-05-2011
		2011-0212649	A1	Stokoe et al.	09-01-2011
		2011-0212650	A1	Amleshi et al.	09-01-2011
		2011-0230095	A1	Atkinson et al.	09-22-2011
		2011-0230096	A1	Atkinson et al.	09-22-2011
		2011-0287663	A1	Gailus et al.	11-24-2011
		2012-0094536	A1	Khilchenko et al.	04-19-2012

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Sheet	6	of	7	GROUP ART UNIT: 2833	EXAMINER: Not Yet Assigned

		2012-0156929	A1	Manter et al.	06-21-2012
		2012-0202363	A1	McNamara et al.	08-09-2012
		2012-0202386	A1	McNamara et al.	08-09-2012
		2012-0214344	A1	Cohen et al.	08-23-2012
		2013-0012038	A1	Kirk et al.	01-10-2013
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		2013-0078870	A1	Milbrand, Jr.	03-28-2013
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		2015-0056856	A1	Atkinson et al.	02-26-2015
		2015-0236451	A1	Cartier, Jr. et al.	08-20-2015
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		2015-0255926	A1	Paniagua	09-10-2015

FOREIGN PATENT DOCUMENTS

Examiner's Initials #	Cite No.	Foreign Patent Document			Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Translation (Y/N)
		Office/ Country	Number	Kind Code			
	*	EP	1 779 472	A1	Amphenol Corp.	05-02-2007	
	*	EP	2 169 770	A2	Amphenol Corporation	03-31-2010	
	*	GB	1272347	A	Amp Inc.	04-26-1972	
	*	JP	07302649	A	Framatome Connectors Int	11-14-1995	Y – Abstract Only
	*	WO	88/05218	A1	Amp Inc.	07-14-1988	
	*	WO	2004/059794	A2	Teradyne, Inc.	07-15-2004	
	*	WO	2004/059801	A1	Teradyne, Inc.	07-15-2004	
	*	WO	2006/039277	A1	Teradyne, Inc.	04-13-2006	
	*	WO	2007/005597	A2	Amphenol Corporation	01-11-2007	
	*	WO	2007/005599	A1	Amphenol Corporation	01-11-2007	
	*	WO	2008/124057	A1	Amphenol Corporation	10-16-2008	
	*	WO	2010/039188	A1	Amphenol Corporation	04-08-2010	

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				FIRST NAMED INVENTOR: Donald W. Milbrand, Jr.	
Sheet	7	of	7	GROUP ART UNIT: 2833	EXAMINER: Not Yet Assigned

OTHER ART – NON PATENT LITERATURE DOCUMENTS

Examiner's Initials #	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	Translation (Y/N)
	*	Extended European Search Report mailed January 24, 2012 for Application No. EP 11166820.8.	
	*	International Search Report and Written Opinion mailed January 26, 2006 for Application No. PCT/US2005/034605.	
	*	International Search Report with Written Opinion mailed October 31, 2007 for Application No. PCT/US2006/025562.	
	*	International Search Report and Written Opinion mailed March 14, 2011 for Application No. PCT/US2010/056482 (A0863.70049WO00).	
	*	International Preliminary Report on Patentability mailed May 24, 2012 for Application No. PCT/US2010/056482 (A0863.70049WO00).	
	*	International Search Report and Written Opinion mailed November 22, 2011 for Application No. PCT/US2011/026139 (A0863.70055WO00).	
	*	International Preliminary Report on Patentability mailed September 7, 2012 for Application No. PCT/US2011/026139 (A0863.70055WO00).	
	*	International Search Report and Written Opinion mailed July 28, 2011 for Application No. PCT/US2011/034747 .	
	*	International Search Report and Written Opinion mailed September 12, 2012 for Application No. PCT/US2012/023689 (A0863.70061WO00).	
	*	International Preliminary Report on Patentability mailed August 15, 2013 for Application No. PCT/US2012/023689 (A0863.70061WO00).	
	*	International Search Report and Written Opinion mailed March 29, 2013 for Application No. PCT/US2012/060610 (A0863.70066WO00).	
		International Search Report and Written Opinion mailed May 13, 2015 for Application No. PCT/US2015/012463 (A0863.70078WO00).	
	*	[NO AUTHOR LISTED], Carbon Nanotubes For Electromagnetic Interference Shielding. SBIR/STTR. Award Information. Program Year 2001. Fiscal Year 2001. Materials Research Institute, LLC. Chu et al. Available at http://sbir.gov/sbirsearch/detail/225895. Last accessed 9/19/13.	
	*	BEAMAN, High Performance Mainframe Computer Cables. 1997 Electronic Components and Technology Conference. 1997;911-7.	
	*	SHI et al, Improving Signal Integrity In Circuit Boards By Incorporating Absorbing Materials. 2001 Proceedings. 51st Electronic Components and Technology Conference, Orlando FL. 2001:1451-56.	

[NOTE – No copies of U.S. patents, published U.S. patent applications, or pending, unpublished patent applications stored in the USPTO's Image File Wrapper (IFW) system, are included. See 37 CFR § 1.98 and 1287OG163. Copies of all other patent(s), publication(s), unpublished, pending U.S. patent applications, or other information listed are provided as required by 37 CFR § 1.98 unless 1) such copies were provided in an IDS in an earlier application that complies with 37 CFR § 1.98, and 2) the earlier application is relied upon for an earlier filing date under 35 U.S.C. § 120.]

EXAMINER:	DATE CONSIDERED:
/FELIX O FIGUEROA/	05/30/2017

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT				FILING DATE: March 9, 2016	CONFIRMATION NO.: 5112
				FIRST NAMED INVENTOR: Donald W. Milbrand	
Sheet	1	of	1	GROUP ART UNIT: 2833	EXAMINER: Felix O. Figueroa

U.S. PATENT DOCUMENTS

Examiner's Initials #	Cite No.	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication or Issue of Cited Document MM-DD-YYYY
		Number	Kind Code		
		6,565,387	B2	Cohen	05-20-2003
		9,300,074	B2	Gailus	03-29-2016
		9,450,344	B2	Cartier, Jr. et al.	09-20-2016
		2010-0099299	A1	Moriyama et al.	04-22-2010
		2012-0077380	A1	Minich et al.	03-29-2012
		2013-0217263	A1	Pan	08-22-2013
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FOREIGN PATENT DOCUMENTS

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/FELIX O FIGUEROA/	05/30/2017

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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15065683	MILBRAND ET AL.
	Examiner	Art Unit
	FELIX O FIGUEROA	2833

CPC- SEARCHED		
Symbol	Date	Examiner
H01R13/65807*, H01R13/6587*, H01R13/6586, H01R13/6585*, H01R13/658, H01R13/646, H01R13/6471	5/30/2017	FF

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
439	607.02, 607.03, 607.05, 607.06, 607.08, 607.1	5/30/2017	FF

SEARCH NOTES		
Search Notes	Date	Examiner
EAST search including US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB		FF
Inventor name search	5/30/2017	FF

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

Docket No.: A0863.70051US04
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor:	Donald W. Milbrand, Jr.
Application No.:	15/065,683
Confirmation No.:	5112
Filed:	March 9, 2016
For:	HIGH PERFORMANCE CABLE CONNECTOR
Examiner:	F. O. Figueroa
Art Unit:	2833

Certificate of Electronic Filing under 37 CFR §1.8
I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being transmitted via the Office's electronic filing system in accordance with 37 CFR § 1.6(a)(4).

Dated: November 6, 2017 Electronic Signature: /Trish McDonald/

AMENDMENT IN RESPONSE TO NON-FINAL OFFICE ACTION UNDER 37 C.F.R. § 1.111

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

INTRODUCTORY COMMENTS

In response to the Office Action dated June 5, 2017, please amend the above-identified U.S. patent application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 8 of this paper.

FORM PTO-1449/A and B (modified PTO/SB/08)				APPLICATION NO.: 15/065,683	ATTY. DOCKET NO.: A0863.70051US04
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				FILING DATE: March 09, 2016	CONFIRMATION NO.: 5112
				FIRST NAMED INVENTOR: Donald W. Milbrand	
Sheet	1	of	1	GROUP ART UNIT: 2833	EXAMINER: Felix O. Figueroa

U.S. PATENT DOCUMENTS

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		Number	Kind Code		
		2009-0061661	A1	Shuey et al.	03-05-2009

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		Office/ Country	Number	Kind Code			
		CN	101790818	A	Framatome Connectors Int	07-28-2010	Y-abstract only
		CN	102239605	A	Amphenol Corp.	11-09-2011	Y-abstract only

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5750185.1

DOCKET NO.: A0863.70051US04

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor:	Donald W. Milbrand
Application No.:	15/065,683
Confirmation No.:	5112
Filed:	March 09, 2016
For:	HIGH PERFORMANCE CABLE CONNECTOR
Examiner:	Felix O. Figueroa
Art Unit:	2833

CERTIFICATE OF ELECTRONIC FILING UNDER 37 C.F.R. § 1.8

The undersigned hereby certifies that this paper, along with any paper referred to as being attached or enclosed, is being transmitted via the Office electronic filing system in accordance with § 1.6(a)(4), on the 6th day of November, 2017.

Electronic Signature: /Trish McDonald/

MAIL STOP AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

STATEMENT FILED PURSUANT TO THE DUTY OF DISCLOSURE UNDER 37 C.F.R. §§ 1.56, 1.97 AND 1.98

Sir:

Pursuant to the duty of disclosure under 37 C.F.R. §§ 1.56, 1.97 and 1.98, the undersigned requests consideration of this Information Disclosure Statement.

PART I: Compliance with 37 C.F.R. § 1.97

This Information Disclosure Statement has been filed more than three months after the filing date of this application and after the mailing date of a first Office Action, but before the mailing date of any of a Final Action under 37 C.F.R. § 1.113, a Notice of Allowance under 37 C.F.R. § 1.311, or an action that otherwise closes prosecution in this application.

Please charge our Credit Card in the amount of $180.00 covering the fee set forth in 37 C.F.R. § 1.17(p).

PART II: Information Cited

The undersigned hereby makes of record in the above-identified application the information listed on the attached form PTO-1449 (modified PTO/SB/08). The order of presentation of the references should not be construed as an indication of the importance of the references.

The undersigned hereby makes the following additional information of record in the above-identified application.

The undersigned would like to bring to the Examiner's attention the following applications that may contain subject matter related to this application:

Serial No.	Filing Date	Inventor(s)	Docket No.
*15/645,931	07-10-2017	Atkinson et al.	A0863.70041US05

*A copy of this reference is not provided as the Office has waived the requirement under 37 C.F.R. § 1.98(a)(2)(iii) for submitting a copy of a cited U.S. patent application if it is scanned to the Image File Wrapper system and is available on Private PAIR.

The above-identified application may include subject matter that is technically-related to subject matter of the present application and may contain claims that recite elements similar to those recited in claims of the present application. In handling prosecution of the above-identified application, the Examiner for this other application presumably will search for relevant prior art and, in some circumstances, may take positions about the prior art and/or the interpretation of the claims that may be material to the examination of the present application.

Accordingly, the Examiner in the present application is requested to review the file history of the above-identified co-pending application to see whether there is any information that the Examiner believes may be relevant to the prosecution of the present application. It is assumed that the Examiner has access to the file history of the above-identified application. However, if the Examiner would like copies of any or all of the information included in the file history of the above-identified application, the Examiner is asked to contact the undersigned representative.

PART III: Remarks

Documents cited anywhere in the Information Disclosure Statement are enclosed unless otherwise indicated. It is respectfully requested that:

1. The Examiner consider completely the cited information, along with any other information, in reaching a determination concerning the patentability of the present claims;

2. The enclosed form PTO-1449 (modified PTO/SB/08) be signed by the Examiner to evidence that the cited information has been fully considered by the United States Patent and Trademark Office during the examination of this application;

3. The citations for the information be printed on any patent which issues from this application.

By submitting this Information Disclosure Statement, the undersigned makes no representation that a search has been performed, of the extent of any search performed, or that more relevant information does not exist.

By submitting this Information Disclosure Statement, the undersigned makes no representation that the information cited in the Statement is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b).

By submitting this Information Disclosure Statement, the undersigned makes no representation that the information cited in the Statement is, or is considered to be, in fact, prior art as defined by 35 U.S.C. § 102.

Notwithstanding any statements by the undersigned, the Examiner is urged to form his or her own conclusion regarding the relevance of the cited information.

An early and favorable action is hereby requested.

The Director is hereby authorized to charge any deficiency or credit any overpayment in the fees occasioned by the filing of this Information Disclosure Statement to our Deposit Account No. 23/2825 under Docket No. A0863.70051US04 from which the undersigned is authorized to draw.

Respectfully submitted,

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Mezzanine-type electrical connectors

Inventor(s):	SHUEY JOSEPH B; JOHNSON LEWIS R; GRAY MARK R ± (SHUEY JOSEPH B, ; JOHNSON LEWIS R, ; GRAY MARK R)
Applicant(s):	FRAMATOME CONNECTORS INT ± (FRAMATOME CONNECTORS INT)
Classification:	**- international:** ***H01R12/00*** **- cooperative:** **H01R23/27**; H01R12/716
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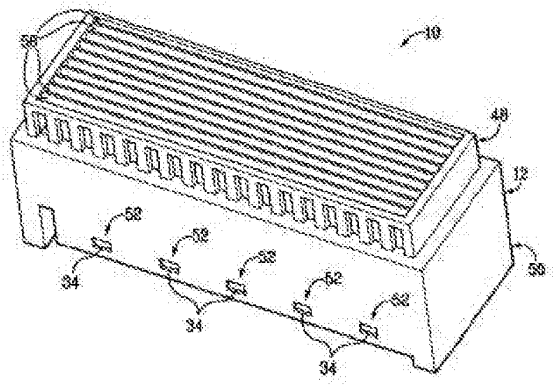
Abstract of CN101790818 (A)

Embodiments of electrical connectors include substantially identical first and second halves. The first and second halves each include insert molded leadframe assemblies that comprise electrical conductors. Each electrical conductor of the first half engages a substantially identical electrical conductor of the second half when the first and second halves are mated.



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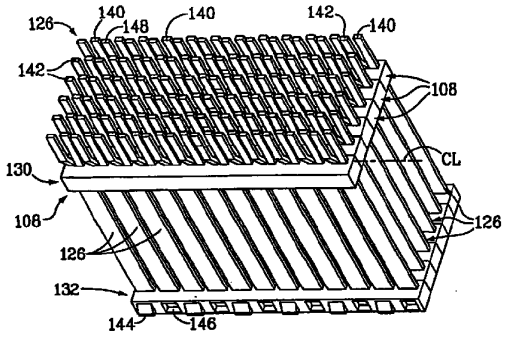
(54)发明名称

夹层型电连接器

(57)摘要

电连接器的实施方式包括基本相同的第一和第二半部。第一和第二半部每个都包括嵌件成型而成的引线框组件，所述组件包含电导体。当第一和第二半部配合时，第一半部的每个电导体可与第二半部基本上相同的电导体啮合。



CN 101790818 A

1. 一种电连接器，包含：

第一半部，所述第一半部包含第一电导体，

其中第一电导体包含两个形状不同的接触梁，并且第一半部构造成与相同的第一半部配合。

2. 一种电连接器，包含：

第一半部；以及

能与第一半部配合的第二半部，

其中第一半部包含第一电导体，第二半部包含与第一电导体基本相同的第二电导体，第一电导体包含两个形状不同的接触梁，第二电导体包含与第一电导体相同的两个形状不同的接触梁，第一电导体和第二电导体彼此相配合。

3. 如权利要求 1 和 2 所述的电连接器，其中：

第一电导体进一步包含引线部分；以及

两个形状不同的接触梁中的第一个基本是直的，而两个形状不同的接触梁中的第二个相对于第一电导体的引线部分的纵轴成一定角度或偏离所述纵轴。

4. 如权利要求 1 和 2 所述的电连接器，其中：

第一电导体进一步包含引线部分、与引线部分电接触的柱、以及安装在所述柱上的第一可熔元件。

5. 如权利要求 1 和 2 所述的电连接器，进一步包含第一框架，其能够承载第一导电体和第二框架，其中第一框架包含凹进，第二框架包含配合入凹进的突起。

6. 如权利要求 1 和 2 所述的电连接器，其中第一电导体由第一框架承载，第一框架包含凹穴，第一可熔元件的至少一部分被放置在所述凹穴内。

7. 如权利要求 1 和 2 所述的电连接器，其中多个第一电导体由第一框架承载，并且相对彼此排成直线。

8. 如权利要求 1 和 2 所述的电连接器，其中两个第一电导体每个都具有相同的可偏斜及不可偏斜的梁，并且两个第一电导体彼此配合。

9. 如权利要求 1 和 2 所述的电连接器，其中第一半部包含仅位于第一半部一侧上的导引销。

10. 如权利要求 1 和 2 所述的电连接器，其中第一半部包含位于第一半部另一侧上的导引销孔。

11. 如权利要求 1 和 2 所述的电连接器，其中第一半部包含仅位于第一半部一侧上的导引销，且导引销可从第一半部上移除。

12. 如权利要求 1 和 2 所述的电连接器，进一步包含仅位于第一半部一侧上的导引销和仅位于第一半部相反一侧上的导引销孔。

13. 一种含有第一半部的电连接器，其中：

第一半部包含位于第一半部一侧上的导引销和位于第一半部另一侧上的导引销孔。

14. 如权利要求 13 所述的电连接器，其中第一半部的另一侧与所述一侧相反。

15. 一种电连接器部分，包含：

第一壳体；以及

电导体阵列，其中，部分电导体阵列沿着公共中线设置，沿着中线设置的电导体阵列的

第一部分包含第一匹配端，沿着中线设置的电导体阵列的最后一部分包含第二匹配端，所述第二匹配端与第一匹配端体形不同。

夹层型电连接器

技术领域

[0001] 本发明涉及一种用于连接第一和第二电器，比如第一和第二电路衬底的电连接器。

背景技术

[0002] 夹层型 (mezzanine-type) 电连接器可包含壳体，多个电导体，和多个易熔元件，比如安装在电导体上的焊料球。

[0003] Roath 的美国专利 No.5,098,311 公开了无极性 (hermaphroditic) 的半连接器。

发明内容

[0004] 电连接器的实施方式可包括基本上相同的第一和第二半部。第一和第二半部每个包括具有电导体的嵌件成型引线框组件 (insert moldedleadframe assemblies)。当第一和第二半部配合时，第一半部的每个电导体可与基本上相同的第二半部的电导体啮合。

[0005] 电连接器实施方式可包括第一半部。第一半部可包括第一电导体。第一电导体可包括两个形状不同的接触梁。第一半部构造成与相同的第一半部配合。第二半部也可以与第一半部配合。第一半部可包括第一电导体。第二半部可包括与第一电导体基本相同的第二电导体。第一电导体可包括两个形状不同的接触梁，比如可偏斜接触梁和不可偏斜接触梁。第二电导体可与第一电导体相同，并可包括同样的两个形状不同的接触梁，比如可偏斜接触梁和不可偏斜接触梁。第一电导体和第二电导体可彼此配合。

[0006] 第一电导体可包括引线部分。两个形状不同的接触梁中的第一个基本是直的，而两个形状不同的接触梁中的第二个可以是相对第一电导体引线部分纵轴成一定角度或偏离该轴的。第一电导体可包括引线部分、与引线部分电接触的柱、以及安装在所述柱上的第一可熔元件。第一框架能够承载第一导电体和第二框架。第一框架可包括凹进，第二框架可包括配合进凹进内的突起。第一电导体可由第一框架承载，第一框架可包含凹穴，第一可熔元件的至少一部分可被放置在所述凹穴内。

[0007] 多个第一电导体可由第一框架承载，并且可相对彼此排成直线。两个第一电导体可彼此配合。第一半部可包括导引销，导引销仅位于第一半部的一侧。第一半部可包括导引销孔，导引销孔位于第一半部的另一侧。导引销可以从第一半部上移除。导引销孔可仅被放置在第一半部的对侧上。

[0008] 电导体的实施方式可包括第一半部，其中第一半部可包括位于第一半部一侧上的导引销和位于第一半部另一侧上的导引销孔。该导引销可以从第一半部上移除。第一半部的另一侧可与所述一侧相对设置。

[0009] 第一半部可构造成安装到第一表面上，而基本相同的第二半部可构造成安装在第二表面上且可与第一半部配合。第一和第二半部每个都可包括壳体和安装在壳体内的嵌件成型引线框组件，其中成型引线框组件包括第一和第二电导体。当第一和第二半部配合的时候，第一半部第一电导体的第一接触梁可以与第二半部电导体的第二接触梁啮合。当第

一和第二半部配合的时候，第一半部电导体的第二接触梁可以与第二半部电导体的第一接触梁啮合。

附图说明

[0010] 对前面的概述以及接下来对优选实施方式的详细介绍进行阅读时，结合所附简图能获得更好的理解。为了解释说明本发明，附图画出的是优选呈现的实施方式。但是，本发明并不限于在附图中所公开的特定技术手段。在附图中：

[0011] 图 1 是电连接器的顶部透视图；

[0012] 图 2 是图 1 所示电连接器的嵌件成型引线框组件的顶部透视图；

[0013] 图 3 是图 1 和 2 中所示的连接器的俯视图；

[0014] 图 4 是图 1-3 中所示的连接器的侧视图；

[0015] 图 5 是图 1-4 中所示的连接器的仰视图；

[0016] 图 6 是图 1-5 中所示的连接器的侧视图，其中视角与图 4 的视角相比旋转了接近九十度；

[0017] 图 7 是图 2 中所示的嵌件成型引线框组件之一的俯视图；

[0018] 图 8 是图 2 和 7 中所示的嵌件成型引线框组件的侧视图；

[0019] 图 9 是图 2，7 和 8 中所示的嵌件成型引线框组件的仰视图；

[0020] 图 10 是图 2 和 7-9 中所示的嵌件成型引线框组件的侧视图，其中视角与图 8 的视角相比旋转了接近九十度；

[0021] 图 11 是图 2 和 7-10 中所示的嵌件成型引线框组件的底部透视图；

[0022] 图 12 是图 11 中标为“A”的区域的放大图，画出了不带焊料球的嵌件成型引线框组件；

[0023] 图 13 是图 11 中标为“A”的区域的放大图，画出了带焊料球的嵌件成型引线框组件；

[0024] 图 14 是图 2 和 7-13 中所示的嵌件成型引线框组件的顶部透视图；

[0025] 图 15 是图 14 中标为“B”的区域的放大图；

[0026] 图 16 是图 1 中所示电连接器替换实施方式的顶部透视图；

[0027] 图 17 是图 16 中所示连接器的底部透视图；

[0028] 图 18 是图 16 和 17 中所示连接器的仰视图；

[0029] 图 19 是图 16-18 中所示连接器的底部透视图；

[0030] 图 20 是图 16-19 中所示连接器的侧视图；

[0031] 图 21 是图 16-20 中所示连接器的侧视图，其中视角与图 20 的视角相比旋转了接近九十度；

[0032] 图 22 是图 1 中所示电连接器另一替换实施方式的顶部透视图，画出了连接器的第一和第二半部部分配合的情况；

[0033] 图 23 是图 22 中所示连接器第一半部的顶部透视图；

[0034] 图 24 是图 22 和 23 中所示连接器的侧视图，画出了连接器的第一和第二半部完全配合的情况；

[0035] 图 25 是图 24 中标为“C”的区域的放大图，其中连接器的第一和第二半部的壳体

被制成透明的以便显露出壳体内配合的电导体；

[0036] 图 26 是图 22-25 中所示连接器的第一半部的俯视图；

[0037] 图 27 是图 22-26 中所示连接器的侧视图，画出了连接器的第一和第二半部完全配合的情况，且其中视角与图 24 的视角相比旋转了接近九十度；

[0038] 图 28 是图 27 中标为“D”的区域的放大图，其中连接器的第一和第二半部的壳体被制成透明的以便显露出壳体内配合的电导体；

[0039] 图 29 是图 22-28 中所示连接器的嵌件成型引线框组件的顶部透视图；

[0040] 图 30 是图 29 中所示嵌件成型引线框组件的顶部透视图；

[0041] 图 31 是图 29 和 30 中所示嵌件成型引线框组件的电导体的顶部透视图；

[0042] 图 32 是图 1 中所示电连接器另一替换实施方式的顶部透视图，画出了连接器的第一和第二半部部分配合的情况；

[0043] 图 33 是图 22 中所示连接器第一半部的顶部透视图；

[0044] 图 34 是图 32 和 33 中所示连接器的侧视图，画出了连接器的第一和第二半部完全配合的情况；

[0045] 图 35 是图 34 中标为“E”的区域的放大图，其中连接器的第一和第二半部的壳体被制成透明的以便显露出壳体内配合的电导体；

[0046] 图 36 是图 32-35 中所示连接器第一半部的俯视图；

[0047] 图 37 是图 32-36 中所示连接器第一半部的侧视图；

[0048] 图 38 是图 32-37 中所示连接器第一半部的侧视图，其中视角与图 37 的视角相比旋转了接近九十度；

[0049] 图 39 是图 32-38 中所示连接器的嵌件成型引线框组件的侧视图；

[0050] 图 40 是图 39 中所示嵌件成型引线框组件的仰视图；

[0051] 图 41 是图 39 和 40 中所示嵌件成型引线框组件的电导体的顶部透视图；

[0052] 图 42 是图 41 中所示电导体的侧视图；

[0053] 图 43 是图 41 和 43 中所示电导体的侧视图，其中视角与图 42 的视角相比旋转了接近九十度；

[0054] 图 44 是图 39 和 40 中所示嵌件成型引线框组件的仰视图；以及

[0055] 图 45 是图 39，40 和 44 中所示嵌件成型引线框组件的侧视图，其中视角与图 39 的视角相比旋转了接近九十度。

具体实施方式

[0056] 图 1 到 15 画出了一种电连接器 10。连接器 10 可组成夹层式连接器系统的一部分，所述系统将第一和第二电装置（比如第一和第二电路衬底电）连接起来。连接器 10 包含电绝缘壳体 12，和多个包含在壳体 12 内部的嵌件成型引线框组件 (1MLA)14。连接器 10 与十个 1MLA14 一起画出只是为了举例而已；替换实施方式可包括多于或少于十个的 1MLA14。

[0057] 每个 1MLA14 包括多个电导体 16，和多个可熔元件，比如焊料球 17。每个 1MLA14 还包括电绝缘上框架 18，和电绝缘下框架 20。所画出的带有三十三个电导体 16 和三十三个焊料球 17 的 1MLA14 仅作为示例之用；替换实施方式 1MLA108 可包括多于或少于三十三个的电导体 16 和焊料球 17。

[0058] 每个电导体 16 包括接触梁 22、邻接接触梁 22 的引线部分 24、和邻接引线部分 24 在接触梁 22 远端的柱 26。相邻的电导体 16 可被定向为使得接触梁 22 面向相对侧的方向，如图 2,10,11,和 14 中所示。

[0059] 每个 IMLA14 上框架 18 被围绕着相关电导体 16 引线部分 24 模制，接近相关接触梁 22，如图 8,11,14,和 15 所示。上框架 18 具有多个形成于之上的圆柱形突起 30。上框架 18 还包括多个圆柱形凹穴或凹进 32。突起 30 和凹进 32 交错地设置在上框架 18 的两侧，因此当连接器 10 组装好时，每个 IMLA14 的突起 30 都位于相邻 IMLA14 的对应凹进 32 中。突起 30 和凹进 32 的尺寸设定为使得每个突起 30 紧密配合在对应的凹进 32 中。突起 30 与相邻 IMLA14 相关凹进 32 周边的啮合有助于相对相邻 IMLA14 定位和限制每个 IMLA14。

[0060] 每个 IMLA14 的下框架 20 被围绕着相关电导体 16 引线部分 24 模制，接近相关接触梁 26，如图 8 和 10-15 所示。下框架 20 具有多个形成于之上的长方形突起 34。下框架 20 还包括多个长方形凹穴或凹进 36。突起 34 和凹进 36 交错地设置在下框架 20 的两侧，因此当连接器 10 组装好时，每个 IMLA14 的突起 34 都位于相邻 IMLA14 的对应凹进 36 中。突起 34 和凹进 36 的尺寸设定为使得每个突起 34 紧密配合在对应的凹进 36 中。突起 34 与相邻 IMLA14 相关凹进 36 周边的啮合有助于相对相邻 IMLA14 定位和限制每个 IMLA14。

[0061] 下框架 20 具有多个形成于之上的凹穴 42，如图 12 和 13 中所示。每个柱 26 部分地定位于相关的一个凹穴 42 中。每个凹穴 40 是由四个基本平坦的表面 43 限定而成，如图 12 所示。每个表面 43 与相关柱 26 的纵向中心线成一定角度。

[0062] 每个焊料球 17 部分位于下框架 20 的相关凹穴 42 中。在连接器 10 置于其配合衬底（未画出）上之后，焊料球 17 经受焊料回流工艺 (reflow process)。焊料回流工艺使焊料球 17 熔化。熔化的焊料遇冷，在电导体 16 和配合衬底上的相关接触垫之间形成焊料接点。凹穴 42 的成角度表面 43 有助于在回流工艺中定位焊料球 17 和熔化的焊料，从而有助于正确地形成所得到的焊料接点。

[0063] 将凹穴 42 集成在每个 IMLA14 的下框架 20 中省去了除壳体 12 之外额外对独立结构的需要，或在壳体 12 本身中额外独立机构的需求，上述独立结构用于容纳焊料球 17。另外，IMLA14 可以被模制成连续的条带，然后切成所需的长度以便适应不同应用中所使用的尺寸不同的壳体 12，从而省去了在制造不同长度的 IMLA14 时需要不同的辅助工具的问题。

[0064] 壳体 12 包括上部 48 和下部 50。穿孔 52 形成于下部 50 的侧壁中，如图 1 和 4 中所示。每个穿孔 52 接纳最外的 IMLA14 之一的相关突起 34。突起 34 和穿孔 52 周边表面之间相干涉有助于将 IMLA14 保持在壳体 12 中。

[0065] 电导体 16 的接触梁 22 定位于壳体 12 的上部 48 内。上部 48 具有形成于其中的槽 56，如图 1 和 3 中所示。每个槽 56 沿着上部 48 的长度方向延伸，并位于相关 IMLA14 的上方。槽 56 为配合连接器（未画出）与接触梁 22 的接触提供了通路。槽 56 还在接触梁 22 和壳体 12 上部 48 的相邻表面之间提供了间隙，以便在接触梁 22 与配合连接器接触部相配合时适应接触梁 22 发生的偏斜。

[0066] 图 16-21 画出了连接器 10 的替换实施方式，形式为连接器 80。连接器 80 包括壳体 82，和多个 IMLA84。IMLA84 比 IMLA14 短，因此 IMLA84 可被定向为基本垂直于壳体 82 的长度方向。或者，IMLA84 也可与 IMLA14 基本相似。

[0067] 壳体 82 具有形成于其中的槽 85。每个槽 85 沿着基本垂直于壳体 82 长度方向的

方向延伸，并位于相关 IMLA84 的上方。槽 85 为配合连接器（未画出）与 IMLA84 接触梁的接触提供了通路。

[0068] 壳体 82 具有形成于其中的穿孔 86。每个穿孔 86 容纳了相关的那个 IMLA84 的下框架的末端，以便将 IMLA84 保持在壳体 82 中。

[0069] 图 22 至 31 画出了另一个替换实施方式，其形式为电连接器 100。连接器 100 包括第一半部 102，和与第一半部 102 匹配的第二半部 104。第一半部 102 和第二半部 104 是无极性的，也就是说，第一半部 102 和第二半部 104 是无性区分的 (non-gender-specific)。

[0070] 连接器 100 的第一半部 102 和第二半部 104 基本相同。接下来的对第一半部 102 的介绍也同样适用于第二半部 104，除非另有说明。

[0071] 第一半部 102 包含壳体 106，和包含在壳体 106 内部的多个 IMLA 108。所画出的带有六个 IMLA108 的连接器 100 仅作为示例之用；替换实施方式可包括多于或少于六个 IMLA108。

[0072] 第一半部 102 的壳体 106 构造成与第二半部 104 基本相同的壳体 106 匹配。每个壳体 106 包括侧壁 112。侧壁 112 包括第一部分 114 和第二部分 116，它们共同组成侧壁 112 的顶部（从图 23 的视角来看）。第一部分 114 被变薄使得第一部分 112 相对于侧壁 112 面向外的表面凹进去，并限定出面向外的凹进 117，如图 23 中所示。第二部分 116 被变薄使得第二部分 116 相对于侧壁 112 面向内的表面凹进来，并限定出面向内的凹进 118。

[0073] 当第一和第二半部 102，104 配合时，每个壳体 106 的侧壁 112 的第一部分 114 被容纳在其他壳体 106 的凹进 118 中。当第一和第二半部 102，104 配合时，每个壳体 106 的侧壁 112 的第二部分 116 被容纳在其他壳体 106 的凹进 117 中。第一和第二部分 114，116 以及凹进 117，118 可见地指示了第一和第二半部 102，104 在配合过程中是否正确定位，并有助于在配合过程中引导第一和第二半部 102，104。

[0074] 每个壳体 106 还包括第一端部 120 和第二端部 122，如图 22-24 中所示。第一和第二端部 120，122 每一个都具有形成与其中的内孔 124。如图 22 和 23 中所示，销 125 紧密配合在每个壳体 106 的第一端部 120 的内孔 124 中。当第一半部 102 和第二半部 104 配合时，销 125 紧密配合在其他壳体 106 第二端部 122 的内孔 124 中。销 124 有助于在第一和第二半部 102，104 配合时引导第一和第二半部 102，104。另外，销 124 和内孔 124 周边表面之间的摩擦有助于将第一和第二半部 102，104 保持在配合状态下。

[0075] 第二端部 122 如图 24 所示基本在壳体 106 的整个高度上延伸。第一端部 120 与第二端部 122 相比较短。更特别地，第二端部 122 的顶部近乎与侧壁 112 的第一部分 114 的底部齐平（从图 24 的视角来看）。这个特征在第一和第二半部 102，104 配合时，防止了每个壳体 106 的第一端部 120 与其他壳体 106 的第二端部 122 相干涉。

[0076] 每个 IMLA108 包括多个电导体 126，和多个可熔元件，比如焊料球 128。IMLA108 在图 29 和 30 中画出。每个 IMLA108 包括电绝缘上框架 130，和电绝缘下框架 132。所画出的带有十二个电导体 126 和十二个焊料球 128 的 IMLA108 仅作为示例之用；替换实施方式 IMLA108 可包括多于或少于十二个电导体 126 和焊料球 128。

[0077] 每个电导体 126 包括接触部分 134、沿着纵轴延伸且邻接接触部分 134 的引线部分 136、以及邻接引线部分 136 在接触部分 134 远端的柱 138，如图 31 中所示。接触部分 134 包括第一接触梁 140 和以并列关系放置的第二接触梁 142。第一接触梁 140 基本是笔直的。

第二接触梁 142 如图 29 所示，与引线部分 136 的纵轴成一定角度。例如，电导体部分可包括第一壳体和电导体 126 阵列，其中电导体 126 阵列的一部分沿着公共中线 CL 设置。电导体 126 阵列中的第一部分可沿中线设置，并可包括含有第一匹配端的第一接触梁 140。电导体 126 阵列中的最后一部分可沿中心线 CL 设置并包括与第一匹配端体形不同的第二匹配端（比如第二接触梁 142）。

[0078] 每个 IMLA108 的上框架 130 围绕相关电导体 126 的引线部分 136 模制，接近于相关的引线部分 134，如图 30 所示。

[0079] 每个 IMLA108 的下框架 132 围绕相关电导体 126 的引线部分 136 模制，接近于相关的柱 138，如图 30 所示。下框架 132 具有多个形成于其上的突起 144。下框架 132 还具有多个形成于其中的凹穴或凹进 146。突起 144 和凹进 146 交错地设置在下框架 132 的两侧。这种设置方式使得每个 IMLA108 的突起 144 在 IMLA108 位于相关壳体 106 中时被放置在相邻 IMLA108 的对应凹进 146 内。

[0080] 突起 144 和凹进 146 的尺寸设定为使得每个突起 144 紧密配合在相邻 IMLA108 的对应凹进 146 中。突起 144 与相邻 IMLA108 相关凹进 146 周边的啮合有助于相对相邻 IMLA108 定位和限制每个 IMLA108。每个突起 144 如图 29 和 30 中所示，可具有相对于竖直方向成一定角度的主表面 148，以便在它们相关的壳体 106 中组装和拆卸 IMLA108。

[0081] 每个壳体 106 具有多个形成于其中的面向内的凹进（未画出），用于容纳最外侧 IMLA 的突起 144。突起 144 和凹进的周边表面之间的干涉可有助于将 IMLA108 保持在壳体 106 中。

[0082] 替换实施方式的上框架 130 可配备凹进和突起，例如下框架 132 的凹进 146 和突起 144。

[0083] 每个 IMLA108 的下框架 132 具有多个形成于其中的凹穴 150，如图 26 中所示。接触部 126 的每个柱 138 部分地定位于相关的那个凹穴 150 内。每个柱 138 具有附着于其上的一个焊料球 128，从而焊料球 128 部分地被放置在相关凹穴 150 内。凹穴 150 可基本地相似于上述连接器 10 的下框架 30 中的凹穴 42。焊料球 128 可发生回流在连接器 100 的第一和第二半部 102，104 与它们各自的安装衬底（未画出）之间形成焊料连接。

[0084] 电导体 126 的接触部分 134 的构造允许当第一和第二半部 102，104 配合时，第一半部 102 的每个电导体 126 与第二半部 104 的相关电导体 126 配合。特别地，当第一和第二半部 102，104 配合时，第一半部 102 每个电导体 126 成角度的第二接触梁 142 与第二半部 104 相关电导体 126 基本笔直的第一接触梁 140 接触并相配合，如图 25 和 28 中所示。当第一和第二半部 102，104 配合时，第一半部 102 每个电导体 126 的第一接触梁 140 以同样地方式与第二半部 104 相关的那个电导体 126 发生接触。

[0085] 第一和第二半部 102，104 相关的第一和第二接触梁 140，142 之间的接触使得每个第二接触梁 142 在第一和第二半部 102，104 配合时远离相关的第一接触梁 140 向外弹性地偏斜。相关的第一和第二接触梁 140，142 之间的接触还导致每个第一接触梁 140 远离相关的第二接触梁 142 向外弹性地偏斜。第一和第二接触梁 140，142 的弹性偏斜导致形成相关第一和第二接触梁 140，142 之间的接触作用力。

[0086] 与性能相当的非无极性式连接器相比，连接器 100 的第一和第二半部 102，104 相同的构造将组建连接器所需部件的不同类型数量降到最小。制造，工具，和与仓储相关的成

本由此由于第一和第二半部 102,104 相同的构造则有可能降低。另外，IMLA108 可以被模制成连续的条带，然后切成所需的长度以便适应不同应用中所使用的尺寸不同的壳体 106。

[0087] 图 32 至 45 画出了另一替换实施方式，其形式为电连接器 200。连接器 200 包括第一半部 202，和与第一半部 202 匹配的第二半部 204。第一半部 202 和第二半部 204 是无极性的。

[0088] 连接器 200 的第一半部 202 和第二半部 204 基本相同。接下来的对第一半部 202 的介绍也同样适用于第二半部 204，除非另有说明。

[0089] 第一半部 202 包含壳体 206，和包含在壳体 206 内部的多个 IMLA208。为了解释清楚，所画出的第一半部 202 上的 IMLA208 数量比其全部数量要少。

[0090] 第一半部 202 的壳体 206 构造成与第二半部 204 基本相同的壳体 206 匹配。每个壳体 206 包括侧壁 212。侧壁 212 包括第一部分 214 和第二部分 216，它们共同组成侧壁 212 的顶部（从图 33 的视角来看）。第一部分 214 被变薄使得第一部分 212 相对于侧壁 212 面向外的表面凹进去，并限定出面向外的凹进 217，如图 33 和 36 中所示。第二部分 216 被变薄使得第二部分 216 相对于侧壁 212 面向内的表面凹进来，并限定出面向内的凹进 218。

[0091] 当第一和第二半部 102,104 配合时，每个壳体 206 的侧壁 212 的第一部分 214 被接收在其他壳体 106 的凹进 218 中。当第一和第二半部 202,204 配合时，每个壳体 206 的侧壁 212 的第二部分 216 被接收在其他壳体 206 的凹进 217 中。第一和第二部分 214,216 以及凹进 217,218 可见地指示了第一和第二半部 202,204 在配合过程中是否正确定位，并有助于在配合过程中引导第一和第二半部 202,204。

[0092] 每个 IMLA208 包括多个电导体 226，和多个可熔元件，比如焊料球 228，如图 39-45 中所示。每个 IMLA208 还包括电绝缘框架 230。所画出的带有十个电导体 226 和十个焊料球 228 的 IMLA208 仅作为示例之用；替换实施方式 IMLA208 可包括多于或少于十个电导体 226 和焊料球 228。

[0093] 每个电导体 226 包括接触部分 234，和邻接接触部分 234 的引线部分 236，如图 41-43 中所示。每个电导体 226 还包括球板 (ball paddle)238。球板 238 邻接引线部分 236 在接触部分 234 的远端，并定向为基本垂直于引线部分 236 的纵轴。

[0094] 接触部分 234 包括第一接触梁 240 和以并列关系放置的第二接触梁 242，如图 39-45 中所示。第一接触梁 240 基本是直的。第二接触梁 242 的一部分是成角度的，从而第二接触梁 242 相对于引线部分 236 的纵轴偏离，如图 43 和 45 中所示。

[0095] 每个 IMLA208 的框架 230 围绕相关电导体 226 的引线部分 236 模制。每个框架 230 的上下末端都相对于框架 230 的其余部分加厚，如图 45 所示，以便将相邻 IMLA208 隔开。

[0096] 电导体 226 的每个球板 238 具有附着于其上的一个焊料球 228，如图 39,44,和 45 所示。焊料球 228 可发生回流在连接器 200 的第一和第二半部 202,204 与它们各自的安装衬底（未画出）之间形成焊料连接。

[0097] 电导体 226 的接触部分 234 的构造允许当第一和第二半部 202,204 配合时，第一半部 202 的每个电导体 226 与第二半部 204 的相关电导体 226 配合。电导体可仅包括两个梁，其中每个梁的形状都不相同。特别地，当第一和第二半部 202,204 配合时，第一半部 202 每个电导体 226 的偏离第二接触梁 242 或可偏斜接触梁与第二半部 204 相关或相同电导体 226 基本直的或基本不可偏斜的第一接触梁 240 相接触并相配合，如图 36 中所示。当第一

和第二半部 202，204 配合时，第一半部 202 每个电导体 226 的第一接触梁 240 以同样地方式与第二半部 204 相关的那个电导体 226 的第二接触梁 242 发生接触。

[0098] 第一和第二半部 202，204 相关的第一和第二接触梁 240，242 之间的接触使得每个第二接触梁 242 在第一和第二半部 202，204 配合时向外弹性地偏斜，远离相关的第一接触梁 202。相关的第一和第二接触梁 202，204 之间的接触还导致每个第一接触梁 202 向外弹性地偏斜，远离相关的第二接触梁 204。第一和第二接触梁 240，242 的弹性偏斜导致形成相关第一和第二接触梁 240，242 之间的接触作用力。

[0099] 与性能相当的非无极性式连接器相比，连接器 200 的第一和第二半部 202，204 相同的构造将组建连接器 200 所需部件的不同类型数量降到最小。另外，IMLA208 可以被模制成连续的条带，然后切成所需的长度以便适应不同应用中所使用的尺寸不同的壳体 206。

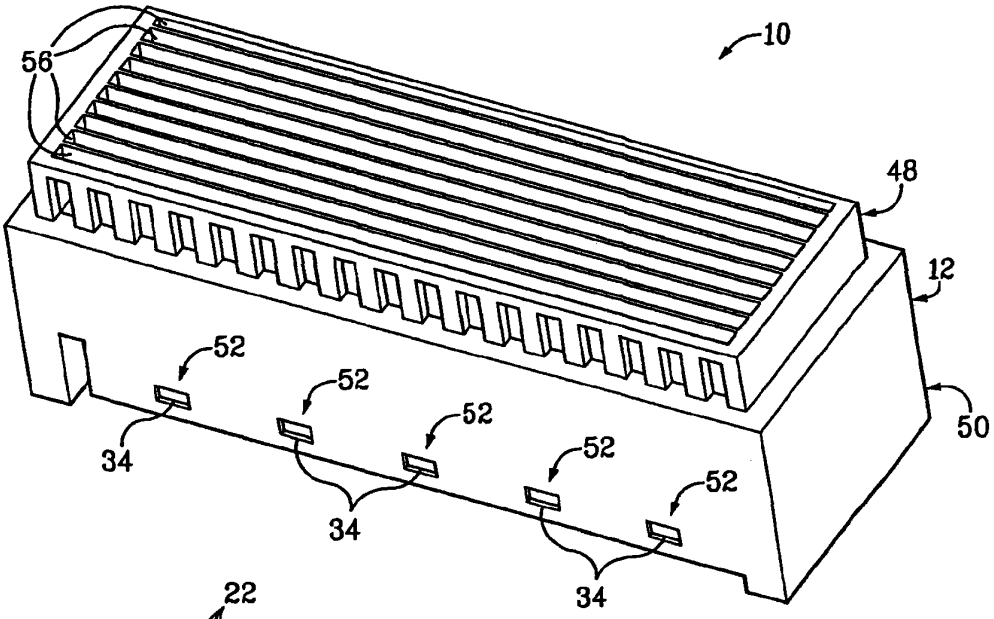


图1

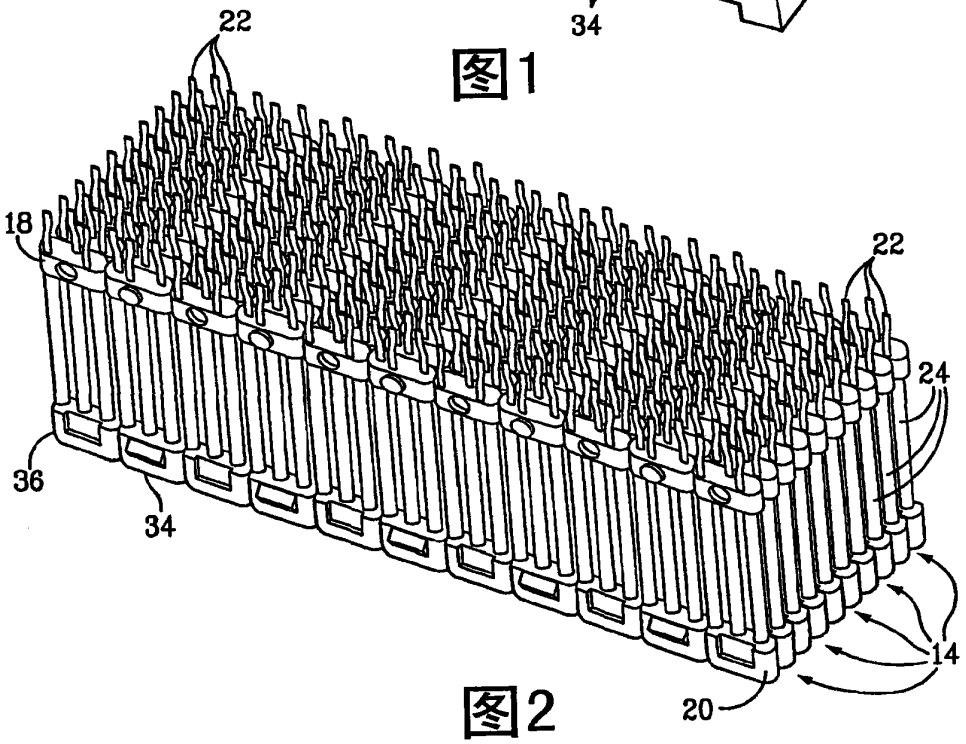


图2

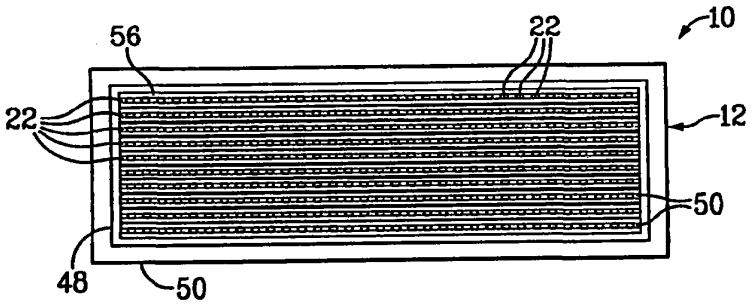


图 3

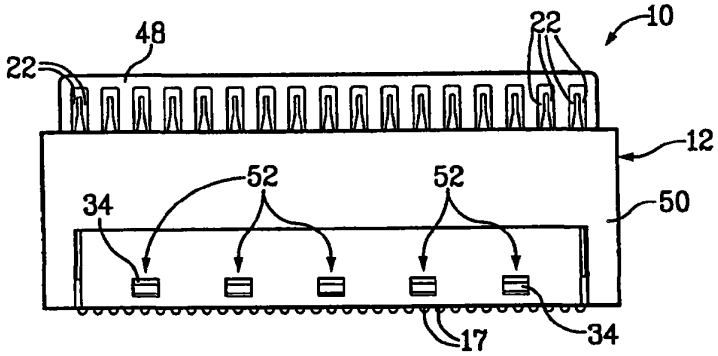


图 4

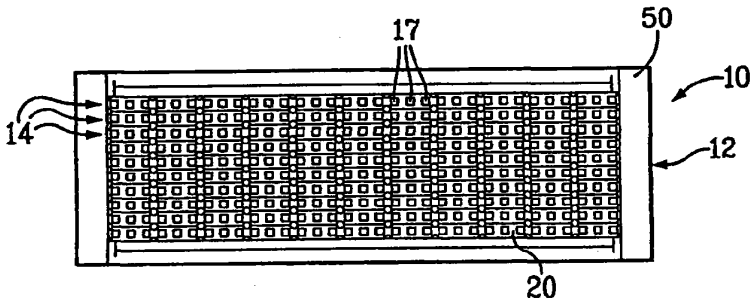


图 5

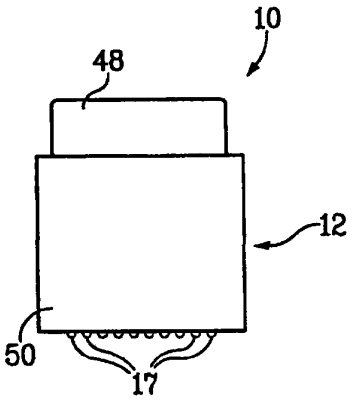


图 6

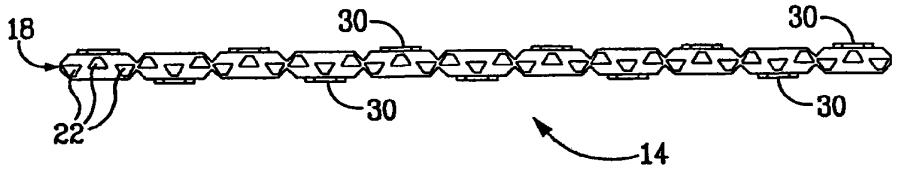
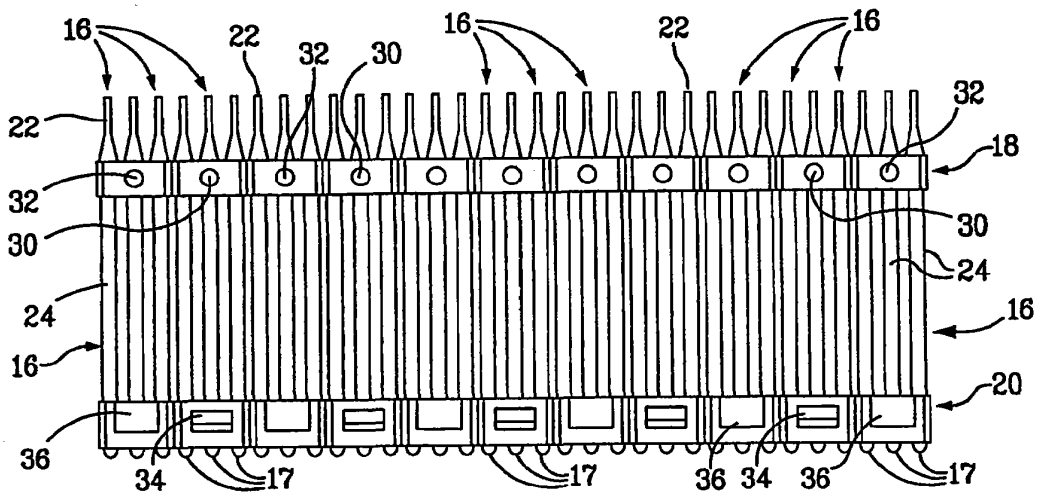


图 7



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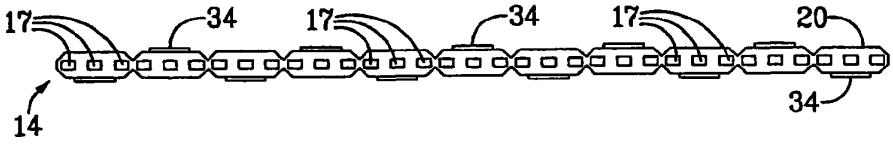

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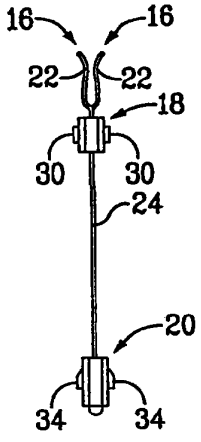

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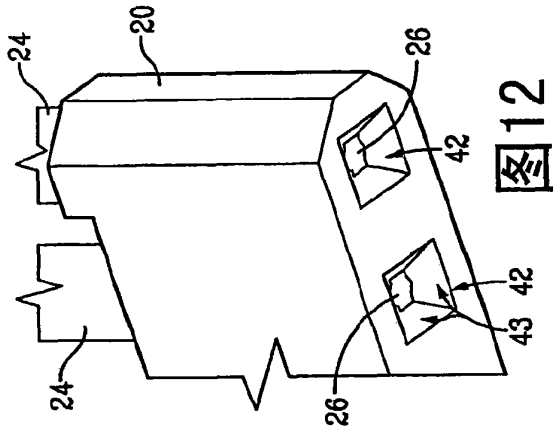

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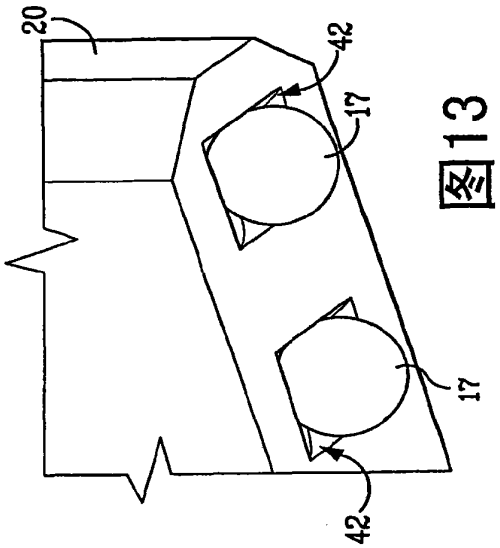

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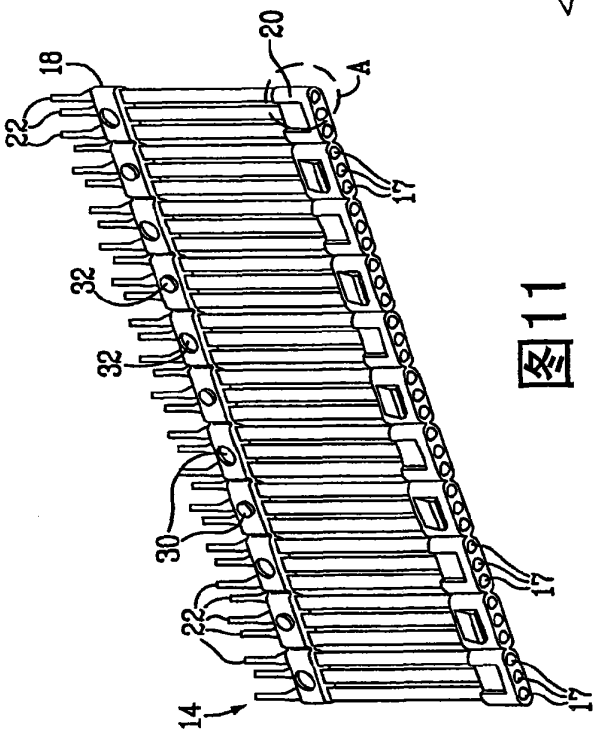

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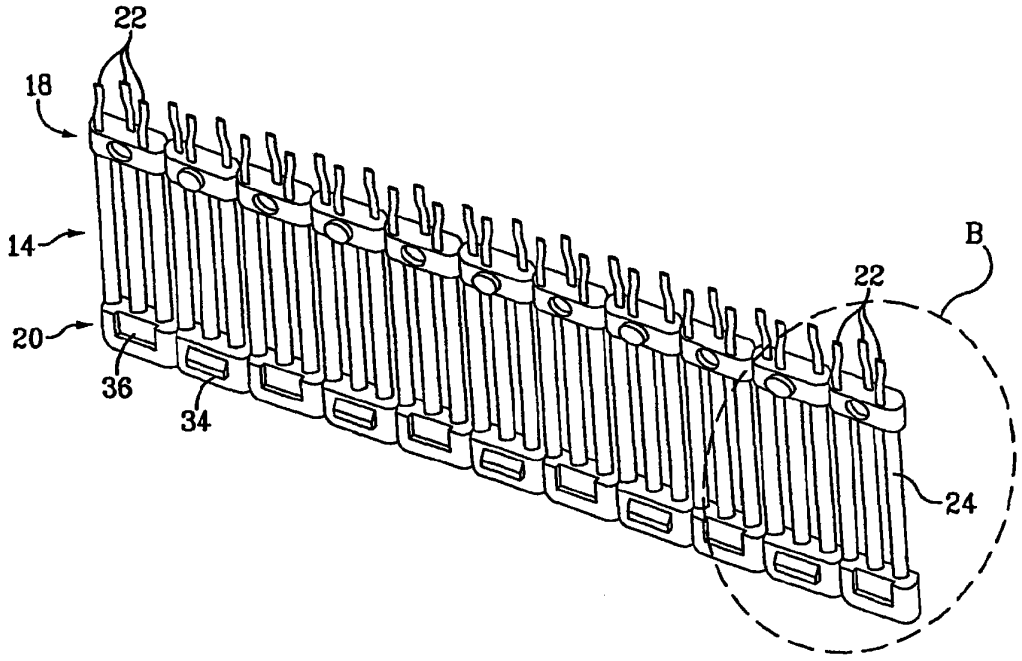

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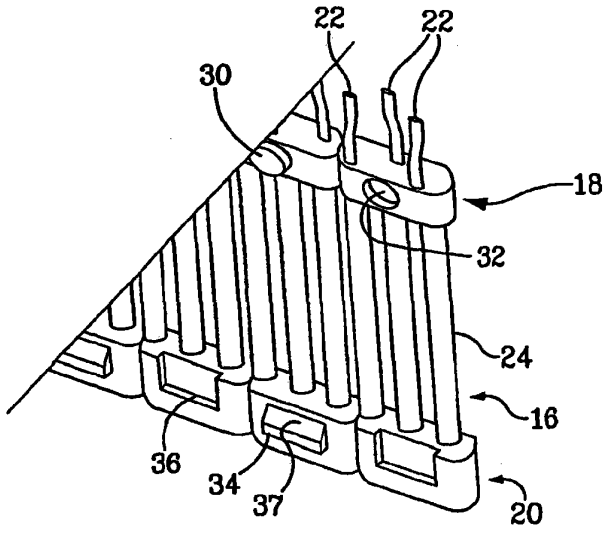

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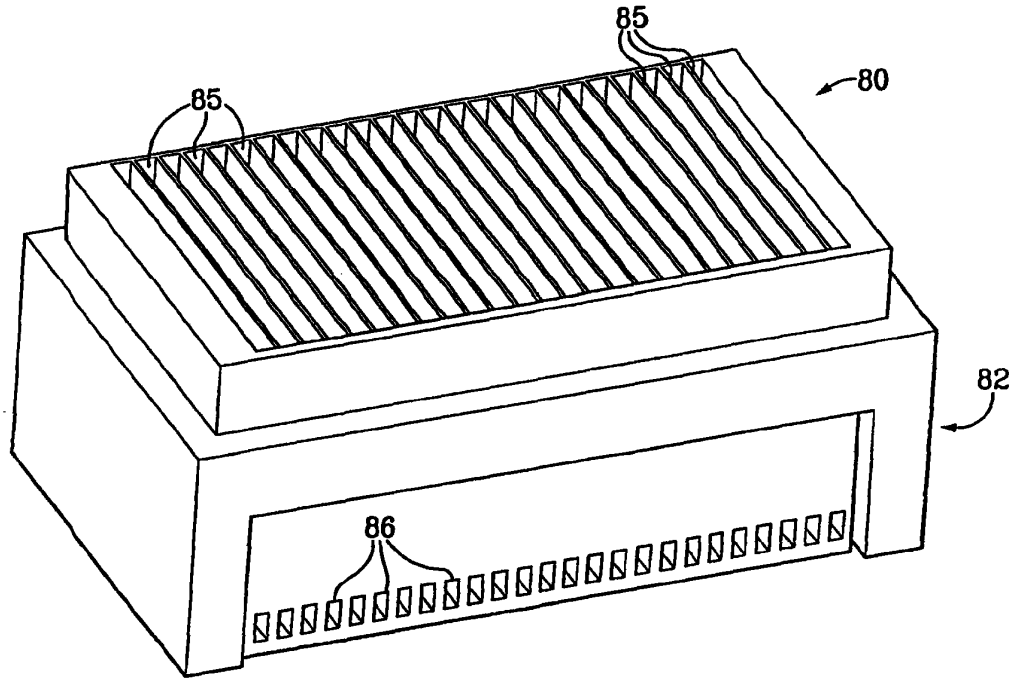

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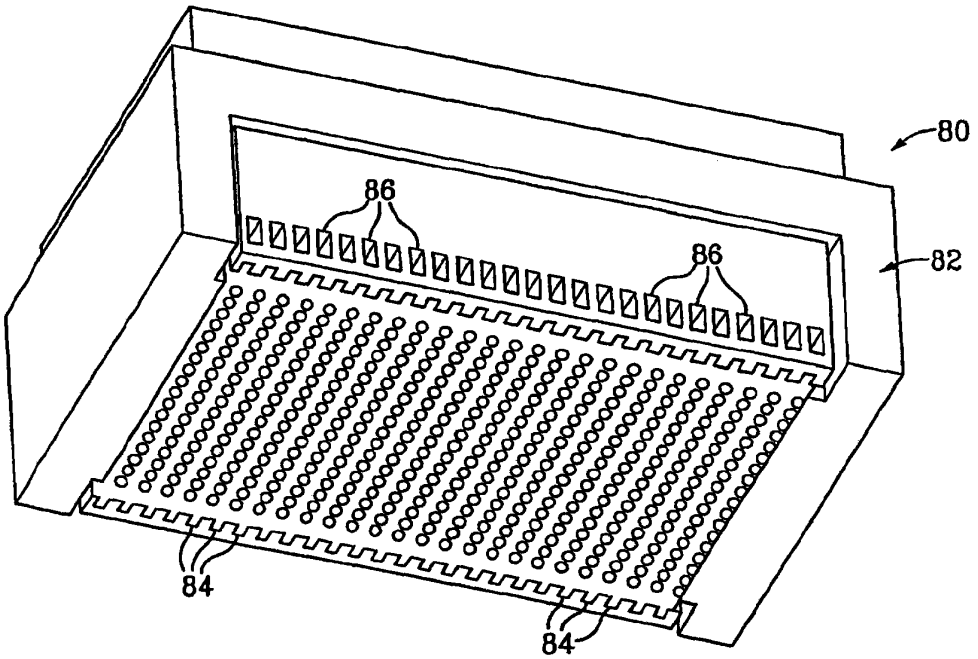

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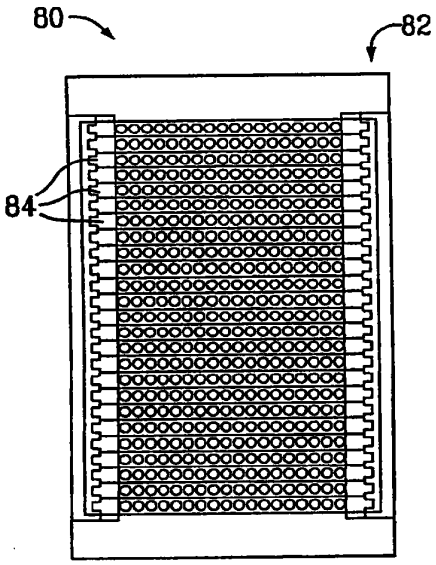

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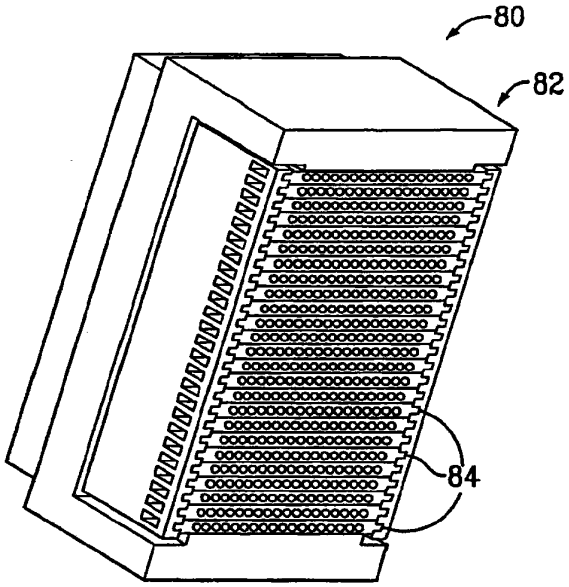

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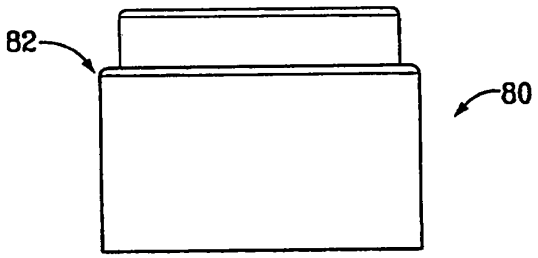

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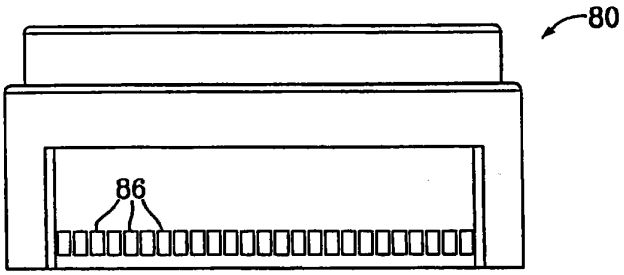

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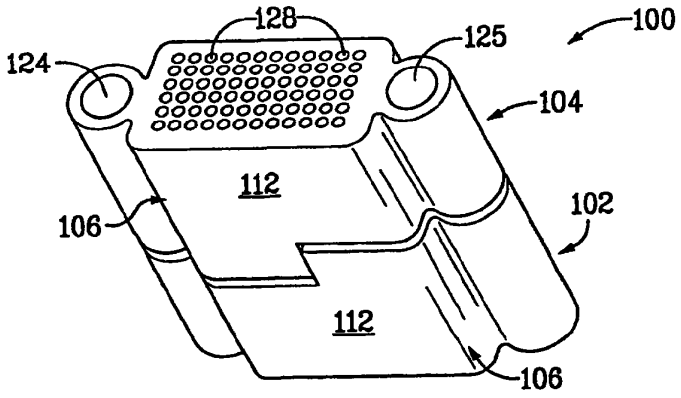

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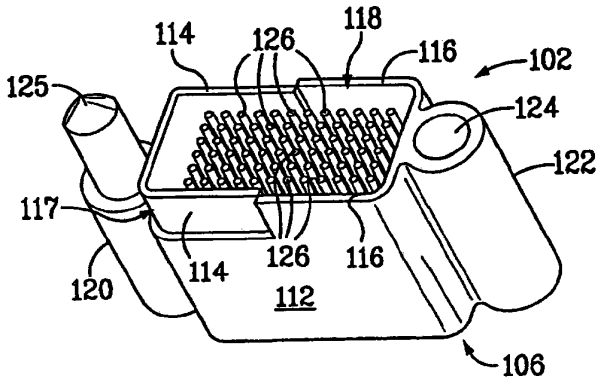

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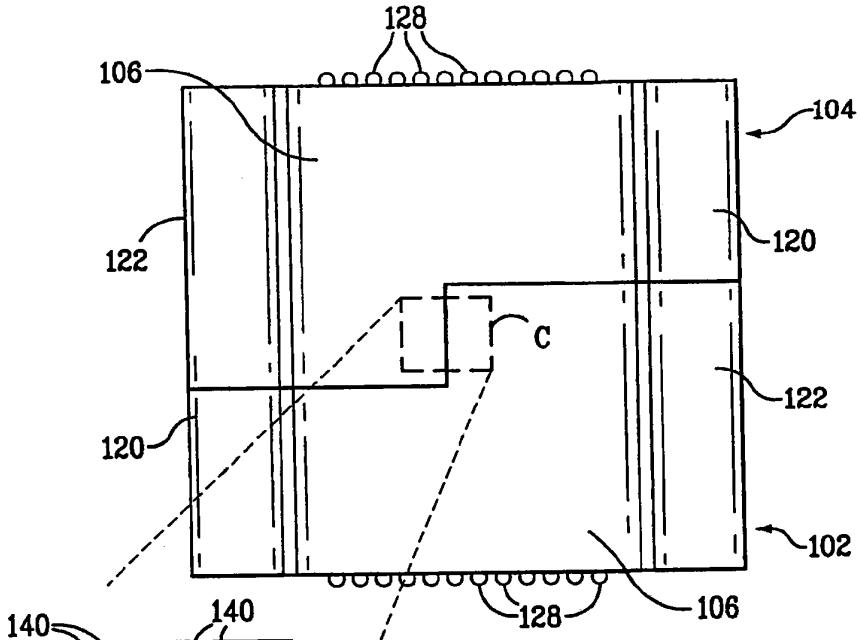

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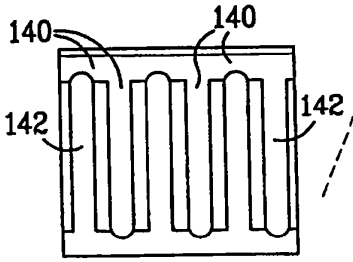

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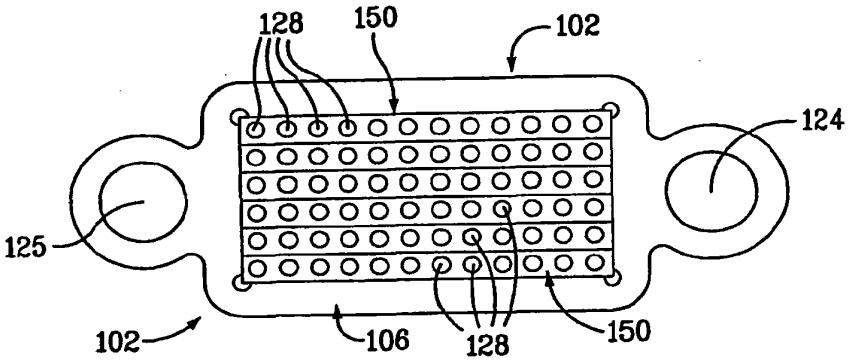

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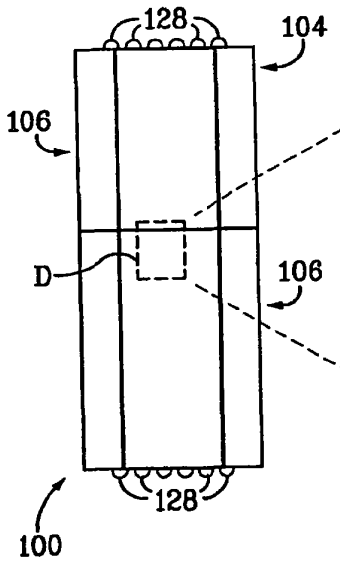

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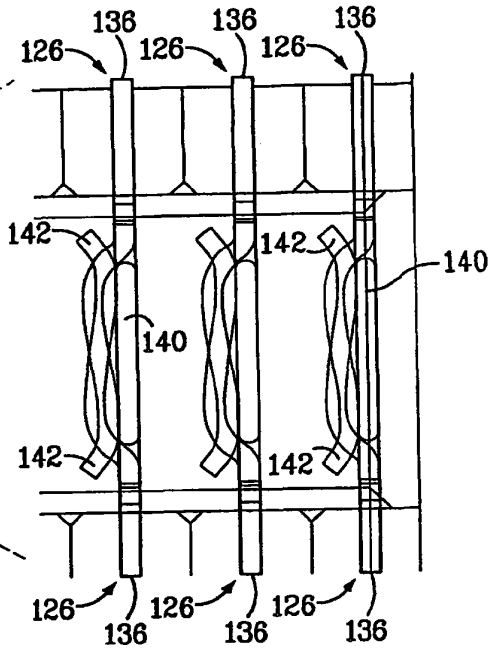

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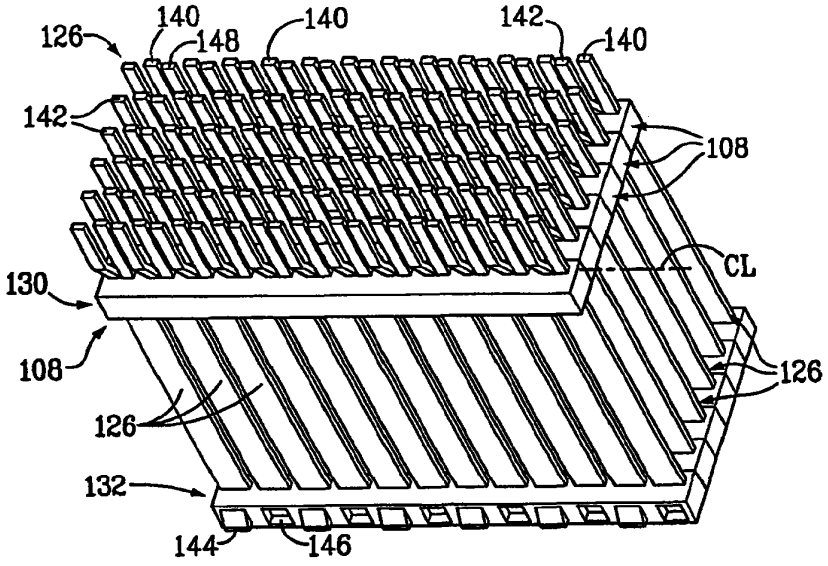

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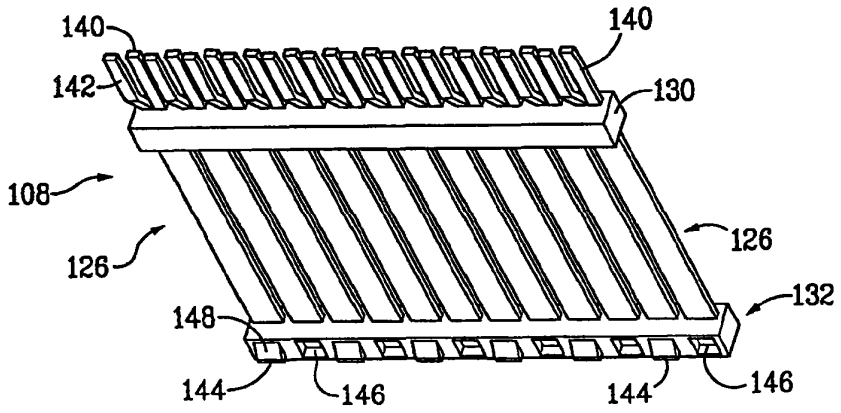

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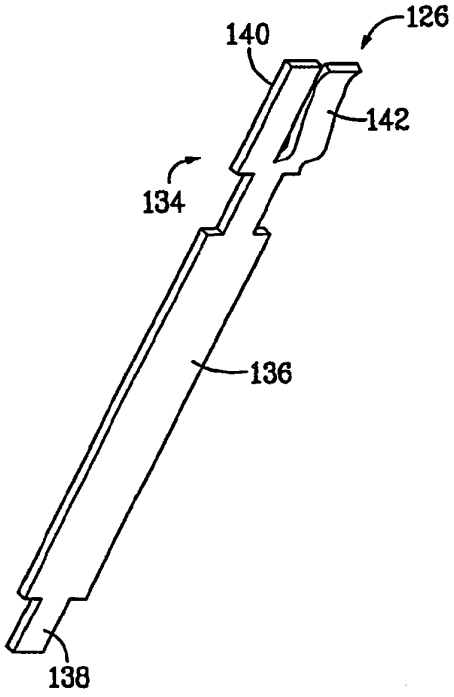

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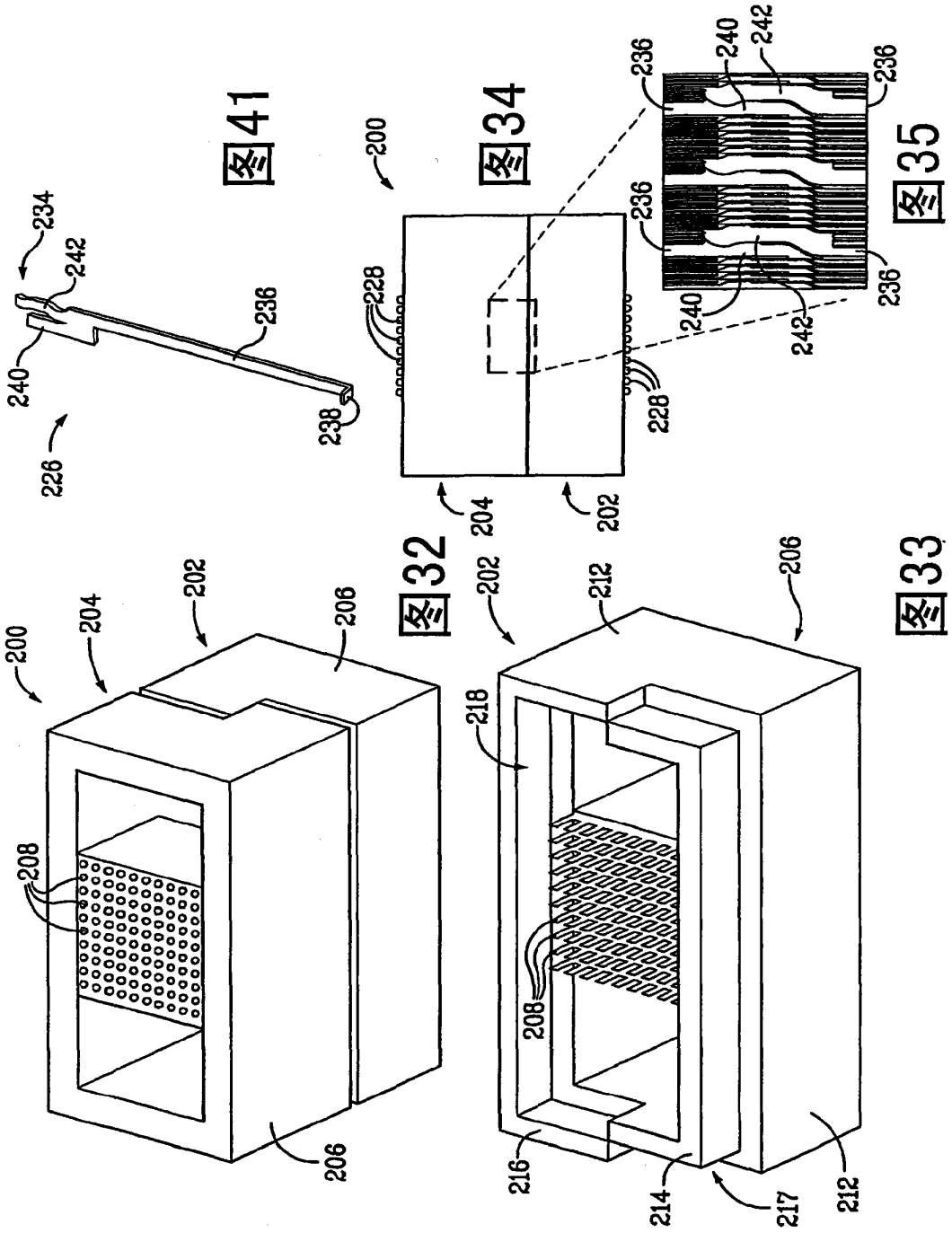

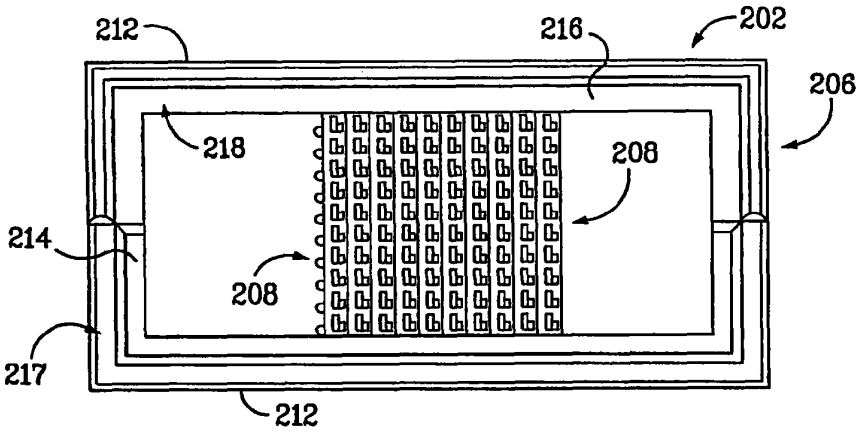

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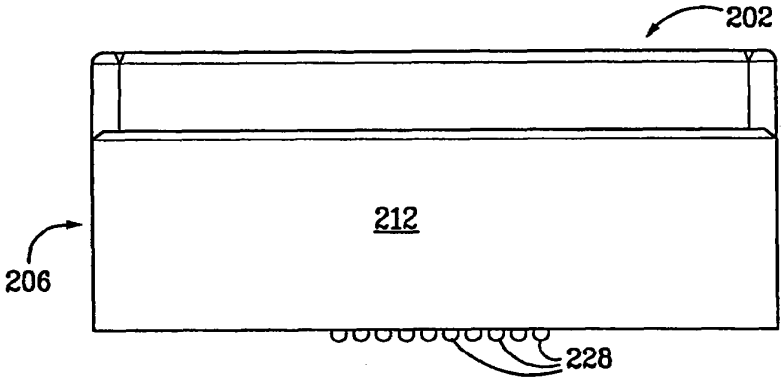

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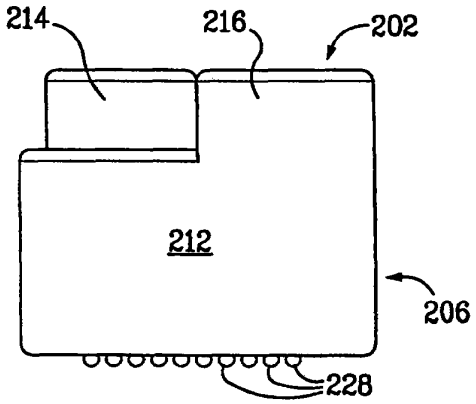

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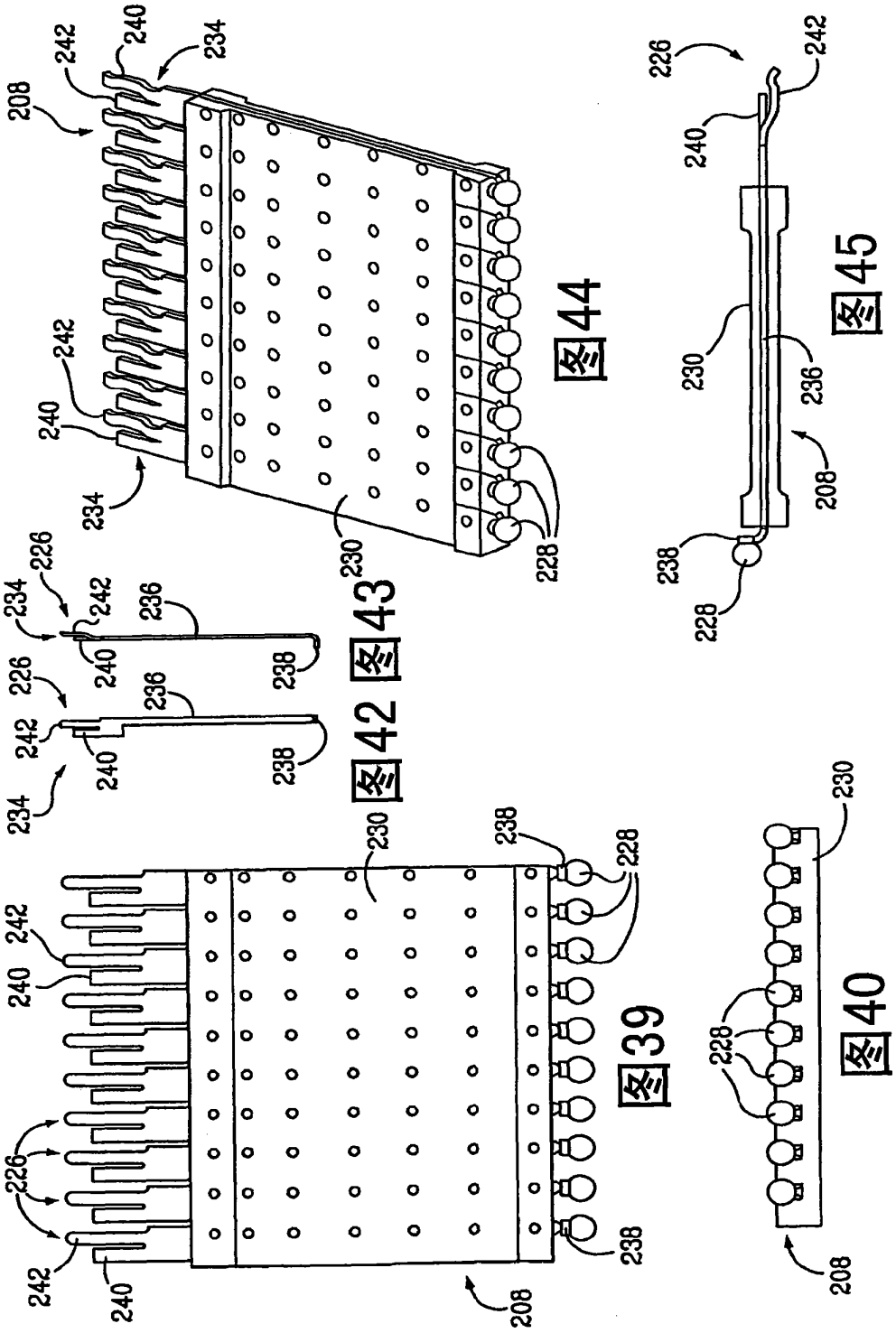

Espacenet

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High speed, high density electrical connector with selective positioning of lossy regions

Inventor(s): BRIAN KIRK; COHEN THOMAS S ± (KIRK BRIAN, ; COHEN THOMAS S)

Applicant(s): AMPHENOL CORP ± (AMPHENOL CORP)

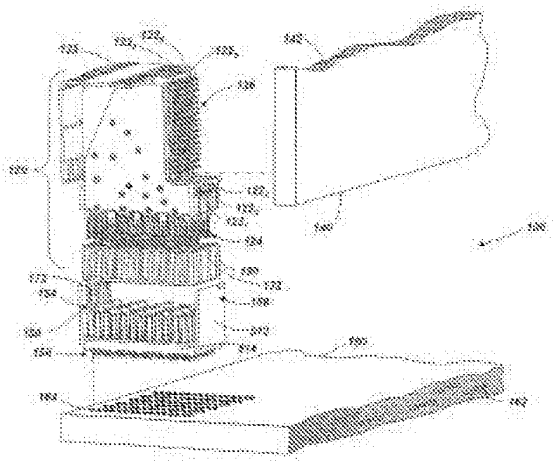
Classification: - international:*H01R13/648*
- cooperative: **H01R12/724**; **H01R13/514**; **H01R23/688**; H01R12/52

Application number: CN2008818749 20080404

Priority number (s): WO2008US04396 20080404 ; US20070921740P 20070404

Also published as: CN102239605 (B) US2008248660 (A1) US7581990 (B2) WO2008124057 (A2)

Abstract of CN102239605 (A)



Provided is an electrical interconnection system with high speed, high density electrical connectors. The connectors incorporate electrically lossy material, selectively positioned to reduce crosstalk without undesirably attenuating signals. The lossy material may be molded through ground conductors that separate adjacent differential pairs within columns of conductive elements in the connector. However, regions of lossy material may be set back from the edges of the ground conductors to avoid undesired attenuation of signals. Also, the lossy material may be positioned in multiple regions along the length of signal conductors. The regions may be separated by holes, notches, gaps or other openings in the lossy material, which can be simply formed as part of a molding operation.

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权利要求书 4 页 说明书 17 页 附图 11 页

(54)发明名称

具有选择性定位的损耗区的高速、高密度电连接器

(57)摘要

一种具有高速、高密度的电连接器的电子互连系统。该连接器包括电损耗材料，其选择性地定位以减少串扰而不会不期望地衰减信号。该损耗材料可通过接地导体模制，该接地导体将连接器中的导电元件列内的相邻差分对隔开。然而，损耗材料区从接地导体边缘缩进，以避免不希望的信号衰减。而且，损耗材料可在沿信号导体长度的多个区域中定位。这些区域可被洞、槽口、缝隙或损耗材料中的其他开口隔开，这些开口可以作为模制操作的一部分简单地形成。

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1. 一种电连接器，包括：

a) 多个信号导体，所述多个信号导体设置在阵列中；

b) 外壳，包括：

i) 至少一个绝缘构件，其用于保持所述阵列中的所述多个信号导体；以及

ii) 沿信号导体长度设置的至少一个损耗构件，其用于在所述信号导体与相邻的信号导体之间提供多个损耗区域，并在相邻的损耗区域之间具有至少一个绝缘区域。

2. 根据权利要求 1 的电连接器，其特征在于，所述损耗区域和所述至少一个绝缘区域被调整和设置成减少所述信号导体与其相邻信号导体之间的串扰，并限制对所述信号导体和相邻的信号导体所传输的信号的衰减。

3. 根据权利要求 1 的电连接器，其特征在于，所述至少一个绝缘构件包括模制塑料，且所述至少一个损耗构件包括具有导电填料的模制塑料。

4. 根据权利要求 1 的电连接器，其特征在于，所述至少一个绝缘构件包括模制塑料，所述至少一个损耗构件包括在模制塑料表面上的镀层，所述镀层在 1GHz 到 12GHz 的频率范围上具有损耗特性。

5. 根据权利要求 1 的电连接器，其特征在于，所述多个信号导体被调整和设置为形成多个差分对，且所述多个损耗区域设置在形成分离的差分信号对的构件的相邻的信号导体之间。

6. 根据权利要求 1 的电连接器，其特征在于：

所述多个信号导体设置在列中；

所述至少一个损耗构件包括与所述列平行的平行区域和从所述平行区域延伸的多个垂直区域；以及

所述至少一个绝缘区域包括在相邻的垂直区域之间的所述平行区域中的至少一个开口。

7. 根据权利要求 6 的电连接器，其特征在于：

所述列中的所述多个信号导体包括多个差分对，各个差分对具有第一和第二信号导体；

所述多个垂直区域中的每一个设置在相邻的差分对之间；以及

所述平行区域中的所述至少一个开口包括定位于差分对的所述第一与第二信号导体之间的至少一个开口。

8. 根据权利要求 7 所述的电连接器，其特征在于，所述至少一个绝缘区域还包括所述垂直区域中的至少一个开口。

9. 根据权利要求 8 所述的电连接器，其特征在于：

所述平行区域中的所述至少一个开口包括在各个相邻垂直区域之间的所述平行区域中的开口；

所述垂直区域中的所述至少一个开口包括在所述垂直区域中的每一个中的开口，所述垂直区域中的各个开口与所述平行区域中的至少一个开口之一连通，

藉此所述多个损耗区域中的各个具有 U 形段，所述 U 形段包括所述平行区域的部分和所述垂直区域的部分，所述多个损耗区被所述垂直区域和所述平行区域中的开口隔开。

10. 根据权利要求 1 所述的电连接器，其特征在于：

所述多个信号导体设置在列中；

所述至少一个损耗构件包括与所述列平行的平行区域和从所述平行区域延伸的多个垂直区域；以及

所述至少一个绝缘区域包括所述多个垂直区域中的至少一个区域中的至少一个开口。

11. 根据权利要求 1 所述的电连接器，其特征在于：

所述多个信号导体设置在包括多个差分对的列中；

所述至少一个损耗构件形成多个沟槽，所述沟槽具有由平行区域限定的底部和由从所述平行区域延伸的相邻垂直区域限定的侧面，各个沟槽接收一个差分对；以及

所述多个损耗区中的每一个包括被所述垂直区域中的开口隔开的所述多个沟槽中的至少一个的一部分。

12. 根据权利要求 1 所述的电连接器，其特征在于，所述至少一个绝缘区域包括空气和 / 或所述至少一个绝缘构件的一部分。

13. 根据权利要求 1 所述的电连接器，其特征在于：

各个信号导体包括配合接触部、接触尾部以及将所述配合接触部电耦合到所述接触尾部的中间部，各个信号导体的所述中间部嵌入所述至少一个绝缘构件中；

所述多个信号导体设置在多个列中，所述多个列中的每一列中的所述多个信号导体包括多个差分对；

所述至少一个损耗构件包括多个平行区域和多个垂直区域，所述多个平行区域中的每一个设置成与所述多列中的一列平行，且所述多个垂直区域中的每一个从平行区域延伸；

所述至少一个绝缘区域包括在相邻的垂直区域之间的所述多个平行区域中的每个中的至少一个开口；

所述至少一个损耗构件包括毗邻所述多个列中的各列的损耗构件，各个损耗构件形成多个沟槽，所述沟槽具有由毗邻所述列的平行区域限定的底部和由毗邻的垂直区域限定的侧面，各个沟槽接收一个差分对，并且所述多个损耗区域中的各个包括由所述损耗构件中的所述开口分隔的所述多个沟槽中的至少一个的一部分；

所述多个垂直区域中的每一个设置在所述多个列中的一列内的相邻差分对之间；以及

所述损耗区域和所述绝缘区域被调整和设置为减少相邻的信号导体对之间的串扰，并限制由所述相邻的信号导体对所传输的信号的损耗。

14. 根据权利要求 13 所述的电连接器，其特征在于，进一步包括多个接地导体，所述接地导体中的每一个电连接至所述多个垂直区域中的一个垂直区域。

15. 根据权利要求 13 所述的电连接器，其特征在于，列中的每个差分对具有不同的长度，而且调整所述损耗区域的尺寸并将其配置成：相比较长的差分对而言，对较短差分对提供更高的每单位长度的损耗。

16. 一种电连接器，包括：

a) 多个信号导体，所述多个信号导体设置在具有至少一列的阵列中；

b) 包括多个损耗区域的外壳，各个损耗区域毗邻所述多个信号导体中的至少一个设置；以及

c) 多个接地导体，所述接地导体中的每一个：

设置在所述至少一列的列中；

毗邻所述列中的所述多个信号导体中的至少一个信号导体设置；以及

具有面对所述至少一个毗邻的信号导体的至少一个边；以及

所述多个损耗区域中的损耗区相对于所述多个接地导体中的接地导体定位，并在远离毗邻所述接地导体的所述信号导体的方向上从所述接地导体的边缘缩进。

17. 根据权利要求 16 所述的电连接器，其特征在于，

还包括至少一个绝缘部，所述绝缘部具有多个绝缘区域；以及

其中对于每个接地导体，所述多个绝缘区域中的绝缘区域设置在毗邻的信号导体与毗邻所述信号导体的损耗区域之间，而且所述绝缘区域定位于所述缩进中。

18. 根据权利要求 17 所述的电连接器，其特征在于，所述绝缘部包括模制塑料，并被调整和设置为保持阵列中的所述多个信号导体。

19. 根据权利要求 17 所述的电连接器，其特征在于，所述绝缘部包括空气区域。

20. 一种电连接器，包括：

a) 多个信号导体，所述多个信号导体设置在具有至少一列的阵列中；

b) 包括多个损耗区域的外壳，各个损耗区域毗邻所述多个信号导体中的至少一个；以及

c) 多个接地导体，所述接地导体中的每一个具有通过其中的开口，所述接地导体中的每一个设置在所述至少一列的一列中，而且所述接地导体中的每一个与所述多个损耗区域中的的损耗区电连接；

其中与各个接地导体电连接的所述损耗区域的一部分被设置成穿过所述接地导体中的所述开口。

21. 根据权利要求 20 所述的电连接器，其特征在于

i) 所述接地导体中的每一个毗邻所述列中的信号导体设置；

ii) 所述接地导体中的每一个具有面对所述相邻的信号导体的边缘；

iii) 与所述接地导体电连接的损耗区域被设置具有从所述边缘的缩进。

22. 根据权利要求 20 所述的电连接器，其特征在于：

i) 所述电连接器包括多个组件，每个组件具有第一面和第二面，而且所述组件并排对齐；

ii) 所述至少一列包括多个列，每个列定位在所述多个组件中的一个独立组件中；以及

iii) 在每个组件中，损耗区域在第一面中露出，且所述损耗区域的所述部分中的至少一个与所述第二面电耦合。

23. 根据权利要求 22 所述的电连接器，其特征在于，在每个组件中，所述部分中的至少一个在第二面中露出。

24. 根据权利要求 23 所述的电连接器，其特征在于，所述多个组件被定位成将所述多个组件的损耗区域电耦合到一起，所述耦合是通过在所述多个组件中的组件的所述第一面中露出的损耗区域耦合到在所述多个组件中的组件的所述第二面中露出的损耗区域来形成。

25. 根据权利要求 22 所述的电连接器，其特征在于，在每个组件中，在所述第二面中露出的导体电连接至所述部分中的至少一个。

26. 一种电连接器，包括：

a) 多个信号导体，所述多个信号导体设置在具有多个列的阵列中；

b) 多个接地导体，所述接地导体中的每一个设置在所述多个列中的一列中；以及

c) 包括多个损耗区域的外壳，

其中所述损耗区域定位在：

i) 两个相邻的信号导体之间的区域中的两个相邻列之间，所述两个相邻的信号导体中的每一个处于所述两个相邻列的不同列中；以及

ii) 两个相邻的接地导体之间，所述两个相邻的接地导体中的每一个在所述两个相邻的列中的一列中。

27. 根据权利要求 26 所述的电连接器，其特征在于：

i) 所述多个信号导体包括多个差分对，且所述多个接地导体中的所述接地导体设置在相邻的差分对之间；以及

ii) 损耗区域设置在两个相邻的差分对之间，每个相邻的差分对处于两个相邻列中的不同列中。

28. 根据权利要求 26 所述的电连接器，其特征在于，每个损耗区域电连接到所述两个相邻的接地导体中的至少一个。

29. 根据权利要求 26 所述的电连接器，其特征在于，所述外壳包括多个组件，每个组件具有保持一列信号导体的绝缘部。

具有选择性定位的损耗区的高速、高密度电连接器

[0001] 相关申请的交叉引用

[0002] 本申请要求 2007 年 4 月 4 日提交的美国临时申请 60/921,740 的优先权，该申请通过引用结合于此。

背景技术

[0003] 1. 技术领域

[0004] 该申请一般涉及电互连系统，更具体地涉及在互连系统中尤其是高速电连接器中提升信号完整性。

[0005] 2. 相关技术讨论

[0006] 电连接器在许多电子系统中使用。相比制作一个单独配置的系统而言，在通过电连接器彼此互连的若干个印刷电路板 (PCBs) 上制作系统更容易也更经济。互连多个 PCB 板的传统方法是使用一个 PCB 板作为底板。其他被称为子板或子卡的 PCB 板再通过电连接器连接到底板。

[0007] 电子系统正在变得更为小巧、快速，并具有更复杂的功能。这些改变意味着在电子系统的给定面积中的电路数量以及这些电路的工作频率近年来显著提高。目前的系统在印刷电路板间传送更多的数据，并要求电连接器能够以比几年前的连接器更高的速率处理更多的数据。

[0008] 制作高密度、高速的连接器的困难之一是连接器中的电线太靠近，从而在相邻的信号线间产生电干扰。为了减少干扰和提供所需的电性能，常在相邻信号线之间或周围设置金属构件。这些金属可作为屏蔽件以防止导线上加载的信号和其他导线发生“串扰”，它还能影响每个导线的阻抗，从而有利于获得需要的电性能。

[0009] 当信号频率提高时，电噪声在连接器中也更可能产生，例如反射、串扰和电磁辐射等形式。因而，电连接器被设计成可以限制不同信号线间的串扰和每个信号通路的特征阻抗。为此，经常在信号线旁设置屏蔽构件。

[0010] 可以通过设置信号通路以使信号线彼此间被设置成更远而与诸如接地面之类的屏蔽相隔更近来限制经过连接器的不同信号通路之间的串扰。如此，不同的信号通路更多的与屏蔽面进行电磁耦合而不是互相耦合。对一个给定程度的串扰来说，当与地线的耦合保持足够时，信号通路就可以设置得彼此更接近。

[0011] 虽然隔离导线的屏蔽件通常由金属组件制成，但转让给与本申请相同的受让人并在此全文引入作为参考的 US6,709,294（`294 专利）还描述了一种采用导电塑料制作连接器中的屏蔽板的延伸。

[0012] 还可以使用其他技术来控制连接器的性能。差分地传送信号也可以减少串扰。差分信号经由一对导电通路传送，称为“差分对”。导电通路之间的电压差表示该信号。一般来说，差分对优选耦合在该对中的导线通路之间。例如，一个差分对的两个导电通路可设置为相比连接器中的邻近信号通路而言彼此更靠近。在差分对的导电通路之间不设置屏蔽，但可以在不同的差分对之间使用屏蔽。电连接器既可设计成用于差分信号也可设计成用于

单端信号。

[0013] 差分电连接器的例子可以在美国专利第6,293,827号、第6,503,103号、第6,776,659号和第7,163,421号中看到，这些专利都转让给与本申请相同的受让人，在此将他们的全文引入作为参考。

[0014] 连接器的电特性还可以通过使用吸收材料加以控制。同样转让给本申请相同的受让人的美国专利第6,786,771号（`771专利），描述了使用吸收材料来减少不必要的谐振和提高连接器性能的方法，尤其是在高速下（例如，1GHz或更高的信号频率，特别是3GHz以上），在此将其全文引入作为参考。

[0015] 也转让给与本申请相同的受让人并在此引入全文作为参考的美国已公开专利申请2006/0068640描述了使用损耗材料来提高连接器性能的方法。

发明内容

[0016] 提供一种具有选择性定位的损耗区的改进的电连接器。该损耗区域可以减少相邻信号导体之间的串扰，同时不会让信号导体上加载的信号发生不希望的衰减。一种选择性定位损耗区的技术涉及提供沿着信号线的绝缘区域隔开的多个损耗材料段。另一种技术涉及将损耗区与接地导体联合定位，并且将损耗区定位成具有从距离接地导体边缘的缩进。另一种技术涉及将损耗区定位成延伸穿过接地导体。还有一种技术涉及将损耗区定位于导电元件的毗邻平行列之间、在相邻列的两个接地导体和两个信号导体之间。这些技术可以单独使用也可以组合使用。

[0017] 因此，在一个方面中，本发明涉及一中包括多个信号导体的电连接器。这多个信号导体以阵列设置。连接器具有外壳，该外壳包含至少一个绝缘构件以将多个信号导体保持在阵列中。该外壳还包括沿信号线的长度设置的至少一个损耗构件，以在信号导体与相邻的信号导体之间提供多个损耗区，且在相邻的损耗区之间有至少一个绝缘区。

[0018] 在另一方面中，本发明涉及一种包括多个信号导体的电连接器。该多个信号导体设置成至少具有一列的阵列。该连接器具有包括多个损耗区的外壳。各个损耗区毗邻多个信号导体中的至少一个设置。连接器中的多个接地导体分别设置于至少一列中的一列中。各个接地导体设置为毗邻该列中的多个信号导体中的至少一个信号导体，并具有正对该至少一个毗邻的信号导体的至少一个边缘。多个损耗区的损耗区相对于该多个接地导体的接地导体定位，并具有在离开毗邻接地导体的信号导体的方向上从接地导体边缘的缩进。

[0019] 在另一方面中，本发明涉及一种包括多个信号导体的电连接器。该多个信号导体设置成具有至少一列的阵列。连接器具有包括多个损耗区的外壳。各个损耗区毗邻多个信号导体中的至少一个。连接器中的多个接地导体中的每个中具有开口。每个接地导体设置在至少一列的一列中，且每个接地导体与多个损耗区中的一个损耗区电连接。和各个接地导体电连接的损耗区的一部分被设置成从接地导体的开口中穿过。

[0020] 在另一方面中，本发明涉及一种包括多个信号导体的电连接器。该多个信号导体设置成具有多列的阵列。该连接器还具有多个接地导体，各个设置在该多个列中的一列中。连接器的外壳包括多个损耗区。这些损耗区被定位成：i）在两个相邻信号导体之间的区域中的相邻的两列之间，该两个相邻的信号导体中的每一个位于相邻两列的不同列中；2）在相邻的接地导体之间，该两个相邻的接地导体中的每一个位于该两相邻列中的一列中。

附图说明

[0021] 附图并没有按照比例绘制。在附图中，不同图中的相同或近似相同的部件由同样的附图标记表示。为清楚起见，并没有标识每张图中的每个组件。在附图中：

[0022] 图 1 是根据本发明一个实施例的电互连系统的立体图；

[0023] 图 2A 和 2B 是形成图 1 的电连接器的一部分的晶片的第一和第二侧视图；

[0024] 图 2C 是图 2B 中所示的晶片沿线 2C-2C 的剖面图；

[0025] 图 3 是根据本发明一个实施例的堆叠到一起的多个晶片的剖面示意图；

[0026] 图 4A 是根据本发明一个实施例的用于连接器制作的引线框架的平面图；

[0027] 图 4B 是图 4A 中由箭头 4B-4B 圈定的区域的放大详图；

[0028] 图 5A 根据本发明一个实施例的底板连接器的剖面示意图；

[0029] 图 5B 是图 5A 中所示的底板连接器沿 5B-5B 线的剖面示意图；

[0030] 图 6A-6C 是根据本发明一个实施例用于底板连接器的制作的导体的放大详图；

[0031] 图 7A 是根据本发明一个实施例的两个晶片的剖面示意图；

[0032] 图 7B 是根据本发明一个实施例的两个晶片的示意图；

[0033] 图 8 是根据本发明的替代实施例的电连接器的两个晶片的剖面示意图；

[0034] 图 9A-9C 是根据本发明的若干实施例的晶片的损耗材料部的剖面示意图；以及

[0035] 图 10A 和 10B 示出了损耗区的替代实施例。

具体实施方式

[0036] 本发明并不限于下文中描述或由图中显示的部件配置及构造细节的应用。本发明可以由其他实施例实现或以不同方式使用。而且，这里使用的术语和措词只是为描述的目的，而不应理解为限制。本文中的“包括”、“包含”、“具有”、“含有”或“涉及”及其变体的使用意味着包括此后列出的项目和其等效项目以及附加项目。

[0037] 参照图 1，示出了一具有两个连接器的电互连系统 100。该电互连系统 100 包括两个子卡连接器 120 和底板连接器 150。

[0038] 子卡连接器 120 被设计成与底板连接器 150 配合，从而在底板 160 和子卡 140 之间形成导电通路。虽然没有清楚显示，但互连系统 100 可以互连具有和底板 160 上的相似底板连接器配合的子卡连接器的多个子卡。因此，通过互连系统连接的部件的数量和类型不作为对本发明的限制。

[0039] 图 1 示出了一个使用直角底板连接器的互连系统。应当理解的是，在其他实施例中，因为本发明可被广泛用于许多种类型的电子连接器，所以电子互连系统 100 还可以包括其他连接器的种类和组合，诸如直角连接器，夹层 (mezzanine) 连接器，卡缘连接器和芯片插座。

[0040] 底板连接器 150 和子连接器 120 各包括导电元件。子卡连接器 120 的导电元件耦合到迹线（其中标注了迹线 142）、接地面或子卡 140 中的其他导电元件。这些迹线载有电信号，而接地面为子卡 140 上的组件提供基准电平。由于任何电压值都可以作为基准值，所以接地面的电压可以是地电压，或相比地电压正或负的电压。

[0041] 类似的，底板连接器 150 中的导电元件也耦合到迹线（其中标注了迹线 162）、接地

面或底板 160 上的其他导电元件。当子卡连接器 120 和底板连接器 150 配合时，这两个连接器的导电元件配合以在底板 160 和子卡 140 的导电元件之间建立导电通路。

[0042] 底板连接器 150 包括底板罩 158 和多个导电元件（参见图 6A-6C）。底板连接器 150 的导电元件延伸通过底板罩 158 的底部 514，在底部 514 的上下各有一部分。此处导电元件在底部 514 上延伸的部分形成配合触点，这些配合触点被共同示为配合触点部分 154，其适于与子卡连接器 120 相应的导电元件配合。在所描述的实施例中，配合触点 154 是叶片接触的形式，但还可以使用其他适合的接触配置，因为本发明并不限于此。

[0043] 共同示为接触尾部 156 的导电元件的尾部在罩底部 514 下延伸，且适于附连至底板 160。这里，该尾部是压配形式，安装于共同显示为底板 160 上的通孔 164 的通孔内的“针眼”顺应部分。然而，其他结构也是合适的，诸如表面安装元件，弹簧触点，可焊接引脚等，因为本发明并不局限于这个方面。

[0044] 在所示的实施例中，底板罩 158 由诸如塑料或尼龙之类的介电材料模制。合适的材料例如液晶聚合物 (LCP)，聚苯硫醚 (PPS)，高温尼龙或聚丙烯 (PPO)。其他适合的材料可以被采用，因为本发明不限于这方面。所有这些材料适合于在制造根据本发明的连接器时的粘合剂材料。用于形成底板罩 158 的粘合剂材料中的某些或全部可包括一种或多种填充物，以控制底板罩 150 的电学或机械性能。例如，可以使用 30％容量被玻璃纤维填充的热塑 PPS 来形成罩 158。

[0045] 在所示实施例中，通过对底板罩 158 模制接收导电元件的开口来制作底板连接器 150。导电元件被形成为具有倒钩或其它保持部，以当插入底板罩 158 的开口时将导电元件保持于适当的位置。

[0046] 如图 1 和图 5A 所示，底板罩 158 还包括侧壁 512，其沿底板罩 158 相对面的长度延伸。侧壁 512 包括沟槽 172，其沿侧壁 512 的内表面垂直地延伸。沟槽 172 通过配合突出部 132 引导子卡连接器 120 的前外壳 130 进入罩 158 的合适位置中。

[0047] 子卡连接器 120 包括耦合到一起的多个晶片 $122_1 \ldots 122_6$，其中每一个都具有外壳 260（参见图 2A-2C）和一列导电元件。在描述的实施例中，每一列都有多个信号导体 420（参见图 4A）和多个接地导体 430（参见图 4A）。这些接地导体应用于每个晶片 $122_1 \ldots 122_6$ 以使信号导体间的串扰最小或控制连接器的电性能。

[0048] 晶片 $122_1 \ldots 122_6$ 可通过模制包围形成有信号导体和接地导体的导电元件的外壳来形成。对于底板连接器 150 的罩 158 而言，外壳 260 可由任何合适的材料形成，可包含具有导电填充物的或产生损耗的部分。

[0049] 在所描述的实施例中，子卡连接器 120 是直角连接器，且具有横越直角的导电元件。因此，导电元件的相对端从晶片 $122_1 \ldots 122_6$ 的直角边缘延伸。

[0050] 晶片 $122_1 \ldots 122_6$ 的各个导电元件具有连接到子卡 140 的至少一个接触尾部，其共同显示为接触尾部 126。子卡连接器 120 中的各个导电元件还具有一个连接到底板连接器 150 中的相应导电元件的配合接触部，其共同显示为配合接触部 124。各个导电元件还具有在配合接触部和接触尾部之间的中间部，其可以由晶片外壳 260（参看图 2）封装或内嵌。

[0051] 接触尾部 126 将子卡连接器 120 中的导电元件电连接至子卡 140 中诸如迹线 142 之类的导电元件。在所描述的实施例中，接触尾部 126 压配“针眼”接触，其通过子卡 140 中的通孔来建立电接触。然而，其他的适合接触机制也可以代替使用或不仅仅使用通孔和压

配接触尾部。

[0052] 在所描述的实施例中，配合接触部 124 中的每个都有与底板连接器 150 的相应配合接触部 154 配合的双梁 (dual beam) 结构。作为信号导体的导电元件可以组成对，由接地导体分开以适用作为差分电连接器。然而，也可能有单端使用的实施例，其中导电元件等距，且没有分隔信号导体的指定接地导体或位于各个信号导体之间的接地导体。

[0053] 在所描述的实施例中，某些导电元件被指定为形成导体差分对，而且某些导电元件指定为接地导体。这种指定指的是导电元件在互连系统中的预期用途，正如本领域技术人员所熟知的那样。例如，虽然导电元件可能有其他用途，但差分对可基于形成该对的导体元件之间的优选耦合来确定。使该对适于传输差分信号的电性能——例如其阻抗——可提供识别差分对的可选的或附加的方法。作为另一个例子，在具有差分对的连接器中，接地导体可以通过其相对于差分对的位置来确定。在其他的实例中，接地导体可以通过其形状或电特性来确定。例如，接地导体可以是相对宽的以提供低阻抗，这对于提供稳定的参考电位是需要的，但提供的阻抗对传输高速信号来说是其所不希望的。

[0054] 仅出于示例的目的，描述了具有六个晶片 $122_1 \ldots 122_6$ 的子卡连接器 120，其中每个晶片具有多个信号导体对和毗邻的接地导体。如图，每个晶片 $122_1 \ldots 122_6$ 包括一列导电元件。然而，本发明并不限于此，因为晶片的数量和各个晶片中信号线以及地线的数量可以因需要而改变。

[0055] 如图所示，各个晶片 $122_1 \ldots 122_6$ 被插入到前外壳 130 中，这样配合接触部 124 被插入前外壳 130 的开口中并固定。前外壳 130 中的开口被定位成使得底板连接器 150 的配合接触部 154 进入前外壳 130 的开口中，并当子卡连接器 120 与底板连接器 150 配合时允许与配合接触部 124 的电连接。

[0056] 子卡连接器 120 可包括代替前支架 130 或除该前支架 130 之外的支承件来固定晶片 $122_1 \ldots 122_6$。在图示的实施例中，加强件 128 支承多个晶片 $122_1 \ldots 122_6$。在所描述的实施例中，加强件 128 是冲压金属件，虽然加强件 128 可由任何适合的材料制作。加强件 128 可冲压有狭缝、孔、凹槽或能接合晶片的其它形状。

[0057] 各个晶片 $122_1 \ldots 122_6$ 可包括接合加强件 128 以相对于彼此定位各个晶片 122 并进一步防止晶片 122 旋转的连接部 242、244(参见图 2A-2B)。当然，本发明并不限于此，也可以不采用加强件。此外，虽然示出了加强件连接到多个晶片的上部和边部的情况，但本发明并不限于此，因为其他适合的定位也可被采用。

[0058] 图 2A-2B 示出了示例性晶片 220A 的相对侧视图。晶片 220A 可以通过注入模制材料整体或部分成形，以形成例如 410A 或 410B(图 4) 的围绕晶片带状组件的外壳 260。在描述的实施例中，晶片 220A 通过两步模制操作形成，从而允许外壳 260 由具有不同材料属性的两种材料形成。绝缘部分 240 在第一步中形成，而损耗区 250 在第二步中形成。然而，外壳 260 也可以使用其他合适的材料种类和数量。在一个实施例中，外壳 260 通过注入模制塑料在一列导体元件周围形成。

[0059] 在某些实施例中，外壳 260 可设置有毗邻信号导体 420 的开口，诸如窗口或狭缝 $264_1 \ldots 264_6$ 以及孔，其中孔 262 被标注。这些开口可用于多种用途，包括 :(i) 保证在注模过程中导体元件被正确定位，和 2) 如果需要，便于插入具有不同电特性的材料。

[0060] 为获得所需的功能特性，本发明的一个实施例将具有不同介电常数的区域选择性

地毗邻晶片的信号导体 310_1B、310_2B...310_4B 定位。例如，在图 2A-2C 中所示的实施例中，外壳 260 包括狭缝 264_1...264_6，这些狭缝将空气设置为毗邻信号导体 310_1B、310_2B...310_4B 定位。

[0061] 将空气或介电常数低于用于形成外壳 260 的其他部分的材料的材料靠近差分对的其中一半放置的能力提供了一种消除信号导体差分对的偏移的机制。电信号从信号连接器的一端传输到另一端所需的时间称为传输延迟。在某些实施例中，需要差分对中的每个信号具有相同的传输延迟，这通常被认为该差分对具有零偏。导体内的传导延迟受导体附近的材料的介电常数影响，其中更低的介电常数意味着更短的传输延迟。介电常数有时也称为相对介电常数。真空具有最低介电常数，其值为 1。空气具有相似的低介电常数，然而诸如 LCP 之类的介电材料具有稍高的介电常数。例如，LCP 的介电常数在约 2.5 到约 4.5 之间。

[0062] 信号对的各个信号导体可具有不同的物理长度，尤其是在直角连接器中。根据本发明的一个方面，为了均衡即使具有不同物理长度的不同信号对之间信号导体的传导延迟，可调节导体周围的不同介电常数的材料的相对比例。在某些实施例中，相比较短的信号对导体而言，可在更长的信号对导体旁边定位更多的空气，从而降低该信号导体周围的有效介电常数并减少其传导延迟。

[0063] 然而，随着介电常数降低，信号导体的阻抗增加。为保持信号对中的阻抗，更靠近空气的信号导体的尺寸需要在厚度或宽度上加大。这导致两个信号导体具有不同的几何外形，但沿信号对的传导延迟和阻抗分布更加平衡。

[0064] 图 2C 示出了晶片 220 沿图 2B 中的 2C-2C 线所取的截面图。如图所示，多个差分对 340_1...340_4 设置在框架 260 的绝缘部分 240 内的阵列中。在所示实施例中，该阵列在剖面上是线性阵列，从而形成导体元件列。

[0065] 狭缝 264_1...264_4 与该剖面相交，因而在图 2C 中可见。正如所示，狭缝 264_1...264_4 在各个差分对 340_1...340_4 中的较长导体旁边设置了空气区域，虽然空气只是可用于平衡连接器的具有低介电常数材料的一个示例。类似于图 2C 中所示的狭缝 264_1...264_4 的区域可采用介电常数比用于形成外壳 260 的其他部分的塑料更低的塑料形成。作为另一个示例，可使用不同类型或量的填充物来形成较低介电常数的区域。例如，较低介电常数区域可由具有比其他区域更少的玻璃纤维加强件的塑料来模制。

[0066] 图 2C 还示出了用于某些实施例的信号和接地导体的定位和相对尺寸。如图 2C 所示，信号导体 310_1A...310_4A 和 310_1B...310_4B 的中间部分嵌于外壳 260 中以形成一列。接地导体 330_1...330_4 的中间部分也被保持在外壳 260 的同一列中。

[0067] 接地导体 330_1、330_2 和 330_3 定位在该列中的两个毗邻差分对 340_1、340_2...340_4 间。在该列的一端或两端可包括附加的接地导体。正如图 2C 所示，在晶片 220A 中，列的一端定位有接地导体 330_4。如图 2C 所示，某些实施例中，每个接地导体 330_1...330_4 优选比差分对 340_1...340_4 的信号导体宽。在所示的剖面中，各个接地导体的中部的宽度等于或大于信号导体中部的宽度的 3 倍甚至更多。在该图示的实施例中，各个接地导体的宽度足以至少跨越与差分对沿该列相同的距离。

[0068] 在图示的实施例中，每个接地导体具有接近 5 倍于信号导体的宽度，以使由导电元件占据的超过 50％的列宽是由接地导体占据。在所示的实施例中，由导电元件占据的列

宽的约 70％由接地导体 $330_1 \ldots 330_4$ 占据。增加由接地导体占据的各列的百分比可降低连接器内的串扰。

[0069] 还可以使用其他技术来制造晶片 220A 以减少串扰和获得其他期望的电性能。在某些实施例中，外壳 260 的一个或多个部分由选择性改变外壳的该部分的电性质和 / 或电磁性质的材料形成，从而抑制噪声和 / 或串扰、改变信号导体的电阻或赋予晶片的信号导体以需要的电性能。

[0070] 在图 2A-2C 显示的实施例中，外壳 260 包括绝缘部 240 和损耗部 250。在一个实施例中，该损耗部 250 可包含一种由导电粒子填充的热塑性材料。该填充体使得该部分“电损耗”。在一个实施例中，该外壳的损耗区配置以降低至少两个相邻差分对 $340_1 \ldots 340_4$ 之间的串扰。外壳的该绝缘区可被配置以使该损耗部不会将由差分对 $340_1 \ldots 340_4$ 传输的信号削弱不希望的程度。

[0071] 在所关心的频率范围上传导、但具有某些损耗的材料一般被称为“损耗”材料。电损耗材料可由损耗的介电和 / 或导电材料形成。所关心的频率范围取决于所使用的连接器的系统的工作参数，但一般在 1GHz 到 25GHz 之间，虽然在某些应用中会使用更高或更低的频率。某些连接器设计可以使用只跨越这个范围一部分的频率范围，如 1 到 10GHz 或 3 到 15GHz 或 3 到 6GHz。

[0072] 电损耗材料可由传统认为是介电材料的材料形成，如在所关心的频率范围中具有约大于 0.003 的电损耗角正切的材料。“电损耗角正切”是该材料的复数介电常数的虚部与实部的比例。

[0073] 电损耗材料也可以由通常被认为是导体但在所关心的频率范围上较差、包含充分分散的颗粒或区域从而不提供高导电性的材料形成，或制备成具有在所关心的频率范围上导致较弱的体导电率的性质的材料形成。电损耗材料通常具有约 1 西门子 / 米至约 6.1×10^7 西门子 / 米、优选约 1 西门子 / 米至约 1×10^7 西门子 / 米、以及最优选约 1 西门子 / 米至约 30,000 西门子 / 米的电导率。

[0074] 电损耗材料可以是部分导电的材料，如具有约 1 欧姆 / 方块与约 10^6 欧姆 / 方块之间的表面电阻率的那些材料。在某些实施例中，电损耗材料具有约 1 欧姆 / 方块和约 10^3 欧姆 / 方块之间的表面电阻率。在某些实施例中，电损耗材料具有约 10 欧姆 / 方块和约 100 欧姆 / 方块之间的表面电阻率。作为一个具体的示例，该材料可具有在约 20 欧姆 / 方块到 40 欧姆 / 方块之间的表面电阻率。

[0075] 在某些实施例中，通过将包含导电颗粒的填料添加到粘合剂而形成电损耗材料。可以用作填料以形成电损耗材料的导电粒子的例子包括形成为纤维、薄片或其他颗粒的碳或石墨。粉末、薄片、纤维形式的金属或其他颗粒也可以用来提供适合的电损耗性能。另外，可以使用填料的组合物。例如，可以使用镀有金属的碳颗粒。银和镍是适用于纤维的金属镀层。涂敷的颗粒可以单独使用或与诸如碳薄片之类的其它填料组合使用。在某些实施例中，设在外壳的损耗区 250 中的导电颗粒以大体上均匀的方式分布，使得损耗部的导电性大体恒定。在另一个实施例中，损耗部 250 的第一区比第二区具有更好的导电性，因而损耗部 250 中的导电性从而损耗量将不同。

[0076] 粘合剂或基质可以是凝固、固化的、或者可以用来定位填充材料的任何材料。在某些实施例中，该粘合剂可以是一种热塑性材料，例如通常用于电连接器的制造以便于将电

损耗材料模制成所需的形状和位置，作为电连接器制造的一部分。然而，也可以使用许多其他形式的粘合剂材料。诸如环氧树脂之类的固化材料可用作粘合剂。此外，也可以用热塑性树脂或粘胶之类的材料。虽然可以使用上述的各种粘合剂材料通过在导电粒子填料周围形成粘合剂来产生电损耗材料，但本发明不限于此。例如，可以将导电粒子注入到成形的基质材料中或涂敷在成形的基质材料上，例如在塑料外壳上涂敷导电涂层。如本文所使用，术语“粘合剂”包括封装填料的材料，是被填料注入的或者是作为支持该填料的基材。

[0077] 优选该填料将以足够的体积百分率存在，以允许颗粒与颗粒之间能够产生导电路径。例如，当使用金属纤维时，该纤维可以以约 3％到 40％的体积存在。填料的数量会影响材料的导电性质。

[0078] 填充的材料可以买到，如由 Ticona 以商品名Celestran®销售的材料。也可使用诸如损耗导电碳填充的粘合剂坯料之类的损耗材料，如美国马萨诸塞州的 Techfilm of Billerica 公司销售的材料。该坯料可包括用碳颗粒填充的环氧粘合剂。粘合剂包围碳颗粒，所述碳颗粒用于坯料的增强。这样的坯料可以插入到晶片 220A 中以形成外壳的全部或部分，也可被定位成粘附至晶片中的接地导体。在某些实施例中，该坯料通过坯料中的粘合剂粘结，该粘合剂在热处理工序中被固化。可使用纺织或无纺形式、经涂敷或非经涂敷的强化纤维的各种形式，。无纺碳纤维是一种合适的材料。可采用诸如由 RTP 公司销售的定制混合物之类的其它合适的材料，因为本发明不限于这个方面。

[0079] 在图 2C 中所示的实施例中，晶片外壳 260 由两种类型的材料模制。在图示的实施例中，损耗区 250 由含有导电填料的材料形成，而绝缘部 240 则由含很少或不含导电填料的材料形成，虽然该绝缘部可能具有诸如玻璃纤维之类可以改变粘合剂材料机械性质或改变粘合剂诸如介电常数之类的其他电性能的填料。在一个实施例中，绝缘部 240 由模制塑料形成，而损耗区由含导电填料的模制塑料形成。在某些实施例中，损耗部分 250 将差分对之间的辐射衰减至充分的程度，以将串扰降低至不需要独立的金属片的程度。

[0080] 为避免信号导体 310_1A、310_1B...310_4A 以及 310_2B 之间短路和 / 或通过损耗区 250 与地短接，由合适的介电材料形成的绝缘部 240 可用来对信号导体绝缘。这些绝缘材料可以是例如添加了不导电纤维的热塑粘合剂，添加不导电纤维是为了增加强度、空间稳定性以及减少高成本粘合剂的使用量。在传统电连接器中的玻璃纤维可以占到约 30％的体积的装填量。在其他实施例中还可以使用其他材料，因为本发明不限于此。

[0081] 在图 2C 所示的实施例中，损耗区 250 包括平行区域 336 和垂直区域 334_1...334_4。在一个实施例中，垂直区域 334_1...334_4 设置于形成独立差分对 340_1...340_4 的相邻导电元件之间。

[0082] 在某些实施例中，外壳 260 的损耗区 336 和 334_1...334_4 与接地导体 330_1...330_4 一起配合对差分对 340_1...340_4 进行屏蔽以减少串扰。损耗区 336 和 334_1...334_4 通过电连接到一个或多个接地导体来进行接地。这种将损耗区与接地导体 330_1...330_4 结合的配置降低了列中的差分对之间的串扰。

[0083] 如图 2C 所示，接地导体 330_1...330_4 的一部分可通过接地导体 340_1...340_4 周围的模制部 250 来与区域 336 和 334_1...334_4 电连接。在某些实施例中，接地导体具有开口，在模制期间形成外壳的材料可经由该开口流出。例如，图 2C 所示的剖面通过接地导体 330_1 中的开口 332 截取。虽然在图 2C 的剖面中不可见，但在诸如 330_2...330_4 之类的其它接地导

体中也具有开口。

[0084] 即使形成晶片 220A 的模腔只在接地导体的一面上具有入口，但通过接地导体的开口流出的材料使得垂直部 334_1...334_4 也可以延展通过接地导体。而且，使材料通过接地导体中的开口流入作为模制工艺的一部分可辅助固定外壳 260 中的接地导体，并能增强损耗部 250 与接地导体之间的电连接。然而，还可以使用其他的合适方法来形成该垂直部 334_1...334_4，包括在接地导体 330_1...330_4 的两面都具有入口的腔中模制晶片 320A。同样，也可以采用其他方式来固定接地接触 330，因为本发明并不限于这个方面。

[0085] 用可模压材料来形成外壳的损耗区域 250 还具有其他好处。例如，可配置一处或多处损耗区处的损耗材料来设定该处的连接器的性能。例如，改变损耗区的厚度使得信号导体离损耗区 250 的间距更近或更远可以改变连接器的性能。这样，可改变一个差分对与地之间和另一差分对与地之间的电磁耦合，从而配置毗邻的差分对之间的辐射的损耗量以及那些差分对所携带的信号的损耗量。因此，根据本发明实施例的连接器能在比常规连接器更高的频率——例如 10-15GHz 的频率下使用。

[0086] 在图 2C 所示的实施例中，晶片 220A 被设计成传输差分信号。这样，各个信号通过信号导体对 310_1A 和 310_1B、...310_4A 和 310_4B 传输。优选，各个信号导体与其所在导体对中的另一个导体的距离比其距离相邻导体对中的导体更近。例如，导体对 340_1 传输一个差分信号，而导体对 340_2 传输另一差分信号。如在图 2C 的剖面中看到的那样，信号导体 310_1B 与信号导体 310_1A 比与信号导体 310_2A 更近。可在导体对之间定位垂直的损耗区域 334_1...334_4 以提供同一列中毗邻的差分对之间的屏蔽。

[0087] 损耗区还可定位成减少不同列中的毗邻对之间的串扰。图 3 示出了与图 2 类似的剖面图，但具有挨着排列的多个组件和晶片 320A、320B，从而形成多个平行的列。

[0088] 如图 3 所示，多个信号导体 340 可设置在多个列的差分对中，该多个列由挨个定位晶片形成。并不需使用相同的晶片，也可以使用不同类型的晶片。

[0089] 期望用于构造子卡连接器的所有类型的晶片具有大致相同尺寸的外壳，以使所有的晶片适合同一包封或附连至诸如加强件 128 之类的同一支承部件上（图 1）。然而，通过在不同的晶片中为信号导体、接地导体和损耗区设置不同的位置，损耗区降低串扰的量相对于其衰减信号的量将更容易配置。在一个实施例中，使用了两种类型的晶片，其在图 3 中被示为组件或晶片 320A 和 320B。

[0090] 晶片 320B 中的各个可包括与图 2A、2B 以及 2C 所示的晶片 320A 相似的结构。如图 3 所示，晶片 320B 具有多个差分对，诸如对 340_5、340_6、340_7 以及 340_8。这些信号对被保持在绝缘区内，如外壳的 240B 中。狭缝或其他结构（没有标注）也可以以狭缝 264_1...264_6 在晶片 220A 中形成的方式相同的方式在外壳中形成，来使偏移均衡（skew equalization）。

[0091] 晶片 320B 的外壳还可包括损耗区，诸如损耗部 250B。如同结合图 2C 中的晶片 320A 所描述的损耗部 250，损耗部 250B 可被定位成减少毗邻差分对之间的串扰。可以改变损耗部 250B 的形状以提供期望的串扰抑制水平，而不会产生不合需要的信号衰减量。

[0092] 在所示的实施例中，损耗区 250B 具有与差分对 340_5...340_8 的列平行的基本平行区 336B。各个损耗区还可包括从平行区域 336B 延伸的多个垂直区域 334_1B...334_5B。垂直区域 334_1B...334_5B 分开，并设置在列中的毗邻差分对之间。

[0093] 晶片 320B 还包括接地导体，如接地导体 330_5...330_9。如同晶片 320A，接地导体毗

邻差分对 340_5...340_8 定位。此外，如在晶片 320A 中一样，接地导体一般具有比信号导体更宽的宽度。在图 3 所示的实施例中，接地导体 330_5...330_8 具有和晶片 320A 中的接地导体 330_1...330_4 大致相同的形状。然而，在所示的实施例中，接地导体 330_9 的宽度小于晶片 320B 中的接地导体 330_5...330_8 的宽度。

[0094] 接地导体 330_9 更窄，从而不要求晶片 320B 有过大宽度就能提供所需的电性质。接地导体 330_9 具有正对差分对 340_8 的边缘。因此，差分对 340_8 相对于接地导体的定位类似于毗邻的差分对例如晶片 320B 中的差分对 330_8 或晶片 320A 中的差分对 340_4。因此，差分对 340_8 的电性质类似于其他差分对的电性质。通过使接地导体 330_9 比接地导体 330_8 或 330_4 更窄，可使晶片 320B 具有更小的尺寸。

[0095] 在晶片 320A 中的毗邻对 340_1 中可包括类似小的接地导体。然而，在所示的实施例中，对 340_1 是子卡连接器 120 中的所有差分对里最短的。虽然在晶片 320A 中包括窄接地导体可使差分对 340_1 的接地配置与晶片 320A 和 320B 中的毗邻差分对的配置更相似，但接地配置中差异的净效果与存在该差异的导体长度成比例。在图 3 所示的实施例中，由于差分对 340_1 相对较短，毗邻差分对 340_1 的第二接地导体可具有相对小的净效果，虽然它会改变该差分对的电特性。然而，在其他实施例中，晶片 320A 还可以包括更多的接地导体。

[0096] 图 3 示出了在使用多种类型的晶片形成子卡连接器时可能存在的更多特征。当晶片 320A 与 320B 挨着放置时，因为晶片 320A 和 320B 中的接触列具有不同的配置，相比与晶片 320B 中的毗邻的信号导体对的对齐而言，晶片 320A 中的差分对与晶片 320B 中的接地导体更近地对齐。反过来，相比晶片 320A 中的毗邻差分对而言，晶片 320B 的差分对与接地导体更近地对齐。

[0097] 例如，差分对 340_6 靠近晶片 320A 中的接地导体 330_2。同样，晶片 320A 中的差分对 340_3 靠近晶片 320B 中的接地导体 330_7。如此，来自一列中差分对的辐射更多的是与相邻列中接地导体耦合，而不是与该相邻列中的信号导体耦合。这种配置减少了相邻列中的差分对之间的串扰。

[0098] 可以以任何合适的方式形成具有不同设置的晶片。图 4A 示出了根据一个实施例的制造晶片 320A 和 320B 的步骤。在所示实施例中，形成了晶片带组件，其中各个包括了子卡连接器中的一列所需的配置的导电元件。然后在嵌入模制操作中在各个晶片带组件的导电元件周围模制外壳以形成晶片。

[0099] 为便于晶片制造，信号导体（其中标注了信号导体 420）和接地导体（其中标注了接地导体 430）如图 4A 所示固定于引线框架 400 上。如图所示，信号导体 420 和接地导体 430 附连到一个或多个载带 402 上。在一个实施例中，信号导体和接地导体在单个薄板上被冲压而用于多个晶片。该薄板可以是金属的或其他可导电并可为制作电连接器中的导电元件提供合适的机械性能的任何材料。磷青铜、铍铜和其他铜合金是可以使用的材料的示例。

[0100] 图 4A 示出了其中已冲压了晶片带组件 410A、410B 的金属薄板的一部分。晶片带组件 410A、410B 可分别用于形成晶片 320A 和 320B。在载带 402 的所需位置保留了导电元件。于是该导电元件在晶片制造过程中可更容易保持。一旦在导电元件周围模制材料，该载带可以用来分离导电元件。该晶片可被组装到任意适当大小的子板连接器上。

[0101] 图 4A 还提供了子卡晶片的导电元件的特征的更详细视图。诸如接地导体 430 之类的接地导体，相对于诸如信号导体 420 之类的信号导体的宽度是明显的。此外，接地导体

中诸如开口 332 之类的开口是可见的。

[0102] 图 4A 中示出的晶片带组件提供可用于晶片制造的部件的仅一个实例。例如，在图 4A 中所示的实施例中，引线框架 400 包括将信号导体 420 和 / 或接地带 430 的不同部分连接至引线框架 400 的连接条 452、454 以及 456。这些连接条在随后的制作流程中可用于提供电分离的导电元件。可冲压金属薄板以使得在其他位置形成一个或多个额外的载带、和 / 或在导电元件间使用桥接元件来定位或支承制造期间的导电元件。图 4A 中所示的细节只是说明性的而并不作为本发明的限制。

[0103] 虽然引线框架 400 被示为包括了接地导体 430 和信号导体 420，但本发明并不限于此。例如，各个导体可形成在两个独立的引线框架中。事实上，可以不需要引线框架而在制作期间采用单独的导电元件。应当理解的是，完全无需在一个或两个引线框架上或独立的导电元件上执行模制，因为晶片可通过将接地导体和信号导体插入到执行的外壳部分来装配，该框架可通过咬合固定等多种部件固定到一起。

[0104] 图 4B 示出了定位于两个接地配合接触 434_1 和 434_2 之间的差分对 424_1 的配合接触末端的详图。如图所示，接地导体可具有不同尺寸的配合接触。图示的实施例具有一个大的配合接触 434_2 和一个小的配合接触 434_1。为减小每个晶片的尺寸，可在晶片的一端或两端上定位小的配合接触 434_1。

[0105] 图 4B 示出了形成子卡连接器 120 的晶片中导电元件的配合接触部分的部件。图 4B 示出了被配置为晶片 320B 的晶片的配合接触部分。所示出的部分示出了诸如可在接地导体 330_9（图 3）的端部处使用的配合接触 434_1。配合接触 424_1 可形成形成差分对 340_8（图 3）的信号导体的配合接触部。类似地，配合接触 434_2 可形成诸如接地导体 330_8 之类的接地导体的配合接触部。

[0106] 在图 4B 所示的实施例中，子卡晶片中的导电元件上的各个配合接触都是双梁接触。配合接触 434_1 包括梁 460_1 和 460_2。配合接触 424_1 包括四个梁，由啮合接触 424_1 封端的差分对的每个信号导体对应两个梁。在图 4B 中，梁 460_3 和 460_4 为差分对的一个信号导体提供了两个用于接触的梁，梁 460_5 和 460_6 为差分对的第二信号导体提供了两个用于接触的梁。类似的，配合接触 434_2 具有两个梁 460_7 和 460_8。

[0107] 每个梁包括配合面，其中梁 460_1 上的配合面 462 被标注。为在子卡连接器 120 的导电元件与底板连接器 150 的相应导电元件间建立可靠的电连接，每个梁 $460_1 \ldots 460_8$ 的形状应被设计成以足够的机械应力靠压在底板连接器 150 的相应配合接触上，从而建立可靠的电连接。每个接触采用两个梁的设计提高了即便其中一个梁损坏、污染或从有效连接中错位还能保持电连接的可能性。

[0108] 梁 $460_1 \ldots 460_8$ 的每个具有与相应接触建立电连接时产生机械力的形状。在图 4B 的实施例中，以配合接触 424_1 封端的信号导体可具有一个在晶片 320D 的外壳中的相对窄的中间部分 484_1 和 484_2。然而，为形成有效电连接，信号导体的配合接触部 424_1 应比中间部 484_1 和 484_2 宽。相应地，图 4B 示出了与各个信号导体对应的展宽部 480_1 和 480_2。

[0109] 在所示实施例中，毗邻展宽部 480_1 和 480_2 的接地导体的形状被形成为与信号导体的毗邻边缘相符合。因此，接地导体的配合接触 434_1 具有形状与展宽部 480_1 相符的互补部 482_1。同样，配合接触 434_2 具有与展宽部 480_2 互补的互补部 482_2。通过在接地导体中设置互补部，即使信号导体的宽度在配合接触区域发生变化以为梁提供需要的机械性能，信号

导体和毗邻的接地导体之间的边－边间距大致保持不变。保持一个恒定的间距可进一步为根据本发明一个实施例的互连系统提供所需的电性能。

[0110] 在制造子卡连接器 120 中为提供需要的性能采取的部分或全部技术也可以在底板连接器 150 中使用。在所示的实施例中，和子卡连接器 120 一样，底板连接器 150 包括用于提供期望的信号传输性质的部件。底板连接器 150 中的信号导体以列的形式排列，每列具有与接地导体散布的差分对。接地导体相对信号导体较宽。而且，相邻的列具有不同的配置。有些列在端部处具有窄的接地导体以节省面积，同时在列的端部处的信号导体周围提供所需的接地配置。此外，一列中的接地导体可毗邻相邻列的差分对设置，以此作为降低从一列到另一列的串扰的手段。另外，在底板连接器 150 的罩中选择性设置损耗材料来降低串扰，却不引起不期望的信号衰减水平。而且，相邻的信号导体和接地导体具有相符合的部分，从而在信号导体或接地导体的轮廓变化处，其信号到接地的间距保持不变。

[0111] 图 5A-5B 详细显示了底板连接器 150 的一个实施例。在所示的实施例中，底板连接器 150 包括具有壁 512 和底板 514 的罩 510。导电元件嵌入到罩 510 中。在所示的实施例中，各个导电元件具有在底板 514 上方延伸的部分。这些部分形成导电元件的配合接触部，这些配合接触部一起被标注为 154。每个导电元件还有在底板 514 下方延伸的部分，这些部分形成接触尾部并一起被标注为 156。

[0112] 底板连接器 150 的导电元件被定位成与子卡连接器 120 的导电元件对齐。相应地，图 5A 示出了底板连接器 150 中排列成多个平行列的导电元件。在所示实施例中，各个平行列包括信号导体的多个差分对，其中标注了差分对 540_1，540_2...540_4。各列还包括多个接地导体。在图 5A 中所示的实施例中，标注了接地导体 530_1，530_2...530_5。

[0113] 定位接地导体 530_1...530_5 和差分对 540_1...540_4 以在底板连接器 150 中形成一列导电元件。该列具有定位成与晶片 320B（图 3）中的导电元件列对齐的导电元件。底板连接器 150 中相邻的导电元件列具有和晶片 320A 中配合接触部对齐的导电元件。底板连接器 150 中的列可以从列到列改变配置从而与图 3 中显示的晶片 320A 和 320B 中的交替图案相匹配。

[0114] 接地导体 530_2、530_3 和 530_4 被显示为相对形成差分对 540_1...540_4 的信号导体较宽。与接地导体 530_2、530_3 和 530_4 相比较窄的窄接地导体元件被包括在列的各个端部处。在图 5A 所示的实施例中，窄接地导体 530_1 和 530_5 被包括在差分对 540_1...540_4 的端部，并可例如通过被设计成配合接触 434_1（图 4B）形状的配合接触部与来自子卡 120 的接地导体配合。

[0115] 图 5B 示出了沿图 5A 中的线 B-B 所取的底板连接器 150 的图示。在图 5B 的图示中，可见列 560A-560B 的交替图案。示出了含有差分对 540_1...540_4 的列 560B。

[0116] 图 5B 示出罩 510 可含有绝缘区和损耗区。在所示实施例中，差分对，诸如差分对 540_1...540_4 之类的差分对中的各个导电元件都被保持在绝缘区 522 中。损耗区 520 定位在同一列中的毗邻差分对之间，以及毗邻列的相邻差分对间。损耗区 520 可连接至诸如 530_1...530_5 之类的接地导体。侧壁 512 可以由绝缘或损耗材料制成。

[0117] 图 6A、6B 以及 6C 详细示出了可用于形成底板连接器 150 的导电元件。图 6A 示出了多条宽接地接触 530_2、530_3 和 530_4。在图 6A 中示出的配置中，接地接触附连至载带 620。该接地接触可从金属或其他导电材料长薄板（包括载带 620）冲压得来。各个接触可在制

作过程的任一合适时间期间从载带 620 分离。

[0118] 如所示，各个接地接触具有形成为叶片形状的配合接触部。为增强刚性，可在各个接触上形成一个或多个紧固结构。在图 6A 的实施例中，肋条 610 形成在各个宽接地导体中。

[0119] 诸如 530_2...530_4 之类的各个宽接地导体包括两个接触尾部。对于接地导体 530_2，标注了接触尾部 656_1 和 656_2。为每个宽接地导体提供两个接触尾部使得在整个互连系统中（包括底板 160 内）的接地结构更均匀分布，因为每个接触尾部 656_1 和 656_2 接合底板 160 中的接地通孔，该接地通孔与载有信号的通孔平行且毗邻。图 4A 示出了还可用于子卡连接器中的每个接地导体的两个接地接触尾部。

[0120] 图 6B 示出了包括诸如接地导体 530_1 和 530_5 之类的窄接地导体的冲模。与图 6A 中的所示的更宽接地导体相比，图 6B 中的更窄接地导体形成为叶片形状的配合接触部。

[0121] 与图 6A 的冲模相比，包含较窄接地的图 6B 的冲模包括载带 630 以便于处理导电元件。各个接地导体可在任何合适的时间——在插入到底板连接器罩 510 之前或之后——从载带 630 分离。

[0122] 在所示的实施例中，诸如 530_1 和 530_2 之类的各个较窄接地导体包含单个接触尾部，诸如接地导体 530_1 上的 656_3，或接地导体 530_5 上的接触尾部 656_4。即使只含有一个接地接触尾部，多个信号导体之间的关系也得以维持，这是由于图 6B 所示的窄接地导体在列的端部处使用，它们在该处毗邻单个信号导体。正如图 6B 中示出的那样，每个窄接地导体的各个接触尾部偏离配合接触的中心线，正如接触尾部 656_1 和 656_2 从宽接触的中心线偏离那样。这种配置可用来保持接地接触尾部和毗邻的信号接触尾部之间的间距。

[0123] 如图 5A 所示，在底板连接器 150 的图示实施例中，诸如 530_1 和 530_5 之类的窄接地导体也短于诸如 530_2...530_4 之类的宽接地导体。图 6B 中示出的较窄接地导体不包括紧固结构，如肋条 610（图 6A）。然而，较窄接地导体的实施例可形成有紧固结构。

[0124] 图 6C 示出了可用来形成底板连接器 150 的信号导体。图 6C 中的信号导体，如图 6A 和 6B 中的接地导体，可从金属薄片冲压得来。在图 6C 的实施例中，信号导体被冲压成对，诸如 540_1 和 540_2。图 6C 的冲压包括载带 640 以便于处理导电元件。诸如 540_1 和 540_2 之类的导体对可在制造期间的任何合适时间点从载带 640 分离。

[0125] 如图 5A、6A、6B 和 6C 所示，底板连接器 150 的信号导体和接地导体的形状可被设计成相互符合，从而在信号导体和接地导体件保持恒定的间距。例如，接地导体具有诸如突出部 660 之类的突出部，其将该接地导体相对于罩 510 的底板 514 定位。信号导体则具有诸如互补部 662（图 6C）之类的互补部，从而当毗邻接地导体的信号导体插入到罩 510 时，信号导体与接地导体边缘之间的间距即便是在该突出部 660 附近也都基本保持一致。

[0126] 同样，信号导体具有诸如突出部 664（图 6C）之类的突出部。该突出部 664 起将该信号导体保持在底板连接器罩 510（图 5A）的底板 514 内的保持部的作用。接地导体可具有互补部，如互补部 666（图 6A）。当信号导体毗邻接地导体放置时，互补部 666 在信号导体与接地导体的边缘之间保持相对均匀的间距，即便是在该突出部 664 附近。

[0127] 图 6A、6B 和 6C 示出了信号和接地导体边缘中的突出部和在毗邻的信号或接地导体中形成的相应的互补部的示例。同样可形成其他类型的突出部以及其它形状的补偿部。

[0128] 为便于使用具有互补部的信号导体和接地导体，可从反向将信号导体和接地导体插入到罩 510 来制造底板连接器 150。如图 5A 所示，接地导体的诸如 660（图 6A）之类的突

出部压靠在底板 514 的底面上。底板连接器 150 可通过将接地导体从底部插入到罩 510、直到突出部 660 接合到底板 514 的下侧来组装。因为底板连接器 150 的信号导体通常与接地导体互补，所以信号导体具有毗邻底板 514 的下表面的窄部。信号导体的较宽部毗邻底板 514 的上表面。因为当导电元件先插入罩 510 窄端时，底板连接器的制造可以简化，所以通过将信号导体从底板 514 的上表面插入罩 510 可组装底板连接器 150。信号导体可以一直插入直到诸如突出部 664 之类的突出部抵达底板的上表面。这种将导电元件从两面插入罩 510 的方法便于带有符合信号和接地导体的连接器部分的制造。

[0129] 图 7A 和 7B 示出了可用于提高连接器的电性质的制作技术的更多细节。如上所述，可在接近信号导体处选择性的定位损耗材料以降低串扰，而不致使信号导体传输的信号产生不期望的大的衰减。图 7A 示出，损耗材料区可在毗邻信号导体的接地导体边缘处缩进而作为一种减少信号衰减的方法。以接地导体 330_8 为例，接地导体 330_8 有一个面对导体对 340_8 的信号导体 7401 的边缘 720。损耗区 734 从边缘 720 缩进距离 D。

[0130] 在一个实施例中，缩进距离 D 的宽度在约 0.1mm 到约 1mm 之间。在某些实施例中，该缩进距离应尽可能大，当然不能大到让损耗区 734 变得太窄以致于它不能有效形成。然而应当理解的是，在其他实施例中，缩进距离 D 可以不同，且可取决于诸如接地导体 330_8 之类的接地导体的宽度。因此，本发明不限于这个方面。通过包括这样的缩进，由差分对 340_4 传输的共模分量的衰减相比损耗区 734 延伸到或超过边缘 720 的实施例而言降低。但是，损耗区 734 被定位成衰减将在相邻的信号导体上产生串扰的来自差分对 340_8 的辐射或将在差分对 340_8 上产生串扰的面向信号对 340_8 传播的辐射。

[0131] 由损耗区 734 离开边缘 720 缩进所产生的空间可由诸如晶片外壳的绝缘部分 240 的绝缘段 724 之类的绝缘材料填充。或者，该缩进部也可由空气或其他损耗性能不如损耗区域 734 的合适的材料填充。

[0132] 图 7B 给出了根据本发明一个实施例的连接器内的损耗材料的期望位置的理想表示。图 7B 示出了连接器内的导电元件的两个相邻列。在图 7B 中，示出了列 710A 和 710B。如图 7A 所示，各列包括接地导体，其中标注了接地导体 330_3、330_4、330_7、330_8 和 330_9。此外，该列还包括差分对，其中标注了差分对 340_3、340_4、330_7 和 330_8。图 7B 还示出了损耗区的理想设置位置，其中标注了损耗区 700_1 和 700_2。

[0133] 在所示的实施例中，损耗区占据了毗邻列中接地导体间的空间。损耗区一般处于两列的毗邻差分对之间的中心。例如，损耗区 700_1 占据列 710A 的接地导体 330_4 和列 710B 中的的接地导体 330_8 之间的空间。损耗区 700_1 位于列 710A 的差分对 340_4 和列 710B 的差分对 340_8 之间的中心处。同样，损耗区 700_2 横跨接地导体 330_3 和 330_8 之间的空间并位于差分对 340_4 和 340_7 之间的中心线附近。

[0134] 采用损耗材料的这种配置，不管是同一列中或相邻列中的相邻差分对之间的串扰将能通过损耗材料和接地导体的屏蔽效应而得以降低。然而，靠近信号导体的区域没有电损耗材料，从而限制了由差分对传输的信号的衰减量。

[0135] 对比图 7B 的示例和根据图 7A 的实施例的实例，可以看出图 7A 的实施例中描述的损耗区基本上占据了示为损耗区域的位置，如图 7B 的 700_1 和 700_2。图 7A 的配置与图 7B 的理想表示不同，从而图 7A 中的配置可以容易被模制。为便于模制，损耗区一般垂直于晶片 320A 和 320B 的主表面延伸。此外，如图 7B 中的上表面所示，所有的损耗区域从各个晶片

的一个表面延伸。和晶片的法向面成角度且与图 7B 中描述的损耗区可比拟的损耗区域由损耗材料的子区域的组合形成，其包括沿晶片上表面延伸和垂直于表面延伸的子区域。例如，区域 700 在理想情况下可使用子区域 750、750_2 和 750_5（图 7A）模制。然而，对诸如晶片 320A 和 320B 之类的晶片构造的调整可以更类似于图 7B 中显示的配置。图 8 显示了这种变化的一个例子。

[0136] 如图 8 所示，在诸如晶片 820A 和 820B 之类的晶片中加入结构，以在相邻列的接地导体之间的空间中扩展屏蔽效应。因为各个列实现于独立的晶片中，因此不存在可以覆盖相邻列的接地导体之间的全部区域的一个连续的结构。通过加入将一个晶片的损耗区域电连接到相邻晶片的损耗区域的结构，所得的结构能更接近于图 7B 中的配置，在图 7B 的配置中，诸如区域 700_1 和 700_2 之类的连续区域横跨相邻列的接地导体之间的区域并电连接到相邻列的接地导体。在图 8 所示的实施例中，通过加入弹簧夹 830 在相邻的晶片损耗区之间形成电连接。弹簧夹可以形成为来自一个或两个晶片内的接地导体上的突出部或以其他合适的方式形成。

[0137] 联系图 9A，9B 和 9C 示出了其中损耗材料的定位被配置成减少串扰而不产生不能接受的大信号衰减的其他实施例。在这些实施例中，损耗区被分成几个独立的区域，其散布在绝缘材料区中。损耗材料区可毗邻信号导体定位以减少毗邻信号导体之间的串扰。通过将损耗材料设置在选定的区域，信号导体传输的信号衰减被降低。通过合理的选择损耗材料区的配置，损耗材料可对连接器的性能产生合适的组合效果。

[0138] 图 9A-9C 示出了根据本发明替代实施例可加入晶片中的损耗材料的剖面图。这里示出的损耗材料可以加入到上述的任何电连接器组件中。损耗材料区可被损耗材料部分中的开口或孔洞分隔开。开口可采用任何合适的方式来形成。

[0139] 图 9A-9C 显示了具有上述开口的损耗材料的多种配置。该开口可在损耗材料的平行区域和垂直区域中的一个或两个中。开口可被配置为孔、缝隙、，槽或其他不含有损耗材料的合适的形状，因为本发明不限制于此方面。损耗区中的开口可以包含空气。然而，如图 2A 和 2C 所示，将损耗材料 250 和绝缘材料 240 一起模制来限定晶片的外壳 260。因此，损耗材料中的开口可由绝缘材料 240 填充。可以通过先在需要的分段中首先模制损耗材料、然后在其上模制填充该开口的绝缘材料来形成这些开口。或者，通过模制绝缘材料而形成占据将要形成开口的空间来形成开口。当在上述绝缘材料上再模制损耗材料时，损耗材料将在所需的位置处形成有开口。

[0140] 图 9A 示出了诸如晶片 320A 和 320B 之类的晶片中的损耗材料。所示的部分是差分对沿其部分长度的中段附近。沿差分对的中部的整个长度以及沿其他差分对还可以定位类似的结构部分。在图 9A 的实施例中，开口是将损耗材料分成 910_1 和 910_2 段的缝隙 938 的形式。

[0141] 每段 910_1 和 910_2 可包括平行区域 936A、936B 和一个或多个垂直区域，如垂直区域 $934_1 \ldots 934_z$。多个沟槽（其中标注了沟槽 932）可被形成为具有由平行区域 936A、936B 限定的底部和由毗邻的垂直区域 $934_1 \ldots 934_4$ 限定的侧面。各个沟槽 932 可被配置成接收差分对，以使从差分对发出的不想要的辐射或朝向差分对的辐射在损耗材料中被衰减。

[0142] 段 910_1 和 910_2 中的每个包括由诸如损耗材料中的缝隙 938 之类的开口或缝隙分隔开的多个沟槽 932 中的至少一个的至少一部分。如图所示，多个段 910_1 和 910_2 的垂直区

934_1...934_2 可相互对齐，以使沟槽 932 横跨损耗材料的诸如段 910_1 和 910_2 之类的多个段。当在诸如 320A 或 320B 之类的晶片中形成时，沟槽 932 和缝隙 938 可被用于形成晶片外壳的较低损耗的材料所占据。然而，可使用任何合适的技术形成缝隙和沟槽。

[0143] 图 9A 示出了两个段。然而，所形成的段的数量取决于影响连接器整体设计的一个或多个因素。例如，相比沿较短差分对的长度而言，在较长差分对的长度可以形成更多段。段的数量还取决于沿差分对的长度的区域的数量，在该些区域需要抑制串扰或避免信号衰减。例如，在一个差分对靠近第二差分对的区域可设置损耗材料段。相反，在信号导体与毗邻的差分对之间有相对较宽的间距处，邻近信号导体的地方需要损耗材料中的间隙以形成单独的段。此外，缝隙的数量和 / 或其长度要与差分对的长度成比例，以在邻近的各个差分对处提供大致相同长度的损耗材料。例如，这种配置可以更有效的为连接器的各个差分对提供大致相同的衰减量，而不管该差分对的长度如何。

[0144] 不考虑所需损耗区的数量、类型和大小，图 9A 的实施例只提供了一种用于在信号导体附近形成多个损耗材料区的制造技术。图 9B 示出了替代的制造技术。在图 9B 的实施例中，在损耗区之间限定分隔的损耗材料开口在垂直区域中形成。

[0145] 损耗区 920_1 和 920_2 也包括沟槽 942，其被配置成接收诸如差分对之类的信号导体。在图 9B 中所示的实施例中，损耗区 920_1 和 920_2 包括平行区 946 和垂直区域 944_1...944_4。在图 9B 的实施例中，损耗区 920_1 和 920_2 被槽口 948_1 和 948_2 分开，该槽口在垂直区域 944_1 和 944_3 以及 944_2 和 944_4 之间形成开口，从而将区域 920_1 从 920_2 分开。

[0146] 图 9C 示出了在其中形成区域的损耗材料的另一实施例。和图 9A 和 9B 的实施例一样，图 9C 示出了配置成形成沟槽 952 的损耗材料。沟槽 952 中可定位信号导体或差分对。图 9C 的实施例中的损耗材料被分成区域 920_3 和 920_4。在所示的实施例中，区域 920_3 和 920_4 被延伸穿过损耗材料的平行区域 956 的开口或孔 958 分开。在该特定实施例中，孔 958 延伸穿过损耗材料的沟槽 952。虽然示出一个大致圆形的孔，但还可使用其他尺寸或形状的孔。该孔可以拉长为形成大致沿沟槽 952 中心的槽。在其他实施例中，可在每个段沿沟槽 952 的长度方向上形成多个孔。

[0147] 区域 920_3 和 920_4 表示可沿设置在沟槽 952 中的一个或多个信号导体的长度形成的两个区域。沿该沟槽 952 内的信号导体的长度可形成任何数量的分离区域。需沿接收信号导体的沟槽的中心线形成开口，以帮助将损耗材料按图 7B 中所示的那样定位。例如，包围差分对 340_4 的损耗材料沟槽的底板中的孔将在信号对 340_4 与接地导体 330_8（图 7B）之间产生相对无损耗材料的区域。然而，平行区域 956 和垂直区域 954_1 和 954_2 中的余下的损耗材料一般位于显示为损耗区域 700_1 和 700_2 的位置处。

[0148] 图 9A-9C 证实可设计损耗区 250 的形状来控制信号损耗相对于串扰抑制的量。如图所示，损耗部 250 可包括形成多个用以接收差分对的沟槽的损耗构件。在一个实施例中，列中的信号导体可具有不同的长度，而损耗区 250 的尺寸将被调节和设置为相比较长的导体而言，在较短导体上为每个单位长度提供更高的损耗。

[0149] 图 9A-9C 中的损耗区域利用两步模制法来形成。然而，损耗材料区域可由任何合适的方法制造。图 10A 和 10B 示出了另一种制造方法。在图 10A 和 10B 的实施例中，损耗区域可通过在诸如绝缘外壳之类的衬底上先镀上一层部分导电的涂层来形成。损耗材料区通过镀损耗材料来形成。替代地，损耗区也可在相对分散的涂层中镀一层相对高导电材料

形成，以提供具有高电阻率的涂层。虽然还可以采用其他的制造方法，包括用分子线轰击基材料以改变基材料的损耗性能。

[0150] 图 10A 示出了形成其中定位了差分对的沟槽 1032 的导电区域的一部分。损耗区 1020_1 通过涂敷部分导电涂层 1010 来形成。部分导电涂层 1010 可以采用任何合适的方法来涂敷。在图示的实施例中，可采用已知的用金属或其他导电材料镀塑料的技术。

[0151] 一旦涂敷了部分导电涂层 1010，损耗区域 1020_1 可用绝缘材料进一步模制。在某些实施例中，在部分导电涂敷之后不进行进一步的晶片制造流程。

[0152] 图 10B 示出了另一个实施例。在图 10B 的实施例中，采用掩模或其他合适的制造技术来控制涂有部分导电涂层 1010 的区域。在图 10B 的实施例中，沟槽 1042 的每一面都被涂敷，但沟槽 1042 的底板未被涂敷。如图 10B 所示，采用部分导电涂层可以为损耗区的定位提供更好的控制。

[0153] 因此描述完本发明至少一个实施例的几个方面后，应当理解，可采用本领域技术人员熟知的各种变化、修改和改进。

[0154] 作为一个示例，用以传输差分信号的连接器用于说明损耗材料的选择设置，以在可接受的信号衰减水平获得所需的串扰抑制。对传输单端信号的连接器也可以采用相同的手段。此外，还可以通过将电损耗部件电容耦合到两个结构来提供屏蔽。由于不需提供直接导电路径，电损耗材料可以是不连续的，在电损耗材料段之间可以有电绝缘材料。

[0155] 此外，尽管参照子板连接器示出和描述了许多发明性方面，但应当理解本发明不限于这个方面，因为发明原理可以包括在诸如底板连接器、电缆连接器、层叠连接器、夹层连接器或芯片插座之类的其他类型的电连接器中。

[0156] 作为进一步的示例，可用列中具有四个差分信号对的连接器来描述发明原理。然而，可以使用具有任何需要数量的信号导体的连接器。

[0157] 此外，图 3 示出了接触各个接地导体的损耗材料的垂直部分，诸如部分 $334_1 \ldots 334_4$。然而，不需要各个垂直部都接触接地导体。损耗区域可以不采用直接连接来与导体或其他损耗区耦合。例如，可通过在损耗材料和实现所需耦合量的接地导体之间建立间距来提供电容耦合和合适的耦合量。而且，不需每个接地导体耦合到垂直部。在某些实施例中，列中的一个或多个接地导体附近可能没有损耗区。忽略或减少与一部分或全部接地导体耦合的垂直部的宽度将减少信号的衰减量。因此，可调节损耗区的设置和宽度以相对于对干扰信号传播的串扰、谐振和其他异常的抑制的情况下提供合适的信号衰减水平。

[0158] 这种改变、修改和改善旨在成为本发明的公开内容的一部分，且在本发明的精神和范围内。因此，上述描述和附图仅为举例。

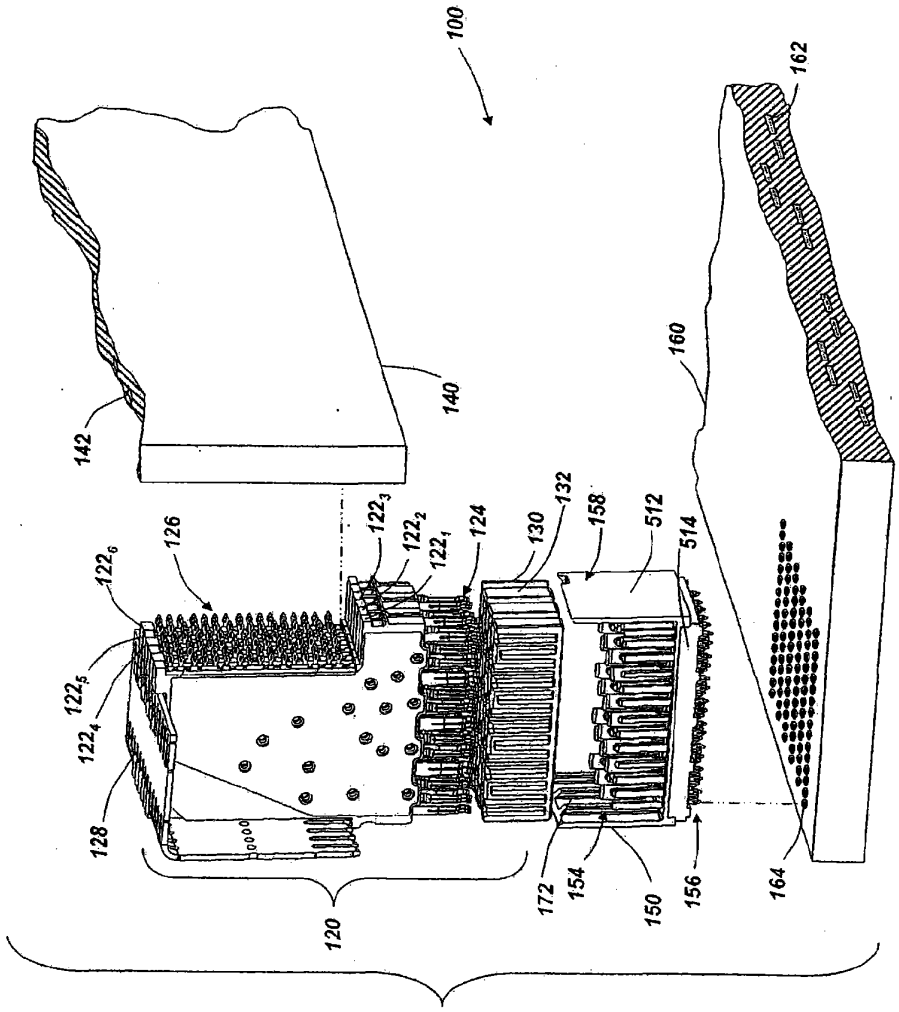

图 1

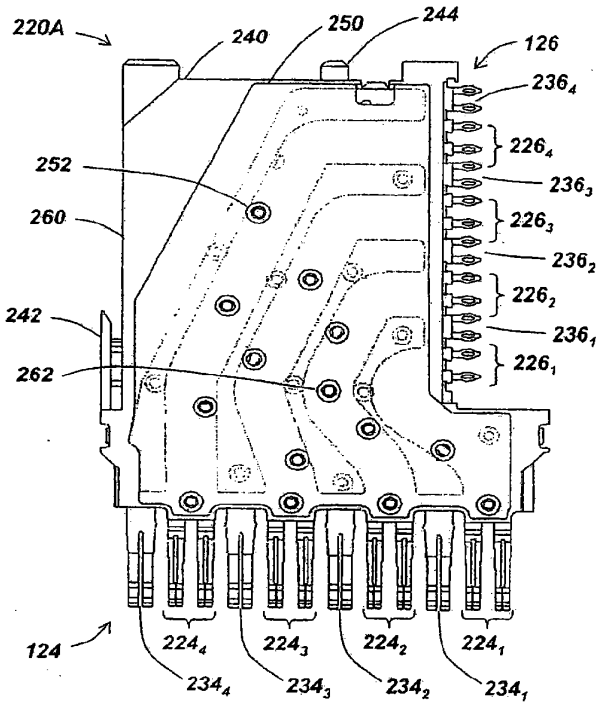

图 2A

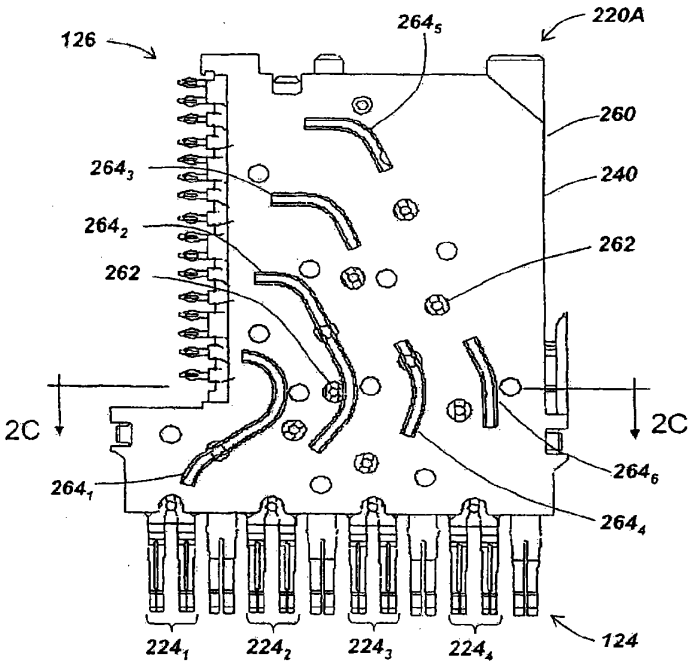

图 2B

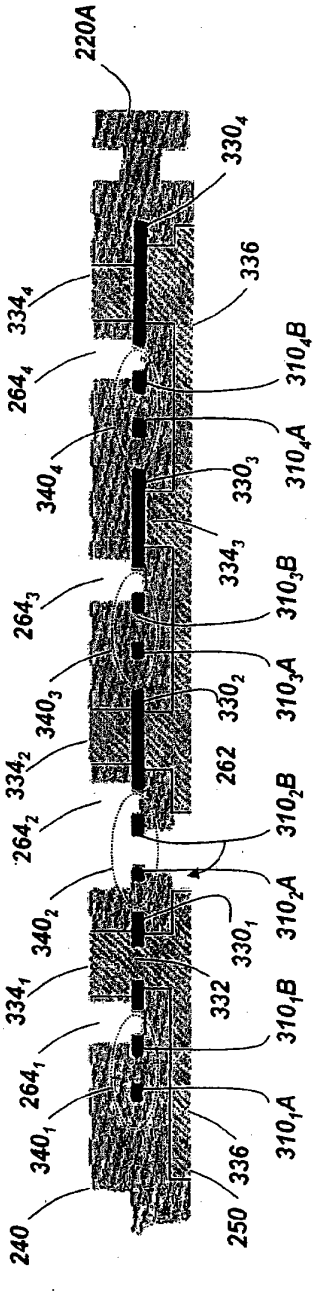

图 2C

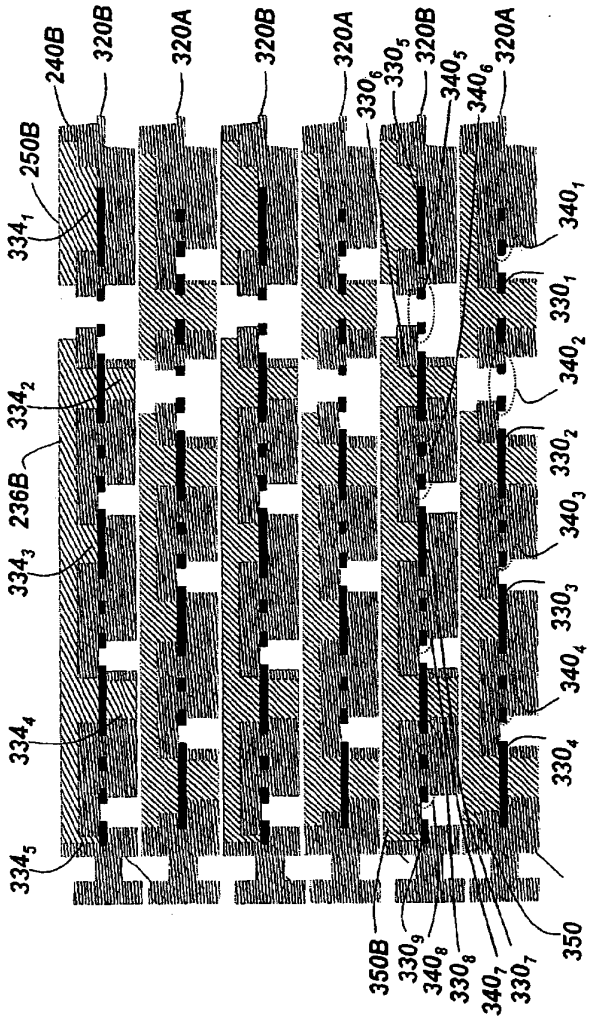

图 3

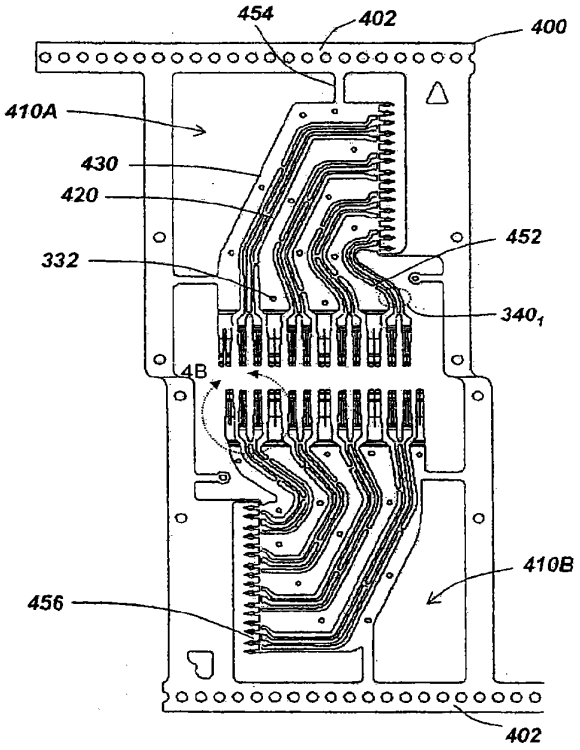

图 4A

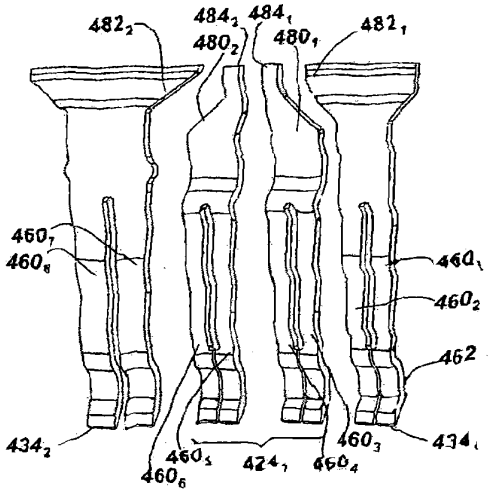

图 4B

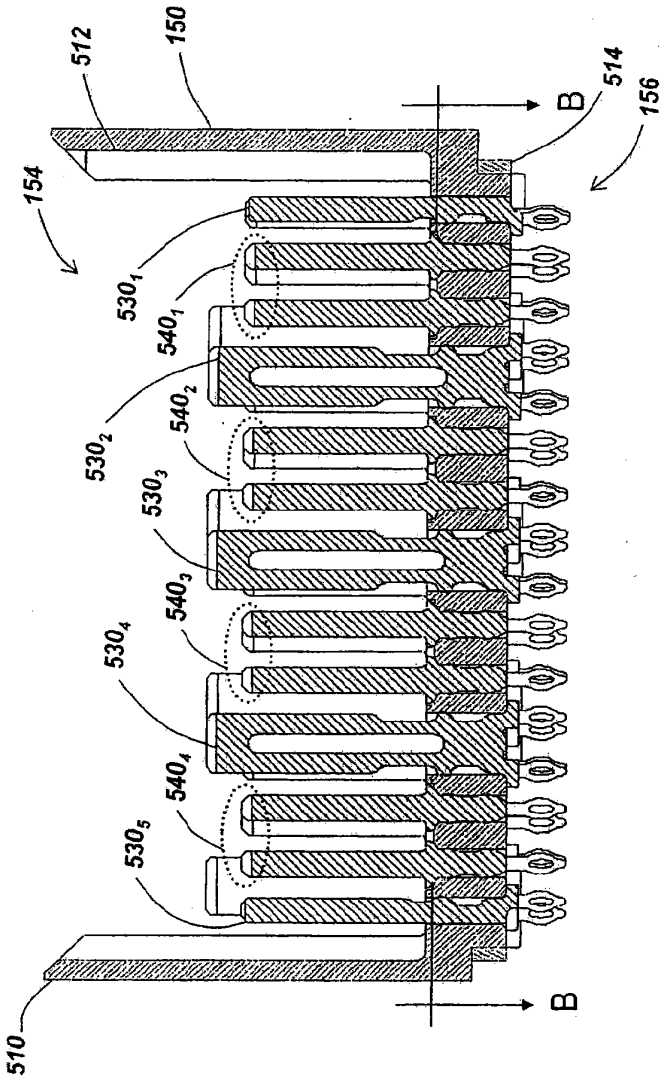

图 5A

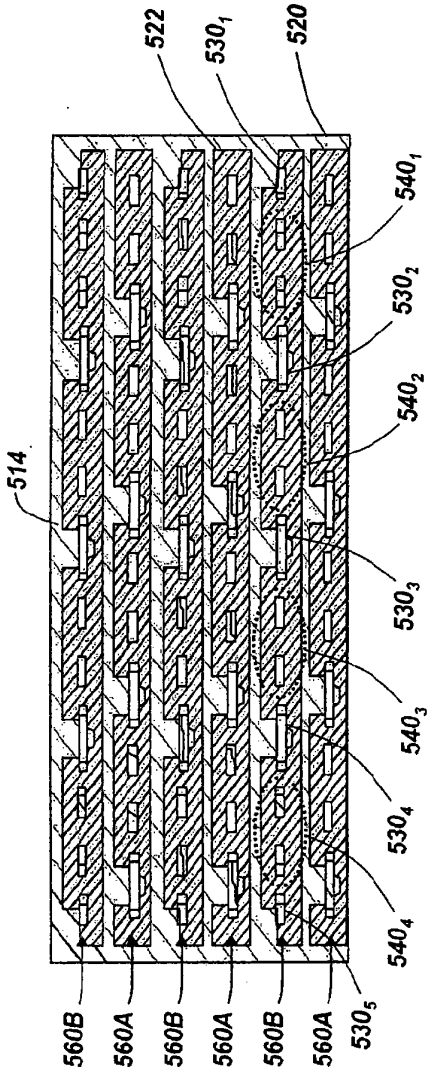

图 5B

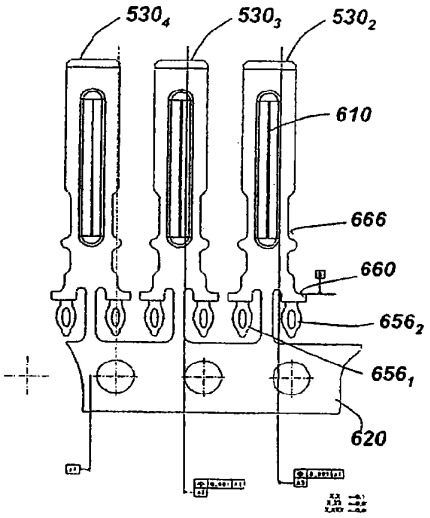

图 6A

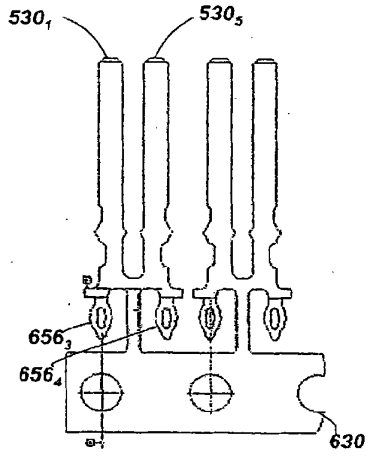

图 6B

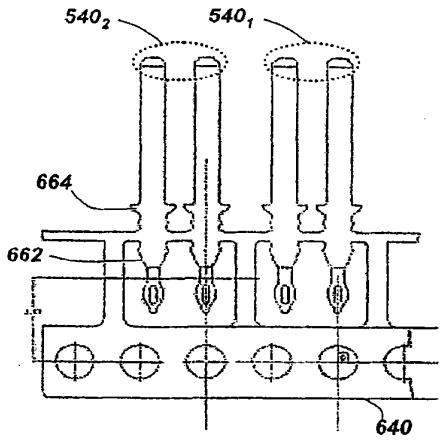

图 6C

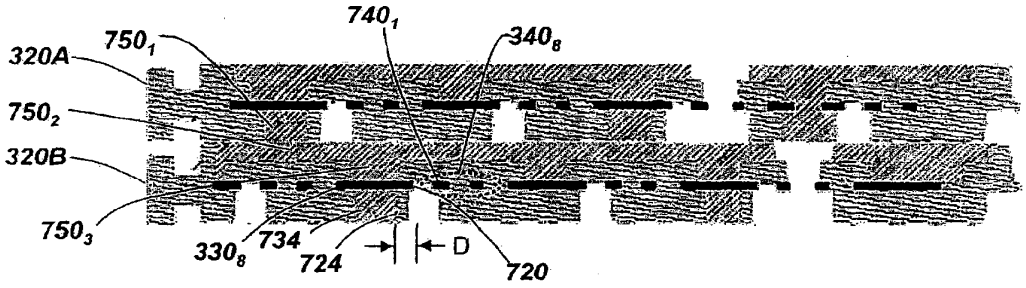

图 7A

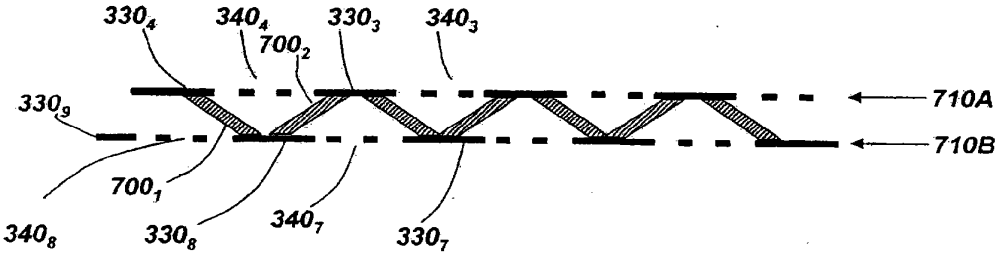

图 7B

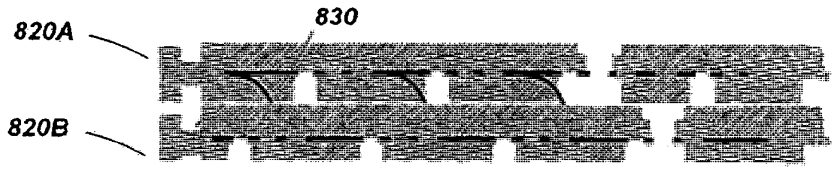

图 8

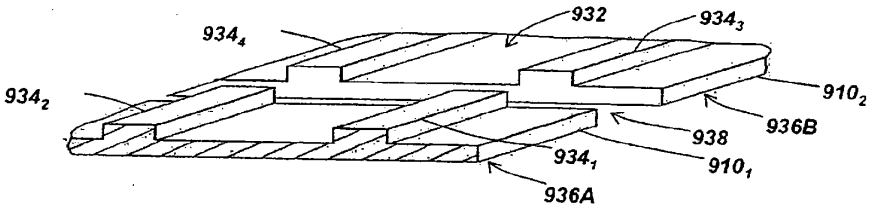

图 9A

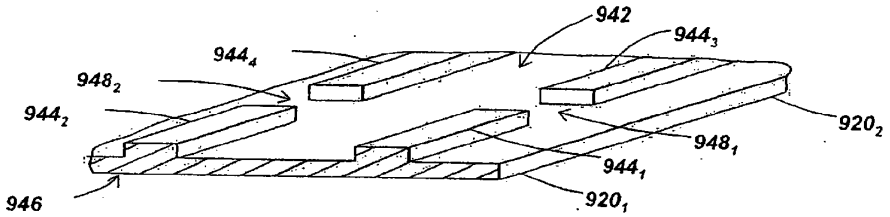

图 9B

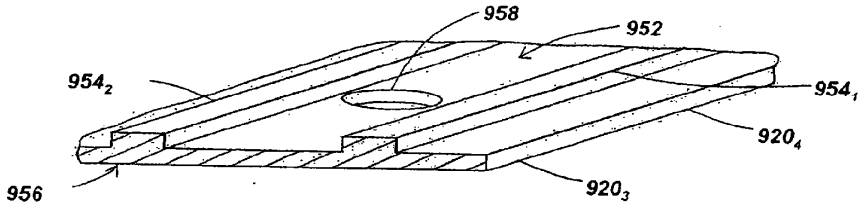

图 9C

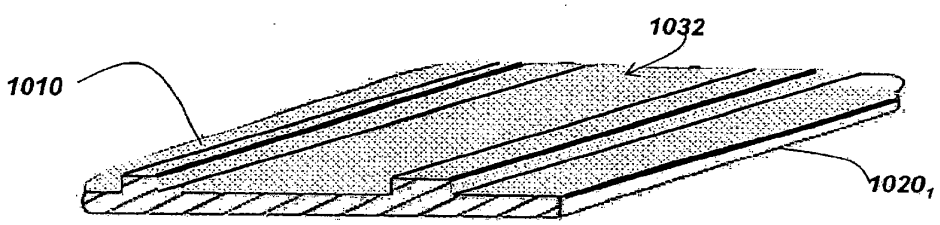

图 10A

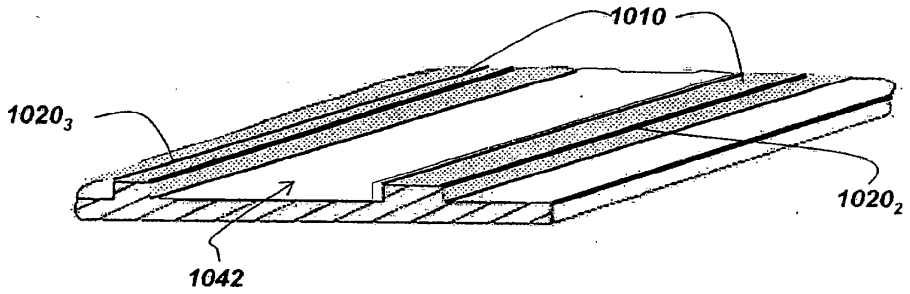

图 10B

Electronic Patent Application Fee Transmittal

Application Number:	15065683
Filing Date:	09-Mar-2016
Title of Invention:	HIGH PERFORMANCE CABLE CONNECTOR
First Named Inventor/Applicant Name:	Donald W. Milbrand
Filer:	Marcus E. Browne/Trish McDonald
Attorney Docket Number:	A0863.70051US04

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
CLAIMS IN EXCESS OF 20	1202	2	80	160
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Extension - 2 months with $0 paid	1252	1	600	600
Miscellaneous:				
Submission- Information Disclosure Stmt	1806	1	180	180
		Total in USD ($)		**940**

Electronic Acknowledgement Receipt	
EFS ID:	30868871
Application Number:	15065683
International Application Number:	
Confirmation Number:	5112
Title of Invention:	HIGH PERFORMANCE CABLE CONNECTOR
First Named Inventor/Applicant Name:	Donald W. Milbrand
Customer Number:	23628
Filer:	Marcus E. Browne/Trish McDonald
Filer Authorized By:	Marcus E. Browne
Attorney Docket Number:	A0863.70051US04
Receipt Date:	06-NOV-2017
Filing Date:	09-MAR-2016
Time Stamp:	17:54:34
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$940
RAM confirmation Number	110717INTEFSW17551700
Deposit Account	232825
Authorized User	Wolf Greenfield
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.17 (Patent application and reexamination processing fees)	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	A086370051US04-TRN-MEB.pdf	25874 acd1320ba69f7b4f31b8de437b1a4eb034cb3046	no	1
Warnings:					
Information:					
2	Extension of Time	A086370051US04-EXT-MEB.pdf	23021 a00451ec550dfd599eb9eea70ef74fa683e1bee6	no	1
Warnings:					
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Multipart Description/PDF files in .zip description

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Applicant Arguments/Remarks Made in an Amendment	8	11
Claims	2	7
Amendment/Req. Reconsideration-After Non-Final Reject	1	1

Warnings:					
Information:					
5		A086370051US04-IDS-MEB.pdf	33005 fc4e2931ef19a322b11cf30b4492cc299412dda4	yes	5

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Information:					
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Information:					
		Total Files Size (in bytes):	3767112		

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc Code: TRAN.LET
Document Description: Transmittal Letter

USED IN LIEU OF PTO/SB/21 (07-09)

TRANSMITTAL FORM *(to be used for all correspondence after initial filing)*			
		Application Number	15/065,683-Conf. #5112
		Filing Date	March 9, 2016
		First Named Inventor	Donald W. Milbrand, Jr.
		Art Unit	2833
		Examiner Name	Felix O. Figueroa
Total Number of Pages in This Submission		Attorney Docket Number	A0863.70051US04

ENCLOSURES (***Check all that apply***)

[x] Fee Transmittal Form	[ ] Drawing(s)	[ ] After Allowance Communication to TC
[ ] Fee Attached	[ ] Licensing-related Papers	[ ] Appeal Communication to Board of Appeals and Interferences
[x] Amendment/Reply	[ ] Petition	[ ] Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
[ ] After Final	[ ] Petition to Convert to a Provisional Application	[ ] Proprietary Information
[ ] Affidavits/declaration(s)	[ ] Power of Attorney, Revocation Change of Correspondence Address	[ ] Status Letter
[x] Extension of Time Request	[ ] Terminal Disclaimer	[x] Other Enclosure(s) (please Identify below):
[ ] Express Abandonment Request	[ ] Request for Refund	• Form PTO – 1449
[x] Information Disclosure Statement	[ ] CD, Number of CD(s) _____	• Copies of Cited References
[ ] Certified Copy of Priority Document(s)	[ ] Landscape Table on CD	
[ ] Reply to Missing Parts/ Incomplete Application	Remarks	
[ ] Reply to Missing Parts under 37 CFR 1.52 or 1.53		

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	WOLF, GREENFIELD & SACKS, P.C.		
Signature	/Marcus E. Browne/		
Printed name	Marcus E. Browne		
Date	November 6, 2017	Reg. No.	71,897

Certificate of Electronic Filing under 37 CFR §1.8

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being transmitted via the Office's electronic filing system in accordance with 37 CFR § 1.6(a)(4).

Dated: November 6, 2017 Electronic Signature: /Trish McDonald/

PTO/AIA/22 (03-13)
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PETITION FOR EXTENSION OF TIME UNDER 37 CFR 1.136(a)	Docket Number (Optional) A0863.70051US04
Application Number 15/065,683-Conf. #5112	Filed March 9, 2016
For HIGH PERFORMANCE CABLE CONNECTOR	
Art Unit 2833	Examiner F. O. Figueroa

This is a request under the provisions of 37 CFR 1.136(a) to extend the period for filing a reply in the above-identified application.

The requested extension and fee are as follows (check time period desired and enter the appropriate fee below):

	Fee	Small Entity Fee	Micro Entity Fee	
☐ One month (37 CFR 1.17(a)(1))	$200	$100	$50	$
☒ Two months (37 CFR 1.17(a)(2))	$600	$300	$150	$ 600.00
☐ Three months (37 CFR 1.17(a)(3))	$1,400	$700	$350	$
☐ Four months (37 CFR 1.17(a)(4))	$2,200	$1,100	$550	$
☐ Five months (37 CFR 1.17(a)(5))	$3,000	$1,500	$750	$

☐ Applicant asserts small entity status. See 37 CFR 1.27.

☐ Applicant certifies micro entity status. See 37 CFR 1.29.
Form PTO/SB/15A or B or equivalent must either be enclosed or have been submitted previously.

☐ A check in the amount of the fee is enclosed.

☒ Payment by credit card. ~~Form PTO-2038 is attached.~~

☐ The Director has already been authorized to charge fees in this application to a Deposit Account.

☒ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number 23/2825 .

☒ Payment made via EFS-Web.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

I am the

☐ applicant.

☒ attorney or agent of record. Registration number 71,897 .

☐ attorney or agent acting under 37 CFR 1.34. Registration number _____ .

/Marcus E. Browne/ — Signature
November 6, 2017 — Date

Marcus E. Browne — Typed or printed name
617.646.8000 — Telephone Number

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. Submit multiple forms if more than one signature is required, see below*.

☐ * Total of 1 forms are submitted.

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Dated: November 6, 2017 Electronic Signature: /Trish McDonald/

FEE TRANSMITTAL

Complete if known	
Application Number	15/065,683-Conf. #5112
Filing Date	March 9, 2016
First Named Inventor	Donald W. Milbrand, Jr.
Examiner Name	Felix O. Figueroa
Art Unit	2833
Practitioner Docket No.	A0863.70051US04

☐ Applicant asserts small entity status. See 37 CFR 1.27.

☐ Applicant certifies micro entity status. See 37 CFR 1.29. Form PTO/SB/15A or B or equivalent must either be enclosed or have been submitted previously.

TOTAL AMOUNT OF PAYMENT ($)940.00

METHOD OF PAYMENT (check all that apply)

☐ Check ☒ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☐ Deposit Account Deposit Account Number: 23/2825 Deposit Account Name: Wolf, Greenfield & Sacks, P.C.

For the above-identified deposit account, the Director is hereby authorized to (check all that apply):

☐ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, **except for the filing fee**

☒ Charge any additional fee(s) or underpayment of fee(s) under 37 CFR 1.16 and 1.17 ☒ Credit any overpayment of fee(s)

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FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES (U = undiscounted fee; S = small entity fee; M = micro entity fee)

	FILING FEES			SEARCH FEES			EXAMINATION FEES			
Application Type	**U ($)**	**S ($)**	**M ($)**	**U ($)**	**S ($)**	**M ($)**	**U ($)**	**S ($)**	**M ($)**	**Fees Paid ($)**
Utility	280	140*	70	600	300	150	720	360	180	
Design	180	90	45	120	60	30	460	230	115	
Plant	180	90	45	380	190	95	580	290	145	
Reissue	280	140	70	600	300	150	2,160	1,080	540	
Provisional	260	130	65	0	0	0	0	0	0	

* The $140 small entity status filing fee for a utility application is further reduced to $70 for a small entity status applicant who files the application via EFS-Web.

2. EXCESS CLAIM FEES

Fee Description	**Undiscounted Fee ($)**	**Small Entity Fee ($)**	**Micro Entity Fee ($)**
Each claim over 20 (including Reissues)	80	40	20
Each independent claim over 3 (including Reissues)	420	210	105
Multiple dependent claims	780	390	195

Total Claims		**Extra Claims**		**Fee ($)**		**Fee Paid ($)**
24	- 22 or HP =	2	x	80.00	=	160.00

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims		**Extra Claims**		**Fee ($)**		**Fee Paid ($)**
3	- 3 or HP =		x		=	

HP = highest number of independent claims paid for, if greater than 3.

Multiple Dependent Claims	
Fee ($)	**Fee Paid ($)**

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $400 ($200 for small entity) ($100 for micro entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets		**Extra Sheets**		**Number of each additional 50 or fraction thereof**		**Fee ($)**		**Fee Paid ($)**
	- 100 =		/50 =		(round **up** to a whole number) x		=	

4. OTHER FEE(S)

	Fees Paid ($)
Non-English specification, $130 fee (no small or micro entity discount)	
Non-electronic filing fee under 37 CFR 1.16(t) for a utility application, $400 fee ($200 small or micro entity)	
Other (e.g., late filing surcharge): 1806 Submission of an Information Disclosure Statement	180.00
1252 Extension for response within second month	600.00

SUBMITTED BY

Signature	/Marcus E. Browne/	Registration No. (Attorney/Agent)	71,897	Telephone	617.646.8000
Name (Print/Type)	Marcus E. Browne			Date	November 6, 2017

Certificate of Electronic Filing under 37 CFR §1.8

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being transmitted via the Office's electronic filing system in accordance with 37 CFR § 1.6(a)(4).

Dated: November 6, 2017 Electronic Signature: /Trish McDonald/

5750207.1

REMARKS

In response to the Office Action mailed June 5, 2017, Applicant respectfully requests reconsideration in view of the amendments and the following remarks. Claims 1-22 were previously pending in this application. Claim 9 has been canceled without prejudice or disclaimer. Claims 1-5, 10, 11, 14, 15, and 18-20 have been amended. New claims 23-25 have been added, As a result, claims 1-8 and 10-25 are pending for examination with claims 1, 24, and 25 being independent claims. No new matter has been added.

Support for the amendments to the claims may be found throughout Applicant's Application as Originally Filed including, for example, at paragraphs [0079]-[0101] and FIGs. 5 and 6.

INTERVIEW SUMMARY

Applicant's representative Marcus E. Browne (Reg. No. 71,897) would like to thank the Examiner for the courtesies extended during the telephone interview conducted on November 2, 2017. During the interview, the participants discussed the Information Disclosure Statement (IDS) filed on March 20, 2016 that was noted as not being considered in the Office Action mailed on June 5, 2017. The Examiner clarified that the references listed on FORM PTO-1449/A and B (hereinafter the "form") were considered on May 30, 2017. Based on the discussion, it appeared that the letter that accompanied the form was separated from the form and classified as a second, separate IDS also filed on March 20, 2016. However, there was only one IDS filed on March 20, 2016, which was considered by the Examiner.

REJECTIONS UNDER 35 U.S.C. § 103

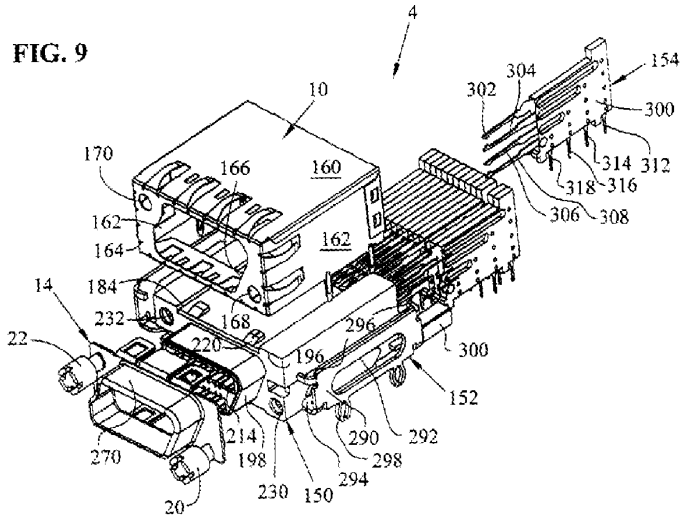
Claims 1-22 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,582,244 to Fogg et al. (hereinafter "Fogg") in view of U.S. Patent No. 7,753,731 to Cohen et al. (hereinafter "Cohen"). Without acceding to the propriety of the rejections, independent claim 1 has been amended. Reconsideration is respectfully requested in view of the foregoing amendments and the following remarks.

Independent claim 1

Independent claim 1, as amended, is directed to a "receptacle adapted for mounting to a printed circuit board" and recites, among other limitations: "a first lead assembly including: a first monolithic housing member; and a first plurality of conductive elements each comprising a contact tail adapted for attachment to the printed circuit board, a mating contact portion disposed along the first surface of the cavity, and an intermediate portion disposed in the first monolithic housing member and coupling the contact tail to the mating contact portion" where "the first surface of the cavity" in the "housing… is parallel to the circuit board." The asserted combination of Fogg and Cohen fails to teach at least these limitations.

Fogg does not teach a lead assembly with a plurality of conductors disposed in a monolithic housing and having mating contact portions disposed along a surface that is parallel to the printed circuit board. Instead, Fogg arranges "terminal assembl[ies] 154" with "mating contact portions 302, 304, 306, and 308" such that the "mating contact portions 302, 304, 306, and 308" are in a column that is ***perpendicular*** to the printed circuit board (See, e.g., Col. 5 Line 64 – Col. 7 Line 7 and FIG. 9 of Fogg). For convenience, FIG. 9 of Fogg is reproduced below:

FIG. 9



Thus, the "mating contact portions 302, 304, 306, and 308" in the "terminal assembl[ies] 154" are not disposed along a surface that is parallel to the printed circuit board. Accordingly, Fogg fails to teach "a first lead assembly including: a first monolithic housing member; and a first plurality of

conductive elements each comprising a contact tail adapted for attachment to the printed circuit board, a mating contact portion disposed along the first surface of the cavity, and an intermediate portion disposed in the first monolithic housing member and coupling the contact tail to the mating contact portion" where "the first surface of the cavity" in the "housing… is parallel to the circuit board." The proposed modification to add an insert to the receptacle of Fogg based on the teachings of Cohen fails to cure the deficiencies of Fogg. Thus, the asserted combination of Fogg and Cohen fails to teach all of the limitations of claim 1. Accordingly, withdrawal of the rejection of claim 1, and each claim that depends from claim 1, is respectfully requested.

NEW CLAIMS 23-25

New claims 23-25 are added to further clarify Applicant's contribution to the state of the art. For reasons that should be apparent from the discussion of the combination of Fogg and Cohen above, it should be appreciated that new claims 23-25 patentably distinguish over the combination of Fogg and Cohen.

GENERAL COMMENTS ON DEPENDENT CLAIMS

Since each of the dependent claims depends from a base claim that is believed to be in condition for allowance, for the sake of brevity, Applicant believes that it is unnecessary at this time to argue the further distinguishing features of the dependent claims. However, Applicant does not necessarily concur with the interpretation of the previously presented dependent claims as set forth in the Office Action, nor does Applicant concur that the basis for rejection of any of the previously presented dependent claims is proper. Therefore, Applicant reserves the right to specifically address the further patentability of the dependent claims in the future.

CONCLUSION

In view of the foregoing amendments and remarks, reconsideration is respectfully requested. This application should now be in condition for allowance; a notice to this effect is respectfully requested. If the Examiner believes, after this amendment, that the application is not in condition for allowance, the Examiner is requested to call the Applicant's attorney at the telephone number listed below.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. Applicant believes no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 23/2825 under Docket No. A0863.70051US04 from which the undersigned is authorized to draw.

Dated: November 6, 2017

Respectfully submitted,

Electronic signature: /Marcus E. Browne/
Marcus E. Browne
Registration No.: 71,897
Edmund J. Walsh
Registration No.: 32,950
WOLF, GREENFIELD & SACKS, P.C.
600 Atlantic Avenue
Boston, Massachusetts 02210-2206
617.646.8000

AMENDMENTS TO THE CLAIMS

Applicant submits below a complete listing of the current claims, including marked-up claims with insertions indicated by underlining and deletions indicated by strikeouts and/or double bracketing. This listing of claims replaces all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) A receptacle adapted for mounting to a printed circuit board, comprising:

a housing having a cavity bounded by a first surface that is parallel to the circuit board and an opposing second surface that is parallel to the circuit board;

a first lead assembly including:

a first monolithic housing member; and

a first plurality of conductive elements ~~disposed in a first housing member~~ each comprising a contact tail adapted for attachment to the printed circuit board, a mating contact portion disposed along the first surface of the cavity, and an intermediate portion disposed in the first monolithic housing member and coupling the contact tail to the mating contact portion; and

a second lead assembly including:

a second monolithic housing member; and

a second plurality of conductive elements ~~disposed in a second housing member,~~ each ~~conductive element of the first and second pluralities of conductive elements~~ comprising a contact tail adapted for attachment to the printed circuit board, a mating contact portion disposed along the second surface of the cavity, and an intermediate portion disposed in the second monolithic housing member coupling the contact tail to the mating contact portion~~, wherein the mating contact portions of the first plurality of conductive elements are disposed along the first surface of the cavity and the mating contact portions of the second plurality of conductive elements are disposed along the second surface of the cavity; and~~

~~an insert disposed between the first and second lead assemblies~~.

2. (Currently Amended) The receptacle as defined in claim 23 [[1]], wherein the insert includes an electrically lossy material.

3. (Currently Amended) The receptacle as defined in claim 23 [[1]], wherein the insert contacts selected ones of the conductive elements.

4. (Currently Amended) The receptacle as defined in claim 23 [[1]], wherein the insert includes projections towards selected ones of the conductive elements.

5. (Currently Amended) The receptacle as defined in claim 4, wherein at least one of the first and second monolithic housing members includes one or more slots for receiving the projections of the insert.

6. (Original) The receptacle as defined in claim 1, wherein the contact tails and the mating contact portions are disposed at right angles.

7. (Original) The receptacle as defined in claim 1, wherein the first plurality of conductive elements and the second plurality of conductive elements form rows of contacts on the first and second surfaces, respectively, of the cavity.

8. (Original) The receptacle as defined in claim 1, wherein the first and second surfaces of the cavity include slots configured to receive the conductive elements of the first plurality of conductive elements and the second plurality of conductive elements, respectively.

9. (Canceled)

10. (Currently Amended) The receptacle as defined in claim 1, wherein the first plurality of conductive elements is molded in the first monolithic housing member, and the second plurality of conductive elements is molded in the second monolithic housing member.

11. (Currently Amended) The receptacle as defined in claim 1, wherein the housing, the first monolithic housing member and the second monolithic housing member are made of an insulative material.

12. (Original) The receptacle as defined in claim 1, wherein the housing includes at least one projection from a lower surface thereof.

13. (Original) The receptacle as defined in claim 1, further comprising a shell adapted for attachment of the housing to the printed circuit board.

14. (Currently Amended) The receptacle as defined in claim 1, wherein the housing further comprises a second cavity bounded by a third surface and an opposing fourth surface, further comprising a third lead assembly including a third plurality of conductive elements disposed in a third monolithic housing member and a fourth lead assembly including a fourth plurality of conductive elements disposed in a fourth monolithic housing member, each conductive element of the third and fourth pluralities of conductive elements comprising a contact tail adapted for attachment to the printed circuit board, a mating contact portion and an intermediate portion coupling the contact tail to the mating contact portion, wherein the mating contact portions of the third plurality of conductive elements are disposed along the third surface of the second cavity and the mating contact portions of the fourth plurality of conductive elements are disposed along the fourth surface of the second cavity.

15. (Currently Amended) The receptacle of claim 23 [[1]], wherein:

for each conductive element of a first subset of the first plurality of conductive elements, a portion of the conductive element is exposed through the first monolithic housing member, and

for each conductive element of a second subset of the second plurality of conductive elements, a portion of the conductive element is exposed through the second monolithic housing member.

16. (Original) The receptacle of claim 15, wherein:

a first surface of the insert comprises a first plurality of projections, each projection of the first plurality of projections being coupled to a conductive element of the first subset; and

a second surface of the insert comprises a second plurality of projections, each projection of the second plurality of projections being coupled to a conductive element of the second subset.

17. (Original) The receptacle of claim 16, wherein:

the first plurality of conductive elements comprises conductive elements disposed in a plurality of pairs of conductive elements; and

the first subset of the first plurality of conductive elements comprises conductive elements each of which is disposed adjacent a pair of the plurality of pairs.

18. (Currently Amended) The receptacle of claim 23 [[1]], wherein the insert includes a conductive material.

19. (Currently Amended) The receptacle of claim 23 [[1]], wherein the insert is at least partially conductive.

20. (Currently Amended) The receptacle as defined in claim 23 [[1]], wherein:

the insert includes an electrically lossy material; and

the electrically lossy material is electrically coupled to selected ones of the first plurality of conductive elements and the second plurality of conductive elements.

21. (Original) The receptacle as defined in claim 20, wherein:

the first plurality of conductive elements are positioned in a first row, the first row comprising pairs of the first plurality of conductive elements separated by single conductive elements of the first plurality of conductive elements;

the second plurality of conductive elements are positioned in a second row, the second row comprising pairs of the second plurality of conductive elements separated by single conductive elements of the second plurality of conductive elements; and

the electrically lossy material is selectively electrically coupled to the single conductive elements of the first plurality of conductive elements and second plurality of conductive elements.

22. (Original) The receptacle as defined in claim 21, wherein:

the insert includes projections towards the selected ones of the conductive elements.

23. (New) The receptacle as defined in claim 1, further comprising an insert disposed between the first and second lead assemblies.

24. (New) A receptacle adapted for mounting to a printed circuit board, comprising:

a housing having a cavity bounded by a first surface that is parallel to the printed circuit board and a second surface that faces the first surface and is parallel to the printed circuit board;

a first lead assembly including:

a first plurality of conductive elements each comprising a mating contact portion disposed along the first surface of the cavity, a contact tail adapted for attachment to the printed circuit board and disposed at a right angle relative to the mating contact portion, and an intermediate portion coupling the contact tail to the mating contact portion; and

a first monolithic housing member molded over the intermediate portions of each conductive element of the first plurality of conductive elements; and

a second lead assembly, separate and distinct from the first lead assembly, including:

a second plurality of conductive elements each comprising a mating contact portion disposed along the second surface of the housing cavity, a contact tail adapted for attachment to the printed circuit board and disposed at a right angle relative to the mating

contact portion, and an intermediate portion coupling the contact tail to the mating contact portion; and

a second monolithic housing member molded over the intermediate portions of each conductive element of the second plurality of conductive elements.

25. (New) A receptacle adapted for mounting to a printed circuit board, comprising:

a monolithic housing made of an insulative material and having a cavity bounded by a first surface that is parallel to the printed circuit board and a second surface that faces the first surface and is parallel to the printed circuit board;

a shell adapted for attachment of the housing to the printed circuit board;

a first lead assembly including:

a first plurality of conductive elements including at least six conductive elements, each of the first plurality of conductive elements comprising a mating contact portion disposed along the first surface of the cavity, a contact tail adapted for attachment to the printed circuit board and disposed at a right angle relative to the mating contact portion, and an intermediate portion coupling the contact tail to the mating contact portion; and

a first monolithic housing member made of an insulative material and molded over the intermediate portions of each conductive element of the first plurality of conductive elements; and

a second lead assembly, separate and distinct from the first lead assembly, including:

a second plurality of conductive elements including at least six conductive elements, each of the second plurality of conductive elements comprising a mating contact portion disposed along the second surface of the housing cavity, a contact tail adapted for attachment to the printed circuit board and disposed at a right angle relative to the mating contact portion, and an intermediate portion coupling the contact tail to the mating contact portion; and

a second monolithic housing member made of an insulative material and molded over the intermediate portions of each conductive element of the second plurality of conductive elements.

PTO/SB/06 (09-11)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 15/065,683	Filing Date 03/09/2016	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)		
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	11/06/2017	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 24	Minus	** 22	= 2	X $0 =	0
	Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X $0 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
ANITA JOHNSON

PTO/SB/06 (09-11)
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 15/065,683	Filing Date 03/09/2016	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)		
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

		(Column 1)		(Column 2)	(Column 3)		
	11/06/2017	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
AMENDMENT	Total (37 CFR 1.16(i))	* 23	Minus	** 22	= 1	X $80 =	80
	Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X $420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	80

		(Column 1)		(Column 2)	(Column 3)		
		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
AMENDMENT	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
ANITA JOHNSON

UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/065,683	03/09/2016	Donald W. Milbrand JR.	A0863.70051US04	5112

23628 7590 01/05/2018
WOLF GREENFIELD & SACKS, P.C.
600 ATLANTIC AVENUE
BOSTON, MA 02210-2206

EXAMINER
FIGUEROA, FELIX O

ART UNIT	PAPER NUMBER
2833	

NOTIFICATION DATE	DELIVERY MODE
01/05/2018	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

Patents_eOfficeAction@WolfGreenfield.com
WGS_eOfficeAction@WolfGreenfield.com

Office Action Summary	Application No. 15/065,683	Applicant(s) MILBRAND ET AL.	
	Examiner FELIX O. FIGUEROA	Art Unit 2833	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11/6/2017*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-8 and 10-25* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-8 and 10-25* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

DETAILED ACTION

Notice of Pre-AIA or AIA Status

The present application is being examined under the pre-AIA first to invent provisions.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of pre-AIA 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 6-8, 10, 23 and 24 are rejected under pre-AIA 35 U.S.C. 102(B) as being anticipated by Trammel (US 6,296,496).

Trammel discloses a receptacle adapted for mounting to a printed circuit board, comprising: a housing (11) having a cavity (17) bounded by a first surface (top) that is parallel to the circuit board and an opposing second surface (bottom) that is parallel to the circuit board; a first lead assembly including a first monolithic housing member (401); and a first plurality of conductive elements (20) each comprising a contact tail (25) adapted for attachment to the printed circuit board, a mating contact portion (23) disposed along the first surface of the cavity, and an intermediate portion (21) disposed in the first monolithic housing member and coupling the contact tail to the mating contact portion; and a second lead assembly including; a second monolithic housing member (402); and a second plurality of conductive elements (20) each comprising a

contact tail (25) adapted for attachment to the printed circuit board, a mating contact portion (23) disposed along the second surface of the cavity, and an intermediate portion (21) disposed in the second monolithic housing member coupling the contact tail to the mating contact portion.

Regarding claim 6, Trammel discloses the contact tails and the mating contact portions disposed at right angles.

Regarding claim 7, Trammel discloses the first plurality of conductive elements and the second plurality of conductive elements forming rows of contacts on the first and second surfaces, respectively, of the cavity.

Regarding claim 8, Trammel discloses the first and second surfaces of the cavity include slots configured to receive the conductive elements of the first plurality of conductive elements and the second plurality of conductive elements, respectively.

Regarding claim 10, Trammel discloses the first plurality of conductive elements is molded in the first housing member, and the second plurality of conductive elements is molded in the second housing member.

Regarding claim 23, Trammel discloses an insert (30) disposed between the first and second lead assemblies.

Regarding claim 24, Trammel discloses a receptacle adapted for mounting to a printed circuit board, comprising: a housing (11) having a cavity (17) bounded by a first surface (top) that is parallel to the printed circuit board and a second surface (bottom) that faces the first surface and is parallel to the printed circuit board; a first lead

assembly including (401): a first plurality of conductive elements (20) each comprising a mating contact portion (23) disposed along the first surface of the cavity, a contact tail (25) adapted for attachment to the printed circuit board and disposed at a right angle (at least a part) relative to the mating contact portion, and an intermediate portion (21) coupling the contact tail to the mating contact portion; and a first monolithic housing member (401) molded over the intermediate portions of each conductive element of the first plurality of conductive elements; and a second lead assembly (402), separate and distinct from the first lead assembly, including: a second plurality of conductive elements (20) each comprising a mating contact portion (23) disposed along the second surface of the housing cavity, a contact tail (25) adapted for attachment to the printed circuit board and disposed at a right angle relative to the mating contact portion, and an intermediate portion (21) coupling the contact tail to the mating contact portion; and a second monolithic housing member (402) molded over the intermediate portions of each conductive element of the second plurality of conductive elements.

Claim Rejections - 35 USC § 103

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-5 and 15-22 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Trammel in view of Cohen et al. (US 7,753,731).

Regarding claim 2, Cohen teaches (in Fig. 4) the use of an insert (160) disposed between the first and second lead assemblies; the insert including an electrically lossy material. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use an insert, as taught by Cohen, in order to provide the desired shielding and reduce crosstalk between the lead assemblies/rows.

Regarding claim 3, Cohen teaches the insert contacting selected ones of the conductive elements.

Regarding claim 4, Cohen teaches the insert including projections towards selected ones of the conductive elements.

Regarding claim 5, Cohen teaches at least one of the first and second housing members including one or more slots for receiving the projections of the insert.

Regarding claim 15, Trammel, as modified by Cohen, discloses that for each conductive element of a first subset of the first plurality of conductive elements, a portion of the conductive element is exposed through the first housing member, and for each conductive element of a second subset of the second plurality of conductive elements, a portion of the conductive element is exposed through the second housing member.

Regarding claim 16, Cohen discloses a first surface of the insert comprising a first plurality of projections, each projection of the first plurality of projections being coupled to a conductive element of the first subset; and a second surface of the insert comprises a second plurality of projections, each projection of the second plurality of projections being coupled to a conductive element of the second subset.

Regarding claim 17, Cohen discloses the first plurality of conductive elements comprising conductive elements disposed in a plurality of pairs of conductive elements; and the first subset of the first plurality of conductive elements comprises conductive elements each of which is disposed adjacent a pair of the plurality of pairs.

Regarding claim 18, Cohen teaches the insert including a conductive material.

Regarding claim 19, Cohen teaches the insert being at least partially conductive.

Regarding claim 20, Cohen teaches the insert including an electrically lossy material; and the electrically lossy material is electrically coupled to selected ones of the first plurality of conductive elements and the second plurality of conductive elements.

Regarding claim 21, Trammel, as modified by Cohen, discloses the first plurality of conductive elements positioned in a first row, the first row comprising pairs of the first plurality of conductive elements separated by single conductive elements of the first plurality of conductive elements; the second plurality of conductive elements positioned in a second row, the second row comprising pairs of the second plurality of conductive elements separated by single conductive elements of the second plurality of conductive elements; and the electrically lossy material is selectively electrically coupled to the single conductive elements of the first plurality of conductive elements and second plurality of conductive elements.

Regarding claim 22, Cohen discloses the insert includes projections towards the selected ones of the conductive elements.

Claims 11-14 and 25 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Trammel in view of Fogg et al. (US 6,582,244).

Regarding claim 11, Trammel discloses the first housing member and the second housing member made of an insulative material. Fogg teaches a housing (150) made of insulating material.

Regarding claim 12, Fogg discloses the housing includes at least one projection from a lower surface thereof.

Regarding claim 13, Fogg discloses a shell (10) adapted for attachment of the housing to the printed circuit board.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the housing of insulating material with a lower projection and a shell, as taught by Fogg, in order to reduce weight and cost of the connector.

Regarding claim 14, Fogg discloses the housing further comprises a second cavity (204) bounded by a third surface (210) and an opposing fourth surface (212), further comprising a third lead assembly including a third plurality of conductive elements (306) disposed in a third housing member and a fourth lead assembly including a fourth plurality of conductive elements (308) disposed in a fourth housing member, each conductive element of the third and fourth pluralities of conductive elements comprising a contact tail adapted for attachment to the printed circuit board, a mating contact portion and an intermediate portion coupling the contact tail to the mating contact portion, wherein the mating contact portions of the third plurality of conductive elements are disposed along the third surface of the second cavity and the

mating contact portions of the fourth plurality of conductive elements are disposed along the fourth surface of the second cavity. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form additional subassemblies, as taught by Fogg, in order to provide the desire interface to transmit the desired signals.

Regarding claim 25, Trammel discloses a receptacle adapted for mounting to a printed circuit board, comprising: a monolithic housing (11) and having a cavity (17) bounded by a first surface (top) that is parallel to the printed circuit board and a second surface (bottom) that faces the first surface and is parallel to the printed circuit board; a first lead assembly (401) including: a first plurality of conductive elements (20) including at least six conductive elements, each of the first plurality of conductive elements comprising a mating contact portion disposed along the first surface of the cavity, a contact tail adapted for attachment to the printed circuit board and disposed at a right angle relative to the mating contact portion, and an intermediate portion coupling the contact tail to the mating contact portion; and a first monolithic housing member (401) made of an insulative material and molded over the intermediate portions of each conductive element of the first plurality of conductive elements; and a second lead assembly (402), separate and distinct from the first lead assembly, including: a second plurality of conductive elements including at least six conductive elements, each of the second plurality of conductive elements comprising a mating contact portion disposed along the second surface of the housing cavity, a contact tail adapted for attachment to the printed circuit board and disposed at a right angle relative to the mating contact

portion, and an intermediate portion coupling the contact tail to the mating contact portion; and a second monolithic housing member (402) made of an insulative material and molded over the intermediate portions of each conductive element of the second plurality of conductive elements.

Fogg teaches a housing (150) made of insulating material; a shell (10) adapted for attachment of the housing to the printed circuit board. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the housing of insulating material with a lower projection and a shell, as taught by Fogg, in order to reduce weight and cost of the connector.

Response to Arguments

Applicant's arguments with respect to the claims have been considered but are moot in view of the new grounds of rejection, as applied.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to FELIX O. FIGUEROA whose telephone number is (571)272-2003. The examiner can normally be reached on Mon.-Fri., 10:00am-6:00pm.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Renee Luebke can be reached on (571) 272-2009. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/FELIX O. FIGUEROA/
Primary Examiner
Art Unit 2833

Notice of References Cited	Application/Control No. 15/065,683	Applicant(s)/Patent Under Reexamination MILBRAND ET AL.	
	Examiner FELIX O. FIGUEROA	Art Unit 2833	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-6,296,496 B1	10-2001	Trammel; John D.	H01R12/725	439/79
	B	US-				
	C	US-				
	D	US-				
	E	US-				
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

FORM PTO-1449/A and B (modified PTO/SB/08)				APPLICATION NO.: 15/065,683	ATTY. DOCKET NO.: A0863.70051US04
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				FILING DATE: March 09, 2016	CONFIRMATION NO.: 5112
				FIRST NAMED INVENTOR: Donald W. Milbrand	
Sheet	1	of	1	GROUP ART UNIT: 2833	EXAMINER: Felix O. Figueroa

U.S. PATENT DOCUMENTS

Examiner's Initials #	Cite No.	U.S. Patent Document Number	Kind Code	Name of Patentee or Applicant of Cited Document	Date of Publication or Issue of Cited Document MM-DD-YYYY
		2009-0061661	A1	Shuey et al.	03-05-2009

FOREIGN PATENT DOCUMENTS

Examiner's Initials #	Cite No.	Foreign Patent Document Office/ Country	Number	Kind Code	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Translation (Y/N)
		CN	101790818	A	Framatome Connectors Int	07-28-2010	Y-abstract only
		CN	102239605	A	Amphenol Corp.	11-09-2011	Y-abstract only

OTHER ART – NON PATENT LITERATURE DOCUMENTS

Examiner's Initials #	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	Translation (Y/N)

[NOTE – No copies of U.S. patents, published U.S. patent applications, or pending, unpublished patent applications stored in the USPTO's Image File Wrapper (IFW) system, are included. See 37 CFR § 1.98 and 1287OG163. Copies of all other patent(s), publication(s), unpublished, pending U.S. patent applications, or other information listed are provided as required by 37 CFR § 1.98 unless 1) such copies were provided in an IDS in an earlier application that complies with 37 CFR § 1.98, and 2) the earlier application is relied upon for an earlier filing date under 35 U.S.C. § 120.]

EXAMINER:	DATE CONSIDERED:
/FELIX O FIGUEROA/	12/28/2017

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

5750185.1

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /F.O.F/

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15065683	MILBRAND ET AL.
	Examiner	Art Unit
	FELIX O FIGUEROA	2833

CPC- SEARCHED		
Symbol	Date	Examiner
H01R13/65807*, H01R13/6587*, H01R13/6586, H01R13/6585*, H01R13/658, H01R13/646, H01R13/6471	5/30/2017	FF
Updated search	12/27/2017	FF

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
439	607.02, 607.03, 607.05, 607.06, 607.08, 607.1	5/30/2017	FF

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

SEARCH NOTES		
Search Notes	Date	Examiner
EAST search including US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB		FF
Inventor name search	5/30/2017	FF

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

Request for Continued Examination (RCE) Transmittal		
Address to: Mail Stop RCE Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450	Application Number	15/065,683-Conf. #5112
	Filing Date	March 9, 2016
	First Named Inventor	Donald W. Milbrand, Jr.
	Art Unit	2833
	Examiner Name	F. O. Figueroa
	Attorney Docket Number	A0863.70051US04

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.

Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, to any international application that does not comply with the requirements of 35 U.S.C 371, or to any design application. See Instruction Sheet for RCEs (not to be submitted to the USPTO on page 2.)

1. Submission required under 37 CFR 1.114 Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).
   - a. [ ] Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.
     - i. [ ] Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
     - ii. [ ] Other _____
   - b. [x] Enclosed
     - i. [x] Amendment/Reply
     - ii. [ ] Affidavit(s)/ Declaration(s)
     - iii. [x] Information Disclosure Statement (IDS)
     - iv. [x] Other Copies of cited references
2. Miscellaneous
   - a. [ ] Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of _____ months. (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)
   - b. [ ] Other _____
3. Fees The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.
   - a. [ ] The Director is hereby authorized to charge the following fees, any underpayment of fees, or credit any overpayments, to Deposit Account No. 23/2825 .
     - i. [x] RCE fee required under 37 CFR 1.17(e)
     - ii. [ ] Extension of time fee (37 CFR 1.136 and 1.17)
     - iii. [ ] Other _____
   - b. [ ] Check in the amount of $ _____ enclosed
   - c. [x] Payment by credit card (~~Form PTO-2038 enclosed~~)

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

Signature	/Marcus E. Browne/	Date	April 5, 2018
Name (Print/Type)	Marcus E. Browne	Registration No.	71,897

~~CERTIFICATE OF MAILING OR TRANSMISSION~~

~~I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450 or facsimile transmitted to the U.S. Patent and Trademark Office on the date shown below.~~

~~Signature~~			
~~Name (Print/Type)~~		~~Date~~	

Certificate of Electronic Filing under 37 C.F.R. § 1.8

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being transmitted via the Office's electronic filing system in accordance with 37 C.F.R. § 1.6(a)(4).

Dated: April 5, 2018 Electronic Signature for : /Eileen M. MacKenzie/

FEE TRANSMITTAL

Complete if known	
Application Number	15/065,683-Conf. #5112
Filing Date	March 9, 2016
First Named Inventor	Donald W. Milbrand, Jr.
Examiner Name	F. O. Figueroa
Art Unit	2833
Practitioner Docket No.	A0863.70051US04

☐ Applicant asserts small entity status. See 37 CFR 1.27.

☐ Applicant certifies micro entity status. See 37 CFR 1.29. Form PTO/SB/15A or B or equivalent must either be enclosed or have been submitted previously.

TOTAL AMOUNT OF PAYMENT ($)1,300.00

METHOD OF PAYMENT (check all that apply)

☐ Check ☒ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☒ Deposit Account Deposit Account Number: 23/2825 Deposit Account Name: Wolf, Greenfield & Sacks, P.C.

For the above-identified deposit account, the Director is hereby authorized to (check all that apply):

☐ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, **except for the filing fee**

☒ Charge any additional fee(s) or underpayment of fee(s) under 37 CFR 1.16 and 1.17 ☒ Credit any overpayment of fee(s)

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FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES (U = undiscounted fee; S = small entity fee; M = micro entity fee)

	FILING FEES			SEARCH FEES			EXAMINATION FEES			
Application Type	**U ($)**	**S ($)**	**M ($)**	**U ($)**	**S ($)**	**M ($)**	**U ($)**	**S ($)**	**M ($)**	**Fees Paid ($)**
Utility	300	150*	75	660	330	165	760	380	190	
Design	200	100	50	160	80	40	600	300	150	
Plant	200	100	50	420	210	105	620	310	155	
Reissue	300	150	75	660	330	165	2,200	1,100	550	
Provisional	280	140	70	0	0	0	0	0	0	

* The $150 small entity status filing fee for a utility application is further reduced to $75 for a small entity status applicant who files the application via EFS-Web.

2. EXCESS CLAIM FEES

Fee Description	**Undiscounted Fee ($)**	**Small Entity Fee ($)**	**Micro Entity Fee ($)**
Each claim over 20 (including Reissues)	100	50	25
Each independent claim over 3 (including Reissues)	460	230	115
Multiple dependent claims	820	410	205

Total Claims		**Extra Claims**	**Fee ($)**		**Fee Paid ($)**
24	- 24 or HP =		x	=	

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims		**Extra Claims**	**Fee ($)**		**Fee Paid ($)**
3	- 3 or HP =		x	=	

HP = highest number of independent claims paid for, if greater than 3.

Multiple Dependent Claims	
Fee ($)	**Fee Paid ($)**

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $400 ($200 for small entity) ($100 for micro entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets		**Extra Sheets**		**Number of each additional 50 or fraction thereof**		**Fee ($)**		**Fee Paid ($)**
	- 100 =		/50 =		(round **up** to a whole number) x		=	

4. OTHER FEE(S)

	Fees Paid ($)
Non-English specification, $130 fee (no small or micro entity discount)	
Non-electronic filing fee under 37 CFR 1.16(t) for a utility application, $400 fee ($200 small or micro entity)	
Other (e.g., late filing surcharge): 1801 Request for continued examination (RCE) - 1st ...	1,300.00

SUBMITTED BY

Signature	/Marcus E. Browne/	Registration No. (Attorney/Agent)	71,897	Telephone	617.646.8000
Name (Print/Type)	Marcus E. Browne			Date	April 5, 2018

Certificate of Electronic Filing under 37 C.F.R. § 1.8

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being transmitted via the Office's electronic filing system in accordance with 37 C.F.R. § 1.6(a)(4).

Dated: April 5, 2018 Electronic Signature for : /Eileen M. MacKenzie/

REMARKS

In response to the Office Action mailed January 5, 2018, Applicant respectfully requests reconsideration in view of the amendments and the following remarks. Claims 1-8 and 10-25 were previously pending in this application. Claims 1, 24, and 25 have been amended. As a result, claims 1-8 and 10-25 are pending for examination with claims 1, 24, and 25 being independent claims. No new matter has been added. The application as presented is believed to be in condition for allowance.

Support for the amendments to the claims may be found throughout Applicant's Application as Originally Filed including, for example, at paragraphs [0059]-[0066] and [0079]-[0101] and FIGs. 1, 5, and 6.

REJECTIONS UNDER 35 U.S.C. §§ 102 & 103

Claims 1, 6-8, 10, 23 and 24 are rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,296,496 to Trammel (hereinafter "Trammel"). Claims 2-5 and 15-22 are rejected under 35 U.S.C. §103(a) as being unpatentable over Trammel in view of U.S. Patent No. 7,753,731 to Cohen et al. (hereinafter "Cohen"). Claims 11-14 and 25 are rejected under 35 U.S.C. §103(a) as being unpatentable over Trammel in view of U.S. Patent No. 6,582,244 to Fogg et al. (hereinafter "Fogg"). Without acceding to the propriety of the rejections, independent claims 1, 24, and 25 have been amended. Reconsideration is respectfully requested in view of the foregoing amendments and the following remarks.

Independent claim 1

Independent claim 1, as amended, is directed to a "receptacle adapted for mounting to a printed circuit board" and recites, among other limitations: "a housing having a cavity bounded by a first surface that is parallel to the printed circuit board and an opposing second surface that is parallel to the printed circuit board, each of the first and second surfaces being disposed above a first side of the printed circuit board," "a first plurality of conductive elements each comprising a contact tail… that is perpendicular to the first side of the printed circuit board," and "a second

plurality of conductive elements each comprising a contact tail… that is perpendicular to the first side of the printed circuit board." Trammel fails to teach at least these limitations.

Trammel does not teach a housing having a cavity with first and second opposing surfaces both disposed on a same side of the printed circuit board or disposing the contact tails of conductors perpendicular to the printed circuit board. Instead, the opposing surfaces of "cavities 17" in the "housing 10" are disposed on opposite sides of the "PCB 2" and the "contact tail[s] 25" are connected to "signal pads 55" on opposing sides of "the PCB 2" that are parallel to the "signal contacts 20" (see, e.g., Col. 2 Line 43 – Col 3 Line 58 and FIGs. 2 and 3). For convenience, FIGs. 2 and 3 of Trammel are reproduced below.

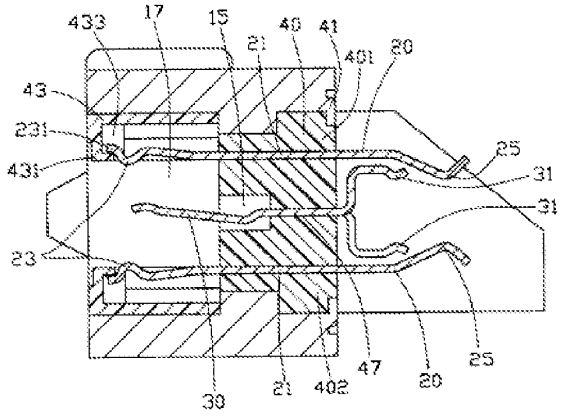

FIG. 2

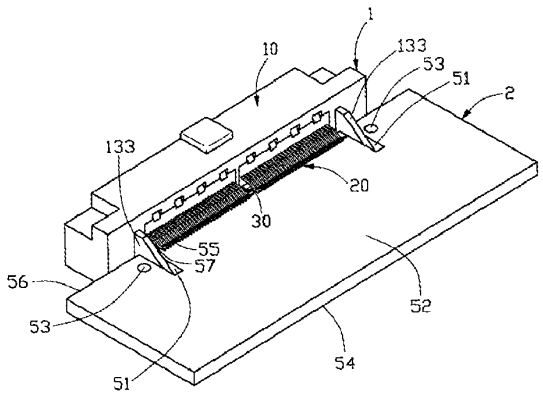

FIG. 3

Thus, the first and second opposing surfaces of the cavity 17 in Trammel are not both disposed on the same side of the PCB 2 and the contact tails 25 are not disposed perpendicular to the PCB 2. Accordingly, Trammel fails to teach "a housing having a cavity bounded by a first surface that is parallel to the printed circuit board and an opposing second surface that is parallel to the printed circuit board, each of the first and second surfaces being disposed above a first side of the printed circuit board," "a first plurality of conductive elements each comprising a contact tail… that is perpendicular to the first side of the printed circuit board," and "a second plurality of conductive elements each comprising a contact tail… that is perpendicular to the first side of the printed circuit board."

Further, one of skill in the art would have had no reason to modify Trammel to have "a first plurality of conductive elements each comprising a contact tail… that is perpendicular to the first side of the printed circuit board," and "a second plurality of conductive elements each comprising a contact tail… that is perpendicular to the first side of the printed circuit board." To the contrary, Trammel teaches a design technique to improve a connector mounted to an edge of printed circuit board. The contact tails are shaped to support that mounting configuration, such that modifying the contact tails to be as claimed would have interfered with the intended functions of the connector of Trammel such that one of skill in the art would have had no reason to make such modifications. Consequently, claim 1 is patentable over Trammel. Accordingly, withdrawal of the rejection of claim 1, and each claim that depends from claim 1, is respectfully requested.

Independent claim 24

Independent claim 24, as amended, is directed to a "receptacle adapted for mounting to a printed circuit board" and recites, among other limitations: "a first plurality of conductive elements each comprising… a contact tail adapted for attachment to the printed circuit board and disposed perpendicular to the mating contact portion, and an intermediate portion coupling the contact tail to the mating contact portion and comprising a right angle bend," and "a second plurality of conductive elements that are longer than the first plurality of conductive elements and each comprise… a contact tail adapted for attachment to the printed circuit board and disposed perpendicular to the mating contact portion, and an intermediate portion coupling the contact tail to the mating contact portion and comprising a right angle bend." Trammel fails to teach at least these limitations.

Trammel does not teach disposing the contact tails of conductors perpendicular to the mating contact portions, the conductors having a right angle bend, or the second plurality of conductive elements being longer than the first plurality of conductive elements. Instead, the "contact tail 25" of each "elongated beam 21" is substantially parallel to the "contact portion 23," the central portion of the "elongated beam 21" is straight, and the "elongated beam[s] 21" in both rows of conductors are the same length (see, e.g., Col. 2 Line 43 – Col 3 Line 58 and FIGs. 2 and 3). Thus, the contact tails 25 are not disposed perpendicular to contact portions 23, the elongated beams 21 do not

comprise a right angle bend, and the elongated beams 21 in the first row are not longer than the elongated beams 21 in the second row. Accordingly, Trammel fails to teach "a first plurality of conductive elements each comprising… a contact tail adapted for attachment to the printed circuit board and disposed perpendicular to the mating contact portion, and an intermediate portion coupling the contact tail to the mating contact portion and comprising a right angle bend," and "a second plurality of conductive elements that are longer than the first plurality of conductive elements and each comprise… a contact tail adapted for attachment to the printed circuit board and disposed perpendicular to the mating contact portion, and an intermediate portion coupling the contact tail to the mating contact portion and comprising a right angle bend."

Further, one of skill in the art would have had no reason to modify Trammel to have "a first plurality of conductive elements each comprising… a contact tail adapted for attachment to the printed circuit board and disposed perpendicular to the mating contact portion, and an intermediate portion coupling the contact tail to the mating contact portion and comprising a right angle bend," and "a second plurality of conductive elements that are longer than the first plurality of conductive elements and each comprise… a contact tail adapted for attachment to the printed circuit board and disposed perpendicular to the mating contact portion, and an intermediate portion coupling the contact tail to the mating contact portion and comprising a right angle bend." To the contrary, Trammel teaches a design technique to improve a connector mounted to an edge of printed circuit board. The conductors are shaped to support that mounting configuration, such that modifying the conductors to be as claimed would have interfered with the intended functions of the connector of Trammel such that one of skill in the art would have had no reason to make such modifications. Thus, claim 24 is patentable over Trammel. Accordingly, withdrawal of the rejection of claim 24 is respectfully requested.

Independent claim 25

Independent claim 25, as amended, is directed to a "receptacle adapted for mounting to a printed circuit board" and recites, among other limitations: "a first plurality of conductive elements" that "each… compris[e]… a contact tail adapted for attachment to at least one first hole in the printed circuit board and disposed perpendicular to the mating contact portion, and an intermediate

portion coupling the contact tail to the mating contact portion and comprising a right angle bend" and "a second plurality of conductive elements" that "each… compris[e]… a contact tail adapted for attachment to at least one second hole in the printed circuit board and disposed perpendicular to the mating contact portion, and an intermediate portion coupling the contact tail to the mating contact portion and comprising a right angle bend." The asserted combination of Trammel and Fogg fails to teach at least these limitations.

Trammel does not teach disposing the contact tails of conductors perpendicular to the mating contact portions, attaching contact tails to holes in the printed circuit board, or the conductors having a right angle bend. Instead, the "contact tail 25" of each "elongated beam 21" is substantially parallel to the "contact portion 23," the "contact tail[s] 25" are connected to "signal pads 55" by solder on opposing sides of "the PCB 2" that are parallel to the "signal contacts 20," and the central portion of the "elongated beam 21" is straight (see, e.g., Col. 2 Line 43 – Col 3 Line 58 and FIGs. 2 and 3). Thus, the contact tails 25 are not disposed perpendicular to contact portions 23, the contact tails 25 are not attached to holes in the PCB 2, and the elongated beams 21 do not comprise a right angle bend. Accordingly, Trammel fails to teach "a first plurality of conductive elements" that "each… compris[e]… a contact tail adapted for attachment to at least one first hole in the printed circuit board and disposed perpendicular to the mating contact portion, and an intermediate portion coupling the contact tail to the mating contact portion and comprising a right angle bend" and "a second plurality of conductive elements" that "each… compris[e]… a contact tail adapted for attachment to at least one second hole in the printed circuit board and disposed perpendicular to the mating contact portion, and an intermediate portion coupling the contact tail to the mating contact portion and comprising a right angle bend." The proposed modification to Trammel to construct the housing out of an insulative material and add a shell based on the teachings of Fogg fails to cure the deficiencies of Trammel. Thus, the asserted combination of Trammel and Fogg fails to teach all of the limitations of claim 25.

Further, one of skill in the art would have had no reason to modify Trammel to have "a first plurality of conductive elements" that "each… compris[e]… a contact tail adapted for attachment to at least one first hole in the printed circuit board and disposed perpendicular to the mating contact portion, and an intermediate portion coupling the contact tail to the mating contact portion and

comprising a right angle bend" and "a second plurality of conductive elements" that "each… compris[e]… a contact tail adapted for attachment to at least one second hole in the printed circuit board and disposed perpendicular to the mating contact portion, and an intermediate portion coupling the contact tail to the mating contact portion and comprising a right angle bend." To the contrary, Trammel teaches a design technique to improve a connector mounted to an edge of printed circuit board. The conductors are shaped to support that mounting configuration, such that modifying the conductors to be as claimed would have interfered with the intended functions of the connector of Trammel such that one of skill in the art would have had no reason to make such modifications. Thus, claim 25 is patentable over the combination of Trammel and Fogg. Accordingly, withdrawal of the rejection of claim 25 is respectfully requested.

GENERAL COMMENTS ON DEPENDENT CLAIMS

Since each of the dependent claims depends from a base claim that is believed to be in condition for allowance, for the sake of brevity, Applicant believes that it is unnecessary at this time to argue the further distinguishing features of the dependent claims. However, Applicant does not necessarily concur with the interpretation of the previously presented dependent claims as set forth in the Office Action, nor does Applicant concur that the basis for rejection of any of the previously presented dependent claims is proper. Therefore, Applicant reserves the right to specifically address the further patentability of the dependent claims in the future.

CONCLUSION

In view of the foregoing amendments and remarks, reconsideration is respectfully requested. This application should now be in condition for allowance; a notice to this effect is respectfully requested. If the Examiner believes, after this amendment, that the application is not in condition for allowance, the Examiner is requested to call the Applicant's attorney at the telephone number listed below.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. Applicant believes no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 23/2825 under Docket No. A0863.70051US04 from which the undersigned is authorized to draw.

Dated: April 5, 2018

Respectfully submitted,

Electronic signature: /Marcus E. Browne/
Marcus E. Browne
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AMENDMENTS TO THE CLAIMS

Applicant submits below a complete listing of the current claims, including marked-up claims with insertions indicated by underlining and deletions indicated by strikeouts and/or double bracketing. This listing of claims replaces all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) A receptacle adapted for mounting to a printed circuit board, comprising:

a housing having a cavity bounded by a first surface that is parallel to the printed circuit board and an opposing second surface that is parallel to the printed circuit board, each of the first and second surfaces being disposed above a first side of the printed circuit board;

a first lead assembly including:

a first monolithic housing member; and

a first plurality of conductive elements each comprising a contact tail adapted for attachment to the printed circuit board that is perpendicular to the first side of the printed circuit board, a mating contact portion disposed along the first surface of the cavity, and an intermediate portion disposed in the first monolithic housing member and coupling the contact tail to the mating contact portion; and

a second lead assembly including:

a second monolithic housing member; and

a second plurality of conductive elements each comprising a contact tail adapted for attachment to the printed circuit board that is perpendicular to the first side of the printed circuit board, a mating contact portion disposed along the second surface of the cavity, and an intermediate portion disposed in the second monolithic housing member coupling the contact tail to the mating contact portion.

2. (Previously presented) The receptacle as defined in claim 23, wherein the insert includes an electrically lossy material.

3. (Previously presented) The receptacle as defined in claim 23, wherein the insert contacts selected ones of the conductive elements.

4. (Previously presented) The receptacle as defined in claim 23, wherein the insert includes projections towards selected ones of the conductive elements.

5. (Previously presented) The receptacle as defined in claim 4, wherein at least one of the first and second monolithic housing members includes one or more slots for receiving the projections of the insert.

6. (Original) The receptacle as defined in claim 1, wherein the contact tails and the mating contact portions are disposed at right angles.

7. (Original) The receptacle as defined in claim 1, wherein the first plurality of conductive elements and the second plurality of conductive elements form rows of contacts on the first and second surfaces, respectively, of the cavity.

8. (Original) The receptacle as defined in claim 1, wherein the first and second surfaces of the cavity include slots configured to receive the conductive elements of the first plurality of conductive elements and the second plurality of conductive elements, respectively.

9. (Canceled)

10. (Previously presented) The receptacle as defined in claim 1, wherein the first plurality of conductive elements is molded in the first monolithic housing member, and the second plurality of conductive elements is molded in the second monolithic housing member.

11. (Previously presented) The receptacle as defined in claim 1, wherein the housing, the first monolithic housing member and the second monolithic housing member are made of an insulative material.

12. (Original) The receptacle as defined in claim 1, wherein the housing includes at least one projection from a lower surface thereof.

13. (Original) The receptacle as defined in claim 1, further comprising a shell adapted for attachment of the housing to the printed circuit board.

14. (Previously presented) The receptacle as defined in claim 1, wherein the housing further comprises a second cavity bounded by a third surface and an opposing fourth surface, further comprising a third lead assembly including a third plurality of conductive elements disposed in a third monolithic housing member and a fourth lead assembly including a fourth plurality of conductive elements disposed in a fourth monolithic housing member, each conductive element of the third and fourth pluralities of conductive elements comprising a contact tail adapted for attachment to the printed circuit board, a mating contact portion and an intermediate portion coupling the contact tail to the mating contact portion, wherein the mating contact portions of the third plurality of conductive elements are disposed along the third surface of the second cavity and the mating contact portions of the fourth plurality of conductive elements are disposed along the fourth surface of the second cavity.

15. (Previously presented) The receptacle of claim 23, wherein:

for each conductive element of a first subset of the first plurality of conductive elements, a portion of the conductive element is exposed through the first monolithic housing member, and

for each conductive element of a second subset of the second plurality of conductive elements, a portion of the conductive element is exposed through the second monolithic housing member.

16. (Original) The receptacle of claim 15, wherein:

a first surface of the insert comprises a first plurality of projections, each projection of the first plurality of projections being coupled to a conductive element of the first subset; and

a second surface of the insert comprises a second plurality of projections, each projection of the second plurality of projections being coupled to a conductive element of the second subset.

17. (Original) The receptacle of claim 16, wherein:

the first plurality of conductive elements comprises conductive elements disposed in a plurality of pairs of conductive elements; and

the first subset of the first plurality of conductive elements comprises conductive elements each of which is disposed adjacent a pair of the plurality of pairs.

18. (Previously presented) The receptacle of claim 23, wherein the insert includes a conductive material.

19. (Previously presented) The receptacle of claim 23, wherein the insert is at least partially conductive.

20. (Previously presented) The receptacle as defined in claim 23, wherein:

the insert includes an electrically lossy material; and

the electrically lossy material is electrically coupled to selected ones of the first plurality of conductive elements and the second plurality of conductive elements.

21. (Original) The receptacle as defined in claim 20, wherein:

the first plurality of conductive elements are positioned in a first row, the first row comprising pairs of the first plurality of conductive elements separated by single conductive elements of the first plurality of conductive elements;

the second plurality of conductive elements are positioned in a second row, the second row comprising pairs of the second plurality of conductive elements separated by single conductive elements of the second plurality of conductive elements; and

the electrically lossy material is selectively electrically coupled to the single conductive elements of the first plurality of conductive elements and second plurality of conductive elements.

22. (Original) The receptacle as defined in claim 21, wherein:

the insert includes projections towards the selected ones of the conductive elements.

23. (Previously presented) The receptacle as defined in claim 1, further comprising an insert disposed between the first and second lead assemblies.

24. (Currently Amended) A receptacle adapted for mounting to a printed circuit board, comprising:

a housing having a cavity bounded by a first surface that is parallel to the printed circuit board and a second surface that faces the first surface and is parallel to the printed circuit board;

a first lead assembly including:

a first plurality of conductive elements each comprising a mating contact portion disposed along the first surface of the cavity, a contact tail adapted for attachment to the printed circuit board and disposed perpendicular ~~at a right angle relative~~ to the mating contact portion, and an intermediate portion coupling the contact tail to the mating contact portion and comprising a right angle bend; and

a first monolithic housing member molded over the intermediate portions of each conductive element of the first plurality of conductive elements; and

a second lead assembly, separate and distinct from the first lead assembly, including:

a second plurality of conductive elements that are longer than the first plurality of conductive elements and each comprise ~~comprising~~ a mating contact portion disposed along the second surface of the housing cavity, a contact tail adapted for attachment to the printed circuit board and disposed perpendicular ~~at a right angle relative~~ to the mating contact

portion, and an intermediate portion coupling the contact tail to the mating contact portion and comprising a right angle bend; and

a second monolithic housing member molded over the intermediate portions of each conductive element of the second plurality of conductive elements.

25. (Currently Amended) A receptacle adapted for mounting to a printed circuit board, comprising:

a monolithic housing made of an insulative material and having a cavity bounded by a first surface that is parallel to the printed circuit board and a second surface that faces the first surface and is parallel to the printed circuit board;

a shell adapted for attachment of the housing to the printed circuit board;

a first lead assembly including:

a first plurality of conductive elements including at least six conductive elements, each of the first plurality of conductive elements comprising a mating contact portion disposed along the first surface of the cavity, a contact tail adapted for attachment to at least one first hole in the printed circuit board and disposed perpendicular ~~at a right angle relative~~ to the mating contact portion, and an intermediate portion coupling the contact tail to the mating contact portion and comprising a right angle bend; and

a first monolithic housing member made of an insulative material and molded over the intermediate portions of each conductive element of the first plurality of conductive elements; and

a second lead assembly, separate and distinct from the first lead assembly, including:

a second plurality of conductive elements including at least six conductive elements, each of the second plurality of conductive elements comprising a mating contact portion disposed along the second surface of the housing cavity, a contact tail adapted for attachment to at least one second hole in the printed circuit board and disposed perpendicular ~~at a right angle relative~~ to the mating contact portion, and an intermediate portion coupling the contact tail to the mating contact portion and comprising a right angle bend; and

a second monolithic housing member made of an insulative material and molded over the intermediate portions of each conductive element of the second plurality of conductive elements.

Docket No.: A0863.70051US04
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor:	Donald W. Milbrand, Jr.
Application No.:	15/065,683
Confirmation No.:	5112
Filed:	March 9, 2016
For:	HIGH PERFORMANCE CABLE CONNECTOR
Examiner:	F. O. Figueroa
Art Unit:	2833

Certificate of Electronic Filing under 37 CFR §1.8
I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being transmitted via the Office's electronic filing system in accordance with 37 CFR § 1.6(a)(4).

Dated: April 5, 2018 Electronic Signature for : /Eileen M. MacKenzie/

AMENDMENT WITH REQUEST FOR CONTINUED EXAMINATION

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

INTRODUCTORY COMMENTS

In response to the Office Action dated January 5, 2018, finally rejecting claims 1-8 and 10-25, please amend the above-identified U.S. patent application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 9 of this paper.

FORM PTO-1449/A and B (modified PTO/SB/08)	APPLICATION NO.: 15/065,683	ATTY. DOCKET NO.: A0863.70051US04
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	FILING DATE: March 9, 2016	CONFIRMATION NO.: 5112
	FIRST NAMED INVENTOR: Donald W. Milbrand, Jr.	
Sheet 1 of 2	GROUP ART UNIT: 2833	EXAMINER: F. O. Figueroa

U.S. PATENT DOCUMENTS

Examiner's Initials #	Cite No.	U.S. Patent Document Number	Kind Code	Name of Patentee or Applicant of Cited Document	Date of Publication or Issue of Cited Document MM-DD-YYYY
		4,632,476	A	Schell	12-30-1986
		4,806,107	A	Arnold et al.	02-21-1989
		4,846,727		Glover et al.	07-11-1989
		4,975,084	A	Fedder et al.	12-04-1990
		5,066,236	A	Broeksteeg	11-19-1991
		5,429,520		Morlion et al.	07-04-1995
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		5,433,617	A	Morlion et al.	07-18-1995
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		5,484,310	A	McNamara et al.	01-16-1996
		5,496,183		Soes et al.	03-05-1996
		6,293,827	B1	Stokoe	09-25-2001
		6,299,438	B1	Shagian et al.	10-09-2001
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		7,887,379	B2	Kirk	02-15-2011
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		8,216,001	B2	Kirk	07-10-2012
		2009-0035955	A1	McNamara	02-05-2009
		2010-0048058	A1	Morgan et al.	02-25-2010
		2011-0256739	A1	Toshiyuki et al.	10-20-2011
		2012-0184154	A1	Frank et al.	07-19-2012
		2013-0316590	A1	Hon	11-28-2013
		2015-0111427	A1	Foxconn	04-23-2015

FOREIGN PATENT DOCUMENTS

Examiner's Initials #	Cite No.	Foreign Patent Document Office/ Country	Number	Kind Code	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Translation (Y/N)
		CN	102598430	A	Amphenol Corp.	07-18-2012	Y-abstract only
		EP	2405537	A1	Hosiden Corporation	01-11-2012	

EXAMINER:	DATE CONSIDERED:

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

6208868.1

FORM PTO-1449/A and B (modified PTO/SB/08) **INFORMATION DISCLOSURE STATEMENT BY APPLICANT**				APPLICATION NO.: 15/065,683	ATTY. DOCKET NO.: A0863.70051US04
				FILING DATE: March 9, 2016	CONFIRMATION NO.: 5112
				FIRST NAMED INVENTOR: Donald W. Milbrand, Jr.	
Sheet	2	of	2	GROUP ART UNIT: 2833	EXAMINER: F. O. Figueroa

		JP	2006-344524	A	Molex Inc.	12-21-2006	Y-abstract only

OTHER ART -- NON PATENT LITERATURE DOCUMENTS

Examiner's Initials #	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	Translation (Y/N)
		International Search Report and Written Opinion for International Application No. PCT/US2017/047905 dated December 04, 2017 (A0863.70102WO00).	

[NOTE – No copies of U.S. patents, published U.S. patent applications, or pending, unpublished patent applications stored in the USPTO's Image File Wrapper (IFW) system, are included. See 37 CFR § 1.98 and 1287OG163. Copies of all other patent(s), publication(s), unpublished, pending U.S. patent applications, or other information listed are provided as required by 37 CFR § 1.98 unless 1) such copies were provided in an IDS in an earlier application that complies with 37 CFR § 1.98, and 2) the earlier application is relied upon for an earlier filing date under 35 U.S.C. § 120.]

EXAMINER:	DATE CONSIDERED:

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

6208868.1

DOCKET NO.: A0863.70051US04

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor:	Donald W. Milbrand, Jr.
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I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being transmitted via the Office's electronic filing system in accordance with 37 CFR § 1.6(a)(4).

Dated: April 5, 2018 Electronic Signature for : /Eileen M. MacKenzie/

MAIL STOP RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

STATEMENT FILED PURSUANT TO THE DUTY OF DISCLOSURE UNDER 37 C.F.R. §§ 1.56, 1.97 AND 1.98

Sir:

Pursuant to the duty of disclosure under 37 C.F.R. §§ 1.56, 1.97 and 1.98, the undersigned requests consideration of this Information Disclosure Statement.

PART I: Compliance with 37 C.F.R. § 1.97

This Information Disclosure Statement has been filed before the mailing of a first Office Action after the filing of a Request for Continued Examination under 37 C.F.R. § 1.114.

No fee or certification is required.

PART II: Information Cited

The undersigned hereby makes of record in the above-identified application the information listed on the attached form PTO-1449 (modified PTO/SB/08). The order of presentation of the references should not be construed as an indication of the importance of the references.

The undersigned hereby makes the following additional information of record in the above-identified application.

The undersigned would like to bring to the Examiner's attention the following co-pending applications that may contain subject matter related to this application:

Serial No.	Filing Date	Inventor(s)	Docket No.
*15/823,494	11-27-2017	Cohen	A0863.70063US03
*15/713,887	09-25-2017	Cartier et al.	A0863.70078US04

*A copy of this reference is not provided as the Office has waived the requirement under 37 C.F.R. § 1.98(a)(2)(iii) for submitting a copy of a cited U.S. patent application if it is scanned to the Image File Wrapper system and is available on Private PAIR .

The above-identified co-pending applications may include subject matter that is technically-related to subject matter of the present application and may contain claims that recite elements similar to those recited in claims of the present application. In handling prosecution of the above-identified applications, the Examiners for these other applications presumably will search for relevant prior art and, in some circumstances, may take positions about the prior art and/or the interpretation of the claims that may be material to the examination of the present application.

Accordingly, the Examiner in the present application is requested to review the file histories of the above-identified co-pending applications to see whether there is any information that the Examiner believes may be relevant to the prosecution of the present application. It is assumed that the Examiner has access to the file histories of the above-identified applications. However, if the Examiner would like copies of any or all of the information included in the file histories of the above-identified applications, the Examiner is asked to contact the undersigned representative.

The undersigned would like to bring to the Examiner's attention the enclosed search report or other communication from a corresponding or related International or Foreign National Application:

Serial No.	Date of Mailing	Type(s) of Communication	Docket No.
PCT/US2017/0478905	**12-04-2017**	**International Search Report and Written Opinion**	**A0863.70102WO00**

PART III: Remarks

Documents cited anywhere in the Information Disclosure Statement are enclosed unless otherwise indicated. It is respectfully requested that:

1. The Examiner consider completely the cited information, along with any other information, in reaching a determination concerning the patentability of the present claims;

2. The enclosed form PTO-1449 (modified PTO/SB/08) be signed by the Examiner to evidence that the cited information has been fully considered by the United States Patent and Trademark Office during the examination of this application;

3. The citations for the information be printed on any patent which issues from this application.

By submitting this Information Disclosure Statement, the undersigned makes no representation that a search has been performed, of the extent of any search performed, or that more relevant information does not exist.

By submitting this Information Disclosure Statement, the undersigned makes no representation that the information cited in the Statement is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b).

By submitting this Information Disclosure Statement, the undersigned makes no representation that the information cited in the Statement is, or is considered to be, in fact, prior art as defined by 35 U.S.C. § 102.

Notwithstanding any statements by the undersigned, the Examiner is urged to form his or her own conclusion regarding the relevance of the cited information.

An early and favorable action is hereby requested.

The Director is hereby authorized to charge any deficiency or credit any overpayment in the fees occasioned by the filing of this Information Disclosure Statement to our Deposit Account No. 23/2825 under Docket No. A0863.70051US04 from which the undersigned is authorized to draw.

Respectfully submitted,

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Compressive contact for high speed electrical connector

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Classification: - international: ***H01R12/58; H01R13/02; H01R13/646; H01R13/6461; H01R43/00***
- cooperative: **H01R12/58**; **H01R12/72**; **H01R13/28**; **H01R13/6471**; **H01R13/658**; **H01R13/6585**; **H01R23/688**; **H01R43/00**; Y10T29/49174; Y10T29/49208

Application number: CN2010849303 20100909 Global Dossier

Priority number (s): WO2010US02452 20100909 ; US20090240890P 20090909 ; US20090289785P 20091223

Also published as: CN102598430 (B) US2011067237 (A1) US2014065883 (A1) US2014329414 (A1) US8550861 (B2) more

Abstract of CN102598430 (A)

An electrical interconnection system with high speed, high density electrical connectors. One of the connectors includes a mating contact portion that generates contact force as it is compressed against a wall of the connector housing. The mating contact portion has multiple segments, each with a contact region extending from the wall, such that multiple points of contact to a complementary mating contact portion in a mating connector are provided for mechanical robustness. Additionally, each signal path through the mating interface portions of the connectors can be narrow and has a relatively uniform cross section to provide a uniform impedance. Additional size reduction may be achieved by mounting a ground contact on an exterior surface of a connector housing in alternating rows.

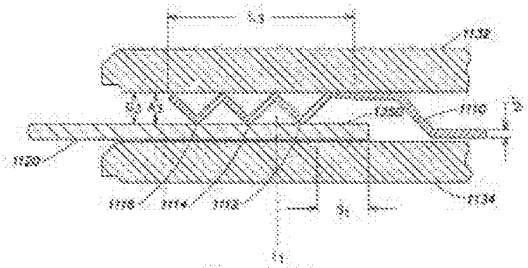

FIG. 12C

Additionally, embodiments in which a wavy contact is used in a cantilevered configuration are also described.

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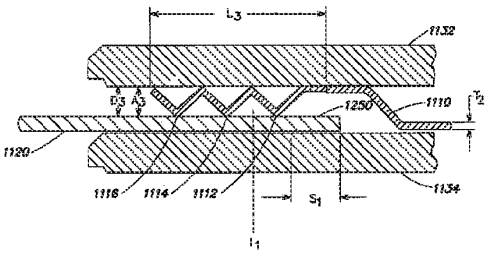
权利要求书 4 页 说明书 28 页 附图 24 页

(54)发明名称

用于高速电连接器的压缩触头

(57)摘要

一种具有高速、高密度电连接器的的电气互连系统。连接器之一包括匹配接触部，当靠着连接器外壳的壁压缩匹配接触部时，匹配接触部产生接触力。匹配接触部具有多个段，每个段均具有从壁延伸的接触区域，从而设置用于匹配连接器中的互补匹配接触部的多个接触点用于机械稳固性。此外，通过连接器的匹配接口部分的每个信号路径可以是窄的并且具有相对一致的截面以提供一致的阻抗。通过在连接器外壳的外表面上在交替的列中安装接地触头可以实现另外的尺寸减小。此外，也描述了在悬臂构型中使用波浪形触头的实施方式。



CN 102598430 A

1. 一种电连接器，所述电连接器包括：

多个列，每一个列均包括多个导电元件，

所述导电元件中的每一个导电元件均包括匹配接触部，

每一个匹配接触部均具有细长的尺寸和远端以及第一表面和相对的第二表面，所述第一表面和所述第二表面在所述细长的尺寸上延伸到所述远端，以及

每一个匹配接触部均包括在所述第二表面上的至少三个接触区域，所述接触区域中的每一个沿所述细长的尺寸设置在距所述远端不同的距离处。

2. 根据权利要求 1 所述的电连接器，其中，所述多个列中的每一个列中的所述多个导电元件包括设置成差分对的导电元件。

3. 根据权利要求 2 所述的电连接器，其中：

所述多个导电元件为信号接触元件；以及

所述多个列中的每一个列还包括多个接地元件，所述接地元件中的每一个均设置在相邻差分对的所述信号接触元件之间。

4. 根据权利要求 1 所述的电连接器，其中：

所述多个导电元件为信号接触元件；以及

所述多个列中的每一个列还包括多个接地元件。

5. 根据权利要求 1 所述的电连接器，其中：

所述连接器还包括外壳，所述外壳具有在其内的多个腔，并且所述多个腔设置用于限定所述多个列；

所述多个腔中的每一个腔均具有用于所述连接器的匹配面的开口；以及

所述多个列中的每一个列的所述多个导电元件中的每一个导电元件均设置在所述多个腔中的腔内。

6. 根据权利要求 5 所述的电连接器，其中：

所述多个腔中的每一个腔均具有从所述开口延伸的壁；以及

设置在腔中的所述多个导电元件中的每一个导电元件均以所述匹配接触部的所述第一表面邻近所述腔的壁的方式定位。

7. 根据权利要求 6 所述的电连接器，所述电连接器与第二连接器结合，其中：

所述多个导电元件包括第一类型导电元件；以及

通过弹力在设置在腔中的所述多个第一类型导电元件中的每一个与来自所述第二连接器的相应的第二类型导电元件之间形成电气连接，所述弹力通过靠着所述腔的壁压缩所述第一类型导电元件产生。

8. 根据权利要求 7 所述的电连接器，其中：

所述电连接器为子卡连接器且所述第二连接器为底板连接器；

所述第一类型导电元件中的每一个均由具有第一原料厚度的原料形成；以及

所述第二类型导电元件中的每一个均由具有第二原料厚度的原料形成，所述第二原料厚度大于所述第一原料厚度。

9. 根据权利要求 8 所述的电连接器，其中，所述第二原料厚度为 8 至 12 毫英寸之间。

10. 根据权利要求 7 所述的电连接器，其中，每个匹配接触部均包括金属条带，所述金属条带包括至少三个弯曲段，每个弯曲段均具有在垂直于所述壁的平面内的曲率半径，并

且每个接触区域均设置在弯曲段上。

11. 根据权利要求 8 所述的电连接器，其中：

对于设置在腔中的每个匹配接触部：

所述匹配接触部包括金属结构，所述金属结构具有平面部和从所述平面部延伸的至少三个段。

所述平面部邻近所述腔的壁设置；以及

所述接触区域中的每一个接触区域均设置在所述至少三个段中的段上。

12. 根据权利要求 11 所述的电连接器，其中，对于设置在腔中的每个匹配接触部，所述至少三个段中的每一个段均包括具有两个端部的细长部，所述细长部在所述两个端部中的每个端部处连接于所述平面。

13. 根据权利要求 1 所述的电连接器，其中：

对于每个导电元件：

所述二个接触区域中的每一个均形成在各自包括回折点的多个段中的段上，所述多个段具有波幅；以及

所述匹配接触部包括细长的段，所述细长的段具有大于所述波幅的长度。

14. 根据权利要求 1 所述的电连接器，所述电连接器与第二连接器结合，其中：

所述多个导电元件包括第一类型导电元件；以及

利用第二类型导电元件上所设计的 1.1mm 或更短的短尾部长度在设置于腔中的所述多个第一类型导电元件中的每一个与来自所述第二连接器的相应的第二类型导电元件之间形成电气连接。

15. 一种用于电连接器的导电元件，所述触头包括：

接触尾部；

匹配接触部；以及

连接所述接触尾部和所述匹配接触部的中间部，其中：

所述匹配接触部在第一方向上是细长的，并且具有在垂直于所述细长方向的第二方向上的厚度以及在垂直于所述第一方向和所述第二方向的第三方向上的宽度；

所述匹配接触部包括多个弯曲段，每个所述弯曲段：

延伸越过所述匹配接触部的宽度；以及

具有回折点。

16. 根据权利要求 15 所述的导电元件，其中：

所述多个弯曲段的所述回折点包括在所述表面上的多个接触点。

17. 根据权利要求 15 所述的导电元件，其中，所述多个接触点中的每一个均包括镀金。

18. 根据权利要求 15 所述的导电元件，其中，所述匹配接触部具有下述尺寸，所述尺寸包括：

大于 0.2mm 的宽度；

大于 3mm 的长度；以及

在 6 至 15 毫英寸之间的厚度。

19. 根据权利要求 17 所述的导电元件，其中，所述匹配接触部具有下述尺寸，所述尺寸包括：

在 0.2mm 至 0.4mm 之间的宽度；

在 3mm 至 10mm 之间的长度；以及

小于 10 毫英寸的厚度。

20. 根据权利要求 15 所述的导电元件，其中，所述触头由金属薄片冲压形成，所述金属薄片包括铜合金。

21. 根据权利要求 15 所述的导电元件，其中，所述匹配接触部在未匹配时具有弯曲包迹。

22. 根据权利要求 21 所述的导电元件，其中，对于每个匹配接触部，当未匹配时：

所述匹配接触部包括远端；

所述多个弯曲段沿所述匹配接触部的区域设置，所述匹配接触部具有在第一距离的区域范围内在所述第二方向上的最大波幅；以及

所述匹配接触部还包括将所述远端连接到所述区域的细长的段，所述细长的段具有大于所述第一距离的在第三方向上的长度的部件。

23. 一种电连接器，包括：

包括多个腔的外壳，每个腔均由第一壁和相对的第二壁界定；

设置在所述多个腔中的多个列的接触元件，每个接触元件均包括匹配接触部，所述匹配接触部包括：

邻近所述第一壁的部分；

至少三个弯曲段，每个弯曲段均包括：

第一构件，所述第一构件连接到所述部分，并且在远离所述第一壁的方向上延伸；

第二构件，所述第二构件在从所述第二壁朝向所述第一壁的方向上延伸；以及

匹配接触区域，所述匹配接触区域连接在所述第一构件与所述第二构件之间。

24. 根据权利要求 23 所述的电连接器，其中，邻近所述第一壁的所述部分嵌入在所述第一壁中。

25. 根据权利要求 23 所述的电连接器，其中，所述接触点中的每一个均包括凹痕。

26. 根据权利要求 23 所述的电连接器，其中，所述多个弯曲段包括波浪形触头。

27. 根据权利要求 23 所述的电连接器，其中，对于每个接触元件：

邻近所述壁的所述部分包括框架；以及

对于所述至少三个弯曲段中的每一个，所述第二构件具有连接到所述匹配接触区域的第一端部以及连接到所述框架的第二端部。

28. 根据权利要求 23 所述的电连接器，其中，所述匹配接触部以 1.3mm 的间距设置。

29. 一种操作电连接器的方法，所述电连接器具有带有多个腔的外壳，所述腔中的每一个均包含触头，每个第一类型触头包括邻近所述多个腔中的腔的壁的部分以及远离所述壁延伸的多个柔性段，所述多个柔性段具有在其上的接触区域，所述第一类型触头具有细长的尺寸，所述方法包括：

将多个平面触头插入到所述外壳中，每个平面触头均与所述多个腔中的腔内的相应的第一类型触头对准；以及

在所述细长的尺寸上相对于相应的第一类型触头滑动每个平面触头，以相继地与所述第一类型触头上的所述多个接触区域中的每一个形成接触，由此压缩所述平面触头与所述

腔的壁之间的所述相应的第一类型触头，以在所述平面触头与所述第一类型触头之间的多个接触区域中的每个处产生弹力。

30. 根据权利要求 29 所述的方法，其中，每个第一类型触头均包括波浪形触头，所述波浪形触头具有至少三个弯曲段，所述至少三个弯曲段中的每一个均提供接触区域。

31. 根据权利要求 29 所述的方法，其中，每个第一类型触头均包括框架以及至少三个构件，每个构件均具有连接到所述框架的第一端部和第二端部以及在所述第一端部和所述第二端部之间的匹配接触区域。

32. 根据权利要求 29 所述的方法，其中，每个第一类型触头和每个平面触头定尺寸成并且设置成提供小于 1.5mm 的滑接区。

33. 一种操作电连接器的方法，所述电连接器具有多个非平面触头，每个非平面触头均邻近外壳的壁并且具有远离所述壁延伸的多个部分，所述非平面触头包括细长的尺寸以及下表面和上表面，所述下表面具有在所述细长的尺寸上间隔开的多个回折点，所述上表面具有邻近所述壁的多个回折点，所述方法包括：

将多个平面触头插入到所述外壳中，每个平面触头均与非平面触头对齐；以及

在所述长形尺寸上相对于所述非平面触头滑动所述平面触头，以相继地与在所述下表面上的所述多个回折点中的每一个形成接触，由此在所述平面触头与所述外壳的壁之间压缩所述非平面触头，以在所述平面触头与所述非平面触头之间的多个接触区域中的每一个处产生弹力。

34. 根据权利要求 33 所述的方法，还包括通过所述电连接器耦合多个高频电气信号，每个高频电气信号均以超过 5Gbps 的速率携载数字数据，并在非平面触头与平面触头之间耦合。

35. 根据权利要求 33 所述的方法，其中，在所述下表面上的所述回折点包括局部最小值。

用于高速电连接器的压缩触头

[0001] 相关申请

[0002] 本申请依照 35U.S.C.§119(e)，要求 2009 年 9 月 9 日提交的发明名称为“COMPRESSIVE CONTACT FOR HIGH SPEEDELECTRICAL CONNECTOR(用于高速电连接器的压缩触头)”的美国临时申请序列号 61/240,890 的优先权，其全部内容结合在此，作为参考。本申请依照 35U.S.C.§119(e)，要求 2009 年 12 月 23 日提交的发明名称为“COMPRESSIVE CONTACT FOR HIGH SPEEDELECTRICAL CONNECTOR(用于高速电连接器的压缩触头)”的美国临时申请序列号 61/289,785 的优先权，其全部内容结合在此，作为参考。

技术领域

[0003] 本发明总体上涉及电气互连系统，更具体地，涉及高密度、高速电连接器。

背景技术

[0004] 电连接器用于许多电子系统中。将系统制造在通过电连接器彼此连接的若干印刷电路板(“PCBs”)上通常比将系统制造为单个组件更容易且更节省成本。用于使若干 PCBs 互连的传统的布置为使一个 PCB 用作底板。然后，称为子板或子卡的其它 PCBs 由电连接器通过底板连接。

[0005] 电子系统总体上已经变得较小、较快速且功能上更复杂。这些变化意味着，电子系统的给定区域中的电路的数量连同电路运行的频率在近些年中已经显著地增大。当前系统在印刷电路板之间传输更多的数据并且需要这样的电连接器，这些电连接器比甚至几年前的连接器能够以更高的速度电气化处理更多的数据。

[0006] 制造高密度、高速连接器的困难之一是连接器中的电导体可能非常靠近以致在相邻的信号导体之间存在电气干扰。为了减少干扰，或者说为了提供所需要的电气特性，通常在相邻的信号导体之间或围绕相邻的信号导体安置屏蔽构件。屏蔽件防止了一个导体上携载的信号在另一导体上产生“串扰”。屏蔽也影响每个导体的阻抗，其可以进一步有助于所需要的电气特性。屏蔽件可以为接地金属结构的形式或可以为电损耗材料的形式。

[0007] 其它技术也可以用来控制连接器的性能。差分地传输信号也可以减小串扰。差分信号携载在被称为“差分对”的一对导电路径上。导电路径之间的电压差产生信号。通常，差分对在所述对的导电路径之间设计有优先耦合。例如，差分对的两个导电路径可以设置成更靠近于彼此延伸而不是更靠近于连接器中的相邻信号路径。在所述对的导电路径之间不需要屏蔽，但屏蔽可以用于差分对之间。电连接器可以为差分信号以及单端信号而设计。

[0008] 保持信号完整性是在连接器的匹配接口方面的特殊挑战。在匹配接口处，必须产生力以将来自可分离的连接器的导电元件压到一起，从而在两个导电元件之间形成可靠的电气连接。通常，该力由连接器之一中的匹配接触部的弹性产生。例如，一个连接器的匹配接触部可以包括一个或更多个成形为梁的构件。连接器被压到一起时，这些梁通过另一连接器中的成形为柱或销的匹配接触部偏转。当梁偏转时由梁产生的弹力提供接触力。

[0009] 为了机械可靠性，许多触头具有多个梁。在一些情况下，梁是相对的，压在来自另

一连接器的导电元件的匹配接触部的相反侧上。可替代地，梁可以是平行的，压在匹配接触部的相同侧上。

[0010] 不管具体的接触结构如何，用于产生机械力的需要被强加到对匹配接触部的形状方面的要求。例如，匹配接触部必须足够大，以产生足够的力从而形成可靠的电气连接。

[0011] 这些机械性的要求会防碍屏蔽的使用或会规定在下述位置处使用导电材料，该位置改变导电元件在匹配接口附近的阻抗。由于在信号导体的阻抗方面的突然变化会改变该导体的信号完整性，因此匹配接触部通常被视作连接器的有嗓音部分。

附图说明

[0012] 附图不是意在按比例绘制。附图中，在各幅图中示出的每一相同或差不多相同的部件由相似的附图标记表示。为了清楚的目的，不是每个部件在每个附图中都被进行标记。在附图中：

[0013] 图 1 为示出本发明的实施方式可以应用的环境的电气互连系统的立体图；

[0014] 图 2A 和图 2B 为形成图 1 中的电连接器的一部分的晶片的第一侧视图和第二侧视图；

[0015] 图 2C 为图 2B 中示出的晶片沿线 2C-2C 截取的剖视图；

[0016] 图 3 为与图 1 中一样在连接器中堆叠到一起的多个晶片的剖视图；

[0017] 图 4A 为在图 1 中的连接器的制造中使用的引线框的平面图；

[0018] 图 4B 为由图 4A 中的箭头 4B-4B 环绕的区域的放大的详细视图；

[0019] 图 5A 为图 1 中的互连系统的底板连接器的剖视图；

[0020] 图 5B 为图 5A 中示出的底板连接器沿线 5B-5B 截取的剖视图；

[0021] 图 6A-6C 为在图 5A 中的底板连接器的制造中使用的导体的放大的详细视图；

[0022] 图 7A 为在两个匹配连接器中的引线框的匹配部的简图；

[0023] 图 7B 为连接器中的导电元件的匹配接触部的替代性构型的简图；

[0024] 图 7C 为连接器中的导电元件的匹配接触部的另一替代性构型的简图；

[0025] 图 8A 为在根据本发明的一些实施方式的连接器的制造中使用的引线框的平面图；

[0026] 图 8B 为在随后的制造步骤中的图 8A 中的引线框的一部分的简图；

[0027] 图 9A 为可以在根据本发明的一些实施方式的连接器的制造中使用的一对晶片的简图；

[0028] 图 9B 为安装在前外壳部中的图 9A 中的所述一对晶片的简图；

[0029] 图 10A 为适于与图 9B 中的连接器匹配的连接器的外壳的简图；

[0030] 图 10B 为在导电元件已经安装到外壳中的制造的后期阶段的图 10A 中的外壳的简图；

[0031] 图 10C 为可以插入到图 10A 中的外壳中的导电元件的简图；

[0032] 图 11 为根据本发明的一些实施方式的匹配连接器的导电元件的匹配接触部的简图；

[0033] 图 12A、图 12B 和图 12C 示出在匹配顺序的各个阶段图 11 中的匹配接触部；

[0034] 图 13 为从与图 12B 中的截面的方向垂直的方向剖切的电连接器的一部分的剖视

图；

[0035] 图 14 为波浪形匹配部元件的替代性实施方式的简图；

[0036] 图 15 为使用根据本发明的一些实施方式的波浪形匹配接触部的连接器的替代性实施方式的简图；

[0037] 图 16 为根据本发明的替代性实施方式的电连接器的一部分的剖视图；

[0038] 图 17A 为根据本发明的一些实施方式的导电元件的匹配接触部的平面图；

[0039] 图 17B 为图 17A 中的匹配接触部的立体图；

[0040] 图 17C 为包括具有如图 17A 和图 17B 中的匹配接触部的导电元件的电连接器的截面；

[0041] 图 18 为根据本发明的另一替代性实施方式的电连接器的一部分的剖视图；

[0042] 图 19A 为匹配接触部的替代性实施方式的简图；

[0043] 图 19B 为图 19A 中的匹配接触部的侧视图；

[0044] 图 20A 为匹配接触部的另一替代性实施方式的简图；以及

[0045] 图 20B 为图 20A 中的匹配接触部的俯视图。

具体实施方式

[0046] 参照图 1，图 1 示出了具有两个连接器的电气互连系统 100。电气互连系统 100 包括了卡连接器 120 和底板连接器 150。

[0047] 子卡连接器 120 被设计用于与底板连接器 150 相匹配，在底板 160 与子卡 140 之间建立导电路径。尽管没有特别地示出，但互连系统 100 可以互连多个子卡，它们具有类似的子卡连接器，类似的子卡连接器匹配到底板 160 上的类似的底板连接器。因此，通过互连系统连接的子组件的数量和类型不是对本发明的限定。

[0048] 图 1 示出本发明的实施方式可以应用的环境。虽然图 1 示出了通常在现有技术中已知的互连系统，但包括如下所述的匹配接触部的导电元件可以代替图 1 中示出的导电元件中的一些或全部。因此，根据一些实施方式的互连系统可以结合比常规设计的连接器密度更大的电连接器。

[0049] 在该示例中，连接器的密度是指沿子卡 140 的边缘的每单位长度上被设计用于携载信号的导电元件的数量。因此，密度可以通过为子卡 140 的边缘的单位长度增加信号导体的列的数量来增加。可替代地或另外地，密度可以通过增加每列中的导电元件的数量来增加。但是，由于互连系统通常仅为连接器提供有限的空间，因此每列的长度不能够任意地增加。例如，图 1 示出平行于底板 160 安装的子卡 140。尽管示出了单个子卡，但互连系统常规地包括以预定间距平行地布置的多个子卡。子卡之间的间距设定出了用于每个连接器沿列方向 C 的最大长度。不管用于增加连接器密度的方法如何，较高密度的连接器很可能具有更密集的接触元件，这些接触元件比在较低密度的连接器中的接触元件小，因此，在用于保持互连系统所需要的电气和机械特性的那些接触元件的设计方面产生挑战。用于增加连接器密度同时提供所需要的电气和机械特性的设计方法在下文中描述。

[0050] 图 1 示出使用直角、底板连接器的互连系统。应当理解，在其它实施方式中，电气互连系统 100 可以包括其它类型和组合的连接器，如本发明可以被广泛地应用于例如直角连接器、夹层连接器、卡缘连接器和芯片插座的多种类型的电连接器。

[0051] 底板连接器 150 和子卡连接器 120 中的每一个均包括导电元件。子卡连接器 120 的导电元件耦接到迹线，其中迹线 142 被标记，接地平面或子卡 140 中的其它导电元件。迹线携载电信号并且接地平面为子卡 140 上的部件提供基准电平。接地平面可以具有接地电压，或相对于接地电压为正或负的电压，如任何电压电平都可以用作基准电平。

[0052] 类似地，底板连接器 150 中的导电元件耦接到迹线，其中迹线 162 被标记，接地平面或底板 160 中的其它导电元件。当子卡连接器 120 和底板连接器 150 匹配时，两个连接器中的导电元件匹配，以在底板 160 和子卡 140 中的导电元件之间形成导电路径。

[0053] 底板连接器 150 包括底板罩 158 和多个导电元件（参见图 6A-6C）。底板连接器 150 的导电元件以部分在基底 514 上方和部分在基底 514 下方的方式延伸穿过底板罩 158 的基底 514。此处，导电元件延伸到基底 514 上方的部分形成匹配触头，它们被共同地示出为匹配接触部 154，匹配触头适于与子卡连接器 120 的相应导电元件匹配。在示出的实施方式中，匹配触头 154 为条片的形式，但也可以采用其它适合的接触构型，因为本发明在该方面不受限制。

[0054] 被共同地示出为接触尾部 156 的导电元件的尾部延伸在罩基底 514 下方并适于附连到底板 160。此处，尾部为压入配合的形式，配合到底板 160 上的、共同地示出为通路孔 164 的通路孔内的“针眼”柔性部分。但是，例如表面安装元件、弹性触头、可软焊的销等等的其它构型也是适合的，因为本发明在该方面不受限制。

[0055] 在示意出的实施方式中，底板罩 158 由例如塑料或尼龙的电介质材料模制。适合的材料的示例为液晶聚合物 (LCP)、聚苯硫醚 (PPS)、高温尼龙或聚丙烯 (PPO)。也可以采用其它适合的材料，因为本发明在该方面不受限制。所有这些材料都适合于在制造根据本发明的连接器时用作粘合材料。一种或更多种填料可以包括在用于形成底板罩 158 的粘合材料的一些或全部中，以控制底板罩 158 的电气或机械性能。例如，体积上填充有 30％的玻璃纤维的热塑性 PPS 可以用于形成罩 158。

[0056] 在示出的实施方式中，底板连接器 150 通过模制具有开口以容纳导电元件的底板罩 158 来制造。导电元件可成形有当插入到底板罩 158 的开口中时使导电元件保持就位的倒钩或其它保持结构。

[0057] 如在图 1 和图 5A 中所示，底板罩 158 还包括沿着底板罩 158 的相对边的长度延伸的侧壁 512。侧壁 512 包括凹槽 172，凹槽 172 沿着侧壁 512 的内表面竖直地延伸。凹槽 172 用于经由匹配突起 132 使子卡连接器 120 的前外壳 130 引导到罩 158 中的适当位置处。

[0058] 子卡连接器 120 包括多个联接到一起的晶片 $122_1 \ldots 122_6$，所述多个晶片 $122_1 \ldots 122_6$ 中的每个均具有外壳 260（参见图 2A-2C）和一列导电元件。在示出的实施方式中，每列具有多个信号导体 420（参见图 4A）和多个接地导体 430（参见图 4A）。接地导体可以在每个晶片 $122_1 \ldots 122_6$ 中被采用，以使信号导体之间的串扰最小化或者以其它方式控制连接器的电气特性。

[0059] 晶片 $122_1 \ldots 122_6$ 可以通过围绕形成信号导体和接地导体的导电元件模制外壳 260 来形成。如同底板连接器 150 的罩 158 一样，外壳 260 可以由任何适合的材料形成，并且可以包括具有导电填料的部分或者是以其它方式产生损耗的部分。

[0060] 在示出的实施方式中，子卡连接器 120 为直角连接器并且具有穿过直角的导电元件。因此，导电元件的相反两端从晶片 $122_1 \ldots 122_6$ 的垂直边缘延伸。

[0061] 晶片 $122_1 \ldots 122_6$ 中的每个导电元件均具有至少一个接触尾部，它们被共同地示出为接触尾部 126，它们可以连接到子卡 140。子卡连接器 120 中的每个导电元件还具有匹配接触部，它们被共同地示出为匹配触头 124，它们可以连接到底板连接器 150 中的相应导电元件。每个导电元件还具有在匹配接触部与接触尾部之间的中间部，中间部可以由晶片外壳 260（参见图 2）包围或者嵌入在晶片外壳 260 内。

[0062] 接触尾部 126 将子卡 140 和连接器 120 内的导电元件电气地连接到例如子卡 140 中的迹线 142 的导电元件。在示出的实施方式中，接触尾部 126 为压入配合的“针眼”触头，该“针眼”触头通过子卡 140 中的通路孔进行电气连接。但是，可以使用任何适合的附连机构来代替或添加到通路孔以及压入配合的接触尾部。

[0063] 在示出的实施方式中，匹配触头 124 中的每个均具有构造用于与底板连接器 150 的相应匹配触头 154 匹配的双梁结构。但是，如下文所述，具有波浪形匹配接触部的导电元件可以代替图 1 中示出的、具有双梁匹配接触部的导电元件中的一些或全部，作为减小匹配接触部之间的间距的方法。通过减小该间距，可以增加沿方向 C 延伸的每列中的每单位长度的导电元件的数量，从而导致连接器密度的增加。

[0064] 用作信号导体的导电元件可以组合成对，并且在适合于用作差分电连接器的构型中通过接地导体分开。但是，实施方式也可用于单端的情况，其中，导电元件在不具有指定的分开信号导体的接地导体的情况下、或者在每个信号导体之间具有接地导体的情况下被均匀地隔开。

[0065] 在示出的实施方式中，一些导电元件被指定为形成导体的差分对而一些导电元件被指定为接地导体。这些指定是指如本领域技术人员将能理解的、导电元件在互连系统中的有目的的使用。例如，尽管导电元件可以有其它用途，但可以根据构成为对的导电元件之间的优先耦接来识别差分对。使所述对适于携载差分信号的、例如所述对的阻抗的所述对的电气特性，可以提供可替代的或另外的识别差分对的方法。如另一示例，在具有差分对的连接器中，接地导体可以通过它们相对于差分对的位置被识别。在其它情况下，接地导体可以通过它们的形状或电气特性被识别。例如，接地导体可以相对较宽以提供低电感，其对于提供稳定的基准电位来说是需要的，但提供了对于携载高速信号来说不需要的阻抗。

[0066] 仅为了示例性目的，子卡连接器 120 示出为具有六个晶片 $122_1 \ldots 122_6$，每个晶片均具有多个成对的信号导体和相邻的接地导体。如图示的，晶片 $122_1 \ldots 122_6$ 中的每个均包括一列导电元件。但是，本发明在该方面不受限制，如晶片的数量以及每个晶片中的信号导体和接地导体的数量可以根据需要而改变。

[0067] 如所示的，每个晶片 $122_1 \ldots 122_6$ 均插入到前外壳 130 内，使得匹配触头 124 插入并保持在前外壳 130 中的开口内。前外壳 130 中的开口定位成当子卡连接器 120 匹配到底板连接器 150 时允许底板连接器 150 的匹配触头 154 进入前外壳 130 中的开口，并允许与匹配触头 124 电气连接。

[0068] 子卡连接器 120 可以包括代替或添加到前外壳 130 以保持晶片 $122_1 \ldots 122_6$ 的支承构件。在图示的实施方式中，加固件 128 支承多个晶片 $122_1 \ldots 122_6$。在示出的实施方式中，加固件 128 为冲压金属构件。但是，加固件 128 可以由任何适合的材料形成。加固件 128 可以冲压有可以接合多个晶片的狭槽、孔、凹槽或其它结构，以支承晶片处于所需要的定位。

[0069] 每个晶片 $122_1 \ldots 122_6$ 均可以包括接合加固件 128 的附连结构 242、244（参见图 2A-2B），以相对于另外的部分定位每个晶片 122 并进一步防止晶片 122 的转动。当然，本发明在该方面不受到限制，并且不需要使用加固件。此外，尽管加固件示出为附连到多个晶片的上部和侧部，但本发明在该方面不受限制，如也可以采用其它适合的位置。

[0070] 图 2A-2B 示出示例性晶片 220A 的相反的侧视图。晶片 220A 可以通过材料的注入模制以形成围绕例如 410A 或 410B（图 4）的晶片条带组件的外壳 260 来整体地或局部地形成。在图示的实施方式中，晶片 220A 通过二次注入模制操作形成，允许外壳 260 由具有不同材料特性的两种类型的材料形成。绝缘部 240 在第一注入时形成而损耗部 250 在第二注入时形成。但是，任何适合数量和类型的材料都可以用于外壳 260。在一个实施方式中，外壳 260 通过注入模制塑料而围绕导电元件的列形成。

[0071] 在一些实施方式中，外壳 260 可以设置有开口，例如邻近信号导体 420 的窗口或狭槽 $264_1 \ldots 264_6$、以及孔，其中孔 262 被标记。这些开口可以用于多个目的，包括：(i) 在注入模制过程期间保证导电元件适当地定位；以及 (ii) 方便具有不同电气特性的材料的插入，如果有这种不同电气特性的需要。

[0072] 为获得所需要的性能特征，本发明的一个实施方式可以采用选择性地靠近晶片的信号导体 310_1B、$310_2B \ldots 310_4B$ 定位的不同介电常数的区域。例如，在图 2A-2C 示出的实施方式中，外壳 260 包括外壳 260 中的狭槽 $264_1 \ldots 264_6$，狭槽 $264_1 \ldots 264_6$ 使空气处于邻近信号导体 310_1B、$310_2B \ldots 310_4B$ 的位置。

[0073] 使空气处于一定位置的能力、或者在非常靠近差分对的一个半体处的具有比用于形成外壳 260 的其它部分的材料的介电常数低的介电常数的其它材料，提供了纠偏差分对的信号导体的机构。电气信号从信号导体的一端传播到另一端所需要的时间已知为传播延迟。在一些实施方式中，需要一对中的两个信号导体具有相同的传播延迟，其通常被称为在所述对中具有零偏差。导体中的传播延迟受到靠近导体的材料的介电常数影响，其中，较低介电常数意味着较小的传播延迟。有时候介电常数也称作相对介电常数。真空具有最低可能性的值为 1 的介电常数。空气具有类似的低的介电常数，但是例如 LCP 的电介质材料具有较高的介电常数。例如，LCP 具有约 2.5 至约 4.5 之间的介电常数。

[0074] 所述信号对的每个信号导体可具有不同的物理长度，特别是在直角连接器中。根据本发明的一个方面，为使差分对的信号导体中的传播延迟均等，既使它们具有不同的物理长度，可以调节导体周围的不同介电常数的材料的相对比例。在一些实施方式中，与所述对的较短的信号导体相比，更多的空气靠近所述对的物理方面较长的信号导体处，由此降低信号导体周围的有效介电常数，并且减少其传播延迟。

[0075] 但是，随着介电常数降低，信号导体的阻抗升高。为保持所述对内的平衡的阻抗，靠近空气的信号导体的尺寸可以在厚度或宽度上增加。其导致沿着所述对的两个信号导体，它们具有不同的物理几何特性、但具有较均等的传播延迟和较统一的阻抗特性。

[0076] 图 2C 示出沿图 2B 中的线 2C-2C 截取的晶片 220 的截面。如所示的，多个差分对 $340_1 \ldots 340_4$ 成阵列保持在外壳 260 的绝缘部 240 内。在示意出的实施方式中，阵列在截面中为线性阵列，从而形成一列导电元件。

[0077] 槽 $264_1 \ldots 264_4$ 被截面穿过并因此在图 2C 中可见。如可以看到的，槽 $264_1 \ldots 264_4$ 产生邻近每个差分对 340_1、$340_2 \ldots 340_4$ 中的较长导体的空气区域。但是，空气仅是可用于

纠偏连接器的具有低介电常数的材料的一个示例。与图 2C 中示出的槽 $264_1 \ldots 264_4$ 占据的区域相当的区域，可以由比用于形成外壳 260 的其它部分的塑料具有更低的介电常数的塑料形成。作为另一示例，较低介电常数的区域可以使用不同类型或数量的填料形成。例如，较低介电常数的区域可以由比其它区域具有更少的玻璃纤维强化材料的塑料模制。

[0078] 图 2C 还示出可以在一些实施方式中使用的信号导体和接地导体的定位和相对尺寸。如图 2C 所示，信号导体 $310_1A \ldots 310_4A$ 以及 $310_1B \ldots 310_4B$ 的中间部嵌入到外壳 260 内以形成列。接地导体 $330_1 \ldots 330_4$ 的中间部也可以在相同的列中保持在外壳 260 内。

[0079] 接地导体 330_1、330_2 和 330_3 定位在列中的两个相邻的差分对 340_1、$340_2 \ldots 340_4$ 之间。另外的接地导体可以包括在列的端部中的任一或两者处。如图 2C 中所示的，在晶片 220A 中，接地导体 330_2 定位在列的一端处。如图 2C 所示，在一些实施方式中，每个接地导体 $330_1 \ldots 330_4$ 均优选地宽于差分对 $340_1 \ldots 340_4$ 的信号导体。在示出的截面中，每个接地导体的中间部具有等于或大于信号导体的中间部的宽度三倍的宽度。在图示的实施方式中，每个接地导体的宽度足以沿着列穿过至少与差分对相同的距离。

[0080] 在图示的实施方式中，每个接地导体均具有大约信号导体的宽度五倍的宽度，使得由导电元件占据的列宽度超过 50％被接地导体占据。在示出的实施方式中，被导电元件占据的列宽度的大约 70％被接地导体 $330_1 \ldots 330_4$ 占据。增加每列中被接地导体占据的百分比可以减少导体中的串扰。但是，用于增加在列方向上的每单位长度（在图 1 中以尺寸 C 示出）的信号导体的数量的一个方法是，减小每个接地导体的宽度。因此，尽管图 2C 示出接地导体与信号导体之间的宽度比为大约 3 ： 1，但更低比率可用于改进密度。在一些实施方式中，比率可以为 2 ： 1 或更小。

[0081] 其它技术也可用于制造晶片 220A 以减小串扰，或者以其它方式具备所需要的电气特性。在一些实施方式中，外壳 260 的一个或更多个部分由选择性地改变外壳的那部分的电气和 / 或电磁特性的材料形成，由此抑制噪音和 / 或串扰、改变信号导体的阻抗、或者以其它方式为晶片的信号导体赋予所需要的电气特性。

[0082] 在图 2A-2C 中示出的实施方式中，外壳 260 包括绝缘部分 240 和损耗部分 250。在一个实施方式中，损耗部分 250 可以包括填充有导电粒子的热塑性材料。填料使该部分产生“电损耗”。在一个实施方式中，外壳的损耗区域构造用于减小在至少两个相邻的差分对 $340_1 \ldots 340_4$ 之间的串扰。外壳的绝缘区域可构造成使得损耗区域不会削弱由差分对 $340_1 \ldots 340_4$ 携载的信号的不必要的量。

[0083] 在有效频率范围内带有一些损耗的传导材料在此处总体上被称为“损耗”材料。电损耗材料可以由有损电介质和 / 或有损导电材料形成。有效频率范围取决于其中使用这种连接器的系统的工作参数，但将总体上处于约 1GHz 至 25GHz 之间，尽管在一些应用中更高频率或更低频率会更有益。一些连接器设计可以具有仅跨过该范围的一部分的有效频率范围，例如 1GHz 至 10GHz 或 3GHz 至 15GHz 或 3GHz 至 6GHz。

[0084] 电损耗材料可以由传统地被认为是电介质材料的材料形成，例如在有效频率范围内具有大于大约 0.003 的电损耗因子的电介质材料。“电损耗因子”为材料的复介电常数的虚部与实部之比。

[0085] 电损耗材料也可以由这样的材料形成：所述材料尽管大体上为导体，但是，它们或是在有效频率范围内的相对不良导体且包括不提供高导电率的充分分散的粒子或区域，或

是具备在有效频率范围内产生相对较弱的体积导电率的特性。电损耗材料通常具有的导电率为约 1 西门子 / 米至约 6.1×10^7 西门子 / 米，优选地为约 1 西门子 / 米至约 1×10^7 西门子 / 米，且最优选地为约 1 西门子 / 米至约 30,000 西门子 / 米。

[0086] 电损耗材料可以是局部导电材料，例如具有 1Ω / 平方米至 10^6Ω / 平方米之间的表面电阻率的那些导电材料。在一些实施方式中，电损耗材料具有 1Ω / 平方米至 10^3Ω / 平方米之间的表面电阻率。在一些实施方式中，电损耗材料具有 10Ω / 平方米至 100Ω / 平方米之间的表面电阻率。作为特定的示例，材料可以具有约 20Ω / 平方米至 40Ω / 平方米之间的表面电阻率。

[0087] 在一些实施方式中，电损耗材料通过在粘合剂中添加包括导电粒子的填料来形成。可以用作填料以形成电损耗材料的导电粒子的示例包括形成为纤维、薄板的碳或石墨或其它粒子。粉末、薄板、纤维形式的金属或其它粒子也可用于提供适合的电损耗特性。可替代地，可以使用填料的组合。例如，可以使用镀有金属的碳粒子。银和镍是适合于纤维的金属镀层。涂覆粒子可以单独地或与例如碳薄板的其它填料组合地使用。在一些实施方式中，设置在外壳的损耗部 250 中的导电粒子可以大致均匀遍布地设置，从而呈现损耗部基本恒定的导电率。在其它实施方式中，损耗部 250 的第一区域可以比损耗部 250 的第二区域更具导电性，使得损耗部 250 中的导电率和因此的损耗量可以变化。

[0088] 粘合剂或基质可以是将凝结、固化或可以其它方式被用于定位填料材料的任何材料。在一些实施方式中，粘合剂可以是，例如传统地在电连接器的生产中使用，以方便作为制造电连接器的一部分的将电损耗材料模制成所需要的形状和位置的热塑性材料。但是，可以使用许多替代形式的粘合剂材料。例如环氧树脂的可固化材料可以用作粘合剂。可替代地，可以使用例如热固性树脂或胶粘剂的材料。而且，尽管上述粘合剂材料通过围绕导电粒子填料形成粘合剂而可以用于产生电损耗材料，但本发明不限于此。例如，导电粒子可以例如通过将导电涂层涂覆到塑性外壳而浸透到已形成的基质材料内或可以涂覆到已形成的基质材料上。如此处所使用的，术语“粘合剂”包括封装填料、浸透有填料或以其它方式用作保持填料的基体的材料。

[0089] 优选地，填料将以足够的体积百分比出现以允许从粒子到粒子地形成导电路径。例如，当使用金属纤维时，纤维以约 3％至 40％的体积百分比出现。填料的量可以影响材料的导电特性。

[0090] 带填料的材料在商业上可以购买，例如由 Ticona 以商标名称**Celestran®**出售的材料。也可以使用例如填充有损耗性导电碳的胶粘剂预成品、例如由美国马萨诸塞州 Billerica 的 Techfilm 出售的那些损耗材料。该预成品可以包括填允有碳粒子的环氧粘合剂。粘合剂包围碳粒子，其充当对于预成品的加强材料。这样的预成品可以插入到晶片 220A 中以形成外壳的全部或一部分，并可以定位成粘附到晶片中的接地导体。在一些实施方式中，预成品可以通过预成品中的胶粘剂粘附，胶粘剂在热处理过程中固化。可以使用编织的或非编织形式的、有涂层的或没有涂层的各种形式的加强纤维。非编织碳纤维是一种适合的材料。可以采用其它适合的材料，例如由 RTP 公司出售的定制的混合物，本发明在该方面不受限制。

[0091] 在图 2C 示出的实施方式中，晶片外壳 260 由两种类型的材料模制。在图示的实施方式中，损耗部 250 由具有导电填料的材料形成，而绝缘部 240 由具有少量导电填料或不具

有导电填料的绝缘材料形成，但是绝缘部可以具有例如玻璃纤维的填料，玻璃纤维改变粘合剂材料的机械特性或影响粘合剂的例如介电常数的其它电气特性。在一个实施方式中，绝缘部 240 由模制的塑料形成而损耗部由具有导电填料的模制的塑料形成。在一些实施方式中，损耗部 250 是充分有损耗的，其将差分对之间的辐射削弱到足够量，使得串扰减小到不需要单独的金属板的水平。

[0092] 为防止信号导体 310_1A、310_1B...310_4A 和 310_4B 一起短路和 / 或通过损耗部 250 到地面短路，由适合的电介质材料形成的绝缘部 240 可以用于绝缘信号导体。绝缘材料可以是例如热塑性粘合剂，不导电纤维引入到粘合剂中用于增加强度、尺寸稳定性并减少高价的粘合剂的使用量。如在常规电连接器中，玻璃纤维可以具有约 30％的体积的装填量。应当理解，在其它实施方式中，可以使用其它材料，本发明并不进行这样的限定。

[0093] 在图 2C 的实施方式中，损耗部 250 包括平行区域 336 和垂直区域 334_1...334_4。在一个实施方式中，垂直区域 334_1...334_4 设置在形成单独的差分对 340_1...340_2 的相邻导电元件之间。

[0094] 在一些实施方式中，外壳 260 的损耗区域 336 和 334_1...334_4 与接地导体 330_1...330_4 配合来屏蔽差分对 340_1...340_4 以减小串扰。损耗区域 336 和 334_1...334_4 可以通过电气地耦接到一个或更多个接地导体接地。这样的耦接可以是电损耗材料与接地导体之间直接接触的结果，或者可以是例如通过电容耦合的间接接触的结果。这种损耗材料结合接地导体 330_1...330_4 的构型减少了列中的差分对之间的串扰。

[0095] 如图 2C 所示，接地导体 330_1...330_4 的部分可以通过围绕接地导体 340_1...340_4 的模制部 250 电气地连接到区域 336 和 334_1...334_4。在一些实施方式中，接地导体可以包括开口，在模制期间形成外壳的材料可以通过该开口流动。例如，图 2C 中示出的截面沿接地导体 330_1 中的开口 332 截取。尽管在图 2C 的截面中不可见，但也可以包括例如 330_2...330_4 的其它接地导体中的其它开口。

[0096] 流动通过接地导体中的开口的材料允许垂直部 334_1...334_4 延伸通过接地导体，甚至通过模腔，模腔用于形成晶片 220A 并仅在接地导体的一侧具有入口。此外，作为模制操作的一部分的，材料通过接地导体中的开口的流动，可以有助于将接地导体固定在外壳 260 中，并可以增强损耗部分 250 与接地导体之间的电气连接。但是，也可以使用形成垂直部 334_1...334_4 的其它适合方法，包括在在接地导体 330_1...330_2 的两侧具有入口的腔中模制晶片 320A。同样，也可以采用用于固定接地触头 330 的其它适合方法，本发明在该方面不受限制。

[0097] 由可模制材料形成外壳的损耗部 250 可提供另加的益处。例如，处于一个或更多个位置处的损耗材料可以构造用于设定连接器在该位置处的性能。例如，改变损耗部的厚度以将信号导体定位成更靠近于或更远离损耗部 250 能够改变连接器的性能。同样，可以改变一个差分对与地面之间以及另一差分对与地面之间的电磁耦合，由此配置相邻的差分对之间的辐射的损耗量以及由那些差分对携载的信号的损耗量。因此，根据本发明的实施方式的连接器与常规连接器相比能够在更高的频率下使用，例如，举例来说 10-15GHz 之间的频率。

[0098] 如图 2C 的实施方式所示，晶片 220A 被设计用于携载差分信号。因此，每个信号由一对信号导体 310_1A 和 310_1B，...310_4A 和 310_4B 来携载。优选地，每个信号导体更靠近于

所述信号导体的对中的其它导体而不是更靠近相邻对中的导体。例如，对 340_1 携载一个差分信号，而对 340_2 携载另一差分信号。如在图 2C 的截面中可以看到的，信号导体 310_1B 更靠近于信号导体 310_1A 而不是信号导体 310_2A。垂直损耗区域 $334_1 \ldots 334_4$ 可以定位在对之间，以在相同列中的相邻差分对之间提供屏蔽。

[0099] 损耗材料也可以定位用于减少不同列中的相邻对之间的串扰。图 3 示出类似于图 2C 的但具有并排地排列以形成多个平行列的多个子组件或晶片 320A、320B 的截面图。

[0100] 如图 3 所示，多个信号导体 340 可以设置在通过并列定位晶片形成的多个列中的差分对中。每个晶片不是必须相同而可以使用不同类型的晶片。

[0101] 理想的是，用于构造子卡连接器的所有类型的晶片具有大约相同尺寸的外部包迹 (envelope)，使得所有晶片安装在相同的外套中或可以附连到例如加固件 128（图 1）的相同的支承构件。但是，通过提供信号导体的不同位置、接地导体以及不同晶片中的损耗部，可以更容易地配置与损耗材料削弱信号的量有关的损耗材料减少串扰的量。在一个实施方式中，使用了两种类型的晶片，它们在图 3 中作为子组件或晶片 320A 和 320B 示出。

[0102] 晶片 320B 中的每个均可以包括与在图 2A、2B 和 2C 中示出的晶片 320A 的结构类似的结构。如图 3 所示，晶片 320B 包括多个差分对，例如对 340_5、340_6、340_7 和 340_8。信号对可以保持在例如外壳的 240B 的绝缘部中。狭槽或其它结构（未标记）可以以与在晶片 220A 中形成的狭槽 $264_1 \ldots 264_6$ 相同的方式形成在外壳中，以使偏差均等化。

[0103] 用于晶片 320B 的外壳也可以包括损耗部，例如损耗部 250B。如同在图 2C 中结合晶片 320A 所描述的损耗部 250 一样，损耗部 250B 可以定位用于减少相邻差分对之间的串扰。损耗部 250B 可以形成在不造成不希望的信号衰减量的情况下，提供所需要程度的串扰抑制。

[0104] 在示出的实施方式中，损耗部 250B 可以具有平行于差分对 $340_5 \ldots 340_8$ 的列的基本平行的区域 336B。每个损耗部 250B 还可以包括从平行区域 336B 延伸的多个垂直区域 $334_1B \ldots 334_5B$。垂直区域 $334_1B \ldots 334_5B$ 可以间隔开并且设置在列中的相邻差分对之间。

[0105] 晶片 320B 还包括接地导体，例如接地导体 $330_5 \ldots 330_9$。如同晶片 320A 一样，接地导体邻近差分对 $340_5 \ldots 340_8$ 定位。同样，如在晶片 320A 中一样，接地导体通常具有比信号导体的宽度大的宽度。在图 3 示出的实施方式中，接地导体 $330_5 \ldots 330_8$ 具有与晶片 320A 中的接地导体 $330_1 \ldots 330_4$ 大致相同的形状。但是，在示出的实施方式中，接地导体 330_9 具有比晶片 320B 中的接地导体 $330_5 \ldots 330_8$ 小的宽度。

[0106] 接地导体 330_9 较窄，以提供所需要的电气特性，而不要求晶片 320B 具有不必要的宽度。接地导体 330_9 具有面对差分对 340_8 的边缘。因此，差分对 340_8 类似于相邻差分对地相对于接地导体定位，例如晶片 320B 中的差分对 330_8 或晶片 320A 中的对 340_4。因此，差分对 340_8 的电气特性类似于其它差分对的电气特性。通过使接地导体 330_9 比接地导体 330_8 或 330_4 更窄，晶片 320B 可以制成为具有较小的尺寸。

[0107] 类似小的接地导体可以邻近对 340_1 包括在晶片 320A 中。但是，在示出的实施方式中，对 340_1 在子卡连接器 120 的所有差分对中是最短的。尽管在晶片 320A 中包括窄的接地导体可以使差分对 340_1 的接地构型更类似于晶片 320A 和 320B 中的相邻差分对的构型，但是接地构型中的差分的净效应与导体的长度成比例，差分存在于导体的长度上。在图 3 的实施方式中，由于差分对 340_1 相对较短，邻近差分对 340_1 的第二接地导体可以具有相对

小的净效应，尽管第二接地导体会改变差分对 340_1 的电气特性。但是，在其它实施方式中，另一接地导体可以包括在晶片 320A 中。图 3 以窄接地导体 330_9 示出用于提供相邻对 350B 的接地结构的可行方法。以下结合图 8A、图 8B、图 9A、图 9B、图 10A、图 10B 和图 10C 描述可以在连接器中提供相同数量但沿列方向占据较少空间的信号导体的替代性方法。如在图 3 的实施方式中，邻近作为连接器中的最长对的对 330_9 提供接地，但是在列的端部处没有为晶片 320A 中的对 340_1 提供类似接地。然而，如同窄接地触头 330_9 一样，可以替代性地或附加地邻近对 340_1 应用图 8A、图 8B、图 9A、图 9B、图 10A、图 10B 和图 10C 中的替代性接地结构。

[0108] 图 3 示出当使用多种类型的晶片以形成了卡连接器时的另一可行结构。由于晶片 320A 和 320B 中的触头的列具有不同的构型，因此当晶片 320A 与晶片 320B 并排定位时，晶片 320A 中的差分对更靠近于晶片 320B 中的接地导体排列而不是更靠近于晶片 320B 中的相邻对的信号导体排列。相反地，晶片 320B 的差分对更靠近于晶片 320A 中接地导体排列而不是更靠近于相邻差分对排列。

[0109] 例如，差分对 340_6 最接近于晶片 320A 中的接地导体 330_2。类似地，晶片 320A 中的差分对 340_3 最接近于晶片 320B 中的接地导体 330_7。以此方式，来自一个列中的差分对的辐射更强地耦合到相邻列中的接地导体而不是耦合到该列中的信号导体。这种构型减少了在相邻列中的差分对之间的串扰。

[0110] 具有不同构型的晶片可以以任何适当的方式形成。图 4A 示出制造根据一个实施方式的晶片 320A 和 320B 的步骤。在示出的实施方式中，形成了晶片条带组件，晶片条带组件中的每个均包括处于子卡连接器的一个列所需要的构型的导电元件。然后，在夹物模制操作中围绕每个晶片条带组件中的导电元件模制外壳，以形成晶片。

[0111] 为便于制造晶片，信号导体，其中信号导体 420 被标记，和接地导体，其中接地导体 430 被标记，可以一起保持在引线框 400 上，如图 4A 中所示。如所示的，信号导体 420 和接地导体 430 附连到一个或更多个载体带 402。在一些实施方式中，用于许多晶片的信号导体和接地导体冲压到单个薄板上。薄板可以是金属的或可以是导电的并提供在电连接器中形成导电元件的适合的机械特性的任何其它材料。磷青铜、铍铜和其它铜合金是可以使用的材料的示例。

[0112] 以下描述导电元件具有不同于图 4A 中示出的构型的实施方式。但是，可以使用类似材料和制造技术以形成这些导电元件。

[0113] 图 4A 示出金属薄板的一部分，其中，晶片条带组件 410A、410B 已经在金属薄板中冲压出。晶片条带组件 410A、410B 可以分别用于形成晶片 320A 和 320B。导电元件可以在需要的位置保持在载体带 402 上。于是，导电元件在制造晶体期间可以更容易地处理。一旦将材料围绕导电元件模制，载体带即可以用来分隔导电元件。然后，可以将晶片组装到任何适当尺寸的子卡连接器中。

[0114] 图 4A 还提供子卡晶片的导电元件的结构的更详细视图。诸如接地导体 430 之类的接地导体相对于诸如信号导体 420 之类的信号导体的宽度是显而易见的。同样，诸如开口 332 的接地导体中的开口是可见的。

[0115] 图 4A 中示出的晶片条带组件只提供可在晶片的制造中使用的部件的一个示例。例如，在图 4A 中示出的实施方式中，引线框 400 包括将信号导体 420 和 / 或接地条带 430

的各个部分连接到引线框 400 的连接条 452、454 和 456。这些连接条可以在随后的生产过程期间用来提供电气分隔的导电元件。金属薄板可以冲压成使得一个或更多个另外的载体带形成在其它位置处和 / 或导电元件之间的桥接构件可以在制造期间用于导电元件的定位和支承。因此，图 4A 中示出的细节是说明性的而不是对本发明的限定。

[0116] 尽管引线框 400 示出为包括接地导体 430 和信号导体 420 两者，但本发明在该方面不受限制。例如，相应导体可以形成在两个独立的引线框中。实际上，不需要使用引线框并且在制造期间可以使用单独的导电元件。应当理解，根本没有必要执行引线框之一或两者、或单独的导电元件上的模制，因为晶片可以通过将接地导体和信号导体插入到已预制的外壳部中来组装，其随后可以通过包括卡扣配合结构的各种结构固定到一起。

[0117] 图 4B 示出定位在两个接地匹配触头 434_1 与 434_2 之间的差分对 424_1 的匹配接触端部的详细视图。如所示的，接地导体可以包括不同尺寸的匹配触头。图示的实施方式具有大匹配触头 434_2 和小匹配触头 434_1。为减小每个晶片的尺寸，小匹配触头 434_1 可以定位在晶片的端部之一或两者处。但是，在希望增加连接器的整体密度的实施方式中，所有的接地导体都可以具有与小匹配触头 434_1 相当的尺寸，接地导体稍微宽于差分对 424_1 的信号导体。在又一实施方式中，信号导体和接地导体两者的匹配接触部可以具有近似相同的宽度。

[0118] 图 4B 示出形成子卡连接器 120 的晶片中的导电元件的匹配接触部的结构。图 4B 示出构造成晶片 320B 的晶片的匹配触头的一部分。所示部分示出例如可以在接地导体 330_9（图 3）的端部使用的匹配触头 434_1。匹配触头 424_1 可以形成例如差分对 340_8（图 3）中的信号导体的匹配接触部。同样，匹配触头 434_2 可以形成例如接地导体 330_8（图 3）的接地导体的匹配接触部。

[0119] 在图 4B 中示出的实施方式中，子卡晶片中的导电元件上的匹配触头中的每个均为双梁触头。匹配触头 434_1 包括梁 460_1 和 460_2。匹配触头 424_1 包括四个梁，两个梁用于终止于匹配触头 424_1 的差分对的信号导体中的每个。在图 4B 的示例中，梁 460_3 和 460_4 为用于所述对的一个信号导体的触头提供两个梁，并且梁 460_5 和 460_6 为用于所述对的第二信号导体的触头提供两个梁。同样，匹配触头 434_2 包括两个梁 460_7 和 460_8。

[0120] 梁中的每个均包括匹配表面，其中梁 460_1 上的匹配表面 462 被标记。为在子卡连接器 120 中的导电元件与底板连接器 150 中的相应导电元件之间形成可靠的电气连接，梁 $460_1 \ldots 460_8$ 中的每个均可以定形成以足够的机械力压靠底板连接器 150 中的相应匹配触头，以建立可靠的电气连接。即使在一个梁被损坏、污染或以其它方式被阻碍形成有效连接的情况下，每个触头具有两个梁也能够增加将形成的电气连接的可能性。

[0121] 梁 $460_1 \ldots 460_8$ 中的每个均具有产生用于对相应的触头进行电气连接的机械力的形状。在图 4B 的实施方式中，终止于匹配触头 424_1 的信号导体可以具有晶片 320D 的外壳中的相对窄的中间部 484_1 和 484_2。但是，为形成有效电气连接，用于信号导体的匹配接触部 424_1 可以宽于中间部 484_1 和 484_2。因此，图 4B 示出与信号导体中的每个相关联的加宽部 480_1 和 480_2。

[0122] 在示出的实施方式中，邻近加宽部 480_1 和 480_2 的接地导体成形成与信号导体的相邻边缘相符。因此，用于接地导体的匹配触头 434_1 具有互补部 482_1，互补部 482_1 具有与加宽部 480_1 相符的形状。同样，匹配触头 434_2 具有互补部 484_2，互补部 484_2 具有与加宽部 480_2 相符的形状。通过结合接地导体中的互补部，即使信号导体的宽度在匹配接触区域改

变以为梁提供所需要的机械特性的情况下，信号导体与相邻接地导体之间的边到边的间距也保持相对不变。保持一致的间距可以进一步有利于根据本发明的实施方式的互连系统的所需要的电气特性。

[0123] 为提供所需要的特性，在子卡连接器 120 中使用的构造技术中的一些或全部可以在底板连接器 150 中使用。在示出的实施方式中，与子卡连接器 120 一样，底板连接器 150 包括用于提供所需要的信号传输特性的结构。底板连接器 150 中的信号导体布置成列，信号导体中的每个均包括散置有接地导体的差分对。接地导体相对于信号导体较宽。同样，相邻列具有不同构型。列中的一些可以在端部处具有窄的接地导体以节省空间；同时，在列的端部处围绕信号导体提供所需要的接地构型。此外，在一个列中的接地导体可以定位成邻近在相邻列中的差分对，以作为减少从一个列到下一个列的串扰的方式。此外，损耗材料可以选择性地定位在底板连接器 150 的罩中，以减少串扰，而不会使信号产生不良程度的衰减。此外，相邻信号导体和接地导体可以具有相符部分，使得在信号导体或接地导体的轮廓改变的位置处，信号导体到接地导体的间距可以被保持。

[0124] 图 5A-5B 更详细地示出底板连接器 150 的实施方式。在示出的实施方式中，底板连接器 150 包括具有壁 512 和基底 514 的罩 510。导电元件插入到罩 510 中。在示出的实施方式中，每个导电元件均具有延伸到基底 514 上方的部分。这些部分形成导电元件的匹配接触部并共同地标记为 154。每个导电元件均具有延伸到基底 514 下方的部分。这些部分形成接触尾部并共同地标记为 156。

[0125] 底板连接器 150 的导电元件定位成与子卡连接器 120 中的导电元件对齐。因此，图 5A 示出在底板连接器 150 中设置成多个平行列的导电元件。在示出的实施方式中，平行列中的每个均包括多个差分对信号导体，其中，差分对 540_1、540_2...540_4 被标记。每列还包括多个接地导体。在图 5A 中示出的实施方式中，接地导体 530_1、530_2...530_5 被标记。

[0126] 接地导体 530_1...530_5 以及差分对 540_1...540_4 定位成形成底板连接器 150 中的一列导电元件。该列具有定位成与如晶片 320B（图 3）中的一列导电元件对齐的导电元件。底板连接器 150 中的相邻列导电元件可以具有定位成与晶片 320A 的匹配接触部对齐的导电元件。底板连接器 150 中的列可以从列到列交替构型，以匹配图 3 中示出的晶片 320A、320B 的交替模式。

[0127] 接地导体 530_2、530_3 和 530_4 示出为相对于构成差分对 540_1...540_4 的信号导体较宽。较窄接地导电元件，它们相对于接地导体 530_2、530_3 和 530_4 较窄，包括在列的每个端部处。在图 5A 中示出的实施方式中，较窄接地导体 530_1 和 530_5 电括在包括差分对 540_1...540_4 的列的端部处，并可以例如，通过成形为匹配触头 434_1（图 4B）的匹配接触部与来自子卡 120 的接地导体匹配。

[0128] 图 5B 示出沿图 5A 中标记为 B-B 的线截取的底板连接器 150 的视图。在图 5B 的示意中，列 560A-560B 的交替模式是可见的。包括差分对 540_1...540_4 的列示出为列 560B。

[0129] 图 5B 示出了罩 510 可以包括绝缘区域和损耗区域两者。在示出的实施方式中，诸如差分对 540_1...540_4 的差分对的导电元件中的每个均保持在绝缘区域 522 中。损耗区域 520 可以定位在相同列中的相邻差分对之间以及相邻列中的相邻差分对之间。损耗区域 520 可以连接到例如 530_1...530_5 的接地触头。侧壁 512 可以由绝缘材料或损耗材料制成。

[0130] 图 6A、图 6B 和图 6C 更详细地示出可以在形成底板连接器 150 时使用的导电元件。

图 6A 示出多个宽的接地触头 530_2、530_3 和 530_4。在图 6A 中示出的构型中，接地触头附连到载体带 620。接地触头可以由长的金属薄板或包括载体带 620 的其它导电材料冲压出。单独的触头可以在制造过程期间的任何适合的时间由载体带 620 分割出。

[0131] 如可以看到的，接地触头中的每个均具有成形为条片的匹配接触部。为了附加的刚度，一个或更多个加固结构可以形成在每个触头中。在图 6A 的实施方式中，例如 610 的肋形成在宽接地导体的每一个中。

[0132] 例如 $530_2 \ldots 530_4$ 的宽接地导体中的每个均包括两个接触尾部。用于接地导体 530_2 的接触尾部 656_1 和 656_2 被标记。为每个宽接地导体提供两个接触尾部可以遍及整个互连系统更均匀地分布接地结构，包括在底板 160 内，因为接触尾部 656_1 和 656_2 中的每个将接合底板 160 中的、平行并邻近携载信号的通路的接地通路。图 4A 示出两个接地接触尾部也可以用于子卡连接器中的每个接地导体。

[0133] 图 6B 示出包括例如接地导体 530_1 和 530_5 的较窄接地导体的冲压件。如同图 6A 中示出的较宽接地导体一样，图 6B 中的较窄接地导体具有定形成类似条片的匹配接触部。

[0134] 如同图 6A 中的冲压件一样，图 6B 中的包括较窄接地导体的冲压件包括载体带 630 以便于处理导电元件。单独的接地导体可以在插入到底板连接器罩 510 中之前或之后的任何适合的时间从载体带 630 分割出。

[0135] 在示出的实施方式中，例如 530_1 和 530_2 的较窄接地导体中的每个均包括例如接地导体 530_1 上的 656_3 或接地导体 530_5 上的接触尾部 656_4 的单个接触尾部。尽管仅包括一个接地接触尾部，但由于如图 6B 中所示的窄接地导体在窄接地导体邻近单个信号导体的列的端部处使用，因此多个信号导体之间的关系得到保持。如从图 6B 的示意中可以看到的，用于较窄接地导体的接触尾部中的每个均以与接触尾部 656_1 和 656_2 从宽触头的中心线移位相同的方式偏离匹配触头的中心线。该构型可以用于保持在接地接触尾部与相邻的信号接触尾部之间的间距。

[0136] 如在图 5A 中可以看到的，在图示的底板连接器 150 的实施方式中，例如 530_1 和 530_5 的较窄接地导体也短于例如 $530_2 \ldots 530_4$ 的较宽接地导体。图 6B 中示出的较窄接地导体不包括例如肋 610（图 6A）的加固结构。但是，较窄接地导体的实施方式可以形成有加固结构。

[0137] 图 6C 示出可以用于形成底板连接器 150 的信号导体。与图 6A 和图 6B 中的接地导体一样，图 6C 中的信号导体可以由金属薄板冲压出。在图 6C 的实施方式中，信号导体被成对地冲压，例如对 540_1 和 540_2。图 6C 中的冲压件包括载体带 640，以便于处理导电元件。例如 540_1 和 540_2 的所述对可以在制造期间的任何适当的时间点从载体带 640 分割出。

[0138] 如从图 5A、图 6A、图 6B 和图 6C 中可以看到的，用于底板连接器 150 的信号导体和接地导体可以成形成彼此相符，以保持在信号导体与接地导体之间的恒定间距。例如，接地导体具有例如突起 660 的突起，突起相对于罩 510 的基底 514 定位接地导体。信号导体具有例如互补部 662（图 6C）的互补部，使得当信号导体紧邻接地导体插入到罩 510 中时，信号导体与接地导体的边缘之间的间距保持相对一致，即使在突起 660 附近。

[0139] 同样，信号导体具有例如突起 664（图 6C）的突起。突起 664 可以用作将信号导体保持在底板连接器罩 510（图 5A）的基底 514 中的保持结构。接地导体可以具有例如互补部 666（图 6A）的互补部。当信号导体邻近接地导体定位时，互补部 666 保持在信号导体与

接地导体的边缘之间的相对一致的间距，即使在突起 664 附近。

[0140] 图 6A、图 6B 和图 6C 示出信号导体和接地导体的边缘处的突起的示例，以及形成在相邻的信号导体和接地导体处的相应互补部。可以形成其它类型的突起并且同样地可以形成其它形状的互补部。

[0141] 为方便具有互补部的信号导体和接地导体的使用，底板连接器 150 可以通过从相反侧将信号导体和接地导体插入到罩 510 中来制造。如在图 5A 中可以看到的，接地导体的例如 660（图 6A）的突起压靠基底 514 的底面。底板连接器 150 可以通过从底部将接地导体插入到罩 510 中直到突起 660 接合基底 514 的底侧来组装。由于底板连接器 150 中的信号导体大致互补于接地导体，因此信号导体具有邻近基底 514 的下表面的窄部。信号导体的较宽部邻近于基底 514 的顶表面。由于如果首先将导电元件的窄端部插入到罩 510 中，底板连接器的制造即可简化，因此，底板连接器 150 可以通过从基底 514 的上表面将信号导体插入到罩 510 中来组装。可以将信号导体插入直到例如突起 664 的突起接合基底的上表面。导电元件从两侧插入到罩 510 中方便了具有相符的信号导体和接地导体的连接器部的制造。

[0142] 图 7A 为例如可以在根据本发明的实施方式的子卡连接器中使用的引线框的一部分的简图。图 7A 示出可以是子卡晶片中的一对信号导体的匹配接触部的匹配触头 424_1。如所示的，匹配触头 424_1 布置成落入子卡连接器中的匹配接触部的列 C 中。

[0143] 同样与匹配接触部的列 C 中的匹配触头 424_1 排成一列的是触头 434_1 和 434_2，触头 434_1 和 434_2 可以形成子卡连接器中的接地导体的匹配接触部。示出的构型将接地导体在匹配触头 424_1 两侧定位在列中。在示出的实施方式中，匹配触头 434_1 窄于匹配触头 434_2。

[0144] 如上所述，在一些实施方式中需要使列中的接地导体宽于信号导体。但是，扩展接地导体的宽度会增加电连接器沿着列的方向的尺寸。在一些实施方式中，需要限制电连接器沿信号导体的列的方向的外形尺寸。如图 7A 中所示，限制连接器的宽度的一个方法是使诸如匹配触头 434_1 之类的在列端部的匹配触头窄于诸如匹配触头 4342 之类的在列中的其它匹配触头。较窄的匹配触头 434_1 或者可以形成有与匹配触头 434_2 相同的形状。

[0145] 用于减少连接器在沿匹配触头的列的方向上的尺寸的替代性方法是，偏移双梁匹配接触部的接触点。在图 7A 的实施方式中，触点不偏移。如所示的，匹配触头 434_2 具有两个梁 460_7 和 460_8。这些梁中的每个分别地具有匹配表面 722_1 和 722_2。当包括匹配表面 722_1 和 722_2 的电连接器与互补的连接器匹配时，匹配触头 434_2 将在匹配表面 722_1 和 722_2 处与互补的连接器中的匹配触头接触。在示出的实施方式中，互补连接器中的匹配触头示出为接地导体 530_2。在该实施方式中，接地导体 530_2 示出为条片例如结合图 5 在上文中描述的可以在底板连接器中使用的条片。但是，匹配触头的形状并不是对本发明的限定。

[0146] 如所示的，匹配表面 722_1 和 722_2 分别在接触点 710_1 和 710_2 处接触接地导体 530_2。对于图 7A 中示出的接触构型来说，接触点 710_1 和 710_2 在列 C 的方向上排列。为保证匹配触头 434_2 与接地导体 530_2 可靠地接触，接地导体 530_2 可以构造成具有沿列方向的宽度 W_1。W_1 大于匹配触头 434_2 在匹配接口处的宽度。该附加的宽度保证了即使在连接器保持的匹配触头 434_2 与连接器保持的接地导体 530_2 之间具有偏移，匹配表面 722_1 和 722_2 也都能够接触接地导体 530_2。

[0147] 在一些实施方式中，需要具有小于 W_1 的宽度的匹配触头。图 7B 和图 7C 示出接地

触头 434_2 的替代性实施方式，该触头可以与和接地导体 530_2 一样成形为条片但具有小于 W_1 的宽度的匹配接地导体一起使用。图 7B 示出可以代替匹配触头 4342 使用的匹配触头 750。在该实施方式中，匹配触头 750 可以形成定位在子卡晶片中的相邻对信号导体之间的宽接地导体的匹配接触部。但是，图 7B 中示出的接触构型可以与任何适合的导电元件一起使用。

[0148] 如同匹配触头 434_2 一样，匹配触头 750 包括两个梁 752_1 和 752_2，其梁 752_1 和 752_2 中的每个均分别提供匹配表面 732_1 和 732_2。但是，梁 752_1 和 752_2 构造成使得匹配表面 732_2 沿垂直于列 C 的方向相对于匹配表面 732_1 偏移。当匹配触头 750 接合接地导体 730 时，匹配表面 732_1 和 732_2 在接触点 734_1 和 734_2 处接合接地导体 730。接触点 734_2 沿方向 O 从接触表面 734_1 偏移。如所示的，方向 O 垂直于列 C。由于接触点 734_1 和 734_2 的该偏移，接地触头 730 可以具有小于接地导体 530_2 的宽度 W_1 的宽度 W_{1B}。

[0149] 在图 7B 的实施方式中，匹配表面 732_2 通过形成梁 752_1 中的梁 752_2 而从匹配表面 732_1 偏移。当具有带梁的匹配触头的引线框结合到电连接器中时，梁的前缘可以以防止梁的远端与匹配导体中的导电元件接触的方式而保持在连接器外壳中。这样的构造可以防止梁上的匹配导体中的导电元件的“卡夹”，“卡夹”会防碍正常的匹配并破坏连接器。对于如图 7B 中示出的匹配触头，梁 752_1 的远端可以安装到外壳中以防止卡夹。梁 752_2 的远端不会受到外壳的保护。但是，所示的构型将梁 752_2 的远端定位在梁 752_1 的远部 736 之后，其防止了接地导体 730 “卡夹”在梁 752_2 上。

[0150] 图 7B 的实施方式只是可以用于形成偏移接触点的构型的一个示例。图 7C 示出替代性实施方式。匹配触头 760 包括梁 762_1 和 762_2。两个梁提供两个匹配表面 742_1 和 742_2。梁 762_2 短于梁 762_1，引起匹配表面 742_2 从接触面 742_1 偏离。因此，当匹配触头 760 接合另一连接器中的例如接地导体 740 的匹配触头时，匹配表面 742_1 和 742_2 在偏置接触点 744_1 和 744_2 处接合接地导体 740。如所示的，接触点 744_2 沿方向 O 从接触点 744_1 偏离。因此，接地导体 740 可以具有窄于接地导体 530_2（图 7A）的宽度 W_1 的宽度 W_{1C}。此外，如在图 7B 的构型中一样，由于梁 762_2 不完全地包括在梁 762_1 中，因此梁 762_1 的在匹配表面 742_1 附近的远端可以窄于梁 752_1 的在匹配表面 732_1（图 7B）附近的远端。因此，在一些实施方式中，接地导体 740 的宽度 W_{1C} 可以窄于接地导体 730（图 7B）的宽度 W_{1B}。图 7C 中的实施方式也可以以减少卡夹的方式使用。梁 762_1 的远端可以在外壳中保护。梁 742_2 的远端由部分 746 保护，由此防止接地导体 740 卡夹在梁 742_2 上。

[0151] 在图 7A 中示出的实施方式中，沿列的相邻对信号导体被终止于例如匹配触头 434_2 的匹配触头的宽接地导体分隔。但是，如图 7B 和图 7C 的实施方式中的偏置接触点可以与其它导电元件一起使用。例如，诸如晶片 320B（图 3）之类的一些晶片可以在列的端部处具有接地导体，该接地导体终止于例如匹配触头 434_1 的较窄匹配触头。这些较窄接地导体可以具有带有偏置接触点的匹配触头。同样，对中的信号导体可以具有也使用带有偏置接触点的多个梁的匹配触头。这种设置允许较窄导电元件用于信号导体和 / 或匹配连接器中的窄接地导体。因此，尽管图 7B 和图 7C 示出仅与宽接地导体有关的偏置接触点，但类似的方法可以关于用于携载信号的导电元件的、或用于接地导体的窄匹配触头的匹配触头而使用。

[0152] 尽管如上所述的电气互连系统 100 提供了具有所需要的电气特性的高速、高密度的互连系统，但也可以结合其它特征以提供甚至更大的密度或以其他方式提供在一些实施

方式中需要的性能特征。

[0153] 图 8A 和图 8B 示出引线框 800，引线框 800 可以在形成子卡连接器中的晶片时取代引线框 400 使用。在图 8A 中示出的实施方式中，引线框 800 包括晶片条带组件 810A 和 810B，晶片条带组件 810A 和 810B 中的每个均可以用于形成不同类型的晶片。此处，晶片条带组件 810A 具有与晶片条带组件 410A（图 4A）相同的形状。

[0154] 晶片条带组件 810B 具有与晶片条带组件 410B（图 4A）的形状类似的形状。但是，晶片条带组件 810B 在由晶片条带组件 810B 的导电元件形成的该列匹配触头中的最外侧接地导体的匹配触头的形状方面不同。在图 4A 中示出的实施方式中，最外侧接地匹配触头 434_5 成形为双梁触头。但双梁触头 434_5 示出为等于例如接地匹配触头 434_2 的其它接地匹配触头。相反地，如图 8A 中示出的，匹配触头 834_5 可以冲压成大致平面的构件。大致平面的构件具有上表面 862 和边缘 860。

[0155] 图 8B 示出在制造的随后阶段中的晶片条带组件 810B。在该阶段，晶片条带组件 810B 已经形成为垂直于冲压出引线框 800 的金属薄板的起始面。因此，在图 8B 中，边缘 860 是可见的，但垂直于边缘 860 的表面 862 不可见。

[0156] 图 8B 示出以这种方式形成接地触头能够增加连接器的密度的方法。在图 8B 中的晶片条带组件 810 上附加前外壳部 830 的轮廓。如可以看到的，前外壳部 830 具有宽度 W_8，宽度 W_8 延伸到接地匹配触头 834_5 的面向外的表面，使接地匹配触头 834_5 的面向外的表面显露于前外壳部 830 的面向外的表面。因此，与可以用于封闭如图 4A 中的匹配触头的外壳相比，不需要前外壳部 830 延伸越过列中的最外侧导体。

[0157] 因此，前外壳部 830 的宽度 W_8 可以小于需要包括例如晶片条带组件 410B（图 4A）的晶片条带组件的匹配接触部的前外壳部的宽度。尽管前外壳部 830 的宽度可以小于封闭晶片条带组件 410B 所需要的宽度，但晶片条带组件 810B 中的成对的信号导体，仍然通过接地触头穿过列束缚到两侧。具体地，最长的一对信号导体 824_4 通过接地触头束缚到任一侧，产生与围绕所述对信号导体 424_4（图 4A）相同的围绕对 824_4 的接地环境。

[0158] 减小列宽度同时保持电气特性改进了高速连接器的密度。例如，图 8B 示出了四对连接器。如果减少由最外侧接地导体的匹配接触部占据的空间的量，则允许另外的对布置到列中，通过沿子卡连接器 140（图 11）的边缘每单位长度允许更多的信号导体，实现了更大的密度。

[0159] 图 9A 示出使用大致具有接地匹配触头 834_5 的形状的外部接地匹配触头形成的晶片。在图 9A 中示出的实施方式中，示出了三对连接器。此外，信号导体和接地导体都包括可以进一步减小列的长度的大致如图 7C 中一样的匹配接触元件。此处，对 924_1、924_2 和 924_3 形成晶片 920B 中的一列导电元件中的三对信号导体。接地匹配触头 934_1、934_2、934_3 和 934_4 同样也包括在列中，使得每一对均定位在相邻两个接地匹配触头之间。

[0160] 第二晶片，晶片 920A 示出与晶片 920B 对齐。在示出的实施方式中，晶片 920B 中的匹配触头的列终止于邻近最长对信号导体的平面接地匹配触头 934_4，最长对信号导体在该示例中为对 924_3。类似的平面匹配触头不是必须包括在晶片 920A 的匹配触头的列的端部。相反，在示出的实施方式中，由晶片 920A 中的匹配触头形成的列中的最后的匹配触头为接地匹配触头 934_5。由于例如晶片 920A 和 920B 的相邻晶片具有不同构型的信号导体和接地导体，因此在晶片 920A 中的接地导体相对于接地匹配触头 934_4 可以具有沿列方向的

不同位置，使得尽管接地匹配触头 934_5 在列方向上宽于接地匹配触头 934_4，晶片 920A 中的接地导体也将装配在具有与接地匹配触头 934_4 重合的最外侧表面的容积中。

[0161] 图 9B 示出具有如图 9A 中示出的匹配接触部的晶片如何集成到连接器中。图 9B 示出前外壳 930。如上所述，前外壳可以由绝缘材料形成、具有或不具有损耗部或其它屏蔽部件。在示出的实施方式中，前外壳 930 由例如塑料的电介质材料模制。

[0162] 前外壳 930 沿外侧模制有槽 950。几列腔 952 模制在前外壳 930 的内部中。腔 952 中的每个在图 9B 中图示的方向从前外壳 930 的顶面到底面穿过。腔 952 中的每个成形用于容纳匹配触头，例如接地匹配触头 934_1、934_2、934_3 或 934_5，或例如对 924_1、924_2 或 924_3 的信号导体对。尽管腔 952 中的匹配接触部在 9B 中不可见，但匹配接触部通过前外壳 930 的底面中的开口露出。通过这些开口，来自匹配的连接器中的导电元件的匹配触头可以进入腔 952，以与来自晶片 920A 和 920B 的匹配触头进行电气连接。

[0163] 每个槽 950 成形用于容纳例如接地匹配触头 934_4 的匹配接触部。因此，当晶片 920A 和 920B 插入到前外壳 930 中时，晶片 920A 和 920B 中的导电元件的匹配接触部占据腔 952 中两列和槽 950。其它晶片对可以类似地插入到前外壳 930 中，产生任何所需要的长度的连接器。

[0164] 在示出的实施方式中，接地匹配触头 934_4 露出在前外壳 930 的侧壁中。被设计用于与使用图 9B 中示出的模块形成的连接器匹配的连接器可以具有定位成在前外壳 930 的外侧与接地匹配触头 934_4 匹配的相应接地匹配触头。这种连接器的示例在示出适合的底板模块的图 10A、10B 和 10C 中提供。

[0165] 图 10A 示出用于形成这样的底板模块的罩 1010。罩 1010 可以以与罩 510（图 5A）相同的方式构造。但是，可以使用任何适合的材料或构造技术。如图 10A 中所示，罩 1010 包括相对的侧壁 1012A 和 1012B。罩 1010 还包括基底 1014。基底 1014 包括开口，接触元件可以通过开口从基底 1014 的上方或下方插入。图 10B 示出具有已插入的导电元件的罩 1010。如在图 10B 中可以看到的，导电元件设置成列并且可以成形为条片，提供匹配接触表面，大致如在图 6A-6C 中所示的。

[0166] 此外，罩 1010 可以包括侧壁槽 1060（图 10A），侧壁槽 1060 适于容纳导电元件，用于与例如露出在外壳 930 的外表面中的 9344 的接地匹配触头匹配。由于在示出的实施方式中，每隔一列的导电元件终止于例如 9344 的平面接地匹配触头，因此底板罩 1010 包括用于每两列的导电元件的槽 1060。

[0167] 如所示的，槽 1060 可以通过罩 1010 的基底 1014 与开口 1052 连通。因此，插入槽 1060 中的接触元件可以具有基底 1014 上方的匹配接触部和基底 1014 下方的接触尾部。如在图 10B 的示例中示出的，导电元件 1030_4 可以通过开口 1052 插入到槽 1060 中。导电元件 1030_4 可以具有接触尾部 1056_{10}。接触尾部 1056_{10} 可以与列中的其它导电元件的接触尾部，例如接触尾部 1056_1 排成一列，列中的其它导电元件定向成与子卡连接器的一个列中的导电元件匹配。

[0168] 导电元件 1030_4 邻近可被指定为信号导体对的对 1040_3 定位。因此，接地导体和信号导体的相对定位可以通过匹配接口实现，该匹配接口在例如使用如图 9B 中示出的模块形成的连接器与使用如图 10B 中示出的模块形成的连接器匹配时形成。

[0169] 图 10C 示出导电元件 1030_4，并且导电元件 1030_2 可以插入到罩 1010 中。在示出

的示例中，导电元件 1030_4 具有接触尾部，此处表示为柔性部分 1056_{10}。在相反端，导电元件 1030_4 包括匹配接触部，此处成形为梁 1064。梁 1064 可以成形用于装配在槽 1060 中。当图 10B 中的连接器模块未匹配到另一连接器时，梁 1064 的远端的接触表面 1066 将延伸出槽 1060。在该位置，当插入例如图 9B 中示出的连接器模块时，接触表面 1066 可以与平面接地匹配触头 934_4 接触。

[0170] 梁 1064 产生使匹配接触面 1066 压靠在平面接地匹配触头 934_4 的弹力。为有助于产生这样的弹力，槽 1060 的尺寸可以设定成提供允许梁 1064 在槽 1060 中移动的间隙。

[0171] 为了在接地匹配触头 934_4 与基质中耦接到接触尾部 1056_{10} 的结构之间提供电气耦合，梁 1064 通过中间部 1062 耦接到接触尾部 1056_{10}。在图 10B 中示出的实施方式中，导电元件 1030_4 可以从下方插入到罩 1010 中，使得中间部 1062 插入在基底 1014 中的槽（未示出）中。保持结构可以包括在中间部 1062 上，以将导电元件 1030_4 保持到罩 1010。

[0172] 转到图 11，图 11 示出用于增加高速连接器的密度的替代性方法。图 11 示出用于匹配接触部的替代性构型，此处称为“波浪形”匹配触头。此处，“波浪形”是指，由沿匹配触头的长度方向交替改变的横向于匹配触头的纵向尺寸的多处弯曲或折叠产生的结构。弯曲或折叠提供折皱的、或“波浪形”的外形。如以下更详细的描述的，每个波浪形触头可以相对较窄，允许导电元件之间的间距减小同时仍提供所需要的电气和机械特性。

[0173] 图 11 中的波浪形匹配接触构型可以与信号导体或接地导体一起使用，或在一些实施方式中，与信号导体和接地导体两者一起使用。波浪形匹配触头可以代替图 7A、图 7B 或图 7C 中示出的匹配接触构型中的任一种而使用。然而，在一些实施方式中，图 11 中的波浪形接触构型可以在这样的连接器中使用：所述连接器包括一些导电元件，所述导电元件与一个或更多个其它导电元件结合使用波浪形接触构型，所述一个或更多个其它导电元件使用图 7A、图 7B 或图 7C 中示出的匹配接触构型的一或更多个。在一些实施方式中，子卡连接器将包括如图 9B 中示出的前外壳，所述前外壳具有嵌入到外壳的外表面中的接地匹配接触部。外壳中的匹配接触部将是波浪形触头。

[0174] 图 11 示出与匹配触头 1120 接合的波浪形匹配触头 1110。匹配触头 1110 可以是信号导电元件或接地导电元件的一部分。尽管在图 11 中未示出，但这样的导电元件可以具有中间部和接触尾部，用于接合到印刷电路板或其它基质。在示出的实施方式中，匹配触头 1110 为子卡连接器中的导电元件的匹配触头。但是，匹配触头 1110 作为示例而不是限定被描述为子卡连接器的一部分。如图 11 中示出的匹配触头可以在任何适合的连接器中使用。

[0175] 匹配触头 1120 可以是适于与包括匹配触头 1110 的连接器匹配的连接器中的导电元件的一部分。在图示的示例性实施方式中，匹配触头 1120 为例如图 5A 或图 10B 中示出的底板连接器中的条片。但是，匹配触头 1120 可以是任何适当的连接器的一部分。应当理解，出于简单的目的，图 11 仅示出，可以在两个匹配电连接器中存在的单套匹配触头。已匹配的连接器可以包括任意数量的导电元件，导电元件可以设置在多个行和 / 或列中，使得所示出的结构可以在电连接器中重复出现。

[0176] 如图 11 中所示，匹配触头 1110 和 1120 在腔 1122 中接合，腔 1122 可以是连接器的前外壳中的腔，例如前外壳 930 中的腔 952（图 9B）。在示出的实施方式中，前外壳由绝缘材料形成并因此具有绝缘壁，使得匹配触头可以邻近壁或甚至压靠在壁上定位，而不产生电气短接。

[0177] 在图 11 中示出的实施方式中，匹配触头 1110 可以由例如由金属薄板冲压出的单个细长的导电构件形成。由于弯曲段提供给匹配触头 1110 的“波浪形”形状，因此多个接触点设置在匹配触头 1110 与匹配触头 1120 之间，弯曲段中的每个均具有提供接触区域的回折点。此处，示出三个接触点 1112、1114 和 1116。由于匹配触头 1110 包括三个弯曲段 1118A、118B 和 1118C，因此在该示例中形成了三个接触点。每个弯曲段均包括回折点。匹配触头 1110 的面向匹配触头 1120 的表面的切线在这些回折点处中的每一个处改变方向，在接触点 1112、1114 和 1116 中的每一个处产生露出表面。在这些接触区域中的这些露出表面处可以被形成用于改进其作为接触区域的有效性。例如，它们可以镀有金或其它软金属和 / 或其它导电的并且抗氧化的化合物。可替代地，每个回折点均可以形成有凹痕或其他窄的结构，凹痕或其他窄的结构在相对较小的区域上集中接触力，其可有助于形成可靠的电气连接。

[0178] 此处，匹配触头 1110 成形用于提供三个接触点。但是，可以提供任何适当数量的接触点。例如，在一些实施方式中，可以通过沿匹配触头 1110 的长度仅具有两个弯曲段来提供两个接触点。相反地，可以通过沿匹配触头 1110 的长度提供三个以上的弯曲段来提供三个以上的接触点。

[0179] 在图 11 的实施方式中，接触点 1112、1114 和 1116 处的接触力通过压缩匹配触头 1110 来提供。如可以看到的，匹配触头 1110 和 1112 被约束在腔 1122 中。匹配触头 1110 邻近腔 1122 的壁 1132 并且被腔 1122 的壁 1132 约束。匹配触头 1120 沿腔 1122 的壁 1134 定位并被腔 1122 的壁 1132 约束。在匹配触头定位在例如前外壳 930（图 9B）的前外壳中的实施方式中，壁 932 和 934 可以由用于模制前外壳 930 的绝缘材料形成。但是，这种壁可以以任何适当的方式形成。

[0180] 图 12A、图 12B 和图 12C 示出匹配顺序，该匹配顺序示范了可以在例如 1112、1114 和 1116 的接触点中的每个处产生接触力的方式。图 12A 示出了被对准以进行匹配时的匹配触头 1110 和 1120。腔 1122 的壁可以成形为便于该对准。例如，壁 1134 示出为具有锥形表面 1222 而壁 1132 示出为具有锥形表面 1224。这些锥形表面定向用于引导匹配触头 1120 进入与匹配触头 1110 的接合。匹配触头 1110 和 1120 都可以是互连系统中的连接器的一部分。此外，如在本领域中已知的，互连系统和连接器都可以包括对准机构，例如引导销（未示出），以有助于匹配触头 1110 和 1120 在所示的位置中的对准。

[0181] 在图 12A 中示出的匹配之前，匹配触头 1110 具有从壁 1132 延伸距离 D_1 的“波浪形”部分。在示出的实施方式中，距离 D_1 可以通过形成具有基本弯曲形状的的匹配触头 1110 来增加。如示出的，匹配触头 1110 具有由波浪形的波幅 A_1 限定的弯曲包迹 E1。此处，波幅表示为最大值与最小值之间的距离，如由回折点之间的在回折点处垂直于触头的表面的方向上的距离限定的距离。此外，距离 D_1 可以通过相对于壁 1132 提供大致的倾斜来增加。

[0182] 匹配触头 1120 具有厚度 T_1，使得距离 D_1 加上厚度 T_1 超过腔 1122 的宽度 W。因此，当如图 12B 中所示的匹配触头 1120 插入到腔 1122 中时，匹配触头 1120 将朝向壁 1132 挤压匹配触头 1110 的波浪形部。

[0183] 如图 12B 中所示，作为匹配触头 1110 与匹配触头 1120 之间的匹配顺序，匹配触头 1120 相对于匹配触头 1110 滑动。匹配触头 1120 首先接合匹配触头 1110 的锥形表面 1250。在本实施方式中，锥形表面 1250 由形成波浪形触头 1110 的弯曲段形成。随着匹配

触头 1120 压靠锥形表面 1250，匹配触头 1120 使匹配触头 1110 朝向壁 1132 偏转。

[0184] 随着匹配触头 1110 的远端朝向壁 1132 偏转，匹配触头 1110 可以保持其如图 12A 中所示的弯曲形状。然而，根据匹配触头 1110 的弯曲段的相对尺寸和形状，匹配触头的形状可以改变。匹配触头 1110 的总体曲率和波浪形段的波幅之一或两者可以改变。此外，匹配触头 1110 的倾斜角度可以减小。因此，图 12B 示出在匹配触头 1110 和 1120 之间接合之后，匹配接触部 1120 具有弯曲包迹 E2，包迹 E2 可以具有比包迹 E1 更大的曲率半径。此外，弯曲段中的一些或全部的波幅可以减小到 A2，并且可以朝向壁 1132 挤压波浪形接触结构使得倾斜角度减小。

[0185] 不论匹配触头 1110 是否在最初改变形状，随着在匹配触头 1120 的细长方向进一步推压匹配触头 1120，匹配触头 1120 将沿锥形表面 1250 进一步滑动，从而朝向壁 1132 挤压匹配触头 1110。当匹配触头 1110 的一部分压靠壁 1132 时，匹配触头 1110 的形状将改变或进一步改变。在匹配触头 1110 具有大致弯曲的形状的实施方式中，远部 1252 将首先与壁 1132 接触。

[0186] 当远部 1252 与壁 1132 接触时，随着匹配触头 1110 压靠壁 1132，匹配触头 1110 中的弯曲将变平。图 12C 示出，当匹配触头 1110 中的弯曲已经通过使匹配触头 1110 压靠壁 1132 而变平时的匹配触头 1110。

[0187] 如通过在图 12A、图 12B 和图 12C 中示出的形状的变化过程可以看到的，在匹配触头 1110 和 1120 接合之前，匹配触头 1110 从壁 1132 延伸距离 D_1。匹配触头 1110 的波浪形远端具有长度 L_1。由于匹配触头 1120 接合锥形表面 1250，因而产生了垂直于壁 1132 的推力。该力使匹配触头 1110 的远端朝向壁 1132 偏转。因此，在图 12B 中示出的状态下，匹配触头 1110 从壁 1132 延伸 D2 的最大量。减小匹配触头 1110 的波浪形端部的曲率的力也可有助于伸长触头。因此，在图 12B 中示出的状态下，匹配触头 1110 的波浪形远端具有长度 L_2。长度 L_2 可以比长度 L_1 长。

[0188] 随着匹配过程继续进行并且匹配触头 1120 沿匹配触头 1110 进一步滑动，可以产生垂直于壁 1132 的另外的力。该力将继续减小匹配触头 1110 的波浪形部的曲率。图 12C 示出这样的实施方式：其中，匹配触头 1110 和 1120 的尺寸相对于腔 1122 的宽度 W 确定成使得当匹配触头 1120 已经完全插入时，匹配触头 1110 的波浪形部被压缩在匹配触头 1120 和壁 1132 之间。

[0189] 在该状态下，波浪形触头 1110 的上表面上的回折点压靠壁 1132 使得匹配触头 1110 的波浪形远端部不再弯曲。此外，波浪形接触部可以压靠壁 1132 使得波浪形触头 1110 中的波的波幅减小。例如，图 12C 示出在匹配时波的波幅已减小到 A_3。在示出的实施方式中，波幅 A_3 也由壁 1132 与匹配触头 1132 上的最远点之间的距离 D_3 限定。如示出的，距离 D_3 可以小于在如图 12A 中示出的非压缩状态下的波浪形触头 1110 中的波的波幅 A_1。压缩匹配触头 1110 的波浪形远端部可以进一步伸长波浪形部，从在匹配触头 1110 和 1120 完全接合时产生长度 L_3。

[0190] 压缩波浪形触头 1110 还产生在波浪形触头 1110 的接触区域中的每一个与匹配触头 1120 之间的接触力。

[0191] 匹配触头 1110 可以由提供适当的电气和机械特性的材料构造。例如，匹配触头 1110 可以由具有提供所需要的接触力的宽度和厚度的材料冲压出。例如，厚度 T_2 可以为大

约 10 毫英寸或更小。在一些实施方式中，厚度可以为约 8 毫英寸或更小。匹配触头 1110 的波浪形部的长度 L_1 可以选择成提供所需要数量的接触点。例如，长度 L_1 可以在 2mm 至 10mm 之间。在一些实施方式中，长度可以为约 4mm。但是，可以使用任何适当的长度。

[0192] 匹配触头 1120 可以形成为具有任何适合的尺寸。但是，图 12A 和图 12B 示出了选择成提供所需要的电气特性的尺寸。可以提供所需电气特性的一种方式是，减少可以产生对高频运行不良的短尾部的触头滑接区。当匹配触头 1110 和 1120 匹配时，匹配触头 1120 的一部分可以延伸越过接触点 1112。该部分，此处表示为短尾部 1250，延伸越过接触点 1112 的量 S_1。这样的构型是需要的，因为它保证了匹配触头 1110 和 1120 之间在所有的目标接触点处的的接触，即使基于保持匹配触头 1110 和 1120 的连接器的设计，轻微的偏移或部件公差会防止匹配触头 1120 在腔 1122 中延伸到所需要的程度。尽管出于电气性能的原因，这种短尾部是不良的，但将短尾部设计到常规连接器中保证了匹配连接器中的匹配触头能够充分匹配，即使偏移或与改变匹配触头的相对位置的制造公差相关的部件尺寸变化。短尾部长度的设计也可以称为触头“滑接区”。在一些情形中，短尾部长度的设计可以从穿过连接器，或在一些情形中，穿过根据生产工艺制造的多个样本连接器的平均短尾部长度推断出。

[0193] 但是，在具有这样的波浪形触头的实施方式中：所述波浪形触头沿匹配接触部在匹配期间的相对运动的方向（这里为匹配触头的细长尺寸）提供布置的多个接触点，由于匹配触头 1110 和 1120 的偏移结果在没有常规触头设计的连接器中显著，因此标称的或设计的短尾部长度 S_1 可以相对于常规连接器减小。例如，如果匹配触头 1120 插入腔 1122 中仅到点 I_1，则匹配触头 1110 和 1120 不会在接触点 1112 处接合。但是，在接触点 1114 和 1116 处可以产生足够的接触。因此，仍然可以提供两个接触点，保证可靠的电气连接，使得连接器的运行不会出现故障。因此，短尾部长度 S_1 可以设计得更短，以改进整体电气性能而不显著地影响接触可靠性。例如，滑接区可以为小于 2mm，在一些实施方式中，滑接区可以小于 1.5mm。在一些实施方式中，滑接区可以为 1.1mm 或更小，例如在一些实施方式中的 0.8mm 或 1.5mm。更短设计的短尾部长度 S_1 导致了连接器性能方面的较少变化。例如，当对具有如图 12C 图示的短尾部长度的设计的多个连接器进行分析时，通过导体的阻抗的方差相对于设计目标 100Ohms 为大约 +/-6Ohms。由于制造公差，一些变化量是导体所固有的。但是，具有类似制造公差的常规设计的连接器的变化水平为大约 +/-14Ohms。

[0194] 图 12A、图 12B 和图 12C 也示出可以影响匹配接触部的电气性能的另一设计因素。通过由单个细长的构件而不是例如如图 7A 中示出的两个梁形成匹配触头 1110，匹配触头的宽度可以减小。匹配触头 1120 的宽度可以具有相应的减小。以该方式减小匹配触头的宽度可以相对于常规电连接器增加匹配接触区域中的阻抗。为保持所需要的阻抗，匹配触头 1120 的厚度 T_1 可以增加。例如，厚度 T_1 可以大于 8 毫英寸。在一些实施方式中，厚度可以处于 8 至 15 毫英寸之间，而在一些实施方式中可以为 10 毫英寸或 12 毫英寸。相反，匹配触头 1110 的厚度 T_2 可以更小。在一些实施方式中，厚度 T_2 可以为大约 8 毫英寸。

[0195] 图 13 示出具有波浪形匹配接触部的电连接器的其它尺寸。图 13 以俯视图示出导电元件的匹配接触部，其中，可以看到波浪形匹配接触部，该波浪形匹配接触部叠加到它们匹配到的平面触头上。此处，示出了一对信号导电元件 1360_{1A} 和 1360_{1B}。在信号导体元件对的任一侧上的是接地导电元件 1350_1 和 1350_2。在信号导电元件 1360_{1A} 和 1360_{1B} 中的接

地导电元件 1350_1 和 1350_2 中的每个均可以占据例如可以在子卡组件的晶片中实施的列中的一个位置。

[0196] 如示出的，接地导电元件 1350_1 和 1350_2 中的每一个以及信号导电元件 1360_{1A} 和 1360_{1B} 中的每一个均包括波浪形匹配触头，示出为分别与接地导电元件 1350_1 和 1350_2 关联的波浪形匹配触头 1352_1 和 1352_2，和分别与信号导电元件 1360_{1A} 和 1360_{1B} 关联的波浪形匹配触头 1362_{1A} 和 1362_{1B}。波浪形匹配触头中的每个均可以大致成形为图 11 中的形状，以通过来自匹配连接器的相关匹配触头提供多个接触点。例如，波浪形匹配触头 1352_1 沿导电元件 1330_1 产生多个接触点。波浪形匹配触头 1362_{1A} 沿导电元件 1340_{1A} 的长度产生多个接触点。波浪形匹配触头 1362_{1B} 沿导电元件 1340_{1B} 的长度产生多个接触点并且波浪形匹配触头 1352_2 沿导电元件 1330_2 的长度产生多个接触点。

[0197] 从图 13 的定向中，可以看到波浪形匹配触头中的每个均可以成形为细长的构件。因此，在一些实施方式中，接触力可以至少部分地通过压缩波浪形构件产生，因此波浪形匹配触头中的每个均可以具有相对较小的宽度。此处，与信号导电元件相关联的波浪形匹配触头中的每个均具有宽度 W_{S2}。宽度 W_{S2} 可以小于 0.5 毫米。在一些实施方式中，宽度可以为大约 0.4 毫米。如在图 13 中可以看到的，该宽度小于导电元件的中间部的宽度。

[0198] 如示出的，波浪形匹配触头中的每个均与大致平面的构件，此处形成为底板连接器的条片相匹配。为了即使在偏移或与制造公差相关的变化出现的情况下保证正常连接，平面构件可以宽于波浪形匹配触头。因此，图 13 示出具有宽度为 W_{S1} 的匹配接触部的信号导电元件 1340_{1A} 和 1340_{1B}，宽度 W_{S1} 稍微宽于宽度 W_{S2}。宽度 W_{S1} 可以为大约 0.6 毫米。但是，连接器可以构造有具有任何适当尺寸的导电元件。但是，波浪形匹配触头的相对紧凑的特性允许信号导体相对靠近地定位。在一些情况下，信号导电元件 1360_{1A} 与信号导电元件 1360_{1B} 之间的沿列的信号间距的中心间距为大约 1.5 毫米或更小。在一些实施方式中，间距可以为 1.35 毫米或 1.3 毫米。

[0199] 在一些实施方式中，例如接地导电元件 1350_1 和 1350_2 的接地导电元件可以具有相同尺寸以及相对于如信号导电元件 1360_{1A} 和 1360_{1B} 的相邻导电元件的间距。但是，在示出的实施方式中，接地导电元件示出为具有比信号导电元件 1360_{1A} 和 1360_{1B} 的匹配触头 1362_{1A} 和 1362_{1B} 稍微更宽的匹配触头 1352_1 和 1352_2。提供更宽的接地导电元件可以改进信号整体性。此处，波浪形匹配接地触头中的每个均具有宽度 W_{G2}，在一些实施方式中，W_{G2} 可以为大约 0.6 毫米。但是，可以使用任何适合的尺寸。

[0200] 如同信号导电元件一样，匹配导电元件的平面部可以宽于波浪形匹配触头。因此，图 13 示出导电元件 1330_1 具有宽度 W_{G1}。例如，在一些实施方式中，宽度 W_{G1} 可以为 0.8 毫米，或者在其它实施方式中为 1.0 毫米。这种宽度可以允许在诸如 1360_{1A} 的信号导电元件与诸如接地导电元件 1350_1 的相邻接地导电元件之间的中心间距为大约 1.5 毫米或更小。在示出的实施方式中，所述间距可以为约 1.3 毫米。

[0201] 在图 13 的实施方式中，一致的中心间距提供在列中的导电元件中的每个之间。但是，其它构型也是可以的。例如，用于信号导电元件 1360_{1A} 和 1360_{1B} 的波浪形匹配触头 1362_{1A} 和 1362_{1B} 不是必须以如用于定位信号导电元件 1360_{1A} 和 1360_{1B} 的其它部分的相同中心线间距来分隔。作为一个示例，波浪形匹配触头 1362_{1A} 和 1362_{1B} 可以形成用于提供比信号导电元件 1360_{1A} 和 1360_{1B} 的其它区域中小的中心线间距。较小的间距可以提供更紧密的

电耦合，其可以减少对噪音的敏感性或者如果使用图 13 中示出的一致间距则提供不同信号阻抗。

[0202] 此外，应当理解，图 13 示出一列导电元件的一部分。在一些实施方式中，多对信号导体将包括在连接器的列中。因此，图 13 中示出的结构可以以重复的样式延续，其中由接地导电元件分开另外对的信号导电元件。该样式可以穿过整个列重复出现，其中信号导电元件中的每个成形在接触区域中，类似信号导电元件 1360_{1A} 和 1360_{1B} 和 1340_{1A} 以及 1340_{1B}。接地导电元件中的每个可以如接地导电元件 1350_1 和 1350_2 和 1330_1 以及 1330_2 一样成形。但是，如上所述，在一些实施方式中以及对连接器中的一些晶片来说，接地导电元件的不同构型可以在列的任一端被采用。例如，如同结合图 8A、图 8B、图 9A、图 9B、图 10A、图 10B 和图 10C 在上文中描述的实施方式一样，子卡连接器模块中的最外侧的接地导电元件可以具有露出在前外壳的外部侧的平面。此外，如结合图 4 和图 8A 所描述的一样，一些列在列的最内端可以不具有接地导体。

[0203] 图 14 和图 15 示出波浪形匹配触头的另一替代性实施方式。例如，图 14 示出波浪形匹配触头不是必须关于平行于导电元件的纵向方向的轴线对称。图 14 示出具有弯曲段 1418A、1418B 和 1418C 的波浪形匹配触头 1462。这些弯曲段成形为使得波浪形匹配触头 1462 压靠壁 1432 的表面区域比面对壁 1434 的要多。可替代地，波浪形匹配触头可以构造有不对称结构，使得压靠平面匹配触头的表面区域比压靠例如壁 1432 的外壳的壁的要多。

[0204] 图 14 只示出用于波浪形触头的一个可行的替代性形状。作为其它可能变型的示例，弯曲段中的每一个的曲率半径可以比所示出的大或小。在一些实施方式中，曲率半径可以足够小使得例如 1418A、1418B 和 1418C 的弯曲段以折叠状而不是逐渐弯曲的连续段出现在细长的构件中。波浪形触头的其它参数也可以变化。例如，弯曲段的数量和之间的间距可以变化以增加或减少波浪形匹配触头 1462 的长度。同样，波浪形段的波幅不是必须沿波浪形匹配触头的长度统一。例如，需要使一个或更多个弯曲段具有比其它弯曲段更大的波幅。

[0205] 图 15 示出也在保持根据本发明的一些实施方式的波浪形触头的外壳中可以进行的改型。图 15 示出类似于图 11 中的匹配触头成形的波浪形匹配触头 1562。此处，波浪形匹配触头 1562 定位在外壳 1522 中，在外壳 1522 中可以形成与来自另一连接器的平面构件 1520 一起的匹配接口。在图 15 的实施方式中，封闭腔 1522 的外壳成形为便于波浪形匹配触头 1562 与平面构件 1520 之间的精确匹配。在示出的实施方式中，外壳包括成形为与壁 1434（图 14）类似的壁 1534。壁 1532 可以成形为通过减少对波浪形匹配触头 1562 的破坏的可能性而便于波浪形匹配触头 1562 与平面构件 1520 之间的匹配。如示出的，限定腔 1522 的一个边界的壁 1532 具有带有锥形面向外部的面 1636 的突起 1638。突起 1638 延伸到腔 1522 中足够距离使得波浪形匹配触头 1562 的远端 1644 由突起 1638 防护。通过该方式，减小了平面构件 1520 卡夹到远端部 1644 上的可能性。

[0206] 通过提供带有锥角的远端部 1544，卡夹的可能性被进一步减小，当平面构件 1520 插入到腔 1522 中时锥角趋向于将平面构件 1520 朝向壁 1534 引导。

[0207] 在一些实施方式中，突起 1538 可以具有突出壁部 1540 或其它结构，它们可以卡住波浪形匹配触头 1562 的远端部 1544。这种结构可以在与平面构件 1520 匹配时限制波浪形匹配触头 1562 的伸长量。例如，如在图 12A、12B 和 12C 中所示，波浪形匹配触头可以从其

非匹配状态时的长度 L_1 展开到其匹配状态时的长度 L_3。该展开是靠着例如壁 1532 的壁压缩波浪形匹配触头的结果。但是，如果连接器的壁 1532 或其它构件包括限制波浪形匹配触头 1562 能够伸长的量的结构，由于平面构件 1520 插入到腔 1522 中则波浪形匹配触头 1562 的部分可以定位在压缩状态中。如果波浪形匹配触头 1562 延长直到远端部 1544 抵接突起 1538 上的表面 1540 则会出现这种状况。当波浪形匹配触头 1562 定位在压缩状态时，另外的接触力可以相对于平面构件 1520 产生。但是，在一些实施方式中，连接器外壳可以形成为使得当匹配时远端 1544 不被限制。这种实施方式在图 18 中示出。图 18 中的实施方式展示了连接器之间的接触力的较少的变化，接触力的变化会产生在远端 1544 相对于表面 1540 的定位中的公差以及在制造连接器的其它结构时的公差。

[0208] 图 14 和图 15 示出具有波浪形部的波幅的波浪形匹配触头，所述波幅相对于包括匹配接触部的腔的宽度足够大，使得插入到腔中的匹配触头将压缩波浪形接触部。图 14 和图 15 中示出的波浪形接触部示出为不具有如结合匹配触头 1110（图 12A）示出的弯曲包迹。但是，图 14 和图 15 中示出的波浪形匹配触头可以替代性地形成有如图 12A 中示出的弯曲包迹。实施方式可以是形成下述区配接触部：单独地或共同地使用弯曲包迹和波浪形接触结构以提供导电元件的匹配接触部，导电元件的匹配接触部通过靠着外壳的腔的侧壁压缩而产生接触力。

[0209] 此外，其它形状的匹配触头可以用于沿匹配触头与在接触顺序期间匹配触头对的相对运动的方向对齐的方向提供多个接触点。图 16 示出构造有根据一些替代性实施方式的匹配接触部的连接器的一部分的截面。在图 16 的实施方式中，匹配接触部成形为沿匹配接触部的细长方向提供多个接触点。在图 16 的实施方式中，接触力也通过朝向包括匹配接触部的外壳的壁压缩匹配接触部的段而产生。如在上述的实施方式中，例如接触部 1320A、1320B 和 1320C 的接触部插入到包括压缩触头 1310A、1310B 和 1310C 的例如 1322A、1322B 和 1322C 的腔中时，可以产生压缩力。

[0210] 图 16 示意性地示出穿过使用这样的触头的连接器的匹配接口的一部分的截面。如示出的，匹配接口定位在前外壳 1630 中，前外壳 1630 包括多个腔，例如 1622A、1622B 和 1622C。多个晶片可以附连到前外壳 1630 以形成连接器模块。此处，示出晶片 1640A、1640B 和 1640C 的一部分。如上文中结合图 2A 和图 2B 所描述的，这种晶片可以通过围绕引线框模制材料而形成。此处，用于形成每个晶片的引线框可以包括一列导电元件，如在结合图 17A... 图 17C 更详细描述的，导电元件中的每一个在一个端部处均具有匹配接触部。

[0211] 出为简单的目的，仅示出了每个均为不同晶片的一部分的三个匹配触头 1610A、1610B 和 1610C。在该示例中，匹配触头 1610A 和匹配触头 1610C 可以与接地导体相关联而匹配触头 1610B 可以与信号导体相关联。但是，每个导电元件均可被指定为携载信号或基准电压电平，以得到具有任何所需要的导电元件的构型的连接器。

[0212] 匹配触头 1610A、1610B 和 1610C 中的每个均为压缩触头，在压缩触头中接触力通过靠着外壳壁压缩匹配接触部的一个或更多个构件产生。这种构型允许例如晶片 1640A、1640B 和 1640C 的晶片以较小的间距间隔开。在一些实施方式中，例如 1340A、1340B 和 1340C 的晶片之间的中心间距可以为大约 1.5 毫米或更小。在一些实施方式中，间距可以为大约 1.35 毫米或在其它实施方式中为 1.3 毫米。例如，对于具有大约 12 毫英寸的壁厚的例如 1132 和 1134（图 11）的壁来说，这样的间距是可行的。距离 D_1 可以处于大约 15 至

30 毫英寸之间。例如，在一些实施方式中，距离 D_1 为大约 25 毫英寸。

[0213] 如在图 16 的示意性示图中可以看到的，当与互补的匹配接触部，例如匹配接触部 1620A...1620C 匹配时，匹配接触部 1610A...1610C 中的每一个均沿匹配接触部的细长尺寸提供多个接触点。因此，图 16 中的构型提供减少滑接区的量的相同的优点，该滑接区对于结合图 12C 在上文中描述的可靠匹配是必须的。

[0214] 图 17A、图 17B 和图 17C 示出匹配触头的一实施方式，该匹配触头提供在上文中结合图 16 示意性地示出的特征。

[0215] 图 17A 示出导电元件 1700 的一部分。在示出的实施方式中，示出了中间部 1700 和匹配接触部 1710。导电元件 1700 可以使用在上文中结合图 4A 和图 4B 中的引线框所描述的材料和技术由金属薄片冲压出并形成。在示出的实施方式中，匹配接触部 1710 宽于中间部 1720。但可以使用任何适合的相对尺寸标准。

[0216] 在提供三个接触点的图 17A 的实施方式中，匹配接触部 1710 冲压有三个段 1732、1734 和 1736 以及大致平面的框架 1740。在该示例中，段 1732、1734 和 1736 中的每个均为具有两个端部的半圆形或弓形，两个端部都连接到框架。如作为导电元件 1700 的立体图的图 17B 所示，段 1732、1734 和 1736 中的每个均可以弯曲到匹配接触部 1710 的平面之外。图 17B 示出段 1732、1734 和 1736 中的每个均向上弯曲角度 α。

[0217] 通过弯曲段 1732、1734 和 1736，多个接触区域形成在匹配接触部 1710 上。每个匹配接触区域均可以在段的最大偏转点处形成在例如段 1732、1734 和 1736 的段上。由于段 1732、1734 和 1736 中的每个均在每个端部处连接到框架 1740，因此最大偏转点也是段中的回折点。

[0218] 每个匹配接触区域均可以成形、涂覆或以其它方式改变以有利于与匹配导电元件中的接触部进行良好的电气接触。在图 17B 的实施方式中，每个匹配接触部均包括凹痕 1712、1714 和 1716。可替代地或另外地，每个匹配接触区域均可以涂覆有金或抗氧化的其它材料。

[0219] 在图 17A 和图 17B 的示例中，接触区域以与在图 11 的实施方式中接触区域与远端部间隔的相同的方式，与匹配接触部的远端部 1742 不同距离地间隔。在图 17A 和图 17B 的实施方式中，接触区域没有示出成共线。但是，应当理解，在一些实施方式中，通过改变段 1732，1734 和 1736 的大小，接触区域可以形成为沿对应于在区配顺序期间匹配接触部的相对运动的方向的线共线。

[0220] 转到图 17C，示出了使用具有如图 17A 和图 17B 中示出的匹配触头的导电元件的电连接器的一部分。图 17C 示出通过连接器的匹配接口的截面，包括具有如图 17A 和图 17B 中示出的匹配接触部的多个导电元件。图 17C 示出两个这样的匹配接触部，匹配接触部 1720A 和 1720B。为简化说明，其它匹配接触部和连接器的其它部分在图 17C 的图示中被省略去。

[0221] 每个匹配接触部利用一部分，在本示例中为框架 1740A，邻近连接器的外壳的壁定位。因此，图 17C 示出邻近腔 1750A 的壁 1732A 的框架 1740A。利用该构型，其中段 1732A 和 1734A 在图 17C 的截面图中可见的段延伸离开腔壁 1732A 进入腔 1750A。来自插入腔 1750A 中的匹配连接器的匹配接触部可以朝向壁 1732A 挤压段 1732A 和 1734A，如以上结合图 16 描述的。压缩力将产生如上所述的接触力，从而提供匹配连接器的导电元件之间的多个接触点。

[0222] 例如腔 1750A 和 1750B 的腔可以成形用于容纳来自匹配连接器的导电元件的匹配接触部，这些匹配接触部如以上结合图 12A、12B、12C 和 13 所示的为大致平面或条片形状。但是，可以使用任何适当的形状。

[0223] 由此描述了本发明的至少一个实施方式的若干方面之后，应当理解，本领域普通技术人员可以容易地想到各种改型、修改和改进。

[0224] 例如，图 18 示出了波浪形匹配接触部的实施方式，其中，仅匹配接触部的一部分压靠置于已匹配的构型中的连接器的壁。如可以看到的，触头 1810 的波浪形部具有以 A_3 表示的波幅。远端部 1852 定位在细长的段 1816 的端部处，细长的段 1816 具有大于波幅 A_3 的长度。

[0225] 这种布置方式形成包括弯曲段的区域，其中回折点形成接触点，以及附接到所述区域中的最远弯曲段的细长的段 1806。尽管细长的段 1816 相对于匹配触头 1810 的细长的尺寸形成角度，但细长的段 1816 沿垂直于匹配触头 1810 的细长的尺寸的方向上具有其长度的分量，所述长度分量超过弯曲段的最大波幅 A_3。

[0226] 在该示例中，匹配触头 1810 的远端部 1852 沿朝向壁 1832 的方向延伸得比回折点 1818A 和 1818B 更远。因此，在示出的实施方式中，远端部 1852 与作为壁 1832 的一部分的支承部 1833 接触。此外，壁成形成仅在一个方向（在本示例中垂直于壁）限制运动，同时允许远端部 1852 沿着壁在连接器的匹配方向上滑动。

[0227] 在该实施方式中，即使当匹配触头 1820 完全插入腔 1822 中时，回折点 1818A 和 1818B 也不接触壁 1832。这种构型可以提供连接器之间的接触力方面的较小变化。但是，由于靠着壁 1832 压缩匹配触头 1810 而产生的力通过细长的段 1816 从远端部 1852 传递到接触点 1812A、1812B 和 1812C，因此仍然可以提供多个可靠的接触点。

[0228] 图 18 示出已匹配的构型。尽管未示出，但当未匹配时，远端部 1852 可以触碰壁 1832，或者在一些实施方式中，在匹配过程中可以从壁 1832 分离并压入壁中。

[0229] 图 18 的触头形状可以与上述其它结构一起使用。例如，在未匹配的构型中，匹配触头 1810 可以具有大致如图 12A 中示出的曲率，其引起远端 1852 与壁 1832 间隔开。但是，在一些实施方式中，即使在匹配触头 1810 不压靠壁 1832 的非匹配构型中，匹配触头 1810 也可以具有使远端 1852 接触壁 1832 的足够的曲率。

[0230] 而且，尽管在图 18 中未示出，但腔 1822 可以具有开口，所述开口成形用于将匹配触头 1820 引导到用于匹配的位置中，或防止远端部 1852 卡夹。此外，在图 18 的实施方式中，远端 1852 不被限制，并且随着匹配触头 1820 插入到腔 1822 中以使匹配触头 1810 压靠壁 1832 而可以沿壁 1832 滑动。在其它实施方式中，匹配触头 1810 可以与外壳一起使用，外壳具有类似于突起壁部 1540 的边缘，其限制远端 1852 的移动范围。

[0231] 图 18 示出，形成在具有回折点的段上的接触点中的每一个不必具有相同的形状。同样，不需要每个接触点产生相同的接触力。在示出的实施方式中，接触点 1812A 和 1812B 中的每个均产生约 40-60 克的接触力。相反地，接触点 1812C 可以设计成大约为这个值的一半，提供大约 20-30gm 的接触力。

[0232] 图 19A 和图 19B 示出波浪形触头的另一实施方式。在该示例中，匹配触头 1910 成形为具有两个波峰的波浪形。波峰形成接触点 1912A 和 1912B。尽管在该构型中示出两个波峰，但应当理解，匹配触头可以形成具有任何适合数量的波峰的“波浪形”构型。

[0233] 在图 19A 的实施方式中，匹配触头 1910 具有延伸的远部 1952，远部 1952 定位用于接触外壳的壁的一部分，匹配触头 1910 可以支承在外壳中。在图 19B 的截面中，远部 1952 示出为接触支承部 1833，支承部 1833 可以是例如壁 1832（图 18）的绝缘壁的一部分。

[0234] 图 20A 和 20B 示出可以在连接器中使用的匹配触头的又一变型。图 20A 示出匹配触头 2010。在该示例中，匹配触头 2010 为分叉触头，包括部分 2020_1 和 2020_2。两个部分 2020_1 和 2020_2 可以由相同的金属件冲压出和形成。在这种情况下，部分 2020_1 和 2020_2 中的每个均为大致相同的尺寸和形状。但是，不是必须两个部分都相同或匹配触头 2010 是对称的。

[0235] 在图 20A 中示出的实施方式中，部分 2020_1 和 2020_2 中的每个成形为具有两个波峰的波浪形，从而提供总共四个接触点 $2012A_1$ 和 $2012A_2$、$2012B_1$ 和 $2012B_2$。图 20B 为匹配触头 2010 的俯视图，示出接触点的相对设置方式。

[0236] 与图 19B 中示出的实施方式相反，匹配触头 2010 被示出不带有远部匹配支承 1833 或绝缘侧壁 1832 的其它部分。而是，匹配触头 2010 的远端 2052 以悬臂的构型示出为可自由浮动。应当理解，具有任何适当形状的匹配触头可以采用有多个回折点，或仅适于接触连接器外壳的绝缘壁的远端。可替代地，匹配触头可以在悬臂的构型中使用。在悬臂的构型中，通过偏转匹配触头产生的弹力可以在匹配的连接器的匹配接触部之间提供适合的接触力。

[0237] 至于其它可能的变化，描述了用于改型电连接器的特性的技术的示例。这些技术可以单独地使用或在任何适合的结合中使用。

[0238] 作为另一示例，图 12C 示出所提供的匹配触头提供单个凸轮面 1250 的示例。但是，应当理解，根据构成接触的段的相对尺寸和位置，在匹配顺序过程中可以接合多个凸轮面。

[0239] 此外，尽管参照子卡连接器示出和描述了发明的许多方面，但应当理解，本发明在这些方面不受限制，如发明性概念可以包括在其它类型的电连接器中，例如底板连接器，电缆连接器，堆栈连接器、夹层连接器或芯片插座。

[0240] 作为可能的变化的另一示例，描述了在列中具有四个差分信号对的连接器。但是，可以使用具有任何所需数量的信号导体的连接器。

[0241] 本发明在其应用中不被限到构造的细节和在上述说明中阐述的或在附图中示出的部件的布置。本发明能够具有其它实施方式并能够以各种方式实践或实施。而且，此处所使用的措词和术语是为了描述的目的而不应当认为是限定。本文中所使用的“包括”、“包含”、“具有”或“含有”以及它们的改型，意在包含它们后面所列的项目和其等同替代以及另外的项目。

[0242] 这种改变、修改、和改进旨在作为本公开的一部分，并且落入本发明的精神和范围之内。因此，前述的说明和附图仅是示例。

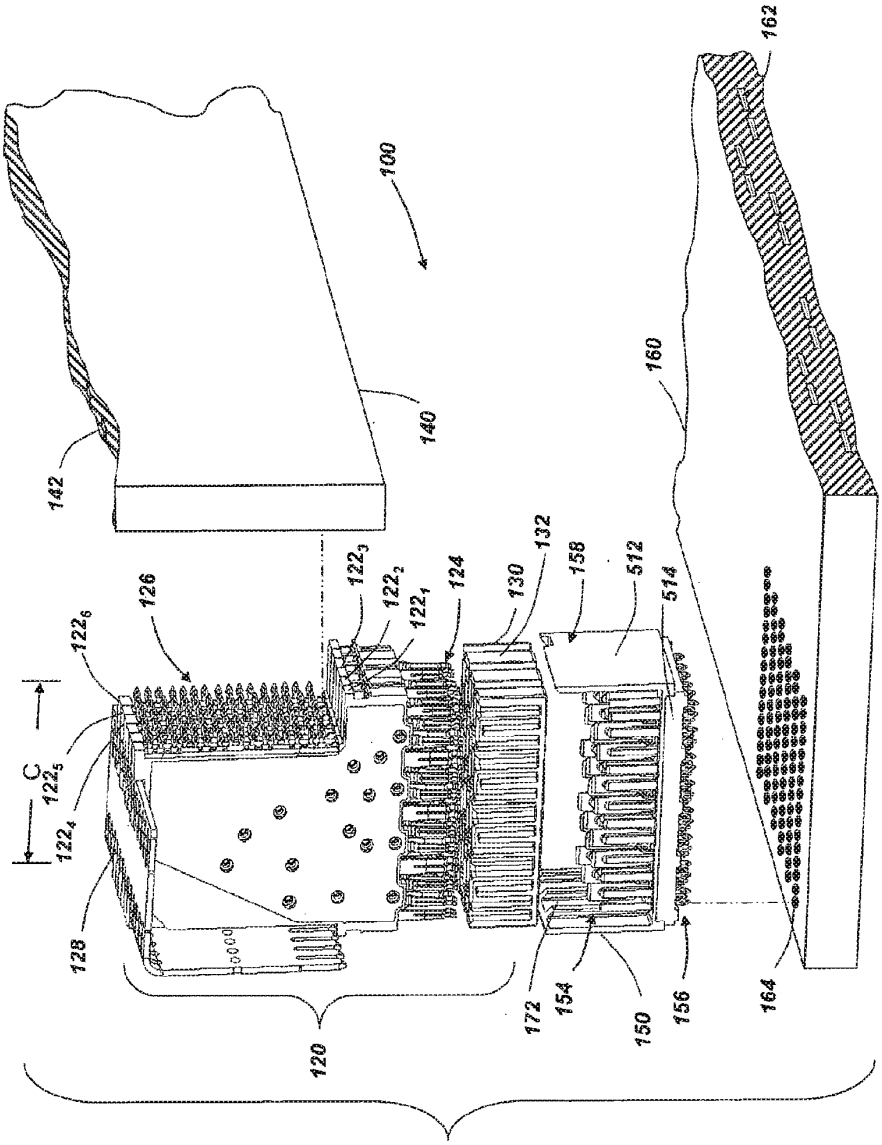


图 1

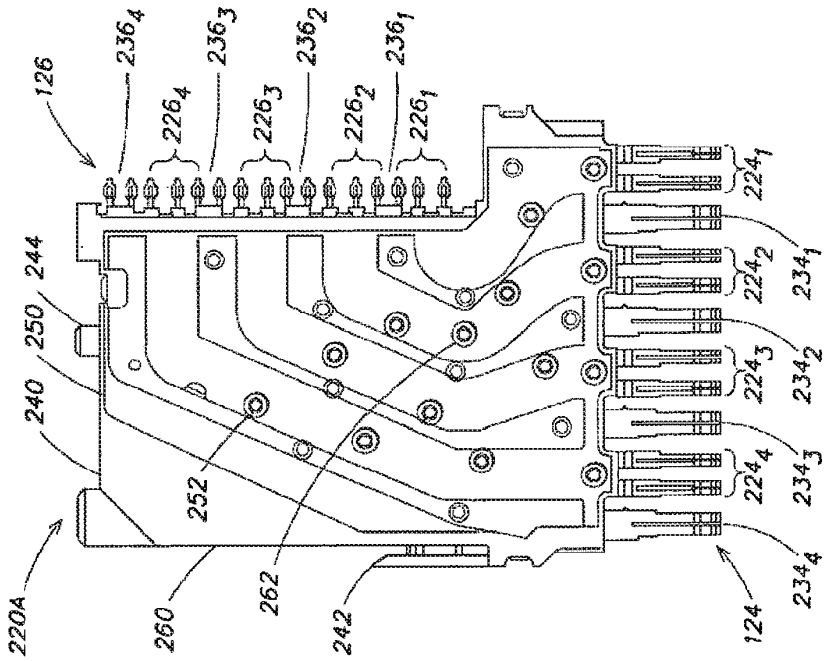


图 2A

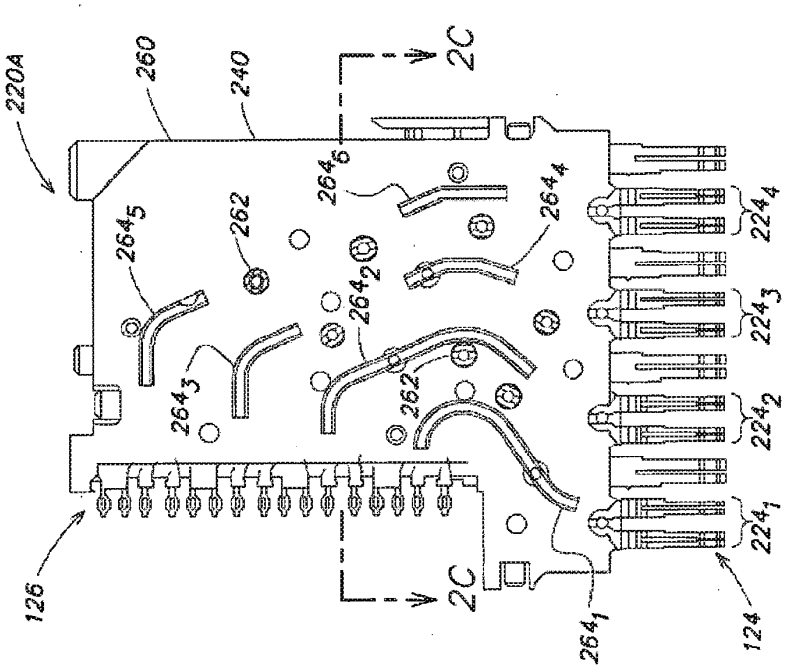


图 2B

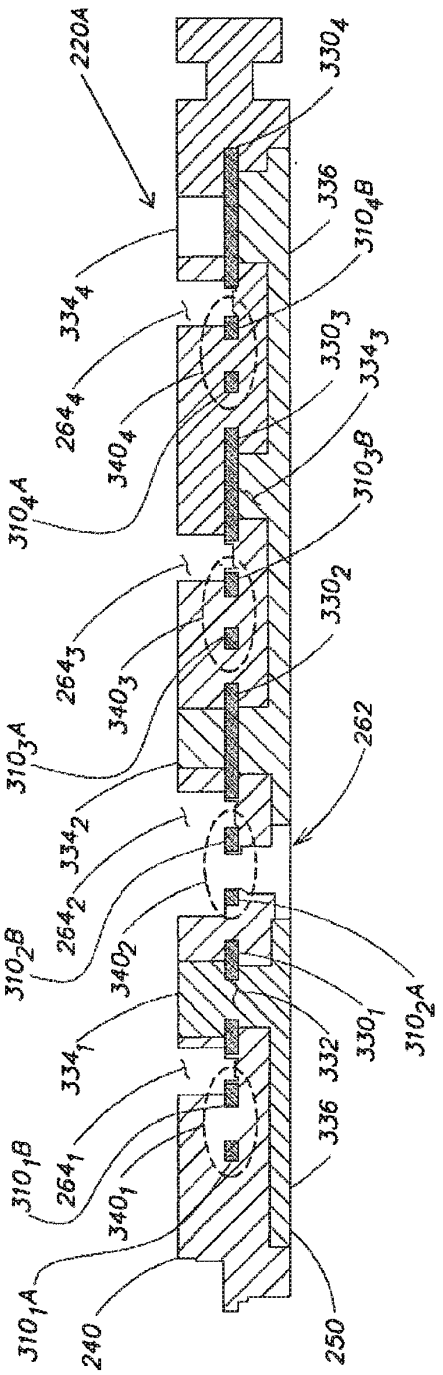


图 2C

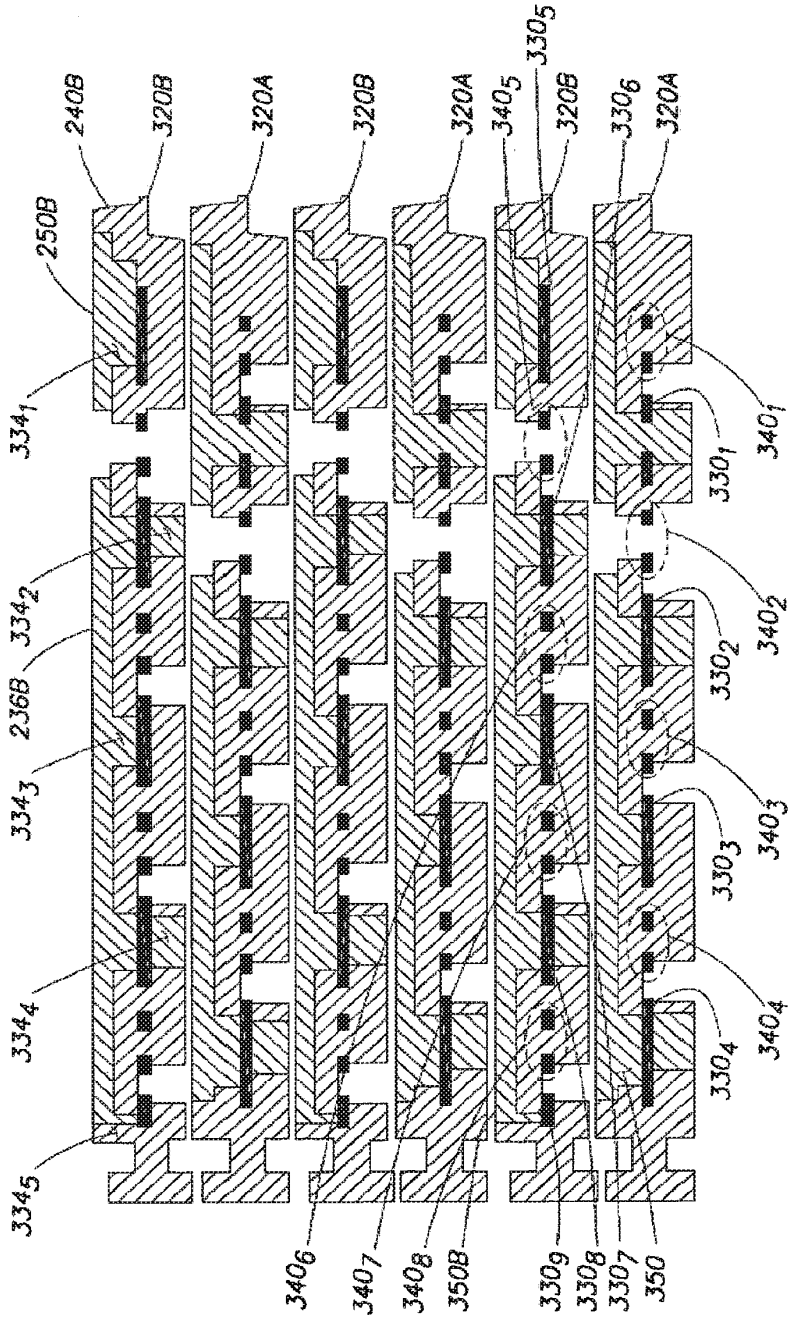


图 3

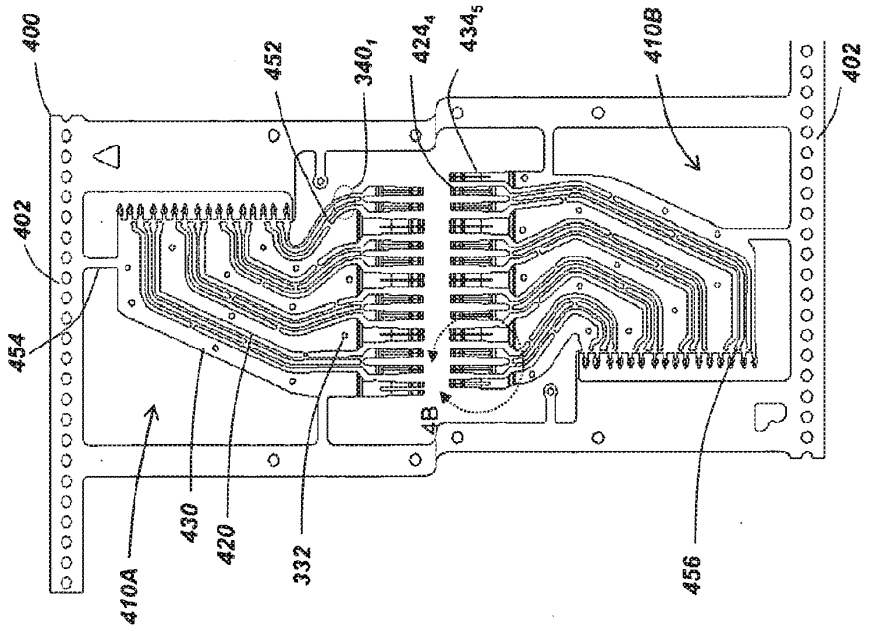


图 4A

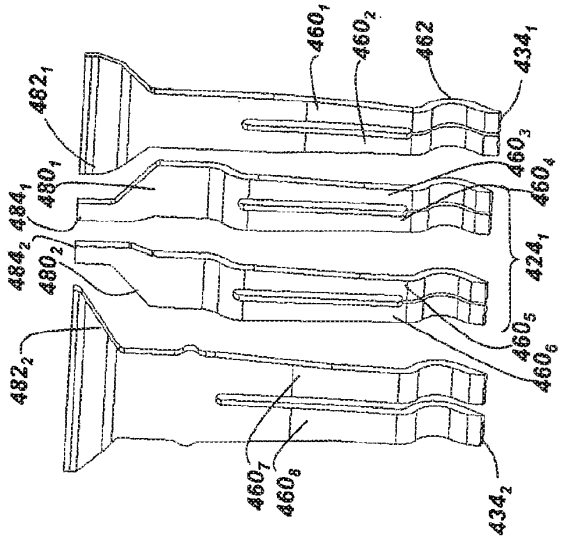


图 4B

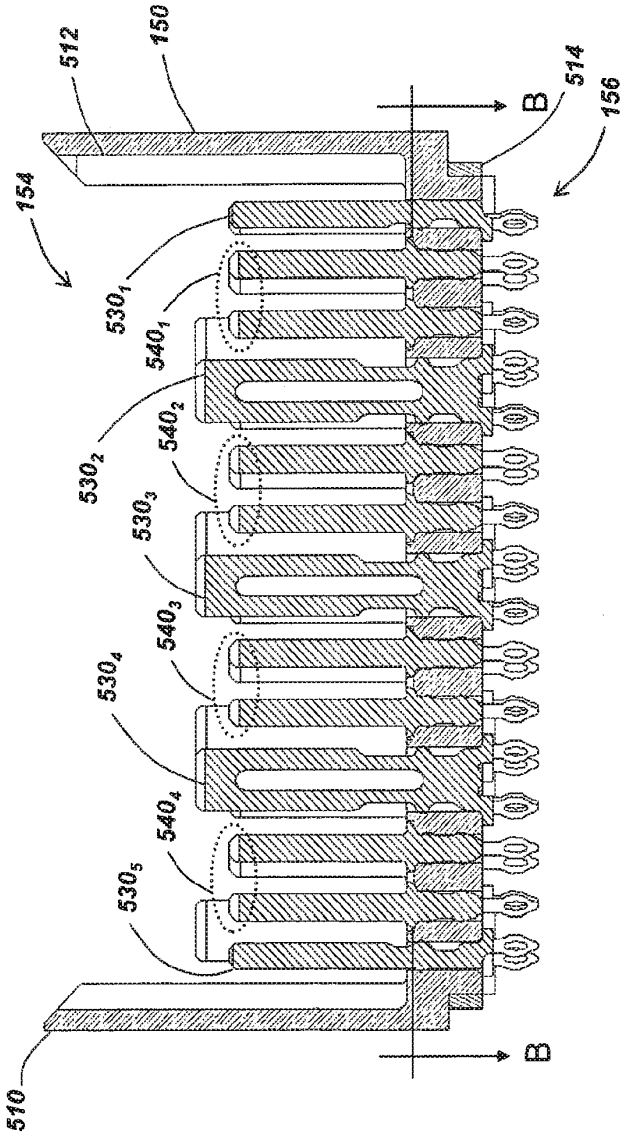


图 5A

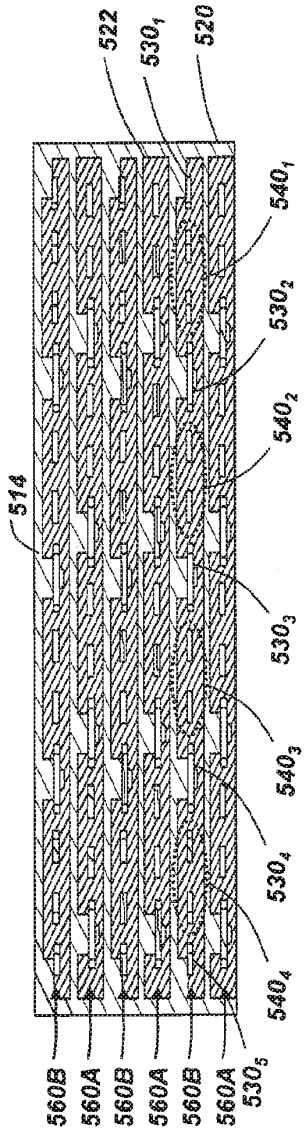


图 5B

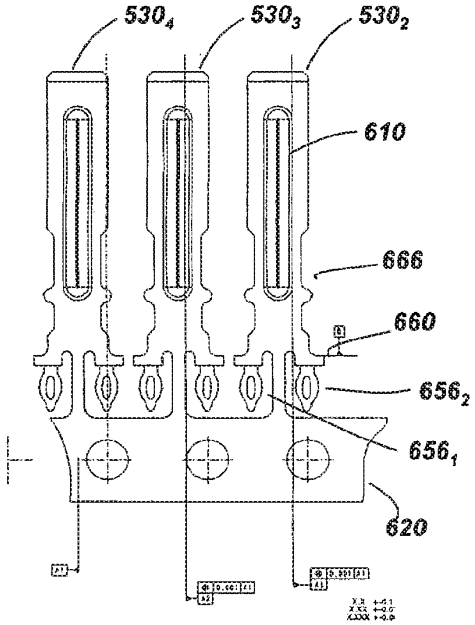


图 6A

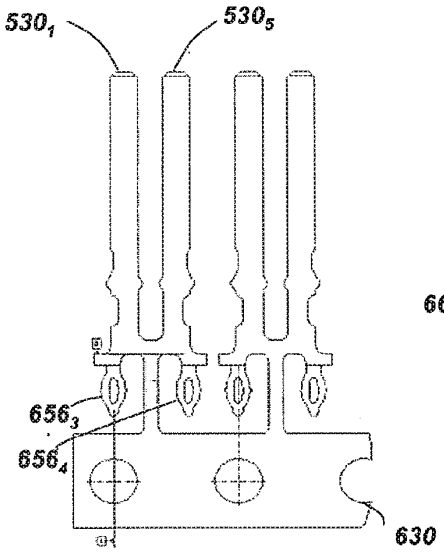


图 6B

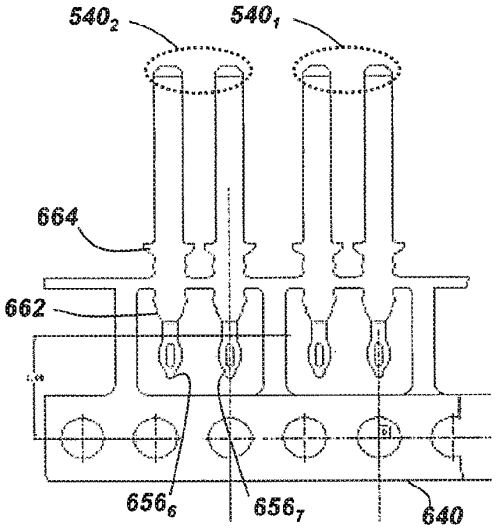


图 6C

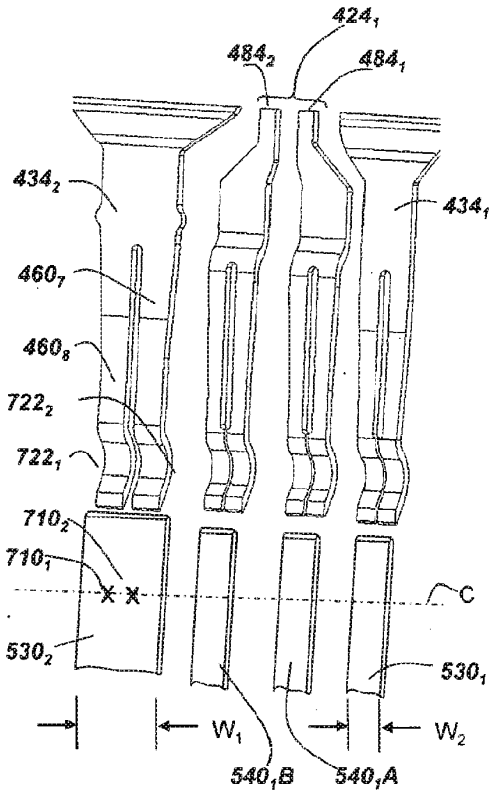


图 7A

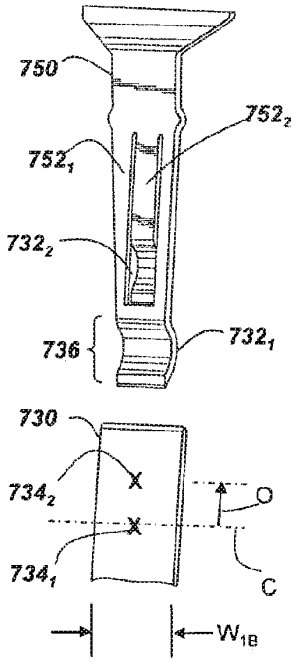


图 7B

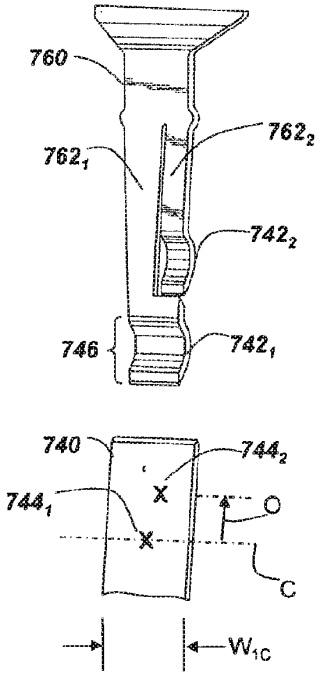


图 7C

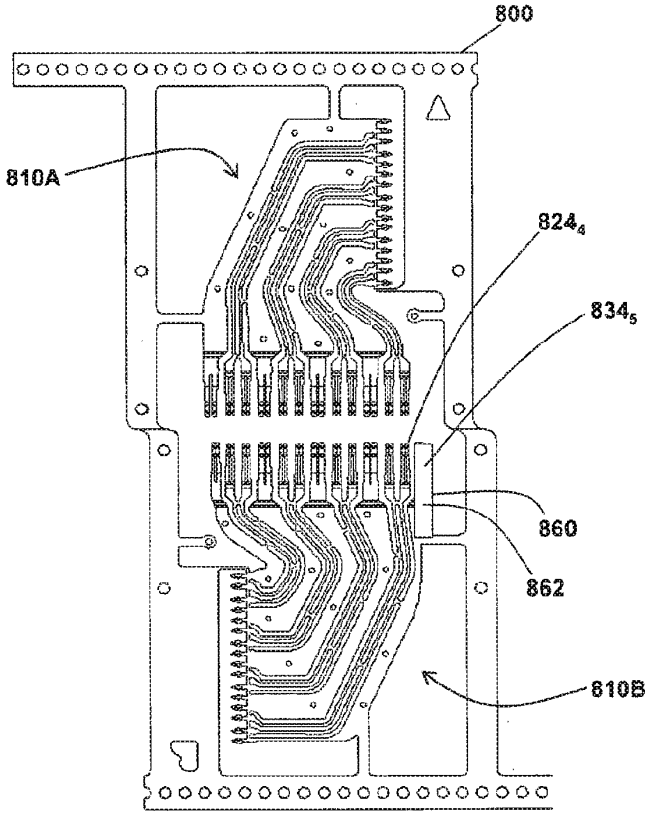


图 8A

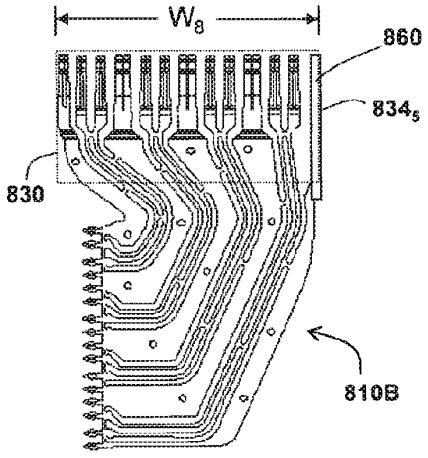


图 8B

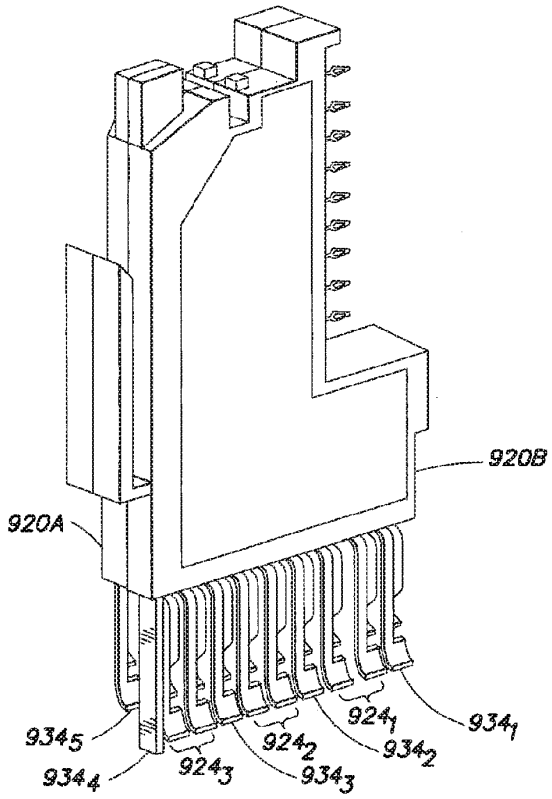


图 9A

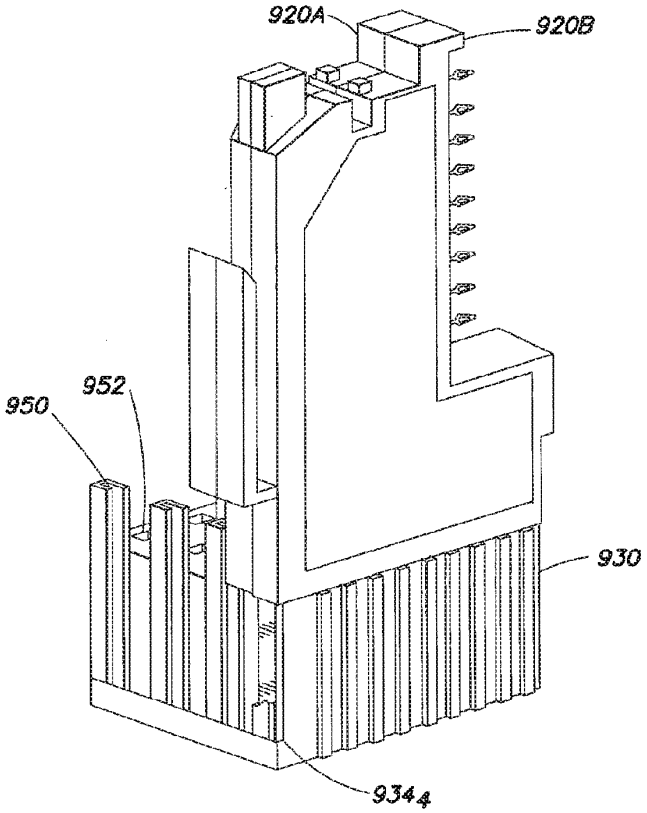


图 9B

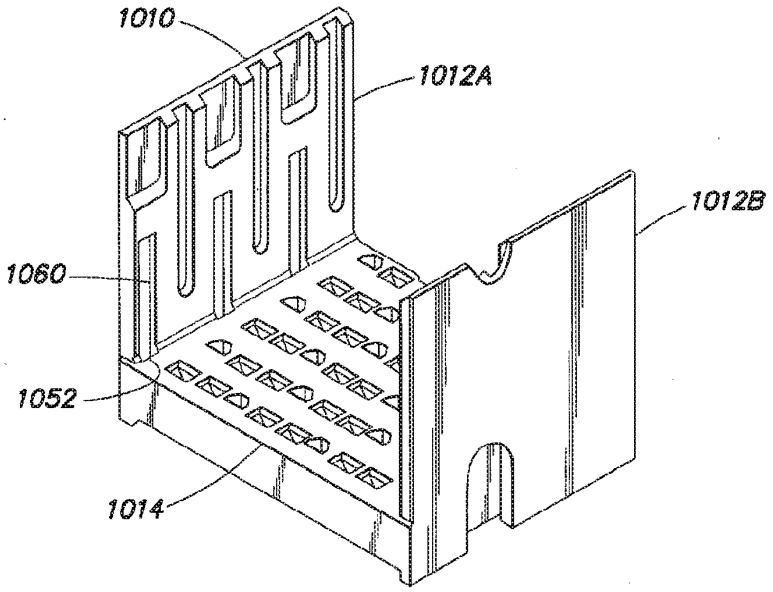


图 10A

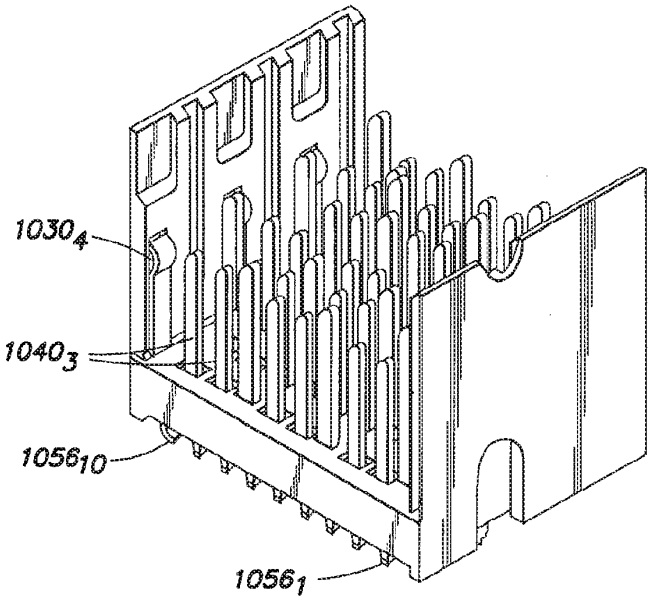


图 10B

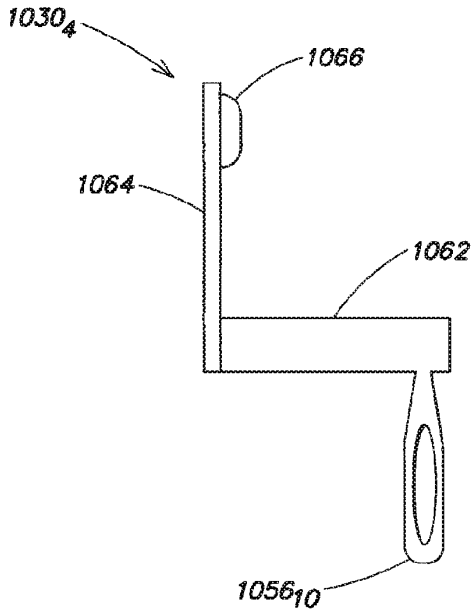


图 10C

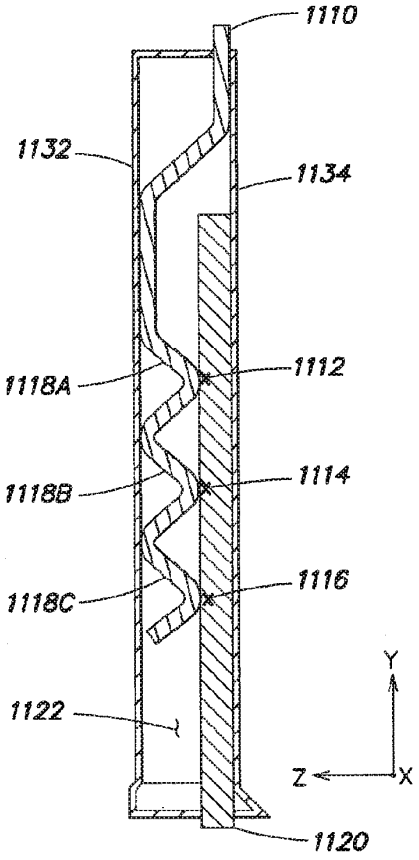


图 11

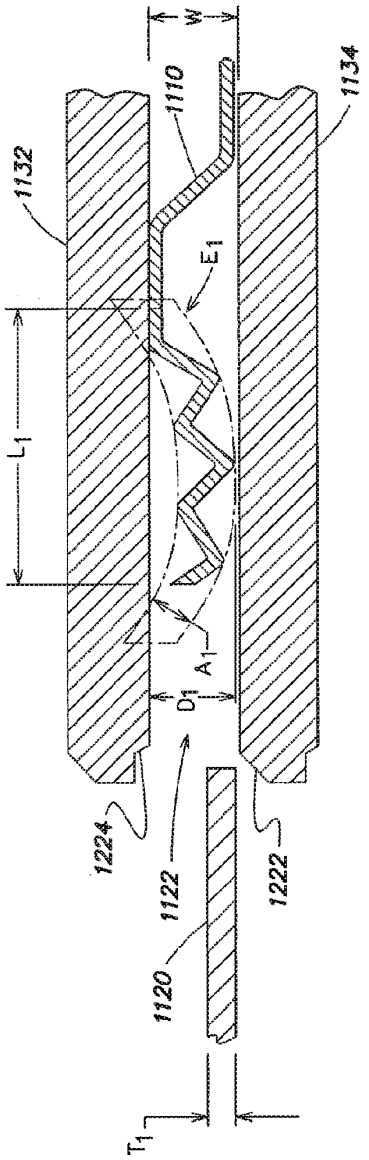


图 12A

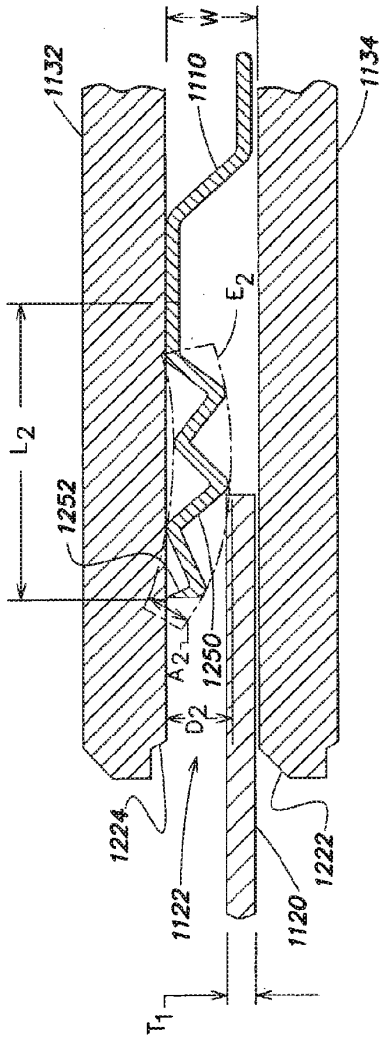


图 12B

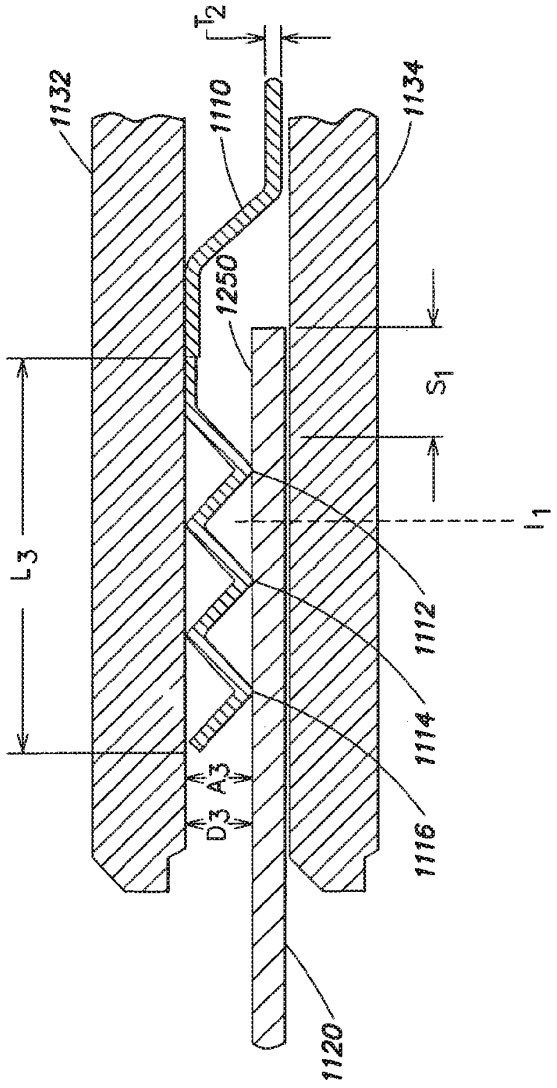


图 12C

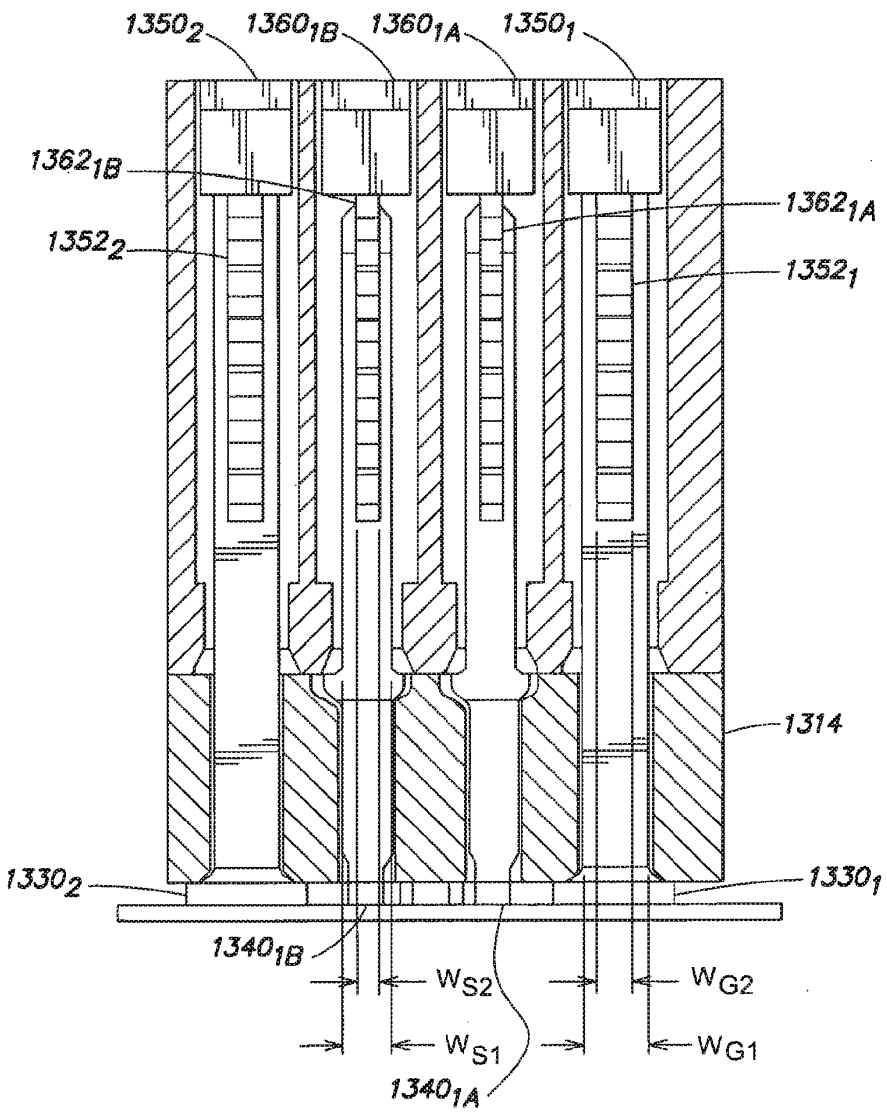


图 13

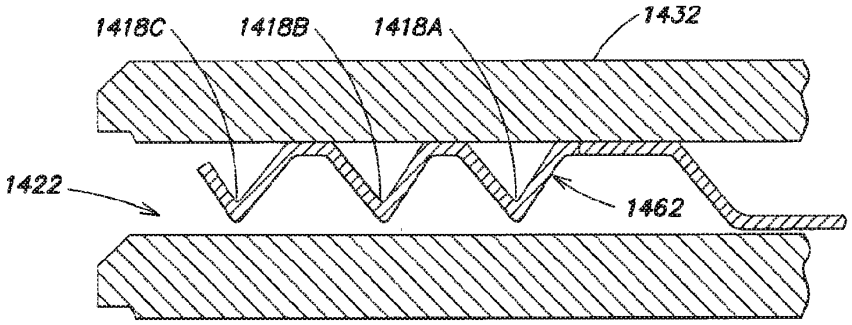


图 14

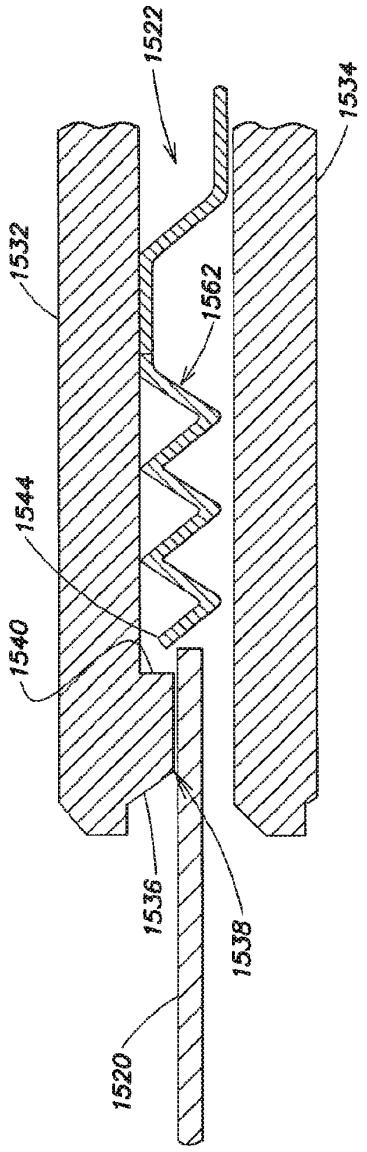


图 15

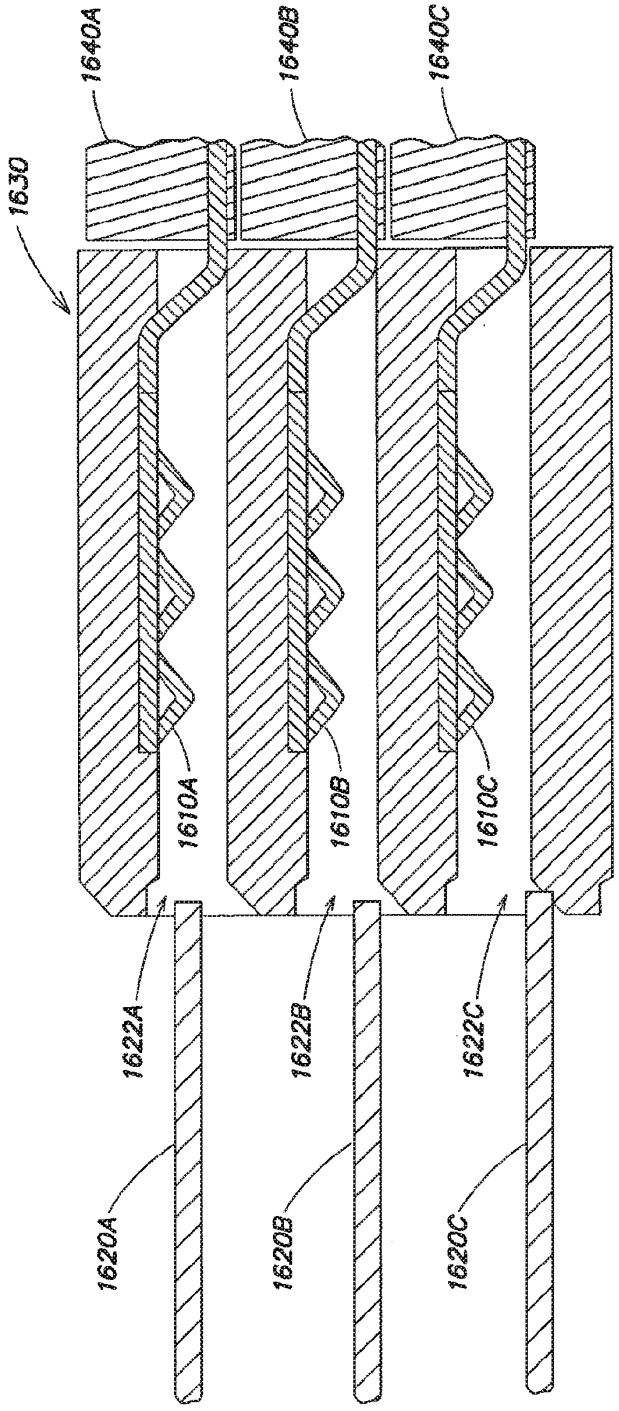


图 16

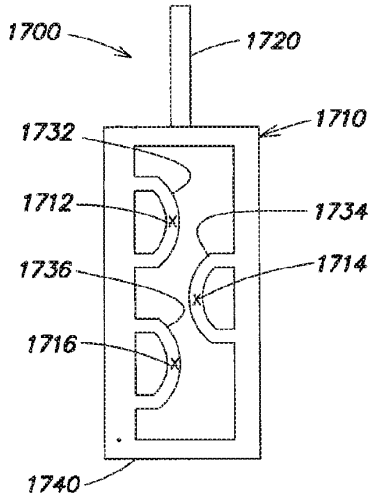


图 17A

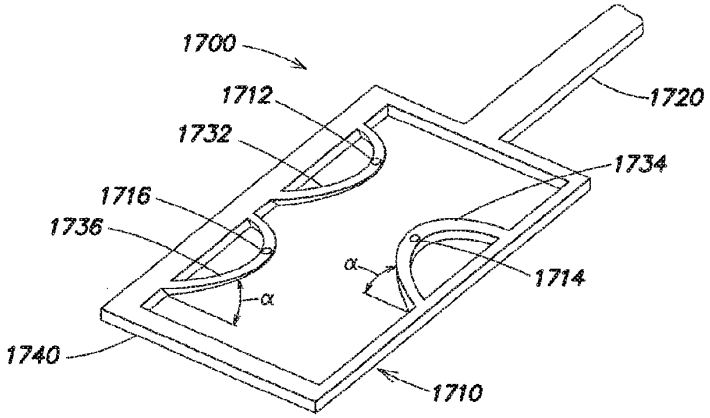


图 17B

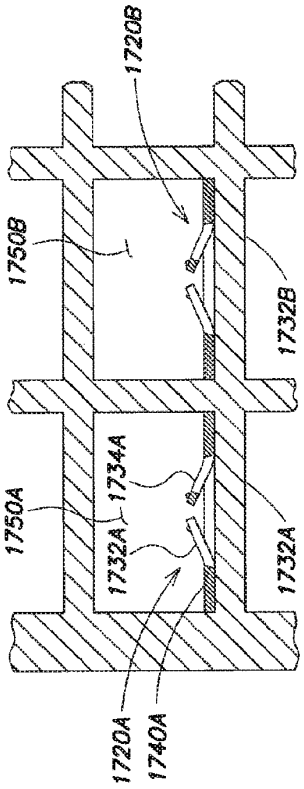


图 17C

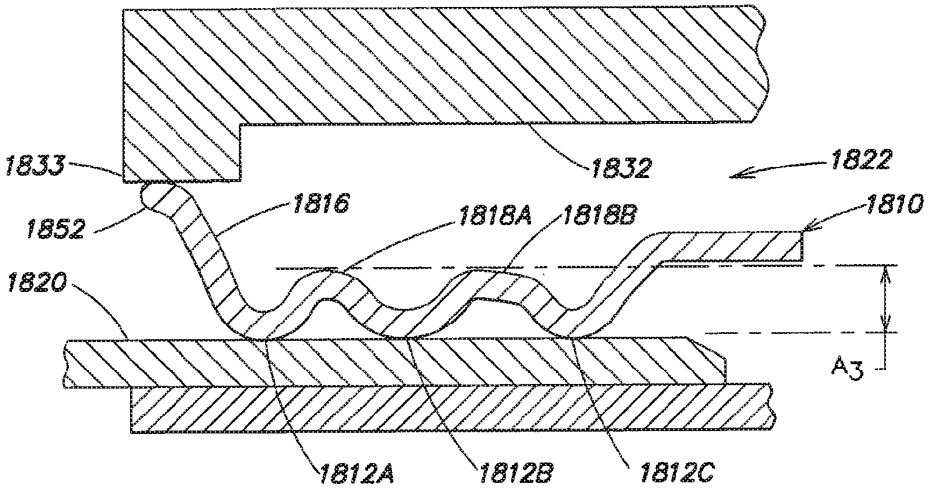


图 18

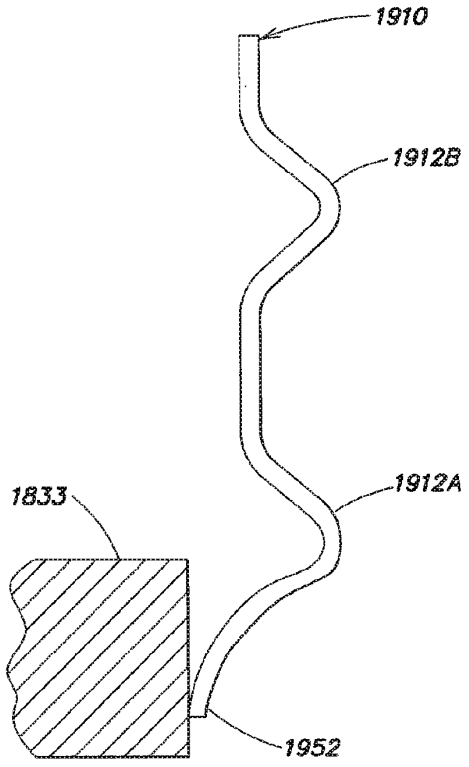


图 19A

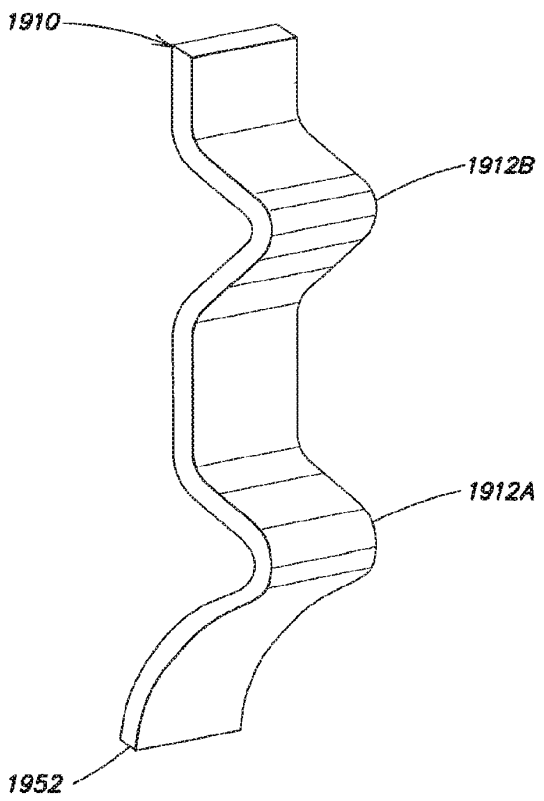


图 19A

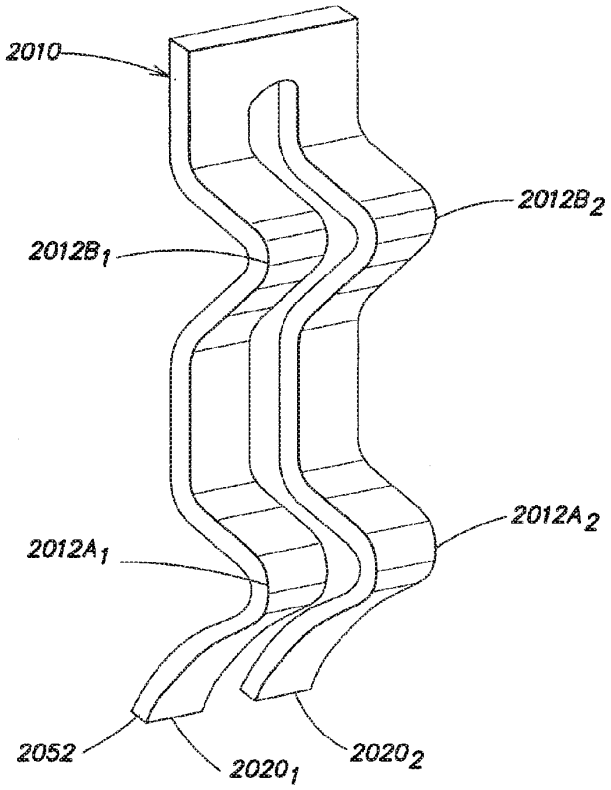


图 20A

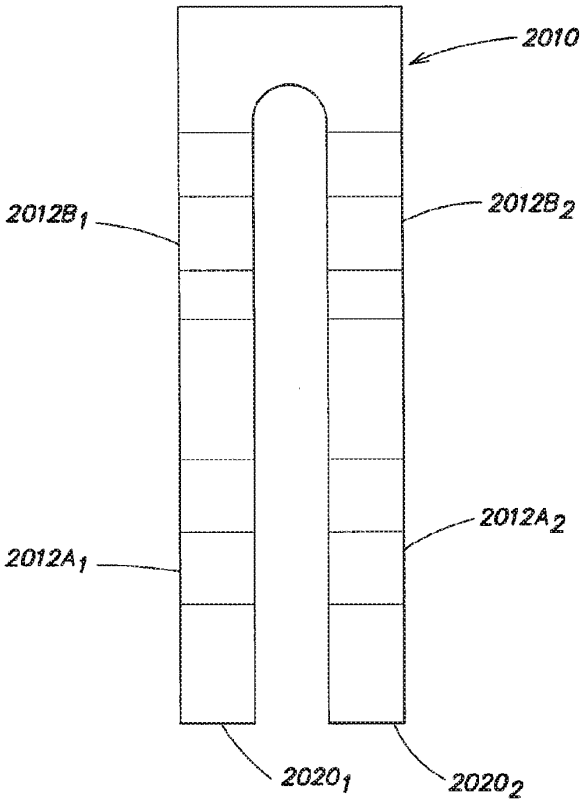


图 20B

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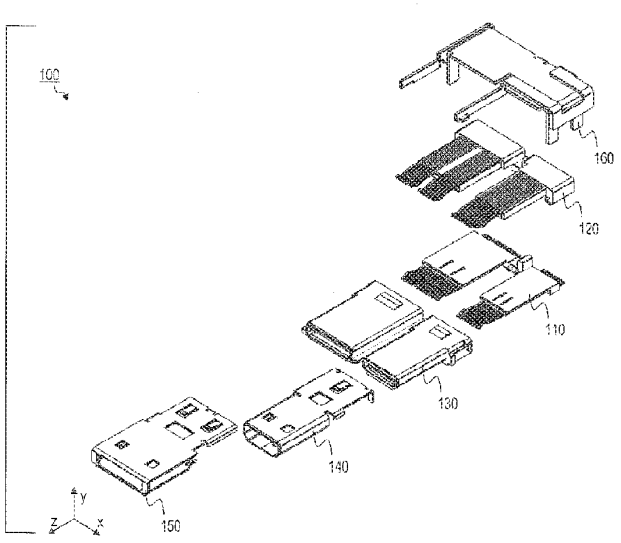
(54) Surface mount multi-connector and electronic apparatus having the same

(57) A surface mount multi-connector having movable contact sections with high contact reliability and providing connection portions with high coplanarity. The surface mount multi-connector includes a first body in which a plurality of first contacts having movable contact sections and end sections that extend oppositely to each other are held by insert molding, a second body in which a plurality of second contacts having movable contact sections and end sections that extend oppositely to each other are held by insert molding, and a third body that incorporates the first body with which the second body has been coupled so that the movable contact sections of the second contacts and the movable contacts section of the first contacts face in the same direction. Tips ahead of the movable contact sections of the first and second contacts elastically mate with catching parts formed on the inner wall of the third body, and connection portions of the end sections of the first contacts and connection portions of the end sections of the second contacts lie in a same plane.

FIG. 4



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Description

TECHNICAL FIELD

[0001] The present invention relates to a surface mount multi-connector connected electrically and an electronic apparatus having a surface mount multi-connector.

BACKGROUND ART

[0002] Japanese Patent Application Laid Open No. 2004-537836 discloses the prior-art one-surface mount multi-connector 10. The creation method and structure of one-surface mount multi-connector 10 disclosed in this patent literature will be described with reference to Fig. 1.

[0003] First, a plurality of first contacts 12 and a plurality of second contacts 22 are formed by punching a metal plate 90. Next, the plurality of first contacts 12 and the plurality of second contacts 22 are placed in a cavity, and then molten plastic etc. is injected into the cavity. The plurality of first contacts 12 and the plurality of second contacts 22 are covered with molted plastic, and the molted plastic is solidified into a desired shape to insert-mold a first body 11 having the plurality of first contacts 12 and a second body 21 having the plurality of second contacts 22.

[0004] The first body 11 and the second body 21 are disconnected from the metal plate 90. A concave portion 11a of the first body 11 and a projection (not shown) of the second body 21 mate with each other to form a body assembly 31. Next, a cover 51 is attached to a body cantilever part 34 of the body assembly 31 to form a connector semi-fabricated body 52. The connector semi-fabricated body 52 is inserted into the mold and a connector housing main body 61 is molded so as to cover part of the first body 11, the second body 21, the cover 51, the first contacts 12 and the second contacts 22. As shown in Fig. 1, the connector housing main body 61 extends downward to the lower end of the connection portions of the first contacts 12 and the second contacts 22. Finally, a cover 71 is attached. The cover 71 is partially supported by the connector housing main body 61 and encloses both the connector housing main body 61 and an inner cover 51.

[0005] This structure allows the connection portions of the first contacts 12 and the second contacts 22 to be placed on the same plane.

SUMMARY OF THE INVENTION

[0006] Since the prior art uses insert molding to secure the first contacts 12 and the second contacts 22 to the first body 11 and the second body 21, respectively, it is difficult to flexibly respond to the size of the corresponding connector, possibly causing loose connection etc.

[0007] To prevent such loose connection etc., preload needs to be applied to the first contacts 12 and the second contacts 22 when the first contacts 12 and the second contacts 22 are of movable type. However, because the first body 11 and the second body 21 are created by insert molding, it is difficult to use these bodies to apply preload to the first contacts 12 and the second contacts 22.

[0008] Alternatively, in a method of inserting contacts into a molded body using press-fitting instead of insert molding, it is difficult to maintain the coplanarity (uniformity and planarity of the lowest surface of components or pins with respect to the mounting surface) of the connection portions with respect to the printed circuit board.

[0009] For these reasons, it is difficult to use two bodies to achieve a compact narrow-pitch connector with two rows of contacts while keeping the connection portions of movable contacts on the same plane.

[0010] An object of the present invention is to provide a surface mount multi-connector that has movable contact sections with high contact reliability and provides high coplanarity for the connection portions.

[0011] To address the problems described above, a surface mount multi-connector according to an embodiment of the present invention has a first body in which a plurality of first contacts having movable contact sections and end sections that extend oppositely to each other are held by insert molding, a second body in which a plurality of second contacts having movable contact sections and end sections that extend oppositely to each other are held by insert molding, and a third body that incorporates the first body with which the second body has been coupled so that the movable contact sections of the second contacts and the movable contact sections of the first contacts face in the same direction, in which tips ahead of the movable contact sections of the first contacts and tips ahead of the movable contact sections of the second contacts elastically mate with catching parts formed on an inner wall of the third body, and connection portions of the end sections of the first contacts and connection portions of the end sections of the second contacts lie in a same plane.

EFFECTS OF THE INVENTION

[0012] The present invention has the effect of providing the movable contact sections with high contact reliability and the connection portions with high coplanarity.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013]

Fig. 1 shows the creation method and structure of a conventional surface mount multi-connector;

Fig. 2 is a perspective view showing the front side, right side, and top face of a surface mount multi-connector 100;

Fig. 3 is a perspective view showing the back side, left side, and bottom face of the surface mount multi-connector 100;

Fig. 4 is an exploded perspective view showing the front side, right side, and top face of the surface mount multi-connector 100;
Fig. 5 is a perspective view showing the front sides, right sides, and top faces of a first body and first contacts;
Fig. 6 is a perspective view showing the front sides, right sides, and bottom faces of a second body and second contacts;
Fig. 7 is a perspective view showing the front side, right side, and top face of the first body with which the second body has been coupled;
Fig. 8 is a perspective view showing the back side, left side, and top face of a third body;
Fig. 9 is a bottom view of the surface mount multi-connector 100;
Fig. 10 is a perspective view showing the cross section p-p' in Fig. 9;
Fig. 11 is an enlarged view of the part enclosed by the dotted line in Fig. 10;
Fig. 12 is a view showing the state where tips mate with catching parts;
Fig. 13 is a view describing the method of mating the tips with the catching parts;
Fig. 14 is a right side view of the surface mount multi-connector 100;
Fig. 15 is a right side view of the surface mount multi-connector 100 when a third cover and the second body in Fig. 14 are assumed to be transparent;
Fig. 16 is a front view of the cross section q-q' in Fig. 9;
Fig. 17 is a perspective view showing the front side, right side, and top face of a first cover;
Fig. 18 is a perspective view showing the front side, right side, and bottom face of a second cover;
Fig. 19 is a left side view of the cross section r-r' in Fig. 9;
Fig. 20 is a perspective view showing the back side, left side, and bottom face of the third cover; and
Fig. 21 is a perspective view showing the surface mount multi-connector 100 mounted on a printed circuit board.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0014] Embodiments of the present invention will be described in detail below.

Surface mount multi-connector 100

[0015] A surface mount multi-connector 100 will be described with reference to Figs. 2, 3, and 4. In the surface mount multi-connector 100, the side facing a printed circuit board is assumed to be the bottom surface and the side into which the corresponding connector is inserted is assumed to be the front side.

[0016] The surface mount multi-connector 100 includes a first body 110, a second body 120, a third body 130, a first cover 140, a second cover 150, and a third cover 160.

[0017] A plurality of the first contacts 112 are arranged in the first body 110 made of synthetic resin such as polyethylene (PE), polypropylene (PP), polyvinylchloride (PVC), etc. and held by insert molding. In the example shown in Fig. 5, the first body 110 is substantially rectangular plate shaped. The movable contact sections 112a at one end of the first contacts 112 and the end sections 112b at the other end extend oppositely to each other from the first body 110.

[0018] Similarly, a plurality of the second contacts 122 are arranged in the second body 120 made of synthetic resin such as polyethylene (PE), polypropylene (PP), polyvinylchloride (PVC), etc. and held by insert molding. In the example shown in Fig. 6 (perspective view seen from the bottom), the second body 120 is substantially rectangular plate shaped. The movable contact sections 122a at one end of the second contacts 122 and the end sections 122b at the other end extend oppositely each other from the second body 120.

[0019] The third body 130 is formed as a molded component made of synthetic resin such as polyethylene (PE), polypropylene (PP), polyvinylchloride (PVC), etc. As shown in Fig. 7, the second body 120 is coupled with the first body 110 so that the movable contact sections 112a of the first contacts 112 and the movable contact sections 122a of the second contacts 122 face in the same direction (toward the front side). In other words, the second body 120 is put on the first body 110. The first body 110 with which the second body 120 is coupled is inserted and incorporated into the third body 130 shown in Fig. 8 (perspective view seen from the back side), which is hollow rectangular parallelepiped-shaped.

About preload

[0020] Fig. 9 is a bottom view of the surface mount multi-connector 100; Fig. 10 is a perspective view showing the cross section p-p' in Fig. 9; Fig. 11 is an enlarged view of the part enclosed by the dotted line in Fig. 10; Fig. 12 shows the state where the tips mate with catching parts. When the first body 110 and the second body 120 are inserted into the third body 130, the tips 112c and 122c ahead of the movable contact sections 112a and 122a of the first body 110 and the second body 120 mate with catching parts 130a and 130b formed on the inner wall of the third body 130, respectively. This structure gives preload to each of the movable contact sections 112a and 122a of the contacts 112 and 122.

[0021] One end of the first contact 112 and one end of the second contact 122 are bent toward the connection interface between the first body 110 and the second body 120 to form the movable contact parts 112a and 122a (see Fig. 7). The first body 110 and the second body 120 are inserted, from the side of the movable contact sections 112a and 122a, into opening 130d in the surface (back side) opposite to the an insertion opening 130c

(see Fig. 2) of the hollow rectangular parallelepiped-shaped third body 130 (see Figs. 4, 7, and 8). The corresponding connector is inserted into the insertion opening 130c (see Fig. 2). Grooves 130e and 130f are formed in the inner surface of the third body 130. The inner surface faces the surfaces of the first body 110 and the second body 120. The Grooves 130e and 130f are formed so as to face the first contacts 112 and the second contacts 122, respectively. The ends of the grooves 130e and 130f on the side of the insertion opening 130c are covered with the parts present on the same surface as the inner surface of the third body 130. The cover parts are the catching parts 130a and 130b (see Figs. 11 and 12).

[0022] When the movable contact sections 112a and 122a are not loaded, the tips 112c and 122c are located inside the catching parts 130a and 130b as shown by the chain double-dashed lines in Fig. 13. Before the first body 110 and the second body 120 are inserted into the third body 130, a jig 94 is inserted into the insertion opening 130c. The jig 94 mates with the movable contact sections 112a and 122a, and lets the movable contact sections 112a and 122a elastically deform outward, as indicated by the dashed lines in Fig. 13. After the first body 110 and the second body 120 are inserted, the jig 94 is removed from the insertion opening 130c. The tip 112c of each of the first contacts 112 and the tip 122c of each of the second contacts 122 are press-fit and elastically mate with the catching parts 130a and 130b, respectively, as shown by the solid lines in Fig. 13. That is, preload is applied to each of the movable contact sections 112a and 122a of the first contacts 112 and the second contacts 122. The preload may be increased by slightly bending middle parts near the movable contact sections 112a and 122a toward the connection interface between the first body 110 and the second body 120 at bending points 112e and 122e in the first contacts 112 and the second contacts 122, respectively.

About coplanarity

[0023] A surface 96 (referred to below as the mounting surface 96) of the surface mount multi-connector 100 faces the printed circuit board during mounting. The mounting surface 96 is parallel to the surface of the first body 110 opposite to the second body 120 and is out of contact with the first body 110, in this example. Fig. 14 is the right side view of the surface mount multi-connector 100; Fig. 15 is a right side view of the surface mount multi-connector 100 when the third cover 160 and the second body 120 in Fig. 14 are assumed to be transparent.

[0024] The end sections 112b of the first contacts 112 and the end sections 122b of the second contacts 122 are bent toward the mounting surface 96 at the back side of the first body 110 and the second body 120, respectively, and then bent backward on the mounting surface 96 to form connection parts 112d and 122d. At this time, the connection parts 112d and 122d are present on the same surface (the mounting surface 96). As shown in Fig. 9, the first contacts 112 and the second contacts 122 are displaced in the right and left direction seen from the direction (y-axis direction) in which the second body 120 is coupled with the first body 110. In addition, the positions of the connection parts 112d and 122d on the mounting surface 96 are displaced in the back and forth direction.

[0025] When, for example, the first contacts 112 and the second contacts 122 are formed by punching a metal plate, the coplanarity of the connection parts 112d and 122d with respect to the mounting surface 96 can be improved.

Details of the first body 110

[0026] In this example, there is a thick section 110b on the surface facing the mounting surface 96 at the end of the first body 110 from which the end sections 112b extend (see Fig. 5). Although not shown in the drawing, the first contacts 112 are insert-molded so that one surface of each of the first contacts 112 is exposed on the same surface as the surface of each of plate sections 110A and 110B of the first body 110 facing the mounting surface 96.

[0027] In this example, a plurality of projections 110c are arranged in the direction in which the first contacts 112 are arranged, on the front side (surface facing the insertion opening for the corresponding connector) of the thick section 110b of the first body 110.

Details of the second body 120

[0028] On the other hand, there is a thick section 120b on the surface opposite to the mounting surface 96 at the end of the second body 120 from which the end sections 122b extend (see Figs. 6 and 7). Side walls 120c are formed integrally with the second body 120 on both sides of the thick section 120b in the direction in which the second contacts 122 are arranged so as to extend toward the mounting surface 96. A projection 120e is formed on the front surface (surface facing the insertion opening for the corresponding connector) of the side wall 120c. It is desirable to provide projection 120e in a position between the mounting surface 96 and the surface of the second body 120 facing the first body 110.

[0029] In addition, there is a second thick section 120j, which is thicker, in the back than in the front of the thick section 120b, on the surface facing the mounting surface 96, at the end of the second body 120 from which the end sections 122b extend (see Fig. 6).

[0030] The second contacts 122 are insert-molded so that one surface of each of the second contacts 122 is exposed on the same surface as the surface of each of plate sections 120A and 120B of the second body 120 opposite to the mounting surface 96 (see Fig. 7).

Details of installation

[0031] As shown in Fig. 7, when the second body 120 is coupled with the first body 110, the thick section 110b of the first body 110 is sandwiched between the side walls 120c. The back side of the thick section 110b of the first body 110 makes contact with the front side of the second thick section 120j of the second body 120. The top face of the thick section 110b of the first body 110 makes contact with the bottom face of the thick section 120b of the second body 120. The side of the thick section 110b of the first body 110 makes contact with the inner side of the side wall 120c of the second body 120. The front side of the thick section 110b of the first body 110 and the front sides of the thick section 120b and the side wall 120c of the second body 120 are present on the same plane. At this time, the surface of the thick section 110b facing the mounting surface 96 and the surfaces of both side walls 120c facing the mounting surface 96 preferably come close to the mounting surface 96.

[0032] When the first body 110 with which the second body 120 has been coupled is inserted into the third body 130, the front sides of the thick sections 110b and 120b and the front sides of side walls 120c make contact with the back side of the third body 130. Accordingly, the surfaces of the first body 110 other than the surface facing the mounting surface 96 make contact with the second body 120 or the third body 130. Since the first body 110 is enclosed by the second body 120 and the third body 130, securing the second body 120 to the third body 130 secures the first body 110. This structure eliminates means for securing the first body 110 to the third body 130, thereby simplifying the component shape.

[0033] In this example, concave portions 130g and 130h are formed on the back side of the third body 130. The projections 110c and 120e are inserted into the concave portions 130g and 130h, respectively. The insertion of the projections 110c and 120e into the concave portions 130g and 130h determines the relative positions of the first body 110, the second body 120, and the third body 130.

[0034] The relative positions of the first body 110, the second body 120, and the third body 130 may be determined by forming concave portions instead of projections 110c and 120e in the same positions, forming projections instead of the concave portions 130g and 130h in the same positions, and mating these projections with concave portions. That is, it is enough to dispose positioning means using concave and convex mating on the back side of the third body 130 and the surfaces on the first body 110 and the second body 120 that make contact with the back side. This structure surely positions the first body 110, the second body 120, and the third body 130.

Two-headed plug

[0035] In this example, there are two insertion openings 130c in the third body 130 (see Fig. 2). Accordingly, the part of the first body 110 to be inserted into the third body 130 is separated into the plate sections 110A and 110B, as shown in Fig. 5. The plate sections 110A and 110B are formed integrally with each other via a connection part 110h, which is an extension of the thick section 110b. In this example, the projections 110c are formed at the front of the connection part 110h.

[0036] As shown in Fig. 6, the part of the second body 120 to be inserted into the third body 130 is also separated into the plate sections 120A and 120B. The plate section 120A is connected to the plate section 120B via a connection part 120h, which is located behind the thick section 120b. The front sides of the connection part 120h and the second thick section 120j are present on the same plane. The connection part 120h is formed by bending a stripe plate into U-shape. The two legs of the connection part 120h are connected to the two thick sections 120b on both sides. The middle section of the connection part 120h is located closer to the mounting surface 96 than the surface of each of the plate sections 120A and 120B of the second body 120 that faces the mounting surface 96. The leg of the connection part 120h on the side of plate section 120B extends upward until it reaches the height of the thick section 120b (see Fig. 7).

[0037] An angular projection 110i, which extends away from the mounting surface 96, is formed integrally with the connection part 110h of the first body 110. The back side of the angular projection 110i makes contact with the front side of the leg on the side of the plate section 120A of the connection part 120h (see Fig. 7). This structure suppresses ratties in the vertical and horizontal directions even when the width of the two-headed plug increases.

[0038] The third body 130 includes two hollow rectangular parallelepiped-like parts 130A and 130B. The plate sections 110A and 120A are inserted in the hollow rectangular parallelepiped-like part 130A. The plate sections 110B and 120B are inserted in the hollow rectangular parallelepiped-like part 130B. The hollow rectangular parallelepiped-like parts 130A and 130B are connected integrally with each other through a connection part 130i at their backs (see Fig. 8).

[0039] This structure allows the two-headed plug-shaped connector to be designed using the same number of components.

Ridges 110g and 120g

[0040] In this example, the first body 110 and the second body 120 are press-fits into the third body 130 with a force applied in the superimposition direction and the movable contact sections 112a and 122a are positioned in the superimposition direction.

[0041] At this time, at least one slim and low ridge 110g extending in the body insertion direction is desirably formed on the surface of the first body 110 opposite to the second body 120 integrally with the first body 110, and at least one slim and low ridge 120g extending in the

body insertion direction is desirably formed on the surface of the second body 120 opposite to the first body 110 integrally with the second body 120 (see Figs. 5 and 6). In this example, two ridges 110g are spaced apart on each of the plate sections 110A and 110B of the first body 110 and two ridges 120g are spaced apart on each of the plate sections 120A and 120B of the second body 120.

[0042] As shown in Fig. 16, in this example, it is desirable that the two ridges 110g disposed on each of the plate sections 110A and 110B of the first body 110 are sandwiched between the two ridges 120g disposed on each of the plate sections 120A and 120B of the second body 120. In addition, the interval of the ridges 110g or 120g on each plate section is desirably the same. Fig. 16 shows the cross section q-q' in Fig. 9.

[0043] When the first body 110 and the second body 120 make contact with each other through their surfaces, if the flatness of the first body 110 and the second body 120 is large, interference may be caused. In addition, the clearance between the first body 110 with which the second body 120 has been coupled and the third body 130 is small, so it is difficult to insert the first body 110 with which the second body 120 has been coupled into the third body 130. With the structure in this example, the clearance between the first body 110 and the second body 120 can be embedded, thereby enabling positioning in the vertical direction. Even if interference between the first body 110 and the second body 120 through their mutually facing surfaces occurs, the ridges 110g or 120g are crushed to enable positioning.

First cover 140

[0044] The third body 130 is covered with the first cover 140 and the second cover 150, which are made of metal. In this example, the hollow rectangular parallelepiped-like parts 130A and 130B of the body 130 are covered with the first cover 140 and the second cover 150, respectively.

[0045] As shown in Fig. 17, the first cover 140 is created by forming a metal plate into a hollow rectangular parallelepiped. The hollow rectangular parallelepiped-like part 130A of the third body 130 is inserted into the first cover 140.

[0046] A surface of the first cover 140 that is in parallel with and more distant from the mounting surface 96 extends to the rear end of the second body 120 to form a fixing extension 140b. The fixing extension 140b extends to the rear end of the second body 120 along the surface of the second body 120 and the third body 130, which is in parallel with the mounting surface 96, and more distant from the mounting surface 96. Locking pieces 140d are formed on both sides at the back of the fixing extension 140b. The locking pieces 140d are bent toward the mounting surface 96. The first body 110 and the second body 120 are surely secured to the third body 130 by mechanically swaging the locking pieces 140d.

Second cover 150

[0047] As shown in Fig. 18, the second cover 150 is formed by bending a metal plate into U-shape. One leg of the second cover 150 is extended backward to form a fixing extension 150b.

[0048] An opening 150c into which the corresponding connector is inserted is formed in the center. The second cover 150 is attached so as to clamp and cover the hollow rectangular parallelepiped-like part 130B of third body 130.

[0049] Fig. 19 shows the cross section r-r' in Fig. 9. A groove 130j is disposed in the external surface of the hollow rectangular parallelepiped-like part 130B of third body 130 that faces the mounting surface 96. The groove 130j is covered at the end (back wall) to form a small engaging hole 130k.

[0050] Small locking pieces 150k are formed on both sides of the other leg (on the side of the mounting surface 96) of the U-shaped second cover 150. Each of the small locking pieces 150k is engaged in the small engaging hole 130k. This structure prevents the second cover 150 from opening downward.

[0051] The fixing extension 150b is parallel with the mounting surface 96 and configures the surface that is more distant from the mounting surface 96. The fixing extension 150b extends to the rear end along the surface of the second body 120 and the third body 130, which is in parallel with the mounting surface 96, and more distant from the mounting surface 96.

[0052] A locking piece 150d is formed in the middle at the extending end of the fixing extension 150b. The locking piece 150d is bent toward the mounting surface 96. The first body 110 and the second body 120 are surely secured to the third body 130 by mechanically swaging the locking piece 150d.

[0053] The third body 130 is covered with the metal covers as described above to obtain shield effects. In this example, the hollow rectangular parallelepiped-like parts 130A and 130B of the third body 130 are covered with the first cover 140 and the second cover 150, which are mutually different components. This structure enables one shield cover (first cover 140) that covers four sides. The plug covered by the shield cover that covers four sides can be used as a transmission and reception plug for high-speed transmission signals.

Tapered locking parts 130p and 130m and rectangular openings 140j and 150m

[0054] In this example, low tapered locking parts 130p and 130m are formed on the external surfaces of the hollow rectangular parallelepiped-like parts 130A and 130B of the third body 130 that are opposite to the mounting surface 96 (see Fig. 8). When the tapered locking parts 130p and 130m that increase in height toward their backs are covered with the first cover 140 and the second cover 150, respectively, the tapered locking parts 130p

and 130m are inserted into rectangular openings 140j and 150m disposed on the fixing extensions 140b and 150b. This structure prevents the covers from being removed forward (Figs. 17 and 18).

Third cover 160

[0055] As shown in Figs. 2 and 20, the third cover 160 covers the fixing extensions 140b and 150b of the first cover 140 and the second cover 150. The third cover 160 covers a surface of the second body 120 and the third body 130, which is orthogonal to the mounting surface 96, and parallel to the contacts. In addition, legs 160a project orthogonally to the mounting surface 96 on the both sides of the third cover 160.

[0056] In this example, legs 160a project in the front and back positions on both sides of the third cover 160. As shown in Fig. 21, the legs 160a are connected by soldering etc. to secure the surface mount multi-connector 100 to a printed circuit board 210.

[0057] The side wall of the third body 130 on the side of the hollow rectangular parallelepiped-like part 130B is bent from the back end to the front and then extends forward to form a locking piece 160b. A locking nail 160c, which is bent externally, is formed at the tip of the locking piece 160b.

[0058] In addition, both arms 160d and 160e of a U-shaped stripe plate are spaced apart along the external surface of the third cover 160. The U-shaped stripe plate is bent at a middle point 160f along the side wall of the hollow rectangular parallelepiped-like part 130B. The arm 160d near the back side is connected to the back end of the third cover 160. The end of the arm 160e extends to a notch 160g which is formed in the middle of the third cover 160. The arm 160e is then bent toward the mounting surface 96. The arm 160e extends forward in a path between the bodies to form a locking piece 160h. The tip of the locking piece 160h is bent externally to form a locking nail 160i.

[0059] Lower tapered locking parts 130n are formed on both sides of the third body 130 (see Fig. 8). When a third cover 160 is put over the lower tapered locking parts 130n, which increases in height toward the front, from the back to the front, the tapered locking parts 130n are inserted into rectangular openings 160m disposed on the side walls of the third cover 160. This structure prevents the third cover 160 from being removed backward.

[0060] A locking piece 160p is bent toward the mounting surface 96 in the middle at the back end of the third cover 160. This structure lets the locking piece 160p mate with the back side of the second body 120 and prevents the third cover 160 from being removed forward.

[0061] Lugs 140e and 150e, which bend obliquely from the back to the front away from the mounting surface 96, are formed on fixing extensions 140b and 150b, respectively. The lugs 140e and 150e bring the first cover 140 and the second cover 150 into secure contact with the third cover 160.

[0062] The locking piece 160b and 160h and the locking nails 160c and 160i constitute latch springs so that the latch springs are formed integrally with the third cover 160. The locking piece 160b and the middle point 160f are held and a force is applied to operate the latches. This structure increases the holding force for the unit having the corresponding receptacle, without increasing the number of parts.

[0063] The third cover 160 can be formed separately with the first cover 140 and the second cover 150. Accordingly, the third cover 160 may be formed of thicker metal material than in the first cover 140 or the second cover 150. This structure improves the mounting strength of printed circuit board. Since the plug thickness dimensions are defined for the first cover 140 and the second cover 150, the thickness of material is limited, thereby making it difficult to obtain a desired strength.

[0064] Fig. 21 shows the state where the surface mount multi-connector 100 is mounted on the printed circuit board 210 of an electric apparatus. This structure allows the electronic apparatus with a predetermined printed circuit board to use the surface mount multi-connector 100 for connection with another electronic apparatus with the corresponding connector. At this time, the holding force can be increased by providing the corresponding connector with the receptacle that mates with the latch spring formed integrally with the third cover 160.

[0065] The present invention is not limited to the above embodiments, and various modifications may be made in the embodiments without departing from the scope of the invention. For example, the surface mount multi-connector 100 may not be two-headed shaped and the shapes of the bodies and covers may be changed as necessary. In addition, the present invention can be practiced without the covers.

Effects

[0066] These structures improve the coplanarity of the connection portions 112d and 122d of the first and second contacts 112 and 122 with respect to the mounting surface 96. Since the tips 112c and 122c of the movable contacts 112a and 122a of the first and second contacts 112 and 122 mate with catching parts 130a and 130b of the third body 130 to give preload, the contact reliability can be improved.

Claims

1. A surface mount multi-connector comprising:

   a first body in which a plurality of first contacts having movable contact sections and end sections that extend oppositely to each other are held by insert molding;

   a second body in which a plurality of second contacts having movable contact sections and

end sections that extend oppositely to each other are held by insert molding; and
a third body that incorporates the first body with which the second body has been coupled so that the movable contact sections of the second contacts and the movable contact sections of the first contacts face in the same direction,
wherein tips ahead of the movable contact sections of the first contacts and tips ahead of the movable contact sections of the second contacts elastically mate with catching parts formed on an inner wall of the third body, and connection portions of the end sections of the first contacts and connection portions of the end sections of the second contacts lie in a same plane.

2. The surface mount multi-connector of claim 1, further comprising a cover that covers a hollow rectangular parallelepiped-like part of the third body, the hollow rectangular parallelepiped-like part accommodating the movable contact sections of the first contacts and the movable contact sections of the second contacts, wherein the cover has a fixing extension that extends backward, the fixing extension has a locking piece at the end thereof, and the locking piece bends toward a mounting surface.

3. The surface mount multi-connector of claim 2, further comprising a third cover that covers the fixing extension of the cover,
wherein legs that the third cover has on both sides project orthogonally to the mounting surface.

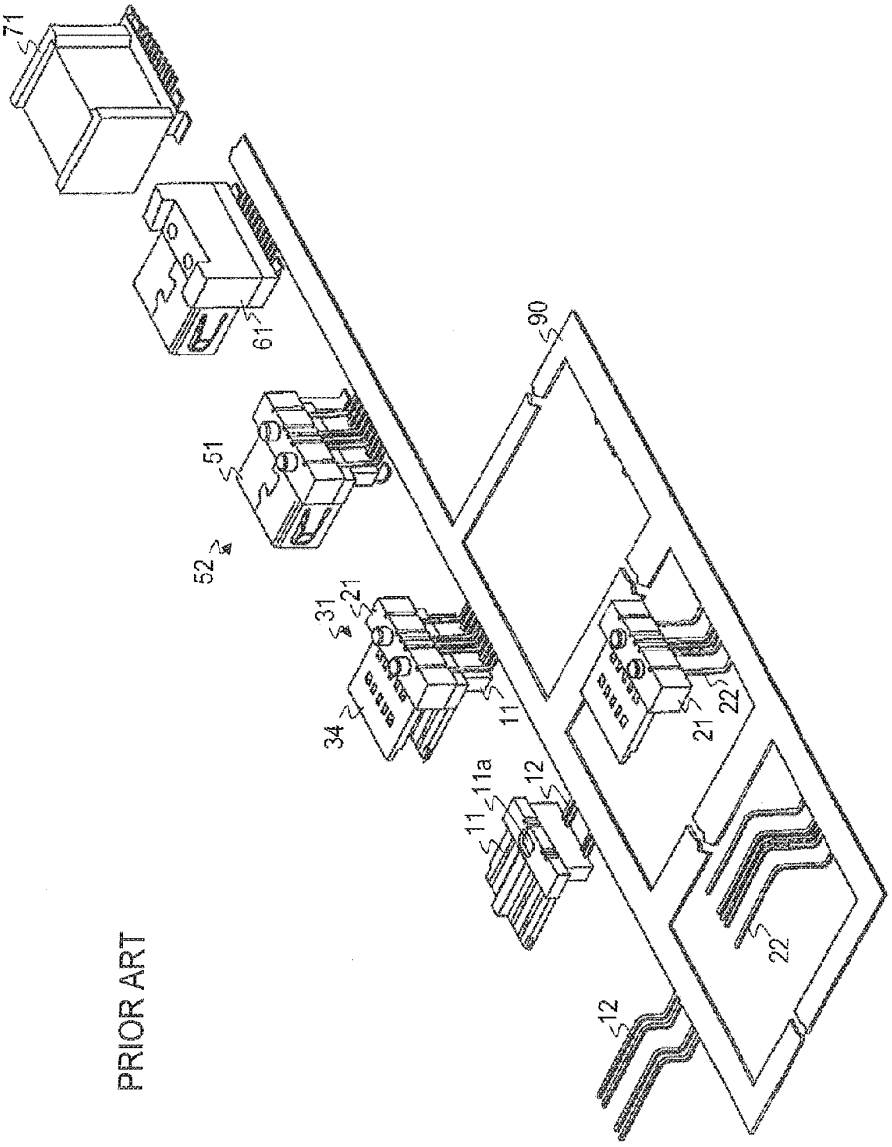
4. The surface mount multi-connector of claim 3, wherein a latch spring that mates with a corresponding receptacle is formed integrally with the third cover.

5. The surface mount multi-connector of any one of claims 1 to 4, wherein the third body has two hollow rectangular parallelepiped-like parts and each of the first body and the second body is separated into two plate sections that are inserted into the two hollow rectangular parallelepiped-like parts respectively.

6. The surface mount multi-connector of claim 5, wherein the cover that covers the third body having the two hollow rectangular parallelepiped-like parts includes a first cover and a second cover, which are mutually different components.

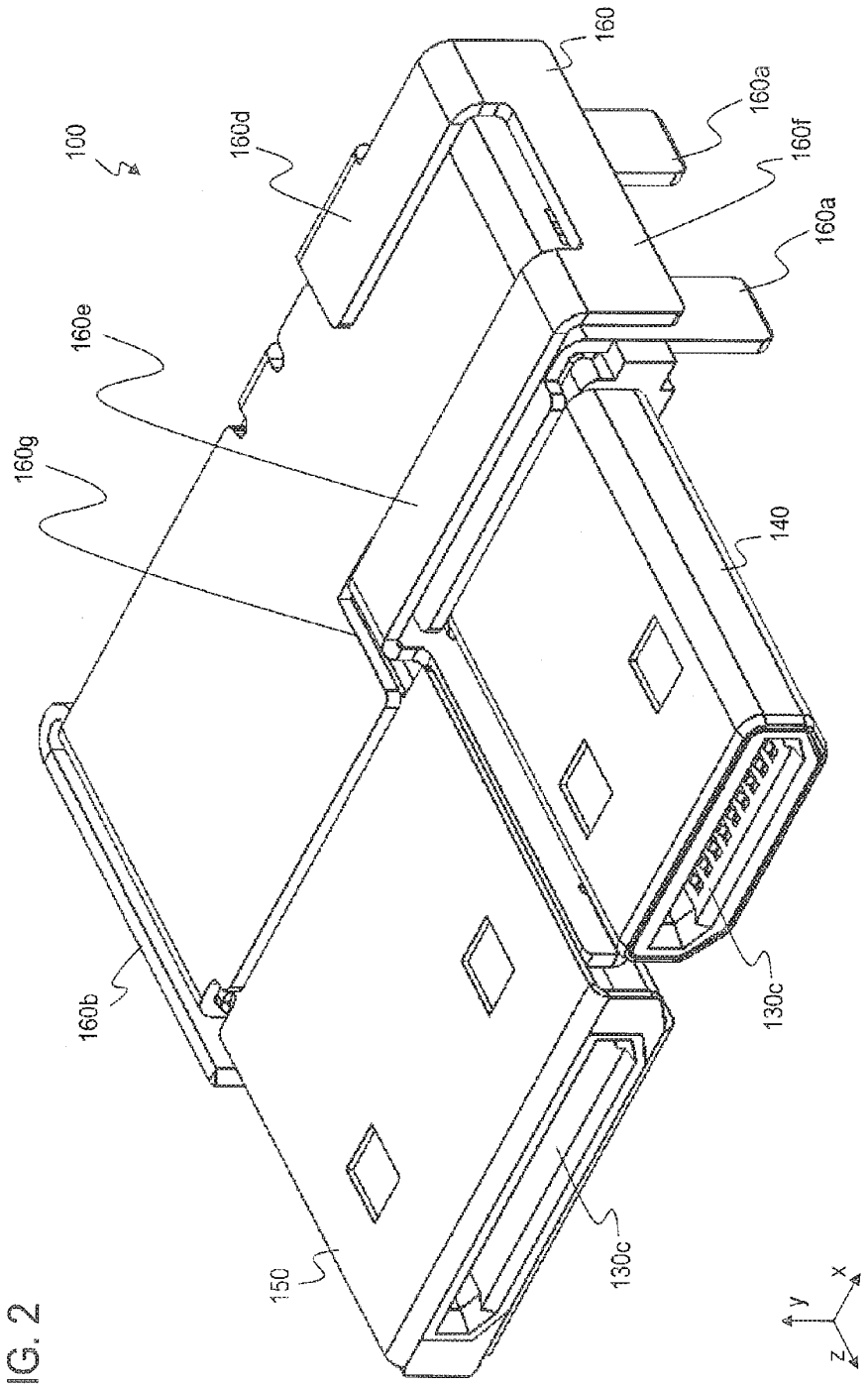
7. The surface mount multi-connector of any one of claims 1 to 6, wherein the surfaces of the first body other than the mounting surface make contact with the second body or the third body.

8. An electronic apparatus having the surface mount multi-connector of any one of claims 1 to 7, wherein the surface mount multi-connector is mounted on a printed circuit board.



PRIOR ART

FIG. 1


100
160
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160d
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140
160b
130c
150
130c
x
y
z

FIG. 2

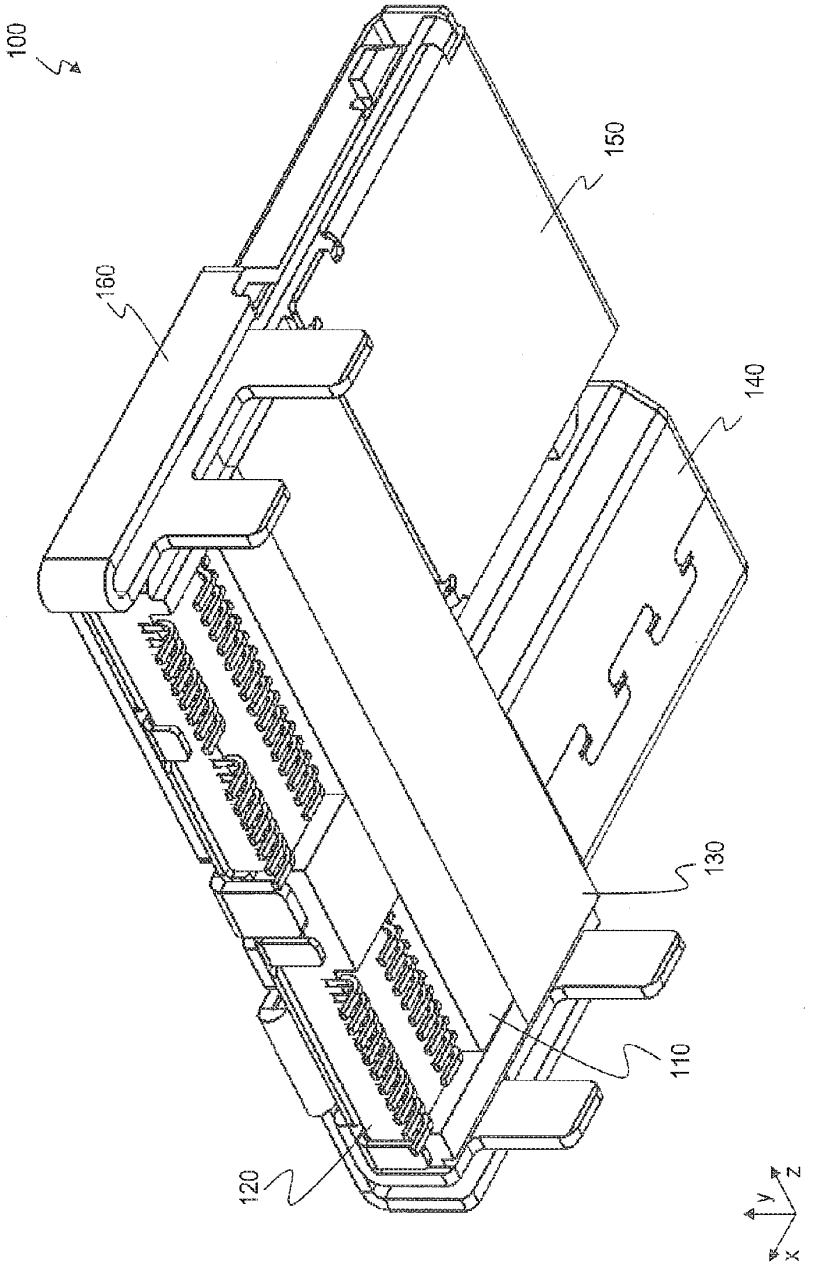


FIG. 3

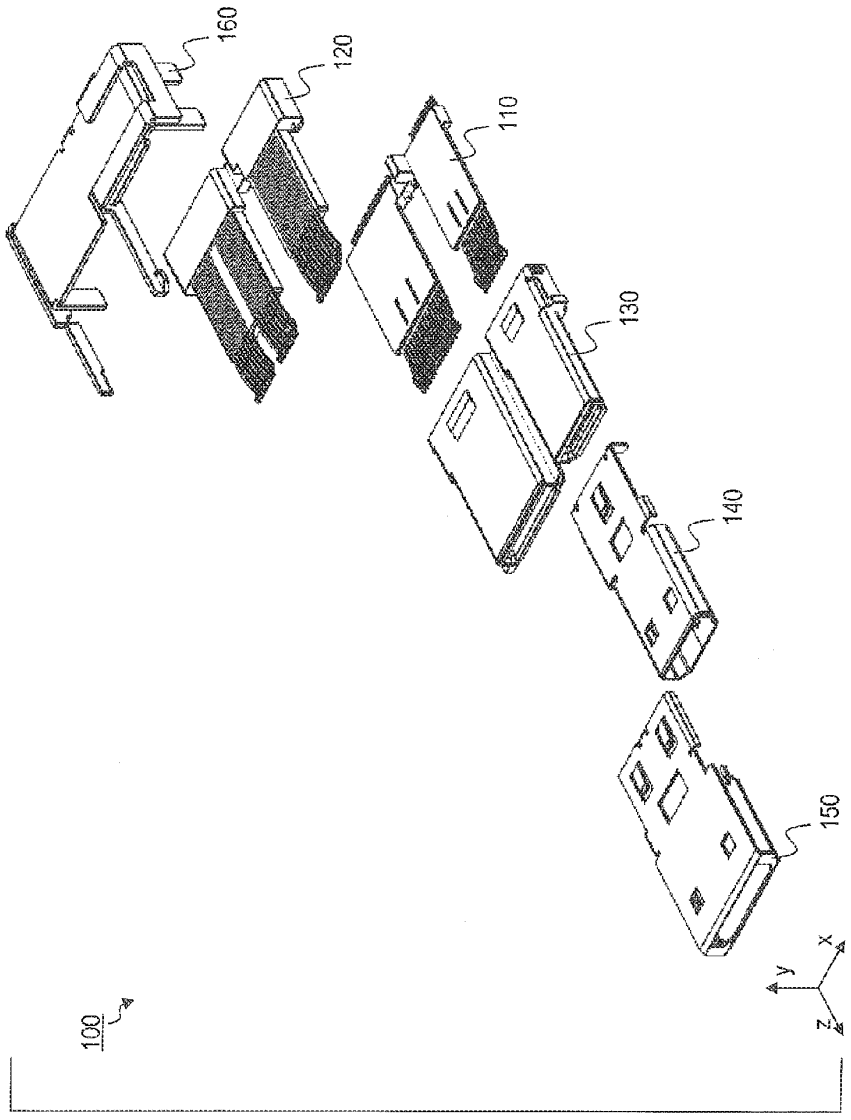


FIG. 4

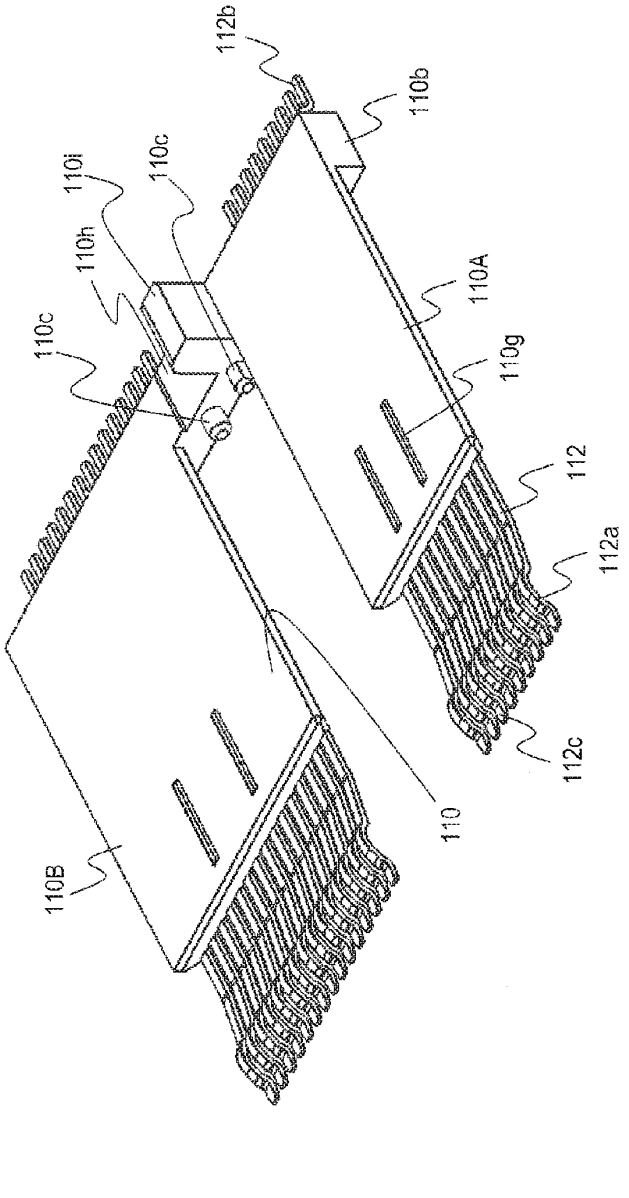
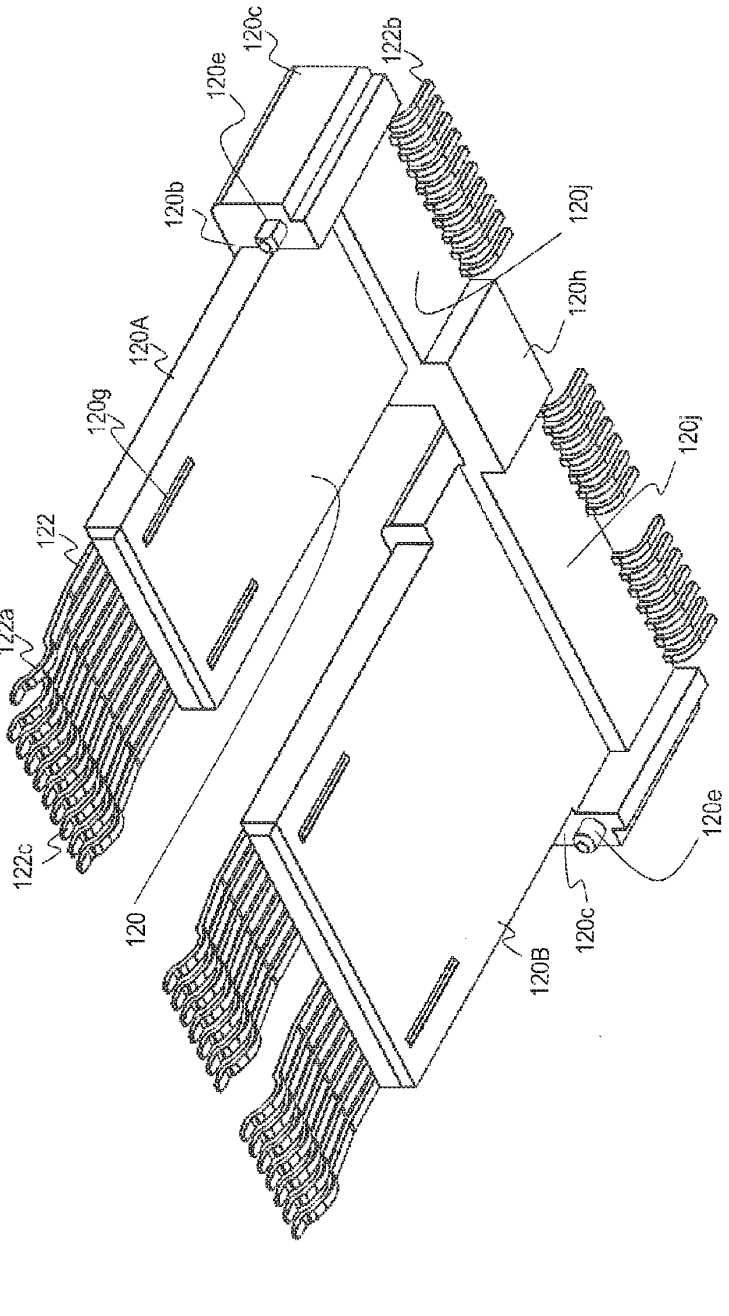


FIG. 5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120b
120j
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120g
120j
122
122a
122c
120e
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120c
120B
y
x
z

FIG. 6

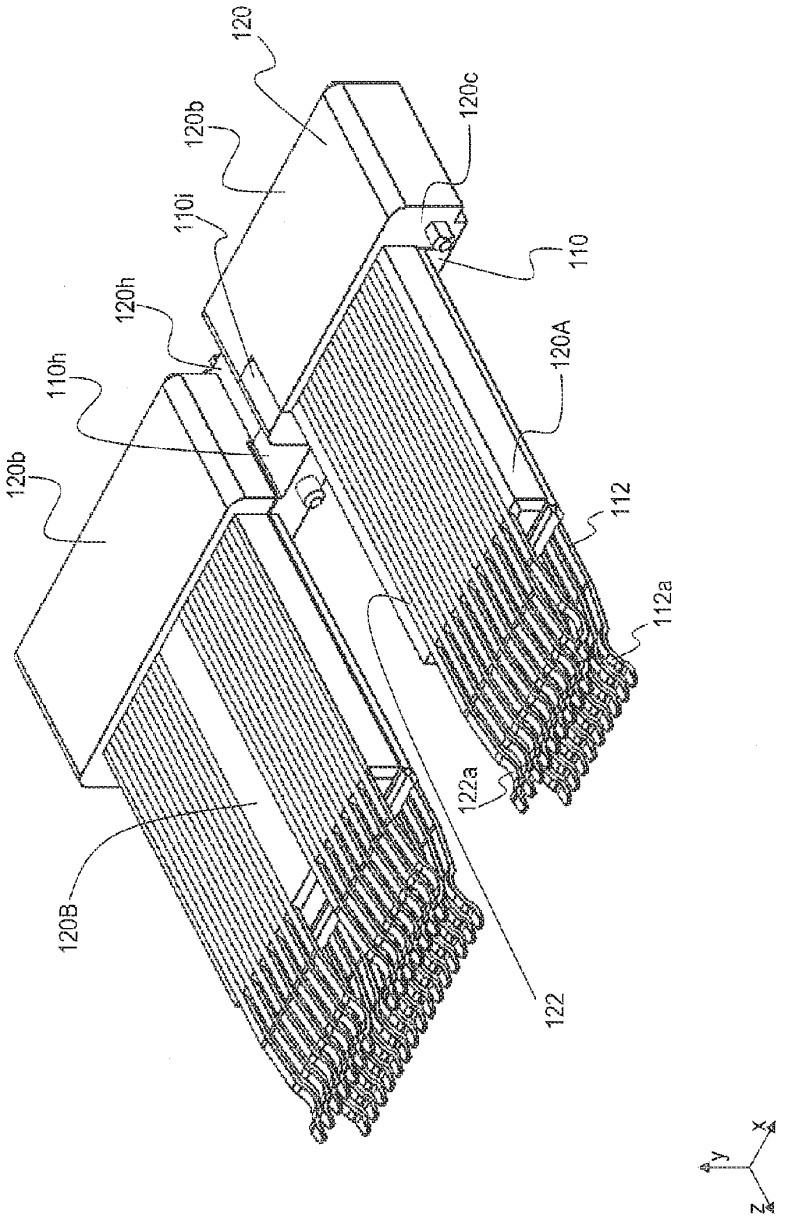
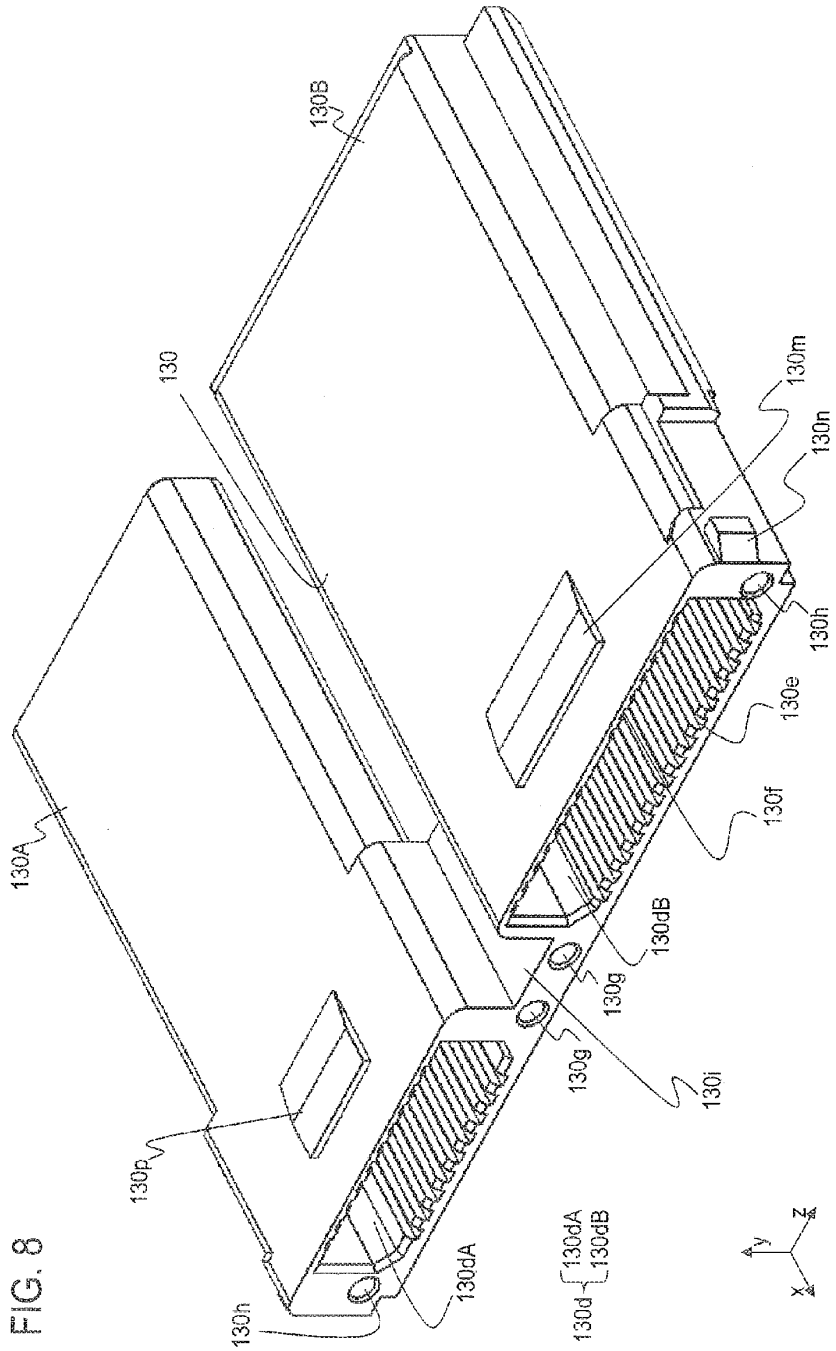


FIG. 7

FIG. 8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130dA
130d
130dA
130dB
y
z
x

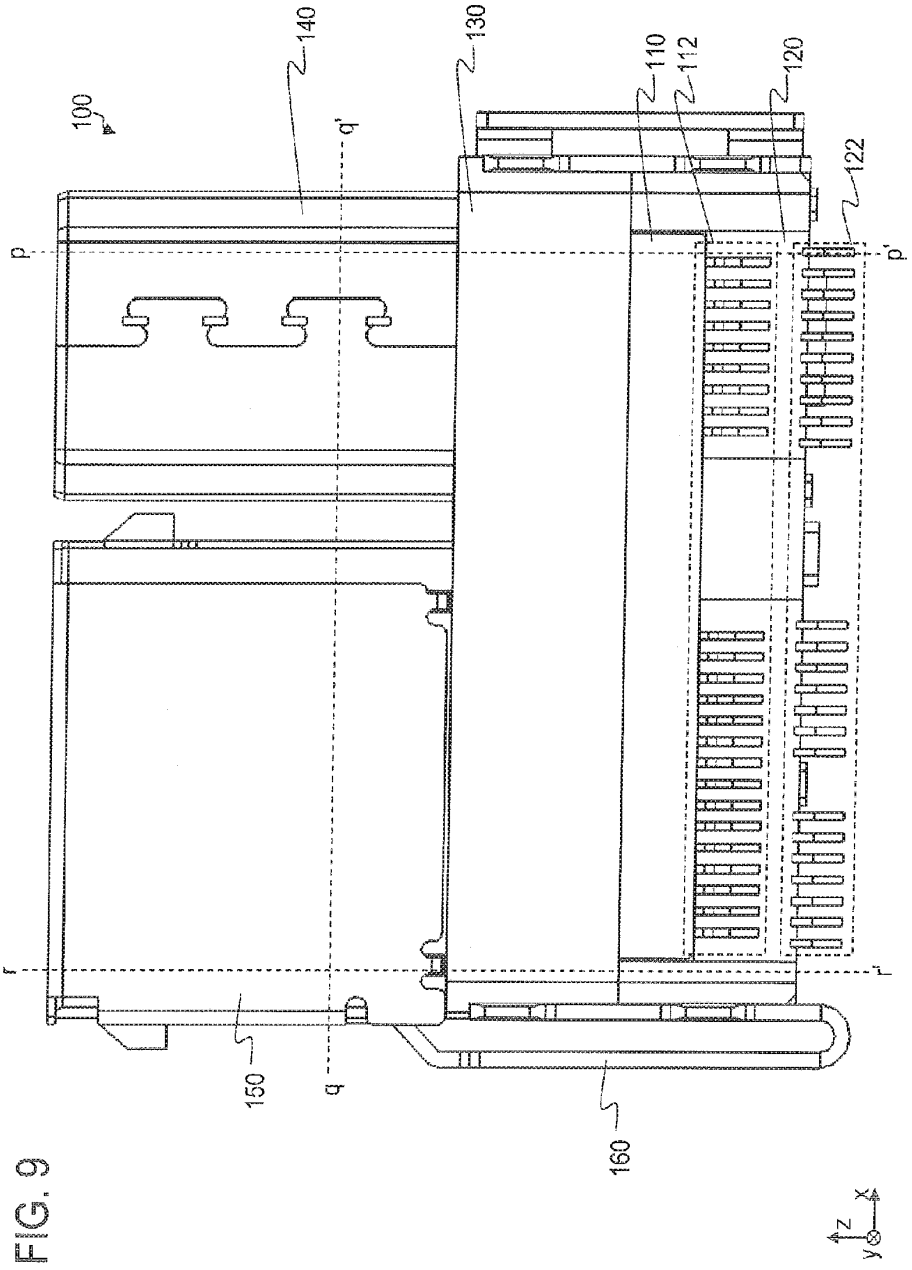


FIG. 9

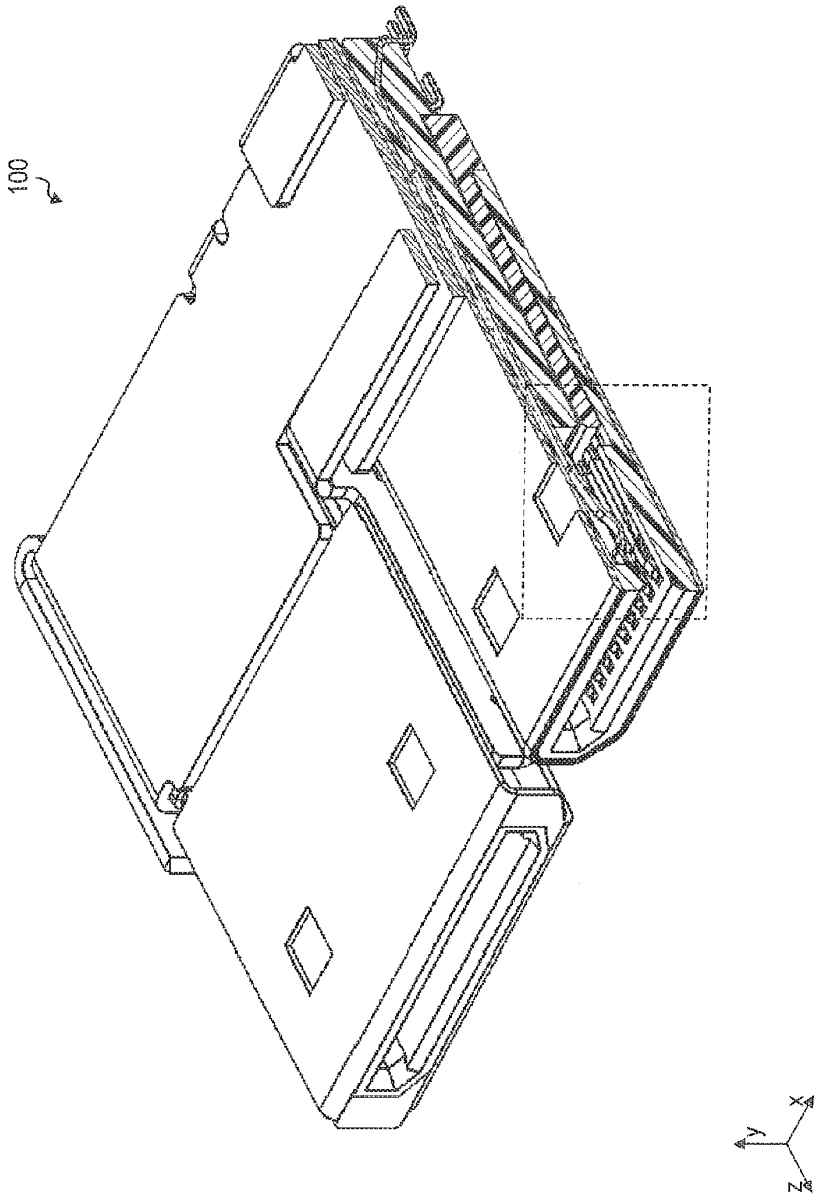


FIG. 10

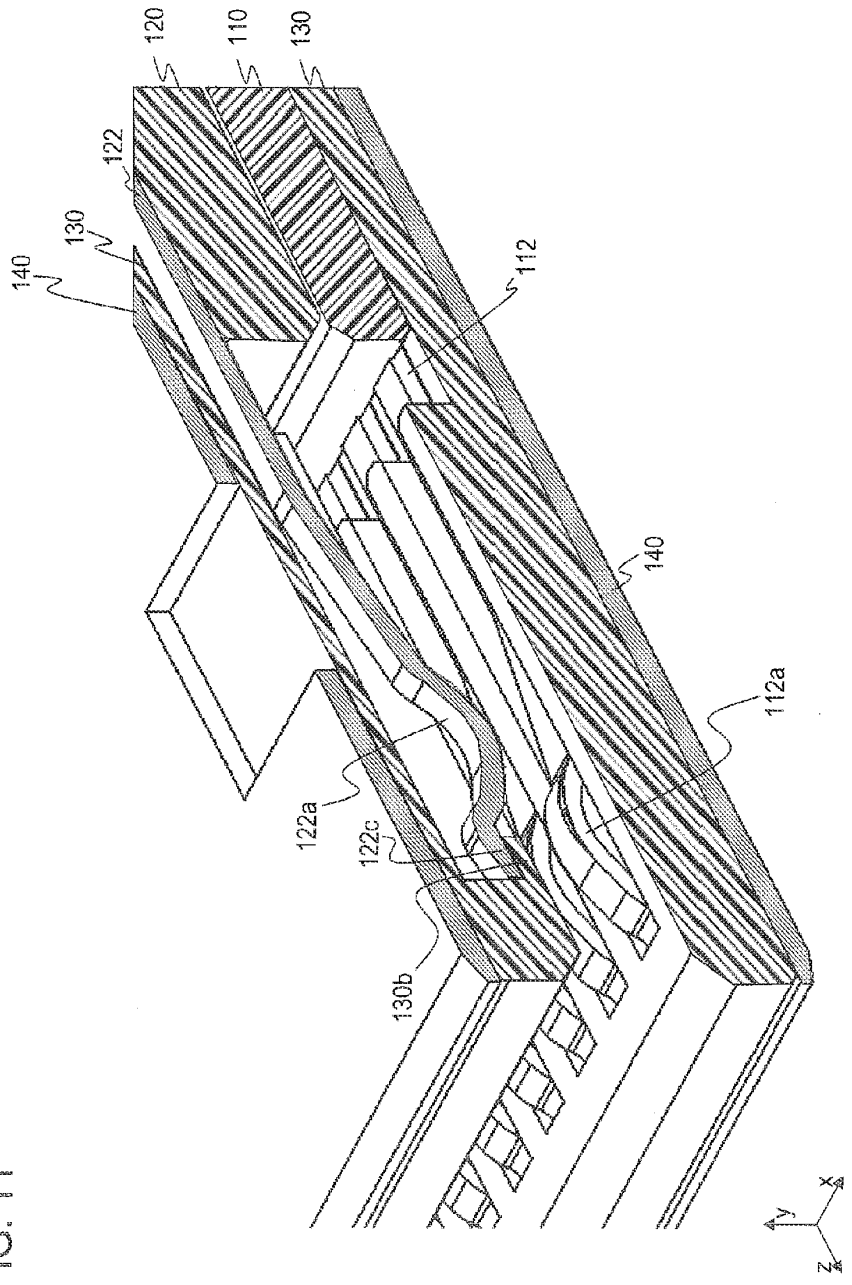
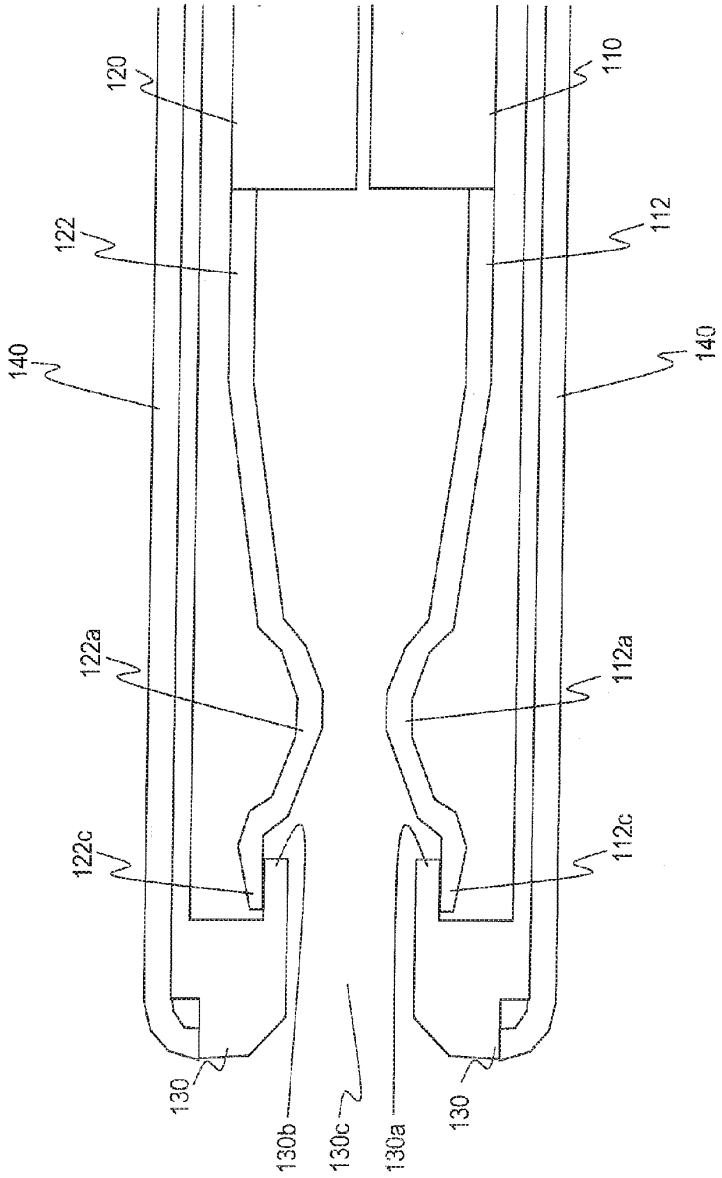


FIG. 11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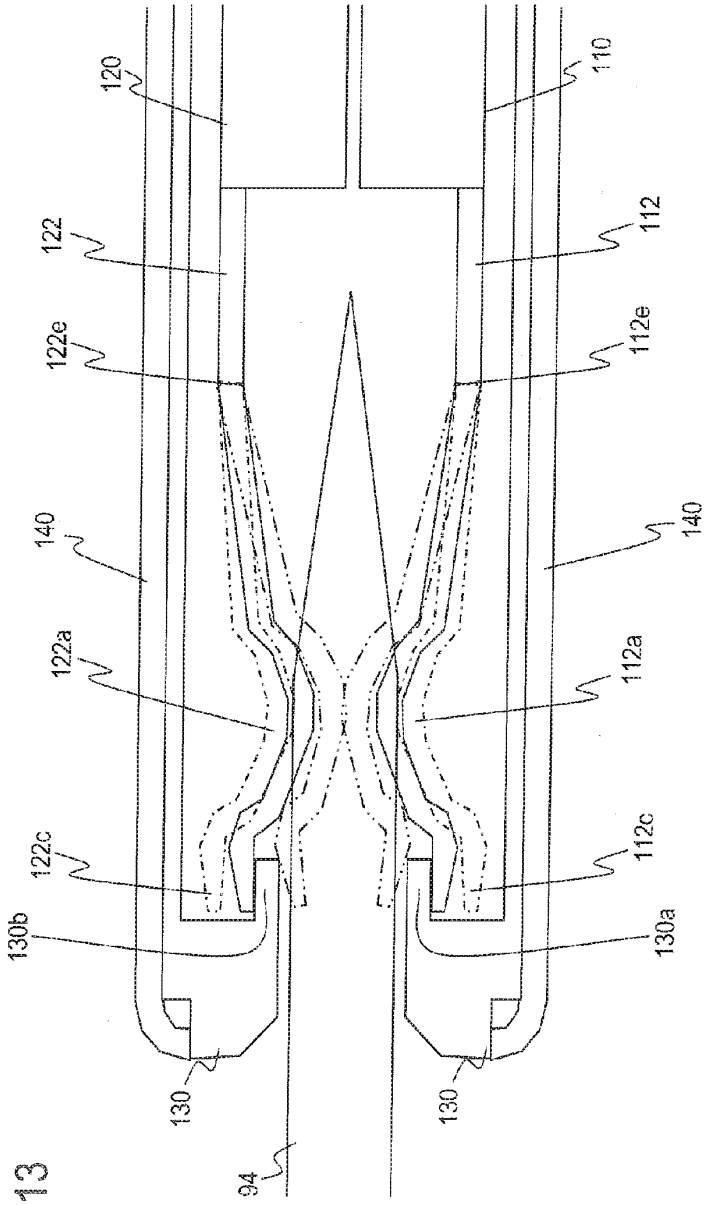
110
122
112
140
140
122a
112a
122c
112c
130
130b
130c
130a
130

FIG. 12


120
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112e
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140
122a
112a
122c
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130b
130a
130
130
94

FIG. 13

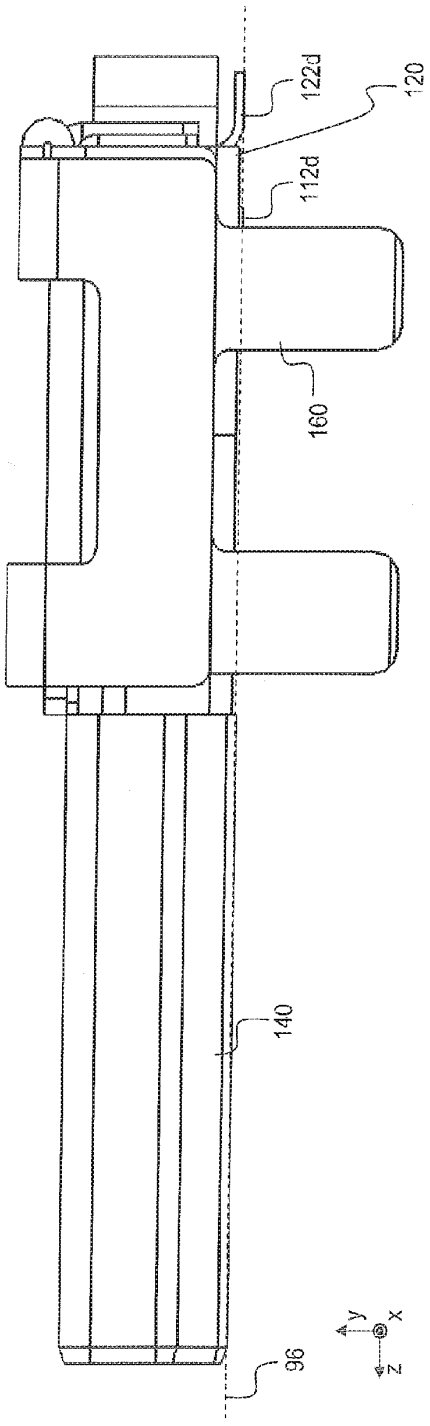


FIG. 14

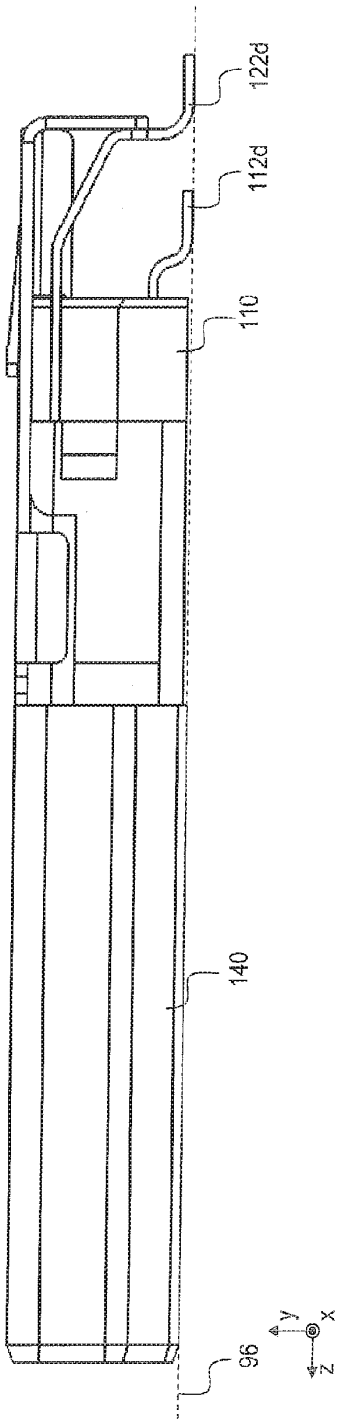


FIG. 15

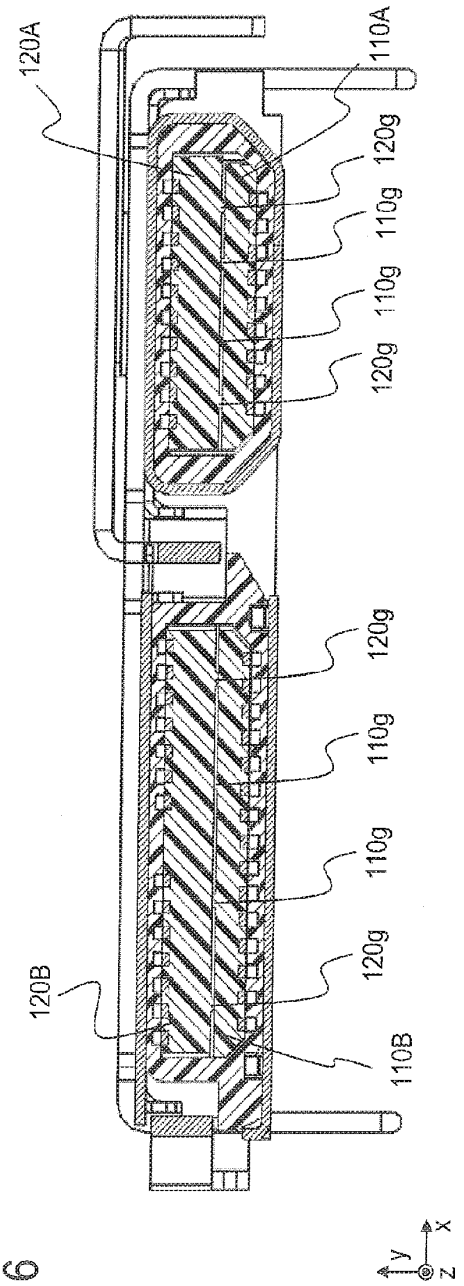


FIG. 16

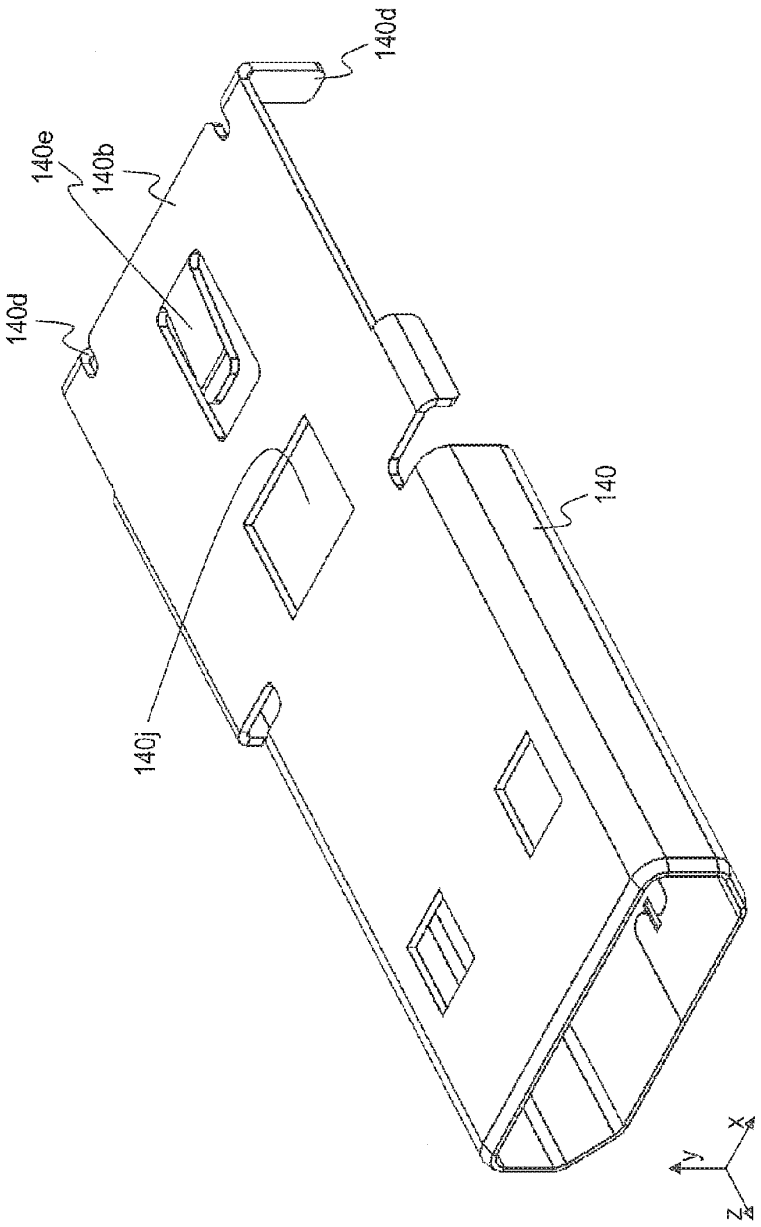


FIG. 17

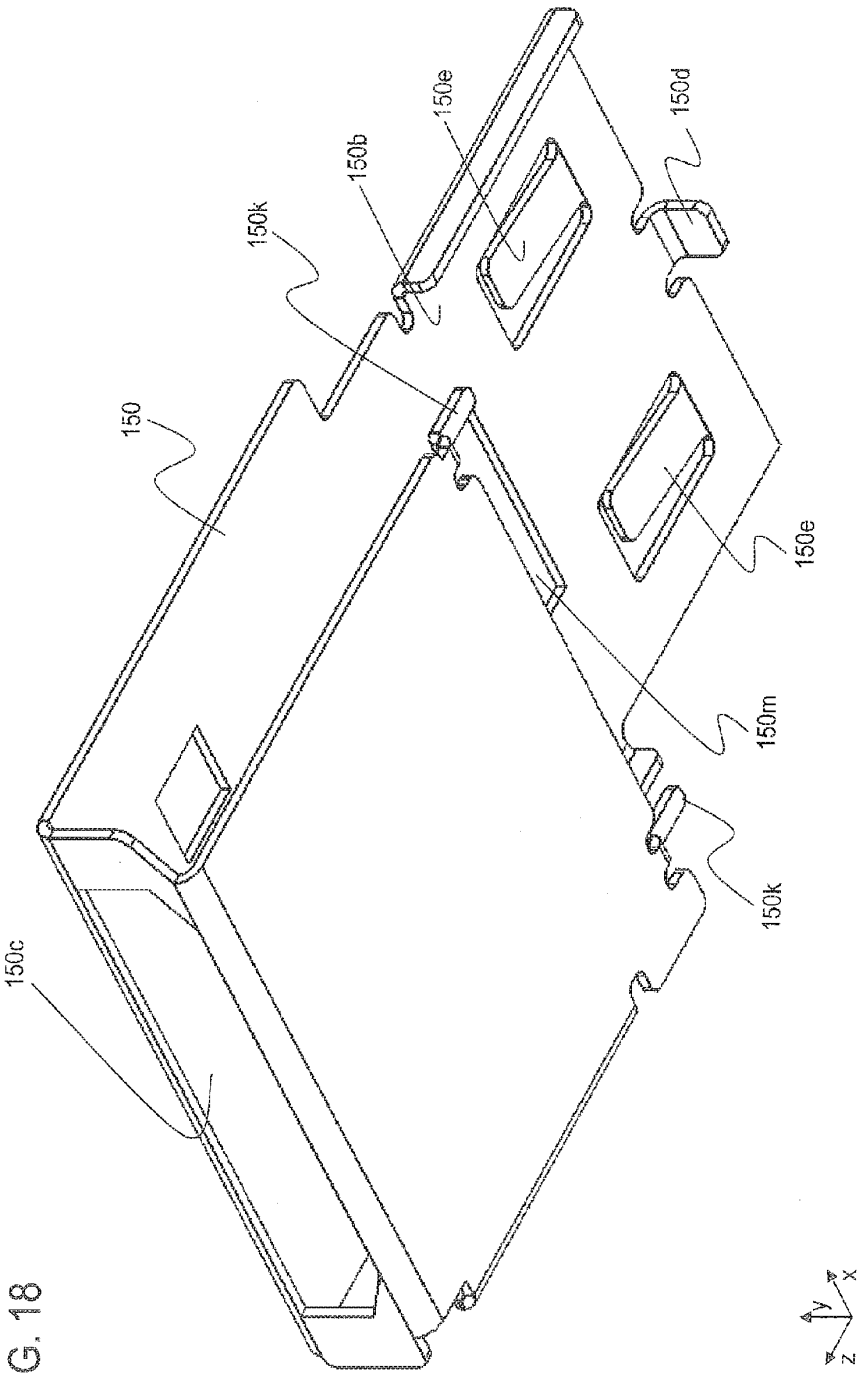


FIG. 18

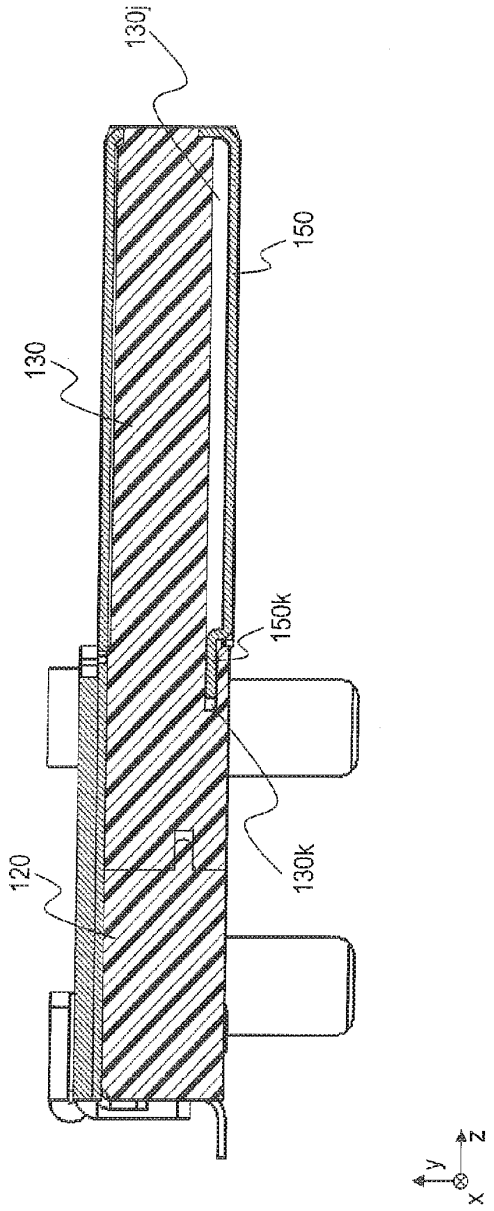
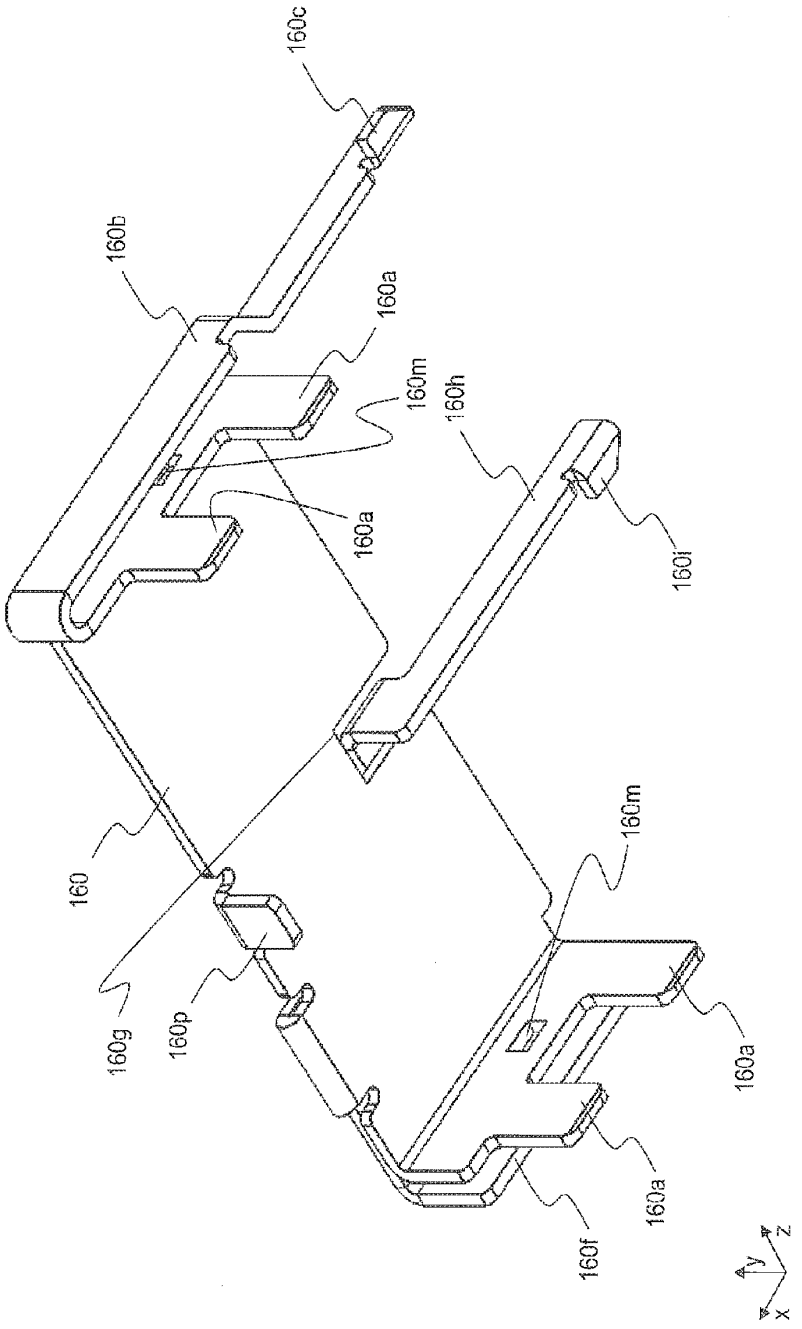


FIG. 19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160g
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160a
160a
160f
z
y
x

FIG. 20

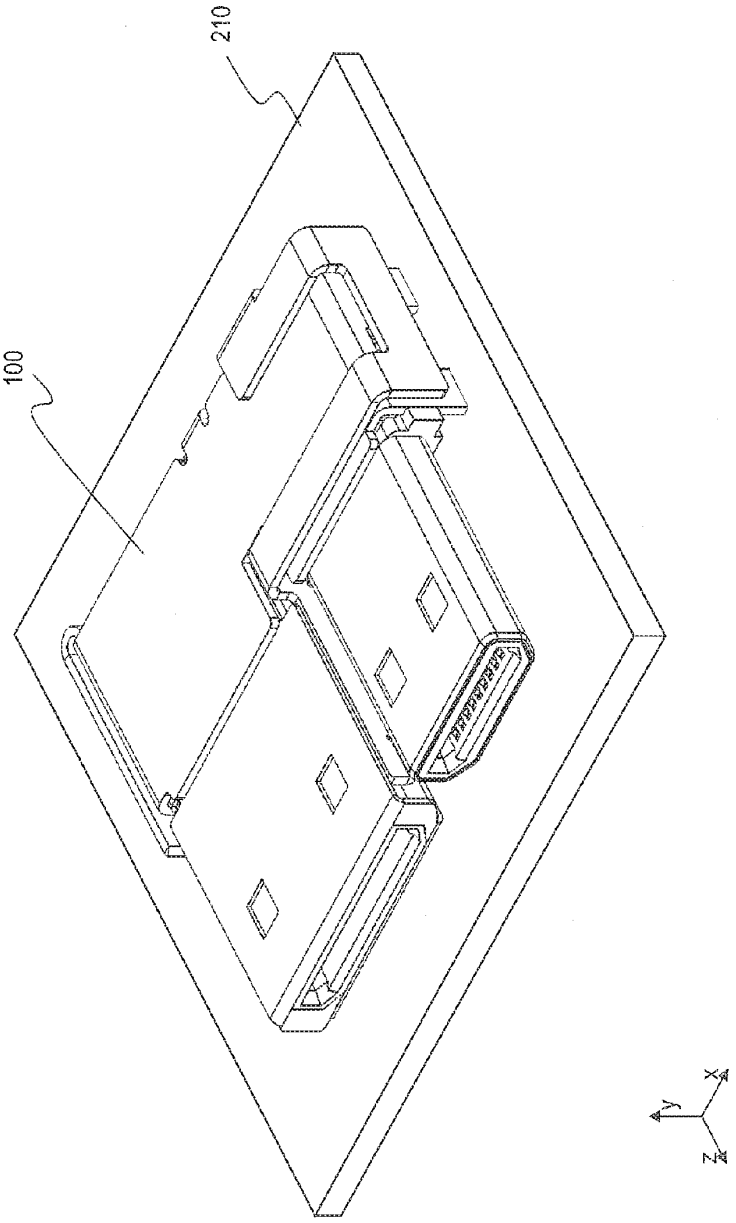

FIG. 21

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European Patent Office
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EUROPEAN SEARCH REPORT

Application Number
EP 11 17 1712

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
Y	US 2005/009401 A1 (HU JINKUI [CN] ET AL) 13 January 2005 (2005-01-13) * paragraph [0025]; figures 1,5,7 *	1-8	INV. H01R13/502 H01R12/72
Y	EP 1 274 151 A2 (FRAMATOME CONNECTORS INC [FR] FRAMATOME CONNECTORS INT [FR]) 8 January 2003 (2003-01-08) * paragraphs [0015], [0021]; figure 4 *	1-8	ADD. H01R13/42 H01R12/57
A	US 5 975 917 A (WANG KUO-CHENG [TW] ET AL) 2 November 1999 (1999-11-02) * claim 1; figures 3-5 *	1	
A,D	JP 2004 537836 A (MOLEX INC) 16 December 2004 (2004-12-16) * abstract *	1	
A	US 5 256 085 A (TAN HAW-CHAN [US] ET AL) 26 October 1993 (1993-10-26) * abstract; claim 2; figures 1-4 *	1	

TECHNICAL FIELDS SEARCHED (IPC)
H01R

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
The Hague	21 September 2011	Jiménez, Jesús

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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T : theory or principle underlying the invention
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ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 11 17 1712

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21-09-2011

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CONNECTOR DEVICE

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Classification:	**- international:*H01R13/652; H01R24/00*** **- cooperative: H01R12/714; H01R12/716; H01R12/775; H01R12/79;** H01R12/57; H01R12/598; H01R12/675; H01R13/6275; H01R13/631; H01R13/6582
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Abstract of JP2006344524 (A)

PROBLEM TO BE SOLVED: To effectively prevent deformation of a position where central stress is generated at a receptacle connector by connection when a plug connector is connected to a receptacle connector. ;SOLUTION: The connector device 1 for connecting a connector 100 fitted at an end of a cable C with a counterpart connector 202 mounted on a base plate P is provided with a fixing means 213R with an outward-bent piece 222 for fixing the site 204R where the central stress is generated at the counterpart connector by connection to prevent it from deformation, when the connector 100 is connected with the counterpart connector 202. ;COPYRIGHT: (C) 2007,JPO&INPIT

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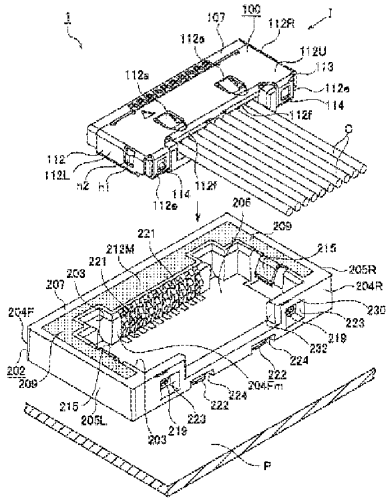
最終頁に続く

(54)【発明の名称】コネクタ装置

(57)【要約】
【課題】プラグコネクタをリセプタクルコネクタに接続した際に、リセプタクルコネクタにおいて接続による集中応力が発生する箇所が変形してしまうことを効果的に防止すること。
【解決手段】ケーブルＣの一端に設けたコネクタ１００を、基板Ｐに取着した相手方コネクタ２０２に接続するためのコネクタ装置１であって、コネクタ１００を前記相手方コネクタ２０２に接続した際に、前記相手方コネクタ２０２において接続による集中応力が発生する箇所２０４Ｒが変形しないように、当該箇所を基板Ｐに対して固定する、外曲片２２２を有する固定手段２１３Ｒを設ける。
【選択図】図２



【特許請求の範囲】
【請求項1】
ケーブル（Ｃ）及びその一端に接続された端子（１２１）をハウジング（１０７）に有するコネクタ（１００）と、
このコネクタ（１００）が接続される相手方コネクタ（２０２）と、を有するコネクタ装置（１）であって、
前記相手方コネクタ（２０２）は、
相手方ハウジング（２０７）と、
この相手方ハウジング（２０７）に設けられ、前記コネクタとの接続の際に前記コネクタの端子（１２１）と接触し、かつ基板に固定される相手方端子（２２１）と、
前記相手方ハウジング（２０７）において、前記相手方端子（２２１）の設置箇所と対向する箇所に前記ケーブル（Ｃ）が挿通される部位として形成されたケーブル挿通部（２０４Ｒ）と、
このケーブル挿通部（２０４Ｒ）を前記基板（Ｐ）に対して固定する固定手段（２１３Ｒ，２２２）とを有することを特徴とするコネクタ装置（１）。
【請求項2】
前記固定手段（２１３Ｒ，２２２）は、前記ケーブル挿通部（２０４Ｒ）に当接又は埋設されて前記ケーブル挿通部（２０４Ｒ）を支持する支持部（２１３Ｒ）と、この支持部（２１３Ｒ）に一体形成され前記基板（Ｐ）に半田付けされる固着部（２２２）とを有することを特徴とする請求項１に記載のコネクタ装置（１）。
【請求項3】
前記固定手段（２１３Ｒ，２２２）は、前記コネクタ（１００）を前記相手方コネクタ（２０２）に接続した際に前記ケーブル（Ｃ）を流れるノイズをグランドに流す金属部材であることを特徴とする請求項２に記載のコネクタ装置（１）。
【請求項4】
前記コネクタ（１００）及び前記相手側コネクタ（２０２）のうちの少なくとも一方には、両コネクタ（１００，２０２）の接続の際に他方のコネクタに掛止される掛止部（２１９）を有することを特徴とする請求項１～３のいずれかに記載のコネクタ装置（１）。
【請求項5】
前記掛止部（２１９）は、前記コネクタ（１００）又は前記相手方コネクタ（２０２）に掛止する弾性片（２１９）であって、前記相手方コネクタ（２０２）又は前記コネクタ（１００）には、この弾性片（２１９）が入る開口（１１４）が形成されていることを特徴とする請求項４に記載のコネクタ装置（１）。
【請求項6】
前記相手方ハウジング（２０７）は、前記ケーブル（Ｃ）を流れるノイズをグランドに流す金属板（２０９）を備え、この金属板（２０９）に前記固定手段（２１３Ｒ，２２２）が形成されていることを特徴とする請求項５に記載のコネクタ装置（１）。
【請求項7】
前記金属板（２０９）の一部に前記掛止部（２１９）が形成されていることを特徴とする請求項６に記載のコネクタ装置（１）。

【発明の詳細な説明】
【技術分野】
【0001】
本発明はコネクタ装置に関する。
【背景技術】
【0002】
携帯電話機やパーソナルコンピュータ等、多量の情報を伝達する通信機器では、高い周波数の信号を伝達するケーブルとして同軸ケーブルが用いられている。
このような同軸ケーブルを平面的に多数並列してフラット状とし、それらの両端にプラグコネクタを取り付けることでケーブル付きプラグコネクタが形成される。

【0003】
ケーブル付きプラグコネクタを介して、電子部品が多数取着された基板同士を接続することにより、各基板に取付けられている電子部品間でデータの信号の各種処理や電源供給等の電気の伝搬が行われる。
【0004】
一方、携帯電話機やパーソナルコンピュータその他の通信機器の軽薄短小化傾向は一層進んでいる。そして、軽薄短小化を実現するために、当然ながらこれら機器の一部品であるコネクタに対し、その低背化・小型化・軽量化の要求は高くなっている。またコネクタの低背化・小型化・軽量化が進むと、作業がしづらくなるが、作業性を向上させるための技術が要求される。
【0005】
図１１は、ケーブル付きプラグコネクタＩを、そのプラグコネクタ３００と接合される相手方コネクタ、いわゆるリセプタクルコネクタ３０２に接続する前の状態を示す。プラグコネクタ３００をリセプタクルコネクタ３０２に接続するには、基板Ｐ上に設けられたリセプタクルコネクタ３０２に対しプラグコネクタ３００を基板Ｐに対して平行に移動する。このようなコネクタ装置を水平式コネクタ装置と称する。
【0006】
なお、符号Ｃは同軸ケーブルを示し、各ケーブルＣは、プラグコネクタ３００の端子（プラグコネクタの端子をプラグ側端子と呼称する。）と各々接続されている。プラグコネクタ３００とリセプタクルコネクタ３０２とが接続されると、リセプタクルコネクタ３０２の端子（リセプタクルコネクタの端子をリセ側端子と呼称する。）とプラグ側端子とが接触し、リセプタクルコネクタ３０２が設けられている基板Ｐ上の図示しない電子部品に対し、同軸ケーブルＣを伝搬してきた信号等の電気が流れる。
【0007】
図１２はプラグコネクタ３００をリセプタクルコネクタ３０２に接続した状態の縦断面図である。図１２からわかるように、両コネクタは共に基板Ｐに近接した状態で接続される。
【0008】
このような水平式コネクタ装置に対し、図１３及び図１４に示すように、基板Ｐに取り付けられているリセプタクルコネクタ４０２へ上方からプラグコネクタ４００を移動して両コネクタを接続するコネクタ装置を垂直式コネクタ装置と称する。
【0009】
垂直式コネクタ装置にあっては、リセプタクルコネクタ４０２上にプラグコネクタ４００が載置される（なお、この明細書において上・下とは、例えば各図に正対した場合における上方側及び下方側を指すものとする。また前・後とは、同軸ケーブルＣをプラグコネクタ１００に取り付けた場合における同軸ケーブルＣの延びる方向においてプラグコネクタ１００のある側が前であり、これと反対側が後である。さらに、左・右とは、前方を向いてその左側及び右側ということにする。）。
【0010】
前記水平式コネクタ装置にあっては、基板Ｐに当接されたプラグコネクタ３００に対しリセプタクルコネクタ３０２が基板Ｐに近接した状態で接続されるから、リセプタクルコネクタにプラグコネクタが載置される垂直式コネクタ装置よりも低背化が可能であり、機器の薄型に寄与する。しかし、接続する際に作業者の手指が基板Ｐに接触し、作業の妨げとなったり、配線を損傷してしまったりすることになる。
【0011】
これに対し、垂直式コネクタ装置の場合、プラグコネクタ４００をリセプタクルコネクタ４０２の上方から接続するので、基板Ｐが邪魔になることはなく作業性は良いが、リセプタクルコネクタ４０２にプラグコネクタ４００が積み重なる。このため、両コネクタを接続した時の寸寸法が大きくなり、低背化の点で問題がある。
【0012】

そこで、作業性に優れるばかりか低背化も可能な垂直式コネクタが提案されている（特許文献１参照）。

図１５及び図１６は、そのような垂直式コネクタの接続構造の一例であって、図１５はリセプタクルコネクタ５０２にプラグコネクタ５００を接続する前の状態を示す縦断面図であり、図１６はリセプタクルコネクタ５０２とプラグコネクタ５００とを接続した状態を示す縦断面図である。

【0013】

リセプタクルコネクタ５０２には、上方に開放され、プラグコネクタ５００を上から嵌め込むようになっている嵌合凹部５０３が形成されている。よって、プラグコネクタとリセプタクルコネクタとの接続作業性を良好にできるという垂直式コネクタ装置の長所を維持しつつ、プラグコネクタ５００がリセプタクルコネクタ５０２内に入るため、低背化が可能である。

【0014】

また、リセプタクルコネクタ５０２には、プラグコネクタ５００をリセプタクルコネクタ５０２に接続した時に同軸ケーブルＣの延びを阻害しないように、嵌合凹部５０３に連通する切欠状の開放孔５１０が形成されている（図１５，図１６参照）。このため、嵌合凹部５０３は上方及び後方に開放されることになる。なお、リセプタクルコネクタ５０２のうち開放孔５１０が形成されている部位を、便宜上、ケーブル挿通部といい符号５０２ｂで示す。

【0015】

ところで、リセ側端子５０５とプラグ側端子５０６との電気的接触を確実にできるように、リセ側端子５０５は、プラグ側端子５０６と当接した際に、リセ側端子５０５とプラグ側端子５０６との間で接触圧力を生じる形状とされている。当該接触圧力は、プラグコネクタ５００とリセプタクルコネクタ５０２との接続状態を維持する力（以下、コネクタ接続状態維持力）としても作用する。

【0016】

当該コネクタ接続状態維持力は、リセプタクルコネクタ５０２の嵌合凹部５０３にプラグコネクタ５００を内嵌した時にプラグコネクタ５００をリセプタクルコネクタ５０２のケーブル挿通部５０２ｂの側に押し付けるように作用するが、ケーブル挿通部５０２ｂには前記後方に開く開放孔５１０がある。そして、この開放孔５１０がリセプタクルコネクタ５０２の嵌合凹部５０３と連通していることで、リセプタクルコネクタ５０２は上方及び後方に開放される嵌合凹部５０３を有することから、リセプタクルコネクタ５０２の機械的強度はそれだけ弱い。

【0017】

特に、切欠状の開放孔５１０が形成されているケーブル挿通部５０２ｂ及びその周辺は、プラグコネクタ５００とリセプタクルコネクタ５０２とを接続した際に、前記接触圧力に起因した集中応力が発生する箇所となり、ひずみを生じるようになる。この結果、リセプタクルコネクタ５０２が変形してしまう虞がある。

【0018】

また、接続されたプラグコネクタ５００とリセプタクルコネクタ５０２とに同軸ケーブルＣが上方にこじられて、プラグコネクタ５００とリセプタクルコネクタ５０２との接続を解除する力が作用したとすると、プラグコネクタ５００がリセプタクルコネクタ５０２から外れてしまい、その結果、コネクタ装置の電気的接続に支障を生じることが考えられる。

【特許文献1】特開２００４－３５５８６３

【発明の開示】

【発明が解決しようとする課題】

【0019】

本発明はこのような実情に鑑みて為されたものであり、その解決しようとする課題は、プラグコネクタをリセプタクルコネクタに接続した際に、リセプタクルコネクタにおいて

接続による集中応力が発生する箇所やその周囲の箇所が変形してしまうことを効果的に防止するとともに、プラグコネクタとリセプタクルコネクタとを接続した後に両コネクタにその接続を解除するような力が作用したとしてもプラグコネクタとリセプタクルコネクタとが外れてしまうことを抑制できる新たな技術を提供することにある。

【課題を解決するための手段】

【0020】

そこで、本発明では次の手段を採用した。

すなわち、本発明は、ケーブル及びその一端に接続された端子をハウジングに有するコネクタと、このコネクタが接続される相手方コネクタと、を有するコネクタ装置であって、前記相手方コネクタは、相手方ハウジングと、この相手方ハウジングに設けられ、前記コネクタとの接続の際に前記コネクタの端子と接触し、かつ基板に固定される相手方端子と、前記相手方ハウジングにおいて、前記相手方端子の設置箇所と対向する箇所に前記ケーブルが挿通される部位として形成されたケーブル挿通部と、このケーブル挿通部を前記基板に対して固定する固定手段とを有することを特徴とする。

【0021】

相手方ハウジングのうちケーブル挿通部が形成された部位は、当該挿通部が形成されていない他の部位に比べ強度的に弱い。このため、コネクタを相手方コネクタに接続した際に、相手方コネクタにおいて接続による接触圧力に起因した集中応力が発生する箇所となるが、ケーブル挿通部は固定手段により基板に固定されるので、その強度を高めることができる。

【0022】

また、前記固定手段は、前記ケーブル挿通部に当接又は埋設されて前記ケーブル挿通部を支持する支持部と、この支持部に一体形成され前記基板に半田付けされる固着部とを有することを特徴としてもよい。ケーブル挿通部が支持部によって支持されてその強度が高まるだけでなく、当該強度が高められたケーブル挿通部が固着部により基板に半田付けされるから、ケーブル挿通部は一層、その強度を高められる。

【0023】

前記コネクタ及び前記相手側コネクタのうちの少なくとも一方には、両コネクタの接続の際に他方のコネクタに掛止される掛止部を有するようにしてもよい。掛止部により、コネクタと相手方コネクタとがロックされ、両コネクタが外れないようにできる。

【0024】

さらに掛止部は、前記コネクタ又は前記相手方コネクタに掛止する弾性片であって、前記相手方コネクタ又は前記コネクタには、この弾性片が入る開口が形成されていると好適である。弾性片がコネクタ又は前記相手方コネクタに掛止することで、コネクタと相手方コネクタとの結合が強固になる。そして弾性により、弾性片のコネクタ又は相手方コネクタへの掛止力が高まる。また開口が形成されていると弾性片が開口内に入るため、掛止の度合いが高まりロックが強固になる。

【0025】

また、前記固定手段は、前記コネクタを前記相手方コネクタに接続した際に前記ケーブルを流れるノイズをグランドに流す金属部材からできていると好適である。

さらに、前記相手方ハウジングは、前記ケーブルを流れるノイズをグランドに流す金属板を備え、この金属板に前記固定手段を形成してもよい。

加えて、金属板の一部に前記掛止部を形成することも考えられる。

【発明の効果】

【0026】

本発明によれば、コネクタを相手方コネクタに接続した際に、相手方コネクタにおいて接続による集中応力が発生する箇所であるケーブル挿通部は固定手段により基板に固定されるので、その強度を高められる。この結果、コネクタと相手方コネクタとを接続した時のコネクタ側端子と相手側コネクタ側端子との接触圧力に起因した応力が、相手方コネクタにおいて発生しても、ケーブル挿通部、延いてはハウジングが変形してしまうことを効

果的に抑制できる。

【0027】

また、掛止部により、コネクタと相手方コネクタとがロックされ、両コネクタが外れないようにできるので、コネクタと相手方コネクタとを接続した後に両コネクタにその接続を解除するような力が作用したとしてもコネクタと相手方コネクタとが外れてしまうことを抑制できる。

【0028】

さらに、ケーブルを流れるノイズをグランドに流せるように固定手段を金属板にすることで固定手段の用途が高まる。

【発明を実施するための最良の形態】

【0029】

本発明の実施の形態（以下、実施形態）を添付した図面を参照して説明する。本実施形態では、垂直式コネクタ装置を適用した場合を例示する。

【0030】

垂直式コネクタ装置１は、図１～図３に明らかなように、ケーブル付きプラグコネクタＩのプラグコネクタ１００を、基板Ｐに取着されたリセプタクルコネクタ２０２に嵌合することで接続する。

【0031】

プラグコネクタ１００は、例えば図１，図４，図６等からわかるように、プラグハウジング１０７と、プラグハウジング１０７をカバーすることでハウジング内部の部品を保持するアッパーシェル１１２とを有している。アッパーシェル１１２は、同軸ケーブルＣを流れるノイズをグランドに流すためのものでもあり、金属などの導電性を有する材料からなる。

【0032】

プラグハウジング１０７は、合成樹脂その他の絶縁材料から形成されている。そして、図１からわかるように、プラグハウジング１０７の前面部には、同軸ケーブルＣと接続されるプラグ側端子１２１が複数横並びに配設されている。

【0033】

図４及び図５に示されているように、プラグ側端子１２１は、側面で見て上方に解放された矩形状をしている。そして、プラグコネクタ１００とリセプタクルコネクタ２０２とを接続した際に、リセプタクルコネクタ２０２のリセ側端子２２１と当接するように、プラグ側端子１２１は、その一部がプラグハウジング１０７の前面に露出されている。

【0034】

同軸ケーブルＣは、図４に示すように、中心に位置する内部導体Ｃ２を内部絶縁体Ｃ４で被覆してなる信号線Ｃ６と、信号線Ｃ６に多数の金属線を縦添えにしたり、横巻き状又は網状等の形態にしたりして覆設する外部導体Ｃ８と、この外部導体Ｃ８を被覆する外部絶縁体Ｃ１０とからなる。

【0035】

そして、プラグ側端子１２１と接続される同軸ケーブルＣの先端部Ｃａは、外部絶縁体Ｃ１０及び外部導体Ｃ８が共に剥離されて信号線Ｃ６が露出された部位と、その直後に位置し外部絶縁体Ｃ１０が残っている残皮部分Ｃ１０ａと、残皮部分Ｃ１０ａの直後に位置し外部絶縁体Ｃ１０のみが剥離され外部導体Ｃ８が露出された部位とからなる。

【0036】

またプラグハウジング１０７には、上方及び後方に開口する凹部１１６が形成され（図４，図５参照）、凹部１１６には、複数の同軸ケーブルＣの先端部Ｃａを横断状に交差した状態で保持する第１ケーブル保持具１０８，第２ケーブル保持具１１０が内嵌されている。

【0037】

第１ケーブル保持具１０８は、凹部１１６の前方に取付けられた板状体であり（図４，図５，図６参照）、第１ケーブル保持具１０８がプラグハウジング１０７に取り付けられ

ると、同軸ケーブルＣの信号線Ｃ６の内部絶縁体Ｃ４を上から押圧した状態で保持する（図４，図５参照）。信号線Ｃ６を第１ケーブル保持具１０８で保持するに当り、第１ケーブル保持具１０８を凹部１１６に取付けると、その時の押圧力により、同軸ケーブルＣの内部絶縁体Ｃ４が、プラグ側端子１２１との圧接により破れて内部導体Ｃ２を露出し、露出した内部導体Ｃ２とプラグ側端子１２１とが電気的に接続される。

【0038】

第２ケーブル保持具１１０は、導電性に優れた金属からなる横断面形状が逆Ｕ字状をした中空棒状体であり（図４，図５及び図６参照）、第１ケーブル保持具１０８の後方に位置する。そして、第２ケーブル保持具１１０を凹部１１６に取付けると、その時の押圧力により、同軸ケーブルＣの先端部Ｃａにおける外部導体Ｃ８とその直後に位置する外部絶縁体Ｃ１０とを、プラグハウジング１０７とにより上下で挟持する（図４，図５及び図６参照）。

【0039】

さらにプラグハウジング１０７は、凹部１１６内の第２ケーブル保持具１１０に対向する箇所に良導体１１９（図４，図５参照）を有する。良導体１１９は、金属などの導電性に優れた材料からできており、プラグハウジング１０７に一体成形され、全ての同軸ケーブルＣの外部導体Ｃ８と電気的に接触されている。

【0040】

また、図４及び図５に示されるように、プラグコネクタ１００をリセプタクルコネクタ２０２に接続したとき、良導体１１９は後述する金属板２０９の後縁面２１３Ｒに当接する。後縁面２１３Ｒについてはリセプタクルコネクタ２０２の説明で詳述する。なお、良導体１１９は、プラグハウジング１０７に必ずしも一体成形されなくてもよく、圧入や接着によって配設されてもよい。

【0041】

プラグハウジング１０７をカバーするアッパーシェル１１２は、図６に示すように、矩形状の上壁１１２Ｕと、この上壁１１２Ｕに対してＬ字形に折り曲げられた左右の側壁１１２Ｌ・１１２Ｒとを有し、上壁１１２Ｕ及び側壁１１２Ｌ・１１２Ｒでプラグハウジング１０７の上面，側面及び下面の一部を保持する。

【0042】

前記側壁１１２Ｌ・１１２Ｒには、係止窓ｈ２が形成されている（図１，図２及び図６参照）。係止窓ｈ２は、プラグハウジング１０７の両側縁に設けられかつ側方へ突出する係合子ｈ１と、アッパーシェル１１２でプラグハウジング１０７をカバーした時に係合される。係止窓ｈ２と係合子ｈ１とが係合することで、アッパーシェル１１２のプラグハウジング１０７からの抜けを防止する。

【0043】

また、前記上壁１１２Ｕには、内側に折り曲げられた一対の曲げ片１１２ａが形成されている。

一対の曲げ片１１２ａは、アッパーシェル１１２でプラグハウジング１０７をカバーした時に第２ケーブル保持具１１０に当接することにより（図５参照）、同軸ケーブルＣの外部導体Ｃ８を流れるノイズを、第２ケーブル保持具１１０を介して、アッパーシェル１１２からやがてグランドに流すためのものである。ノイズを除去するルートについては、作用効果の項で詳しく説明する。

【0044】

さらに、上壁１１２Ｕの後端縁の左右両端部は、Ｌ字形に折り曲げられた折曲部１１２ｅがそれぞれ形成されている（図６参照）。

折曲部１１２ｅは、その後面に符号１１４で示す開口が形成されている（図２，図６，図８～図１０参照）。

【0045】

アッパーシェル１１２の上壁１１２Ｕの後端縁のうち、折曲部１１２ｅの間の部分は、折曲部１１２ｅよりも短めに下方に折り曲げられた一対の下向き片１１２ｆとされている

（図２，図４，図６等参照）。
下向き片１１２ｆを形成することにより、アッパーシェル１１２の上壁１１２Ｕの後縁中央部には、切欠き部１１３が形成される（図２，図４，図６等参照）。
【0046】
なお、同軸ケーブルＣをプラグコネクタ１００に取り付けるにあたり、同軸ケーブルＣは、予めその先端部Ｃａの外皮が剥離され、信号線Ｃ６と外部導体Ｃ８とが露出された状態にある（図４，図５参照）。
信号線Ｃ６にとっての外皮は外部導体Ｃ８と外部絶縁体Ｃ１０であり、外部導体Ｃ８にとっての外皮は外部絶縁体Ｃ１０である（図４，図５参照）。
【0047】
次に、図１～図５等を参照して、リセプタクルコネクタ２０２について述べる。
リセプタクルコネクタ２０２は、その全体形状が扁平直方体形状のリセプタクルハウジング２０７と、リセプタクルハウジング２０７に配設された金属板２０９とからなる。
【0048】
リセプタクルハウジング２０７は、合成樹脂その他の絶縁材料から形成されている。そして、リセプタクルハウジング２０７の中央部には、プラグコネクタ１００が内嵌される嵌合凹部２０３を有する。
【0049】
嵌合凹部２０３は、前方及び後方に位置する一対の前方長縁壁２０４Ｆ・後方長縁壁２０４Ｒと、これら長縁壁２０４Ｆ・２０４Ｒを連結する左方短縁壁２０５Ｌ・右方短縁壁２０５Ｒと、底板２０６とにより囲繞されて形成されるものであり、後方長縁壁２０４Ｒの中央部には、嵌合凹部２０３に連通する切欠状で矩形の開放孔２３２が形成されている。それ故、嵌合凹部２０３は、上方及び後方に開放されるようになる（例えば図１及び図３参照）。
【0050】
開放孔２３２は、プラグコネクタ１００をリセプタクルコネクタ２０２に接続した時に同軸ケーブルＣの延びを阻害しないようにするためのものである。開放孔２３２の長さ寸法は、ケーブル付きプラグコネクタＩのケーブル幅よりもわずかに大きめに形成されている。開放孔２３２が形成されている後方長縁壁２０４Ｒをケーブル挿通部ということにする。
【0051】
嵌合凹部２０３の平面形状は、次に詳述する前記金属板２０９の形状に左右される。なお、金属板２０９を明示するため、図中、金属板２０９には、グラデーションを付してある。
【0052】
図７に示すように、金属板２０９は、平面形状で長四角形状をしており、その中央は大きく開口する。そして、対向する一対の長辺が折り曲げられて、端面形状が扁平逆Ｕ字形をしている形状体であり（なお前記開口を符号２１１ａで示す。）、開口２１１ａを有する主面２１１と、前縁面２１３Ｆと、後縁面２１３Ｒとからなる。開口２１１ａは打抜き加工により形成され、主面２１１のうち、一方の長縁を除く他の長縁及び残りの短縁は、所定幅を有する残留部とされ、それぞれ前方残留部２１１Ｆ，左残留部２１１Ｌ及び右残留部２１１Ｒで示す。
【0053】
前方残留部２１１Ｆには、その両端近傍に矩形状の切り欠き２１２Ｌ・２１２Ｒが形成され、当該切り欠き２１２Ｌ・２１２Ｒの間は中央部２１２Ｍとされている。
また、左残留部２１１Ｌ及び右残留部２１１Ｒのほぼ中央部には、内側に垂れ下がった耳片２１５がそれぞれ対向する位置に形成されている。
【0054】
左右の耳片２１５は、リセプタクルコネクタ２０２とプラグコネクタ１００とを接続したときにプラグコネクタ１００のアッパーシェル１１２の左右の側壁１１２Ｌ・１１２Ｒ

と当接する部分であり（図２及び図３参照）、耳片２１５を押圧すると弾撓する。
　また、金属板２０９の後縁面２１３Ｒは、その中央部が上方に開放された矩形状の切り欠き２１７が打抜き形成され、後縁面２１３Ｒの両端部にはそれぞれ内側に折り曲げられた内曲片２１９が形成されている。
【0055】
　切り欠き２１７は、リセプタクルハウジング２０７の後方長縁壁２０４Ｒの開放孔２３２と合致するようにその大きさ及び形状が決められている。後縁面２１３Ｒは、後方長縁壁２０４Ｒを補強してその強度を高めるためのものである。
【0056】
　また内曲片２１９は、図８からわかるように内側に折り曲げられた一端固定他端自由な片持ち梁状の金属片であるから、プラグコネクタ１００をリセプタクルコネクタ２０２に接続した際に先端側に外力を受けると弾性を生じるようになる。また内曲片２１９は、プラグコネクタ１００をリセプタクルコネクタ３０２に接続した際に、アッパーシェル１１２の前記折曲部１１２ｅに形成された開口１１４と対向する位置関係にある。よってプラグコネクタ１００をリセプタクルコネクタ３０２に接続すると、内曲片２１９は、前記弾性により開口１１４に掛止する。よって内曲片２１９は掛止部（弾性片）といえる。
【0057】
　そして、金属板２０９の後縁面２１３Ｒの下縁のうち前記切り欠き２１７の両端部に対する箇所には、外方に折り曲げられた一対の外曲片２２２が一体形成されている。後縁面２１３Ｒのうち外曲片２２２を含む部分の横断面形状は、図４に示した状態で見るとＬの字を横倒しにした如き形状をしている。
【0058】
　このような形態の金属板２０９が配設されるリセプタクルハウジング２０７は、金属板２０９の後縁面２１３Ｒがリセプタクルハウジング２０７の後方長縁壁２０４Ｒの内面と対向し、金属板２０９の前縁面２１３Ｆがリセプタクルハウジング２０７の前方長縁壁２０４Ｆと対向し、金属板２０９の両端がリセプタクルハウジング２０７の左方短縁壁２０５Ｌ及び右方短縁壁２０５Ｒとそれぞれ対向する状態になるように、金属板２０９を合成樹脂その他の絶縁材料によって封止する一体成形により形成される。
【0059】
　なお、金属板２０９は必ずしも一体成形で配設されなくてもよく、リセプタクルハウジング２０７への圧入や接着によって配設してもよい。要するにリセプタクルハウジング２０７と金属板２０９とは当接状態にあればよい。また、後縁面２１３Ｒは、リセプタクルハウジング２０７の後方長縁壁２０４Ｒの外面と当接されるようにしても、後方長縁壁２０４Ｒに埋設されるようにしてもよい。
【0060】
　そして、金属板２０９が配設されているリセプタクルハウジング２０７の後方長縁壁２０４Ｒのうち内曲片２１９に対する箇所は開口２２３が形成され（図２，図３参照）、一対の外曲片２２２に対する箇所は下方及び後方に開口された凹部２２４（図２，図３参照）が形成されている。
【0061】
　また、リセプタクルハウジング２０７の前方長縁壁２０４Ｆのうち、金属板２０９の中央部２１２Ｍに対する箇所は、側面で横倒しＳ字形状をしたリセ側端子２２１を、リセプタクルハウジング２０７の長縁に沿って並列できるように成形されている（図２，図４及び図５参照）。当該箇所をリセ側端子配置箇所といい符合２０４Ｆｍで示す。
【0062】
　リセ側端子配置箇所２０４Ｆｍに配列されるリセ側端子２２１の数は、プラグ側端子１２１の数と同じである。
　そして、これら複数のリセ側端子２２１が並列されたリセ側端子配置箇所２０４Ｆｍの長さ寸法（左右方向における寸法）にほぼ合致して、リセプタクルハウジング２０７の後方長縁壁２０４Ｒに形成された前記開放孔２３２の長さが設定されている。

【0063】
また、プラグコネクタ１００とリセプタクルコネクタ２０２とを接続すると、リセ側端子２２１とプラグ側端子１２１とが当接し、リセ側端子２２１がプラグ側端子１２１からの押圧力により圧縮され、前後方向に押し縮められるようになる（図４，図５参照）。そして、リセ側端子２２１はその形状がＳ字形状であるが故、押し縮められると弾性を生じるようになり、プラグ側端子１２１との間で接触圧力を生じる。当該接触圧力は、コネクタ接続状態維持力として作用し、プラグコネクタ１００とリセプタクルコネクタ２０２との接続状態を維持する。
【0064】
次にこのようなプラグコネクタ１００とリセプタクルコネクタ２０２とからなる垂直式コネクタ装置１の作用効果について説明する。
プラグコネクタ１００とリセプタクルコネクタ２０２とを接続する前にリセプタクルコネクタ２０２を基板Ｐに取着する。この取着にあたり、リセ側端子２２１と基板Ｐとを半田付けすると共に、一対の外曲片２２２を基板Ｐに半田付けして固着（固定）する。
【0065】
このようにすることで、プラグコネクタ１００をリセプタクルコネクタ２０２に接続した際に同軸ケーブルＣの外部導体Ｃ８を伝搬するノイズや、基板Ｐ及びその周辺に接続されている電気／電子部品から発生し、信号へ影響を与えるノイズは、外部導体Ｃ８－第２ケーブル保持具１１０－アッパーシェル１１２の一対の曲げ片１１２ａ－上壁１１２Ｕ－左右の側壁１１２Ｌ・１１２Ｒ－金属板２０９の左右の耳片２１５－金属板２０９の左残留部２１１Ｌ（又は右残留部２１１Ｒ）－後縁面２１３Ｒ－外曲片２２２－基板Ｐの図示しないグランドラインというルートで除去される。
【0066】
また、プラグコネクタ１００をリセプタクルコネクタ２０２に接続したときに、内曲片２１９は図１０に示すようにアッパーシェル１１２の折曲部１１２ｅと接触している。このため、内曲片２１９経由でもプラグコネクタ１００をリセプタクルコネクタ２０２に接続したときに同軸ケーブルＣの外部導体Ｃ８を伝搬するノイズは、基板Ｐに落とされる。その場合の経路は、外部導体Ｃ８－第２ケーブル保持具１１０－アッパーシェル１１２の一対の曲げ片１１２ａ－アッパーシェル１１２の折曲部１１２ｅ－金属板２０９の内曲片２１９－後縁面２１３Ｒ－外曲片２２２－基板Ｐのグランドラインである。
【0067】
さらにこれらのルート以外に同軸ケーブルＣの外部導体Ｃ８を流れる前記ノイズを除去するルートは、外部導体Ｃ８－良導体１１９－一対の外曲片２２２－基板Ｐのグランドラインというルートがある。
【0068】
同軸ケーブルＣの外部導体Ｃ８と外曲片２２２との距離が短いほど、信号への影響を少なくすることができ、この結果、信号への影響を抑制できる。その意味では最後のルートが前二者のルートよりも短い。
上記の説明より、アッパーシェル１１２、金属板２０９及び良導体１１９は、同軸ケーブルＣを流れるノイズをグランドに流すためのものとなる。
【0069】
そして、プラグコネクタ１００をリセプタクルコネクタ２０２の嵌合凹部２０３に嵌め込むと、Ｓ字のリセ側端子２２１が弾性変形し（図４，図５参照）、プラグ側端子１２１とリセ側端子２２１との間で接触圧力を生じる。
【0070】
当該接触圧力によりプラグコネクタ１００はその全体が後方長縁壁２０４Ｒの側に移動されるようになり、その時の押圧力によって後方長縁壁２０４Ｒを撓ませるようになる。また後方長縁壁２０４Ｒには、開放孔２３２が形成されているから、後方長縁壁２０４Ｒには集中応力が生じるようになる。
【0071】

しかし、リセプタクルハウジング２０７の後方長縁壁２０４Ｒには、後方長縁壁２０４Ｒを補強してその強度を高める金属板２０９の後縁面２１３Ｒが支持部として機能する。よって、後方長縁壁２０４Ｒに開放孔２３２が形成されていても後方長縁壁２０４Ｒの強度を高められる。

【0072】

また、後縁面２１３Ｒには、その一部分である一対の外曲片２２２が基板Ｐに半田付けして固着されているので、プラグコネクタ１００とリセプタクルコネクタ２０２とを接続した時のプラグ側端子１２１とリセ側端子２２１との接触圧力に起因した集中応力が、リセプタクルハウジング２０７の後方長縁壁２０４Ｒに生じても、一対の外曲片２２２を介して、後方長縁壁２０４Ｒを基板Ｐに固定できるので、後方長縁壁２０４Ｒは、開放孔２３２の有無に拘らずがその強度を高めることができる。この結果、後方長縁壁２０４Ｒ、延いては、リセプタクルハウジング２０７が変形してしまうことを効果的に抑制できる。この関係で、外曲片２２２を含む後縁面２１３Ｒは、後方長縁壁２０４Ｒを基板Ｐに対して固定する固定手段といえる。

【0073】

また、一対の外曲片２２２は、金属板２０９の一部であって、金属板２０９は、リセプタクルハウジング２０７内に配設されているので、後方長縁壁２０４Ｒの強度を高めるために一対の外曲片２２２を別途用意する必要もなく作業性が向上し、また部品点数を削減できる。

【0074】

さらに、内曲片２１９は、プラグコネクタ１００をリセプタクルコネクタ２０２に接続した際に、アッパーシェル１１２の前記折曲部１１２ｅに形成された開口１１４と掛止されるので、プラグコネクタ１００と、リセプタクルコネクタ２０２とのロックが強固になる（図８及び図９参照）。

【0075】

よって、接続されたプラグコネクタ１００とリセプタクルコネクタ２０２とに同軸ケーブルＣが上方にこじられて、プラグコネクタ１００とリセプタクルコネクタ２０２との接続を解除する力が作用しても、プラグコネクタ１００がリセプタクルコネクタ２０２から外れてしまうことを抑制できる。

【0076】

この結果、電気的接続に支障を生じることもない。

また、開口１１４があると、内曲片２１９がプラグコネクタ１００に深く入り込み易くなり、ロックが強固になる（図１０参照）。

【0077】

加えて、本発明は、上述の図示例にのみ限定されるものではなく、本発明の要旨を逸脱しない範囲内において種々変更を加え得ることは勿論である。

例えば、上述の実施形態では、内曲片２１９をリセプタクルコネクタ２０２に設け、内曲片２１９が掛止する開口１１４をプラグコネクタ１００に設けたものを開示したが、内曲片２１９及び開口１１４の設置箇所を入れ替え、プラグコネクタ１００に内曲片２１９を設け、リセプタクルコネクタ２０２に開口１１４を設けることもできる。

【0078】

そして、この実施形態では、外曲片２２２が金属板２０９の一部として形成されているものを開示したが、外曲片２２２を金属板２０９とは別の金属部材とし別個に設け、当該外曲片２２２をケーブルＣを流れるノイズをグランドに流し、かつ単独で、後方長縁壁２０４Ｒを基板Ｐに取り付けるための固定手段にすることもできる。

【0079】

加えて、外曲片２２２を有する後縁面２１３Ｒを金属板２０９の一部ではなく、別の金属部材として設けてもよい。

さらに、アッパーシェル１１２と電気的に接続されている金属板２０９の一部に基板Ｐと電気的に接続するグランド端子を設け、当該グランド端子を介してケーブルＣを流れる

ノイズの除去に適用させてもよい。

【0080】

また、垂直式コネクタだけでなく、水平式コネクタ装置に適用することもできる。水平式コネクタ装置にあっても、そのコネクタを相手方コネクタに接続した際に相手方コネクタにおいて接続によるプラグ側端子とリセ側端子との接触圧力による集中応力が発生する箇所はあり得る。したがって、当該箇所を固定手段により基板に対して固着すれば、当該集中応力が発生する箇所を基板に対して固定できるので、その強度を高めることができる。したがって、当該集中応力が発生する箇所やその周囲の変形を抑制することができる。

【図面の簡単な説明】

【0081】

【図1】本発明に係る垂直式コネクタ装置のリセプタクルコネクタ及びプラグコネクタを接続する前の状態を斜め上前方から見た分解斜視図である。

【図2】本発明に係るコネクタ装置のリセプタクルコネクタ及びプラグコネクタを接続する前の状態を斜め上後方から見た分解斜視図である。

【図3】図２の状態のリセプタクルコネクタ及びプラグコネクタを接続した状態を示す斜視図である。

【図4】図１のＡ－Ａ線断面図である。

【図5】図３のＢ－Ｂ線断面図である。

【図6】プラグコネクタのハウジングにアッパーシェルをカバーする前の状態を示す斜視図である。

【図7】金属板を斜め上後方から見た斜視図である。

【図8】図１のＣ－Ｃ線断面図である。

【図9】図３のＤ－Ｄ線に沿った断面図である。

【図10】図９の要部拡大図である。

【図11】従来技術を説明するための図であって、水平式コネクタ装置のプラグコネクタをリセプタクルコネクタに接続する前の状態を示す斜視図である。

【図12】図１１の状態のリセプタクルコネクタ及びプラグコネクタを組み付けた状態での縦断面である。

【図13】垂直式コネクタ装置のプラグコネクタをリセプタクルコネクタに接続する前の状態の縦断面図である。

【図14】図１３リセプタクルコネクタ及びプラグコネクタを組み付けた状態を示す縦断面である。

【図15】従来技術を説明するための図であって、別の垂直式コネクタ装置のプラグコネクタをリセプタクルコネクタに接続する前の状態を示す斜視図である。

【図16】図１５のリセプタクルコネクタ及びプラグコネクタを組み付けた状態を示す縦断面である。

【符号の説明】

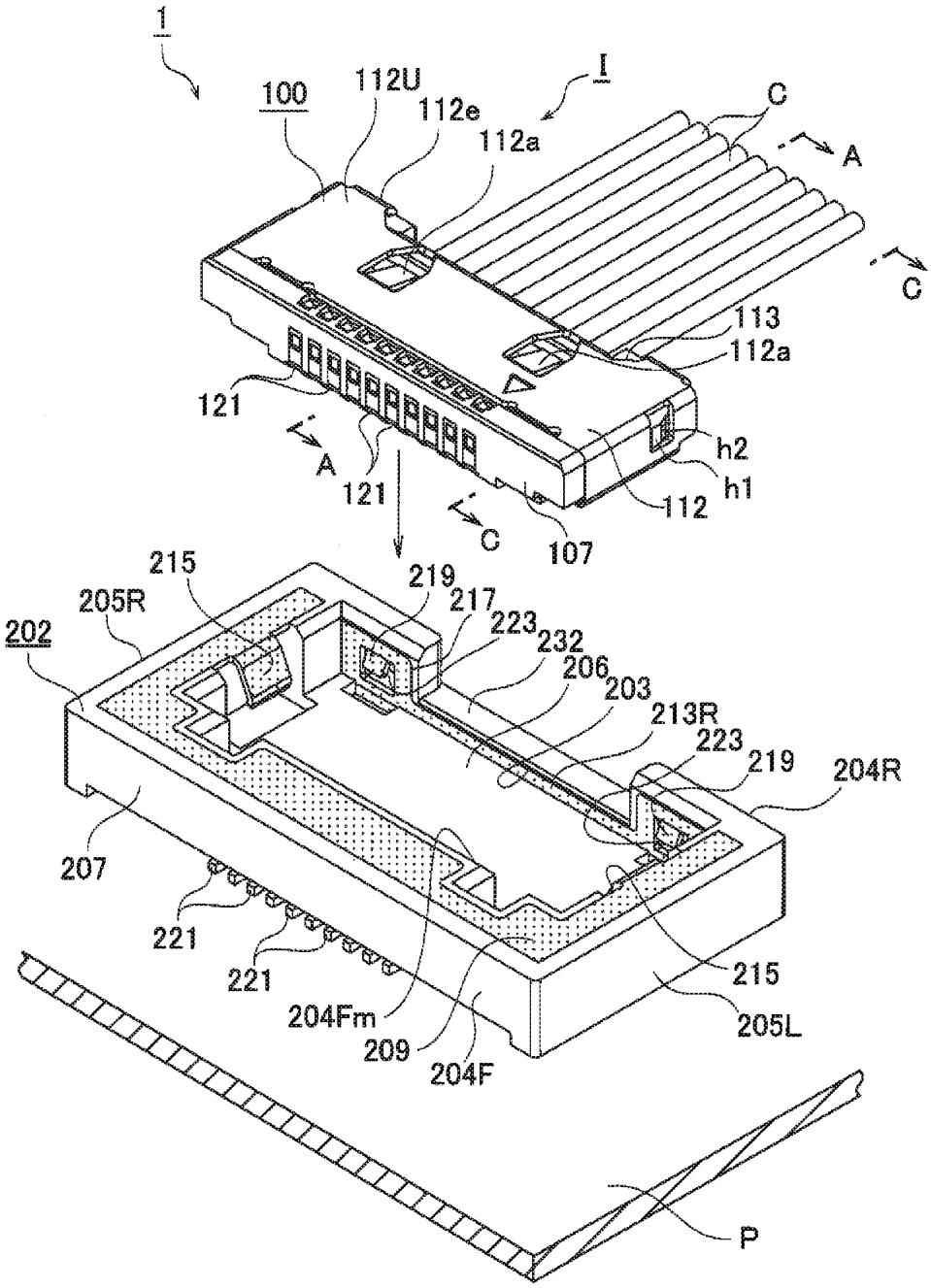
【0082】

１　垂直式コネクタ装置
１００　プラグコネクタ（コネクタ）
１０７　プラグハウジング（ハウジング）
１０８　第１ケーブル保持具
１１０　第２ケーブル保持具
１１２　アッパーシェル
１１２Ｌ　左側壁
１１２Ｒ　右側壁
１１２Ｕ　上壁
１１２ａ　曲げ片
１１２ｅ　折曲部
１１２ｆ　下向き片

１１３　切欠き部
１１４　開口
１１６　凹部
１１９　良導体
１２１　プラグ側端子（端子）
２０２　リセプタクルコネクタ（相手方コネクタ）
２０３　嵌合凹部
２０４Ｆ　前方長縁壁
２０４Ｆｍ　リセ側端子配置箇所
２０４Ｒ　後方長縁壁（集中応力が発生する箇所，ケーブル挿通部）
２０５Ｌ　左方短縁壁
２０５Ｒ　右方短縁壁
２０６　底板
２０７　リセプタクルハウジング（相手方ハウジング）
２０９　金属板
２１１　主面
２１１Ｆ　前方残留部
２１１Ｌ　左残留部
２１１Ｒ　右残留部
２１１ａ　主面の開口
２１２Ｍ　中央部
２１２　Ｌ　切り欠き
２１２Ｒ　切り欠き
２１３Ｆ　前縁面
２１３Ｒ　後縁面（固定手段，支持部）
２１５　耳片
２１７　切り欠き
２１９　内曲片（弾性片，掛止部）
２２１　リセ側端子（相手方端子）
２２２　外曲片（固着部，固定手段）
２２３　開口
２２４　凹部
２３２　開放孔
３００　プラグコネクタ
３０２　リセプタクルコネクタ
４００　プラグコネクタ
４０２　リセプタクルコネクタ
５００　プラグコネクタ
５０２　リセプタクルコネクタ
５０２ｂ　ケーブル挿通部
５０３　嵌合凹部
５０５　リセ側端子
５０６　プラグ側端子
５１０　開放孔
Ｃ　同軸ケーブル
Ｃ１０　外部絶縁体
Ｃ１０ａ　残皮部分
Ｃ２　内部導体
Ｃ４　内部絶縁体
Ｃ６　信号線

Ｃ８　外部導体
Ｃａ　同軸ケーブルの先端部
１　ケーブル付きプラグコネクタ
Ｐ　基板
ｈ１　係合子
ｈ２　係止窓

【図1】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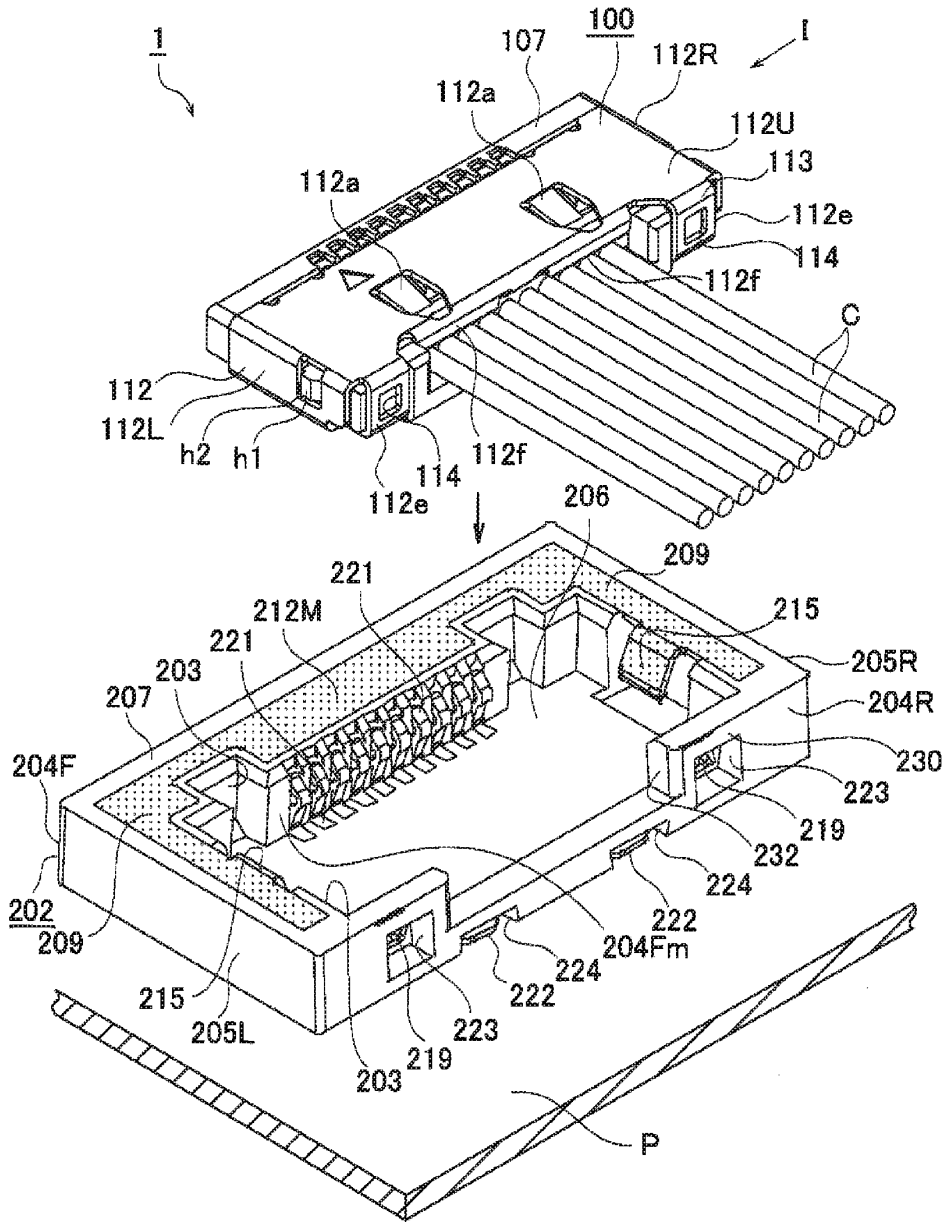
100
112U
112e
112a
I
C
A
C
113
112a
121
A
121
h2
h1
112
C
107
215
205R
219
217
223
232
206
203
213R
223
219
204R
202
207
221
221
204Fm
209
204F
215
205L
P

【図2】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I
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112U
113
112a
112e
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112f
C
112
112L
h2
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112f
112e
206
209
221
212M
215
221
205R
203
204R
207
230
204F
223
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232
224
202
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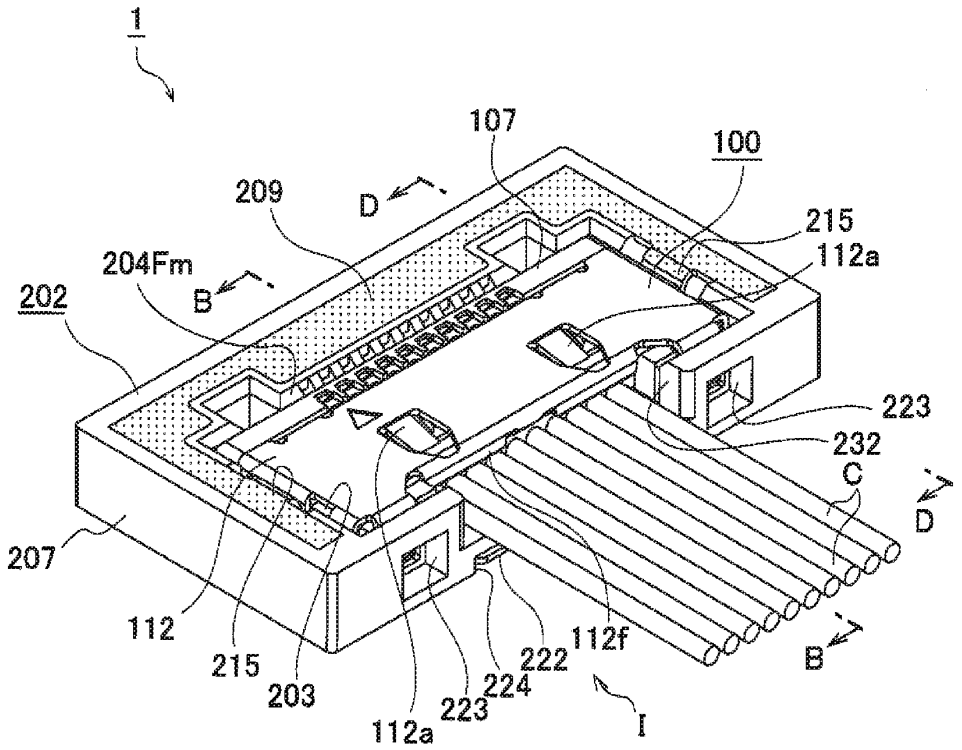
222
204Fm
224
222
215
205L
223
219
203
P

【図３】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100
209
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215
112a
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215
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112a
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224
222
112f
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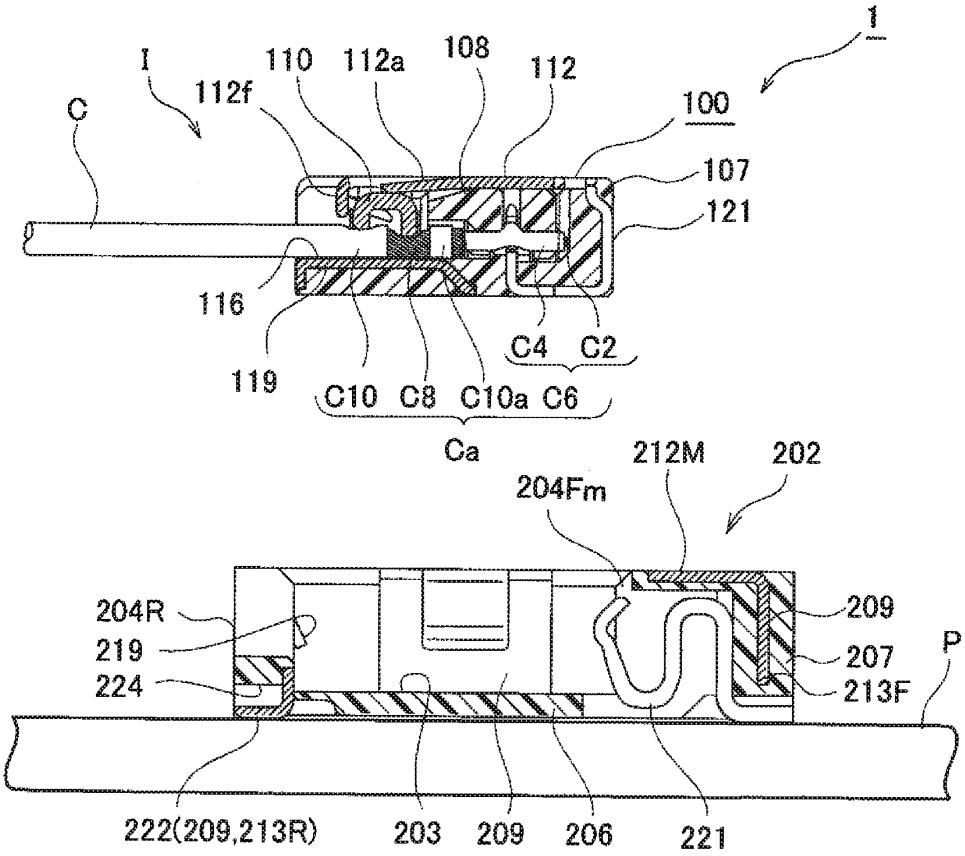
【図4】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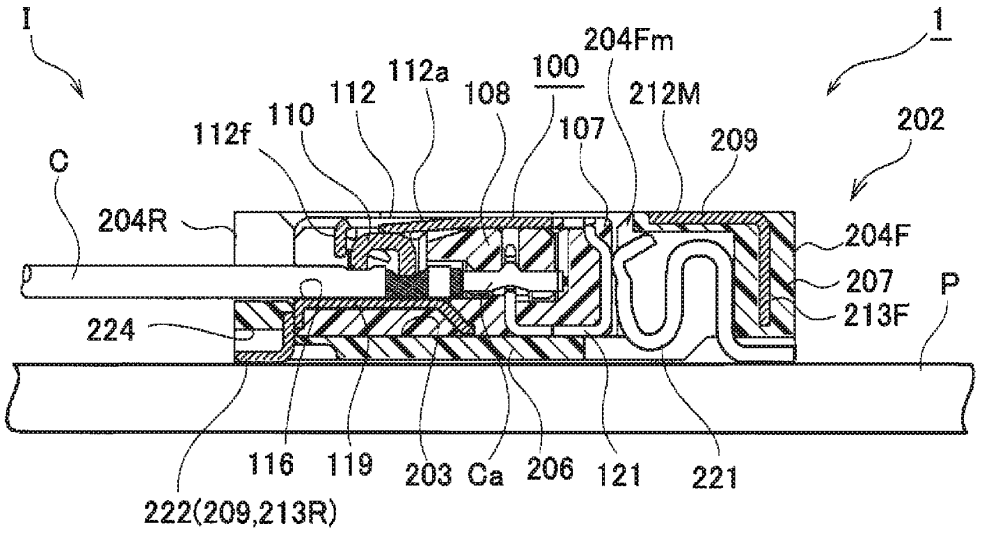
112a
108
112
112f
C
100
107
121
116
119
C10
C8
C10a
C6
C4
C2
Ca
212M
202
204Fm
204R
219
224
209
207
213F
P
222(209,213R)
203
209
206
221

【図5】


I
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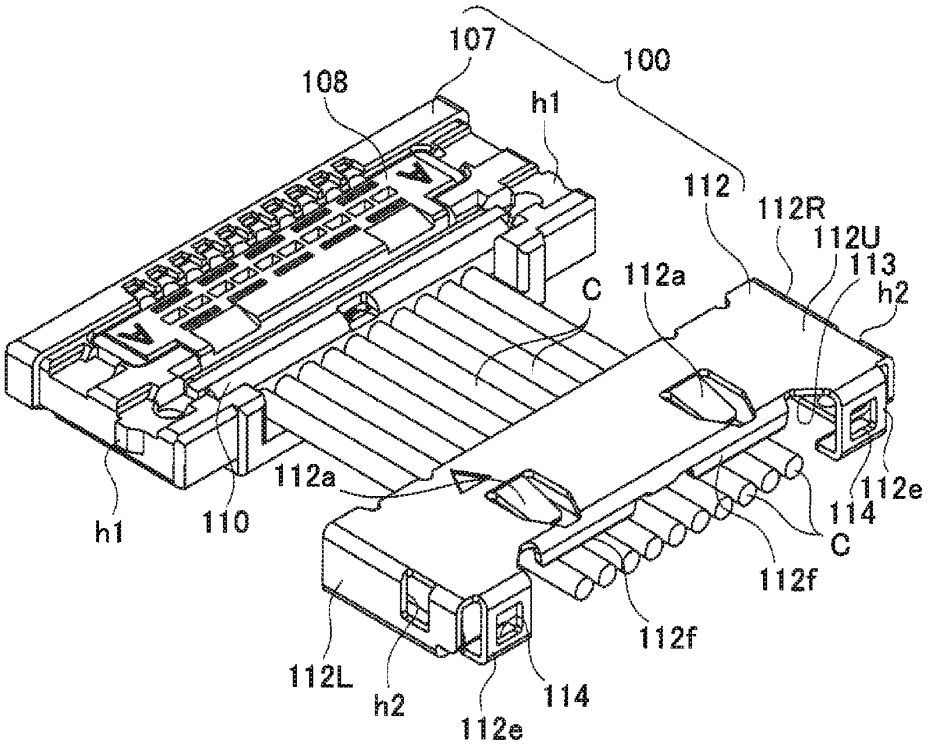
204Fm
112a
100
112
110
108
212M
112f
107
209
202
C
204R
204F
207
213F
P
224
116
119
203
Ca
206
121
221
222(209,213R)

【図6】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112
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114
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112L
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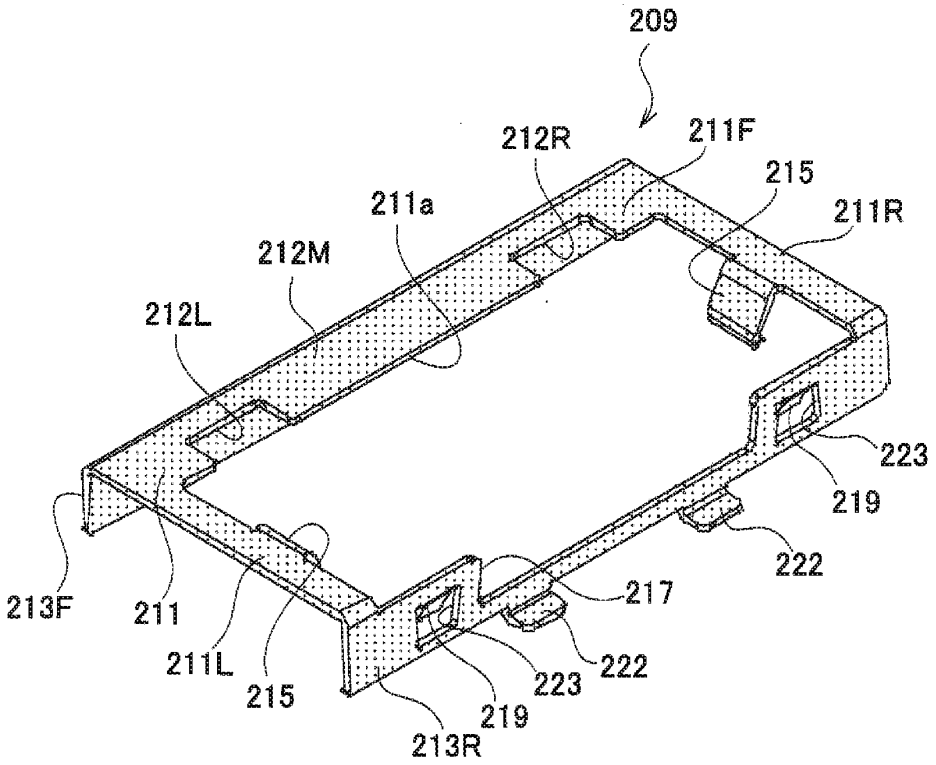
114
112e

【図7】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211F
215
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211a
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212L
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222
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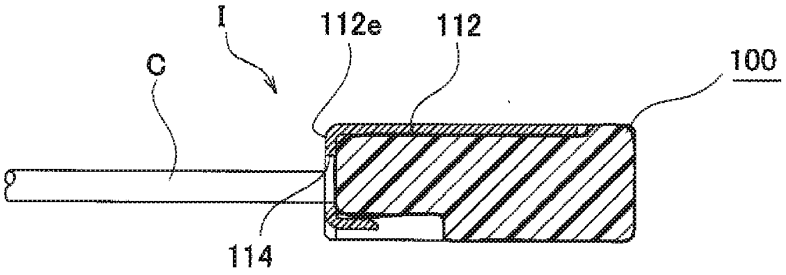
213F
211
211L
215
223
222
219
213R

【図8】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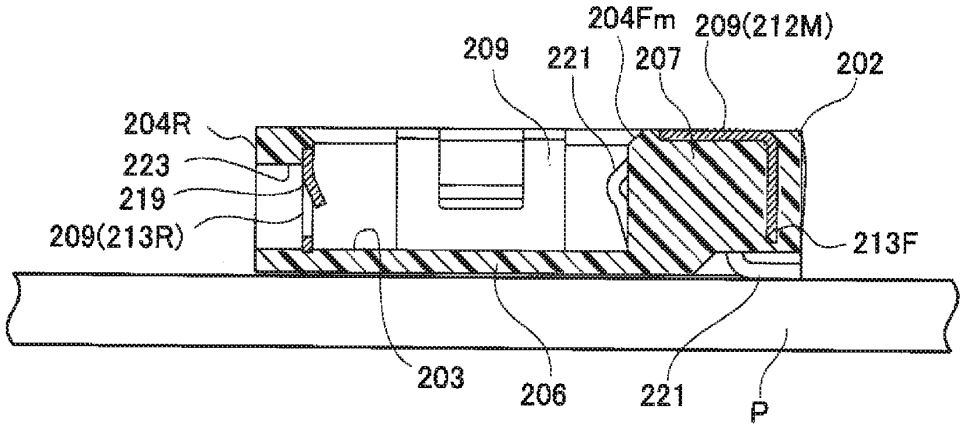
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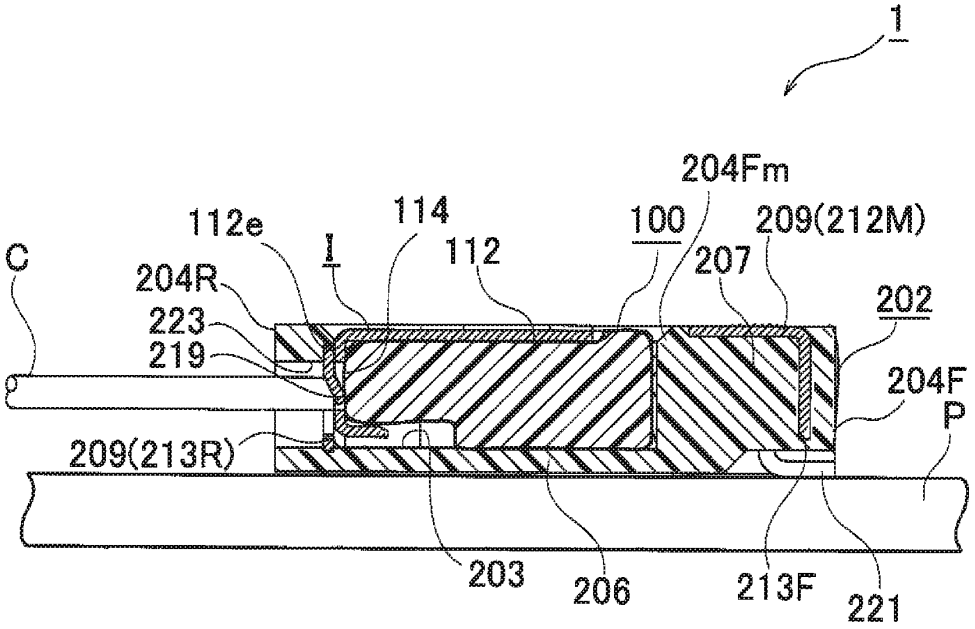
【図9】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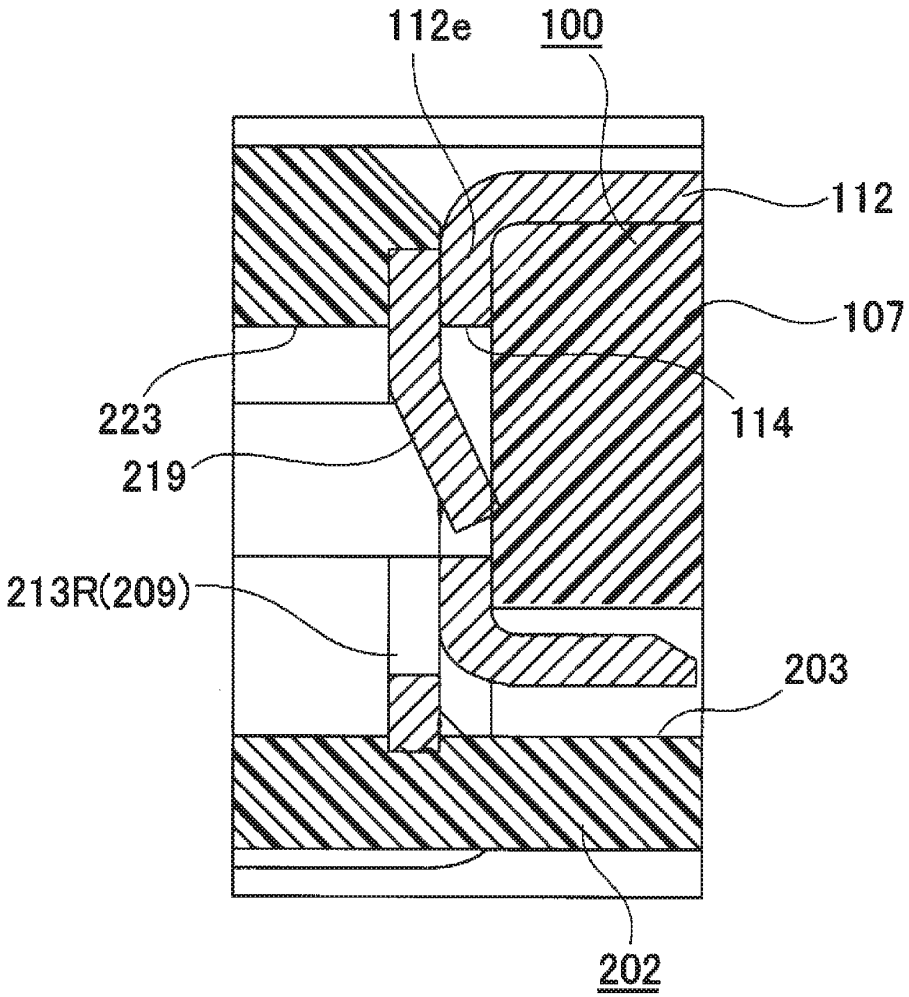
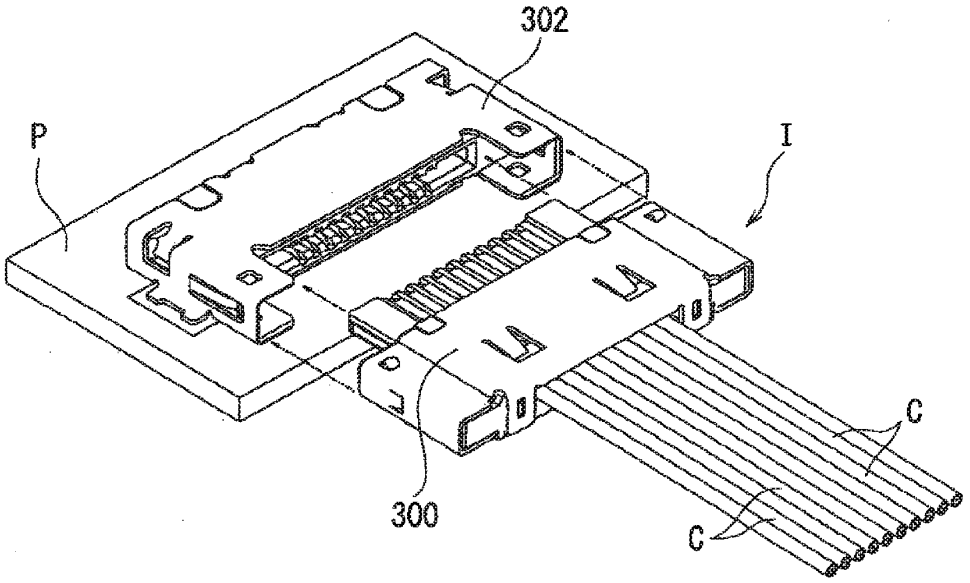
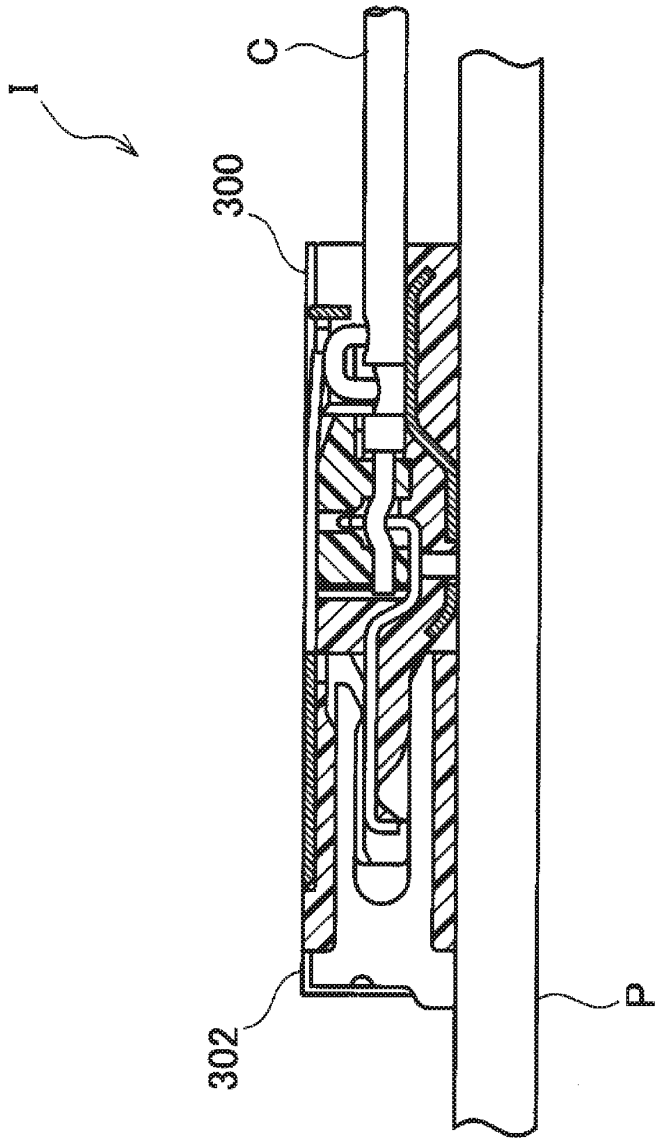
【図10】



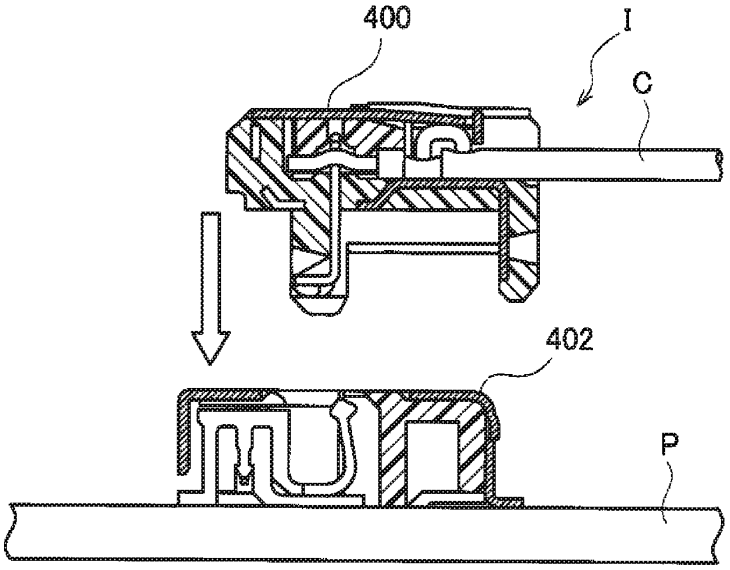
【図11】



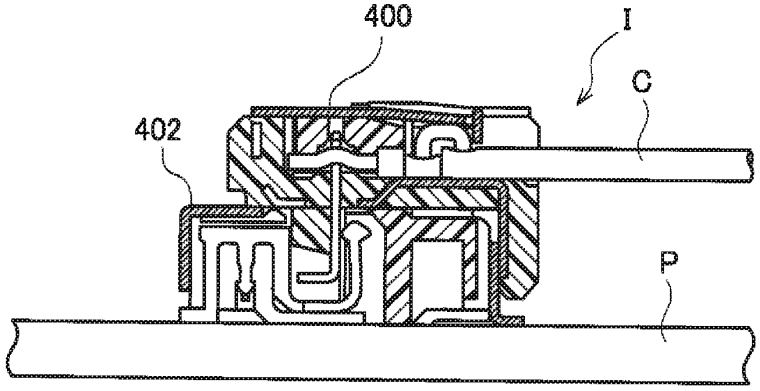
【図12】



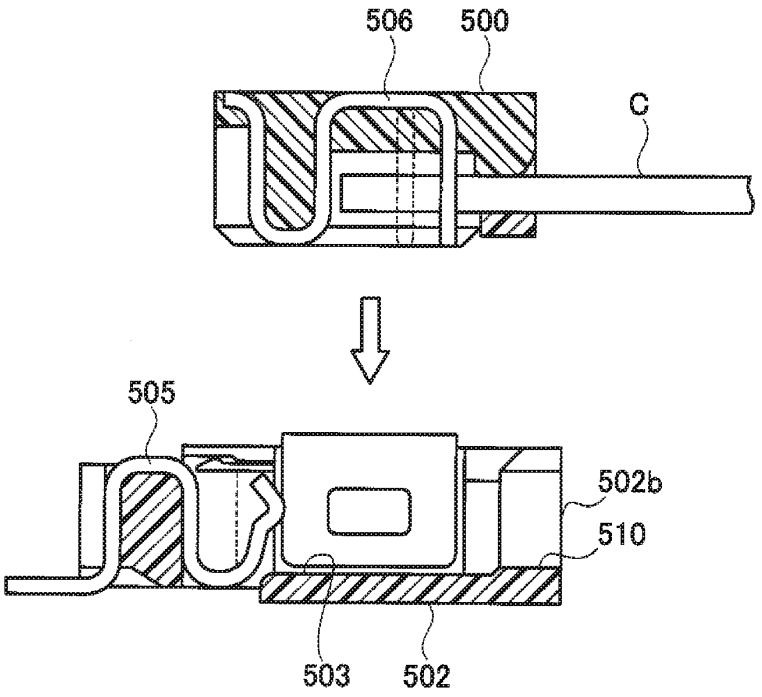
【図13】



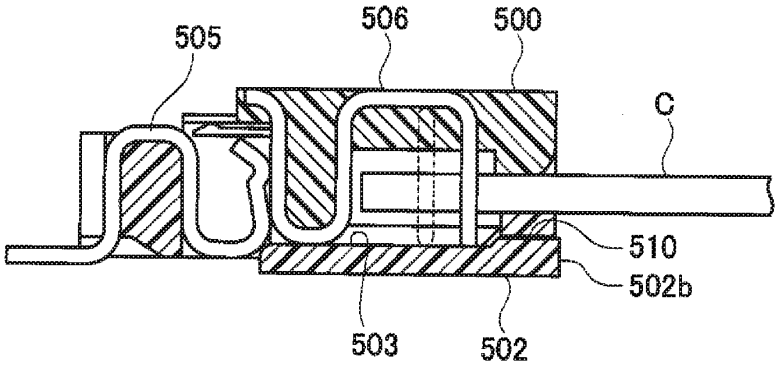
【図14】



【図15】



【図16】



Ｆターム(参考) 5E021 FA05 FA14 FA16 FB11 FC08 FC19 LA06 LA09 LA15
5E023 AA04 BB02 BB10 CC26 EE04 EE07 GG02 GG08 HH12 HH22

PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

To:
WALSH, EDMUND J.

WOLF, GREENFIELD & SACKS, P.C. 600 ATLANTIC AVENUE BOSTON MA 02210-2206 USA

PCT

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL SEARCH REPORT AND THE WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY, OR THE DECLARATION

(PCT Rule 44.1)

Date of mailing *(day/month/year)*	04 December 2017 (04.12.2017)
Applicant's or agent's file reference: A0863.70102	**FOR FURTHER ACTION** See paragraphs 1 and 4 below
International application No.: **PCT/US2017/047905**	International filing date *(day/month/year)*: **22 August 2017 (22.08.2017)**

Applicant
AMPHENOL CORPORATION

1. ☒ The applicant is hereby notified that the international search report and the written opinion of the International Searching Authority have been established and are transmitted herewith.

Filing of amendments and statement under Article 19:

The applicant is entitled, if he so wishes, to amend the claims of the international application (see Rule 46):

When? The time limit for filing such amendments is normally two months from the date of transmittal of the international search report.

How? Directly to the International Bureau of WIPO preferably through ePCT or on paper to, 34 chemin des Colombettes 1211 Geneva 20, Switzerland, Facsimile No.: +41 22 338 82 70

For more detailed instructions, see *PCT Applicant's Guide*, International Phase, paragraphs 9.004 . 9-011.

2. ☐ The applicant is hereby notified that no international search report will be established and that the declaration under Article 17(2)(a) to that effect and the written opinion of the International Searching Authority are transmitted herewith.

3. ☐ **With regard to any protest** against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:

☐ the protest together with the decision thereon has been transmitted to the International Bureau together with any request to forward the texts of both the protest and the decision thereon to the designated Offices.

☐ no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.

4. **Reminders**

The applicant may submit comments on an informal basis on the written opinion of the International Searching Authority to the International Bureau. These comments will be made available to the public after international publication. The International Bureau will send a copy of such comments to all designated Offices unless an international preliminary examination report has been or is to be established.

Shortly after the expiration of **18 months** from the priority date, the international application will be published by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau before the completion of the technical preparations for international publication (Rules 90*bis*.1 and 90*bis*.3).

Within **19 months** from the priority date, but only in respect of some designated Offices, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase **until 30 months** from the priority date (in some Offices even later); otherwise, the applicant must, **within 20 months** from the priority date, perform the prescribed acts for entry into the national phase before those designated Offices. In respect of other designated Offices, the time limit of **30 months** (or later) will apply even if no demand is filed within 19 months. For details about the applicable time limits, Office by Office, see www.wipo.int/pct/en/texts/time_limits.html and the *PCT Applicant's Guide*, National Chapters.

Within **22 months** from the priority date, the applicant may request that a supplementary international search be carried out by a different International Searching Authority, that offers this service (Rule 45*bis*.1). The procedure for requesting supplementary international search is described in the *PCT Applicant's Guide*, International Phase, paragraphs 8.006-8.032.

Name and mailing address of the ISA/KR International Application Division Korean Intellectual Property Office 189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea	Authorized officer COMMISSIONER
Facsimile No. 82-42-481-8578	Telephone No. 82-42-481-5875

Form PCT/ISA/220 (July 2017)

* Attention

Copies of the documents cited in the international search report can be searched in the following Korean Intellectual Property Office English website for six months(expire date : **2018.06.04**) from the date of mailing of the international search report.

http://www.kipo.go.kr/en/ => PCT Service => PCT Services

ID : PCT international application number
PW : **2KP69GX7**

Inquiries related to PCT International Search Report or Written Opinion prepared by KIPO as an International Searching Authority can be answered not only by KIPO but also through IPKC (Intellectual Property Korea Center), located in Vienna, VA, which functions as a PCT Help Desk for PCT applicants.

Homepage: http://www.ipkcenter.com

Email: ipkc@ipkcenter.com

Notes to Form PCT/ISA/220 (July 2014)

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference A0863.70102	**FOR FURTHER ACTION**	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
International application No. **PCT/US2017/047905**	International filing date *(day/month/year)* **22 August 2017 (22.08.2017)**	(Earliest) Priority Date *(day/month/year)* 23 August 2016 (23.08.2016)

Applicant

AMPHENOL CORPORATION

This International search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of **3** sheets.

☐ It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**
   a. With regard to the **language**, the international search was carried out on the basis of :
      ☒ the international application in the language in which it was filed
      ☐ a translation of the international application into _____ , which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))
   b. ☐ This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6*bis*(a)).
   c. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.
2. ☐ **Certain claims were found unsearchable** (See Box No. II)
3. ☐ **Unity of invention is lacking** (See Box No. III)
4. With regard to the **title,**
   ☒ the text is approved as submitted by the applicant.
   ☐ the text has been established by this Authority to read as follows:
5. With regard to the **abstract,**
   ☒ the text is approved as submitted by the applicant.
   ☐ the text has been established, according to Rule 38.2, by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.
6. With regard to the drawings,
   a. the figure of the **drawings** to be published with the abstract is Figure No. **2**
      ☒ as suggested by the applicant.
      ☐ as selected by this Authority, because the applicant failed to suggest a figure.
      ☐ as selected by this Authority, because this figure better characterizes the invention.
   b. ☐ none of the figures is to be published with the abstract.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2017/047905

A. CLASSIFICATION OF SUBJECT MATTER

H01R 13/652(2006.01)i, H01R 12/71(2011.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01R 13/652; H01R 24/62; H05K 1/11; H01R 13/6461; H01R 13/514; H01R 24/28; H01R 12/16; H01R 12/71

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: conductive element, lossy material, bar, latch, contact

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2011-0256739 A1 (TOSHIYUKI NAKAIE et al.) 20 October 2011 See paragraphs [0031]-[0042], claim 1 and figures 1-3.	1-25
A	US 2015-0111427 A1 (FOXCONN INTERCONNECT TECHNOLOGY LIMITED) 23 April 2015 See paragraphs [0024]-[0028], claim 1 and figures 3-6.	1-25
A	US 2013-0316590 A1 (HON HAI PRECISION INDUSTRY CO., LTD.) 28 November 2013 See paragraphs [0014]-[0020], claims 1-5 and figures 1-5.	1-25
A	US 2012-0184154 A1 (FRANK M. STRAKA et al.) 19 July 2012 See paragraphs [0031]-[0036], claims 1-5 and figures 6A-6B.	1-25
A	JP 2006-344524 A (MOLEX INC.) 21 December 2006 See paragraphs [0030]-[0041] and figures 1-5.	1-25

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
04 December 2017 (04.12.2017)	**04 December 2017 (04.12.2017)**

Name and mailing address of the ISA/KR
International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea
Facsimile No. +82-42-481-8578

Authorized officer
KIM, Sung Gon
Telephone No. +82-42-481-8746

Form PCT/ISA/210 (second sheet) (January 2015)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2017/047905

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2011-0256739 A1	20/10/2011	CN 102292881 A	21/12/2011
		EP 2538499 A1	26/12/2012
		JP 4654328 B1	16/03/2011
		US 8267728 B2	18/09/2012
		WO 2011-101922 A1	25/08/2011
US 2015-0111427 A1	23/04/2015	CN 104577577 A	29/04/2015
		US 9246284 B2	26/01/2016
US 2013-0316590 A1	28/11/2013	CN 202695788 U	23/01/2013
		US 8936493 B2	20/01/2015
US 2012-0184154 A1	19/07/2012	AU 2009-322495 A1	10/06/2010
		AU 2009-322495 B2	07/08/2014
		CA 02745291 A1	10/06/2010
		CA 2745291 C	28/02/2017
		CN 102232259 A	02/11/2011
		CN 102232259 B	18/06/2014
		EP 2371041 A1	05/10/2011
		EP 2371041 B1	20/04/2016
		HK 1157074 A1	21/04/2017
		JP 2012-510707 A	10/05/2012
		JP 2013-093335 A	16/05/2013
		JP 5209798 B2	12/06/2013
		JP 5623567 B2	12/11/2014
		KR 10-1622117 B1	18/05/2016
		KR 10-2011-0096125 A	29/08/2011
		MX 2011005785 A	24/06/2011
		US 2010-0197162 A1	05/08/2010
		US 2014-0154919 A1	05/06/2014
		US 2015-0188260 A1	02/07/2015
		US 2016-0248203 A1	25/08/2016
		US 8167661 B2	01/05/2012
		US 8632362 B2	21/01/2014
		US 8979588 B2	17/03/2015
		US 9331431 B2	03/05/2016
		WO 2010-065588 A1	10/06/2010
JP 2006-344524 A	21/12/2006	CN 101238613 A	06/08/2008
		CN 101238613 B	31/08/2011
		JP 4889243 B2	07/03/2012
		US 2011-0151708 A1	23/06/2011
		US 8043114 B2	25/10/2011
		WO 2007-110699 A2	04/10/2007
		WO 2007-110699 A3	27/12/2007

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:
WALSH, EDMUND J.

WOLF, GREENFIELD & SACKS, P.C. 600 ATLANTIC AVENUE BOSTON MA 02210-2206 USA

PCT

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43bis.1)

Date of mailing *(day/month/year)*	**04 December 2017 (04.12.2017)**
Applicant's or agent's file reference A0863.70102	**FOR FURTHER ACTION** See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US2017/047905	**22 August 2017 (22.08.2017)**	23 August 2016 (23.08.2016)

International Patent Classification (IPC) or both national classification and IPC
H01R 13/652(2006.01)i, H01R 12/71(2011.01)i

Applicant
AMPHENOL CORPORATION

1. This opinion contains indications relating to the following items:

- [x] Box No. I Basis of the opinion
- [ ] Box No. II Priority
- [ ] Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- [ ] Box No. IV Lack of unity of invention
- [x] Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step and industrial applicability; citations and explanations supporting such statement
- [ ] Box No. VI Certain documents cited
- [ ] Box No. VII Certain defects in the international application
- [x] Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1bis(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.
For further options, see Form PCT/ISA/220.

Name and mailing address of the ISA/KR	Date of completion of this opinion	Authorized officer
International Application Division Korean Intellectual Property Office 189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea Facsimile No. +82-42-481-8578	04 December 2017 (04.12.2017)	KIM, Sung Gon Telephone No. +82-42-481-8746

Form PCT/ISA/237 (cover sheet) (January 2015)

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2017/047905

Box No. I Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of :

   ☒ the international application in the language in which it was filed

   ☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(a))

3. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of a sequence listing:

   a. ☐ forming part of the international application as filed:
      ☐ in the form of an Annex C/ST.25 text file.
      ☐ on paper or in the form of an image file.

   b. ☐ furnished together with the international application under PCT Rule 13*ter*.1(a) for the purposes of international search only in the form of an Annex C/ST.25 text file.

   c. ☐ furnished subsequent to the international filing date for the purposes of international search only:
      ☐ in the form of an Annex C/ST.25 text file (Rule 13*ter*.1(a)).
      ☐ on paper or in the form of an image file (Rule 13*ter*.1(b) and Administrative Instructions, Section 713).

4. ☐ In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that forming part of the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2017/047905

Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Claims	1-25	YES
	Claims	NONE	NO
Inventive step (IS)	Claims	1-25	YES
	Claims	NONE	NO
Industrial applicability (IA)	Claims	1-25	YES
	Claims	NONE	NO

2. Citations and explanations :

Reference is made to the following documents:

D1: US 2011-0256739 A1 (TOSHIYUKI NAKAIE et al.) 20 October 2011
D2: US 2015-0111427 A1 (FOXCONN INTERCONNECT TECHNOLOGY LIMITED) 23 April 2015
D3: US 2013-0316590 A1 (HON HAI PRECISION INDUSTRY CO., LTD.) 28 November 2013
D4: US 2012-0184154 A1 (FRANK M. STRAKA et al.) 19 July 2012
D5: JP 2006-344524 A (MOLEX INC.) 21 December 2006

1. Novelty and Inventive Step

1.1 Claims 1-10

The subject matter of claim 1 differs from these prior art documents in a member comprising lossy material and a plurality of conductive, compliant members extending from the lossy material, wherein conductive compliant members of the plurality of conductive compliant members make contact with a portion of conductive elements of a first plurality of conductive elements and a portion of conductive elements of a second plurality of conductive elements. And it is not obvious to a person skilled in the art by the documents, taken alone or in combination. Therefore, claim 1 meets the requirements of PCT Article 33(2) and (3) with respect to novelty and inventive step.

Claims 2-10 are dependent on claim 1 and therefore meet the requirements of PCT Article 33(2) and (3).

1.2 Claims 11-18

The subject matter of claim 11 differs from these prior art documents in a member comprising an electrically lossy body and a plurality of conductive, compliant members extending from the lossy body, wherein the conductive compliant members make contact with a portion of the plurality of conductive elements. And it is not obvious to a person

Continued on Supplemental Box

Box No. VIII Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

The phrase 'a portion of conductive elements' in line 15 of claim 1 is considered to be a typo for 'a portion of the conductive elemen ts'. Therefore, claim 1 does not meet the requirements of PCT Article 6.

The phrase 'the first surface and a second surface' in line 2 of claim 5 is considered to be a typo for 'the first surface and second surf ace'. Therefore, claim 5 does not meet the requirements of PCT Article 6.

Claim 16 is worded in reference to 'the metal member' of claim 14. However, 'a metal member' has not been previously defined. Therefore, claim 16 is unclear, contrary to PCT Article 6.

Claim 19 relates to the electrical connector, but claims 21-25 directly or indirectly dependent on claim 19 relate to the assembly. As claims 21-25 do not clear define the matter for which protection is sought, these claims do not meet the requirements of PCT Article 6.

Claims 21 is worded in reference to 'the printed circuit board' of claim 19. However, 'a printed circuit board' has not been previously defined. Therefore, claim 21 is unclear, contrary to PCT Article 6.

Claim 23 is worded in reference to 'the conductive web' of claim 19. However, 'a conductive web' has not been previously defined. Therefore, claim 23 is unclear, contrary to PCT Article 6.

Supplemental Box

In case **the space in any of the preceding boxes is not sufficient.**
Continuation of : Box No. V

skilled in the art by the documents, taken alone or in combination. Therefore, claim 11 meets the requirements of PCT Article 33(2) and (3) with respect to novelty and inventive step.

Claims 12-18 are dependent on claim 11 and therefore meet the requirements of PCT Article 33(2) and (3).

1.3 Claims 19-25
The subject matter of claim 19 differs from these prior art documents in a member comprising lossy material and a plurality of conductive members extending from the lossy material, wherein conductive members of the plurality of conductive members make contact with a portion of conductive elements of a first plurality of conductive elements and a portion of conductive elements of a second plurality of conductive elements. And it is not obvious to a person skilled in the art by the documents, taken alone or in combination. Therefore, claim 19 meets the requirements of PCT Article 33(2) and (3) with respect to novelty and inventive step.

Claims 20-25 are dependent on claim 19 and therefore meet the requirements of PCT Article 33(2) and (3).

2. Industrial Applicability
Claims 1-25 are industrially applicable under PCT Article 33(4).

Electronic Patent Application Fee Transmittal

Application Number:	15065683
Filing Date:	09-Mar-2016
Title of Invention:	HIGH PERFORMANCE CABLE CONNECTOR
First Named Inventor/Applicant Name:	Donald W. Milbrand
Filer:	Marcus E. Browne/Eileen MacKenzie
Attorney Docket Number:	A0863.70051US04

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
RCE- 1st Request	1801	1	1300	1300
		Total in USD ($)		**1300**

Electronic Acknowledgement Receipt	
EFS ID:	32260741
Application Number:	15065683
International Application Number:	
Confirmation Number:	5112
Title of Invention:	HIGH PERFORMANCE CABLE CONNECTOR
First Named Inventor/Applicant Name:	Donald W. Milbrand
Customer Number:	23628
Filer:	Marcus E. Browne/Eileen MacKenzie
Filer Authorized By:	Marcus E. Browne
Attorney Docket Number:	A0863.70051US04
Receipt Date:	05-APR-2018
Filing Date:	09-MAR-2016
Time Stamp:	18:18:14
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$1300
RAM confirmation Number	040618INTEFSW18191100
Deposit Account	232825
Authorized User	Wolf Greenfield
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.17 (Patent application and reexamination processing fees)	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Continued Examination (RCE)	A086370051US04-RCE-MEB.pdf	26725 8755011752ff1105e2b4cd82436a1c642cdc0808	no	1
Warnings:					
This is not a USPTO supplied RCE SB30 form.					
Information:					
2	Fee Worksheet (SB06)	A086370051US04-FEE-MEB.pdf	31168 12194c0557451b95e86110c05f104f3887021e91	no	1
Warnings:					
Information:					
3		A086370051US04-AMN-MEB.pdf	116996 d0c63d2d0a828a9ffc20da66e69f2b50201dba7f	yes	15

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Applicant Arguments/Remarks Made in an Amendment	9	15
	Claims	2	8
	Amendment Submitted/Entered with Filing of CPA/RCE	1	1

Warnings:					
Information:					
4		A086370051US04-IDS-MEB.pdf	63717 71428d56c98685702b44f243eb98ff665a52a06b	yes	6

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Information Disclosure Statement (IDS) Form (SB08)	5	6

	Transmittal Letter		1	4	
Warnings:					
Information:					
5	Foreign Reference	CN102598430A.pdf	9197040 e6bda1e122291f2ebb09f4d56d7db10a374b1854	no	59
Warnings:					
Information:					
6	Foreign Reference	EP2405537A1.pdf	3545385 ca8fcf58684b464ff98f204c81571dc2058ecb15	no	32
Warnings:					
Information:					
7	Foreign Reference	JP2006344524A.pdf	1880392 f3107dbc02d32bf260a4a3b31e77a57c1a9b63b2	no	30
Warnings:					
Information:					
8	Non Patent Literature	A086370102WO00_ISRWO_Dated_12-04-2017.pdf	1574121 ee601b54247cbb9e930b711c0f0a8310ff00c5b1	no	10
Warnings:					
Information:					
9	Fee Worksheet (SB06)	fee-info.pdf	30668 3c461d468d4a94f8627e31643dc1b417e77a4066	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	16466212		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 15/065,683	Filing Date 03/09/2016	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT **04/05/2018**

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 24	Minus	** 23	= 1	X $100 =	100
Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X $460 =	0
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	**100**

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
DEBORAH SCOTT

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/065,683	03/09/2016	Donald W. Milbrand JR.	A0863.70051US04	5112

23628 7590 05/21/2018
WOLF GREENFIELD & SACKS, P.C.
600 ATLANTIC AVENUE
BOSTON, MA 02210-2206

EXAMINER	
FIGUEROA, FELIX O	

ART UNIT	PAPER NUMBER
2833	

NOTIFICATION DATE	DELIVERY MODE
05/21/2018	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

Patents_eOfficeAction@WolfGreenfield.com
WGS_eOfficeAction@WolfGreenfield.com

Office Action Summary	Application No. 15/065,683	Applicant(s) MILBRAND ET AL.	
	Examiner FELIX O. FIGUEROA	Art Unit 2833	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *5/5/2018*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-8 and 10-25* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-8 and 10-25* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

DETAILED ACTION

Notice of Pre-AIA or AIA Status

The present application is being examined under the pre-AIA first to invent provisions.

Claim Rejections - 35 USC § 103

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 6-8, 10, 23 and 24 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Trammel (US 6,296,496) in view of Niwa et al. (US 5,474,472).

Trammel discloses a receptacle adapted for mounting to a printed circuit board, comprising: a housing (11) having a cavity (17) bounded by a first surface (top) that is parallel to the printed circuit board and an opposing second surface (bottom) that is parallel to the printed circuit board; a first lead assembly including a first monolithic housing member (401); and a first plurality of conductive elements (20) each comprising a contact tail (25) adapted for attachment to the printed circuit board, a mating contact portion (23) disposed along the first surface of the cavity, and an intermediate portion (21) disposed in the first monolithic housing member and coupling the contact tail to the mating contact portion; and a second lead assembly including; a second monolithic housing member (402); and a second plurality of conductive elements (20) each

comprising a contact tail (25) adapted for attachment to the printed circuit board, a mating contact portion (23) disposed along the second surface of the cavity, and an intermediate portion (21) disposed in the second monolithic housing member coupling the contact tail to the mating contact portion.

Niwa teaches a housing (24) having a cavity bounded by first and second surfaces (top and bottom) that are disposed above a first side of the printed circuit board; a plurality of conductive elements (16a, 16b) comprising a tail that is perpendicular to the first side of the PCB; and a second plurality of conductive elements (16c, 16d) comprising a tail that is perpendicular to the first side of the PCB. It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the first and second surfaces disposed above the PCB, as taught by Niwa, in order to accommodate environmental parameters.

Regarding claim 6, Trammel discloses the contact tails and the mating contact portions disposed at right angles.

Regarding claim 7, Trammel discloses the first plurality of conductive elements and the second plurality of conductive elements forming rows of contacts on the first and second surfaces, respectively, of the cavity.

Regarding claim 8, Trammel discloses the first and second surfaces of the cavity include slots configured to receive the conductive elements of the first plurality of conductive elements and the second plurality of conductive elements, respectively.

Regarding claim 10, Trammel discloses the first plurality of conductive elements is molded in the first housing member, and the second plurality of conductive elements is molded in the second housing member.

Regarding claim 23, Trammel discloses an insert (30) disposed between the first and second lead assemblies.

Regarding claim 24, Trammel discloses a receptacle adapted for mounting to a printed circuit board, comprising: a housing (11) having a cavity (17) bounded by a first surface (top) that is parallel to the printed circuit board and a second surface (bottom) that faces the first surface and is parallel to the printed circuit board; a first lead assembly including (401): a first plurality of conductive elements (20) each comprising a mating contact portion (23) disposed along the first surface of the cavity, a contact tail (25) adapted for attachment to the printed circuit board and disposed at a right angle (at least a part) relative to the mating contact portion, and an intermediate portion (21) coupling the contact tail to the mating contact portion; and a first monolithic housing member (401) molded over the intermediate portions of each conductive element of the first plurality of conductive elements; and a second lead assembly (402), separate and distinct from the first lead assembly, including: a second plurality of conductive elements (20) each comprising a mating contact portion (23) disposed along the second surface of the housing cavity, a contact tail (25) adapted for attachment to the printed circuit board and disposed at a right angle relative to the mating contact portion, and an intermediate portion (21) coupling the contact tail to the mating contact portion; and a

second monolithic housing member (402) molded over the intermediate portions of each conductive element of the second plurality of conductive elements.

Niwa teaches a plurality of conductive elements (16c, 16d) comprising a tail that is perpendicular to the first side of the PCB, with an intermediate portion comprising a right angle bend; and a second plurality of conductive elements (16a, 16b) that are longer than the first plurality of conductive elements and each comprising a tail that is perpendicular to the first side of the PCB, with an intermediate portion comprising a right angle bend. It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the conductive elements, as taught by Niwa, in order to accommodate environmental parameters.

Claims 2-5 and 15-22 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Trammel and Niwa, and further in view of Cohen et al. (US 7,753,731).

Regarding claim 2, Cohen teaches (in Fig. 4) the use of an insert (160) disposed between the first and second lead assemblies; the insert including an electrically lossy material. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use an insert, as taught by Cohen, in order to provide the desired shielding and reduce crosstalk between the lead assemblies/rows.

Regarding claim 3, Cohen teaches the insert contacting selected ones of the conductive elements.

Regarding claim 4, Cohen teaches the insert including projections towards selected ones of the conductive elements.

Regarding claim 5, Cohen teaches at least one of the first and second housing members including one or more slots for receiving the projections of the insert.

Regarding claim 15, Trammel, as modified by Cohen, discloses that for each conductive element of a first subset of the first plurality of conductive elements, a portion of the conductive element is exposed through the first housing member, and for each conductive element of a second subset of the second plurality of conductive elements, a portion of the conductive element is exposed through the second housing member.

Regarding claim 16, Cohen discloses a first surface of the insert comprising a first plurality of projections, each projection of the first plurality of projections being coupled to a conductive element of the first subset; and a second surface of the insert comprises a second plurality of projections, each projection of the second plurality of projections being coupled to a conductive element of the second subset.

Regarding claim 17, Cohen discloses the first plurality of conductive elements comprising conductive elements disposed in a plurality of pairs of conductive elements; and the first subset of the first plurality of conductive elements comprises conductive elements each of which is disposed adjacent a pair of the plurality of pairs.

Regarding claim 18, Cohen teaches the insert including a conductive material.

Regarding claim 19, Cohen teaches the insert being at least partially conductive.

Regarding claim 20, Cohen teaches the insert including an electrically lossy material; and the electrically lossy material is electrically coupled to selected ones of the first plurality of conductive elements and the second plurality of conductive elements.

Regarding claim 21, Trammel, as modified by Cohen, discloses the first plurality of conductive elements positioned in a first row, the first row comprising pairs of the first plurality of conductive elements separated by single conductive elements of the first plurality of conductive elements; the second plurality of conductive elements positioned in a second row, the second row comprising pairs of the second plurality of conductive elements separated by single conductive elements of the second plurality of conductive elements; and the electrically lossy material is selectively electrically coupled to the single conductive elements of the first plurality of conductive elements and second plurality of conductive elements.

Regarding claim 22, Cohen discloses the insert includes projections towards the selected ones of the conductive elements.

Claims 11-14 and 25 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Trammel and Niwa, and further in view of Fogg et al. (US 6,582,244).

Regarding claim 11, Trammel discloses the first housing member and the second housing member made of an insulative material. Fogg teaches a housing (150) made of insulating material.

Regarding claim 12, Fogg discloses the housing includes at least one projection from a lower surface thereof.

Regarding claim 13, Fogg discloses a shell (10) adapted for attachment of the housing to the printed circuit board.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the housing of insulating material with a lower projection and a shell, as taught by Fogg, in order to reduce weight and cost of the connector.

Regarding claim 14, Fogg discloses the housing further comprises a second cavity (204) bounded by a third surface (210) and an opposing fourth surface (212), further comprising a third lead assembly including a third plurality of conductive elements (306) disposed in a third housing member and a fourth lead assembly including a fourth plurality of conductive elements (308) disposed in a fourth housing member, each conductive element of the third and fourth pluralities of conductive elements comprising a contact tail adapted for attachment to the printed circuit board, a mating contact portion and an intermediate portion coupling the contact tail to the mating contact portion, wherein the mating contact portions of the third plurality of conductive elements are disposed along the third surface of the second cavity and the mating contact portions of the fourth plurality of conductive elements are disposed along the fourth surface of the second cavity. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form additional subassemblies, as taught by Fogg, in order to provide the desire interface to transmit the desired signals.

Regarding claim 25, Trammel discloses a receptacle adapted for mounting to a printed circuit board, comprising: a monolithic housing (11) and having a cavity (17)

bounded by a first surface (top) that is parallel to the printed circuit board and a second surface (bottom) that faces the first surface and is parallel to the printed circuit board; a first lead assembly (401) including: a first plurality of conductive elements (20) including at least six conductive elements, each of the first plurality of conductive elements comprising a mating contact portion disposed along the first surface of the cavity, a contact tail adapted for attachment to the printed circuit board and disposed at a right angle relative to the mating contact portion, and an intermediate portion coupling the contact tail to the mating contact portion; and a first monolithic housing member (401) made of an insulative material and molded over the intermediate portions of each conductive element of the first plurality of conductive elements; and a second lead assembly (402), separate and distinct from the first lead assembly, including: a second plurality of conductive elements including at least six conductive elements, each of the second plurality of conductive elements comprising a mating contact portion disposed along the second surface of the housing cavity, a contact tail adapted for attachment to the printed circuit board and disposed at a right angle relative to the mating contact portion, and an intermediate portion coupling the contact tail to the mating contact portion; and a second monolithic housing member (402) made of an insulative material and molded over the intermediate portions of each conductive element of the second plurality of conductive elements.

Fogg teaches a housing (150) made of insulating material; a shell (10) adapted for attachment of the housing to the printed circuit board. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the housing of

insulating material with a lower projection and a shell, as taught by Fogg, in order to reduce weight and cost of the connector.

Niwa teaches a plurality of conductive elements (16c, 16d) comprising a tail that is perpendicular to the first side of the PCB, with an intermediate portion comprising a right angle bend; and a second plurality of conductive elements (16a, 16b) that are longer than the first plurality of conductive elements and each comprising a tail that is perpendicular to the first side of the PCB, with an intermediate portion comprising a right angle bend. It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the conductive elements, as taught by Niwa, in order to accommodate environmental parameters.

Response to Arguments

Applicant's arguments with respect to the claims have been considered but are moot in view of the new grounds of rejection, as applied.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to FELIX O. FIGUEROA whose telephone number is (571)272-2003. The examiner can normally be reached on Mon.-Fri., 10:00am-6:00pm.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an

interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Renee Luebke can be reached on (571) 272-2009. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/FELIX O. FIGUEROA/
Primary Examiner
Art Unit 2833

Notice of References Cited	Application/Control No. 15/065,683	Applicant(s)/Patent Under Reexamination MILBRAND ET AL.	
	Examiner FELIX O. FIGUEROA	Art Unit 2833	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-5,474,472 A	12-1995	Niwa; Takeo	H01R13/6585	439/607.08
	B	US-				
	C	US-				
	D	US-				
	E	US-				
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

FORM PTO-1449/A and B (modified PTO/SB/08)	APPLICATION NO.: 15/065,683	ATTY. DOCKET NO.: A0863.70051US04
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	FILING DATE: March 9, 2016	CONFIRMATION NO.: 5112
	FIRST NAMED INVENTOR: Donald W. Milbrand, Jr.	
Sheet 1 of 2	GROUP ART UNIT: 2833	EXAMINER: F. O. Figueroa

U.S. PATENT DOCUMENTS

Examiner's Initials #	Cite No.	U.S. Patent Document Number	Kind Code	Name of Patentee or Applicant of Cited Document	Date of Publication or Issue of Cited Document MM-DD-YYYY
		4,632,476	A	Schell	12-30-1986
		4,806,107	A	Arnold et al.	02-21-1989
		4,846,727		Glover et al.	07-11-1989
		4,975,084	A	Fedder et al.	12-04-1990
		5,066,236	A	Broeksteeg	11-19-1991
		5,429,520		Morlion et al.	07-04-1995
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Examiner's Initials #	Cite No.	Foreign Patent Document Office/ Country	Number	Kind Code	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Translation (Y/N)
		CN	102598430	A	Amphenol Corp.	07-18-2012	Y-abstract only
		EP	2405537	A1	Hosiden Corporation	01-11-2012	

EXAMINER:	DATE CONSIDERED:

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

6208868.1

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /F.O.F/

FORM PTO-1449/A and B (modified PTO/SB/08)				APPLICATION NO.: 15/065,683	ATTY. DOCKET NO.: A0863.70051US04
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				FILING DATE: March 9, 2016	CONFIRMATION NO.: 5112
				FIRST NAMED INVENTOR: Donald W. Milbrand, Jr.	
Sheet	2	of	2	GROUP ART UNIT: 2833	EXAMINER: F. O. Figueroa

		JP	2006-344524	A	Molex Inc.	12-21-2006	Y-abstract only

OTHER ART -- NON PATENT LITERATURE DOCUMENTS

Examiner's Initials #	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	Translation (Y/N)
		International Search Report and Written Opinion for International Application No. PCT/US2017/047905 dated December 04, 2017 (A0863.70102WO00).	

[NOTE – No copies of U.S. patents, published U.S. patent applications, or pending, unpublished patent applications stored in the USPTO's Image File Wrapper (IFW) system, are included. See 37 CFR § 1.98 and 1287OG163. Copies of all other patent(s), publication(s), unpublished, pending U.S. patent applications, or other information listed are provided as required by 37 CFR § 1.98 unless 1) such copies were provided in an IDS in an earlier application that complies with 37 CFR § 1.98, and 2) the earlier application is relied upon for an earlier filing date under 35 U.S.C. § 120.]

EXAMINER:	DATE CONSIDERED:
/FELIX O FIGUEROA/	05/07/2018

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

6208868.1

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /F.O.F/

Docket No.: A0863.70051US04
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor:	Donald W. Milbrand, Jr.
Application No.:	15/065,683
Confirmation No.:	5112
Filed:	March 9, 2016
For:	HIGH PERFORMANCE CABLE CONNECTOR
Examiner:	F. O. Figueroa
Art Unit:	2833

Certificate of Electronic Filing under 37 CFR §1.8
I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being transmitted via the Office's electronic filing system in accordance with 37 C.F.R. § 1.6(a)(4).

Dated: August 21, 2018 Electronic Signature for: /Trish McDonald/

RESPONSE TO NON-FINAL OFFICE ACTION UNDER 37 C.F.R. § 1.111

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

INTRODUCTORY COMMENTS

In response to the Office Action dated May 21, 2018, rejecting claims 1-8, and 10-25, please amend the above-identified U.S. patent application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 11 of this paper.

Electronic Patent Application Fee Transmittal

Application Number:	15065683
Filing Date:	09-Mar-2016
Title of Invention:	HIGH PERFORMANCE CABLE CONNECTOR
First Named Inventor/Applicant Name:	Donald W. Milbrand
Filer:	Edmund J. Walsh/Trish McDonald
Attorney Docket Number:	A0863.70051US04

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
CLAIMS IN EXCESS OF 20	1202	5	100	500
INDEPENDENT CLAIMS IN EXCESS OF 3	1201	1	460	460
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**960**

Electronic Acknowledgement Receipt	
EFS ID:	33495279
Application Number:	15065683
International Application Number:	
Confirmation Number:	5112
Title of Invention:	HIGH PERFORMANCE CABLE CONNECTOR
First Named Inventor/Applicant Name:	Donald W. Milbrand
Customer Number:	23628
Filer:	Edmund J. Walsh/Trish McDonald
Filer Authorized By:	Edmund J. Walsh
Attorney Docket Number:	A0863.70051US04
Receipt Date:	21-AUG-2018
Filing Date:	09-MAR-2016
Time Stamp:	18:34:17
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$960
RAM confirmation Number	082218INTEFSW18353100
Deposit Account	232825
Authorized User	Wolf Greenfield
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees)	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	A086370051US04-TRN-EJW.pdf	25035 335c1c6db70426dd1d325f161a6a12f7954003f4	no	1
Warnings:					
Information:					
2	Fee Worksheet (SB06)	A086370051US04-FEE-EJW.pdf	31524 1724bb039f65aab636232c7b5640fde2cec7d461	no	1
Warnings:					
Information:					
3		A086370051US04-AMN-EJW.pdf	73981 9c235a504dd02135cbcf443fab78de7e3e048bbd	yes	17

Multipart Description/PDF files in .zip description

Document Description	Start	End
Applicant Arguments/Remarks Made in an Amendment	11	17
Claims	2	10
Amendment/Req. Reconsideration-After Non-Final Reject	1	1

Warnings:					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	32373 e328477af382ed93bb33d17a7412c02210b6a477	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	162913		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

REMARKS

In response to the Office Action mailed May 21, 2018, Applicant respectfully requests reconsideration in view of the foregoing amendments and the following remarks. Claims 1-8, and 10-25 were previously pending in this application. No claims are canceled herein. Claims 1, 24 & 25 are amended herein. Claims 26-30 are added herein. As a result, claims 1-8, and 10-30 are pending for examination with claims 1, 24, 25 and 27 being independent claims. No new matter is added herein.

REJECTIONS UNDER 35 U.S.C. § 103

I.) Independent claims 1 and 24 are rejected under 35 U.S.C. 103 as being unpatentable over US 6,296,496 to Trammel (hereinafter "Trammel") in view of US 5,474,472 to Niwa et al. (hereinafter "Niwa").

Without agreeing that the rejection of independent claim 1 was proper, the claim is amended herein to advance prosecution. Support for amended independent claim 1 can be found throughout the application as filed, and specifically at least in Fig. 6. Support for amended independent claim 24 can be found throughout the application as filed, and specifically at least in Figs. 3 and 6. Accordingly, reconsideration is requested in view of the foregoing amendments and the following remarks.

Amended independent claim 1 recites:

A receptacle adapted for mounting to a printed circuit board, comprising:

a housing having a cavity bounded by a first surface that is parallel to the printed circuit board and an opposing second surface that is parallel to the printed circuit board, ***each of the first and second surfaces being disposed above a first side of the printed circuit board***;

a first lead assembly including:

a first monolithic housing member comprising exterior projections extending in a direction parallel to the first surface; and

a first plurality of conductive elements each comprising a contact tail adapted for attachment to the printed circuit board that is perpendicular to the first side of the printed circuit board, a mating contact portion disposed along the first surface of the cavity, and an intermediate portion disposed in the first monolithic housing member and coupling the contact tail to the mating contact portion; and

a second lead assembly including:

a second monolithic housing member comprising exterior projections extending in the direction parallel to the first surface; and

a second plurality of conductive elements each comprising a contact tail adapted for attachment to the printed circuit board that is perpendicular to the first side of the printed circuit board, a mating contact portion disposed along the second surface of the cavity, and an intermediate portion disposed in the second monolithic housing member coupling the contact tail to the mating contact portion (Emphasis added).

Trammel and Niwa fail to describe at least the above emphasized limitations. Trammel describes an electrical connector (1) comprising a cavity (17) having top and bottom surfaces, and terminal cores (401) and (402). However, Trammel does not describe at least exterior projections extending from the terminal cores (401) and (402) in a direction parallel to the surfaces of the cavity (17).

Niwa describes an electrical connector (10) comprising a cavity with top and bottom surfaces, but Niwa fails to describe at least first and second monolithic housing members comprising exterior projections extending in a direction parallel to a surface. Even if one were to combine the Trammel and Niwa references (which Applicant does not concede is proper), the alleged combination would still fail to describe housing members comprising exterior projections extending in a direction parallel to a surface of the cavity. Thus, amended independent claim 1 patentably distinguishes over the alleged combination of Trammel and Niwa. Accordingly, withdrawal of the rejection of independent claim 1 is respectfully requested.

Without agreeing that the rejection of independent claim 24 was proper, the claim is amended herein to advance prosecution. Support for amended independent claim 24 can be found throughout the application as filed, and specifically at least in Figs. 3 and 6.

Amended independent claim 24 recites:

A receptacle adapted for mounting to a printed circuit board, comprising:

a housing having a cavity bounded by a first surface that is parallel to the printed circuit board and a second surface that faces the first surface and is parallel to the printed circuit board;

a first lead assembly including:

a first plurality of conductive elements disposed along a first direction, each comprising a mating contact portion extending along the first surface of the cavity in a second direction perpendicular to the first direction, a contact tail adapted for attachment to the printed circuit board and disposed perpendicular to the mating contact portion, and an intermediate portion coupling the contact tail to the mating contact portion and comprising a right angle bend; and

a first monolithic housing member ***molded over the intermediate portions of each conductive element of the first plurality of conductive elements***; and

a second lead assembly, separate and distinct from the first lead assembly, including:

a second plurality of conductive elements disposed along a first direction, that are longer than the first plurality of conductive elements and each comprise a mating contact portion extending along the second surface of the housing cavity in the second direction, a contact tail adapted for attachment to the printed circuit board and disposed perpendicular to the mating contact portion, and an intermediate portion coupling the contact tail to the mating contact portion and comprising a right angle bend; and

a second monolithic housing member ***molded over the intermediate portions of each conductive element of the second plurality of conductive elements***; and

> ***wherein the contact tails of the first plurality of conductive elements are aligned along the first direction, and the contact tails of the second plurality of conductive elements are aligned along the first direction*** (Emphasis added).

Trammel and Niwa fail to describe at least the above emphasized limitations. Trammel describes a connector (1) having signal contacts (20) and (23). However, Trammel fails to describe at least the signal contacts (20) and (23) having an intermediate portion comprising a right angle bend.

Niwa describes a connector (10) having contacts (e.g. 16a) along a cavity surface in a first direction. However, the contact tails of Niwa are offset in the direction of insertion (Fig. 2). Thus, Niwa fails to describe at least contact tails aligned along the first direction. Moreover, the offset configuration of Niwa is not amenable to a "housing member molded over the intermediate portions of each conductive element …," as required by the claim.

Even if one were to combine the connector of Trammel with the contacts of Niwa (which Applicant does not concede is proper), the alleged combination would fail to have 1) intermediate contact portions having right angle bends and 2) contact tails aligned in the first direction; and 3) a housing member molded over the intermediate portions of each conductive element. Thus, amended independent claim 24 patentably distinguishes over Trammel and Niwa.

Accordingly, withdrawal of the rejection of independent claims 1 and 24, and the claims that depend from them, is respectfully requested.

II.) Independent claim 25 is rejected under 35 U.S.C. 103 as being unpatentable over Trammel and Niwa, and in further view of US 6,582,244 to Fogg et al. (hereinafter "Fogg"). Without agreeing that the rejection of independent claim 25 was proper, the claim is amended herein to advance prosecution. Support for amended independent claim 25 can be found throughout the application as filed, and specifically at least in Fig. 6. Accordingly, reconsideration is requested in view of the foregoing amendments and the following remarks.

Amended independent claim 25 recites:

A receptacle adapted for mounting to a printed circuit board, comprising:

a monolithic housing made of an insulative material and having a cavity bounded by a first surface that is parallel to the printed circuit board and a second surface that faces the first surface and is parallel to the printed circuit board;

a first lead assembly including:

a first plurality of conductive elements disposed along a first direction, each of the first plurality of conductive elements comprising a mating contact portion extending along the first surface of the cavity in a second direction perpendicular to the first direction, a contact tail adapted for attachment to at least one first hole in the printed circuit board and disposed perpendicular to the mating contact portion, and an intermediate portion coupling the contact tail to the mating contact portion and comprising a right angle bend; and

a first monolithic housing member made of an insulative material, molded over the intermediate portions of each conductive element of the first plurality of conductive elements, and ***comprising exterior projections extending along the first direction***; and

a second lead assembly, separate and distinct from the first lead assembly, including:

a second plurality of conductive elements disposed along the first direction, each of the second plurality of conductive elements comprising a mating contact portion extending along the second surface of the housing cavity in the first direction, a contact tail adapted for attachment to at least one second hole in the printed circuit board and disposed perpendicular to the mating contact portion, and an intermediate portion coupling the contact tail to the mating contact portion and comprising a right angle bend; and

a second monolithic housing member made of an insulative material~~, and~~ molded over the intermediate portions of each conductive element of the second plurality of conductive elements, and ***comprising exterior projections extending along the first direction*** (Emphasis added).

The alleged combination of Trammel, Niwa and Fogg fails to describe at least the above emphasized limitations. As described earlier with regard to amended independent claim 1, Trammel does not describe at least exterior projections extending from the terminal cores (401) and (402) in a direction parallel to the surfaces of the cavity (17) and Niwa fails to describe at least first and second monolithic housing members comprising exterior projections extending in a direction parallel to a surface.

Fogg fails to cure the deficiency of the other two references, because Fogg also fails to describe at least first and second monolithic housing members comprising exterior projections extending in a direction parallel to a surface. Thus, even if one were to combine the Trammel, Niwa and Fogg references (which Applicant does not concede is proper), the alleged combination would still fail to describe exterior projections extending from housing members in a direction parallel to a cavity surface. Thus Amended independent claim 25 patentably distinguishes over Trammel, Niwa and Fogg. Accordingly, withdrawal of the rejection of independent claim 25 is respectfully requested.

NEW CLAIMS

Claims 26-30 are added herein, with claim 27 being independent. Support for claims 26-30 can be found throughout the application as filed, and specifically at least in figs. 5 and 6.

GENERAL COMMENTS ON DEPENDENT CLAIMS

Since each of the dependent claims depends from a base claim that is believed to be in condition for allowance, for the sake of brevity, Applicant believes that it is unnecessary at this time to argue the further distinguishing features of the dependent claims. However, Applicant does not necessarily concur with the interpretation of the previously presented dependent claims as set forth in the Office Action, nor does Applicant concur that the basis for rejection of any of the previously presented dependent claims is proper. Therefore, Applicant reserves the right to specifically address the further patentability of the dependent claims in the future.

CONCLUSION

In view of the foregoing amendments and remarks, reconsideration is respectfully requested. This application should now be in condition for allowance; a notice to this effect is respectfully requested. If the Examiner believes, after this amendment, that the application is not in condition for allowance, the Examiner is requested to call the Applicant's attorney at the telephone number listed below.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. Applicant believes no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 23/2825 under Docket No. A0863.70051US04 from which the undersigned is authorized to draw.

Dated: August 21, 2018

Respectfully submitted,

By /Edmund J. Walsh
Edmund J. Walsh
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WOLF, GREENFIELD & SACKS, P.C.
600 Atlantic Avenue
Boston, Massachusetts 02210-2206
617.646.8000

AMENDMENTS TO THE CLAIMS

Applicant submits below a complete listing of the current claims, including marked-up claims with insertions indicated by underlining and deletions indicated by strikeouts and/or double bracketing. This listing of claims replaces all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently amended) A receptacle adapted for mounting to a printed circuit board, comprising:

a housing having a cavity bounded by a first surface that is parallel to the printed circuit board and an opposing second surface that is parallel to the printed circuit board, each of the first and second surfaces being disposed above a first side of the printed circuit board;

a first lead assembly including:

a first monolithic housing member comprising exterior projections extending in a direction parallel to the first surface; and

a first plurality of conductive elements each comprising a contact tail adapted for attachment to the printed circuit board that is perpendicular to the first side of the printed circuit board, a mating contact portion disposed along the first surface of the cavity, and an intermediate portion disposed in the first monolithic housing member and coupling the contact tail to the mating contact portion; and

a second lead assembly including:

a second monolithic housing member comprising exterior projections extending in the direction parallel to the first surface; and

a second plurality of conductive elements each comprising a contact tail adapted for attachment to the printed circuit board that is perpendicular to the first side of the printed circuit board, a mating contact portion disposed along the second surface of the cavity, and an intermediate portion disposed in the second monolithic housing member coupling the contact tail to the mating contact portion.

2. (Previously presented) The receptacle as defined in claim 23, wherein the insert includes an electrically lossy material.

3. (Previously presented) The receptacle as defined in claim 23, wherein the insert contacts selected ones of the conductive elements.

4. (Previously presented) The receptacle as defined in claim 23, wherein the insert includes projections towards selected ones of the conductive elements.

5. (Previously presented) The receptacle as defined in claim 4, wherein at least one of the first and second monolithic housing members includes one or more slots for receiving the projections of the insert.

6. (Original) The receptacle as defined in claim 1, wherein the contact tails and the mating contact portions are disposed at right angles.

7. (Original) The receptacle as defined in claim 1, wherein the first plurality of conductive elements and the second plurality of conductive elements form rows of contacts on the first and second surfaces, respectively, of the cavity.

8. (Original) The receptacle as defined in claim 1, wherein the first and second surfaces of the cavity include slots configured to receive the conductive elements of the first plurality of conductive elements and the second plurality of conductive elements, respectively.

9. (Canceled)

10. (Previously presented) The receptacle as defined in claim 1, wherein the first plurality of conductive elements is molded in the first monolithic housing member, and the second plurality of conductive elements is molded in the second monolithic housing member.

11. (Previously presented) The receptacle as defined in claim 1, wherein the housing, the first monolithic housing member and the second monolithic housing member are made of an insulative material.

12. (Original) The receptacle as defined in claim 1, wherein the housing includes at least one projection from a lower surface thereof.

13. (Original) The receptacle as defined in claim 1, further comprising a shell adapted for attachment of the housing to the printed circuit board.

14. (Previously presented) The receptacle as defined in claim 1, wherein the housing further comprises a second cavity bounded by a third surface and an opposing fourth surface, further comprising a third lead assembly including a third plurality of conductive elements disposed in a third monolithic housing member and a fourth lead assembly including a fourth plurality of conductive elements disposed in a fourth monolithic housing member, each conductive element of the third and fourth pluralities of conductive elements comprising a contact tail adapted for attachment to the printed circuit board, a mating contact portion and an intermediate portion coupling the contact tail to the mating contact portion, wherein the mating contact portions of the third plurality of conductive elements are disposed along the third surface of the second cavity and the mating contact portions of the fourth plurality of conductive elements are disposed along the fourth surface of the second cavity.

15. (Previously presented) The receptacle of claim 23, wherein:

for each conductive element of a first subset of the first plurality of conductive elements, a portion of the conductive element is exposed through the first monolithic housing member, and

for each conductive element of a second subset of the second plurality of conductive elements, a portion of the conductive element is exposed through the second monolithic housing member.

16. (Original) The receptacle of claim 15, wherein:

a first surface of the insert comprises a first plurality of projections, each projection of the first plurality of projections being coupled to a conductive element of the first subset; and

a second surface of the insert comprises a second plurality of projections, each projection of the second plurality of projections being coupled to a conductive element of the second subset.

17. (Original) The receptacle of claim 16, wherein:

the first plurality of conductive elements comprises conductive elements disposed in a plurality of pairs of conductive elements; and

the first subset of the first plurality of conductive elements comprises conductive elements each of which is disposed adjacent a pair of the plurality of pairs.

18. (Previously presented) The receptacle of claim 23, wherein the insert includes a conductive material.

19. (Previously presented) The receptacle of claim 23, wherein the insert is at least partially conductive.

20. (Previously presented) The receptacle as defined in claim 23, wherein:

the insert includes an electrically lossy material; and

the electrically lossy material is electrically coupled to selected ones of the first plurality of conductive elements and the second plurality of conductive elements.

21. (Original) The receptacle as defined in claim 20, wherein:

the first plurality of conductive elements are positioned in a first row, the first row comprising pairs of the first plurality of conductive elements separated by single conductive elements of the first plurality of conductive elements;

the second plurality of conductive elements are positioned in a second row, the second row comprising pairs of the second plurality of conductive elements separated by single conductive elements of the second plurality of conductive elements; and

the electrically lossy material is selectively electrically coupled to the single conductive elements of the first plurality of conductive elements and second plurality of conductive elements.

22. (Original) The receptacle as defined in claim 21, wherein:

the insert includes projections towards the selected ones of the conductive elements.

23. (Previously presented) The receptacle as defined in claim 1, further comprising an insert disposed between the first and second lead assemblies.

24. (Currently amended) A receptacle adapted for mounting to a printed circuit board, comprising:

a housing having a cavity bounded by a first surface that is parallel to the printed circuit board and a second surface that faces the first surface and is parallel to the printed circuit board;

a first lead assembly including:

a first plurality of conductive elements disposed along a first direction, each comprising a mating contact portion ~~disposed~~ extending along the first surface of the cavity in a second direction perpendicular to the first direction, a contact tail adapted for attachment to the printed circuit board and disposed perpendicular to the mating contact portion, and an intermediate portion coupling the contact tail to the mating contact portion and comprising a right angle bend; and

a first monolithic housing member molded over the intermediate portions of each conductive element of the first plurality of conductive elements; and

a second lead assembly, separate and distinct from the first lead assembly, including:

a second plurality of conductive elements disposed along a first direction, that are longer than the first plurality of conductive elements and each comprise a mating contact portion ~~disposed~~ extending along the second surface of the housing cavity in the second

direction, a contact tail adapted for attachment to the printed circuit board and disposed perpendicular to the mating contact portion, and an intermediate portion coupling the contact tail to the mating contact portion and comprising a right angle bend; and

a second monolithic housing member molded over the intermediate portions of each conductive element of the second plurality of conductive elements; and

wherein the contact tails of the first plurality of conductive elements are aligned along the first direction, and the contact tails of the second plurality of conductive elements are aligned along the first direction.

25. (Currently amended) A receptacle adapted for mounting to a printed circuit board, comprising:

a monolithic housing made of an insulative material and having a cavity bounded by a first surface that is parallel to the printed circuit board and a second surface that faces the first surface and is parallel to the printed circuit board;

~~a shell adapted for attachment of the housing to the printed circuit board;~~

a first lead assembly including:

a first plurality of conductive elements disposed along a first direction ~~including at least six conductive elements~~, each of the first plurality of conductive elements comprising a mating contact portion ~~disposed~~ extending along the first surface of the cavity in a second direction perpendicular to the first direction, a contact tail adapted for attachment to at least one first hole in the printed circuit board and disposed perpendicular to the mating contact portion, and an intermediate portion coupling the contact tail to the mating contact portion and comprising a right angle bend; and

a first monolithic housing member made of an insulative material, ~~and~~ molded over the intermediate portions of each conductive element of the first plurality of conductive elements, and comprising exterior projections extending along the first direction; and

a second lead assembly, separate and distinct from the first lead assembly, including:

a second plurality of conductive elements disposed along the first direction ~~including at least six conductive elements~~, each of the second plurality of conductive elements

comprising a mating contact portion ~~disposed~~ extending along the second surface of the housing cavity in the first direction, a contact tail adapted for attachment to at least one second hole in the printed circuit board and disposed perpendicular to the mating contact portion, and an intermediate portion coupling the contact tail to the mating contact portion and comprising a right angle bend; and

a second monolithic housing member made of an insulative material, ~~and~~ molded over the intermediate portions of each conductive element of the second plurality of conductive elements, and comprising exterior projections extending along the first direction.

26. (New) The receptacle as defined in claim 1, wherein the contact tails of the first and second plurality of conductive elements are configured for attachment to conductive pads on a surface of the printed circuit board.

27 (New) A receptacle adapted for mounting to a printed circuit board, comprising:

a housing made of an insulative material and having:

a first cavity shaped to receive a first plug in an insertion direction, wherein the first cavity is bounded by a first surface that is parallel to the printed circuit board and a second surface that faces the first surface and is parallel to the printed circuit board;

a second cavity offset from the first cavity in a direction perpendicular to the insertion direction, wherein the second cavity is shaped to receive a second plug in the insertion direction, and the second cavity and is bounded by a third surface that is parallel to the printed circuit board and a fourth surface that faces the third surface and is parallel to the printed circuit board;

a first lead assembly comprising:

a first plurality of conductive elements disposed in a row extending in a first direction, each of the first plurality of conductive elements comprising a mating contact portion extending along the first surface of the cavity in a second direction parallel to the insertion direction, a contact tail extending from the monolithic housing, and an intermediate

portion coupling the contact tail to the mating contact portion and comprising a right angle bend; and

a first housing member made of an insulative material, molded over the intermediate portions of each conductive element of the first plurality of conductive elements; and

a second lead assembly, separate and distinct from the first lead assembly, comprising:

a second plurality of conductive elements disposed in a row extending in the first direction, each of the second plurality of conductive elements comprising a mating contact portion extending along the second surface of the first cavity in the second direction, a contact tail extending from the monolithic housing, and an intermediate portion coupling the contact tail to the mating contact portion and comprising a right angle bend; and

a second housing member made of an insulative material, molded over the intermediate portions of each conductive element of the second plurality of conductive elements;

a third lead assembly comprising:

a third plurality of conductive elements disposed in a row extending in the first direction, each of the third plurality of conductive elements comprising a mating contact portion extending along the third surface of the second cavity in the second direction, a contact tail extending from the monolithic housing, and an intermediate portion coupling the contact tail to the mating contact portion and comprising a right angle bend; and

a third housing member made of an insulative material, molded over the intermediate portions of each conductive element of the third plurality of conductive elements; and

a fourth lead assembly, comprising:

a fourth plurality of conductive elements disposed in a row extending in the first direction, each of the fourth plurality of conductive elements comprising a mating contact portion extending along the fourth surface of the second cavity in the second direction, a contact tail extending from the monolithic housing, and an intermediate portion coupling the contact tail to the mating contact portion and comprising a right angle bend; and

a fourth housing member made of an insulative material, molded over the intermediate portions of each conductive element of the fourth plurality of conductive elements;

wherein the first, second, third and fourth housing members engage with the housing to hold the intermediate portions of the first, second, third and fourth plurality of conductive elements relative to the circuit board.

28. (New) The receptacle as defined in claim 27, wherein the contact tails of the first, second, third and fourth plurality of conductive elements are configured for attachment to conductive pads on a surface of the printed circuit board.

29. (New) The receptacle as defined in claim 27, wherein the first housing member engages with the second housing member and the third housing member engages with the fourth housing member.

30. (New) The receptacle as defined in claim 27, wherein:

each of the first, second, third and fourth lead assemblies is L-shaped; and

the first, second, third and fourth housing members engage with the housing so as to hold the first, second, third and fourth lead assemblies within the housing with the L-shaped first, second, third and fourth housing members nested.

Doc Code: TRAN.LET
Document Description: Transmittal Letter

USED IN LIEU OF PTO/SB/21 (07-09)

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission	

Application Number	15/065,683-Conf. #5112
Filing Date	March 9, 2016
First Named Inventor	Donald W. Milbrand, Jr.
Art Unit	2833
Examiner Name	F. O. Figueroa
Attorney Docket Number	A0863.70051US04

ENCLOSURES (*Check all that apply*)

- [x] Fee Transmittal Form
- [ ] Fee Attached
- [x] Amendment/Reply
- [ ] After Final
- [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Reply to Missing Parts/ Incomplete Application
- [ ] Reply to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s) _____
- [ ] Landscape Table on CD
- [ ] After Allowance Communication to TC
- [ ] Appeal Communication to Board of Appeals and Interferences
- [ ] Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- [ ] Proprietary Information
- [ ] Status Letter
- [ ] Other Enclosure(s) (please Identify below):

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	WOLF, GREENFIELD & SACKS, P.C.		
Signature	/ Edmund J. Walsh/		
Printed name	Edmund J. Walsh		
Date	August 21, 2018	Reg. No.	32,950

Certificate of Electronic Filing under 37 C.F.R. § 1.8

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Dated: August 21, 2018 Electronic Signature for: /Trish McDonald/

6553210.1

FEE TRANSMITTAL

Complete if known	
Application Number	15/065,683-Conf. #5112
Filing Date	March 9, 2016
First Named Inventor	Donald W. Milbrand, Jr.
Examiner Name	F. O. Figueroa
Art Unit	2833
Practitioner Docket No.	A0863.70051US04

☐ Applicant asserts small entity status. See 37 CFR 1.27.

☐ Applicant certifies micro entity status. See 37 CFR 1.29. Form PTO/SB/15A or B or equivalent must either be enclosed or have been submitted previously.

TOTAL AMOUNT OF PAYMENT ($)960.00

METHOD OF PAYMENT (check all that apply)

☐ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☒ Deposit Account Deposit Account Number: 23/2825 Deposit Account Name: Wolf, Greenfield & Sacks, P.C.

For the above-identified deposit account, the Director is hereby authorized to (check all that apply):

☐ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, **except for the filing fee**

☒ Charge any additional fee(s) or underpayment of fee(s) under 37 CFR 1.16 and 1.17, **except for any excess claims fees or multiple dependent claim fee** ☐ Charge any additional fee(s) or underpayment of fee(s) under 37 CFR 1.16 and 1.17

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FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES (U = undiscounted fee; S = small entity fee; M = micro entity fee)

	FILING FEES			SEARCH FEES			EXAMINATION FEES			
Application Type	**U ($)**	**S ($)**	**M ($)**	**U ($)**	**S ($)**	**M ($)**	**U ($)**	**S ($)**	**M ($)**	**Fees Paid ($)**
Utility	300	150*	75	660	330	165	760	380	190	
Design	200	100	50	160	80	40	600	300	150	
Plant	200	100	50	420	210	105	620	310	155	
Reissue	300	150	75	660	330	165	2,200	1,100	550	
Provisional	280	140	70	0	0	0	0	0	0	

* The $150 small entity status filing fee for a utility application is further reduced to $75 for a small entity status applicant who files the application via EFS-Web.

2. EXCESS CLAIM FEES

Fee Description	**Undiscounted Fee ($)**	**Small Entity Fee ($)**	**Micro Entity Fee ($)**
Each claim over 20 (including Reissues)	100	50	25
Each independent claim over 3 (including Reissues)	460	230	115
Multiple dependent claims	820	410	205

Total Claims		**Extra Claims**		**Fee ($)**		**Fee Paid ($)**
29	- 24 or HP =	5	x	100.00	=	500.00

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims		**Extra Claims**		**Fee ($)**		**Fee Paid ($)**
4	- 3 or HP =	1	x	460.00	=	460.00

HP = highest number of independent claims paid for, if greater than 3.

Multiple Dependent Claims

Fee ($)	**Fee Paid ($)**

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $400 ($200 for small entity) ($100 for micro entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets		**Extra Sheets**		**Number of each additional 50 or fraction thereof**	**Fee ($)**		**Fee Paid ($)**
	- 100 =		/50 =	(round **up** to a whole number)	x	=	

4. OTHER FEE(S)

	Fees Paid ($)
Non-English specification, $130 fee (no small or micro entity discount)	
Non-electronic filing fee under 37 CFR 1.16(t) for a utility application, $400 fee ($200 small or micro entity)	
Other (e.g., late filing surcharge):	

SUBMITTED BY

Signature	/ Edmund J. Walsh/	Registration No. (Attorney/Agent)	32,950	Telephone	617.646.8000
Name (Print/Type)	Edmund J. Walsh			Date	August 21, 2018

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Dated: August 21, 2018 Electronic Signature for: /Trish McDonald/

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PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 15/065,683	Filing Date 03/09/2016	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $80 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $420 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	08/21/2018	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 29	Minus	** 24	= 5		x $100 =	500
	Independent (37 CFR 1.16(h))	* 4	Minus	*** 3	= 1		x $460 =	460
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	960

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	zuriashwork zenebe
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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FORM PTO-1449/A and B (modified PTO/SB/08)				APPLICATION NO.: 15/065,683	ATTY. DOCKET NO.: A0863.70051US04
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				FILING DATE: March 9, 2016	CONFIRMATION NO.: 5112
				FIRST NAMED INVENTOR: Donald W. Milbrand, Jr.	
Sheet	1	of	1	GROUP ART UNIT: 2833	EXAMINER: F. O. Figueroa

U.S. PATENT DOCUMENTS

Examiner's Initials #	Cite No.	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication or Issue of Cited Document MM-DD-YYYY
		Number	Kind Code		
		5,166,527	A	Solymar	11-24-1992
		7,806,729	B2	Nguyen et al.	10-05-2010
		10,122,129	B2	Milbrand, Jr. et al.	11-06-2018

FOREIGN PATENT DOCUMENTS

Examiner's Initials #	Cite No.	Foreign Patent Document			Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Translation (Y/N)
		Office/ Country	Number	Kind Code			
		WO	2010/030622	A1	Molex Inc.	03-18-2010	

OTHER ART -- NON PATENT LITERATURE DOCUMENTS

Examiner's Initials #	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	Translation (Y/N)

[NOTE – No copies of U.S. patents, published U.S. patent applications, or pending, unpublished patent applications stored in the USPTO's Image File Wrapper (IFW) system, are included. See 37 CFR § 1.98 and 1287OG163. Copies of all other patent(s), publication(s), unpublished, pending U.S. patent applications, or other information listed are provided as required by 37 CFR § 1.98 unless 1) such copies were provided in an IDS in an earlier application that complies with 37 CFR § 1.98, and 2) the earlier application is relied upon for an earlier filing date under 35 U.S.C. § 120.]

EXAMINER:	DATE CONSIDERED:

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

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61/171,066	20 April 2009 (20.04.2009)	US
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(81) **Designated States** *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) **Designated States** *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

(54) **Title**: CONNECTOR WITH IMPEDANCE TUNED TERMINAL ARRANGEMENT

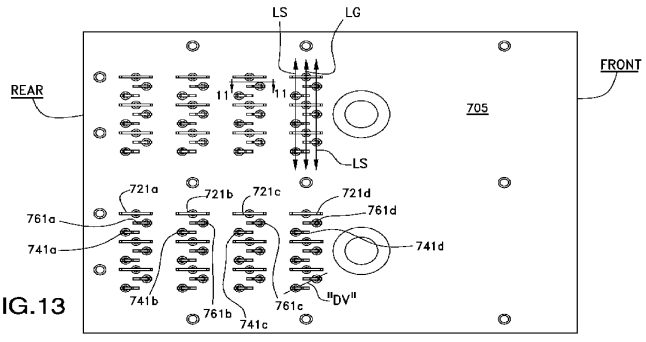


FIG.13

(57) **Abstract**: A connector housing includes a plurality of wafers containing terminal dedicated to either ground signals or differential signals. Terminals in adjacent wafers can be arranged to provide broadside coupled differential signal pairs. Terminals dedicated for use as ground terminals can be wider than the signal terminals to provide shielding between adjacent differential signal pairs. The signal terminals of each differential signal terminal pair can a constant width from their contact portions to a location proximate their tail portions and the terminals diverge from broadside alignment and increase in their width until they end at the terminal tail portions.

WO 2010/030622 A1

PATENT

Connector With Impedance Tuned Terminal Arrangement

Reference to Related Applications

[0001] This application claims priority to United States Provisional Appln. No. 61/095,450, filed September 9, 2008; to Appln. No. 61/110,748, filed November 3, 2008; to Appln. No. 61/117,470, filed November 24, 2008; to Appln. No. 61/153,579, filed February 18, 2009, to Appln. No. 61/170,956 filed April 20, 2009, to Appln. No. 61/171,037, filed April 20, 2009 and to Appln. No. 61/171,066, filed April 20, 2009, all of which are incorporated herein by reference in their entirety. This application was filed concurrently with the following application, which is not admitted as prior art to this application and which is incorporated herein by reference in its entirety:

Application Serial No. TBD , entitled FLEXIBLE USE CONNECTOR, and having Attorney Docket No. A9-043J-PCT.

Background of The Invention

[0001] The present invention generally relates to connectors suitable for transmitting data, more specifically to input/output (I/O) connectors with improved electrical performance.

[0002] There is an ongoing effort in the telecommunications field to increase performance, while reducing the size of connectors used in the field. For I/O connectors used in data communication, these efforts create somewhat of a problem. Using higher frequencies (for increased data rates) requires reliable electrical separation between signal terminals in a connector that minimizes cross-talk. However, reducing the size of the connector and making the terminal arrangement more dense, brings the terminals closer together, which typically results in a decrease in electrical separation.

[0003] There is also a desire to improve manufacturing. For example, as signaling frequencies increase, the tolerance of locations of terminals, as well as their physical characteristics become more important in that they influence the operation of the connector. Therefore, certain individuals would appreciate improvements to a connector

design that would facilitate manufacturing while still providing a dense, high-performance connector.

Summary Of The Invention

[0004] A connector assembly includes a hollow housing supports a plurality of wafers. Each wafer includes an insulative frame that supports multiple terminals. Each terminal includes a tail portion positioned along a mounting face of the connector and a contact portion positioned at a mating face of the connector and a body portion therebetween. The mounting and mating faces can be arranged so that they are at right angles to each other. The mating face can include two card-receiving slots. The wafers can be configured to provide either ground terminals or signal terminals and the wafers can be arranged in a predetermined pattern. For example, wafers can be configured so that there is one ground wafer and two signal wafers and each wafer has a different exterior shape and can only be inserted into the housing in particular locations. Wafers supporting signal terminals are configured so that the signal terminals in adjacent wafers can be broadside coupled together. A wafer supporting ground terminals can be positioned between two pair of wafers that support broadside coupled signal terminals and body portions of the ground terminals can be wider than body portions of the signal terminals. In an embodiment, the signal terminals that form a broadside coupled pair are kept a consistent distance apart through the body portion but have tails that diverge away from each other. To help reduce impedance changes through the tail portion, the tail portions can be wider. The tails portions diverge away from each other in a symmetric manner.

Brief Description Of The Drawings

[0005] Throughout the course of the following detailed description, reference will be made to the drawings in which like reference numbers identify like parts and in which:

[0006] FIG. 1 illustrates a perspective view of an embodiment of a connector;

[0007] FIG. 2 illustrates a sectional view of the connector depicted in FIG. 1, taken along lines **2-2** thereof;

[0008] FIG. 3 illustrates a sectional view of the connector depicted in FIG. 1, taken along lines **3-3** thereof;

[0009] FIG. 4 illustrates a perspective view of the connector depicted in FIG. 1, with the housing front portion removed to show the internal terminal assemblies;

[0010] FIG. 5 illustrates a sectional view of the connector of FIG. 1, taken along lines **5-5** thereof;

[0011] FIG. 6 illustrates a perspective view of an underside of the connector depicted in FIG. 1;

[0012] FIG. 7 illustrates an elevated side view of an embodiment of an array of ground terminals as may be supported within a ground wafer;

[0013] FIG. 8. illustrates a sectional view taken through a stack of terminal assemblies of the connector of FIG. 1 with the supporting frame of the wafer removed;

[0014] FIG. 9 illustrates a perspective detailed view of an embodiment of an array of broadside coupled signal terminals flanked by ground terminals;

[0015] FIG. 10 illustrates another perspective view of the terminals depicted in FIG. 9 with one set of ground terminals removed;

[0016] FIG. 11 illustrates an enlarged elevated side detail view of the terminals depicted in FIG. 10;

[0017] FIG. 12 illustrates a sectional view of FIG. 11, taken along lines **12-12** thereof;

[0018] FIG. 13 illustrates a top plan view of an array of terminals removed from their supporting wafers and sectioned in the same manner as FIG. 12;

[0019] FIG. 14 is a sectional view taken through a ground terminal assembly of the connector of FIG. 1;

[0020] FIG. 15A illustrates an embodiment of a board with an exemplary via pattern; and

[0021] FIG. 15B illustrates an embodiment of board with a ganged array of the via pattern depicted in FIG. 15A.

Detailed Description Of The Illustrated Embodiments

[0022] As required, detailed embodiments are disclosed herein; however, it is to be understood that the disclosed embodiments are merely exemplary. Therefore, specific details disclosed herein are not to be interpreted as limiting, but merely as a basis for the

claims and as a representative basis for teaching one skilled in the art to variously employ the disclosure in virtually any appropriate manner, including employing various features disclosed herein in combinations that might not be explicitly disclosed herein.

[0023] FIG. 1 illustrates a connector 100. The connector 100 includes a housing 101, which may be formed of a insulative material and is illustrated as having two interengaging first and second (or front and rear) pieces, or parts, 102, 103. The housing 101, as shown in FIG. 1, has a wide body portion 104 that extends between a rear face 105 and the front face 106. A mating portion 107 that takes the form of an elongated nose portion 108 projects forwardly of the front face 106 and terminates in a front mating face 109. The mating face 109 may have one or more circuit card-receiving slots 110 which are formed widthwise in the mating face 109, with two such slots 110 being shown in FIG. 1.

[0024] As shown in FIGS. 2-3, the housing 101 has a hollow interior portion 112 that receives a plurality of individual terminal assemblies 114 that take the form of a wafer 115. Each such wafer 115 contains a plurality of conductive terminals 116, and each such terminal includes tail portions 117 projecting out from a first edge 118 and contact portions 119 projecting from a second edge 120 of the wafer 115. In the illustrated embodiment, the two edges 118, 120 are adjacent each other and at a right angle to each other. The first edge 118 of the terminal assemblies 114 serves as a mounting face for the block of terminal assemblies shown in FIG. 4. The second edge 120 serves as a mating face for the terminal assemblies 120. The terminals 116 further include body portions 121 that interconnect the tail portion 117 and contact portions 119 together. The wafer 115 may have openings 123 formed therein in the form of slots that extend along the terminal body portions 121 to expose them to air and thereby affect the terminal impedance.

[0025] The terminal assemblies 114 are held together as a block within the housing 101 in a manner such that the terminal tail portions 117 extend out through the bottom of the housing 101 and the terminal contact portions 119 extend from the edges 120 of their wafers 115 into the housing nose portion 108. The terminal contact portions 119 are arranged in the wafers 115 as pairs of terminals and these pairs are located on the upper

and lower sides of the card-receiving slots 110. (FIGS. 2 and 3.) As explained in greater detail below, the depicted terminals 116 are arranged in sets of ground terminals 116b or signal terminals 116a within a wafer, with certain wafers containing only ground terminals 116b and other wafers containing only signal terminals 116a. In an embodiment, two signal terminal-carrying wafers are arranged side-by-side such that they define pairs of signal terminals 116a which are broadside coupled. In this manner the terminals can transmit differential signals through the connector.

[0026] The terminals 116 are further provided as sets of thin signal terminals 116a as shown in FIG. 2, and wide ground terminals 116b, as shown in FIG. 3. All of the terminals 116, as noted above, project forwardly from the second edge 120 of the terminal assembly wafers 115 and selected portions 124 of the wafers 115 extend past the second edge 120. The selected portions 124 are provided to hold the terminal contact portions 119 in place within the forward nose portion and to move the point "**P,**" around which the terminal contact portions deflect, into the nose portion 108 of the housing 101, as shown in FIG. 3. As shown in FIG. 6, the terminal tail portions 117 of each distinct set of wafers 115 are aligned laterally (widthwise) of the connector 100. That is, the ground terminal tail portions 117b are arranged on respective widthwise lines, or common axis, such as "**LG**" in FIG. 6. Likewise, the signal terminal tail portions 117a can also be arranged along their own coincident lines "**LS**". It can be seen that the two signal lines **LS** lie on opposite sides of the ground line **LG**.

[0027] As can be understood from the drawings, the contact portions 119 are cantilevered in their structure and act as contact beams that deflect away from the slots 110 when a circuit card is inserted therein. In order to accommodate this upward and downward deflection of the contact portions 119, the nose portion 108 of the housing 101 has terminal-receiving cavities 125 that extend from a vertical preselected above and below centerlines of each slot 110. Preferably, as will be explained more below, the ends of the selected portions 124 run along a line "**D**" that is close to, or most preferably, substantially coincident with the deflection points "**P**" (FIG. 2.). The connector 100 may be enclosed in a shielded, exterior housing, not shown, and as such, the height of the connector is restricted, not only to a height that will fit inside of an exterior housing, but

also a height that accommodates the two edge, or paddle, cards of an opposing connector while allowing that opposing connector to be compactly designed.

[0028] Returning to FIGS. 1-4, the housing 101 has its two pieces 102, 103 mate along an irregular mating line 126 that extends upwardly through the sides of the housing 101 along a path that extends from front to rear of the housing 101. This irregular mating line facilitates the molding of the housings and it is explained in greater detail in United States Provisional Patent Application No. 61/122,102, filed December 12, 2008 for "Two-Piece Thin Wall Housing." The two housing parts 102, 103 interlock together or engage with each other along this irregular and non-linear mating line 126. With this irregular configuration, a pair of rails 128 and channels 129 are defined in the two housing pieces 102, 103 with the rails 128 fitting into the channels 129. Outer ribs 131 may also be formed on the exterior side surfaces of the rear housing part 103 and these ribs 131 are preferably horizontally aligned with the rails 128 to provide reinforcement to the rails 128 and can also provide a means for positioning the connector subassembly 100 within an exterior housing or shield.

[0029] FIG. 5 is a rear elevational view of the connector 100. The hollow interior is configured to provide different slots for the different ground and signal terminal assembly wafers. This configuration, while not required, can help prevent incorrect assembly of wafers in the connector. This configuration also permits the different types of wafers to be located and inserted as groups.

[0030] As depicted, the wafer at the leftmost edge of the interior of the housing 101 is a first wafer 115a. In order from the left, a second wafer 115b is beside the first wafer 115a and a third wafer 115c is beside the second wafer 115b. If the first wafer 115a is a ground wafer (it supports ground terminals) and the second and third terminal 115b, 115c are each a signal wafer (they support signal terminals), the depicted configuration supports a repeating pattern of ground, signal, signal wafers. This allows two terminals in adjacent signal wafers to form a differential pair that can be coupled together (as depicted, broadside coupled) as terminal pair while providing a ground wafer between the broadside coupled terminals. As can be appreciated, therefore, the connector can have a plurality of signal wafers that form pairs of coupled differential signal terminal and each

pair of signal wafers is separated by a ground wafer. In an embodiment, broadside-coupled terminal pairs can be arranged in four rows of terminals, 140a, 140b, 140c and 140d. The differential signal terminal pairs in rows 140a and 140c engage contacts disposed on the upper surfaces of two edge cards of an opposing, mating connector (not shown), while the differential signal terminal pairs in rows 140b and 140d engage contacts disposed on the lower surfaces of the two edges cards.

[0031] As depicted, each wafer is polarized, or keyed, by virtue of its external configuration. The ground wafer 115a has a first height and as depicted is taller than the signal wafers 115b, 115c. Consequentially, the ground wafer 115a can only be inserted into the slots 169a disposed in the front half 102 of the housing 101. The second wafer 115b is configured with a step 168b with a first orientation that allows the second wafer 115b to mate with a slot 169b but does allow insertion into slot 169c. The third wafer 115c has a step 168c that allows it to be received in slot 169c.

[0032] Theses steps 168b, c that are formed in the signal terminal assembly wafers 115b, 115c engage two sides of projection member 170 of the housing 101. Other means of polarizing, or keying, the wafers 115 may be utilized, such as varying the height of the wafers 115 and the slots 169. In this manner, each distinct set of terminal assembly wafers may be loaded into the housing 101 as a group to facilitate assembly. One aspect that can be appreciated is that the three-wafer system can be stitched into the housing interior 112 without first combining two or more of the wafers 115 together, so that each set of wafers is fully stitchable. This has the benefit of providing a convenient manufacturing process. Importantly, due to the difference of heights and or steps, when the taller wafer is inserted first, the proper wafers can only be inserted into their predetermined slots, thus providing a high performance three-wafer construction while ensuring the wafers are installed properly.

[0033] It should be noted that while a poke-a-yoke type assembly configuration for a wafer has been determined to be desirable, it is not required. Furthermore, the additional height used for the wafers that support the ground terminals is also not required. One benefit of using the taller wafers for ground terminals is that the additional space makes it easier to use wider ground terminals. To provide the poke-a-yoke assembly

configuration, however, one can also use wafers with other shapes, such as a V or inverted V shape that only allows those wafers to be inserted in the appropriate channels in the housing.

[0034] FIG. 7 illustrates a ground terminal assembly 7000 removed from its supporting insert wafer frame, illustrating that ground terminals 7010 are significantly wider than their corresponding signal terminals. This difference is size occurs primarily in the width dimension of the ground terminals and FIG. 8 illustrates the size difference by showing a signal terminal assembly 8000, also removed from its supporting insert wafer frame. The signal terminals 116a of this assembly 8000 are illustrated in broadside alignment with a set of adjacent ground terminals 116b. The signal terminals have contact portions 743 that will engage the opposing surfaces of edge cards 89 of an opposing, mating connector 88 (FIG. 8), tail portions 722 that fit into vias 709 or other openings in a circuit board and body portions 8012 that connect the contact and tail portions together.

[0035] Four ground terminals 721a-d are illustrated in FIG. 7, and each ground terminal can be seen to have contact portions 723 at one end and tail portions 722 at opposing ends. The contact portions 723 and tail portions 722 are joined by intervening body portions 725 that extend therebetween. As shown, each of the ground terminal body portions includes a vertical component 725' extending to the tail portion 722 and a horizontal component 725" extending to the contact portion 723. Three of the terminals shown further include an angled component 7210, while the remaining ground terminal 721d, the one that is nearest to the intersection of the housing mating face and mounting face, has no such angled component.

[0036] In an embodiment, manufacturability of the connectors can be increased by the configuration of the ground terminals 116b. As shown best in FIGS. 7 and 8, some of the ground terminals 721a-c of each ground terminal insert wafer are provided with notches 726 that are formed in the edges of the ground terminal body portions 121b. These notches 726 are provided in sets of pairs of notches, with each notch 726 of each pair extending inwardly of the ground terminal from the opposing outer edges 725a of the terminal body portions. Preferably, the pairs of notches 726 are formed in the angled

components 7210 of the terminal body portions 725, and not in either of the vertical or horizontal components 725', 725".

[0037] As shown in the Figures, the notches 726 of each pair of notches are aligned with each other so that their inner edges 726a confront each other. The notches 726 are formed in the terminal body portion angled components, where the ground terminal body portions are the widest. These notches 726 provide improved retention of the ground terminals 116b within each such ground terminal assembly wafer 115a. The notches 726 also facilitate the molding of the ground terminal assembly wafers 115a by providing additional, interconnected flowpaths for the molding material to traverse during the molding of the wafer 115a over the wide ground terminals 116b. In this regard, and as shown, the notches 726 of the ground terminals 116b are offset from any of the notches in any adjacent ground terminals. This type of alignment is preferred because the notches provide areas of strength where the molding material from which the ground terminal insert wafer is made may extend from one side of the wafer to the other side, through the plane of the ground terminal body portion notches. As shown in FIG. 8, three terminals 721a-c of the four ground terminals 116b of each ground terminal assembly wafer 115b have at least one pair of notches 726, but the lowermost ground terminal 721d, which has no significant body portion angled component 7210 has no notches. This lowermost (fourth) ground terminal 721d is the terminal that is nearest the intersection of the housing mating and mounting faces.

[0038] The ground terminals, as shown in FIG. 8, also have a narrow horizontal length where the ground terminals are reduced in their width, but still are wider than either of the two signal terminals adjacent thereto. This assists in reducing the overall height of the terminal assembly. This reduced height and reduced parallel length reduces the crosstalk over the length of the terminals even in the horizontal extents, and as they approach the contact portions the ground terminals are wider than their corresponding and adjacent signal terminals.

[0039] One issue with respect to electrical separation in a stacked connector is that electrical separation between horizontally arranged differential signal terminal pairs is relatively easy to attain in a compact area by using ground shields, or ground terminals that extend in vertical columns disposed between the differential signal terminal pairs.

The ground terminals can couple with the adjacent signal pairs and helps limit any coupling between two adjacent differential pairs. However, maintaining electrical separation between horizontal rows of differential signal pairs can be more difficult to ensure. One method of doing so would be to include ground shields between the rows but this would be somewhat problematic because the small dimensions of the connector make it difficult to have additional terminals or shielding in the wafers, especially near the mating face of the connector. The difficulty in ensuring electrical separation between rows is increased in connectors with small height dimensions, such as the connectors depicted herein, and particularly if the connector system utilizes edge cards as a mating interface.

[0040] To address this issue, the depicted connector provides wafers where the signal terminals 116a are first separated by an edge-to-edge spacing of **D1** between adjacent vertical components 742c of the signal terminal body portions 742. That spacing **D1** is reduced by about 20% to an edge-to-edge spacing **D2** between the angled components 742a of the signal terminal body portions 742, and that spacing **D2** is again reduced by about another 20% to an edge-to-edge spacing **D3** between the horizontal components 742b of the signal terminal body portions 742. The spacing **D1**, **D2** and **D3** is between differential pairs and serve to isolate the pairs. As the separation distance decreases, the likelihood of bothersome crosstalk rises.

[0041] It can be appreciated that the spacing **D3** is about 40% less than the spacing **D1** and hence the likelihood of crosstalk between the differential signal terminal pairs in the rows 140a and 140b increases. It has been determined that reducing the distance that the rows are separated by the distance D3 (which is driven by the fact that the connector provides two card receiving slots on the mating face) helps improve the performance of the connector. In this regard, the use of the angled portions of the terminal body portions is effective in reducing the horizontal components 742b of rows of adjacent differential signal terminal rows, rather than pure right angle configured terminals. With the angled portions, the horizontal components 742b of the signal terminals do not extend past the angled line "**V**", shown in FIG. 8, which runs diagonally between opposite corners of the terminal wafers. This terminal configuration thereby minimizes the length of the signal terminal horizontal components at the reduced spacing in an attempt to keep undesirable

crosstalk down to a minimum. Preferably the horizontal length of the topmost signal terminal (e.g., the longest horizontal terminal length, "**TTL**") does not exceed about 60% of the length "**WL**" as shown in FIG. 8, which is the distance from the rear edge of the wafer to the forward edge of the wafer portion 124 separating a row of adjacent terminals.

[0042] In order to increase the electrical separation and minimize cross talk between adjacent rows of differential signal terminal pairs, the terminal assembly wafers are each preferably provided with a plurality of recesses, or channels, 900 that extend widthwise, or transversely through the connector between the horizontal extents of the signal terminal body portions 742 as best illustrated in FIG. 8. These channels locate pockets of air between the adjacent rows 140a-d of signal terminal pairs, the pockets of air serving to provide greater electrical separation, and are preferably located proximate to the intersection of the horizontal and angled components of the ground terminal body portions. By using distinct channels as opposed to continuous slots, the strength of the wafer 115 can be maintained and a desired spring force is maintained so the ground and signal terminal contact portions 723, 743 apply a certain contact force on an edge card 89 inserted therebetween.

[0043] It should be noted, as can be appreciated from FIG. 10, that adjacent signal terminals are positioned a first distance apart and that distance is maintained through the body of the terminal. The distance between the terminals increases, however, at a divergent body portion near the tails. More will be discussed regarding this point below.

[0044] As can be appreciated, the terminal configuration of the illustrated embodiments provides broad-side coupled differential signal terminals through the terminal insert wafers between the mating and mounting faces of the housing. Due to the desired small size of the connectors of the present invention, the tails 744 of the signal terminals 116a are preferably spread apart from each other, rather than aligned with each other and the ground terminal tail portions 722. This is done to accommodate a pattern of respective ground and signal vias 708, 709 in a circuit board 705 which provides enough space for necessary exit traces as well as for a secure mechanical connection. In addition, the use of adjacent, broadside coupled terminals (if the side-by-side arrangement was

maintained) would result in via spacing that could weaken the circuit board in an undesirable manner. Therefore, it has been determined that spacing the vias 708, 709 apart helps provide sufficient space in which to drill the via patterns while maintaining mechanical integrity of the circuit board 705.

[0045] One issue with such a configuration is that the adjacent ground terminal typically is not wide enough to effectively shield the two spaced-apart terminals. One method to address shielding the terminals at the board interface is to use two or more vias and have a portion of the ground terminal couple multiple ground terminals together. Such a configuration, however, is less suitable for smaller, high-density connectors.

[0046] It has been discovered, however, that the ground terminals of the present invention can maintain their wider configuration all the way to the circuit board, as illustrated in FIGS. 9-14. In other words, the ground retains a width that is substantially wider than the signal terminal beyond an edge of the frame of the wafer. This allows for effective shielding up to the circuit board interface, while still allowing for a compact design, as discussed above. In an embodiment, the ground terminals may be configured so that they are at least as wide as the signal terminals over the entire path between the first side and the second side of the wafer.

[0047] In an embodiment, the body portions of the signal terminals nearest their tail portions are specially configured to reduce skew. Turning to FIGS. 11 & 12, a wide ground terminal 721a is shown located next to a first (right) signal terminal 761a and a second (left) signal terminal 741a. The two signal terminals 761a, 741a are arranged in confronting pairs of terminals and are associated with at least one ground terminal 721a. The ground terminal body portion 725 is larger in size than either of the first and second signal terminals, while the dimensions of the signal terminals 761a, 741a, remain constant relatively from their contact portions 743 through their body portions 742 until proximate to the signal terminal tail portions 744, where the body portions diverge from their confronting relationship.

[0048] As shown in the enlarged detailed view of FIG. 11, the first and second signal terminal body portion vertical components 742c diverge longitudinally (e.g., from left to right or right to left in FIG. 13) from their confronting alignment along an axis of symmetry "**AS**" that extends down the centerline of the differential signal pair to form

divergent body portions 742d. The first terminal 761a diverges toward the rear of the terminal assembly wafer (or to the right in FIG. 11), while the second signal terminal 741a diverges toward the front of the terminal assembly wafer (or to the left of FIG. 11). As the first and second signal terminals diverge longitudinally, they do so preferably symmetrically, i.e., in either the front to back or back to front directions, the spacing of the terminal edges stays the same for the signal pair. For example, the end points "**A**" and "**B**" shown in FIG. 11 will be spaced the same horizontal distance from the axis "**AS**", as well as any point on the interior of the terminal tails, such as "**C**". This symmetry not only extends along a vertical axis **AS**, but also it preferably extends from any horizontal axis, typically a longitudinal one (extending from front to back or back to front of the connector) chosen in the tail body portions, i.e., even the singulation terminal stubs 745 of the signal terminal body portions will be the same distance from any chosen horizontal datum, such as "**AH**". This bidirectional symmetry reduces the skew of the connectors. Additionally the boundaries **B2** of the signal terminals fall within the boundary B1 of the side edges of the ground terminals, including their singulation portions.

[0049] As the signal terminal body portions transition from their vertical components 742c (which, as noted above, are a first distance apart) to their divergent portions 742d, the width of the signal terminals is increased. This helps modify capacitance between the signal terminals that make up the differential signal pair and helps compensate for the increased separation between the terminals. As can be appreciated, controlling the capacitance helps control the inductance and therefore can help reduce any impedance discontinuity. In an embodiment, the divergent portions (at approximately point **A**) are at least 30 percent larger and preferably are between about 45% to about 60% larger than the body portions 742 (at an angled component of the terminal body portion). It can be appreciated from the Figures that the signal terminal body portions have a relatively constant width, while the signal terminal divergent body portions have a variable width which changes as the terminals diverge from each other. Thus, the impedance and skew of the terminals may be controlled. In this manner, the mounting of the differential signal terminal tails is also facilitated in that the tail portions of the first and second signal terminals are spaced apart, or offset, from each other along their own common axis "**LS**"

that lie on opposite sides of the ground terminal tail portion common axis "**LG**". Thus, a simple via pattern may be utilized and drilled into a supporting circuit board 705 in diagonal rows as shown best in FIG. 13. The vias for each differential signal terminal pair are arranged in diagonal rows adjacent each ground terminal as shown by the line "**DV**" in FIG. 13.

[0050] This pattern of terminals facilitates a repeating three wafer system that can provide a ground, signal, signal pattern that repeats and separates pairs of signal terminals with ground terminals. The adjacent signal terminals provide good differential coupling while the relatively wider ground terminals help provide electrical shielding between differential pairs in the same row. In other words, the wider grounds help ensure electrical separation between pairs of adjacent signal terminals.

[0051] Turning to FIGS. 15A-15B, a via pattern 1010 is depicted. The via pattern includes rows 1012 that that are configured to receive terminal tails associated with terminals that are provided on one side of a card-receiving slot. Thus, with four rows 1012, the via pattern 1010 is configured to correspond to a dual card-slot connector. As can be further appreciated, each row comprises a first via 1015, a second via 1016 and a third via 1017. The third via 1017 forms a line down a center of the row and the first and second via 1015, 1016 are spaced an equal distance on both sides of the line. In operation, the first and second via can be configured for use as signal vias for a differential pair and the third via provides a ground terminal. Because of the alignment of the signal vias and ground vias in the via pattern 1010, it is straightforward to route all the traces away from the vias. For a multi-layer board, it is relatively straightforward to route the traces away from the via pattern without substantially going substantially outside the boundary of the via pattern 1010. For example, the traces can be configured so that they only extend outside the via pattern 1010 on one side of the via pattern 1010.

[0052] As can be appreciated, therefore, the via pattern 1010 can be repeated for each connector and this repeatability enables a 1x4 ganged solution on a board with via patterns that are identical. With the depicted connector configuration, the board is configured to receive two single connectors (1x1) that are placed in two nonadjacent via patterns 1010. Or, alternatively, a 1x2 ganged connector can be placed in two adjacent via patterns and a 1x1 connector can be placed in a spaced apart via pattern. Or a 1x4

ganged connector can be mounted to the board. Thus a single board pattern is configured to receive at least three variations in connectors, including a 1x4 ganged connector, a 1x2 and a 1x1 connector, or 2 1x1 connectors. Therefore, unlike conventional via patterns where the via pattern is limited to a particular connector configuration, the depicted board configuration provides substantially more flexibility. As can be appreciated, this simplifies board manufacture as it becomes simple to provide four via patterns in a ganged array and then populate the board with a desired connector configuration (as is appropriate for the particular end product). Thus, the depicted design of the gnaged 1x4 via pattern 1010, while not required, can provide improvements in the usefulness of a circuit board.

[0053] It will be understood that there are numerous modifications of the illustrated embodiments described above which will be readily apparent to one of skill in the art, such as many variations and modifications of the compression connector assembly and/or its components including combinations of features disclosed herein that are individually disclosed or claimed herein, explicitly including additional combinations of such features, or alternatively other types of contact array connectors. Also, there are many possible variations in the materials and configurations. These modifications and/or combinations fall within the scope of knowledge of a person of ordinary skill in the art and unless otherwise noted are intended to be within the scope of the appended claims. It is noted, as is conventional, the use of a singular element in a claim is intended to cover one or more of such an element.

CLAIMS

What is claimed is:

1. A connector, comprising:

a housing having a mating face and a mounting face;

a plurality of first wafers disposed within the housing, the first wafers each supporting a plurality of ground terminals, each ground terminal having a contact portion, a tail portion and an intervening body portion;

a plurality of second wafers disposed within the housing, each second wafer supporting a plurality of first signal terminals, each first signal terminal having a contact portion, a tail portion and an intervening body portion;

a plurality of third wafers disposed within the housing, each third wafer supporting a plurality of second signal terminals, each second signal terminal having a contact portion, a tail portion and an intervening body portion, wherein the second and third wafers are arranged to be positioned adjacent each other to form a pair of wafers with a first wafer position between each pair of wafers, the signal terminals in the pair of wafers being positioned in alignment so that the signal terminals in the adjacent wafer are, in operation, coupled together and the body portions of the coupled signal terminals are positioned a first distance apart, and wherein the signal terminals include divergent portions adjacent the tail portions, the divergent portions causing the signal terminals to be separated by a second distance that is greater than the first distance.

2. The connector of claim 1, wherein the body portions of the signal terminals have a first width and the divergent portions have second width, the second width being larger than the first width.

3. The connector of Claim 2, wherein the second width is at least 30% larger than the first width.

4. The connector of Claim 2, wherein the ground terminal body portion has third width which is greater than the second width.

5. The connector of Claim 1, wherein the ground terminal tail portions are aligned along a first common axis and the first and second signal terminal tail portions are respectively aligned along second and third common axis, the second and third common axis being disposed on opposite sides of the first common axis.

6. The connector of Claim 1, wherein the first and second divergent portions are symmetrical to each other around a first axis of symmetry.

7. The connector of Claim 6, wherein the first and second signal terminal divergent body portions are symmetrical to each other around a second axis of symmetry.

8. The connector of Claim 7, wherein the first and second axis of symmetry extend in different directions.

9. The connector of Claim 6, wherein the first axis of symmetry extends in a longitudinal direction.

10. The connector of Claim 1, wherein the ground terminal is wider than an overlap of a combination of the first and second signal terminal body portions.

11. The connector of Claim 1, wherein the first, second and third wafers each includes a channel that extends a width of the respective wafer, each channel defining an air pocket between terminals in the same wafer.

12. The connector if Claim 1, wherein the first and second signal terminal body portions have a horizontal component with a first length and the second and third wafer have a horizontal length, and the first length is not more than about 60% of the horizontal length.

13. A connector, comprising:

a housing, the housing having a mating face for engaging with an opposing connecting element, and a mounting face for mounting the connector to a circuit board;

a plurality of conductive signal and ground terminals supported in the housing, the signal terminals being arranged in sets of differential signal terminal pairs, each differential signal terminal pair having at least one ground terminal associated therewith, the signal terminals having contact portions that extend along the connector mating face and tail portions that extend along the connector mounting face and body portions that

interconnect the signal terminal contact and terminal portions together, the signal terminal body portions further including divergent body portions interconnecting the signal terminal tail and body portions together; and

the differential signal terminal pairs being arranged in side-by-side in order to effect broadside capacitive coupling therebetween from the signal terminal contact portions to the signal terminal divergent body portions, and wherein the signal terminal divergent body portions diverge longitudinally from the side-by-side order.

14. The connector of Claim 13, wherein the signal terminal tail portions of each of the differential signal terminal pairs are longitudinally spaced apart from each other

15. The connector of Claim 14, where each of the ground terminals includes a contact portion aligned with the differential signal terminal pair contact portions, a tail portion and a body portion interconnecting the ground terminal contact and tail portions together, the ground terminal body portion confronting one of the signal terminal body portions.

16. The connector of Claim 15, wherein the ground terminal body portion is wider than either of the differential signal terminal pair body portions.

17. The connector of Claim 15, wherein the signal terminal tail portions of each of the differential signal terminal pair lie on opposite sides of the tail portion of an associated ground terminal.

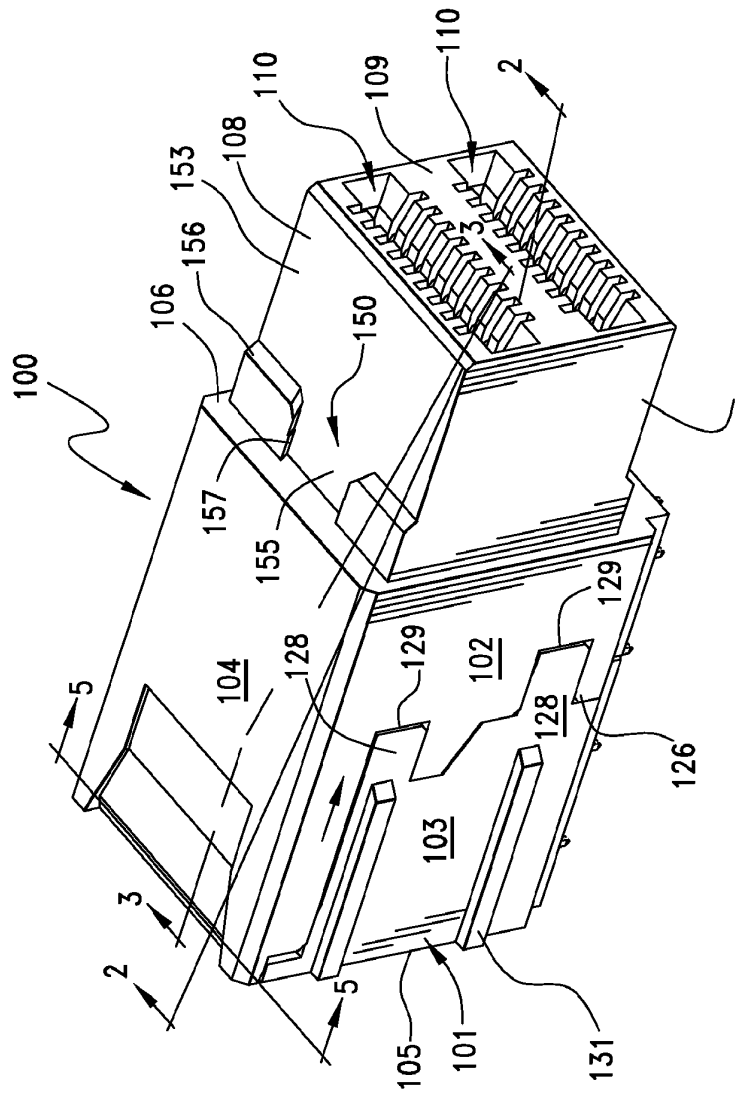
18. The connector of Claim 15, wherein the signal terminal tail portions are arranged in an imaginary diagonal line.

19. The connector of Claim 13, wherein the signal terminal body portions have a first width and the signal terminal divergent body portions have a second width, the first width being a constant width and the second width being a variable width.

20. The connector of Claim 13, wherein the first and second signal terminal divergent body portions are symmetrical with each other around a first axis of symmetry.

21. The connector of Claim 20, wherein the first and second signal terminal divergent body portions are symmetrical with each other around a second axis of symmetry.

22. The connector of Claim 13, wherein the first and second axis of symmetry extend in different directions.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103
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101
131

FIG.1

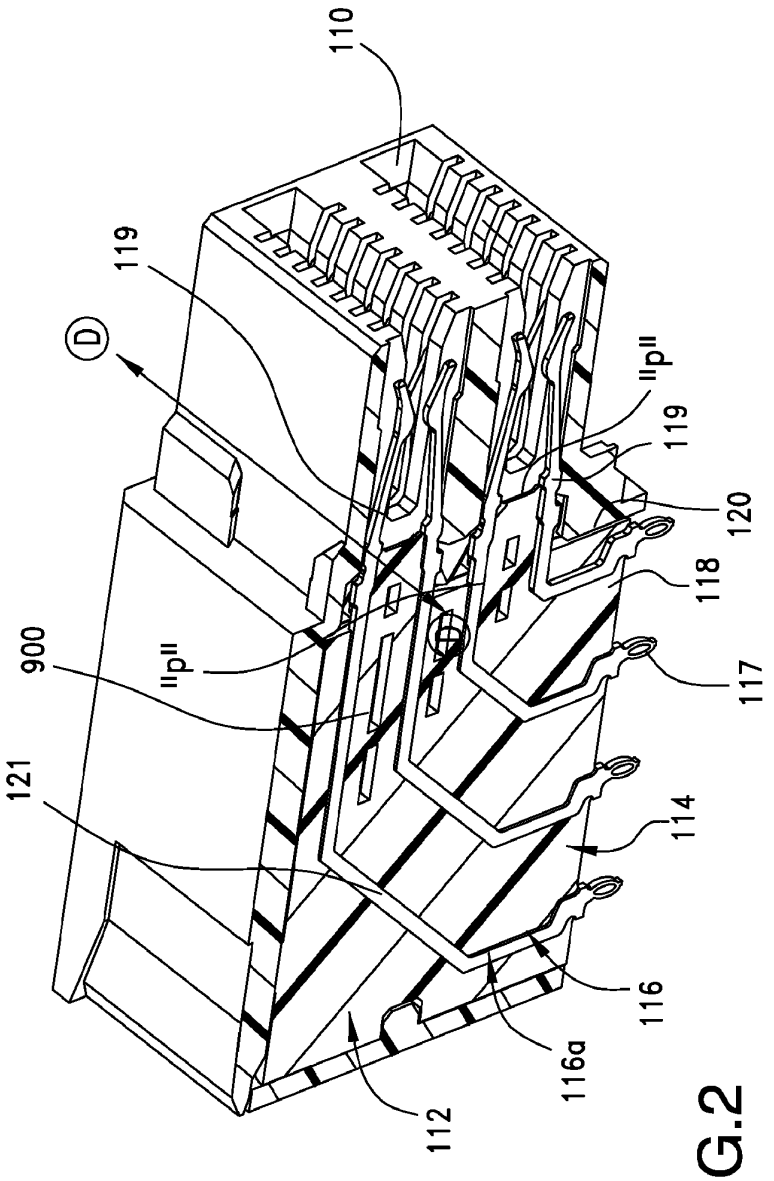
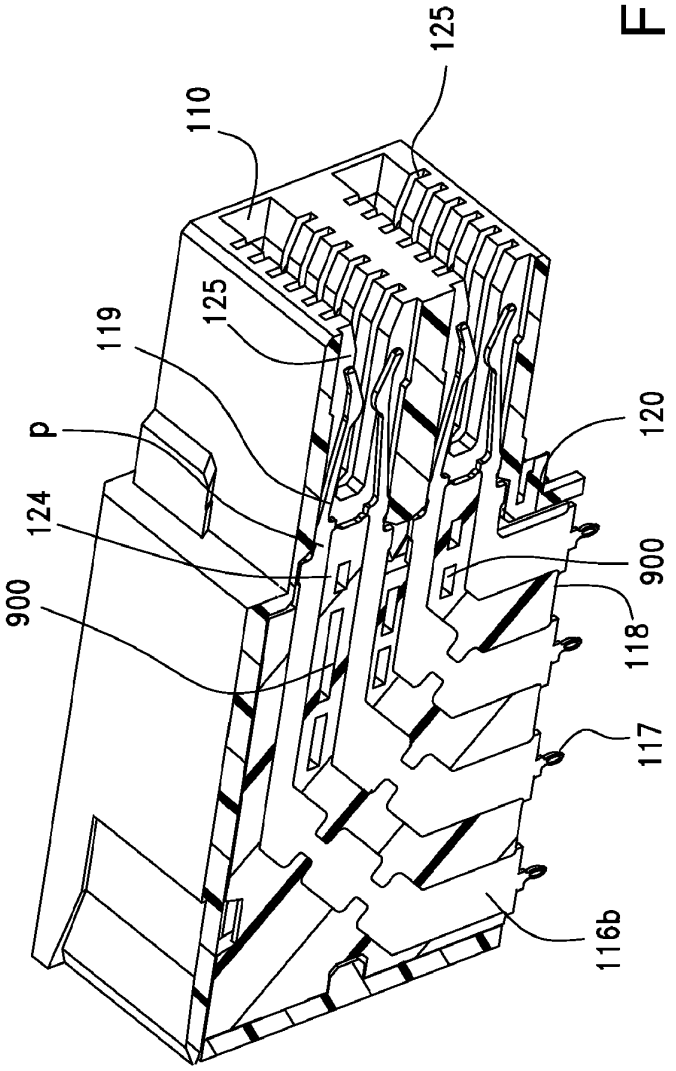


FIG.2

FIG.3



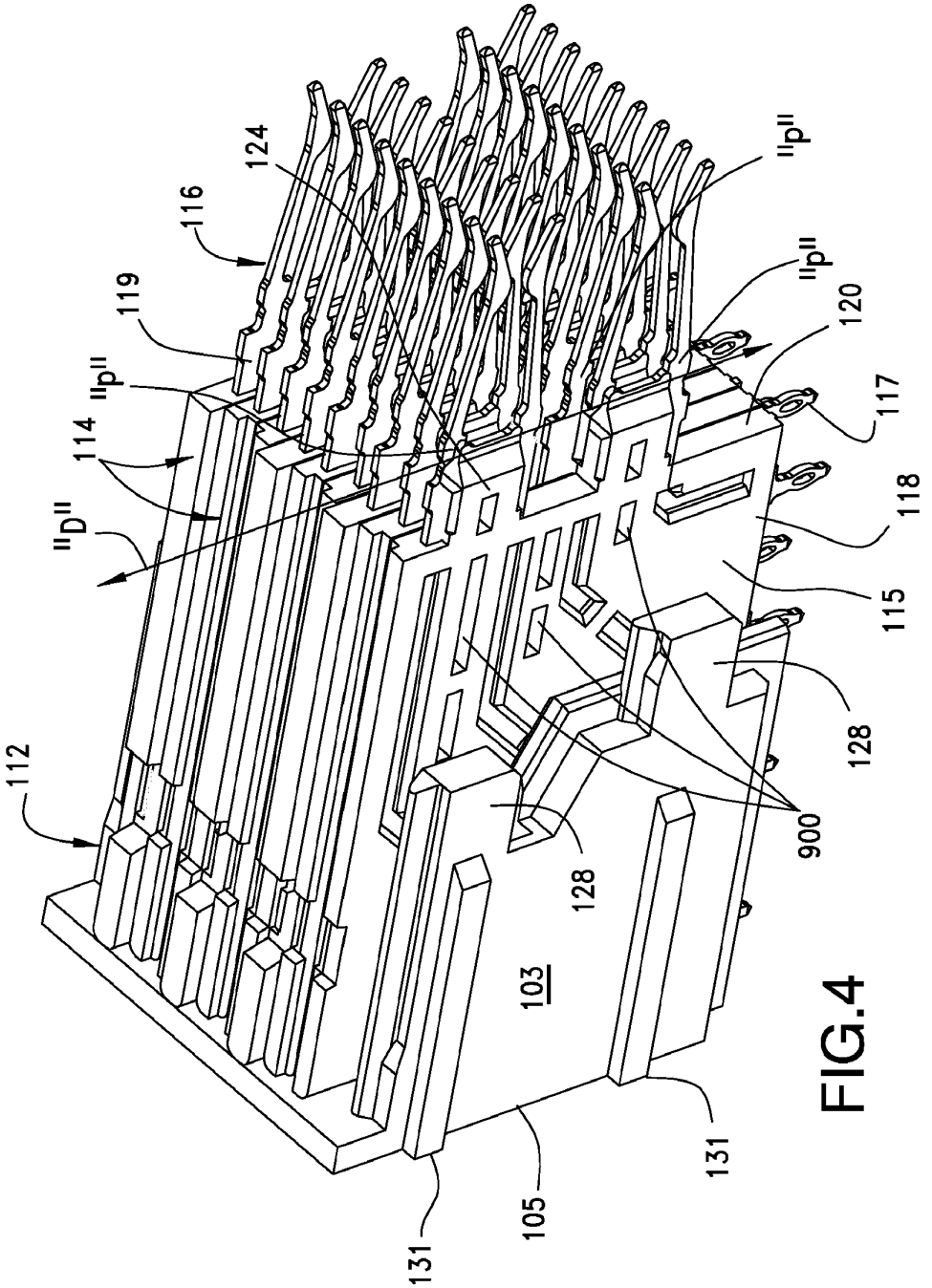
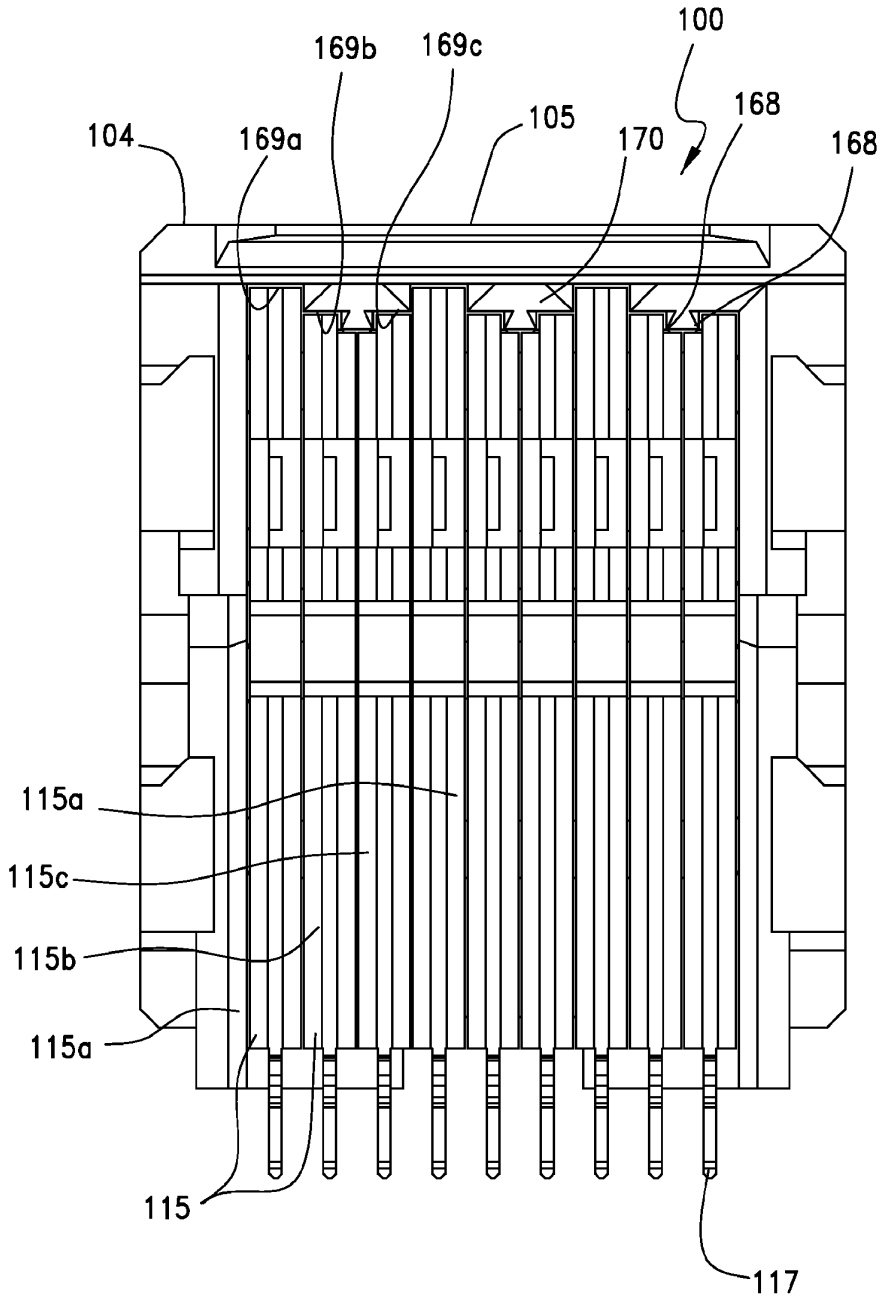

124
116
119
"p"
114
"D"
112
"p"
"p"
120
117
118
115
128
900
128
103
131
105
131

FIG.4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115b
115a
115
117

FIG.5

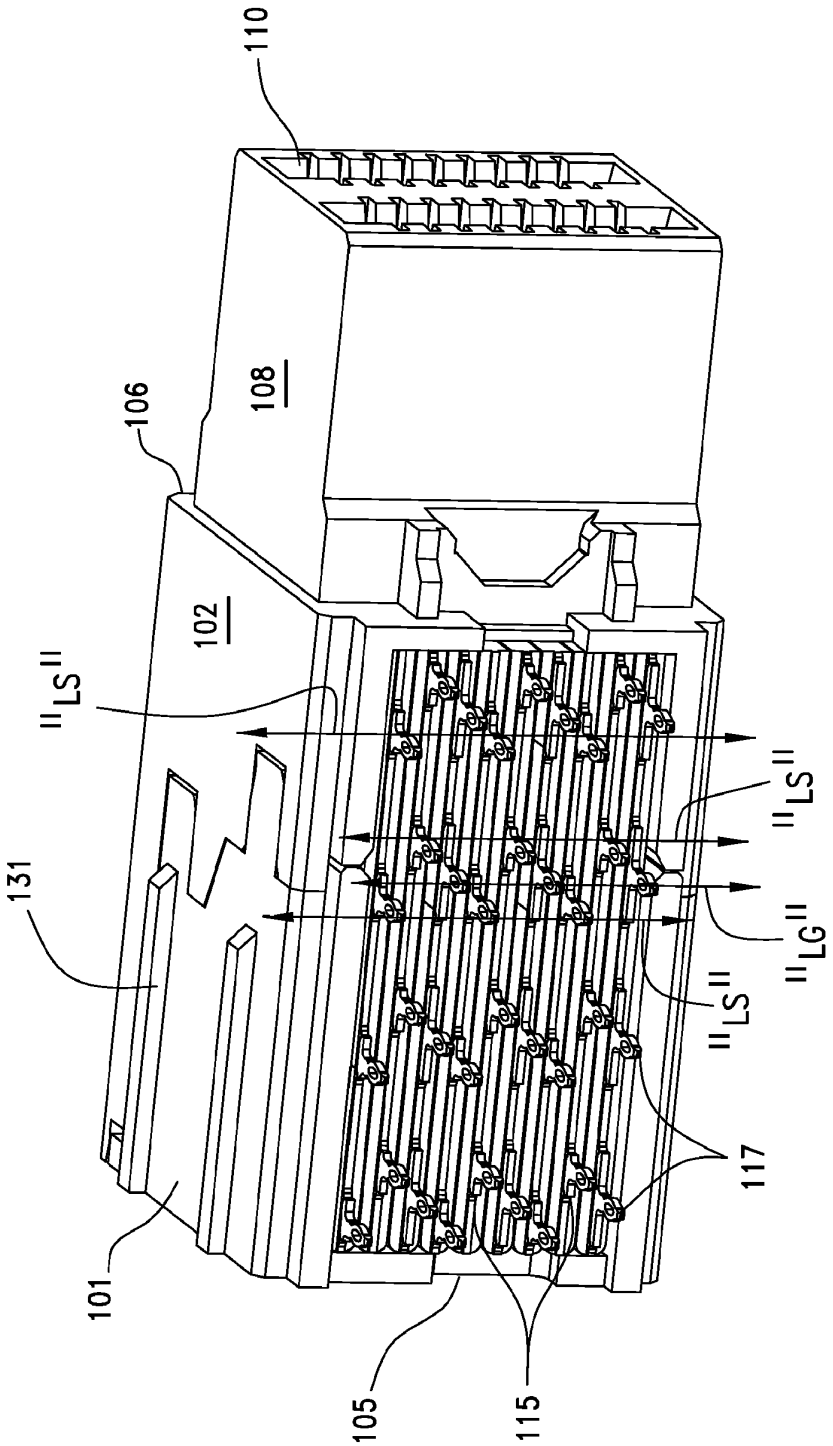


FIG.6

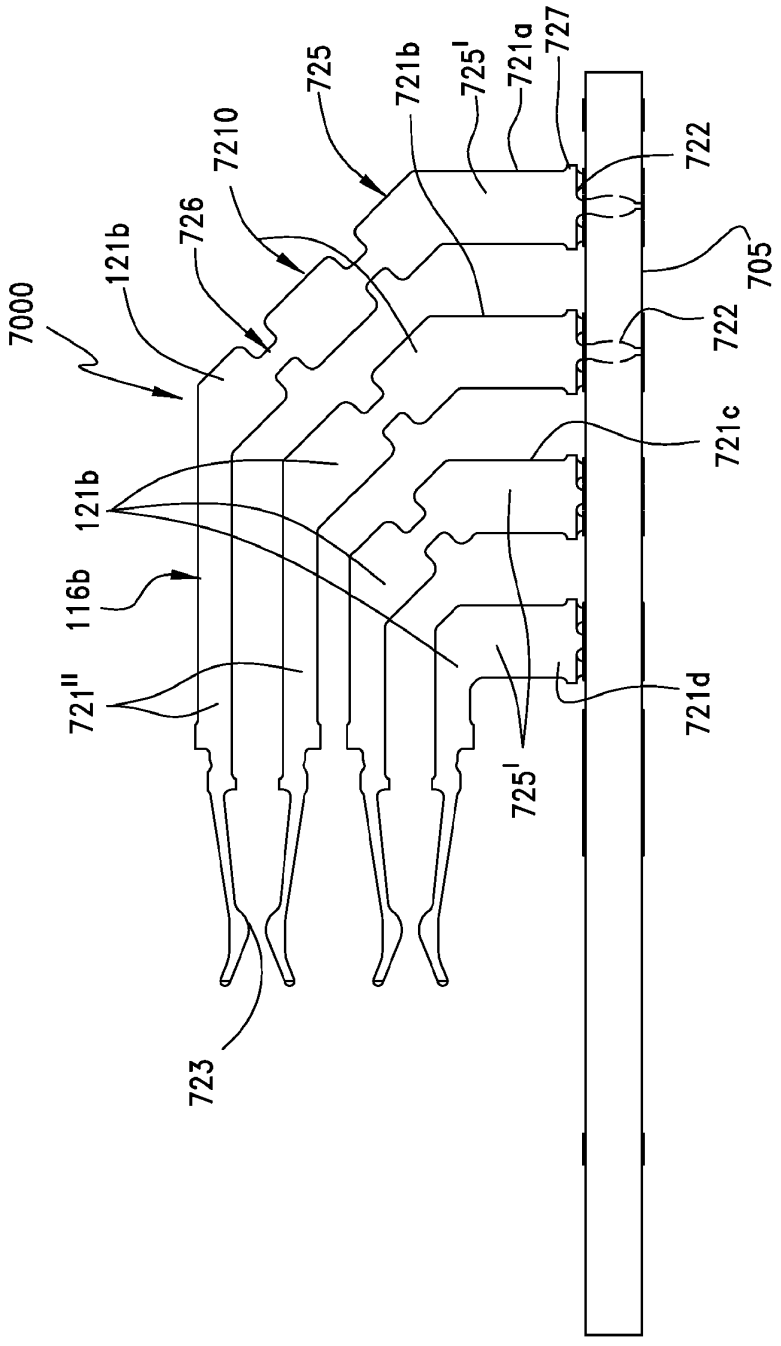

7000
121b
726
7210
725
721b
725'
721a
727
722
705
722
721c
121b
116b
721''
721d
725'
723

FIG.7

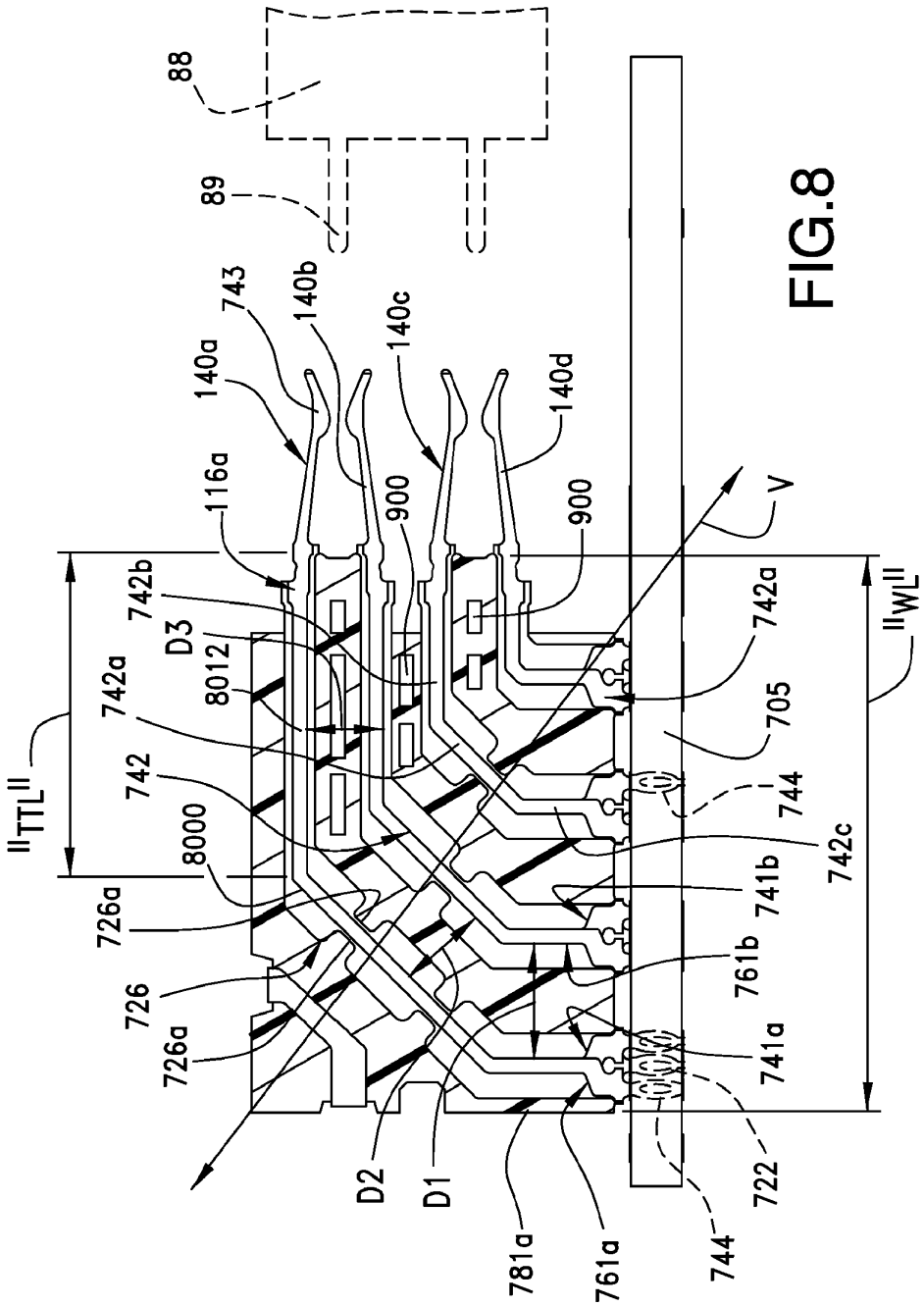

88
89
743
140b
140c
140a
140d
116a
900
900
V
742b
D3
8012
742a
742a
705
742
744
8000
742c
726a
741b
726
761b
726a
741a
D2
D1
722
781a
761a
744
l_{TTL}
l_{WL}

FIG.8

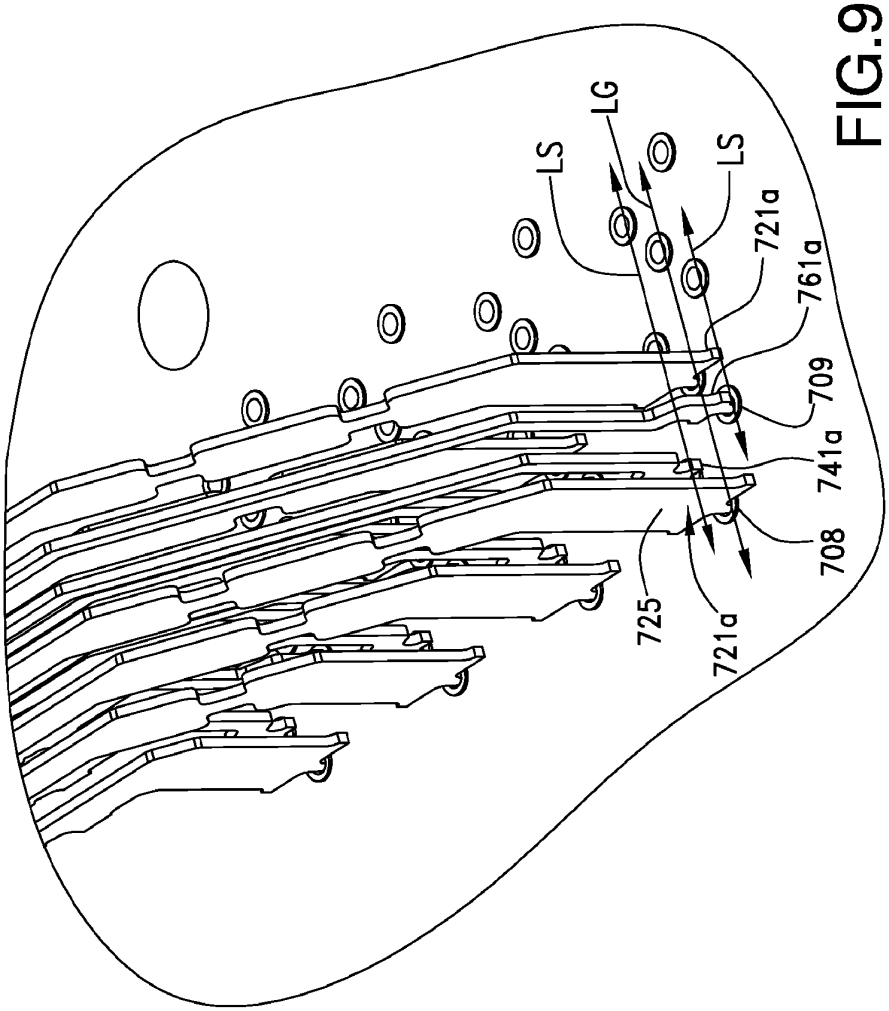
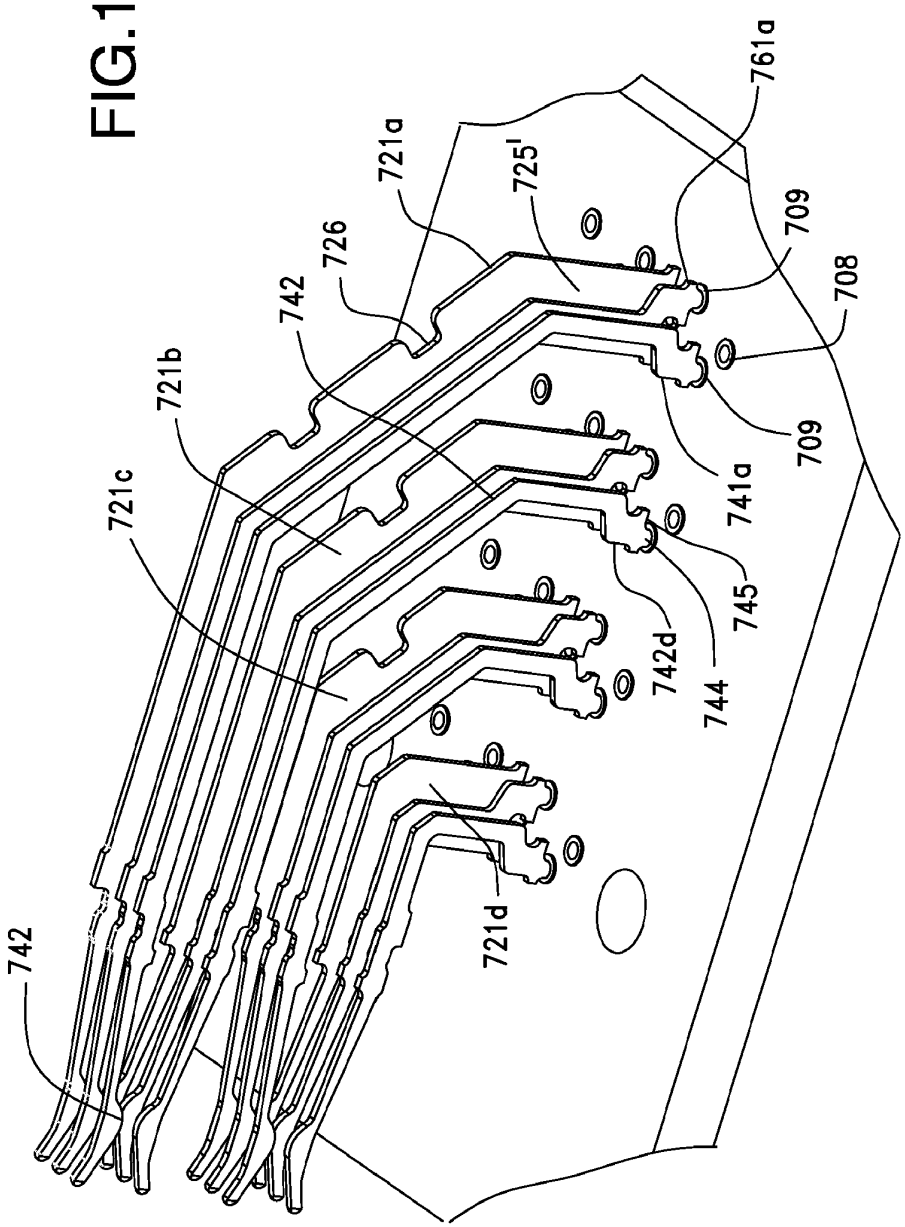


FIG.9

FIG.10


761a
721a
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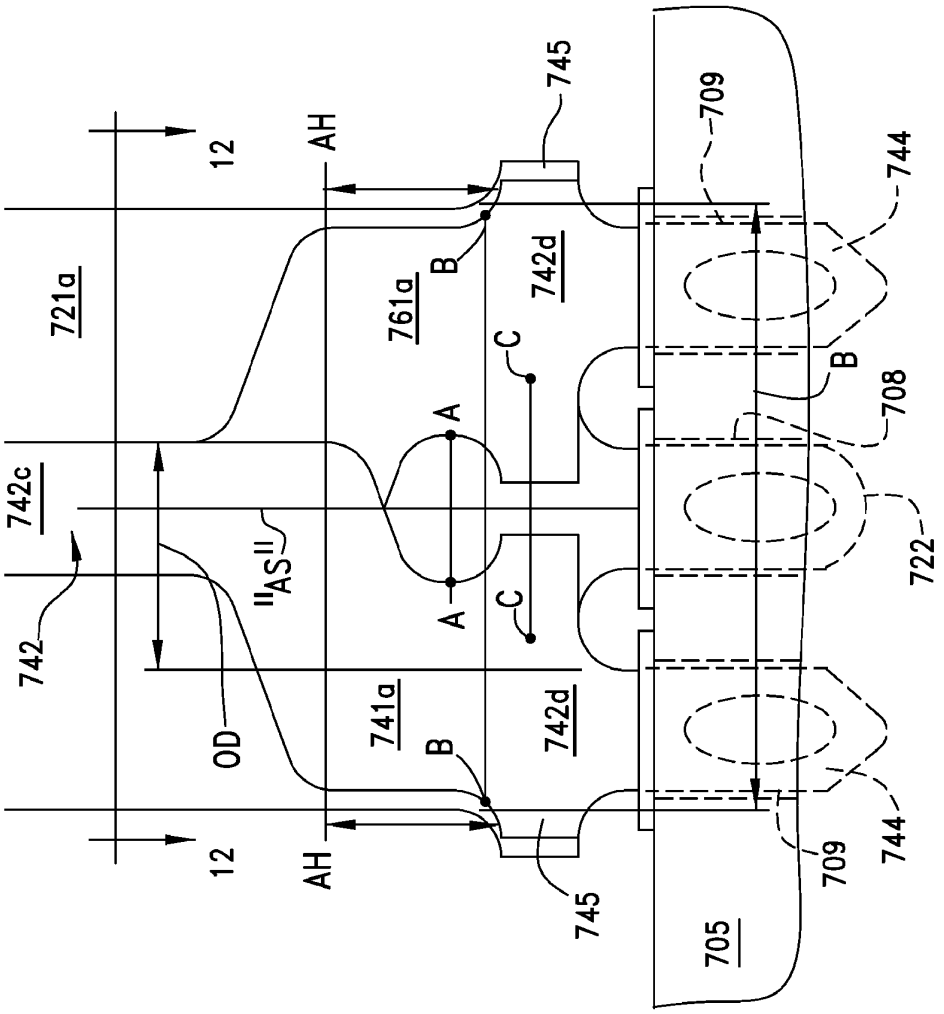
742
721d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742c
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OD
741a
722
705

FIG.11

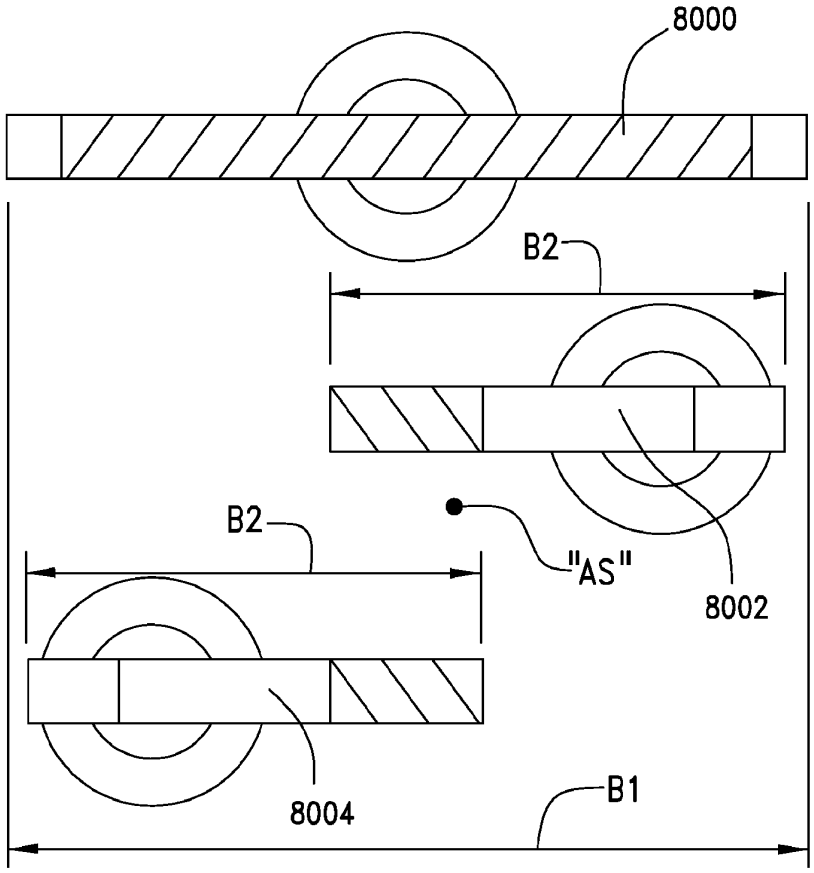
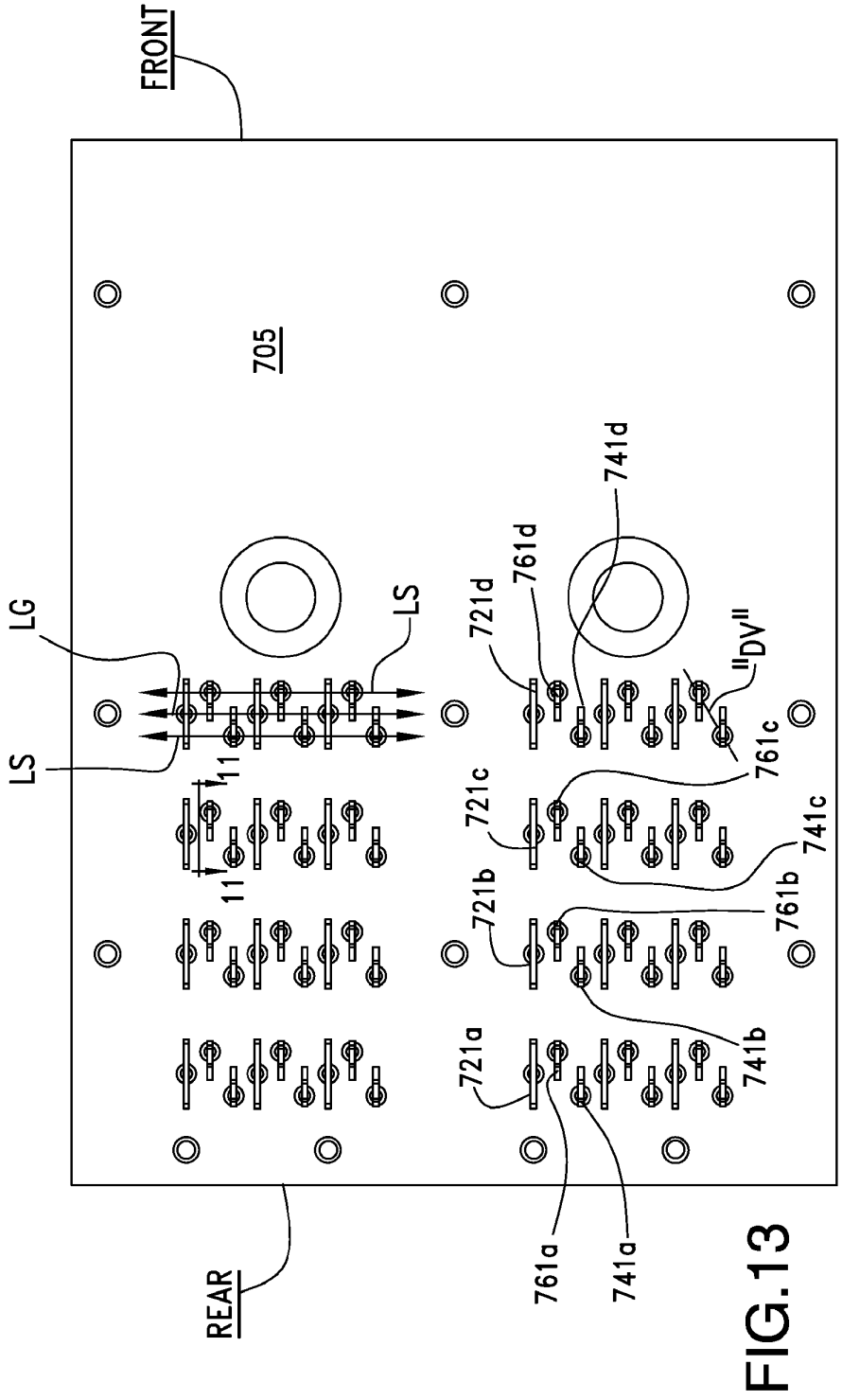


FIG.12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741d
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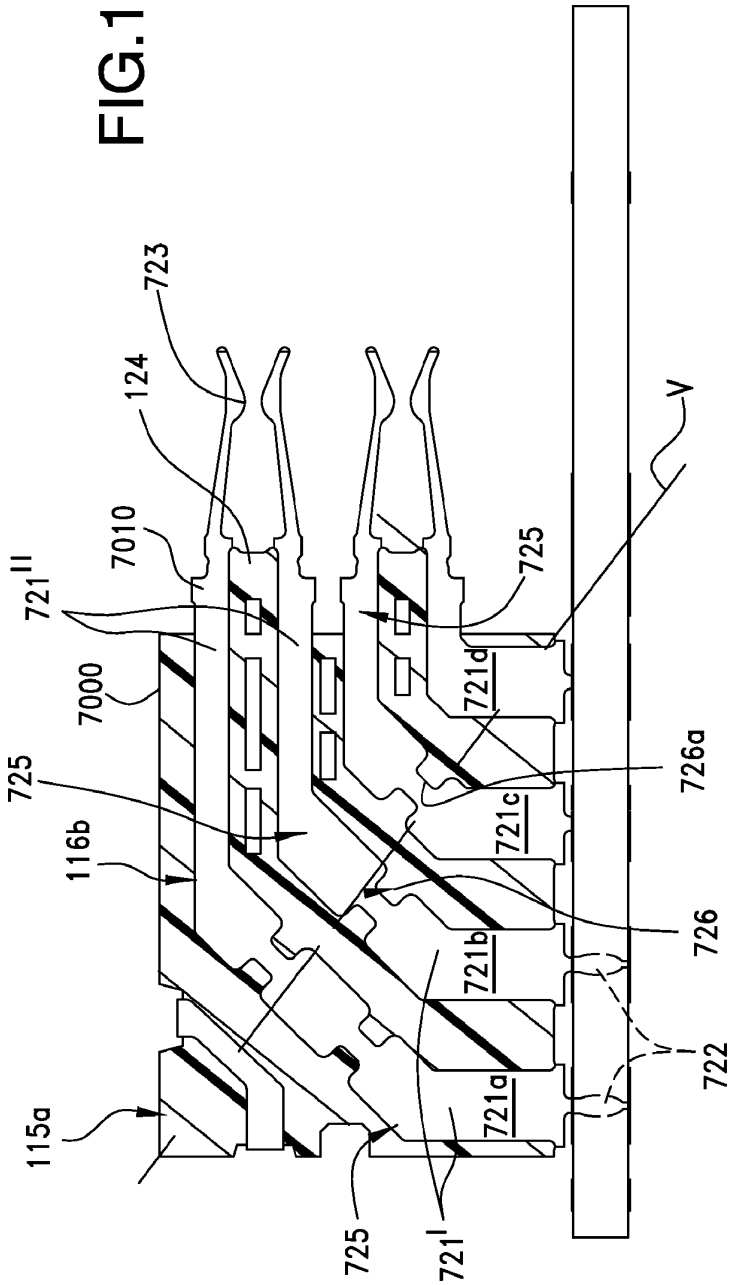
REAR

FIG.13

FIG.14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721I

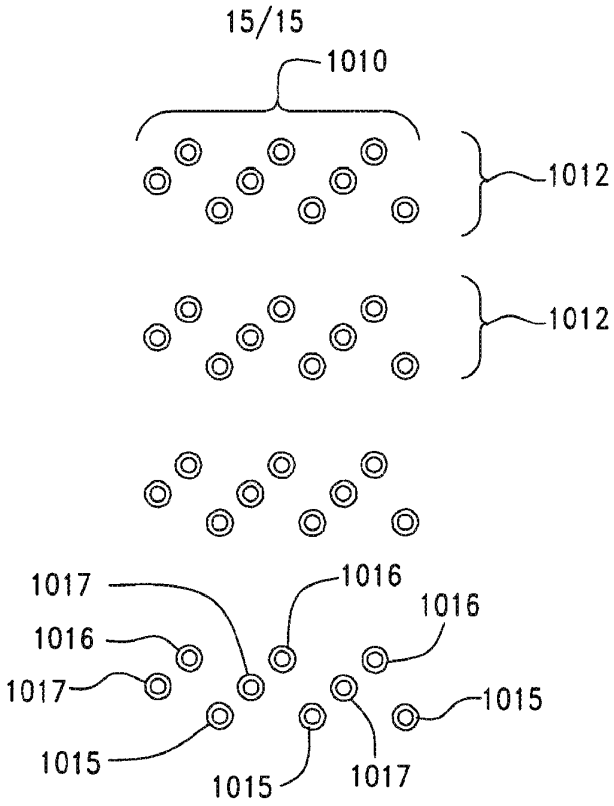

FIG.15A

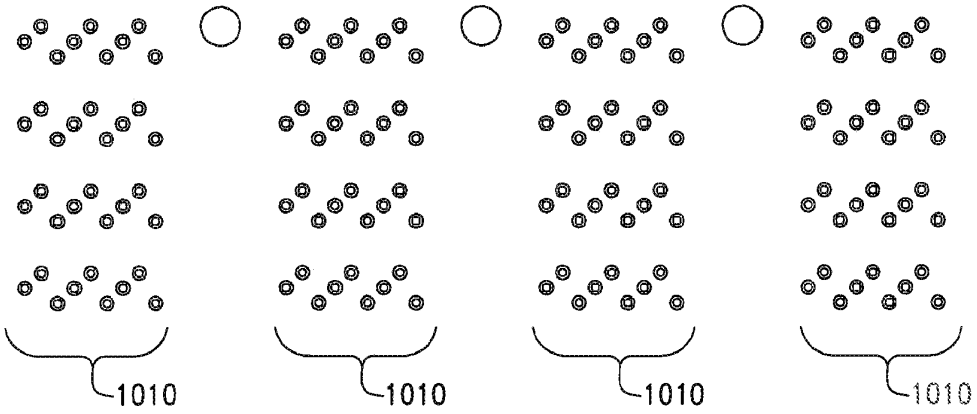

FIG.15B

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2009/056303

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01R12/28

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01R

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2006/068641 A1 (HULL GREGORY A [US] ET AL) 30 March 2006 (2006-03-30) paragraphs [0034] - [0040]; figures 6-11 paragraphs [0044] - [0046]	1-22
A	US 6 293 827 B1 (STOKOE PHILIP T [US]) 25 September 2001 (2001-09-25) column 4, lines 12-67; figures 2-7 columns 5-8	1-22
A	US 7 278 886 B2 (COHEN THOMAS S [US] ET AL COHEN THOMAS S [US] ET AL) 9 October 2007 (2007-10-09) figures 6-11a columns 4-8	1-22

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
8 January 2010	19/01/2010

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Durand, François

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2009/056303

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2006068641 A1	30-03-2006	US 2009191756 A1	30-07-2009
US 6293827 B1	25-09-2001	AU 3660701 A	14-08-2001
		CN 1401147 A	05-03-2003
		EP 1256148 A1	13-11-2002
		JP 2003522387 T	22-07-2003
		WO 0157964 A1	09-08-2001
US 7278886 B2	09-10-2007	US 2006024983 A1	02-02-2006
		US 2006276081 A1	07-12-2006

Form PCT/ISA/210 (patent family annex) (April 2005)

Electronic Patent Application Fee Transmittal

Application Number:	15065683
Filing Date:	09-Mar-2016
Title of Invention:	HIGH PERFORMANCE CABLE CONNECTOR
First Named Inventor/Applicant Name:	Donald W. Milbrand
Filer:	Edmund J. Walsh/Kyle Spencer
Attorney Docket Number:	A0863.70051US04

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
SUBMISSION- INFORMATION DISCLOSURE STMT	1806	1	240	240
		Total in USD ($)		**240**

Electronic Acknowledgement Receipt

EFS ID:	34470384
Application Number:	15065683
International Application Number:	
Confirmation Number:	5112
Title of Invention:	HIGH PERFORMANCE CABLE CONNECTOR
First Named Inventor/Applicant Name:	Donald W. Milbrand
Customer Number:	23628
Filer:	Edmund J. Walsh/Kyle Spencer
Filer Authorized By:	Edmund J. Walsh
Attorney Docket Number:	A0863.70051US04
Receipt Date:	03-DEC-2018
Filing Date:	09-MAR-2016
Time Stamp:	17:49:06
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$240
RAM confirmation Number	120418INTEFSW17495900
Deposit Account	232825
Authorized User	Wolf Greenfield
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.17 (Patent application and reexamination processing fees)	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	A086370051US04-TRN-EJW.pdf	26112 266693dec0a6dc61254615423e6392bf55c804a3	no	1
Warnings:					
Information:					
2	Fee Worksheet (SB06)	A086370051US04-FEE-EJW.pdf	32591 197a8059d224dec37fccb5ad93ea80f72fdef62e	no	1
Warnings:					
Information:					
3	Transmittal Letter	A086370051US04-IDSBODY-EJW.pdf	28598 a6c703cc1e9ffde329634bd12a90c90c97b360e8	no	3
Warnings:					
Information:					
4	Information Disclosure Statement (IDS) Form (SB08)	A086370051US04-IDSSB08-EJW.pdf	21588 e300a23a07feaaf3207f696e3a009cff6f77b2cc	no	1
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
5	Foreign Reference	WO2010030622A1.pdf	1412525 efaf7d6f99ba291bb7d825cb4bb0226ec68e45f8	no	36
Warnings:					
Information:					
6	Fee Worksheet (SB06)	fee-info.pdf	30869 21b0f5b74a2d0e77fc37460dd195e93f697a379c	no	2
Warnings:					

Information:	
Total Files Size (in bytes):	1552283

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

DOCKET NO.: A0863.70051US04

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor:	Donald W. Milbrand, Jr.
Application No.:	15/065,683
Confirmation No.:	5112
Filed:	March 9, 2016
For:	HIGH PERFORMANCE CABLE CONNECTOR
Examiner:	F. O. Figueroa
Art Unit:	2833

Certificate of Electronic Filing under 37 C.F.R. § 1.8

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being transmitted via the Office's electronic filing system in accordance with 37 C.F.R. § 1.6(a)(4).

Dated: December 3, 2018 Signature: ___/Kyle D. Spencer/___ (Kyle D. Spencer)

MAIL STOP AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

STATEMENT FILED PURSUANT TO THE DUTY OF DISCLOSURE UNDER 37 C.F.R. §§ 1.56, 1.97 AND 1.98

Sir:

Pursuant to the duty of disclosure under 37 C.F.R. §§ 1.56, 1.97 and 1.98, the undersigned requests consideration of this Information Disclosure Statement.

PART I: Compliance with 37 C.F.R. § 1.97

This Information Disclosure Statement has been filed more than three months after the filing date of this application and after the mailing date of a first Office Action, but before the mailing date of any of a Final Action under 37 C.F.R. § 1.113, a Notice of Allowance under 37 C.F.R. § 1.311, or an action that otherwise closes prosecution in this application.

Please charge our Credit Card in the amount of $240.00 covering the fee set forth in 37 C.F.R. § 1.17(p).

PART II: Information Cited

The undersigned hereby makes of record in the above-identified application the information listed on the attached form PTO-1449 (modified PTO/SB/08). The order of presentation of the references should not be construed as an indication of the importance of the references.

PART III: Remarks

Documents cited anywhere in the Information Disclosure Statement are enclosed unless otherwise indicated. It is respectfully requested that:

1. The Examiner consider completely the cited information, along with any other information, in reaching a determination concerning the patentability of the present claims;

2. The enclosed form PTO-1449 (modified PTO/SB/08) be signed by the Examiner to evidence that the cited information has been fully considered by the United States Patent and Trademark Office during the examination of this application;

3. The citations for the information be printed on any patent which issues from this application.

By submitting this Information Disclosure Statement, the undersigned makes no representation that a search has been performed, of the extent of any search performed, or that more relevant information does not exist.

By submitting this Information Disclosure Statement, the undersigned makes no representation that the information cited in the Statement is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b).

By submitting this Information Disclosure Statement, the undersigned makes no representation that the information cited in the Statement is, or is considered to be, in fact, prior art as defined by 35 U.S.C. § 102.

Notwithstanding any statements by the undersigned, the Examiner is urged to form his or her own conclusion regarding the relevance of the cited information.

An early and favorable action is hereby requested.

The Director is hereby authorized to charge any deficiency or credit any overpayment in the fees occasioned by the filing of this Information Disclosure Statement to our Deposit Account No. 23/2825 under Docket No. A0863.70051US04 from which the undersigned is authorized to draw.

Respectfully submitted,

By: /Edmund J. Walsh/_____
Edmund J. Walsh, Reg. No. 32,950
Wolf, Greenfield & Sacks, P.C.
600 Atlantic Avenue
Boston, Massachusetts 02210-2206
Telephone: (617) 646-8000

Docket No.: A0863.70051US04
Date: December 2, 2018

Doc Code: TRAN.LET
Document Description: Transmittal Letter

USED IN LIEU OF PTO/SB/21 (07-09)

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission	

Application Number	15/065,683-Conf. #5112
Filing Date	March 9, 2016
First Named Inventor	Donald W. Milbrand, Jr.
Art Unit	2833
Examiner Name	F. O. Figueroa
Attorney Docket Number	A0863.70051US04

ENCLOSURES (*Check all that apply*)

- [x] Fee Transmittal Form
- [ ] Fee Attached
- [ ] Amendment/Reply
- [ ] After Final
- [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [x] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Reply to Missing Parts/ Incomplete Application
- [ ] Reply to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s) _____
- [ ] Landscape Table on CD
- [ ] After Allowance Communication to TC
- [ ] Appeal Communication to Board of Appeals and Interferences
- [ ] Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- [ ] Proprietary Information
- [ ] Status Letter
- [x] Other Enclosure(s) (please Identify below):

Form PTO - 1449

Copy of Cited Reference

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	WOLF, GREENFIELD & SACKS, P.C.		
Signature	/Edmund J. Walsh/		
Printed name	Edmund J. Walsh		
Date	December 2, 2018	Reg. No.	32,950

Certificate of Electronic Filing under 37 C.F.R. § 1.8

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being transmitted via the Office's electronic filing system in accordance with 37 C.F.R. § 1.6(a)(4).

Dated: December 3, 2018 Signature: ___/Kyle D. Spencer/___ (Kyle D. Spencer)

6723163.1

FEE TRANSMITTAL

Complete if known	
Application Number	15/065,683-Conf. #5112
Filing Date	March 9, 2016
First Named Inventor	Donald W. Milbrand, Jr.
Examiner Name	F. O. Figueroa
Art Unit	2833
Practitioner Docket No.	A0863.70051US04

☐ Applicant asserts small entity status. See 37 CFR 1.27.

☐ Applicant certifies micro entity status. See 37 CFR 1.29. Form PTO/SB/15A or B or equivalent must either be enclosed or have been submitted previously.

TOTAL AMOUNT OF PAYMENT ($)240.00

METHOD OF PAYMENT (check all that apply)

☐ Check ☒ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☒ Deposit Account Deposit Account Number: 23/2825 Deposit Account Name: Wolf, Greenfield & Sacks, P.C.

For the above-identified deposit account, the Director is hereby authorized to (check all that apply):

☐ Charge fee(s) indicated below

☐ Charge fee(s) indicated below, **except for the filing fee**

☒ Charge any additional fee(s) or underpayment of fee(s) under 37 CFR 1.16 and 1.17, **except for any excess claims fees or multiple dependent claim fee**

☐ Charge any additional fee(s) or underpayment of fee(s) under 37 CFR 1.16 and 1.17

☒ Credit any overpayment of fee(s)

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES (U = undiscounted fee; S = small entity fee; M = micro entity fee)

	FILING FEES			SEARCH FEES			EXAMINATION FEES			
Application Type	**U ($)**	**S ($)**	**M ($)**	**U ($)**	**S ($)**	**M ($)**	**U ($)**	**S ($)**	**M ($)**	**Fees Paid ($)**
Utility	300	150*	75	660	330	165	760	380	190	
Design	200	100	50	160	80	40	600	300	150	
Plant	200	100	50	420	210	105	620	310	155	
Reissue	300	150	75	660	330	165	2,200	1,100	550	
Provisional	280	140	70	0	0	0	0	0	0	

* The $150 small entity status filing fee for a utility application is further reduced to $75 for a small entity status applicant who files the application via EFS-Web.

2. EXCESS CLAIM FEES

Fee Description	**Undiscounted Fee ($)**	**Small Entity Fee ($)**	**Micro Entity Fee ($)**
Each claim over 20 (including Reissues)	100	50	25
Each independent claim over 3 (including Reissues)	460	230	115
Multiple dependent claims	820	410	205

Total Claims _____ - 29 or HP = _____ **Extra Claims** x **Fee ($)** _____ = **Fee Paid ($)** _____

HP = highest number of total claims paid for, if greater than 20.

Multiple Dependent Claims **Fee ($)** _____ **Fee Paid ($)** _____

Indep. Claims _____ - 4 or HP = _____ **Extra Claims** x **Fee ($)** _____ = **Fee Paid ($)** _____

HP = highest number of independent claims paid for, if greater than 3.

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $400 ($200 for small entity) ($100 for micro entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets _____ - 100 = _____ **Extra Sheets** /50 = _____ **Number of each additional 50 or fraction thereof** (round **up** to a whole number) x **Fee ($)** _____ = **Fee Paid ($)** _____

4. OTHER FEE(S) **Fees Paid ($)**

Non-English specification, $130 fee (no small or micro entity discount) _____

Non-electronic filing fee under 37 CFR 1.16(t) for a utility application, $400 fee ($200 small or micro entity) _____

Other (e.g., late filing surcharge): 1806 Submission of an Information Disclosure Statement 240.00

SUBMITTED BY

Signature	/Edmund J. Walsh/	Registration No. (Attorney/Agent)	32,950	Telephone	617.646.8000
Name (Print/Type)	Edmund J. Walsh			Date	December 2, 2018

Certificate of Electronic Filing under 37 C.F.R. § 1.8

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being transmitted via the Office's electronic filing system in accordance with 37 C.F.R. § 1.6(a)(4).

Dated: December 3, 2018 Signature: ___/Kyle D. Spencer/___ (Kyle D. Spencer)

6723160.1

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/065,683	03/09/2016	Donald W. Milbrand JR.	A0863.70051US04	5112

23628 7590 12/04/2018

WOLF GREENFIELD & SACKS, P.C.
600 ATLANTIC AVENUE
BOSTON, MA 02210-2206

EXAMINER	
FIGUEROA, FELIX O	

ART UNIT	PAPER NUMBER
2833	

NOTIFICATION DATE	DELIVERY MODE
12/04/2018	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

Patents_eOfficeAction@WolfGreenfield.com
WGS_eOfficeAction@WolfGreenfield.com

Office Action Summary	**Application No.** 15/065,683	**Applicant(s)** Milbrand et al.	
	Examiner FELIX O FIGUEROA	**Art Unit** 2833	**AIA Status** No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 21 August 2018.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☑ This action is **FINAL.** 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1-7 and 9-30 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1-7 and 9-30 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

DETAILED ACTION

Notice of Pre-AIA or AIA Status

The present application is being examined under the pre-AIA first to invent provisions.

Claim Objections

Claim 24 is objected to because of the following informalities: In claim 24 line 15, "a first direction" should be --the first direction--, as per line 6. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 6-8, 10, and 23-30 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Trammel (US 6,296,496) in view of Niwa et al. (US 5,474,472).

Trammel discloses a receptacle adapted for mounting to a printed circuit board, comprising: a housing (11) having a cavity (17) bounded by a first surface (top) that is parallel to the printed circuit board and an opposing second surface (bottom) that is parallel to the printed_circuit board; a first lead assembly including a first monolithic housing member (401) comprising exterior projections extending in a direction parallel to the first surface (on top of where 40 points in Fig. 2, aligned with 41); and a first

plurality of conductive elements (20) each comprising a contact tail (25) adapted for attachment to the printed circuit board, a mating contact portion (23) disposed along the first surface of the cavity, and an intermediate portion (21) disposed in the first monolithic housing member and coupling the contact tail to the mating contact portion; and a second lead assembly including; a second monolithic housing member (402) comprising exterior projections extending in a direction parallel to the first surface (on top of where 402 points in Fig. 2); and a second plurality of conductive elements (20) each comprising a contact tail (25) adapted for attachment to the printed circuit board, a mating contact portion (23) disposed along the second surface of the cavity, and an intermediate portion (21) disposed in the second monolithic housing member coupling the contact tail to the mating contact portion.

Niwa teaches a housing (24) having a cavity bounded by first and second surfaces (top and bottom) that are disposed above a first side of the printed circuit board; a plurality of conductive elements (16a, 16b) comprising a tail that is perpendicular to the first side of the PCB; and a second plurality of conductive elements (16c, 16d) comprising a tail that is perpendicular to the first side of the PCB. It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the first and second surfaces disposed above the PCB, as taught by Niwa, in order to accommodate environmental parameters.

Regarding claim 6, Trammel discloses the contact tails and the mating contact portions disposed at right angles.

Regarding claim 7, Trammel discloses the first plurality of conductive elements and the second plurality of conductive elements forming rows of contacts on the first and second surfaces, respectively, of the cavity.

Regarding claim 8, Trammel discloses the first and second surfaces of the cavity include slots configured to receive the conductive elements of the first plurality of conductive elements and the second plurality of conductive elements, respectively.

Regarding claim 10, Trammel discloses the first plurality of conductive elements is molded in the first housing member, and the second plurality of conductive elements is molded in the second housing member.

Regarding claim 23, Trammel discloses an insert (30) disposed between the first and second lead assemblies.

Regarding claim 24, Trammel discloses a receptacle adapted for mounting to a printed circuit board, comprising: a housing (11) having a cavity (17) bounded by a first surface (top) that is parallel to the printed circuit board and a second surface (bottom) that faces the first surface and is parallel to the printed circuit board; a first lead assembly including (401): a first plurality of conductive elements (20) each comprising a mating contact portion (23) disposed along the first surface of the cavity, a contact tail (25) adapted for attachment to the printed circuit board and disposed at a right angle (at least a part) relative to the mating contact portion, and an intermediate portion (21) coupling the contact tail to the mating contact portion; and a first monolithic housing member (401) molded over the intermediate portions of each conductive element of the first plurality of conductive elements; and a second lead assembly (402), separate and

distinct from the first lead assembly, including: a second plurality of conductive elements (20) each comprising a mating contact portion (23) disposed along the second surface of the housing cavity, a contact tail (25) adapted for attachment to the printed circuit board and disposed at a right angle relative to the mating contact portion, and an intermediate portion (21) coupling the contact tail to the mating contact portion; and a second monolithic housing member (402) molded over the intermediate portions of each conductive element of the second plurality of conductive elements.

Niwa teaches a plurality of conductive elements (16c, 16d) disposed along a first direction (vertical, at 16c', 16d'), each comprising a mating contact portion extending along the first surface in a second direction (horizontal) perpendicular to the first direction, and a tail that is perpendicular to the first side of the PCB, with an intermediate portion comprising a right angle bend; and a second plurality of conductive elements (16a, 16b) disposed along *a first direction*, that are longer than the first plurality of conductive elements and each comprising a tail that is perpendicular to the first side of the PCB, each comprising a mating contact portion extending along the second surface in the second direction (horizontally), with an intermediate portion comprising a right angle bend; wherein the contact tails of the first plurality of conductive elements are aligned along the first direction, and the contact tails of the second plurality of conductive elements are aligned along the first direction. It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the conductive elements, as taught by Niwa, in order to accommodate environmental parameters.

Regarding claim 25, Trammel discloses a receptacle adapted for mounting to a printed circuit board, comprising: a monolithic housing (11) and having a cavity (17) bounded by a first surface (top) that is parallel to the printed circuit board and a second surface (bottom) that faces the first surface and is parallel to the printed circuit board; a first lead assembly (401) including: a first plurality of conductive elements (20) including at least six conductive elements, each of the first plurality of conductive elements comprising a mating contact portion extending along the first surface of the cavity in a second direction (horizontal), a contact tail adapted for attachment to the printed circuit board and disposed at a right angle relative to the mating contact portion, and an intermediate portion coupling the contact tail to the mating contact portion; and a first monolithic housing member (401) made of an insulative material and molded over the intermediate portions of each conductive element of the first plurality of conductive elements, and comprising exterior projections (were 40 points in Fig. 2) extending in the first direction (vertically); and a second lead assembly (402), separate and distinct from the first lead assembly, including: a second plurality of conductive elements including at least six conductive elements, each of the second plurality of conductive elements comprising a mating contact portion disposed along the second surface of the housing cavity, a contact tail adapted for attachment to the printed circuit board and disposed at a right angle relative to the mating contact portion, and an intermediate portion coupling the contact tail to the mating contact portion; and a second monolithic housing member (402) made of an insulative material and molded over the intermediate portions of each conductive element of the second plurality of conductive elements; and comprising

exterior projections (under where 402 point in Fig. 2) extending along the first direction (vertically).

Niwa teaches a plurality of conductive elements (16c, 16d) disposed along a first direction (at 16c', 16d' vertical in Fig. 2), each comprising a tail (16c', 16d') that is perpendicular to the first side of the PCB, with an intermediate portion comprising a right angle bend; and a second plurality of conductive elements (16a, 16b), disposed along the first direction (at 16a', 16b' vertically in Fig. 2), that are longer than the first plurality of conductive elements and each comprising a tail that is perpendicular to the first side of the PCB, with an intermediate portion comprising a right angle bend. It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the conductive elements, as taught by Niwa, in order to accommodate environmental parameters.

Regarding claim 26, Trammel discloses the contact tails of the first and second plurality of conductive elements configured for attachment to conductive pads on a surface of the printed circuit board.

Regarding claim 27, Trammel discloses a receptacle adapted for mounting to a printed circuit board, comprising: a housing (11) made of an insulative material and having: a first cavity (17) shaped to receive a first plug in an insertion direction (horizontal in Fig. 2), wherein the first cavity is bounded by a first surface (top) that is parallel to the printed circuit board and a second surface (bottom) that faces the first surface and is parallel to the printed circuit board; a first lead assembly (401) comprising: a first plurality of conductive elements (20) disposed in a row extending in a

first direction (direction of cross sectional arrow 2-2 in Fig. 1), each of the first plurality of conductive elements comprising a mating contact portion extending along the first surface of the cavity in a second direction (horizontal in Fig. 2) parallel to the insertion direction, a contact tail (25) extending from the monolithic housing, and an intermediate portion (21) coupling the contact tail to the mating contact portion; and a first housing member (40, 401) made of an insulative material, molded over the intermediate portions of each conductive element of the first plurality of conductive elements; and a second lead assembly (402), separate and distinct from the first lead assembly, comprising: a second plurality of conductive elements disposed in a row extending in the first direction, each of the second plurality of conductive elements comprising a mating contact portion extending along the second surface of the first cavity in the second direction, a contact tail (25) extending from the monolithic housing, and an intermediate portion coupling the contact tail to the mating contact portion; and a second housing member (402) made of an insulative material, molded over the intermediate portions of each conductive element of the second plurality of conductive elements;

Trammel discloses substantially the claimed invention except for the right angle bend on the conductive elements and the second cavity with third and fourth lead assemblies. Niwa teaches conductive elements having a right angle bend; and a second cavity offset from the first cavity in a direction perpendicular to the insertion direction, wherein the second cavity is shaped to receive a second plug in the insertion direction, and the second cavity and is bounded by a third surface that is parallel to the printed circuit board and a fourth surface that faces the third surface and is parallel to the printed circuit board; a third lead assembly comprising: a third plurality of conductive

elements disposed in a row extending in the first direction, each of the third plurality of conductive elements comprising a mating contact portion extending along the third surface of the second cavity in the second direction, a contact tail extending from the monolithic housing, and an intermediate portion coupling the contact tail to the mating contact portion and comprising a right angle bend; and a fourth lead assembly, comprising: a fourth plurality of conductive elements disposed in a row extending in the first direction, each of the fourth plurality of conductive elements comprising a mating contact portion extending along the fourth surface of the second cavity in the second direction, a contact tail extending from the monolithic housing, and an intermediate portion coupling the contact tail to the mating contact portion and comprising a right angle bend; wherein the first, second, third and fourth housing members engage with the housing to hold the intermediate portions of the first, second, third and fourth plurality of conductive elements relative to the circuit board. It would have been obvious to one having ordinary skill in the art at the time the invention was effectively filed to form the terminals with a right angle bend and to include a second cavity with third and fourth lead assemblies, as taught by Niwa, in order to accommodate environmental parameters, and to provide extra connection interfaces.

Regarding claim 28, Trammel, as modified by Niwa, discloses the contact tails of the first, second, third and fourth plurality of conductive elements configured for attachment to conductive pads on a surface of the printed circuit board.

Regarding claim 29, Trammel, as modified by Niwa, discloses the first housing member engaging with the second housing member and the third housing member engaging with the fourth housing member.

Regarding claim 30, Trammel, as modified by Niwa, discloses each of the first, second, third and fourth lead assemblies being L-shaped; and the first, second, third and fourth housing members engage with the housing so as to hold the first, second, third and fourth lead assemblies within the housing with the L-shaped first, second, third and fourth housing members nested.

Claims 2-5 and 15-22 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Trammel and Niwa, and further in view of Cohen et al. (US 7,753,731).

Regarding claim 2, Cohen teaches (in Fig. 4) the use of an insert (160) disposed between the first and second lead assemblies; the insert including an electrically lossy material. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use an insert, as taught by Cohen, in order to provide the desired shielding and reduce crosstalk between the lead assemblies/rows.

Regarding claim 3, Cohen teaches the insert contacting selected ones of the conductive elements.

Regarding claim 4, Cohen teaches the insert including projections towards selected ones of the conductive elements.

Regarding claim 5, Cohen teaches at least one of the first and second housing members including one or more slots for receiving the projections of the insert.

Regarding claim 15, Trammel, as modified by Cohen, discloses that for each conductive element of a first subset of the first plurality of conductive elements, a portion of the conductive element is exposed through the first housing member, and for

each conductive element of a second subset of the second plurality of conductive elements, a portion of the conductive element is exposed through the second housing member.

Regarding claim 16, Cohen discloses a first surface of the insert comprising a first plurality of projections, each projection of the first plurality of projections being coupled to a conductive element of the first subset; and a second surface of the insert comprises a second plurality of projections, each projection of the second plurality of projections being coupled to a conductive element of the second subset.

Regarding claim 17, Cohen discloses the first plurality of conductive elements comprising conductive elements disposed in a plurality of pairs of conductive elements; and the first subset of the first plurality of conductive elements comprises conductive elements each of which is disposed adjacent a pair of the plurality of pairs.

Regarding claim 18, Cohen teaches the insert including a conductive material.

Regarding claim 19, Cohen teaches the insert being at least partially conductive.

Regarding claim 20, Cohen teaches the insert including an electrically lossy material; and the electrically lossy material is electrically coupled to selected ones of the first plurality of conductive elements and the second plurality of conductive elements.

Regarding claim 21, Trammel, as modified by Cohen, discloses the first plurality of conductive elements positioned in a first row, the first row comprising pairs of the first plurality of conductive elements separated by single conductive elements of the first plurality of conductive elements; the second plurality of conductive elements positioned in a second row, the second row comprising pairs of the second plurality of conductive elements separated by single conductive elements of the second plurality of conductive

elements; and the electrically lossy material is selectively electrically coupled to the single conductive elements of the first plurality of conductive elements and second plurality of conductive elements.

Regarding claim 22, Cohen discloses the insert includes projections towards the selected ones of the conductive elements.

Claims 11-14 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Trammel and Niwa, and further in view of Fogg et al. (US 6,582,244).

Regarding claim 11, Trammel discloses the first housing member and the second housing member made of an insulative material. Fogg teaches a housing (150) made of insulating material.

Regarding claim 12, Fogg discloses the housing includes at least one projection from a lower surface thereof.

Regarding claim 13, Fogg discloses a shell (10) adapted for attachment of the housing to the printed circuit board.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the housing of insulating material with a lower projection and a shell, as taught by Fogg, in order to reduce weight and cost of the connector.

Regarding claim 14, Fogg discloses the housing further comprises a second cavity (204) bounded by a third surface (210) and an opposing fourth surface (212), further comprising a third lead assembly including a third plurality of conductive elements (306) disposed in a third housing member and a fourth lead assembly including a fourth plurality of conductive elements (308) disposed in a fourth housing

member, each conductive element of the third and fourth pluralities of conductive elements comprising a contact tail adapted for attachment to the printed circuit board, a mating contact portion and an intermediate portion coupling the contact tail to the mating contact portion, wherein the mating contact portions of the third plurality of conductive elements are disposed along the third surface of the second cavity and the mating contact portions of the fourth plurality of conductive elements are disposed along the fourth surface of the second cavity. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form additional subassemblies, as taught by Fogg, in order to provide the desire interface to transmit the desired signals.

Response to Arguments

Applicant's arguments with respect to the claims have been considered but are moot in view of the new grounds of rejection, as applied.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to FELIX O FIGUEROA whose telephone number is (571)272-2003. The examiner can normally be reached on M-F 9am-6pm.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/FELIX O FIGUEROA/
Primary Examiner, Art Unit 2833

Request for Continued Examination (RCE) Transmittal		
Address to: Mail Stop RCE Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450	Application Number	15/065,683-Conf. #5112
	Filing Date	March 9, 2016
	First Named Inventor	Donald W. Milbrand, Jr.
	Art Unit	2833
	Examiner Name	F. O. Figueroa
	Attorney Docket Number	A0863.70051US04

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.

Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, to any international application that does not comply with the requirements of 35 U.S.C 371, or to any design application. See Instruction Sheet for RCEs (not to be submitted to the USPTO on page 2.)

1. Submission required under 37 CFR 1.114 Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).
   - a. [ ] Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.
     - i. [ ] Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
     - ii. [ ] Other _____
   - b. [x] Enclosed
     - i. [x] Amendment/Reply
     - ii. [ ] Affidavit(s)/ Declaration(s)
     - iii. [x] Information Disclosure Statement (IDS)
     - iv. [x] Other Petition for Extension of Time; Fee Transmittal; FORM PTO-1449; Cited References
2. Miscellaneous
   - a. [ ] Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of _____ months. (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)
   - b. [ ] Other _____
3. Fees The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.
   - a. [ ] The Director is hereby authorized to charge the following fees, any underpayment of fees, or credit any overpayments, to Deposit Account No. 23/2825 .
     - i. [x] RCE fee required under 37 CFR 1.17(e)
     - ii. [x] Extension of time fee (37 CFR 1.136 and 1.17)
     - iii. [ ] Other _____
   - b. [ ] Check in the amount of $ _____ enclosed
   - c. [x] Payment by credit card ~~(Form PTO-2038 enclosed)~~

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED			
Signature	/Edmund J. Walsh/	Date	April 4, 2019
Name (Print/Type)	Edmund J. Walsh	Registration No.	32,950

~~***CERTIFICATE OF MAILING OR TRANSMISSION***~~			
~~I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450 or facsimile transmitted to the U.S. Patent and Trademark Office on the date shown below.~~			
~~Signature~~			
~~Name (Print/Type)~~		~~Date~~	

Certificate of Electronic Filing under 37 C.F.R. § 1.8

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being transmitted via the Office's electronic filing system in accordance with 37 C.F.R. § 1.6(a)(4).

Dated: April 4, 2019 Electronic Signature for: /Trish McDonald/

7058897.1

PTO/AIA/22 (03-13)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

PETITION FOR EXTENSION OF TIME UNDER 37 CFR 1.136(a)	Docket Number (Optional) A0863.70051US04
Application Number 15/065,683-Conf. #5112	Filed March 9, 2016
For HIGH PERFORMANCE CABLE CONNECTOR	
Art Unit 2833	Examiner F. O. Figueroa

This is a request under the provisions of 37 CFR 1.136(a) to extend the period for filing a reply in the above-identified application.

The requested extension and fee are as follows (check time period desired and enter the appropriate fee below):

	Fee	Small Entity Fee	Micro Entity Fee	
[X] One month (37 CFR 1.17(a)(1))	$200	$100	$50	$ 200.00
[ ] Two months (37 CFR 1.17(a)(2))	$600	$300	$150	$
[ ] Three months (37 CFR 1.17(a)(3))	$1,400	$700	$350	$
[ ] Four months (37 CFR 1.17(a)(4))	$2,200	$1,100	$550	$
[ ] Five months (37 CFR 1.17(a)(5))	$3,000	$1,500	$750	$

[ ] Applicant asserts small entity status. See 37 CFR 1.27.

[ ] Applicant certifies micro entity status. See 37 CFR 1.29.
Form PTO/SB/15A or B or equivalent must either be enclosed or have been submitted previously.

[ ] A check in the amount of the fee is enclosed.

[X] Payment by credit card. ~~Form PTO-2038 is attached.~~

[ ] The Director has already been authorized to charge fees in this application to a Deposit Account.

[X] The Director is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number 23/2825 .

[X] Payment made via EFS-Web.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

I am the

[ ] applicant.

[X] attorney or agent of record. Registration number 32,950 .

[ ] attorney or agent acting under 37 CFR 1.34. Registration number _____.

/Edmund J. Walsh/	April 4, 2019
Signature	Date
Edmund J. Walsh	617.646.8000
Typed or printed name	Telephone Number

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. Submit multiple forms if more than one signature is required, see below*.

[ ] * Total of 1 forms are submitted.

Certificate of Electronic Filing under 37 C.F.R. § 1.8

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being transmitted via the Office's electronic filing system in accordance with 37 C.F.R. § 1.6(a)(4).

Dated: April 4, 2019 Electronic Signature for: /Trish McDonald/

FEE TRANSMITTAL

Complete if known	
Application Number	15/065,683-Conf. #5112
Filing Date	March 9, 2016
First Named Inventor	Donald W. Milbrand, Jr.
Examiner Name	F. O. Figueroa
Art Unit	2833
Practitioner Docket No.	A0863.70051US04

☐ Applicant asserts small entity status. See 37 CFR 1.27.

☐ Applicant certifies micro entity status. See 37 CFR 1.29. Form PTO/SB/15A or B or equivalent must either be enclosed or have been submitted previously.

TOTAL AMOUNT OF PAYMENT ($)2,100.00

METHOD OF PAYMENT (check all that apply)

☐ Check ☒ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☒ Deposit Account Deposit Account Number: 23/2825 Deposit Account Name: Wolf, Greenfield & Sacks, P.C.

For the above-identified deposit account, the Director is hereby authorized to (check all that apply):

☐ Charge fee(s) indicated below

☐ Charge fee(s) indicated below, **except for the filing fee**

☒ Charge any additional fee(s) or underpayment of fee(s) under 37 CFR 1.16 and 1.17, **except for any excess claims fees or multiple dependent claim fee**

☐ Charge any additional fee(s) or underpayment of fee(s) under 37 CFR 1.16 and 1.17

☒ Credit any overpayment of fee(s)

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES (U = undiscounted fee; S = small entity fee; M = micro entity fee)

	FILING FEES			SEARCH FEES			EXAMINATION FEES			
Application Type	**U ($)**	**S ($)**	**M ($)**	**U ($)**	**S ($)**	**M ($)**	**U ($)**	**S ($)**	**M ($)**	**Fees Paid ($)**
Utility	300	150*	75	660	330	165	760	380	190	
Design	200	100	50	160	80	40	600	300	150	
Plant	200	100	50	420	210	105	620	310	155	
Reissue	300	150	75	660	330	165	2,200	1,100	550	
Provisional	280	140	70	0	0	0	0	0	0	

* The $150 small entity status filing fee for a utility application is further reduced to $75 for a small entity status applicant who files the application via EFS-Web.

2. EXCESS CLAIM FEES

Fee Description	**Undiscounted Fee ($)**	**Small Entity Fee ($)**	**Micro Entity Fee ($)**
Each claim over 20 (including Reissues)	100	50	25
Each independent claim over 3 (including Reissues)	460	230	115
Multiple dependent claims	820	410	205

Total Claims		**Extra Claims**		**Fee ($)**		**Fee Paid ($)**	**Multiple Dependent Claims**	
29	- 29 or HP =		x		=		**Fee ($)**	**Fee Paid ($)**

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims		**Extra Claims**		**Fee ($)**		**Fee Paid ($)**
4	- 4 or HP =		x		=	

HP = highest number of independent claims paid for, if greater than 3.

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $400 ($200 for small entity) ($100 for micro entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets		**Extra Sheets**		**Number of each additional 50 or fraction thereof**		**Fee ($)**		**Fee Paid ($)**
	- 100 =		/50 =		(round **up** to a whole number) x		=	

4. OTHER FEE(S)

	Fees Paid ($)
Non-English specification, $130 fee (no small or micro entity discount)	
Non-electronic filing fee under 37 CFR 1.16(t) for a utility application, $400 fee ($200 small or micro entity)	
Other (e.g., late filing surcharge): 1251 Extension for response within first month	200.00
1820 Request for continued examination (RCE) - 2nd and ...	1,900.00

SUBMITTED BY

Signature	/Edmund J. Walsh/	Registration No. (Attorney/Agent)	32,950	Telephone	617.646.8000
Name (Print/Type)	Edmund J. Walsh			Date	April 4, 2019

Certificate of Electronic Filing under 37 C.F.R. § 1.8

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being transmitted via the Office's electronic filing system in accordance with 37 C.F.R. § 1.6(a)(4).

Dated: April 4, 2019 Electronic Signature for: /Trish McDonald/

7058894.1

Docket No.: A0863.70051US04
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor:	Donald W. Milbrand, Jr.
Application No.:	15/065,683
Confirmation No.:	5112
Filed:	March 9, 2016
For:	HIGH PERFORMANCE CABLE CONNECTOR
Examiner:	F. O. Figueroa
Art Unit:	2833

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Dated: April 4, 2019 Electronic Signature for: /Trish McDonald/

AMENDMENT FILED WITH A REQUEST FOR CONTINUED EXAMINATION

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

INTRODUCTORY COMMENTS

In response to the Office Action dated December 4, 2018, finally rejecting claims 1-7 and 9-30, please amend the above-identified U.S. patent application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 12 of this paper.

AMENDMENTS TO THE CLAIMS

Applicant submits below a complete listing of the current claims, including marked-up claims with insertions indicated by underlining and deletions indicated by strikeouts and/or double bracketing. This listing of claims replaces all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently amended) A receptacle adapted for mounting to a printed circuit board, comprising:

a housing having a cavity bounded by a first surface that is parallel to the printed circuit board and an opposing second surface that is parallel to the printed circuit board, each of the first and second surfaces being disposed above a first side of the printed circuit board;

a first lead assembly including:

a first monolithic housing member ~~comprising exterior projections extending in a direction parallel to the first surface~~; and

a first plurality of conductive elements each comprising a contact tail adapted for attachment to the printed circuit board that is perpendicular to the first side of the printed circuit board, a mating contact portion disposed along the first surface of the cavity, and an intermediate portion disposed in the first monolithic housing member and coupling the contact tail to the mating contact portion,

wherein the first monolithic housing member comprises exterior projections extending away from the first plurality of conductive elements along a direction parallel to the first surface; and

a second lead assembly including:

a second monolithic housing member ~~comprising exterior projections extending in the direction parallel to the first surface~~; and

a second plurality of conductive elements each comprising a contact tail adapted for attachment to the printed circuit board that is perpendicular to the first side of the printed circuit board, a mating contact portion disposed along the second surface of the cavity, and

an intermediate portion disposed in the second monolithic housing member coupling the contact tail to the mating contact portion,

wherein the second monolithic housing member comprises exterior projections extending away from the second plurality of conductive elements along the direction parallel to the first surface.

2. (Previously presented) The receptacle as defined in claim 23, wherein the insert includes an electrically lossy material.

3. (Previously presented) The receptacle as defined in claim 23, wherein the insert contacts selected ones of the conductive elements.

4. (Previously presented) The receptacle as defined in claim 23, wherein the insert includes projections towards selected ones of the conductive elements.

5. (Previously presented) The receptacle as defined in claim 4, wherein at least one of the first and second monolithic housing members includes one or more slots for receiving the projections of the insert.

6. (Original) The receptacle as defined in claim 1, wherein the contact tails and the mating contact portions are disposed at right angles.

7. (Original) The receptacle as defined in claim 1, wherein the first plurality of conductive elements and the second plurality of conductive elements form rows of contacts on the first and second surfaces, respectively, of the cavity.

8. (Original) The receptacle as defined in claim 1, wherein the first and second surfaces of the cavity include slots configured to receive the conductive elements of the first plurality of conductive elements and the second plurality of conductive elements, respectively.

9. (Canceled)

10. (Previously presented) The receptacle as defined in claim 1, wherein the first plurality of conductive elements is molded in the first monolithic housing member, and the second plurality of conductive elements is molded in the second monolithic housing member.

11. (Currently amended) The receptacle as defined in claim 1, wherein:

the housing, the first monolithic housing member, and the second monolithic housing member are made of an insulative material;

the receptacle is in combination with a metallic cage; and

the receptacle is disposed within the cage.

12. (Original) The receptacle as defined in claim 1, wherein the housing includes at least one projection from a lower surface thereof.

13. (Original) The receptacle as defined in claim 1, further comprising a shell adapted for attachment of the housing to the printed circuit board.

14. (Previously presented) The receptacle as defined in claim 1, wherein the housing further comprises a second cavity bounded by a third surface and an opposing fourth surface, further comprising a third lead assembly including a third plurality of conductive elements disposed in a third monolithic housing member and a fourth lead assembly including a fourth plurality of conductive elements disposed in a fourth monolithic housing member, each conductive element of the third and fourth pluralities of conductive elements comprising a contact tail adapted for attachment to the printed circuit board, a mating contact portion and an intermediate portion coupling the contact tail to the mating contact portion, wherein the mating contact portions of the third plurality of conductive elements are disposed along the third surface of the second cavity and

the mating contact portions of the fourth plurality of conductive elements are disposed along the fourth surface of the second cavity.

15. (Previously presented) The receptacle of claim 23, wherein:

for each conductive element of a first subset of the first plurality of conductive elements, a portion of the conductive element is exposed through the first monolithic housing member, and

for each conductive element of a second subset of the second plurality of conductive elements, a portion of the conductive element is exposed through the second monolithic housing member.

16. (Original) The receptacle of claim 15, wherein:

a first surface of the insert comprises a first plurality of projections, each projection of the first plurality of projections being coupled to a conductive element of the first subset; and

a second surface of the insert comprises a second plurality of projections, each projection of the second plurality of projections being coupled to a conductive element of the second subset.

17. (Original) The receptacle of claim 16, wherein:

the first plurality of conductive elements comprises conductive elements disposed in a plurality of pairs of conductive elements; and

the first subset of the first plurality of conductive elements comprises conductive elements each of which is disposed adjacent a pair of the plurality of pairs.

18. (Previously presented) The receptacle of claim 23, wherein the insert includes a conductive material.

19. (Previously presented) The receptacle of claim 23, wherein the insert is at least partially conductive.

20. (Previously presented) The receptacle as defined in claim 23, wherein:

the insert includes an electrically lossy material; and

the electrically lossy material is electrically coupled to selected ones of the first plurality of conductive elements and the second plurality of conductive elements.

21. (Original) The receptacle as defined in claim 20, wherein:

the first plurality of conductive elements are positioned in a first row, the first row comprising pairs of the first plurality of conductive elements separated by single conductive elements of the first plurality of conductive elements;

the second plurality of conductive elements are positioned in a second row, the second row comprising pairs of the second plurality of conductive elements separated by single conductive elements of the second plurality of conductive elements; and

the electrically lossy material is selectively electrically coupled to the single conductive elements of the first plurality of conductive elements and second plurality of conductive elements.

22. (Original) The receptacle as defined in claim 21, wherein:

the insert includes projections towards the selected ones of the conductive elements.

23. (Previously presented) The receptacle as defined in claim 1, further comprising an insert disposed between the first and second lead assemblies.

24. (Currently amended) A receptacle adapted for mounting to a printed circuit board, comprising:

a housing having a cavity bounded by a first surface that is parallel to the printed circuit board and a second surface that faces the first surface and is parallel to the printed circuit board;

a first lead assembly including:

a first plurality of conductive elements disposed along a first direction, each comprising a mating contact portion extending along the first surface of the cavity in a second direction perpendicular to the first direction, a contact tail adapted for attachment to the printed circuit board and disposed perpendicular to the mating contact portion, and an

intermediate portion coupling the contact tail to the mating contact portion and comprising a right angle bend,

wherein the first plurality of conductive elements comprise signal pairs and ground conductors with the signal pairs positioned between adjacent ground conductors; and

a first monolithic housing member molded over the intermediate portions of each conductive element of the first plurality of conductive elements; and

a second lead assembly, separate and distinct from the first lead assembly, including:

a second plurality of conductive elements disposed along [[a]]the first direction, that are longer than the first plurality of conductive elements and each comprise a mating contact portion extending along the second surface of the ~~housing~~ cavity in the second direction, a contact tail adapted for attachment to the printed circuit board and disposed perpendicular to the mating contact portion, and an intermediate portion coupling the contact tail to the mating contact portion and comprising a right angle bend,

wherein the second plurality of conductive elements comprise signal pairs and ground conductors with the signal pairs positioned between adjacent ground conductors; and

a second monolithic housing member molded over the intermediate portions of each conductive element of the second plurality of conductive elements; and

wherein the contact tails of the first plurality of conductive elements are aligned along the first direction, and the contact tails of the second plurality of conductive elements are aligned along the first direction.

25. (Currently amended) A receptacle adapted for mounting to a printed circuit board, comprising:

a monolithic housing made of an insulative material and having a cavity bounded by a first surface that is parallel to the printed circuit board and a second surface that faces the first surface and is parallel to the printed circuit board;

a first lead assembly including:

a first plurality of conductive elements disposed along a first direction, each of the first plurality of conductive elements comprising a mating contact portion extending along

the first surface of the cavity in a second direction perpendicular to the first direction, a contact tail adapted for attachment to at least one first hole in the printed circuit board and disposed perpendicular to the mating contact portion, and an intermediate portion coupling the contact tail to the mating contact portion and comprising a right angle bend, such that each intermediate portion comprises a first portion parallel to the first surface and a second portion perpendicular to the first surface; and

a first monolithic housing member made of an insulative material[[,]] molded over the first portions of the intermediate portions of each conductive element of the first plurality of conductive elements and disposed within the monolithic housing~~, and comprising exterior projections extending along the first direction~~; and

a second lead assembly, separate and distinct from the first lead assembly, including:

a second plurality of conductive elements disposed along the first direction, each of the second plurality of conductive elements comprising a mating contact portion extending along the second surface of the ~~housing~~ cavity in the first direction, a contact tail adapted for attachment to at least one second hole in the printed circuit board and disposed perpendicular to the mating contact portion, and an intermediate portion coupling the contact tail to the mating contact portion and comprising a right angle bend, such that each intermediate portion comprises a first portion parallel to the first surface and a second portion perpendicular to the first surface; and

a second monolithic housing member made of an insulative material[[,]] molded over the first portions of the intermediate portions of each conductive element of the second plurality of conductive elements and disposed within the monolithic housing~~, and comprising exterior projections extending along the first direction~~.

26. (Previously presented) The receptacle as defined in claim 1, wherein the contact tails of the first and second plurality of conductive elements are configured for attachment to conductive pads on a surface of the printed circuit board.

27. (Currently amended) A receptacle adapted for mounting to a printed circuit board, comprising:

a housing made of an insulative material and having:

a first cavity shaped to receive a first plug in an insertion direction, wherein the first cavity is bounded by a first surface that is parallel to the printed circuit board and a second surface that faces the first surface and is parallel to the printed circuit board;

a second cavity offset from the first cavity in a direction perpendicular to the insertion direction, wherein the second cavity is shaped to receive a second plug in the insertion direction, and the second cavity and is bounded by a third surface that is parallel to the printed circuit board and a fourth surface that faces the third surface and is parallel to the printed circuit board;

a first lead assembly comprising:

a first plurality of conductive elements disposed in a row extending in a first direction, each of the first plurality of conductive elements comprising a mating contact portion extending along the first surface of the cavity in a second direction parallel to the insertion direction, a contact tail extending from the monolithic housing, and an intermediate portion coupling the contact tail to the mating contact portion and comprising a right angle bend; and

a first housing member made of an insulative material, molded over the intermediate portions of each conductive element of the first plurality of conductive elements; and

a second lead assembly, separate and distinct from the first lead assembly, comprising:

a second plurality of conductive elements disposed in a row extending in the first direction, each of the second plurality of conductive elements comprising a mating contact portion extending along the second surface of the first cavity in the second direction, a contact tail extending from the monolithic housing, and an intermediate portion coupling the contact tail to the mating contact portion and comprising a right angle bend; and

a second housing member made of an insulative material, molded over the intermediate portions of each conductive element of the second plurality of conductive elements;

a third lead assembly comprising:

a third plurality of conductive elements disposed in a row extending in the first direction, each of the third plurality of conductive elements comprising a mating contact portion extending along the third surface of the second cavity in the second direction, a contact tail extending from the monolithic housing, and an intermediate portion coupling the contact tail to the mating contact portion and comprising a right angle bend; and

a third housing member made of an insulative material, molded over the intermediate portions of each conductive element of the third plurality of conductive elements; and

a fourth lead assembly, comprising:

a fourth plurality of conductive elements disposed in a row extending in the first direction, each of the fourth plurality of conductive elements comprising a mating contact portion extending along the fourth surface of the second cavity in the second direction, a contact tail extending from the monolithic housing, and an intermediate portion coupling the contact tail to the mating contact portion and comprising a right angle bend; and

a fourth housing member made of an insulative material, molded over the intermediate portions of each conductive element of the fourth plurality of conductive elements;

wherein:

the first, second, third and fourth housing members engage with the housing to hold the intermediate portions of the first, second, third and fourth plurality of conductive elements relative to the circuit board, and

the receptacle is in combination with a metallic cage, and the receptacle is disposed within the cage.

28. (Previously presented) The receptacle as defined in claim 27, wherein the contact tails of the first, second, third and fourth plurality of conductive elements are configured for attachment to conductive pads on a surface of the printed circuit board.

29. (Previously presented) The receptacle as defined in claim 27, wherein the first housing member engages with the second housing member and the third housing member engages with the fourth housing member.

30. (Previously presented) The receptacle as defined in claim 27, wherein:

each of the first, second, third and fourth lead assemblies is L-shaped; and

the first, second, third and fourth housing members engage with the housing so as to hold the first, second, third and fourth lead assemblies within the housing with the L-shaped first, second, third and fourth housing members nested.

31. (New) The receptacle as defined in claim 24, wherein:

each of the first plurality of conductive elements and of the second plurality of conductive elements have a broad side and edges;

the first plurality of conductive elements are disposed with an edge of each conductive element facing an edge of an adjacent conductive element of the first plurality of conductive elements; and

the second plurality of conductive elements are disposed with an edge of each conductive element facing an edge of an adjacent conductive element of the second plurality of conductive elements.

32. (New) The receptacle as defined in claim 31, wherein:

the right angle bend of the intermediate portions of the first plurality of conductive elements is about a line perpendicular to the edges of the first plurality of conductive elements; and

the right angle bend of the intermediate portions of the second plurality of conductive elements is about a line perpendicular to the edges of the second plurality of conductive elements.

33. (New) The receptacle as defined in claim 24, wherein:

the ground conductors of the first plurality of conductive elements are wider in the first direction than the conductive elements comprising signal pairs of the first plurality of conductive elements; and

the ground conductors of the second plurality of conductive elements are wider in the first direction than the conductive elements comprising signal pairs of the second plurality of conductive elements.

REMARKS

In response to the Office Action mailed December 4, 2018, Applicant respectfully requests reconsideration in view of the amendments and the following remarks. Claims 1-8 and 10-30 were previously pending in this application. No claims are canceled herein. Claims 1, 11, 24, 25, and 27 are amended herein. Claims 31-33 are added herein. As a result, claims 1-8 and 10-33 are pending for examination with claims 1, 24, 25, and 27 being independent claims. No new matter is added herein. The application as presented is believed to be in condition for allowance.

CLAIM OBJECTIONS

Claim 24 is objected to for reciting "a first direction." The claim is amended herein to recite, at least in part, "the first direction." Accordingly, withdrawal of the objection to claim 24 is respectfully requested.

REJECTIONS UNDER 35 U.S.C. § 103

Claims 1, 6-8, 10, and 23-30 are rejected under 35 U.S.C. § 103 as allegedly being unpatentable over U.S. Patent No. 6,296,496 to Trammel (hereinafter "Trammel") in view of U.S. Patent No. 5,474,472 to Niwa et al. (hereinafter "Niwa"). Reconsideration is requested in view of the foregoing amendments and the following remarks.

A. Independent Claim 1

Without conceding that the rejection of independent claim 1 was proper, the claim is amended herein to advance prosecution. Support for amended claim 1 can be found throughout the application, including at least in FIGs. 5-6. Amended independent claim 1 recites:

> A receptacle adapted for mounting to a printed circuit board, comprising:
>
> a housing having a cavity bounded by a first surface that is parallel to the printed circuit board and an opposing second surface that is parallel to the printed circuit board, each of the first and second surfaces being disposed above a first side of the printed circuit board;

a first lead assembly including:

a first monolithic housing member; and

a first plurality of conductive elements each comprising a contact tail adapted for attachment to the printed circuit board that is perpendicular to the first side of the printed circuit board, a mating contact portion disposed along the first surface of the cavity, and an intermediate portion disposed in the first monolithic housing member and coupling the contact tail to the mating contact portion,

wherein the first monolithic housing member comprises exterior projections extending away from the first plurality of conductive elements along a direction parallel to the first surface; and

a second lead assembly including:

a second monolithic housing member; and

a second plurality of conductive elements each comprising a contact tail adapted for attachment to the printed circuit board that is perpendicular to the first side of the printed circuit board, a mating contact portion disposed along the second surface of the cavity, and an intermediate portion disposed in the second monolithic housing member coupling the contact tail to the mating contact portion,

wherein the second monolithic housing member comprises exterior projections extending away from the second plurality of conductive elements along the direction parallel to the first surface (emphasis added).

Trammel and Niwa fail to describe at least the above-emphasized language of amended independent claim 1. In particular, Trammel and Niwa fail to disclose "wherein the first monolithic housing member comprises exterior projections extending away from the first plurality of conductive elements along a direction parallel to the first surface," and "wherein the second monolithic housing member comprises exterior projections extending away from the second plurality of conductive elements along the direction parallel to the first surface." The Office Action alleges that terminal cores 401 and 402 in Trammel have projections as claimed. However, even if

terminal cores 401 and 402 can be regarded as having projections, there are no projections extending away from signal contacts 20 along a direction parallel to a first surface of main body 11 (Trammel, FIGs. 1-2). Furthermore, no other portions of Trammel describe this language. To the contrary, FIG. 1 of Trammel the exterior surfaces of terminal cores 401 and 402 from which projections would have to be located to "extend[ing] away from the second plurality of conductive elements along the direction parallel to the first surface."

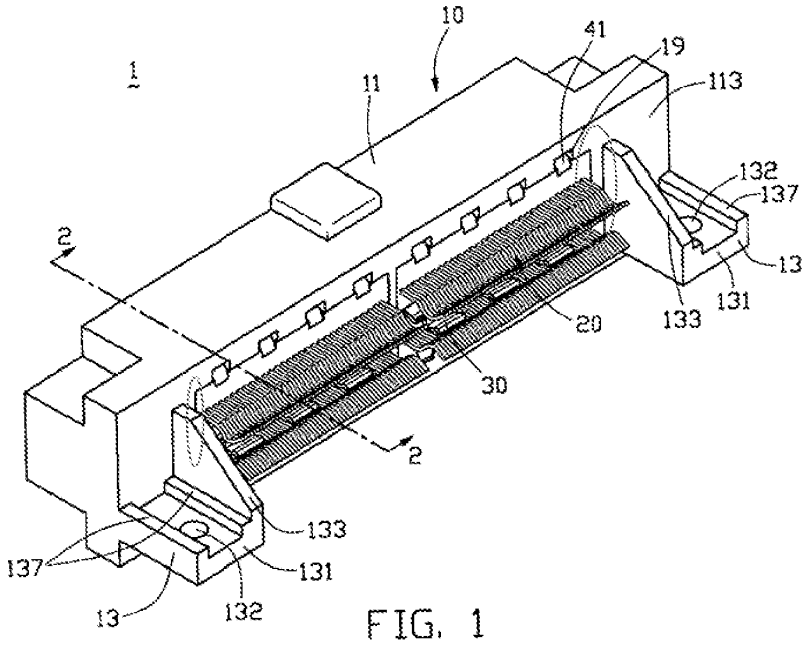

FIG. 1

Thus, Trammel fails to describe at least the "exterior projections" of amended independent claim 1.

Niwa fails to cure the deficiency in Trammel, at least because Niwa also fails to describe "wherein the first monolithic housing member comprises exterior projections extending away from the first plurality of conductive elements along a direction parallel to the first surface," and "wherein the second monolithic housing member comprises exterior projections extending away from the second plurality of conductive elements in the direction parallel to the first surface," and the Office Action does not allege that Niwa does.

For at least these reasons, amended independent claim 1 patentably distinguishes over Trammel and Niwa, both alone and in combination. Accordingly withdrawal of the rejection of independent claim 1 and claims depending therefrom is respectfully requested.

B. Independent Claim 24

Without conceding that the rejection of independent claim 24 was proper, the claim is amended herein to advance prosecution. Support for amended independent claim 24 can be found throughout the application, including at least in FIG. 6. Amended independent claim 24 recites:

> A receptacle adapted for mounting to a printed circuit board, comprising:
>
> a housing having a cavity bounded by a first surface that is parallel to the printed circuit board and a second surface that faces the first surface and is parallel to the printed circuit board;
>
> a first lead assembly including:
>
> a first plurality of conductive elements disposed along a first direction, each comprising a mating contact portion extending along the first surface of the cavity in a second direction perpendicular to the first direction, a contact tail adapted for attachment to the printed circuit board and disposed perpendicular to the mating contact portion, and an intermediate portion coupling the contact tail to the mating contact portion and comprising a right angle bend,
>
> ***wherein the first plurality of conductive elements comprise signal pairs and ground conductors with the signal pairs positioned between adjacent ground conductors***; and
>
> a first monolithic housing member molded over the intermediate portions of each conductive element of the first plurality of conductive elements; and
>
> a second lead assembly, separate and distinct from the first lead assembly, including:
>
> a second plurality of conductive elements disposed along the first direction, that are longer than the first plurality of conductive elements and each comprise a mating contact portion extending along the second surface of the cavity in the

> second direction, a contact tail adapted for attachment to the printed circuit board and disposed perpendicular to the mating contact portion, and an intermediate portion coupling the contact tail to the mating contact portion and comprising a right angle bend,
>
> ***wherein the second plurality of conductive elements comprise signal pairs and ground conductors with the signal pairs positioned between adjacent ground conductors***; and
>
> a second monolithic housing member molded over the intermediate portions of each conductive element of the second plurality of conductive elements; and
>
> ***wherein the contact tails of the first plurality of conductive elements are aligned along the first direction, and the contact tails of the second plurality of conductive elements are aligned along the first direction*** (emphasis added).

Trammel and Niwa fail to describe at least the above-emphasized language of amended independent claim 24. Trammel and Niwa fail to describe "wherein the first plurality of conductive elements comprise signal pairs and ground conductors with the signal pairs positioned between adjacent ground conductors" and "wherein the second plurality of conductive elements comprise signal pairs and ground conductors with the signal pairs positioned between adjacent ground conductors," as detailed below.

Both Trammel and Niwa have different ground structures such that, even if combined, the combination would not have the pattern of signal and ground contacts recited in the claims. Trammel includes rows of signal contacts 21 with a ground plate 30 disposed between the rows (FIG. 2 and col. 3, lines 5-30). Niwa similarly has a metal plate (20, 42) as in Trammel. Thus, Trammel and Niwa, whether considered alone or in combination, fail to describe at least "the first plurality of conductive elements comprise signal pairs and ground conductors with the signal pairs positioned between adjacent ground conductors" and "the second plurality of conductive elements comprise signal pairs and ground conductors with the signal pairs positioned between adjacent ground conductors."

Further, even if the combination of Trammel and Niwa were modified to have the claimed pattern of signal and ground conductors, which Applicants contend would be improper, the combination would fail to have "the contact tails of the first plurality of conductive elements are aligned along the first direction, and the contact tails of the second plurality of conductive elements are aligned along the first direction."

The alleged combination of Trammel and Niwa allegedly has contact tails as in Niwa to include a right angle bend. However, as can be seen, for example in FIG. 2 of Niwa, contact tails of each of the rows of contacts 16a, 16b, 16c and 16d are not aligned. Rather, the tail of every contact is offset from the adjacent contacts in the row. Thus, the proposed combination would not meet the language of the claim requiring "the contact tails of the first plurality of conductive elements are aligned along the first direction, and the contact tails of the second plurality of conductive elements are aligned along the first direction."

For at least these reasons, amended independent claim 24 patentably distinguishes over Trammel and Niwa. Accordingly, withdrawal of the rejection of independent claim 24 is respectfully requested.

C. Independent Claim 25

Without conceding that the rejection of independent claim 25 was proper, the claim is amended herein to advance prosecution. Support for amended independent claim 25 can be found throughout the application, including at least in FIG. 6. Amended independent claim 25 recites:

> A receptacle adapted for mounting to a printed circuit board, comprising:
>
> > ***a monolithic housing made of an insulative material*** and having a cavity bounded by a first surface that is parallel to the printed circuit board and a second surface that faces the first surface and is parallel to the printed circuit board;
> >
> > a first lead assembly including:
> >
> > > a first plurality of conductive elements disposed along a first direction, each of the first plurality of conductive elements comprising a mating contact portion extending along the first surface of the cavity in a second direction perpendicular to the first direction, a contact tail adapted for attachment to at least one first hole in the printed circuit board and disposed perpendicular to

> the mating contact portion, and an intermediate portion coupling the contact tail to the mating contact portion and comprising a right angle bend, ***such that each intermediate portion comprises a first portion parallel to the first surface and a second portion perpendicular to the first surface***; and
>
> ***a first monolithic housing member made of an insulative material molded over the first portions of the intermediate portions of each conductive element of the first plurality of conductive elements and disposed within the monolithic housing***; and
>
> a second lead assembly, separate and distinct from the first lead assembly, including:
>
> a second plurality of conductive elements disposed along the first direction, each of the second plurality of conductive elements comprising a mating contact portion extending along the second surface of the cavity in the first direction, a contact tail adapted for attachment to at least one second hole in the printed circuit board and disposed perpendicular to the mating contact portion, and an intermediate portion coupling the contact tail to the mating contact portion and comprising a right angle bend, ***such that each intermediate portion comprises a first portion parallel to the first surface and a second portion perpendicular to the first surface***; and
>
> ***a second monolithic housing member made of an insulative material molded over the first portions of the intermediate portions of each conductive element of the second plurality of conductive elements and disposed within the monolithic housing*** (emphasis added).

Applicants respectfully disagree that Trammel and Niwa teach a receptacle meeting all language of the claim 25, including at the above-emphasized language of amended independent claim 25.

The Office Action cites Trammel as teaching the "housing" and the "first monolithic housing member" and "the second monolithic housing member" of the claim 25. However, Trammel has a die cast metal housing 10 (FIG. 3 and col. 2, lines 38-43), and does not meet the language of claim 25 reciting "a monolithic housing made of an insulative material." There is no reason that one of skill in the art would have modified the die cast metal component to be "a monolithic housing made of an insulative material." Thus, the rejection should be withdrawn.

As a further reason that the rejection should be withdrawn, one of skill in the art would not have ***both*** modified the die cast metal housing 10 of Trammel to be "made of an insulative material"

and retained the components that the Office Action alleges are the "first monolithic housing member" and the second monolithic housing member." The Office Action cites elements 401 and 402 of Trammel as being the claimed "first monolithic housing member made of an insulative material" and the second monolithic housing member made of an insulative material." However, Trammel describes these components as "terminal cores," which are understood to have insulative portions to insulate the signal contacts from the metal housing 10. If the housing 10, were made of "a monolithic housing made of an insulative material," then the insulative material would terminal cores elements 401 and 402 would no longer be necessary. To the contrary, the signal conductors could be inserted into the housing without an intermediate insulator, as is shown, for example, in FIG. 2 of Niwa, which is illustrated as having an insulative housing.

Thus, amended independent claim 25 patentably distinguishes over Trammel and Niwa, both alone and in combination. Accordingly, withdrawal of the rejection of independent claim 25 is respectfully requested.

D. Independent Claim 27

Without conceding that the rejection of independent claim 27 was proper, the claim is amended herein to advance prosecution. Support for amended independent claim 27 can be found throughout the application, including at least in FIGs. 2-3. Amended independent claim 27 recites:

> A receptacle adapted for mounting to a printed circuit board, comprising:
>
> ***a housing made of an insulative material*** and having:
>
> a first cavity shaped to receive a first plug in an insertion direction, wherein the first cavity is bounded by a first surface that is parallel to the printed circuit board and a second surface that faces the first surface and is parallel to the printed circuit board;
>
> a second cavity offset from the first cavity in a direction perpendicular to the insertion direction, wherein the second cavity is shaped to receive a second plug in the insertion direction, and the second cavity and is bounded by a third surface that is parallel to the printed circuit board and a fourth

surface that faces the third surface and is parallel to the printed circuit board;

a first lead assembly comprising:

a first plurality of conductive elements disposed in a row extending in a first direction, each of the first plurality of conductive elements comprising a mating contact portion extending along the first surface of the cavity in a second direction parallel to the insertion direction, a contact tail extending from the monolithic housing, and an intermediate portion coupling the contact tail to the mating contact portion and comprising a right angle bend; and

a first housing member made of an insulative material, molded over the intermediate portions of each conductive element of the first plurality of conductive elements; and

a second lead assembly, separate and distinct from the first lead assembly, comprising:

a second plurality of conductive elements disposed in a row extending in the first direction, each of the second plurality of conductive elements comprising a mating contact portion extending along the second surface of the first cavity in the second direction, a contact tail extending from the monolithic housing, and an intermediate portion coupling the contact tail to the mating contact portion and comprising a right angle bend; and

a second housing member made of an insulative material, molded over the intermediate portions of each conductive element of the second plurality of conductive elements;

a third lead assembly comprising:

a third plurality of conductive elements disposed in a row extending in the first direction, each of the third plurality of conductive elements comprising a mating contact portion extending along the third surface of the second cavity in the second direction, a contact tail extending from the monolithic housing, and an intermediate portion coupling the contact tail to the mating contact portion and comprising a right angle bend; and

> a third housing member made of an insulative material, molded over the intermediate portions of each conductive element of the third plurality of conductive elements; and
>
> a fourth lead assembly, comprising:
>
> a fourth plurality of conductive elements disposed in a row extending in the first direction, each of the fourth plurality of conductive elements comprising a mating contact portion extending along the fourth surface of the second cavity in the second direction, a contact tail extending from the monolithic housing, and an intermediate portion coupling the contact tail to the mating contact portion and comprising a right angle bend; and
>
> a fourth housing member made of an insulative material, molded over the intermediate portions of each conductive element of the fourth plurality of conductive elements;
>
> wherein:
>
> the first, second, third and fourth housing members engage with the housing to hold the intermediate portions of the first, second, third and fourth plurality of conductive elements relative to the circuit board, and
>
> ***the receptacle is in combination with a metallic cage, and the receptacle is disposed within the cage*** (emphasis added).

One of ordinary skill in the art would not have modified Trammel such that "the receptacle is in combination with a metallic cage, and the receptacle is disposed within the cage," in combination with the other language of claim 27, including "a housing made of an insulative material," "a first housing member made of an insulative material, molded over the intermediate portions of each conductive element of the first plurality of conductive elements,"… "a fourth housing member made of an insulative material, molded over the intermediate portions of each conductive element of the fourth plurality of conductive elements."

Trammel has a die cast metal housing 10 (FIG. 3 and col. 2, lines 38-43). As should be appreciated from the discussion of Trammel in connection with claim 25, one of skill in the art had no reason to substitute the die cast metal housing of trammel for "a housing made of an insulative material." Moreover, even if such a substitution were made, there would have been no reason to also retain the elements of Trammel that the Office Action asserts are "a first housing member made of an insulative material, molded over the intermediate portions of each conductive element of the first plurality of conductive elements,"… "a fourth housing member made of an insulative material, molded over the intermediate portions of each conductive element of the fourth plurality of conductive elements."

Further, there is no reason that one of skill in the art would have, after converting the die cast metal housing into "a housing made of an insulative material" to then add "a metallic cage, and the receptacle is disposed within the cage." To the contrary, Trammel specifically teaches simplifying manufacture (col. 1, 57-58). The proposed modification results in adding a component to achieve the same metal exterior provided by Trammel in its un-modified form. Such a modification would have been contrary to the teachings of Trammel and cannot be a basis for finding the claim obvious.

For at least this reason, amended independent claim 27 patentably distinguishes over Trammel and Niwa, both alone and in combination. Accordingly, withdrawal of the rejection of independent claim 27 and claims depending therefrom is respectfully requested.

NEW CLAIMS

Claims 31-33 are added herein. Support for claims 31-33 can be found throughout the application, including at least in FIG. 6. Claims 31-33 depend from independent claim 24 and are allowable for at least the same reasons. Accordingly, allowance of claims 31-33 is respectfully requested.

GENERAL COMMENTS ON DEPENDENT CLAIMS

Since each of the dependent claims depends from a base claim that is believed to be in condition for allowance, for the sake of brevity, Applicant believes that it is unnecessary at this time

to argue the further distinguishing features of the dependent claims. However, Applicant does not necessarily concur with the interpretation of the previously presented dependent claims as set forth in the Office Action, nor does Applicant concur that the basis for rejection of any of the previously presented dependent claims is proper. Therefore, Applicant reserves the right to specifically address the further patentability of the dependent claims in the future.

CONCLUSION

In view of the foregoing amendments and remarks, reconsideration is respectfully requested. This application should now be in condition for allowance; a notice to this effect is respectfully requested. If the Examiner believes, after this amendment, that the application is not in condition for allowance, the Examiner is requested to call the Applicant's attorney at the telephone number listed below.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. Applicant believes no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 23/2825 under Docket No. A0863.70051US04 from which the undersigned is authorized to draw.

Dated: April 4, 2019

Respectfully submitted,

By /Edmund J. Walsh/
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DOCKET NO.: A0863.70051US04

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor:	Donald W. Milbrand, Jr.
Application No.:	15/065,683
Confirmation No.:	5112
Filed:	March 9, 2016
For:	HIGH PERFORMANCE CABLE CONNECTOR
Examiner:	F. O. Figueroa
Art Unit:	2833

Certificate of Electronic Filing under 37 C.F.R. § 1.8

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being transmitted via the Office's electronic filing system in accordance with 37 C.F.R. § 1.6(a)(4).

Dated: April 4, 2019 Electronic Signature for: /Trish McDonald/

MAIL STOP RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

STATEMENT FILED PURSUANT TO THE DUTY OF DISCLOSURE UNDER 37 C.F.R. §§ 1.56, 1.97 AND 1.98

Sir:

Pursuant to the duty of disclosure under 37 C.F.R. §§ 1.56, 1.97 and 1.98, the undersigned requests consideration of this Information Disclosure Statement.

PART I: Compliance with 37 C.F.R. § 1.97

This Information Disclosure Statement has been filed before the mailing of a first Office Action after the filing of a Request for Continued Examination under 37 C.F.R. § 1.114.

No fee or certification is required.

PART II: Information Cited

The undersigned hereby makes of record in the above-identified application the information listed on the attached form PTO-1449 (modified PTO/SB/08). The order of presentation of the references should not be construed as an indication of the importance of the references.

The undersigned hereby makes the following additional information of record in the above-identified application.

The undersigned would like to bring to the Examiner's attention the following co-pending applications that may contain subject matter related to this application:

Serial No.	Filing Date	Inventor(s)	Docket No.
*15/683,199	08-22-2017	Kirk et al.	A0863.70102US01
*15/742,244	01-05-2018	Sasame et al.	A1156.70241US00

*A copy of this reference is not provided as the Office has waived the requirement under 37 C.F.R. § 1.98(a)(2)(iii) for submitting a copy of a cited U.S. patent application if it is scanned to the Image File Wrapper system and is available on Private PAIR .

The above-identified co-pending applications may include subject matter that is technically-related to subject matter of the present application and may contain claims that recite elements similar to those recited in claims of the present application. In handling prosecution of the above-identified applications, the Examiners for these other applications presumably will search for relevant prior art and, in some circumstances, may take positions about the prior art and/or the interpretation of the claims that may be material to the examination of the present application.

Accordingly, the Examiner in the present application is requested to review the file histories of the above-identified co-pending applications to see whether there is any information that the Examiner believes may be relevant to the prosecution of the present application. It is assumed that the Examiner has access to the file histories of the above-identified applications. However, if the Examiner would like copies of any or all of the information included in the file histories of the above-identified applications, the Examiner is asked to contact the undersigned representative.

PART III: Remarks

Documents cited anywhere in the Information Disclosure Statement are enclosed unless otherwise indicated. It is respectfully requested that:

1. The Examiner consider completely the cited information, along with any other information, in reaching a determination concerning the patentability of the present claims;

2. The enclosed form PTO-1449 (modified PTO/SB/08) be signed by the Examiner to evidence that the cited information has been fully considered by the United States Patent and Trademark Office during the examination of this application;

3. The citations for the information be printed on any patent which issues from this application.

By submitting this Information Disclosure Statement, the undersigned makes no representation that a search has been performed, of the extent of any search performed, or that more relevant information does not exist.

By submitting this Information Disclosure Statement, the undersigned makes no representation that the information cited in the Statement is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b).

By submitting this Information Disclosure Statement, the undersigned makes no representation that the information cited in the Statement is, or is considered to be, in fact, prior art as defined by 35 U.S.C. § 102.

Notwithstanding any statements by the undersigned, the Examiner is urged to form his or her own conclusion regarding the relevance of the cited information.

An early and favorable action is hereby requested.

The Director is hereby authorized to charge any deficiency or credit any overpayment in the fees occasioned by the filing of this Information Disclosure Statement to our Deposit Account No. 23/2825 under Docket No. A0863.70051US04 from which the undersigned is authorized to draw.

Respectfully submitted,

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Docket No.: A0863.70051US04
Date: April 4, 2019

FORM PTO-1449/A and B (modified PTO/SB/08)	APPLICATION NO.: 15/065,683	ATTY. DOCKET NO.: A0863.70051US04
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	FILING DATE: March 9, 2016	CONFIRMATION NO.: 5112
	FIRST NAMED INVENTOR: Donald W. Milbrand, Jr.	
Sheet 1 of 2	GROUP ART UNIT: 2833	EXAMINER: F. O. Figueroa

U.S. PATENT DOCUMENTS

Examiner's Initials #	Cite No.	U.S. Patent Document Number	Kind Code	Name of Patentee or Applicant of Cited Document	Date of Publication or Issue of Cited Document MM-DD-YYYY
		5,176,538	A	Hansell III et al.	01-05-1993
		5,334,050	A	Andrews	08-02-1994
		6,409,543	B1	Astbury, Jr. et al.	06-25-2002
		10,243,304		Kirk et al.	03-26-2019
		2004-0005815	A1	Mizumura et al.	01-08-2004
		2005-0233610	A1	Tutt et al.	10-20-2005
		2006-0255876	A1	Kushta et al.	11-16-2006
		2009-0305533	A1	Feldman et al.	12-10-2009
		2018-0062323	A1	Kirk et al.	03-01-2018
		2018-0145438	A1	Cohen	05-24-2018
		2018-0219331	A1	Cartier et al.	08-02-2018

FOREIGN PATENT DOCUMENTS

Examiner's Initials #	Cite No.	Foreign Patent Document Office/ Country	Number	Kind Code	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Translation (Y/N)
		CN	1179448	C	Whitaker Corp	12-08-2004	Y
		CN	1799290	A	Nippon Electric Co	07-05-2006	Y
		CN	101120490	B	Amphenol Corp	11-17-2010	Y
		CN	101176389	A	Teradyne Inc	05-07-2008	Y
		CN	101600293	A	Hongfujin Prec Ind Shenzhen	12-09-2009	Y
		CN	101600293	B	Hongfujin Prec Ind Shenzhen	05-16-2012	Y
		CN	201846527	U	Molex Inc	05-25-2011	Y
		DE	60216728	T2	Amphenol Corp	11-08-2007	Y-abstract only; see also US6409543
		EP	1018784	A1	Fci S Hertogenbosch Bv	07-12-2000	
		JP	2001-510627	A		07-31-2001	Y-abstract only; see also WO9835409
		MX	9907324	A	Teradyne, Inc.	08-01-2000	Y-abstract only
		WO	98/35409	A1	Teradyne, Inc	08-13-1998	

EXAMINER:	DATE CONSIDERED:

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

7061174.1

FORM PTO-1449/A and B (modified PTO/SB/08)				APPLICATION NO.: 15/065,683	ATTY. DOCKET NO.: A0863.70051US04
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				FILING DATE: March 9, 2016	CONFIRMATION NO.: 5112
				FIRST NAMED INVENTOR: Donald W. Milbrand, Jr.	
Sheet	2	of	2	GROUP ART UNIT: 2833	EXAMINER: F. O. Figueroa

OTHER ART -- NON PATENT LITERATURE DOCUMENTS

Examiner's Initials #	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	Translation (Y/N)

[NOTE – No copies of U.S. patents, published U.S. patent applications, or pending, unpublished patent applications stored in the USPTO's Image File Wrapper (IFW) system, are included. See 37 CFR § 1.98 and 1287OG163. Copies of all other patent(s), publication(s), unpublished, pending U.S. patent applications, or other information listed are provided as required by 37 CFR § 1.98 unless 1) such copies were provided in an IDS in an earlier application that complies with 37 CFR § 1.98, and 2) the earlier application is relied upon for an earlier filing date under 35 U.S.C. § 120.]

EXAMINER:	DATE CONSIDERED:

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

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Application number: CN19971097808
Application date: 19970909
Priority: US19960714024 19960911 US19960714024; US19970882795 19970626 US19970882795;
Assignee: ????? ;
Assignee[std]: WHITAKER CORP ;
Inventor: RN WHYNE ; SK MICKIEVICZ ; S?K?????? ; ?? ;
Inventor[std]: WHYNE R N ; MICKIEVICZ S K ;
International class[1-7]: H01R23/68 ;
International class[8]: H01R12/50;
Cooperative Patent class: H01R13/6587 ;
Family members: AU199742599 A1 CN1179448 C CN1230296 A DE69711716 D1 DE69711716 T2 EP1012925 A1 EP1012925 B1 JP2002513502 T2 JP3889447 B2 US5795191 A WO9811633 A1

Title: CONNECTOR ASSEMBLY WITH SHIELDED MODULES AND METHOD OF MAKING SAME ??????????????????

Title: 带有屏蔽模件的连接器组件及其制造方法

Abstract:

??????(10),???????(12)?????????????(30)??????????(60)??????(30)???????????????(42,44),???????(50)????????????,????,?????(42)????????????(54)??????????(32)??,??????(44)???????????(54)?,?????????(34)???????????(10)?,????(42)???(32)????(60)?????,?????(44)???(34)????(60)?????,???????????(40)????????(60)????????????(40)????????

Abstract:

电连接器组件(10)，它包括绝缘机壳(12)和装配到其上的多个终端组件(30)和在其间的导电屏蔽件(60)。各终端模件(30)包括呈交错构型的第一和第二接点(42，44)，它们的中间部分(50)形成在沿之所选择的位置上，沿此位置，使第一接点(42)的中间部分封装到绝缘腹板(54)中与此模件的第一侧面(32)邻近，且使第二接点(44)的中间部分密封到此腹板(54)中，与此模件的第二侧面(34)邻近。在组装好的连接器(10)中，第一接点(42)沿表面(32)与屏蔽件(60)分开得较近，而第二接点(44)沿表面(34)与屏蔽件(60)分开得较近，由此确保了在各信号接点(40)与相应接地屏蔽件(60)之间而不是与相邻信号接点(40)之间有基本耦合。

The electrical connector assembly (10) comprising an insulating housing (12) and fitted to a plurality of terminal assembly thereon (30) therebetween and a conductive shield (60). Each terminal module (30) comprises a staggered configuration of the first and second contacts (42, 44), which intermediate portion (50) is formed at a position of the selected edge on the edge position of the first contact point (42) to the intermediate portion of the first side surface of the insulating package web (54) with the mold member (32) adjacent and the second contact point (44) of the intermediate portion of this sealing web (54), and this module is the second side (34) adjacent. In the assembled connector (10), the first contacts (42) along the surface (32) of the shield member (60) more closely to separate, and the second contact point (44) along the surface (34) of the shield member (60) more closely to separate, thereby ensuring between signal contacts (40) with the corresponding ground shield member (60) while substantially not coupled between adjacent signal contact (40).

Claims:

1.电连接器组件(10，110)，包括绝缘机壳(12，112)，组装在其上的多个终端模件(30，130)和其间的导电屏蔽件(60，160)，各终端模件(30，130)有多个信号接点(40，140)，这些接点包括配合接点部(46，146)、导线连接部(52，152)和在它们之间的中间部分(50，150)，而所述中间部分中的至少一个是封装在绝缘腹板(54，154)之中，每个模件上还安装有导电的屏蔽件(60，160)，这种连接器组件(10，110)的特征在于，各终端模件(30，130)包括取交错构型的第一和第二接点(42，142；44，144)，此第一和第二接点(42，142；44，144)的中间部分(54，154)形成于沿之所选择的位置上，使得第一接点的中间部分(50，150)封装在与此模件(30，130)的第一主侧面(32，132)邻接的并与其

1. The electrical connector assembly (10, 110), comprising an insulating housing (12, 112), assembled on which a plurality of terminal modules (30, 130) and a conductive shield member therebetween (60, 160), each terminal modules (30, 130) has a plurality of signal contacts (40, 140), the contacts including a mating contact portion (46, 146), the wire connecting portion (52, 152) and in which the between the intermediate portion (50, 150), and said at least one intermediate portion is encapsulated in the insulating web (54, 154) respectively, each module is also equipped with a conductive shield member (60,160) such a connector assembly (10, 110) is characterized in

相对的第二主面(34，134)隔开的绝缘腹板(154)中，而第二接点(44，144)的中间部分(54，154)则封装在与模件(30，130)的第二主面(34，134)邻接且与其第一主面(32，132)相隔开的腹板中，由此，在把此终端模件(30，130)和其间的导电屏蔽件(60，160)组装到绝缘机壳(12，112)中时，第一接点(42，142)的中间部分(50，150)沿第一主面(32，132)与第一接地屏蔽件(60，160)隔开得相对于与第二接点(44，144)的中间部分(50，150)较近，而第二接点(44，144)的中间部分(50，150)则沿第二主面(34，134)与第二接地屏蔽件(60，160)隔开得相对于与第一接点(42，142)的中间部分(50，150)较近，由此能保证在各信号接点(42，142；44，144)和相应的接地屏蔽件(60，160)之间而不是和相邻的信号接点(44，144；42；142)的耦合。

2.权利要求1所述的连接器组件(110)，其中各终端模件(130)包括互补的半模件(131，133)，各个半模件(131，133)包括一批此第一和第二接点(142，144)中之一。

3.电连接器组件(110)，包括绝缘机壳(112)，组装在其上的多个终端模件(130)和在其间的导电屏蔽件(160)，各终端模件(130)有多个信号接点(140)，这些接点包括配合接点部(146)、导线连接部(152)和在它们之间的中间部分(150)，而所述中间部分(150)中的至少一个是封装在绝缘腹板(154)之中，每个模件上还安装有导电的屏蔽件(160)，这种连接器组件(110)的特征在于，各终端模件(130)包括互补的第一和第二半模件(131，133)以及第一和第二接点(142，144)的交错构型，此第一和第二接点(142，144)的中间部分(150)形成于沿之所选择的位置上，使得第一接点(142)的中间部分(150)封装于限定出此模件(130)的第一主侧面(132)的第一半模件(131)的绝缘腹板中，而第二接点(144)的中间部分(150)封装于限定出此模件(130)的第二主面(134)的第二半模件(133)的腹板中；这样当此第一与第二终端半模件(131，133)组合到一起，并将导电屏蔽件(160)放置在相邻的模件(130)之间，然后把它们插入绝缘机壳(112)中时，此第一接点(142)的中

that each terminal module (30,130) includes interleaving configurations may take first and second contacts (42, 142; 44, 144), the first and second contacts (42, 142; 44, 144) of the intermediate portion (54, 154) is formed at a position on the direction of the selected, such that the intermediate portion of the first contact (50, 150) encapsulated in this module (30 intermediate 34, 134) separated by an insulating web (154), and second contacts (44, 144), and 130) of the first main side (32, 132) and adjacent to the second main surface opposite thereto (portion (54, 154) is encapsulated in the mold member (30, 130) of the second main surface (34, 134) and adjacent to its first main surface (32, 132) spaced from the web, thereby, in the terminal when the module (30, 130) therebetween, and a conductive shield (60, 160) assembled to the insulating housing (12, 112), the first contacts (42, 142) of the intermediate portion (50, 150) along a first main surface (32, 132) and the first ground shield (60, 160) are spaced with respect to the second contacts (44, 144) of the intermediate portion (50, 150) is closer than the second contacts (44, 144) of the intermediate portion (50, 150) along the second major surface (34, 134) and the second ground shield (60, 160) are spaced relative to the first contacts (42,142) the intermediate portion (50, 150) closer, thereby can guarantee each signal contacts (42, 142; 44, 144) and between the respective ground shield member (60, 160) and not the adjacent signal contacts (42;; 142) coupling 44, 144.

2. The connector assembly (110) according to claim 1, wherein each of the terminal modules (130) include a complementary half-modules (131,133), each half-mold (131, 133) includes a number of the first and second contacts (142, 144) in one.

间部分(150)沿第一主面(132)与第一接地屏蔽件(160)隔开得相对于与第二接点(44，144)的中间部分(150)较近，而第二接点(144)的中间部分(150)沿第二主面(134)与第二接地屏蔽件(160)隔开得相对于与第一接点(142)的中间部分(150)较近，由此确保了在各信号接点(142，144)与相应接地屏蔽件(160)之间而不是与相邻信号接点(144，142)的耦合。

4.制造终端模件(130)的方法，此模件有多个按交错构型排列的第一和第二接点(142，144)，各接点(142，144)具有配合的接点部(146)、导线连接部(152)以及在其间的中间部分(150)，所述方法包括下述步骤：提供具有所述第一接点(142)的第一引线框(141a)；提供具有所述第二接点(144)的第二引线框(141b)；以绝缘材料模制上述第一引线框(141a)的中间接点部分(150)，使所述绝缘材料形成围绕此中间部分(150)的绝缘腹板(154)，以把此中间部分(150)精确和稳定地保持就位，同时限定出第一半模件(131)，而所述第一接点(142)的中间接点部分(150)则与此第一半模件的选定侧面相邻；将上述第一和第二半模件(131，133)紧固到一起而限定出所述终端模件(130)，以此第一和第二半模件的侧表面朝外来构成所述模件(130)的外侧面；和沿此终端模件(130)的一个外侧面设置接地屏蔽件(160)，确定出屏蔽的终端模件，而所述第一和第二半模件(131，133)之一的中间接点部分(150)则与此接地屏蔽件相邻。

3. The electrical connector assembly (110) comprising an insulating housing (112), a plurality of terminal modules assembled thereto (130) and the conductive shield therebetween (160), each terminal module (130) has a plurality of signal contacts (140), the contacts including a mating contact portion (146), (152) and an intermediate portion of the wire connecting portion between them (150), and the intermediate (150) in at least one part is encapsulated in the insulating web (154) respectively, each module is also equipped with a conductive shield member (160), the connector assembly (110) is characterized in that each terminal module (130) comprises first and second complementary half-modules (131,133) and first and second contacts (142,144) of the staggered configuration, the first and second contacts (142,144) the intermediate portion of the intermediate portion (150) formed at selected locations along the upper, so that the first contacts (142) (150) encapsulated in the module defining (130) a first main side (132) of a first half-modules (131) of the insulating web, and the second contacts (144) of the intermediate portion (150) defining a package in the module (130) a second main surface (134) of the second half-mold (133) of the webs; such that when said first and second terminal half-modules (131,133) are grouped together, and the conductive shield member (160) disposed between adjacent modules (130), and then inserting them into the insulating housing (112) when the first contacts (142) of the intermediate portion (150) along a first main surface (132) and the first ground shield (160) are spaced with respect to the second contacts (44, 144) of the intermediate portion (150) is closer than the second contacts (144) of the intermediate portion (150) along the second major surface (134) and the second ground shield (160) are spaced

relative to and the first contacts (142) of the intermediate portion (150) closer, thereby ensuring between signal contacts (142, 144) with the corresponding ground shield (160) rather than the adjacent signal contacts (144,142) coupling.

4. Manufacturing terminal module (130) of the method, a plurality of the modules are arranged in a staggered configuration of the first and second contacts (142,144), the contacts (142, 144) having a mating contact portion (146), the wire connecting portion (152) and the intermediate portion therebetween (150), said method comprising the steps of: providing a first lead having a first contact point (142) frame (141a); providing a second said contacts (144) of the second lead frame (141b); to said first insulating material molded lead frame (141a) contacts an intermediate portion (150), so that the insulating material this is formed around an intermediate portion (150) of the insulating web (154) to the intermediate portion of this (150) stably and accurately held in place, while defining a first mold half (131), and said first contact (142) contacts an intermediate portion (150) corresponding to this first mold half adjacent the side member selected; said first and second half-modules (131,133) fastened together and defining said terminal module (130), as a first member and a second mold half to form an outer side surface of the outward side of said module (130); and a ground shields disposed along an outer side surface of the terminal module (130) (160), to determine the shielded terminal module, and the intermediate portion of the contact (150) of said first and second half-modules (131,133), one of the ground shield adjacent to this.

Description:

带有屏蔽模件的连接器组件 及其制造方法

技术领域

本发明涉及电连接器组件，具有用来屏蔽数列相邻终端使其不受串音影响的屏蔽模件。

背景技术

电子工业中，一般采用直角的连接器用作两块印刷电路板之间或印刷电路板与导线之间的电连接。这种直角连接器通常有着大量的销接纳终端以及与其成直角的，同印刷电路板作电接触的销(例如柔性销)。另一印刷电路板上的接线柱或接线柱连接件则可以插入上述销接纳终端中在其间形成电连接。通过这些连接器的电信号传输频率是很高的，这不仅要求与电路板有匹配的阻抗和这些终端模件内的各个接点有平衡的电容，以减少信号的滞后与反射，还要求在各排的终端间进行屏蔽以减少串音。

终端接点的阻抗匹配问题业已在美国专利No.5066 236和No.5496183中论述到，其中还讨论了低成本和设计简单的直角连接器，这方面的模件设计虽便于生产较短或较长的连接器而不必对全新的连接器作重新设计与加工，但却只能生产出一种新的机壳部来把许多一致的终端模件装配于其内。正如专利No.5066236中所表明的，可以在相邻终端模件之间插入屏蔽件。以上两专利中所讨论的模件是这样制造的：按所选择的形状冲压出引线框，再用绝缘材料于选择的区域中模制到此引线框上，形成把接点保持于所需布置形式中的绝缘腹板。接点的形状和腹板片的厚度控制成能在模件的接点间提供阻抗匹配。这些接点在散热片之间分开成使它们离组装好的相邻屏蔽件等距离。

专利EP-A-0486298中公开的一种连接器中，具有呈交替图案的第一和第二接点。由于每个第二模件中的接点有较宽的中间部分，就能取得屏蔽效果。

发明内容

本发明的目的在于提供一种改进了的终端模件，它具有较大的阻抗控制，用于在高密度的连接器中载运高速信号。

Shielded modular connector assembly and manufacturing method

FIELD

The present invention relates to an electrical connector assembly having a shield for the number of columns of adjacent terminals from crosstalk effects it shielding modules.

BACKGROUND electronics industry, the general right angle connector as an electrical conductor or a printed circuit board and between two printed circuit board connection. Such right angle connector typically has a large number of pin receiving terminals and at right angles thereto, with a printed circuit board for electrical contact pins (e.g. flexpin). Another terminal or terminal connector printed circuit board can be inserted into the pin receiving terminal in electrical connection therebetween. These connectors are high frequency signal transmission, which requires not only the circuit board and a matching impedance of each contact within these terminal modules balanced capacitance to reduce the lag of the reflected signal, also requires each between rows of terminals shielded to reduce crosstalk. impedance matching terminal contacts have been discussed in U.S. Patent No.5066 236 and into No.5496183, which also discussed the cost and design simplicity of right angle connectors, in this regard, although modular design to facilitate shorter production or longer connectors without having to re-make the new connector design and processing, but it can only produce a new cabinet within the unit to the many identical terminal modules are assembled thereon. As indicated in the patent No.5066236, the shield can be inserted between adjacent terminal modules. Module two patents discussed above are thus produced: selected according to the shape of the

本发明的另一目的在于提供一种连接器，它在信号接点与相关的接地屏蔽件之间提高了耦合性，而在有源信号线之间降低了耦合性。

本发明的又一目的在于提供一种连续的屏蔽件，它在各列终端之间并基本上沿着接点的整个长度从配合界面延伸主板的界面，在接地电路与屏蔽件之间形成可靠和有效的电连接。

本发明的再一个目的在于提供有效和低成本的制造这种组件的方法。

通过提供一电连接器组件，达到本发明的一个目的电连接器组件包括绝缘机壳，组装在其上的多个终端模件和在其间的导电屏蔽件。各终端模件有多个接点，接点包括配合接点部、导线连接部和在它们之间的中间部分，而所述中间部中的至少一个是封装在绝缘腹板之中。每个模件上还安装有导电的屏蔽件，这种连接器组件的特征在于，各终端模件包括取交错构型的第一和第二接点，此第一和第二接点的中间部分形成于沿之所选择的位置上，使得第一接点的中间部分封装在与此模件的第一主侧面邻接的并与其相对的第二主面隔开的绝缘腹板中，而第二接点的中间部分则封装在与模件的第二主面邻接且与其第一主面相隔开的腹板中。在把此终端模件和其间的导电屏蔽件组装到绝缘机壳中时，第一接点的中间部分沿第一主面与第一接地屏蔽件隔开得相对于与第二接点的中间部分较近，而第二接点的中间部分则沿第二主面与第二接地屏蔽件隔开得相对于与第一接点的中间部分较近，由此能保证在各信号接点和相应的接地屏蔽件之间而不是和相邻的信号接点的基本耦合。

本发明的另一目的业已这样地实现：即通过使信号接点之间和周围的介电材料量减至最少，由此来减小信号接点的电容，因此就减小了信号接点之间的耦合以及噪音。

本发明的再一目的已在此终端模件的又一实施形式得以实现，其中各终端模件包括互补的第一和第二半模件以及第一和第二接点的交错构型。此第一和第二接点的中间部分形成于沿之所选择的位置上，使得

stamped lead frame, and then an insulating material on a selected area of the lead frame molded to this, the contact support is formed in a desired arrangement insulating web. Shape and thickness of the web contacts the sheet controlled to provide impedance matching between the contact module. The contacts between the fins to make them separate from the assembled adjacent shield equidistant.

A connector patent EP-A-0486298 disclosed having showed a pattern of alternating first and second contacts. Since each of the second contact module has a wide middle portion, the shielding effect can be achieved.

Summary object of the present invention to provide an improved terminal module, which has a large impedance control, used to carry high-speed signals in high-density connector.

It is another object of the present invention is to provide a connector, it is between the signal contacts ground shield associated with improved coupling, and between the active signal line reduces the coupling.

A further object of the

the present invention is to provide a continuous shield member, which contacts and substantially along the whole length of the circuit between the ground and the shield member extending from the mating interface board interface between columns terminals, a reliable and efficient electrical connection. is a further object of the present invention is to provide an effective and low-cost method of manufacturing such an assembly. by providing an electrical connector assembly, one objective of the present invention, an electrical connector assembly comprising an insulating housing, which is assembled on the

第一接点的中间部分封装于限定出此模件的第一主侧面的第一半模件的绝缘腹板中，而第二接点的中间部分封装于限定出此模件的第二主面的第二半模件的腹板中。第一与第二半模件组合到一起，并将导电屏蔽件的放置在相邻的终端模件之间。然后将这样形成的组件插入绝缘机壳中。此第一接点的中间部分沿第一主面与第一接地屏蔽件隔开得相对于与第二接点的中间部分较近，而第二接点的中间部分沿第二主面与第二接地屏蔽件隔开得相对于与第一接点的中间部分较近，由此确保了在各信号接点与相应接地屏蔽件之间而不是与相邻信号接点间的基本耦合。

本发明也提出制造终端模件的方法，此模件有多个按交错构型排列的第一和第二接点，各接点具有配合的接点部、导线连接部以及在其间的中间部分，所述方法包括下述步骤：提供具有所述第一接点的第一引线框；提供具有所述第二接点的第二引线框；以绝缘材料模制上述第一引线框的中间接点部分，使所述绝缘材料形成围绕此中间部分的绝缘腹板，以把此中间部分精确和稳定地保持就位，同时限定出第一半模件，而所述第一接点的中间接点部分则与此第一半模件的选定侧面相邻；将上述第一和第二半模件紧固到一起而限定出所述终端模件，以此第一和第二半模件的侧表面朝外来构成所述模件的外侧面；和沿此终端模件的一个外侧面设置接地屏蔽件，确定出屏蔽的终端模件，而所述第一和第二半模件之一的中间接点部分则与此接地屏蔽件相邻。

现在参看附图说明本发明的实施形式。

附图说明

图1是其中设有依据本发明制备的一批终端模件的连接器的一部分的透视图，此模件与屏蔽件组件是从机壳和匹配连接器的底板和一个片段部分分解出的；图2是终端模件中形成的接点在封装前的布置形式的透视图，其中为便于图示，除去了载承带；图3是图2中的接点封装后的终端模件的透视图，同时示明了接点的配合部；图4是从板安装部分所见的图3所示终端模件的透视图；图5是此终端模件沿平行于其斜支承结构的直线截取的剖面图，同时示

plurality of terminal modules and electrically conductive shields therebetween. Each terminal module has a plurality of contacts, the contacts including a mating contact portion, the wire connecting portion and an intermediate portion therebetween, the intermediate portion and said at least one insulating web being encapsulated. Also installed on each module has a conductive shield, characterized in that the connector assembly in that each terminal module taking interleaving configurations may include first and second contacts, the intermediate portions of the first and second contacts are formed in the direction of the selected position, the intermediate portion such that the first contact of the first package in this main side mold member adjacent thereto and a second main surface opposite the web of insulation spaced, and the second contact in the middle part of the package with the second main surface of the mold and its adjacent first main surface in spaced webs. When the assembly of the terminal module and the conductive shield therebetween to the insulating housing, a first intermediate portion along the first contact with the first main surface of the ground shield are spaced with respect to the middle portion of the second contact compared near, intermediate portions of the second contacts along the second major surface of the second ground shield member are spaced with respect to the intermediate portion of the first contacts close, thereby to ensure that in the corresponding signal contacts and ground shield and instead of coupling between adjacent signal and basic contact. is another object of the present invention has been implemented in such a manner: that is, through the signal amount between the contact and dielectric material surrounding minimized, thereby reducing the capacitance of the signal contacts, signal contacts and

明了接点在此模件中的位置；图6是本发明的插孔连接器的配合面的平面图；图7是连接器组件表面放大的局部图；图8是此插孔连接器经部分剖开的顶视平面图，同时示明了由配合连接器的互补接点的信号和接地接点配合部；图9是具有许多依本发明制备的终端模件的连接器另一实施形式一部分的透视图，此模件与屏蔽件组件是从机壳分解出的；图10是图9的连接器部分的透视图，其中模件是从连接器机壳分解出的；图11是图9中终端模件与接地平面组件的分解图，用于说明模件的制备方法；图12是图11中的接点在封装后的终端模件的透视图，且具有从其中分解出的接地屏蔽件同时示明了模件的板安装面；图13是图12的终端模件的板安装面的平面图，示明了沿此面上的两个半模件的交错情形；图14是组合好的图12中模件和接地屏蔽件的侧视平面图；图15是已屏蔽好的图14中模件的顶视平面图；图16是图9中插孔连接器的顶视平面图，经部分剖开，同时示明了由配合连接器的互补接点所配合的信号和接地接点的配合部。

具体实施方式

图1示出的连接器10具有机壳12和多个依据本发明制备的屏蔽的终端模件30。所示的连接器10是从电路板或底板74分解出的。机壳12包括配合面14、安装面16、装配面18、多个信号接点接纳通道26和从装配面18延伸到配合面14的多个接地接点接纳通道28。信号接点通道26包括在配合面14上的孔27，用来接纳配合连接器80的互补信号接点84。接地接点通道28包括在配合面14上的槽29，用以接纳配合连接器80的互补接地接点86，如图6和7所示。

配合连接器80包括机壳82，此机壳有许多信号接点84排列成与连接器10的信号接点阵列互补的交错阵列。机壳82还包括许多适合接纳在连接器10的接地接点62之间的接地片86。配合连接器80可安装到电路板(未示明)上，且属于美国专利No 4975 084中所公开的这种类型。

现在参看图2至4，每个终端模件30有相对的第一和第二主侧面32和34、引导或前端边缘36和板安装边缘38。模件30包括许多统一以40标明的接点，此接点包括第一和

therefore reducing the between the coupling and noise.

A further object of the present invention has been achieved in the form of yet another embodiment of the terminal module wherein each terminal module includes a first member and a second mold half and the first and second contacts of the complementary staggered configuration. This intermediate portions of the first and second contacts are formed in selected locations along the upper, middle portion such that the first contact on the package defines a first major side a first half mold insulating web in this module while the middle part of the second package contacts in defining a second main surface of this second mold half-modules of the webs. The first and second half-mold element assemblies together, and the conductive shield member is disposed between adjacent terminal modules. The assembly thus formed is then inserted into the insulating housing. The intermediate portion of this first contact the first main surface and along a first ground shield member are spaced with respect to the second intermediate portion closer contact, and an intermediate portion along the second main surface of the second contact point and the second ground shield member are spaced with respect to the intermediate portion of the first contacts close, thereby ensuring substantially the coupling between signal contacts and respective ground shield rather than between adjacent signal contacts.

The present invention also provides a method of manufacturing a terminal module, this module has a plurality of first and second contacts arranged in a staggered configuration, the contacts having a mating contact portion, the wire connecting portion and an intermediate portion therebetween, said method comprising the steps of: providing a first

第二实施形式42和44。每个接点40包括一其上具有接触面48的配合接触部46、板安装部52和在其间延伸的中间部分50。上述第一和第二接点实施形式42、44相互不同，使得中间部分50沿相对方向成形或弯曲，而把相应中间部分50置放于接近终端模件30的相对主侧面32、34中的一个，后面将对此更详细地说明。相应终端40的各中间部分50至少有某些是封装在一绝缘腹板54中，以一部分绝缘体56环绕相应的中间接点部50，如图3与4所清楚表明的。图3与4还表明了第一接点42的中间部分50较靠近第一主侧面32，而第二接点44则邻近第二主侧面34。图4中还示明了从模件30分解出的接地屏蔽件60。

终端模件30的结构便于其采用自动化的制造和装配过程。接点冲压成引线框构型，中间部分50形成为第一和第二接点42、44的交错阵列，然后将此引线框用腹板材料54模制。如这些实施形式所示，板连接部42是以焊引线的形式示明的，但也可采用柔顺销或其它的构型。

参看图3和4可以最清楚地理解所示模制腹板54的结构。腹板54包括许多薄塑料带56，它们基本上围住了对应的中间终端部分50的三个侧面。腹板54大致呈矩形，包括在板安装面附近的支座55以及沿其外表面的用于在图1所示连接器10的组件中固定到加强件70上的槽58。加强件70由卡子71固定在机壳12上并取与美国专利No.4952172中所示相同的类型。

在所示腹板条56中第一和第二接点42、44的相应中间部分50的位置可从图5的剖面图中最好地看清。第一接点42的中间部分50和第一主侧面隔开得较近，而第二接点44的中间部分50则同第二主侧面隔开得较近。

如图4和5所示，由于终端模件30的直角构型，中间接点部40具有不同的长度，而接点的长度不同意味着它们有不同的电容，而这是高速数据传输中所不希望的，其理由已较详细地说明了上面引述的专利中。模件30中于选择的位置处设有气袋以补偿接点的长度差。气袋用来减小相邻接点间的介电常数，并使中间接点部的电容相互匹配，这是出于前述专利中所述的相同理

lead frame having said first contacts; providing a second lead frame having said second contacts; intermediate portion contacts said first insulating material molded leadframe, said insulating material is formed around the intermediate portion of the insulating webs to the middle portion of the precision and stably held in position while the mold halves defining a first member, and said first contact portion of the contact is with this intermediate selected side surfaces of the adjacent first half-mold; to said first and second mold halves are fastened together to define said terminal module, as the first and second mold halves to the outwardly facing surface of the side member constituting an outer side surface of said module; and a grounded shield member disposed along an outer side surface of the terminal modules, determined shielded terminal module, and said first contact point and the intermediate portion of the second member of one of the mold halves this ground shield adjacent.

Referring now to the drawings illustrate embodiments of the present invention.

Brief Description of the

1 is a perspective view of a portion in which is provided a connector of the present invention is prepared by a number of terminal modules, this module and shield assembly exploded from the housing and the base plate, and a fragment of the mating connector portions out; FIG. 2 is a perspective view of the contact arrangement in the form of pre-packaged terminal modules formed, which for ease of illustration, remove the bearing carrier tape; Figure 3 is a terminal module in FIG. 2 contacts encapsulated perspective, and shows with the clear portion of the contact; Figure 4 is a perspective view of the terminal module installation Figure 3

由。结果，对于所选定的接点，使得沿此接点传送的信号延迟，从而实质上均衡了信号沿任何一个接点传输过模件的时间，应该指出，板连接部52都是在同一平面内，即使相应的中间部30和配合部46则并不处在同一平面中，这些配合部46如同相关的中间部分50，邻近模件30的同一主侧面。

现在参看图4，接地屏蔽件60基本上是一平面件，它所具有的接点配合部62包括：上面形成有接触面64的多个悬臂63、平面体部件66以及沿着其板安装边缘延伸的板安装段68。接地屏蔽件60的尺寸使其能设置在相邻的终端模件30之间，如图1所示。最好是用插入到绝缘腹板的槽57中的接头65将屏蔽件固定到各模件30之上。屏蔽件60如图4所示实质上覆盖模件30的一个主侧面的整个表面。

图6示明了配合面14而图7示明了连接器机壳12的装配面18，其中信号接点接纳通道26设在接地接点接纳通道28的对角线的相对端部处。图8示明了连接器机壳12的一个片段部分，其中配合连接器80的信号插销84同信号接点40的相应的接点配合部46配合，同时配合连接器80的各接地接头则与接地接点的接点配合部62配合。从这些图中可见，信号接点46同相关的接地屏蔽件60比同相应的信号接点40隔开得更近，即在终端模件30中与之相邻。信号接点40与相应的接地屏蔽件60的紧邻，保证了各个信号接点与相应的接地屏蔽件之间而不与相邻的信号接点之间的耦联，从而就减少了与串音和噪音有关的问题。

正如美国专利No.5066236和No.5496183中所公开的，图1中的终端模件30和接地屏蔽件60然后并排地装配到机壳模件12的背面，在此，销接纳端38用于接纳互补的插销终端，而连接终端52则是用于同印刷电路板上的通孔导电接触。在所示实施例中，信号接点的各终端52容纳于电路板74的通孔76中，而接地屏蔽件60的板安装段68则容纳于板74的通孔78中，如图1所示。

图9和10示明了另一个连接器的实施例110，它具有机壳112和许多依据本发明制备的屏蔽的终端模件130。机壳112包括配

seen from the plate portion; Figure 5 is the terminal module along a line parallel to its support structure, taken obliquely cross-sectional view, also shows clear this module in the contact position; FIG. 6 is a plan view of the mating face of the receptacle connector of the present invention; FIG. 7 is a surface of the connector assembly partially enlarged; Figure 8 is connected to this jack is partially cut-away top plan view, also shows clear by the complementary mating connector contact signal and ground contact mating portion; FIG. 9 is another embodiment having a number of terminal connector modules under this invention is prepared as part of a perspective, this module is the shield assembly from the chassis exploded out; FIG. 10 is a perspective view of the connector portion 9, wherein the module connector from the chassis exploded out; Fig. 11 is 9 exploded view of the terminal module and the ground plane assemblies for illustrate the preparation of the mold member; Fig. 12 in FIG. 11 is a perspective view of the package after the contact terminal modules, and has exploded out of the ground from which the shield at the same time It shows clear module mounting face plate; FIG. 13 is a plan view of a board mounting face of the terminal modules in Fig. 12, showing the two mold halves clear cross member along the surface of the case; FIG. 14 FIG. 12 is a good composition side plan view of the module and the ground shield member; Figure 15 is blocked in a top plan view of the module 14 good; Figure 16 is a top plan view of the receptacle connector of FIG. 9, partially broken away, also shows understood by the complementary mating connector contacts with the mating portion of the signal and ground contacts.

DETAILED DESCRIPTION

合面114、安装面116、一批信号接点接纳通道116和一批接地接点接纳通道128。机壳112基本上按前述机壳12的相同方式构造。为便于说明，连接器110有10排信号接点而连接器10有8排接点。连接器110与前述的连接器80类似，适合与互补的连接器配合。

现在参看图11-15，各个终端模件130分别包括互补的第一和第二半模件131、133。装配好的模件130具有相对的第一和第二主侧面132、134、引导或前端边缘136、板安装边缘138和由第一与第二组142、144组成的多个接点140。每个接点140包括其上有接触面142的配合接触部146、板安装部152和在其间延伸的中间部150。第一半模件131包括第一接点组142，第一半模件133包括第二接点组144。此第一和第二接点组142、144相互不同，使得第一组142的各中间部150成形或弯曲成在与第二组144的接点的中间部分150的相对方向上与板安装部152邻接。如这些图中所示，各组中的接点在组装起的模件130中是交错的。在所示实施例中，在组装后的连接器110内，第一接点组142包括一、三、五、七、九排中的接点，第二接点组144包括二、四、六、八、十排中的接点。各个弯曲段的位置选择成使得各中间部分150的大部分与终端模件130的相对主侧面132、134之一邻接，而在模件131装配好时，相应的板安装部152基本上是从板安装边缘136的中间延伸出，后面将对此作更详细的说明。各终端140的每个中间部分150的至少一部分封装于绝缘腹板154中，可从图11和12中清楚看到。图11和12还表明了，第一组接点142的中间部分150更靠近第一主侧面132，而第二组接点144的中间部分150则与第二主侧面134相邻。图12还示明了从模件130上分解出的接地屏蔽件160。

终端模件130的结构可使其适合自动化制造和装配方法。各组接点冲压成引线框构型141a，141b，而中间部分沿所选方向成形。然后各个引线框再用腹板材料54模制来形成半模件131或133中之一。如这些实施例中所示，板连接部152取得引线形式，但也可采用柔顺的部段或其它构型。

Figure 1 shows a connector 10 having a housing 12 and a plurality of the present invention prepared in accordance with shield terminal modules 30. Connector 10 is shown from the circuit board or backplane 74 decomposition of. Housing 12 includes a mating surface 14, the mounting surface 16, the mounting surface 18, a plurality of signal contact receiving passages 26 and 18 extending from the mounting surface to the mating surfaces of a plurality of ground contact 14 of the receiving channel 28. Signal contact 26 comprises a channel 14 in the mating face of the hole 27, 80 for receiving a complementary mating connector signal contacts 84. Channel 28 comprises a ground contact on a mating surface 14 of the groove 29 for receiving a complementary mating connector 80 contacts the ground 86, as shown in Figures 6 and 7. mating connector 80 includes a housing 82, which housing has a staggered array of a plurality of signal contacts 84 and the connector signal contacts arranged in array 10 is complementary. 82 further comprises a housing adapted to receive a number of ground contacts between the connector 62 of the ground plate 10 86. Mating connector 80 may be mounted to a circuit board (not shown) on, and fall into this category U.S. Patent No 4975 084 disclosed.

Referring now to Figures 2 through 4, each terminal module 30 has opposed first and second major side surfaces 32 and 34, or the front edge of the guide plate 36 and the mounting edge 38. Unity module 30 includes a plurality of contacts 40 indicated, this joint comprising first and second embodiments 42 and 44. Each contact 40 includes a mating contact portion 46 of the contact surface 48, mounting plate 52 and the intermediate portion therebetween extending portion 50 a thereon. Said first and second contact embodiments 42,44

参考图11和12可以最好地理解所示的这种模制的腹板154的结构。腹板154包括薄的基本上是实心的壁，限定了模件130的两个主侧面132、134之一。上述壁充分地环绕中间的终端部分150，将中间接点位置精确和稳定地保持于半模件之中。各个腹板154大致为矩形，以其各侧包括终端模件130对应边缘的一个/半个厚度。如图11和13所示，各个相应的板安装部152由腹板材料的“指形件”138a或138b所围绕。这些指形件138a、138b在半模件131、133组装成模件130时相互交错。从图11中可以清楚地看到，至少有一个半模件包括一对柱135，同时至少其中一个半模件包括一对用来将这两个半模件固定到一起的互补孔137。至少半模件的外表面还包括凹部和由此外延的凸部139，用来与屏蔽件160配合，下面将对此更全面地说明。

如上所述，终端模件130的直角状构型使得中间接触部分150具有不同的长度，结果导致接点具有不同的电容。为了调节相应接点的电容和补偿不同的长度，腹板154如图14所示，沿各个接点中间部分150的表面，设有许多穿过腹板的孔158。此外，为了使组合的模件130获得所需的电性质，半模件131、133在装配到一起时于其间形成一个气袋。应该指出，板连接部152处于同一平面中。即使相应的中间部分150和配合部146不处于同一平面中。

现在参看图14和15，接地屏蔽件160基本上是类似于前述屏蔽件60的平面件。屏蔽件160具有的接点配合部162包括许多在其上形成有接触面164的悬臂、平面体部件166和沿其板安装边缘延伸的许多板安装段168。接地屏蔽件160所取尺寸能使其如前所述置于相邻的终端模件130之间。在所示的这一实施例中，屏蔽件160包括一凹角部165，具有穿过它的孔167并适合固定到半模件131的柱139上。接地屏蔽件160可以固定到装配好的模件上，或者可在增加第二个半模件133而形成屏蔽的模件130前，将屏蔽件160装附到半模件131之上。图7是图6中的装配好的模件的顶视图，上面安装了接地屏蔽件160。然后如前所述，将终端模件130和接地屏蔽件160并排地组装到机壳模件112的背部上。

differ from each other in the form, so that the intermediate portion 50 formed or bent in opposite directions, and the corresponding intermediate portions 50 placed in proximity of the terminal module 30 of the opposite major sides 32, 34 of a, which will be described later in more detail. 40 corresponding to the intermediate portion of each terminal 50 is encapsulated in at least some of the one insulating web 54, the insulator 56 surrounds a portion of the respective intermediate contact portions 50, as shown in Figure 3 and 4 clearly shown. Figures 3 and 4 also show that the first contact 42 of the intermediate portion 50 closer to the first major side surface 32, and the second contact point 44 adjacent second major side surface 34. Also shown in Figure 4 from the apparent decomposition module 30 and ground shield 60.

The configuration of terminal module 30 facilitates its use of automated manufacturing and assembly processes. Contact lead frame punched into a configuration, the intermediate portion 50 is formed as a staggered array of the first and second contacts 42, 44, and this lead frame 54 is molded with the web material. As these forms of embodiment, the plate connecting portion 42 in the form of solder tails showing, but may also be compliant pins or other configurations.

Structure Referring to Figures 4 and 3 can be understood most clearly shown in the web 54 of the molding. Web 54 includes a plurality of thin plastic strip 56, which are substantially surrounded three sides of the corresponding intermediate terminal portion 50. Substantially rectangular webs 54, including the mounting plate 55 and the abutment surface close to the fixed along the outer surface of the component for the connector shown in FIG. 10 of the groove 70 in the reinforcing member 58. Stiffener

图16示明了连接器机壳112的一个局部，其中配合连接器180的信号插销184同信号接点140的相应接点配合部146配合，而配合连接器180的相应接地接头186则如连接器实施形式10一样同接地接点的接点配合部62配合。如这些图中所示，信号接点140的配合部146相对于一相关的接地屏蔽件160隔开得很接近，而且同在终端模件130中与之相邻的相应信号接点140相比，更紧密地与此屏蔽件160相关联。

70 and taking the same type as shown in US Patent No.4952172 fixed to the casing 12 by a clamp 71.

In the web strip 56 in the position shown in the middle portion 50 of the respective first and second contacts 42, 44 can best see from the sectional view of FIG. 5. The first contact point 50 and the intermediate portion 42 of the first main side spaced more closely, and the intermediate portion 44 of the second contact point 50 with the second major side surfaces are spaced more closely. as shown in Figure 4 and 5, since the terminal module 30 of rectangular configuration, the intermediate contact portion 40 having different lengths, and different lengths of the contacts mean that they have different capacitance, which is a high-speed data transmission undesirable, for the reasons described in detail than the above cited patents. Module 30 is provided at a position selected bag to compensate for the difference in length between the contacts. Bag for reducing the dielectric constant between adjacent contacts, and match the capacitance of the intermediate contact portion with each other, which is the same as that for the reasons described in the aforementioned patents. As a result, for the selected contacts, such that contact will be transmitted along the signal delay, thereby substantially equalized signal transmitted along any one of the contacts of the module over time, it should be noted that the board connecting portions 52 are in the same plane, even though the intermediate portion 30 and the corresponding mating portions 46 are not in the same plane as the mating portion 46 of the associated intermediate portion 50, adjacent the side modules 30 of the same master.

Referring now to Figure 4, ground shield 60 is a substantially planar member, the

contact having a mating portion 62 it comprises: a contact surface 64 formed thereon a plurality of cantilevers 63, and a planar member 66 along the plate mounting edge extending mounting portion 68. The size of the ground shield member 60 so that it can be set between adjacent terminal modules 30 as shown in FIG. Is preferably inserted into the groove 57 of the insulating web of the shield connector 65 is fixed to the top of each module 30. The shield member 60 shown in FIG. 4 substantially covers the entire surface of a mold 30 of the primary side.

Figure 6 shows apparent mating surfaces 14 and FIG. 7 shows apparent connector mounting surface 18 of the housing 12, wherein the signal contact receiving passages 26 provided in diagonal ground contact receiving passage 28 at opposite ends. Figure 8 shows a fragment of apparent connector portion 12 of the housing, wherein the mating connector 80 of the signal pin 84 contacts with the respective signal contacts 40 with mating portion 46, mating connector while each of the ground connector 80 and ground contact the contact with the mating portion 62. Seen, the signal contact 46 associated with the ground shield member 60 from these figures with the corresponding signal contacts 40 spaced closer than that in the adjacent terminal modules (30). Signal contacts 40 and the respective adjacent ground shield 60 to ensure that the contacts between the respective signals corresponding ground shield rather than between adjacent signal contacts are coupled, thereby reducing crosstalk and noise with related The problem.

As the U.S. Patent No.5066236 and No.5496183 disclosed in FIG. 1 terminal modules 30 and ground shield 60 and then fitted to the back of the chassis side module 12, in this, the pin receiving end

38 for receiving a complementary pin terminal, the terminal 52 is connected through holes for electrically conductive contact with the printed circuit board. In the illustrated embodiment, each terminal 52 of the signal contacts accommodated in the through hole 76 in the circuit board 74, and ground shield 60 of mounting portion 68 received in the through hole 78 in the plate 74, shown in Figure 1.

Figures 9 and 10 show another apparent connector embodiment 110 having a housing 112 and a number of preparation according to the present invention is shielded terminal modules 130. Housing 112 includes a mating surface 114 of the mounting surface 116, a group of signal contact receiving channel 116 and a number of ground contact receiving channel 128. Housing 112 substantially in the same manner of the aforementioned housing structure 12. For purposes of illustration, the connector 110 has 10 rows of signal contacts and connector 10 has eight rows of contacts. Connector 110 is similar to the aforementioned connector 80 for mating with a complementary connector.

Referring now to Figures 11-15, respectively, each terminal module 130 includes complementary first and second mold halves 131,133. The assembled module 130 having first and second opposed major sides 132, 134, or the front edge of the guide 136, mounting plate 138 and a plurality of edge contacts 140 by the first and second sets 142, 144 thereof. Each contact 140 includes a mating contact portion on which the contact surface 142 of 146, and the board mounting portion 152 in the intermediate portion 150 extending therebetween. The first mold half 131 includes a first set of contacts 142, 133. The first mold half 144 includes a second set of contacts. This set of first and second contacts 142,144 different from

each other, so that each intermediate portion of the first group of 142 to 150 formed or bent in the opposite direction of the intermediate 144 contact portion 150 and the second set of plate mounting portion 152 adjacent. As shown in these figures, each group of contacts in the module 130 is assembled from the interleaved. In the illustrated embodiment, in the assembled connector 110, the first contact group 142 includes one, three, five, seven, nine rows contact, second contact group 144 includes two, four, six, eight, ten rows of contacts. Position of each of the curved section selected such that the majority of the intermediate and terminal modules opposite sides of the main portion 150 of the abutment 130 of 132,134, while in the assembled module 131, the corresponding board mounting portions 152 is essentially from the intermediate plate mounting edge 136 extends, as will be later described in more detail. Each terminal 140 at least a portion of each intermediate portion 150 is encapsulated in an insulating web 154, best seen in FIG. 11 and 12. 11 and 12 also show, the first set of contacts 142 of the intermediate portion 150 closer to the first main side 132, and a second set of contacts 144 of intermediate portion 150 adjacent the second major side surface 134. 12 also shows a clear exploded from the ground shield 130 module 160. configuration of the terminal module 130 may make it suitable for automated manufacturing and assembly methods. Each set of contacts stamped into a leadframe configuration 141a, 141b, and the selected direction intermediate portion molded. Then each of the lead frame 54 and then the web material is molded to form one mold half 131 or 133. As shown in these embodiments, the plate connecting portions 152 made of leads, but may also be compliant sections or other configurations. with reference to FIG. 11 and 12 can be best

appreciated that the structure of the molded web 154 shown. The web 154 includes a thin substantially solid wall defining two major sides 132, 134 of the mold 130. Fully surround the middle of the wall of the terminal portion 150 contacts the intermediate position accurately and stably maintained in the mold halves into pieces. Each web 154 is substantially rectangular, each side of its terminal module 130 includes a corresponding one / half the thickness of the edge. 11 and 12, each respective plate mounting portion 152 by the web material "fingers" surrounded 138a or 138b 13. These fingers 138a, 138b in the mold halves 131,133 assembled into modules 130 intersect. It can be clearly seen from FIG. 11, at least one mold half 135 includes a pair of posts, while at least one of which includes a pair of mold halves for fixing the two mold halves together complementary hole 137. At least half of the outer surface of the mold member further comprises a concave portion and a convex portion 139 whereby the extension, to cooperate with the shield 160, as will now be explained more fully.

As described above, the terminal module 130 of the right angle configuration such that the intermediate contact portions 150 having different lengths, resulting in the contacts having different capacitances. In order to adjust the capacitance of the respective contacts and compensate for the different lengths, web 154 shown in Figure 14, along the surface of the intermediate portion 150 of each contact, provided with a plurality of holes 158 through the web. Further, in order to make the module 130 combined to achieve the desired electrical properties, the mold halves 131,133 when assembled together to form a bag therebetween. It should be noted, the plate connecting portions 152 in the same plane. Even mating portion 150

and intermediate portion 146 corresponding not in the same plane.

Referring now to Figures 14 and 15, ground shield 160 is substantially similar to the aforementioned flat member 60 of the shield member. Shield mating contacts 160 include portions 162 having a number of contact surfaces 164 of the cantilever, and a planar mounting member 166 extending along the edge of the board mounting portion 168 in a number of formed thereon. The ground shield 160 is sized to make it as described previously taken place between adjacent terminal modules 130. In the illustrated embodiment, the shield member 160 includes a recess 165 corner portion, having a hole 167 therethrough and adapted to be secured to the mold half 131 on the column 139. Ground shield 160 may be secured to the assembled module, or may be an increase in the second half mold 133 and the mold member 130 is formed before the shield, the shield member 160 to the attaching member 131 on the mold half. Fig. 7 is 6 assembled a top view of the module, installed above ground shield 160. Then as previously described, the terminal modules 130 and ground shields 160 are assembled side by side to the back 112 of the module housing.

Figure 16 shows apparent connector housing 112 of a partial, in which the contact mating portion corresponding mating connector signal pin 180 184 140 146 with signal contacts with, and the corresponding ground connector mating connector 186 of the connector 180 embodiment 10 is the same as the contact with the mating ground contact portion 62. As shown in these figures, the signal contacts 140 of the mating portion 146 with respect to an associated ground shields 160 spaced very close, but with the terminal module 130 adjacent the corresponding signal contact 140

compared to the more 160 closely associated with this shield.

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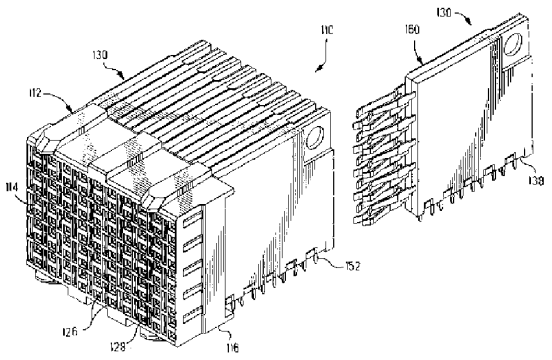
[54] 发明名称

带有屏蔽模件的连接器组件及其制造方法

[57] 摘要

电连接器组件(10)，它包括绝缘机壳(12)和装配到其上的多个终端组件(30)和在其间的导电屏蔽件(60)。各终端模件(30)包括呈交错构型的第一和第二接点(42，44)，它们的中间部分(50)形成在沿之所选择的位置上，沿此位置，使第一接点(42)的中间部分封装到绝缘腹板(54)中与此模件的第一侧面(32)邻近，且使第二接点(44)的中间部分密封到此腹板(54)中，与此模件的第二侧面(34)邻近。在组装好的连接器(10)中，第一接点(42)沿表面(32)与屏蔽件(60)分开得较近，而第二接点(44)沿表面(34)与屏蔽件(60)分开得较近，由此确保了在各信号接点(40)与相应接地屏蔽件(60)之间而不是与相邻信号接点(40)之间有基本耦合。



1.电连接器组件(10，110)，包括绝缘机壳(12，112)，组装在其上的多个终端模件(30，130)和其间的导电屏蔽件(60，160)，各终端模件(30，130)有多个信号接点(40，140)，这些接点包括配合接点部(46，146)、导线连接部(52，152)和在它们之间的中间部分(50，150)，而所述中间部分中的至少一个是封装在绝缘腹板(54，154)之中，每个模件上还安装有导电的屏蔽件(60，160)，这种连接器组件(10，110)的特征在于，各终端模件(30，130)包括取交错构型的第一和第二接点(42，142；44，144)，此第一和第二接点(42，142；44，144)的中间部分(54，154)形成于沿之所选择的位置上，使得第一接点的中间部分(50，150)封装在与此模件(30，130)的第一主侧面(32，132)邻接的并与其相对的第二主面(34，134)隔开的绝缘腹板(154)中，而第二接点(44，144)的中间部分(54，154)则封装在与模件(30，130)的第二主面(34，134)邻接且与其第一主面(32，132)相隔开的腹板中，由此，在把此终端模件(30，130)和其间的导电屏蔽件(60，160)组装到绝缘机壳(12，112)中时，第一接点(42，142)的中间部分(50，150)沿第一主面(32，132)与第一接地屏蔽件(60，160)隔开得相对于与第二接点(44，144)的中间部分(50，150)较近，而第二接点(44，144)的中间部分(50，150)则沿第二主面(34，134)与第二接地屏蔽件(60，160)隔开得相对于与第一接点(42，142)的中间部分(50，150)较近，由此能保证在各信号接点(42，142；44，144)和相应的接地屏蔽件(60，160)之间而不是和相邻的信号接点(44，144；42；142)的耦合。

2.权利要求1所述的连接器组件(110)，其中各终端模件(130)包括互补的半模件(131，133)，各个半模件(131，133)包括一批此第一和第二接点(142，144)中之一。

3.电连接器组件(110)，包括绝缘机壳(112)，组装在其上的多个终端模件(130)和在其间的导电屏蔽件(160)，各终端模件(130)有多个信号接点(140)，这些接点包括配合接点部(146)、导线连接部(152)和在它们之间的中间部分(150)，而所述中间部分(150)中的至少一个是封装在绝缘腹板(154)之中，每个模件上还安装有导电的屏蔽件(160)，这种连接器组件(110)的特征在于，各终端模件

(130)包括互补的第一和第二半模件(131，133)以及第一和第二接点(142，144)的交错构型，此第一和第二接点(142，144)的中间部分(150)形成于沿之所选择的位置上，使得第一接点(142)的中间部分(150)封装于限定出此模件(130)的第一主侧面(132)的第一半模件(131)的绝缘腹板中，而第二接点(144)的中间部分(150)封装于限定出此模件(130)的第二主面(134)的第二半模件(133)的腹板中；这样当此第一与第二终端半模件(131，133)组合到一起，并将导电屏蔽件(160)放置在相邻的模件(130)之间，然后把它们插入绝缘机壳(112)中时，此第一接点(142)的中间部分(150)沿第一主面(132)与第一接地屏蔽件(160)隔开得相对于与第二接点(44，144)的中间部分(150)较近，而第二接点(144)的中间部分(150)沿第二主面(134)与第二接地屏蔽件(160)隔开得相对于与第一接点(142)的中间部分(150)较近，由此确保了在各信号接点(142，144)与相应接地屏蔽件(160)之间而不是与相邻信号接点(144，142)的耦合。

4.制造终端模件(130)的方法，此模件有多个按交错构型排列的第一和第二接点(142，144)，各接点(142，144)具有配合的接点部(146)、导线连接部(152)以及在其间的中间部分(150)，所述方法包括下述步骤：

提供具有所述第一接点(142)的第一引线框(141a)；

提供具有所述第二接点(144)的第二引线框(141b)；

以绝缘材料模制上述第一引线框(141a)的中间接点部分(150)，使所述绝缘材料形成围绕此中间部分(150)的绝缘腹板(154)，以把此中间部分(150)精确和稳定地保持就位，同时限定出第一半模件(131)，而所述第一接点(142)的中间接点部分(150)则与此第一半模件的选定侧面相邻；

将上述第一和第二半模件(131，133)紧固到一起而限定出所述终端模件(130)，以此第一和第二半模件的侧表面朝外来构成所述模件(130)的外侧面；和

沿此终端模件(130)的一个外侧面设置接地屏蔽件(160)，确定出屏蔽的终端模件，而所述第一和第二半模件(131，133)之一的中间接点部分(150)则与此接地屏蔽件相邻。

带有屏蔽模件的连接器组件及其制造方法

技术领域

本发明涉及电连接器组件，具有用来屏蔽数列相邻终端使其不受串音影响的屏蔽模件。

背景技术

电子工业中，一般采用直角的连接器用作两块印刷电路板之间或印刷电路板与导线之间的电连接。这种直角连接器通常有着大量的销接纳终端以及与其成直角的，同印刷电路板作电接触的销(例如柔性销)。另一印刷电路板上的接线柱或接线柱连接件则可以插入上述销接纳终端中在其间形成电连接。通过这些连接器的电信号传输频率是很高的，这不仅要求与电路板有匹配的阻抗和这些终端模件内的各个接点有平衡的电容，以减少信号的滞后与反射，还要求在各排的终端间进行屏蔽以减少串音。

终端接点的阻抗匹配问题业已在美国专利No.5066 236和No.5496183中论述到，其中还讨论了低成本和设计简单的直角连接器，这方面的模件设计虽便于生产较短或较长的连接器而不必对全新的连接器作重新设计与加工，但却只能生产出一种新的机壳部来把许多一致的终端模件装配于其内。正如专利No.5066236中所表明的，可以在相邻终端模件之间插入屏蔽件。以上两专利中所讨论的模件是这样制造的：按所选择的形状冲压出引线框，再用绝缘材料于选择的区域中模制到此引线框上，形成把接点保持于所需布置形式中的绝缘腹板。接点的形状和腹板片的厚度控制成能在模件的接点间提供阻抗匹配。这些接点在散热片之间分开成使它们离组装好的相邻屏蔽件等距离。

专利EP-A-0486298中公开的一种连接器中，具有呈交替图案的第一和第二接点。由于每个第二模件中的接点有较宽的中间部分，就能取得屏蔽效果。

发明内容

本发明的目的在于提供一种改进了的终端模件，它具有较大的阻抗控制，用于在高密度的连接器中载运高速信号。

本发明的另一目的在于提供一种连接器，它在信号接点与相关的接

地屏蔽件之间提高了耦合性，而在有源信号线之间降低了耦合性。

本发明的又一目的在于提供一种连续的屏蔽件，它在各列终端之间并基本上沿着接点的整个长度从配合界面延伸主板的界面，在接地电路与屏蔽件之间形成可靠和有效的电连接。

本发明的再一个目的在于提供有效和低成本的制造这种组件的方法。

通过提供一电连接器组件，达到本发明的一个目的电连接器组件包括绝缘机壳，组装在其上的多个终端模件和在其间的导电屏蔽件。各终端模件有多个接点，接点包括配合接点部、导线连接部和在它们之间的中间部分，而所述中间部中的至少一个是封装在绝缘腹板之中。每个模件上还安装有导电的屏蔽件，这种连接器组件的特征在于，各终端模件包括取交错构型的第一和第二接点，此第一和第二接点的中间部分形成于沿之所选择的位置上，使得第一接点的中间部分封装在与此模件的第一主侧面邻接的并与其相对的第二主面隔开的绝缘腹板中，而第二接点的中间部分则封装在与模件的第二主面邻接且与其第一主面相隔开的腹板中。在把此终端模件和其间的导电屏蔽件组装到绝缘机壳中时，第一接点的中间部分沿第一主面与第一接地屏蔽件隔开得相对于与第二接点的中间部分较近，而第二接点的中间部分则沿第二主面与第二接地屏蔽件隔开得相对于与第一接点的中间部分较近，由此能保证在各信号接点和相应的接地屏蔽件之间而不是和相邻的信号接点的基本耦合。

本发明的另一目的业已这样地实现：即通过使信号接点之间和周围的介电材料量减至最少，由此来减小信号接点的电容，因此就减小了信号接点之间的耦合以及噪音。

本发明的再一目的已在此终端模件的又一实施形式得以实现，其中各终端模件包括互补的第一和第二半模件以及第一和第二接点的交错构型。此第一和第二接点的中间部分形成于沿之所选择的位置上，使得第一接点的中间部分封装于限定出此模件的第一主侧面的第一半模件的绝缘腹板中，而第二接点的中间部分封装于限定出此模件的第二主面的第二半模件的腹板中。第一与第二半模件组合到一起，并将导电屏蔽件的放置在相邻的终端模件之间。然后将这样形成的组件插入绝缘机壳中。此第一接点的中间部分沿第一主面与第一接地屏蔽件隔开得相对于与第二接点的中间部分较近，而第二接点的中间部分沿第二主面与第二接地

屏蔽件隔开得相对于与第一接点的中间部分较近，由此确保了在各信号接点与相应接地屏蔽件之间而不是与相邻信号接点间的基本耦合。

本发明也提出制造终端模件的方法，此模件有多个按交错构型排列的第一和第二接点，各接点具有配合的接点部、导线连接部以及在其间的中间部分，所述方法包括下述步骤：提供具有所述第一接点的第一引线框；提供具有所述第二接点的第二引线框；以绝缘材料模制上述第一引线框的中间接点部分，使所述绝缘材料形成围绕此中间部分的绝缘腹板，以把此中间部分精确和稳定地保持就位，同时限定出第一半模件，而所述第一接点的中间接点部分则与此第一半模件的选定侧面相邻；将上述第一和第二半模件紧固到一起而限定出所述终端模件，以此第一和第二半模件的侧表面朝外来构成所述模件的外侧面；和沿此终端模件的一个外侧面设置接地屏蔽件，确定出屏蔽的终端模件，而所述第一和第二半模件之一的中间接点部分则与此接地屏蔽件相邻。

现在参看附图说明本发明的实施形式。

附图说明

图1是其中设有依据本发明制备的一批终端模件的连接器的一部分的透视图，此模件与屏蔽件组件是从机壳和匹配连接器的底板和一个片段部分分解出的；

图2是终端模件中形成的接点在封装前的布置形式的透视图，其中为便于图示，除去了载承带；

图3是图2中的接点封装后的终端模件的透视图，同时示明了接点的配合部；

图4是从板安装部分所见的图3所示终端模件的透视图；

图5是此终端模件沿平行于其斜支承结构的直线截取的剖面图，同时示明了接点在此模件中的位置；

图6是本发明的插孔连接器的配合面的平面图；

图7是连接器组件表面放大的局部图；

图8是此插孔连接器经部分剖开的顶视平面图，同时示明了由配合连接器的互补接点的信号和接地接点配合部；

图9是具有许多依本发明制备的终端模件的连接器另一实施形式一部分的透视图，此模件与屏蔽件组件是从机壳分解出的；

图10是图9的连接器部分的透视图，其中模件是从连接器机壳分解

出的；

图11是图9中终端模件与接地平面组件的分解图，用于说明模件的制备方法；

图12是图11中的接点在封装后的终端模件的透视图，且具有从其中分解出的接地屏蔽件同时示明了模件的板安装面；

图13是图12的终端模件的板安装面的平面图，示明了沿此面上的两个半模件的交错情形；

图14是组合好的图12中模件和接地屏蔽件的侧视平面图；

图15是已屏蔽好的图14中模件的顶视平面图；

图16是图9中插孔连接器的顶视平面图，经部分剖开，同时示明了由配合连接器的互补接点所配合的信号和接地接点的配合部。

具体实施方式

图1示出的连接器10具有机壳12和多个依据本发明制备的屏蔽的终端模件30。所示的连接器10是从电路板或底板74分解出的。机壳12包括配合面14、安装面16、装配面18、多个信号接点接纳通道26和从装配面18延伸到配合面14的多个接地接点接纳通道28。信号接点通道26包括在配合面14上的孔27，用来接纳配合连接器80的互补信号接点84。接地接点通道28包括在配合面14上的槽29，用以接纳配合连接器80的互补接地接点86，如图6和7所示。

配合连接器80包括机壳82，此机壳有许多信号接点84排列成与连接器10的信号接点阵列互补的交错阵列。机壳82还包括许多适合接纳在连接器10的接地接点62之间的接地片86。配合连接器80可安装到电路板(未示明)上，且属于美国专利No 4975 084中所公开的这种类型。

现在参看图2至4，每个终端模件30有相对的第一和第二主侧面32和34、引导或前端边缘36和板安装边缘38。模件30包括许多统一以40标明的接点，此接点包括第一和第二实施形式42和44。每个接点40包括一其上具有接触面48的配合接触部46、板安装部52和在其间延伸的中间部分50。上述第一和第二接点实施形式42、44相互不同，使得中间部分50沿相对方向成形或弯曲，而把相应中间部分50置放于接近终端模件30的相对主侧面32、34中的一个，后面将对此更详细地说明。相应终端40的各中间部分50至少有某些是封装在一绝缘腹板54中，以一部分绝缘体56环绕相应的中间接点部50，如图3与4所清楚表明的。图3与4还表明了第一接点42的中间部分50较靠近第一主侧面32，而第二接点44则邻近第二主侧面34。图4中还示明了从模件30分解出的接地屏蔽件60。

终端模件30的结构便于其采用自动化的制造和装配过程。接点冲压成引线框构型，中间部分50形成为第一和第二接点42、44的交错阵列，然后将此引线框用腹板材料54模制。如这些实施形式所示，板连接部42是以焊引线的形式示明的，但也可采用柔顺销或其它的构型。

参看图3和4可以最清楚地理解所示模制腹板54的结构。腹板54包括许多薄塑料带56，它们基本上围住了对应的中间终端部分50的三个侧面。腹板54大致呈矩形，包括在板安装面附近的支座55以及沿其外表面的用于在图1所示连接器10的组件中固定到加强件70上的槽58。加强件70由卡子71固定在机壳12上并取与美国专利No.4952172中所示相同的类型。

在所示腹板条56中第一和第二接点42、44的相应中间部分50的位置可从图5的剖面图中最好地看清。第一接点42的中间部分50和第一主侧面隔开得较近，而第二接点44的中间部分50则同第二主侧面隔开得较近。

如图4和5所示，由于终端模件30的直角构型，中间接点部40具

有不同的长度，而接点的长度不同意味着它们有不同的电容，而这是高速数据传输中所不希望的，其理由已较详细地说明了上面引述的专利中。模件30中于选择的位置处设有气袋以补偿接点的长度差。气袋用来减小相邻接点间的介电常数，并使中间接点部的电容相互匹配，这是出于前述专利中所述的相同理由。结果，对于所选定的接点，使得沿此接点传送的信号延迟，从而实质上均衡了信号沿任何一个接点传输过模件的时间，应该指出，板连接部52都是在同一平面内，即使相应的中间部30和配合部46则并不处在同一平面中，这些配合部46如同相关的中间部分50，邻近模件30的同一主侧面。

现在参看图4，接地屏蔽件60基本上是一平面件，它所具有的接点配合部62包括：上面形成有接触面64的多个悬臂63、平面体部件66以及沿着其板安装边缘延伸的板安装段68。接地屏蔽件60的尺寸使其能设置在相邻的终端模件30之间，如图1所示。最好是用插入到绝缘腹板的槽57中的接头65将屏蔽件固定到各模件30之上。屏蔽件60如图4所示实质上覆盖模件30的一个主侧面的整个表面。

图6示明了配合面14而图7示明了连接器机壳12的装配面18，其中信号接点接纳通道26设在接地接点接纳通道28的对角线的相对端部处。图8示明了连接器机壳12的一个片段部分，其中配合连接器80的信号插销84同信号接点40的相应的接点配合部46配合，同时配合连接器80的各接地接头则与接地接点的接点配合部62配合。从这些图中可见，信号接点46同相关的接地屏蔽件60比同相应的信号接点40隔开得更近，即在终端模件30中与之相邻。信号接点40与相应的接地屏蔽件60的紧邻，保证了各个信号接点与相应的接地屏蔽件之间而不与相邻的信号接点之间的耦联，从而就减少了与串音和噪音有关的问题。

正如美国专利No.5066236和No.5496183中所公开的，图1中的终端模件30和接地屏蔽件60然后并排地装配到机壳模件12的背面，在此，销接纳端38用于接纳互补的插销终端，而连接终端52则是用于同印刷电路板上的通孔导电接触。在所示实施例中，信号接点的各终端52容纳于电路板74的通孔76中，而接地屏蔽件60的板安装段68则容纳于板74的通孔78中，如图1所示。

图9和10示明了另一个连接器的实施例110，它具有机壳112和

许多依据本发明制备的屏蔽的终端模件130。机壳112包括配合面114、安装面116、一批信号接点接纳通道116和一批接地接点接纳通道128。机壳112基本上按前述机壳12的相同方式构造。为便于说明，连接器110有10排信号接点而连接器10有8排接点。连接器110与前述的连接器80类似，适合与互补的连接器配合。

现在参看图11-15，各个终端模件130分别包括互补的第一和第二半模件131、133。装配好的模件130具有相对的第一和第二主侧面132、134、引导或前端边缘136、板安装边缘138和由第一与第二组142、144组成的多个接点140。每个接点140包括其上有接触面142的配合接触部146、板安装部152和在其间延伸的中间部150。第一半模件131包括第一接点组142，第一半模件133包括第二接点组144。此第一和第二接点组142、144相互不同，使得第一组142的各中间部150成形或弯曲成在与第二组144的接点的中间部分150的相对方向上与板安装部152邻接。如这些图中所示，各组中的接点在组装起的模件130中是交错的。在所示实施例中，在组装后的连接器110内，第一接点组142包括一、三、五、七、九排中的接点，第二接点组144包括二、四、六、八、十排中的接点。各个弯曲段的位置选择成使得各中间部分150的大部分与终端模件130的相对主侧面132、134之一邻接，而在模件131装配好时，相应的板安装部152基本上是从板安装边缘136的中间延伸出，后面将对此作更详细的说明。各终端140的每个中间部分150的至少一部分封装于绝缘腹板154中，可从图11和12中清楚看到。图11和12还表明了，第一组接点142的中间部分150更靠近第一主侧面132，而第二组接点144的中间部分150则与第二主侧面134相邻。图12还示明了从模件130上分解出的接地屏蔽件160。

终端模件130的结构可使其适合自动化制造和装配方法。各组接点冲压成引线框构型141a，141b，而中间部分沿所选方向成形。然后各个引线框再用腹板材料54模制来形成半模件131或133中之一。如这些实施例中所示，板连接部152取得引线形式，但也可采用柔顺的部段或其它构型。

参考图11和12可以最好地理解所示的这种模制的腹板154的结构。腹板154包括薄的基本上是实心的壁，限定了模件130的两个主侧面132、134之一。上述壁充分地环绕中间的终端部分150，将中间接点

位置精确和稳定地保持于半模件之中。各个腹板154大致为矩形，以其各侧包括终端模件130对应边缘的一个/半个厚度。如图11和13所示，各个相应的板安装部152由腹板材料的“指形件”138a或138b所围绕。这些指形件138a、138b在半模件131、133组装成模件130时相互交错。从图11中可以清楚地看到，至少有一个半模件包括一对柱135，同时至少其中一个半模件包括一对用来将这两个半模件固定到一起的互补孔137。至少半模件的外表面还包括凹部和由此外延的凸部139，用来与屏蔽件160配合，下面将对此更全面地说明。

如上所述，终端模件130的直角状构型使得中间接触部分150具有不同的长度，结果导致接点具有不同的电容。为了调节相应接点的电容和补偿不同的长度，腹板154如图14所示，沿各个接点中间部分150的表面，设有许多穿过腹板的孔158。此外，为了使组合的模件130获得所需的电性质，半模件131、133在装配到一起时于其间形成一个气袋。应该指出，板连接部152处于同一平面中。即使相应的中间部分150和配合部146不处于同一平面中。

现在参看图14和15，接地屏蔽件160基本上是类似于前述屏蔽件60的平面件。屏蔽件160具有的接点配合部162包括许多在其上形成有接触面164的悬臂、平面体部件166和沿其板安装边缘延伸的许多板安装段168。接地屏蔽件160所取尺寸能使其如前所述置于相邻的终端模件130之间。在所示的这一实施例中，屏蔽件160包括一凹角部165，具有穿过它的孔167并适合固定到半模件131的柱139上。接地屏蔽件160可以固定到装配好的模件上，或者可在增加第二个半模件133而形成屏蔽的模件130前，将屏蔽件160装附到半模件131之上。图7是图6中的装配好的模件的顶视图，上面安装了接地屏蔽件160。然后如前所述，将终端模件130和接地屏蔽件160并排地组装到机壳模件112的背部上。

图16示明了连接器机壳112的一个局部，其中配合连接器180的信号插销184同信号接点140的相应接点配合部146配合，而配合连接器180的相应接地接头186则如连接器实施形式10一样同接地接点的接点配合部62配合。如这些图中所示，信号接点140的配合部146相对于一相关的接地屏蔽件160隔开得很接近，而且同在终端模件130中与之相邻的相应信号接点140相比，更紧密地与此屏蔽件160相关联。

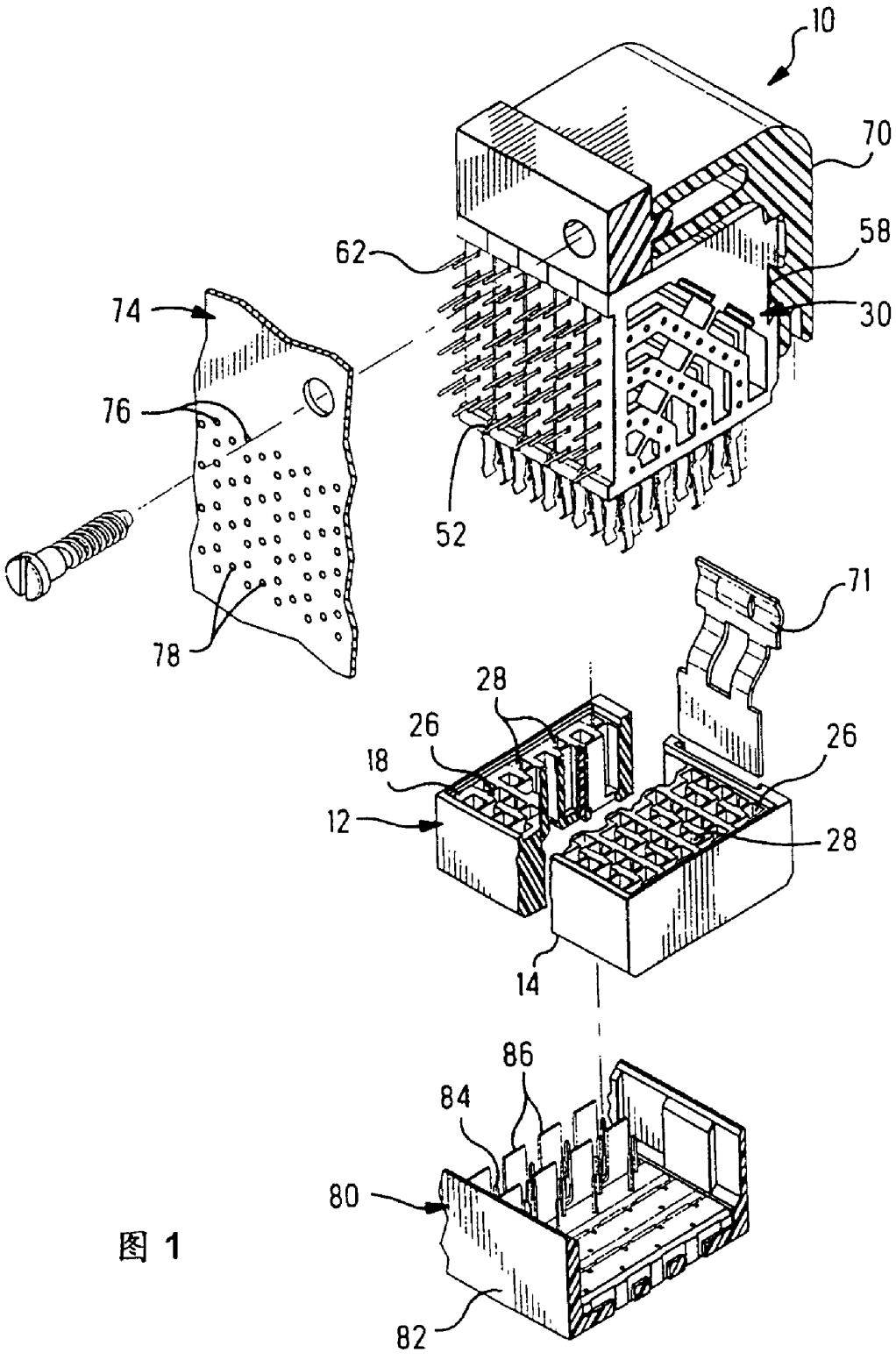


图 1

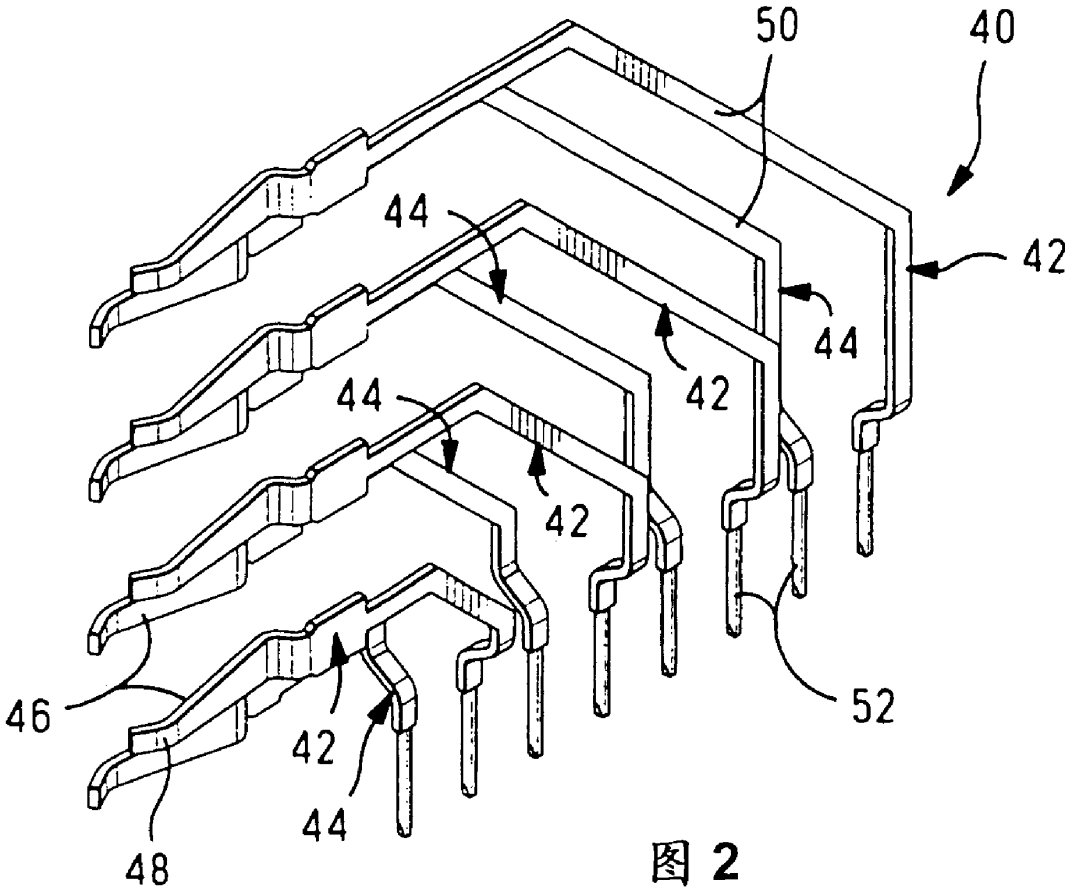


图 2

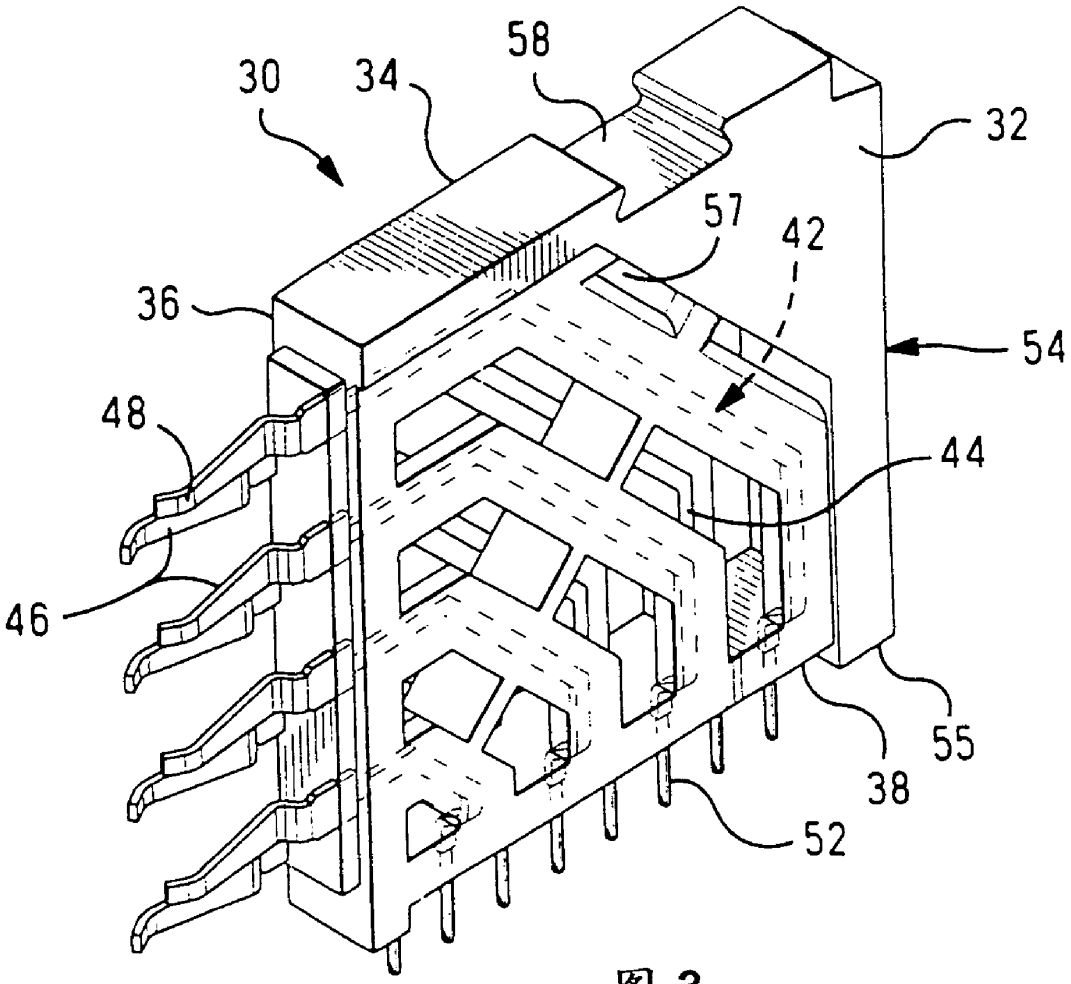


图 3

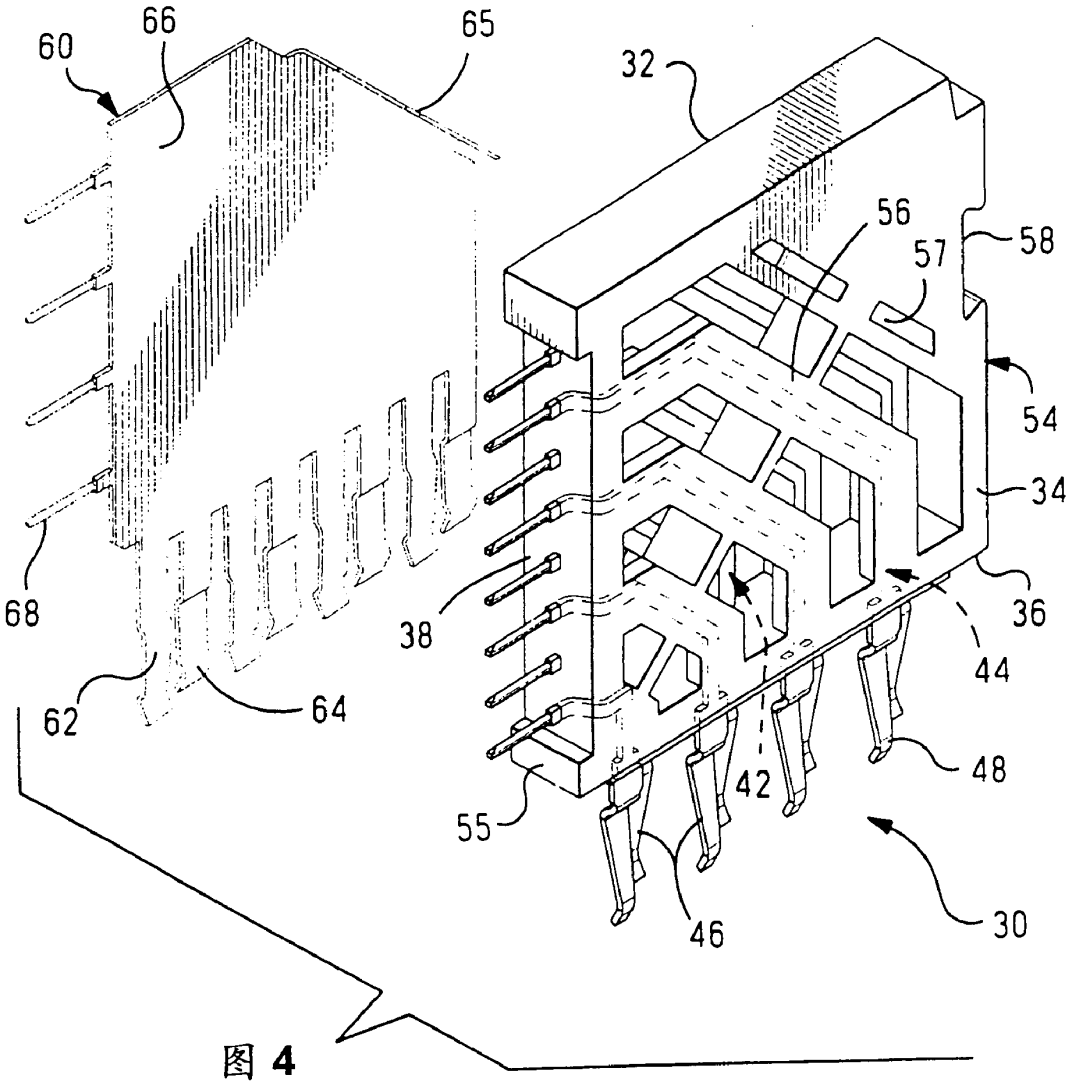


图 4

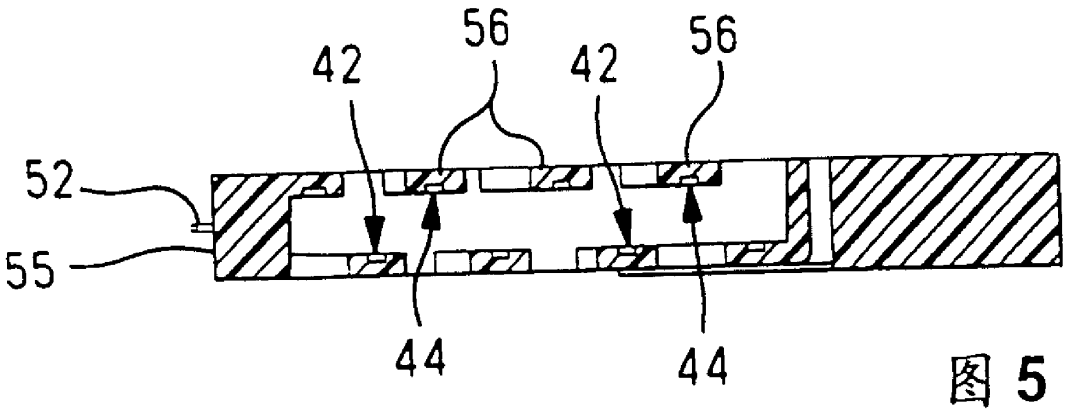


图 5

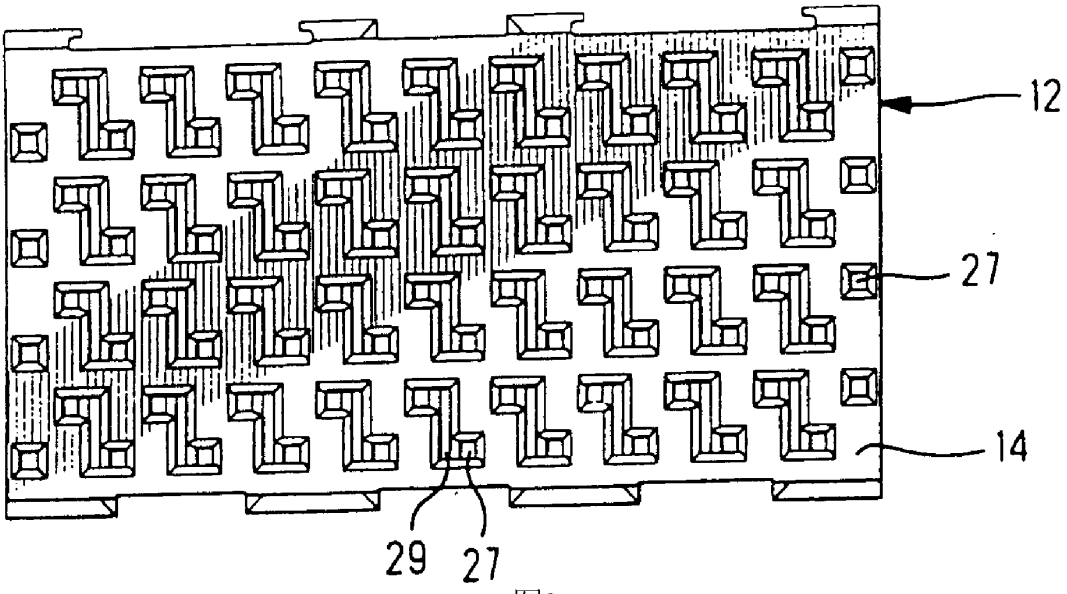


图6

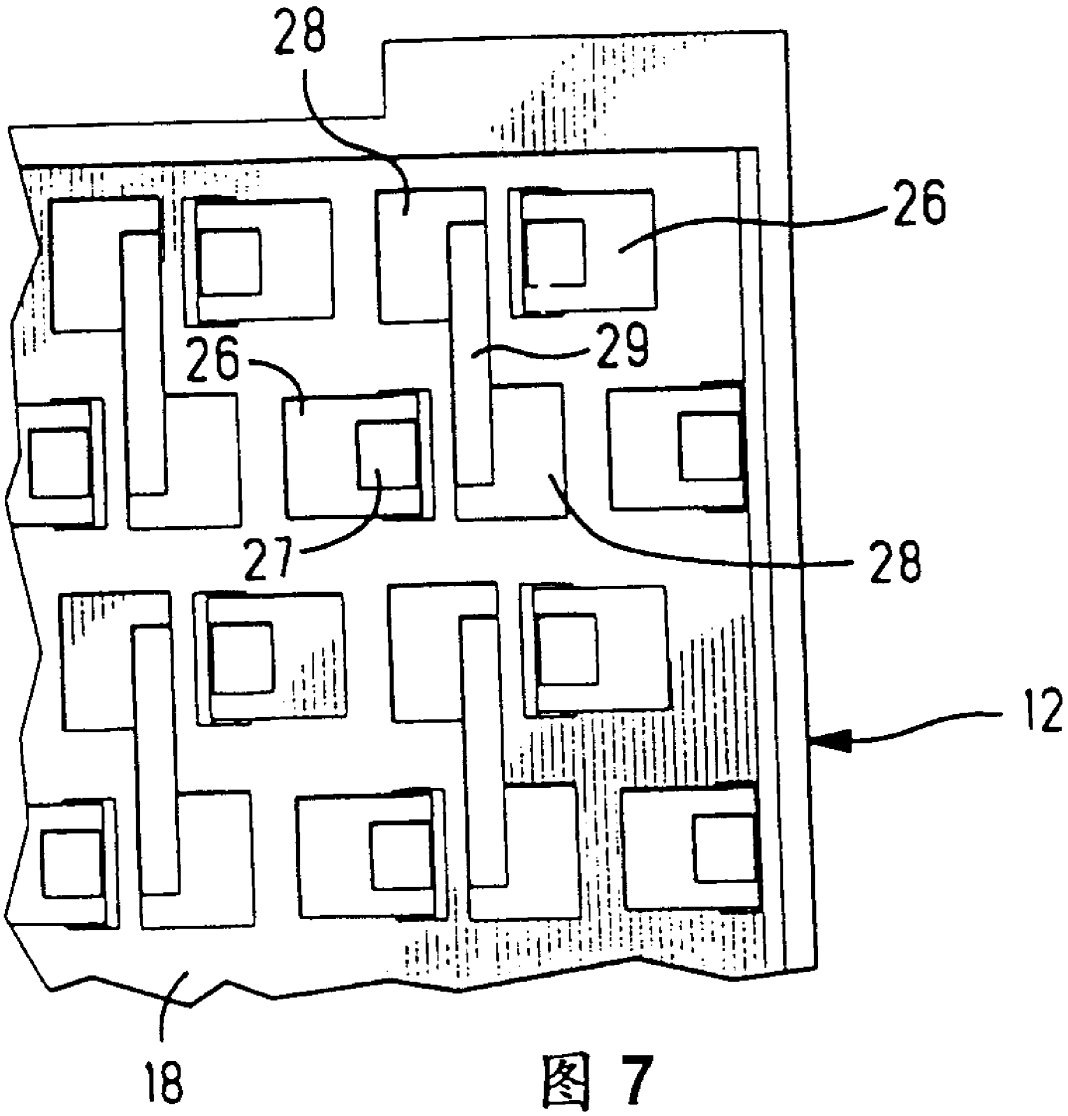


图 7

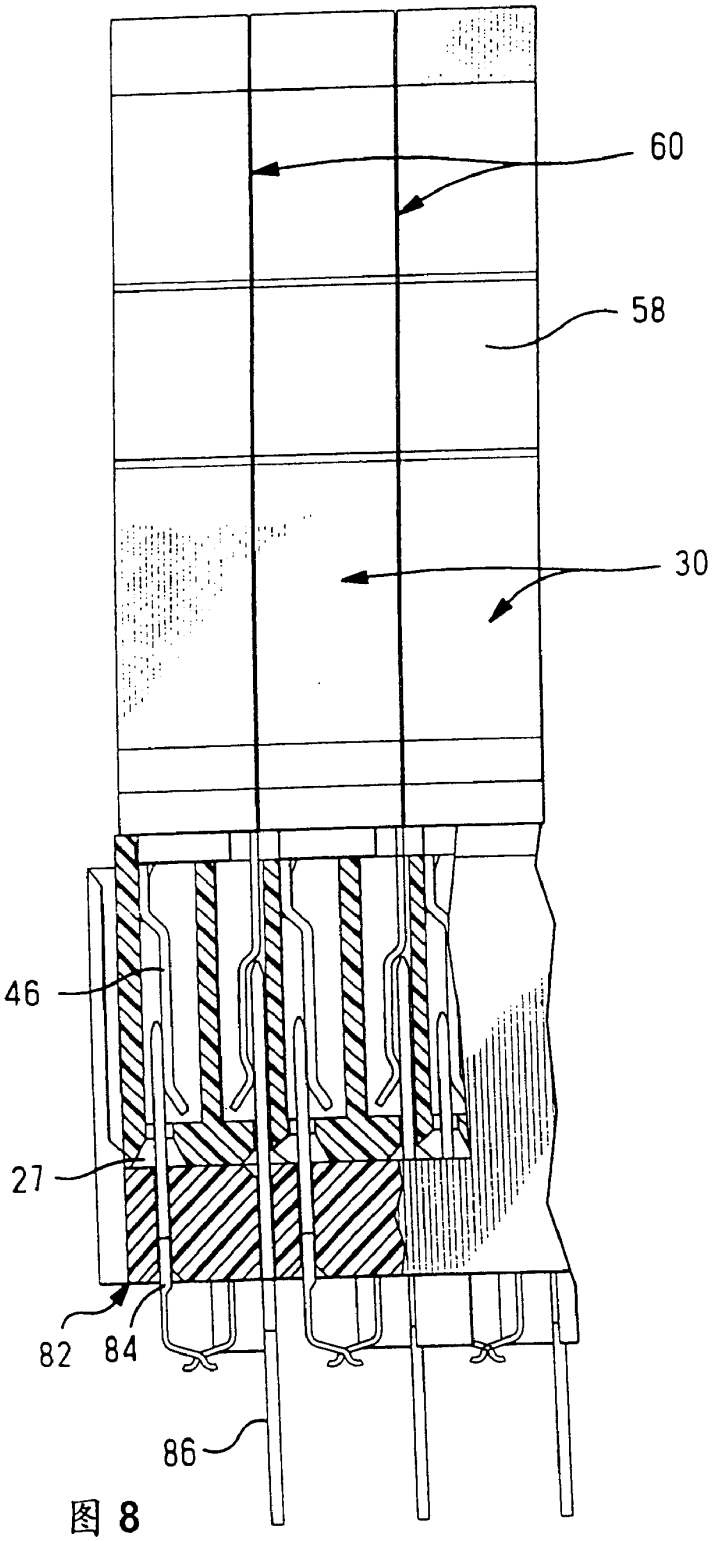


图 8

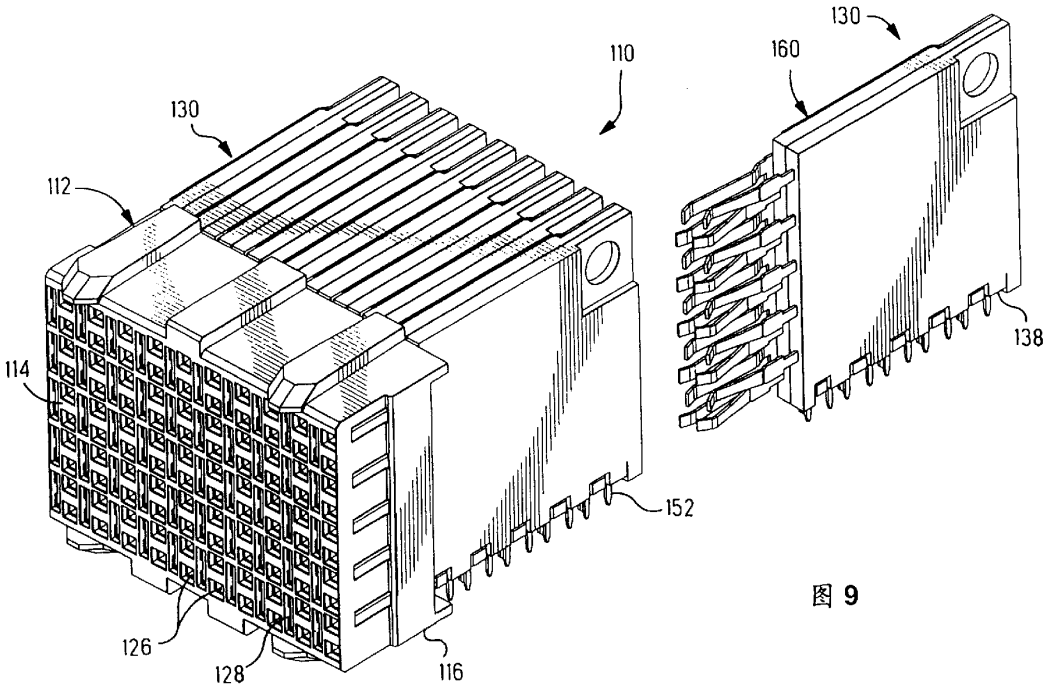
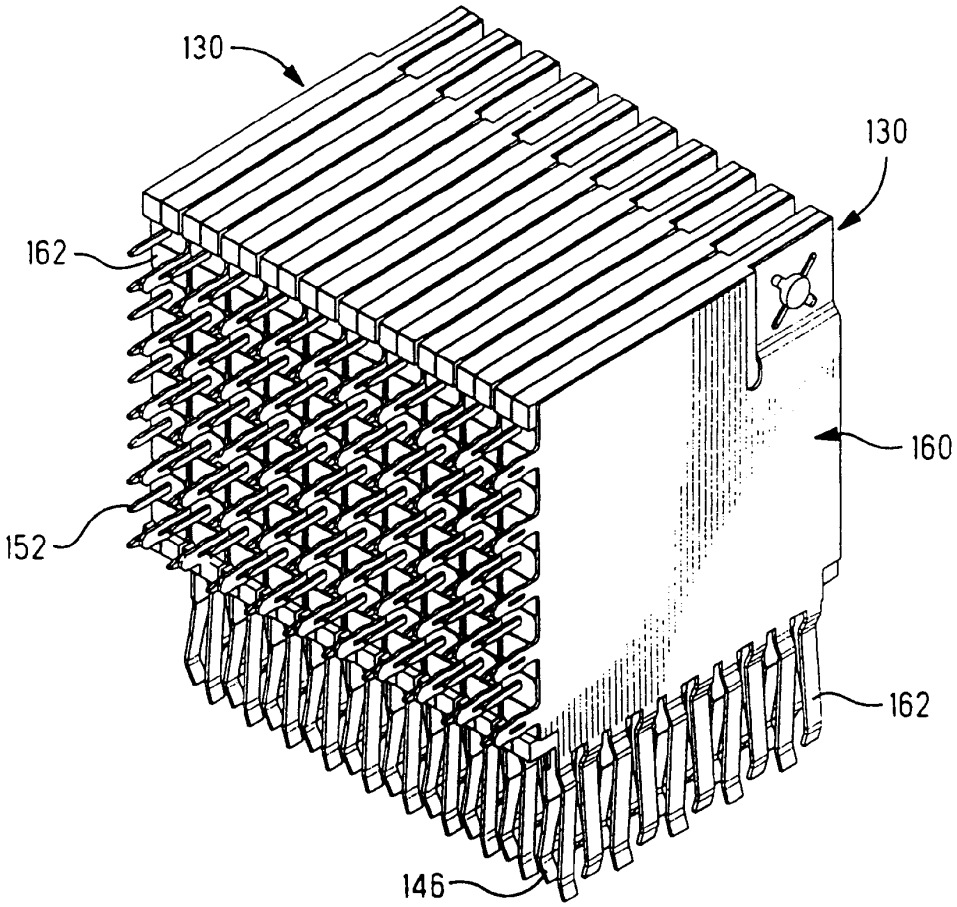


图 9



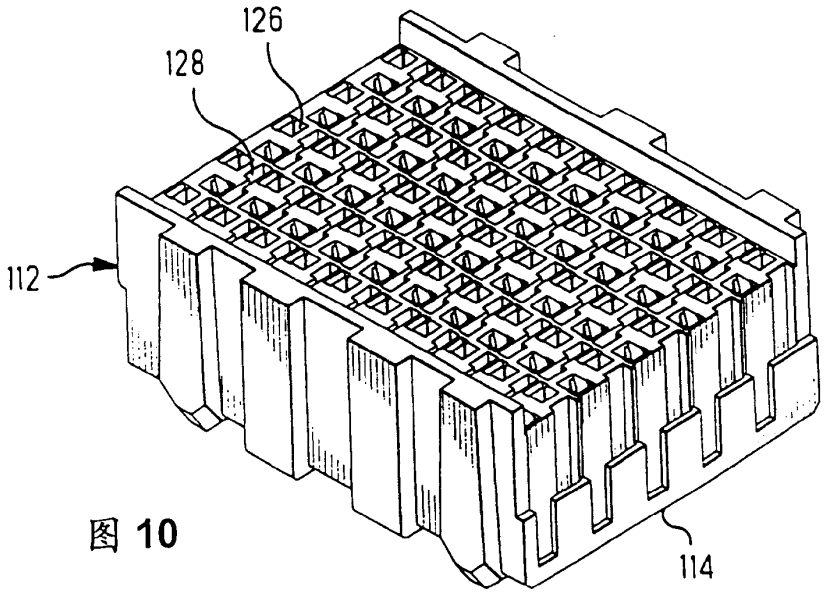


图 10

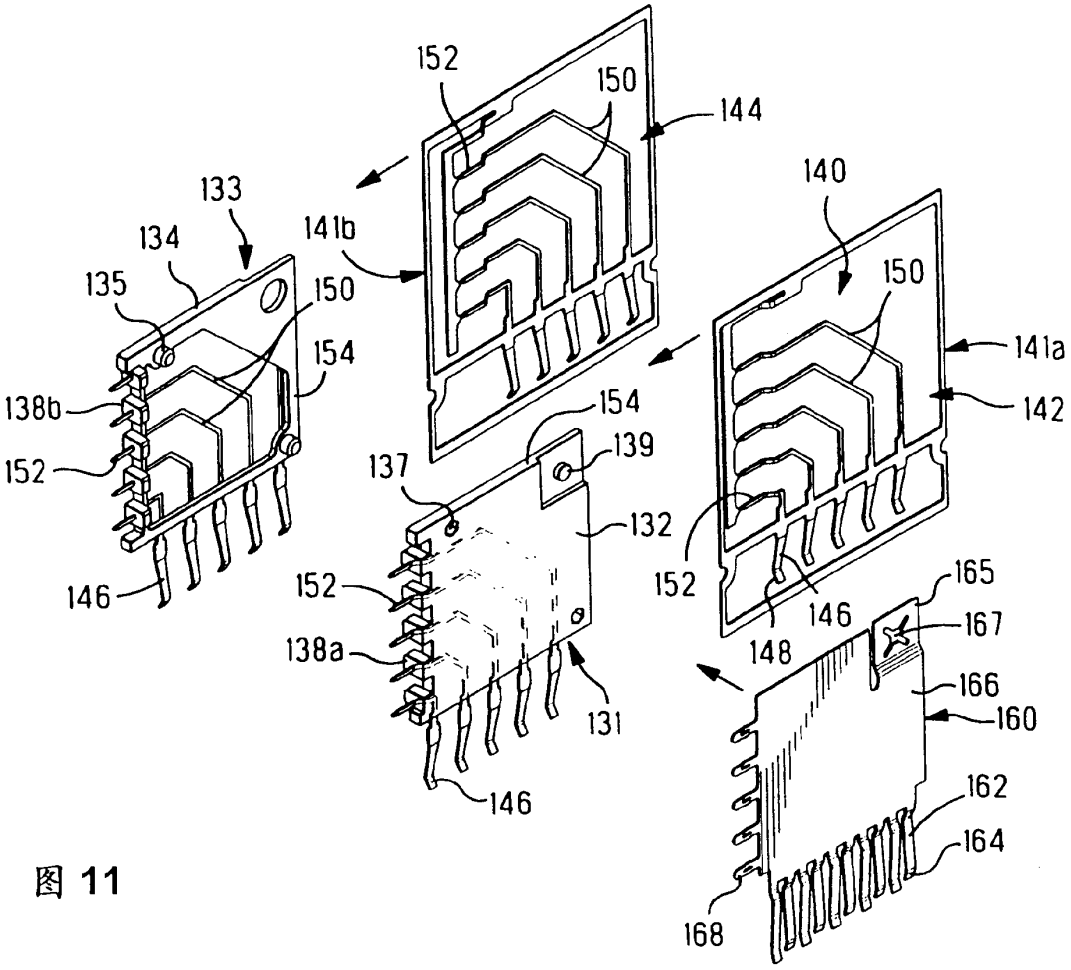


图 11

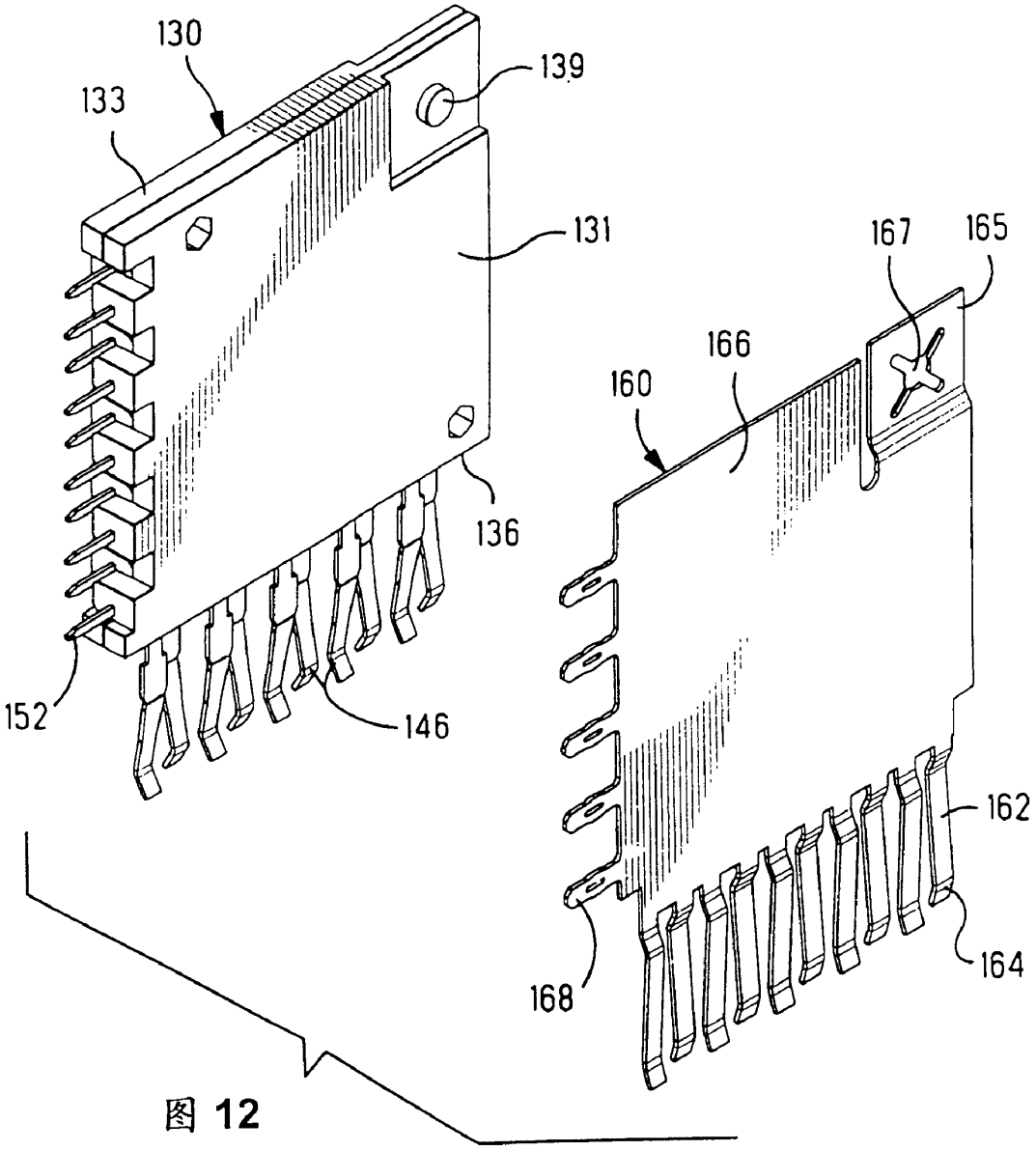


图 12

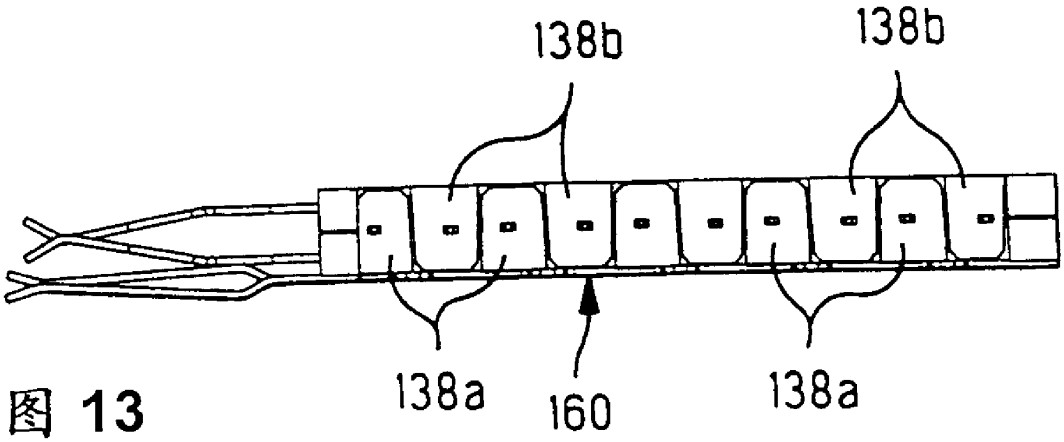


图 13

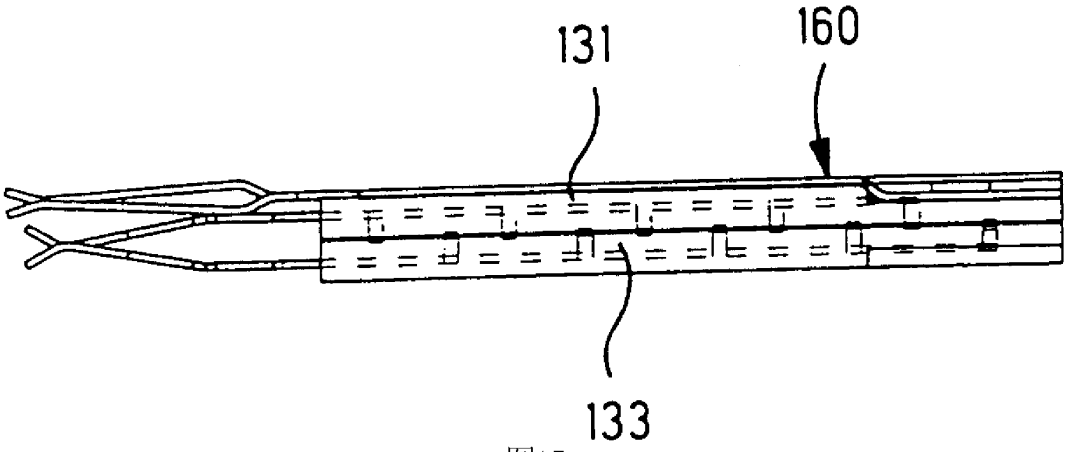


图15

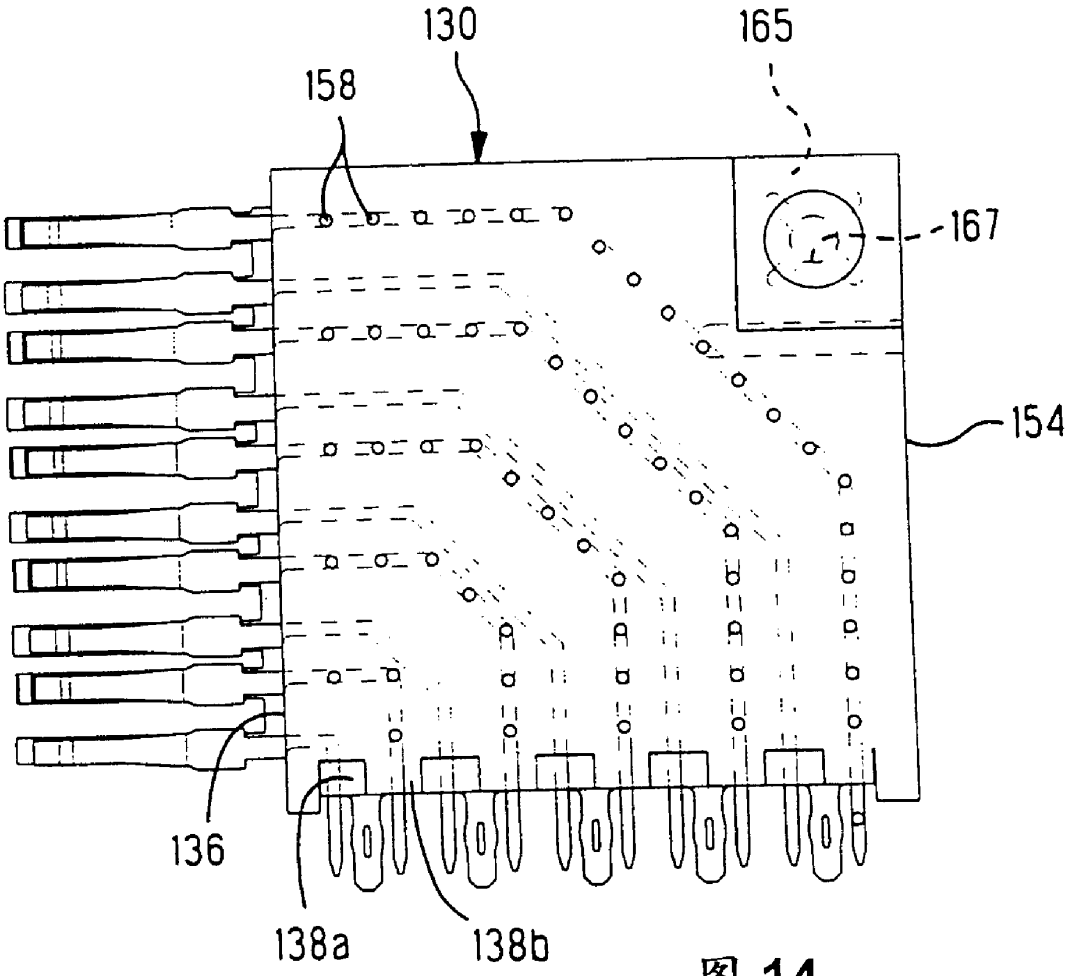


图 14

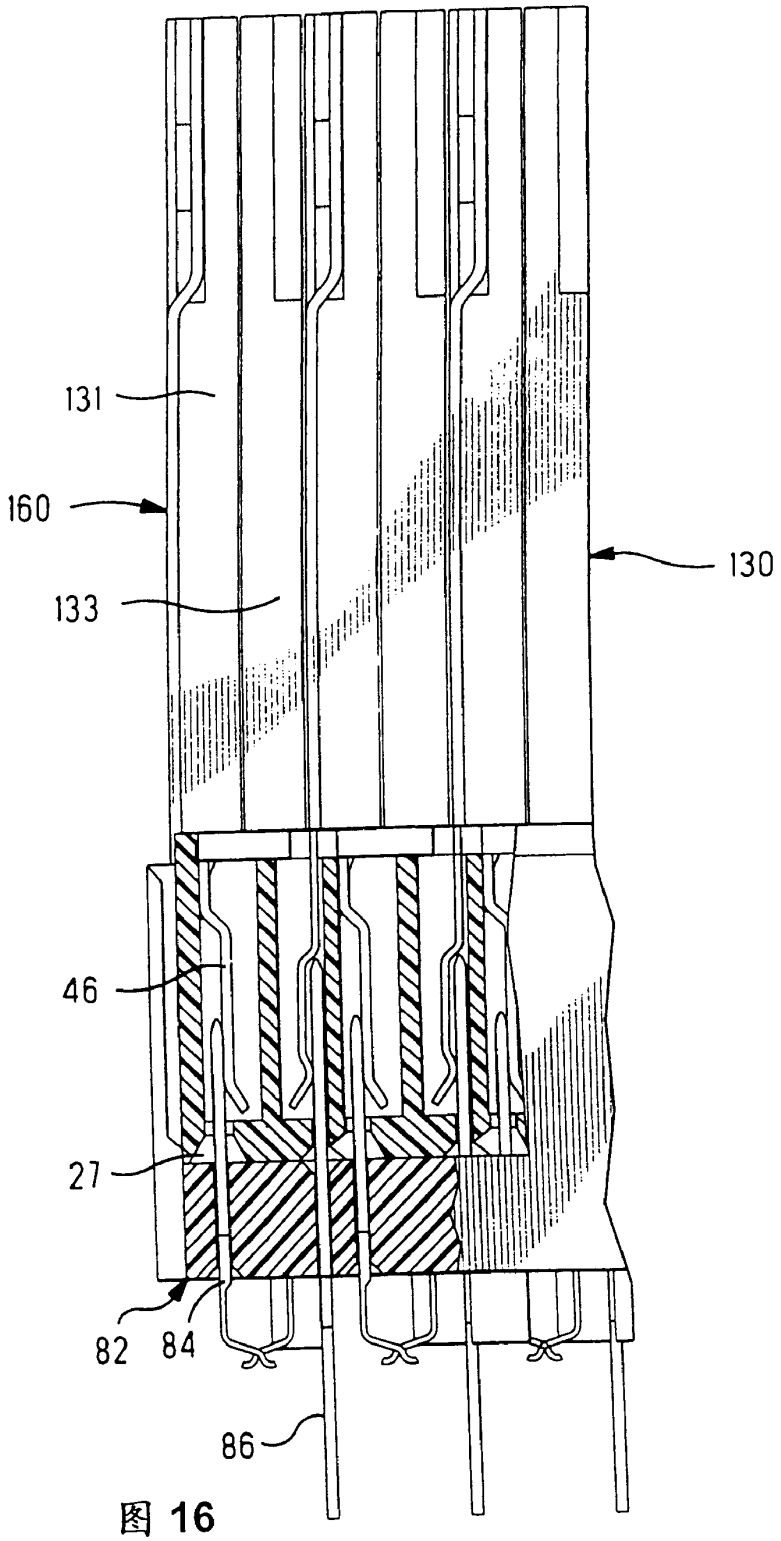


图 16

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Cooperative Patent class: H05K1/0222 ; H01P3/06 ; H05K1/024 ; H05K1/0251 ; H05K3/429 ; H05K2201/0187 ; H05K2201/09063 ; H05K2201/09536 ; H05K2201/09618 ; H05K2201/09718 ; H05K2201/09809 ;

Family members: CN1799290 A JP2004107830 A1 JP4652230 B1 JP4652230 B2 US2006255876 AA US2009091406 AA US7463122 BB US7750765 BB WO04107830 A1

Title: Compact via transmission line for printed circuit board and its designing method

Title: 印刷电路板用小型转接传输线路及其设计方法

Abstract:

一种印刷电路板用小型转接传输线路及其设计方法，包括：形成小型转接传输线路的内侧导体边界并构成转接孔的中心导体(101)；设置在中心导体的周围形成外侧导体边界的多个接地转接孔(102)；以及由印刷电路板的导体层构成的接地板。并且，在所述内侧导体边界与所述外侧导体边界之间设置结构参数调整用转接孔(103)，在信号转接孔中传播的信号与其他信号在高频信号频带被电性隔离不会产生交扰。实现了具有好的特性阻抗且包含多层印刷电路板的小型化的同时，还能扩大安装在该

A printed circuit board with a compact design and a transmission line switching method, comprising: forming a compact adapter inner conductor of the transmission line and the boundary of the central conductor constituting the via holes (101); a central conductor disposed around the outside of the boundary forming conductor a plurality of ground via holes (102); and a printed circuit board by a conductor layer composed of a ground plate. Further, the boundary

印刷电路板上的转接孔传输线路的频率范围。

between the inner conductor and the outer conductor boundaries set by structural adjustment parameters via holes (103), a signal with other signals in the signal propagation via holes in the high-frequency signal band is not electrically isolated It will produce crosstalk. It achieved both good characteristic impedance and including miniaturized multilayer printed circuit board, via holes but also expand the frequency range of the transmission line mounted on the printed circuit board.

Claims:

1. 一种印刷电路板用小型转接传输线路，其设置在印刷电路板上， 5 包括： 构成所述小型转接传输线路的内侧导体边界，传递信号的中心导体； 构成所述小型转接传输线路的外侧导体边界的多个接地转接孔； 由连接在所述接地转接孔上的所述印刷电路板的导体层构成的接地 板；以及 10 设置在所述内侧导体边界与所述外侧导体边界之间，用于调整所述印 刷电路板的结构参数的结构参数调整用转接孔， 所述结构参数调整用转接孔，由具有与构成所述印刷电路板的绝缘层 的第1结构参数不同的第二结构参数的一样的介质或复合介质填充。

1 A printed circuit board with a small adapter transmission line disposed on a printed circuit board 5 comprising: forming the inner boundary of the small conductor transmission line switching, transmission signal center conductor; the plurality of ground via hole constituting the outer boundary of the small conductor transmission line switching; on the ground by the connection of the via holes of the printed circuit board of a conductor layer ground plate; and 10 provided in the boundary between said inner conductor and said outer conductor boundary, structural parameter for adjusting the structural parameters of the printed circuit board with via holes adjustment, adjusting the structural parameters via holes, having constituting the printing like medium or filling medium the composite structure parameters of the first circuit board a second insulating layer different structural parameters.

2.根据权利要求1所述的印刷电路板用小型转接传输线路，其中： 15 所述印刷电路板是具有多个导体层的多层印刷电路板。

2 according to the printed circuit board 1 with a small transmission line adapter as claimed in claim wherein: the printed circuit board 15 having a plurality of conductor layers of a multilayer printed circuit board.

3.根据权利要求1所述的印刷电路板用小型转接传输线路，其中： 所述第1和第2结构参数是介电常数和相对导磁率中的至少任意一 个。

3 according to one of the printed circuit board using a small adapter transmission line claim, wherein: the first and the

4.根据权利要求1所述的印刷电路板用小型转接传输线路，其中： 20 所述小型转接传输线路，与安装在所述印刷电路板上并连接在所述小 型转接传输线路上的内部连接电路取得阻抗匹配。

5.根据权利要求3所述的印刷电路板用小型转接传输线路，其中： 所述第2结构参数的值比所述第1结构参数的值小。

6. —种印刷电路板用小型转接传输线路，其设置在印刷电路板上， 25 包括： 构成所述小型转接传输线路的内侧导体边界，传递信号的中心导体； 构成所述小型转接传输线路的外侧导体边界的多个接地转接孔； 由连接在所述接地转接孔上的所述印刷电路板的导体层构成的接地 板； 30 设置在所述内侧导体边界与所述外侧导体边界之间，用于调整所述印 刷电路板的结构参数的结构参数调整用转接孔；以及 在所述内侧导体边界与所述外侧导体边界之间穿过所述印刷电路板 而设置的空气孔。

7.根据权利要求6所述的印刷电路板用小型转接传输线路，其中： 5 所述空气孔，设置在所述印刷电路板上，从而调整设置在所述印刷电 路板上的转接传输线路与连接在该转接传输线路上的内部连接电路之间的特性阻抗。

8.根据权利要求6所述的印刷电路板用小型转接传输线路，其中： 所述空气孔,至少包含由2个不同大小的圆形形状构成的所述空气孔。

10 9.根据权利要求6所述的印刷电路板用小型转接传输线路，其中： 所述空气孔，不规则地配置在所述内侧导体边界与所述外侧导体边界 之间。

10.根据权利要求6所述的印刷电路板用小型转接传输线路，其中： 所述空气孔，相对于所述信号转接孔配置为对称。

15 11.根据权利要求6所述的印刷电路板用小型转接传输线路，其中： 所述空气孔的截面形状的最大长度，是在所述印刷电路板的绝缘层中 传播的信号的给定频率范围的最小波长的1/8以下。

12.根据权利要求1～11中的任意一项所述的印刷电路板用小型转接 传输线路，其中： 20 所述接地转接孔排列在圆周上。

13.根据权利要求1～11中的任意一项所述的印刷电路板用小型转接 传输线路，其中： 所述接地转接孔排列在正方形上。

14.根据权利要求7所述的印刷电路板用小型转接传输线路，其中： 25 在所述印刷

second parameter is the structure and relative dielectric constant of permeability optionally at least one.

.

4 according to claim 1, wherein the printed circuit board with a small adapter transmission line, wherein: said compact switching transmission line 20, and mounted on the printed circuit board and compact adapter connected to said transmission line connected to an internal impedance matching circuitry.

5 3 according to the printed circuit board with a small transmission line adapter as claimed in claim wherein: said second value smaller than the value of structural parameter of the first structural parameters.

.

6 - type printed circuit board with a small adapter transmission line disposed on a printed circuit board 25 comprising: forming the inner boundary of the small conductor transmission line switching, transmission signal the center conductor; constituting the plurality of ground conductor via holes outer boundary compact switching transmission line; ground plate connected to the ground by a via hole of the printed circuit board of a conductor layer; settings 30 the boundary between the inner conductor and the outer conductor boundary, structural parameters for adjusting the structural parameters of the printed circuit board with via holes adjustment; and the boundary between the inner conductor and the outer conductor boundary air passing through the holes provided in the printed circuit board.

7 according to the printed circuit board 6 with a small transmission line adapter as claimed in claim wherein: the air holes 5 is provided on the printed circuit board, in

电路板上传播的主要电磁波的电场和磁场相对于传播方 向，是垂直方向，并且电场与磁场彼此正交。

15. —种印刷电路板用小型转接传输线路，其设置在印刷电路板上， 包括： 构成小型转接传输线路的2个内侧导体边界，传播差动信号的2个中 30 心导体；构成分别配置在2个中心导体的周围的2个外侧导体边界的多个接地 转接孔； 由连接在所述接地转接孔上的所述印刷电路板的导体层构成的接地 板；以及 5 设置在所述2个内侧导体边界与所述2个外侧导体边界之间，用于调 整所述印刷电路板的结构参数的2个结构参数调整用转接孔， 所述2个结构参数调整用转接孔，分别由具有与构成所述印刷电路板 的绝缘层的第1结构参数不同的第二结构参数的一样的介质或复合介质填 充。

10 16. 一种印刷电路板用小型转接传输线路的设计方法，该印刷电路板 用小型转接传输线路包括：构成设置在印刷电路板上的所述小型转接传输 线路的内侧导体边界、传递信号的中心导体；构成所述小型转接传输线路 的外侧导体边界的多个接地转接孔；以及由连接在所述接地转接孔上的所 述印刷电路板的导体层构成的接地板，其中： 15 在所述内侧导体边界与所述外侧导体边界之间设置用于调整所述印刷电路板的结构参数的结构参数调整用转接孔，所述结构参数调整用转接 孔，分别由具有与构成所述印刷电路板的绝缘层的第1结构参数不同的第 二结构参数的一样的介质或复合介质填充。

17.根据权利要求16所述的印刷电路板用小型转接传输线路的设计 20 方法，其中•• 所述第二结构参数比所述第一结构参数小。

18.根据权利要求16所述的印刷电路板用小型转接传输线路的设计 方法，其中.• 所述第1和第2结构参数是介电常数和相对导磁率中的至少任意一 25 个。

19.根据权利要求16所述的印刷电路板用小型转接传输线路的设计 方法，其中： 所述小型转接传输线路，与安装在所述印

order to adjust the settings the transfer of the transmission line and the printed circuit board is connected to the internal transfer characteristic impedance transmission line connections between circuits.

Said air hole, comprising at least the shape of a circular two different sizes consisting of:

8 claimed by a small adapter transmission line, according to claim 6, wherein the printed circuit board said air hole.

10 9. According to the printed circuit board 6 with a small transmission line adapter of claim wherein: the air holes, arranged irregularly in the boundary and the inner conductor the boundary between the outer conductor.

.

10 according to claim 6, wherein the printed circuit board with a small adapter transmission line, wherein: said air hole, with respect to the signal via hole configured symmetrically.

15 11. According to the printed circuit board 6 with a small transmission line adapter of claim wherein: the maximum length of the cross-sectional shape of the air holes, in the printed circuit board given the frequency range of the minimum wavelength of the signal propagating in the insulating layer of 1/8 or less.

.

12 1~11 according to any of claims adapter printed circuit board with a small transmission line, wherein: the ground via holes 20 are arranged on the circumference.

刷电路板上并连接在所述小 型转接传输线路上的内部连接电路取得阻抗匹配。

30 20. 一种印刷电路板用小型转接传输线路的设计方法，该印刷电路板 用小型转接传输线路包括：构成设置在印刷电路板上的所述小型转接传输 线路的内侧导体边界、传递信号的中心导体；构成所述小型转接传输线路 的外侧导体边界的多个接地转接孔；以及由连接在所述接地转接孔上的所 述印刷电路板的导体层构成的接地板，其中.• 5 在所述内侧导体边界与所述外侧导体边界之间设置用于调整所述印 刷电路板的结构参数的结构参数调整用转接孔，在所述内侧导体边界与所 述外侧导体边界之间还形成穿过所述印刷电路板的空气孔。

21.根据权利要求20所述的印刷电路板用小型转接传输线路的设计 方法，其中：10 所述空气孔，设置在所述印刷电路板上，从而调整设置在所述印刷电 路板上的转接传输线路与连接在该转接传输线路上的内部连接电路之间 的特性阻抗。

22.根据权利要求21所述的印刷电路板用小型转接传输线路的设计 方法，其中：15 在所述印刷电路板上传播的主要电磁波的电场和磁场对于传播方向， 是垂直方向，并且电场与磁场彼此正交。

23.根据权利要求20所述的印刷电路板用小型转接传输线路的设计 方法，其中：所述空气孔的截面形状的最大长度，是在所述印刷电路扳的绝缘层中 20 传播的信号的给定频率范围的最小波长的1/8以下。

13 1~11 according to any one of the printed circuit board with a small transmission line adapter as claimed in claim wherein: said ground via holes are arranged in the square.

14 7 according to the printed circuit board using a small adapter transmission line claim, wherein: the main electric and magnetic fields of electromagnetic waves in the printed circuit board 25 with respect to the spread of propagation direction, vertical direction, and electric and magnetic fields perpendicular to each other.

.

15 - type printed circuit board with a small transmission line adapter, the printed circuit board, which comprises setting: 2 small inner conductors of the transmission line switching boundary, the differential propagation the center conductor 30 two signals; respectively constituting a plurality of ground via holes arranged around two central conductors 2 of the outer conductor boundary; on the ground by the connection of the via holes of the printed circuit board a conductor layer composed of a ground plate; two structural parameters and 5 disposed between the two outer conductors of the boundary inner conductors of the two, for adjusting the structural parameters of the printed circuit board with via holes adjustment, the two structural parameter adjustment via holes were filled with the first structural parameters constituting the insulating layer of the printed circuit board of a second, different structural parameters or a composite medium as a medium.

10 16. A printed circuit board with a compact design of the transmission line switching method, the printed circuit board with a small transmission line adapter comprising: forming said printed circuit board is disposed small inner

conductor switching boundary of the transmission line center conductor transmitting signals; a plurality of grounding via holes constituting the outer conductor of the transmission line switching compact boundary; and connected by the via holes in the ground printed circuit board conductor layer ground plate, wherein: 15 between the inner conductor and the outer conductor boundaries boundary set parameters for structural adjustment structural adjustment parameters of the printed circuit board with via holes, the said adjusting structural parameters via holes were filled with the first structural parameters constituting the insulating layer of the printed circuit board of a second, different structural parameters or a composite medium as a medium.

17. 20 Methods compact design of the transmission line switching according to claim 16, wherein the printed circuit board, wherein said second structure ﬀ parameter smaller than said first structure parameter.

18. 16 according to the printed circuit board design method according to claim small adapter transmission line, wherein. ﬁ The first and second structural parameters and relative permittivity any one of at least 25 in permeability.

19 16 According to the printed circuit board design method according to claim small switching transmission line, wherein: said adapter compact transmission line, and mounted on the printed circuit board and connected on the small adapter to connect the internal circuit transmission line impedance matching.

30 20. A printed circuit board with a compact design of the transmission line switching method, the printed circuit board with a small transmission line adapter comprising: forming said printed

circuit board is disposed small inner conductor switching boundary of the transmission line center conductor transmitting signals; a plurality of grounding via holes constituting the outer conductor of the transmission line switching compact boundary; and connected by the via holes in the ground a printed circuit board composed of a conductor layer ground plate, wherein. 5 at the boundary between the inner conductor and the outer conductor of the border provided for adjusting the structural parameters of the structural parameters of the printed circuit board with via holes adjustment, the boundary between the inner conductor and the outer conductor is also formed through the boundary of the printed circuit board air holes.

21 20 According to the printed circuit board design method according to claim small switching transmission line, wherein: the air hole 10, provided in the printed circuit board, so that adjust the settings on the printed circuit board and internal transmission line adapter is connected to the adapter connected to the transmission line between the impedance characteristics of the circuit.

The main electric and magnetic fields of the electromagnetic wave propagation 15 of the printed circuit board:.

22 according to claim 21 wherein the printed circuit board design method with a small switching transmission line, wherein for the propagation direction, vertical direction, and electric and magnetic fields perpendicular to each other.

23 20 According to the printed circuit board design method according to claim small switching transmission line, wherein: the maximum length of the cross-sectional shape of the air holes, in the printed given the frequency range of

the minimum wavelength of the signal circuit pull insulating layer 20 propagating 1/8 or less.

Description:

说明书 用转接孔；所述2个结构参数调整用转接孔分别由具有与构成所述印刷电 路板的绝缘层的第1结构参数不同的第二结构参数的一样的介质或复合介 质填充。

本发明的第4方面是一种印刷电路板用小型转接传输线路的设计方法， 5 该印刷电路板用小型转接传输线路包括：构成所述小型转接传输线路的内 侧导体边界，信号传递的中心导体；构成所述小型转接传输线路的外侧导 体边界的多个接地转接孔；连接在所述接地转接孔上的所述印刷电路板的 导体层构成的接地板；在所述内侧导体边界和所述外侧导体边界之间设置 用于调整所述印刷电路板的结构参数的结构参数调整用转接孔，所述结构 10 参数调整用转接孔分别由具有与构成所述印刷电路板的绝缘层的第1结构 参数不同的第二结构参数的一样的介质或复合介质填充。

所述第二结构参数比所述第一结构参数小。

所述第1和第2结构参数是介电常数和相对导磁率中的至少任意一个。

所述小型转接传输线路安装在所述印刷电路板上，与连接在所述小型 15 转接传输线路上的内部连接电路取得阻抗匹配。

本发明的第5方面是一种印刷电路板用小型转接传输线路的设计方法， 该印刷电路板用小型转接传输线路包括：构成所述小型转接传输线路的内 侧导体边界，信号传递的中心导体；构成所述小型转接传输线路的外侧导 体边界的多个接地转接孔；连接在所述接地转接孔上的所述印刷电路板的 20 导体层构成的接地板；在所述内侧导体边界和所述外侧导体边界之间设置 用于调整所述印刷电路板的结构参数的结构参数调整用转接孔，在所述外 侧导体边界之间穿过所述印刷电路板而形成空气孔。

Specification with via holes; structural parameters of the two via holes respectively, by adjusting the medium having the same structural parameters of the first printed circuit board constituting the insulating layer of a second, different structural parameters or composite media fill.

A fourth aspect of the present invention is a method of designing a printed circuit board with a small adapter transmission line, the printed circuit board 5 with a small adapter transmission line comprising: a compact adapter constituting the inner boundary of the transmission line conductor, center conductor signal transmission; the plurality of ground via hole constituting the outer boundary of the small conductor transmission line switching; connected to the ground via holes of the printed circuit board of a conductor layer ground plate; structure parameters between the inner conductor and the outer conductor boundary boundary adjusting the structural parameters of the printed circuit board is provided with via holes for adjustment, the parameter adjustment structure 10 having via holes constituting the respective Like the composite dielectric filling medium or the structural parameters of the first printed circuit board of the second insulating layer different structural parameters. parameter is smaller than the second structure of the first structure parameter.

The first and second dielectric constant and structural parameters is relative permeability of at least any one.

所述空气孔设置在所述印刷电路板上，从而调整设置在所述印刷电路 板上的转接传输线路和连接在该转接传输线路上的内部连接电路的特性阻 25 抗。

在所述印刷电路板上传播的主要电磁波的电场和磁场对于传播方向， 是垂直方向，并且电场和磁场彼此正交。

所述空气孔的截面形状的最大长度是在所述印刷电路板的绝缘层中传 播的信号的给定频率范围的最小波长的1/8以下。

附图说明 下面简要说明附图。

图IA是在印刷电路板中表示本发明的小型转接传输线路的平面图。

5 图IB是在印刷电路板中表示本发明的小型转接传输线路的纵剖视图。

图2A是在印刷电路板中表示把接地转接孔配置在圆周上的本发明的 小型转接传输线路的平面图。

图2B是在印刷电路板中表示把接地转接孔配置在圆周上的本发明的 小型转接传输线路的纵剖视图。

10 图3A是在印刷电路板中表示把接地转接孔配置在正方形上的本发明 的小型转接传输线路的平面图。

图3B是在印刷电路板中表示把接地转接孔配置在正方形上的本发明 的小型转接传输线路的纵剖视图。

图4A是在印刷电路板中表示在小型转接传输线路的结构参数调整用 15 转接孔的区域中形成空气孔的本发明的小型转接传输线路的平面图。

图4B是在印刷电路板中表示在小型转接传输线路的结构参数调整用 转接孔的区域中形成空气孔的本发明的小型转接传输线路的纵剖视图。

图5A是在印刷电路板中表示具有形成在中心导体和接地转接孔之间 的空气孔，具有结构参数调整用转接孔和形成印刷电路板

The compact transmission line adapter mounted on the printed circuit board, and connected to the adapter 15 compact transmission line connected to the internal impedance matching circuitry.

A fifth aspect of the present invention is a method of designing a printed circuit board with a small adapter transmission line, the printed circuit board using a small adapter transmission line comprising: a conductor constituting the inner boundary of a small adapter transmission line, center conductor signal transmission; a plurality of ground via holes constituting the outer boundary of the small conductor transmission line adapter; conductor layer 20 is connected to the ground via holes of the printed circuit board composed of a ground plate; structural parameters of the boundary between the inner conductor and the outer conductor boundary structural adjustment parameters of the printed circuit board is provided with via holes for adjustment, the boundary between the outer conductor through the printed circuit board and forming an air hole.

The air hole is provided in the printed circuit board, thereby adjusting the transfer characteristic of a transmission line disposed on said printed circuit board and connected to the adapter internal transmission line 25 connected to the anti-blocking circuit.

Electric and magnetic fields

on the printed circuit board of the main propagation direction of propagation of electromagnetic waves, the vertical direction, and the electric and magnetic fields orthogonal to each other.

The maximum length of

the cross-sectional shape of the air holes in the printed circuit board insulating layer propagates a signal given frequency

的接地层的导体 20 板的本发明的小型转接传输线路的平面图。

图5B是在印刷电路板中表示具有形成在中心导体和接地转接孔之间 的空气孔，具有结构参数调整用转接孔和形成印刷电路板的接地层的导体 板的本发明的小型转接传输线路的纵剖视图。

图6A是在印刷电路板中表示形成圆形并且不同大小的空气孔的本发 25 明的小型转接传输线路的平面图。

图6B是在印刷电路板中表示形成圆形并且不同大小的空气孔的本发 明的小型转接传输线路的纵剖视图。

图7是表示本发明的形成正方形以及长方形的空气孔的小型转接传输 线路的平面图。

30 图8是表示本发明的按照预先决定的基准，配置空气孔的小型转接传 输线路的平面图。

图9是表示本发明的不规则地配置空气孔的小型转接传输线路的平面 图。

图IOA是在印刷电路板中表示从本发明的小型转接传输线路到带状线 5 的传输线路的平面图。

图IOB是在印刷电路板中表示从本发明的小型转接传输线路到带状线 的传输线路的纵剖视图。

图IIA是在印刷电路板中表示从本发明的小型转接传输线路到微波传 输带线的传输线路的平面图。

10 图IIB是在印刷电路板中表示从本发明的小型转接传输线路到微波传 输带线的传输线路的纵剖视图。

图12是在印刷电路板中表示为了传输差动信号而形成小型转接传输线 路，并且具有与2个带状线连接的复合转接孔构造的2个基本单元的平面 图。

range of the minimum wavelength of 1/8 or less.

Brief Description brief description.

Figure IA is a plan view of a small transit transmission line of the present invention are shown in the printed circuit board.

5 Fig. IB is a longitudinal sectional view of small transit transmission line of the present invention are shown in the printed circuit board.

2A is a grounding via holes arranged in a plan view of a small adapter of the present invention the transmission line on the circumference of the printed circuit board.

2B is a grounding via holes arranged in the vertical transfer of small transmission line of the present invention on the circumference of a cross-sectional view of the printed circuit board.

10 3A is a grounding via holes arranged in a plan view of a small transit transmission line of the present invention in a square on the printed circuit board.

3B is a grounding via holes arranged in the vertical transfer of small transmission line of the present invention, a cross-sectional view of a square on the printed circuit board.

4A is a compact structure parameters in a transmission line switching plan view of a small adjustment of the transmission line switching region 15 is formed in the via holes of the present invention, air holes in the printed circuit board.

Figure 4B shows the structural parameters of the transmission line transfer small vertical adjustment of the transmission line transfer area small via holes are formed in the air hole of the

15 图13是在印刷电路板中表示形成本发明的小型转接传输线路，与带状 线连接的SMA连接器的转接孔构造的平面图。

图14A是在印刷电路板中表示在圆周上配置接地转接孔，从多层印刷 电路板表面到途中形成中心导体、接地转接孔、结构参数调整用转接孔、 填充用介质的本发明的小型转接传输线路的平面图。

20 图14B是在印刷电路板中表示在圆周上配置接地转接孔，从多层印刷 电路板表面到途中形成中心导体、接地转接孔、结构参数调整用转接孔、 填充用介质的本发明的小型转接传输线路的纵剖视图。

图15A是表示在小型转接传输线路的结构参数调整用转接孔的区域中 形成空气孔，从多层印刷电路板表面到途中形成中心导体、接地转接孔、 25 结构参数调整用转接孔、填充用介质的本发明的小型转接传输线路的平面 图。

图15B是表示在小型转接传输线路的结构参数调整用转接孔的区域中 形成空气孔，从多层印刷电路板表面到途中形成中心导体、接地转接孔、 结构参数调整用转接孔、填充用介质的本发明的小型转接传输线路的纵剖 30 视图。

图16A是表示对安装在由12层的导体层构成的多层衬底上的通常的转 接传输线路以及本发明的小型转接传输线路的反射系数的仿真结果的图。

图16B是表示对安装在由12层的导体层构成的多层衬底上的通常的转 接传输线路以及本发明的小型转接传输线路的透过系数的仿真结果的图。

5 图17A是表示对安装在由12层的导体层构成的多层衬底上的通常的转 接传输线路以及本发明的小型转接传输线路的反射系数的仿真结果的图。

图17B是表示对安装在由12层的导体层构成的多层衬底上的通常的转 接传输线路以及本发明的小型转接传输线路的透过系数的仿真结果的图。

present invention in a cross-sectional view of the printed circuit board.

5A is a diagram showing an air hole is formed between the center conductor and the ground via holes in the printed circuit board having a via hole adjusting structural parameters and forming a printed circuit board ground plane conductor 20 of the plate a plan view of a small transit transmission line to the invention.

5B is an air vent is formed between the center conductor and the ground via holes in the printed circuit board having a via hole adjusting structural parameters and forming a printed circuit board ground plane of the conductive plate of the present invention, a longitudinal cross-sectional view of the adapter compact transmission lines.

6A is a plan view and a circular air holes of different sizes small adapter present invention the transmission line 25 in the printed circuit board.

Figure 6B is a cross-sectional view showing a circular and longitudinal sizes of the air holes of the present invention is compact switching transmission lines in the printed circuit board.

FIG. 7 is a plan view of a compact transmission line adapter of the present invention is formed of a square and rectangular air hole Fig.

30 8 is the reference in accordance with a pre-determined plan view showing the configuration of a small air hole adapter transmission line of the present invention.

FIG. 9 is a plan view showing the configuration of the present invention irregularly small air holes transit transmission line.

图18A是表示对安装在由12层的导体层构成的多层衬底上的通常的转 10 接传输线路以及本发明的小型转接传输线路的反射系数的仿真结果的图。

图18B是表示对安装在由12层的导体层构成的多层衬底上的通常的转 接传输线路以及本发明的小型转接传输线路的透过系数的仿真结果的图。

具体实施方式 15 下面，说明本发明实施例的概要。

本发明的小型转接传输线路具有：形成所述小型转接传输线路的内侧 导体层的边界，构成信号用转接孔的中心导体；配置在中心导体的周围， 形成小型转接传输线路的外侧导体边界的多个接地转接孔；由印刷电路板 导体层构成的多个导体板；为了在小型转接传输线路的内侧导体层的边界 20 传播的信号与外侧导体层的边界电位在高频信号频带中不串扰而电分离的 结构参数调整用转接孔。该结构参数调整用转接孔可以由一样的物质或不 同的多个物质构成的复合材料填充。作为特别的例子，有在构成信号用转 接孔的中心导体与转接传输线路的接地转接孔之间形成空气孔，调整印刷 电路板的结构参数的方法。

25 选择填充本发明的结构参数调整用转接孔的填充用介质，从而使印刷 电路板小型化，并且通常把小型转接传输线路和安装在印刷电路板上并且 连接在小型转接传输线路上的电路的特性阻抗匹配。通过把填充结构参数 调整用转接孔的介质材料或空气孔的介电常数和导磁率的任意一方或双方 的参数选择为不同，能使印刷电路板小型化，所以能提高安装密度。此外， 30 使用本发明的转接传输线路的印刷电路板能在宽阔频带的频率下工作，所 以能传输高速的数字信号。

下面参照附图详细说明本发明实施例。

在以下的实施例中，主要关于包含一个信号转接孔的小型转接传输线 路进行说明，但是本发明并不一定局限于小型转接传输线路，此外，例如 5 像1对信号转接孔那样，对安装在印刷电路板上的小型转接传

Figure IOA is a plan view of a printed circuit board, said stripline transmission line 5 from the small adapter to the transmission line of the present invention.

Figure IOB is a cross-sectional transmission line from a small adapter of the present invention to a vertical stripline transmission lines in view of the printed circuit board.

FIG IIA is a plan view showing a printed circuit board transmission lines with a microwave transmission line from the small adapter to the transmission line of the present invention.

10 is a sectional diagram IIB from small adapter transmission line of the present invention to a vertical transmission line microwave transmission line with a view of the printed circuit board.

FIG. 12 is a differential signal and to transmit a transmission line to form a compact adapter, and having a via hole and a plane view of a composite strip line 2 connected to the basic structure of the two units in the printed circuit board.

15 13 is a plan view of the SMA connector of the present invention, the formation of a small adapter transmission line, and stripline structure connected via holes are shown in the printed circuit board. in FIG. 14A is a printed circuit board on the ground via holes disposed circumferentially, the center conductor is formed from the surface of the multilayer printed circuit board on the way to the ground via holes, the via holes adjusting structural parameters, filled with medium a plan view of a small transit transmission line of the present invention.

20 14B is disposed circumferentially on the ground via holes, the center conductor is formed from the surface of the multilayer printed circuit board on the way to the ground via holes, via holes

输线路的任 意多个信号传输线路，也能容易应用。

复杂、高密度地配置转接孔的任意数量的小型转接传输线路能用于连 接平面传输线路等任意种类的内部连接电路。此外，本发明的小型转接传 输线路对于具有任意的传输线路的多层印刷电路板，也能应用。

10 图IA和图IB是在印刷电路板中，表示本发明的小型转接传输线路的 平面图以及纵剖视图。如果参照图IA和图1B，则作为多层印刷电路板的 设计例，表示形成在由10层的导体层1～10构成的多层印刷电路板上的小 型转接传输线路的例子。在多层印刷电路板中，通过由绝缘层105绝缘的 导体层1～10，形成接地线107、信号线108、电源线109。小型转接传输线 15 路采用包含以下部分的结构：中心导体101、配置在中心导体101的周围的 接地转接孔102、由导体层106形成的接地板106、由填充用介质104填充 的直径dde的结构参数调整用转接孔103。这里，构成信号转接孔的中心 导体101传输高频信号。

为了满足小型化和与内部电路的特性阻抗匹配的双方，选择填充用介 20 质104的结构参数例如介电常数或导磁率的一方或双方，从而与绝缘层105 的结构参数不同。即从与小型转接传输线路结合的电路入射的电磁波信号 的能量在该结合点，由于反射，其一部分返回，但是通过调整小型转接传 输线路的尺寸、介电常数或导磁率的一方或双方的值，能极端减小反射， 使信号振幅几乎不衰减，进行信号的传输。

25 此外，当形成转接传输线路的外侧导体边界的接地转接孔的数量多到 相邻的接地转接孔之间的距离小于X/4（X是在给定频率范围中，印刷电 路板的绝缘层的传输信号的最小波长）的程度时，能把该转接传输线路作 为充分绝缘的传输线路考察。此外，包含接地转接孔的转接传输线路的外侧边界能作为基于近似连续的导体的边界考察。可以用把基于连续的导体 30 的边界视为同轴电缆的一部分，信号波沿着该边界前进的近似计算转接传 输线路的特性阻抗。

adjusting structural parameters in the printed circuit board, filled with small vertical cross-sectional view of the transmission line transfer medium of the present invention. in FIG. 15A is a compact structural parameter adjustment area of the transmission line switching via holes formed in the air hole with the center conductor, the grounding via holes 25 are formed from the multilayer structure to adjust the parameters of the printed circuit board on the way to the surface with via holes, a plan view of a small transit transmission line filled with medium of the present invention.

15B is compact in structure parameter adjustment area of transit transmission lines via holes formed in the air hole, the center conductor is formed from the surface of the multilayer printed circuit board on the way to the ground via holes, adjusting structural parameters 30 a longitudinal sectional view of the transmission line transfer of small via holes filled with the medium of the present invention.

FIG. 16A is a diagram showing simulation results usually turn connected to the transmission line and the reflection coefficient of the small transit transmission line of the present invention is mounted on the multilayer substrate 12 by a conductor layer composed of a layer of FIG.

FIG. 16B is a diagram of a conventional transmission line connection switch mounted on the multilayer substrate layer of a conductive layer 12 composed of a transmission line and a small adapter of the present invention through the simulation coefficient FIG.

5 FIG. 17A is a diagram showing simulation results usually turn connected to the transmission line and the reflection coefficient of the small transit transmission line of the present invention

为了说明用于把安装在印刷电路板上的转接传输线路小型化的物理基 础条件，考察关于接地转接孔的几个典型的几何学形状和配置。

图2A以及图2B是在印刷电路板中，表示把接地转接孔配置在圆周上 5 的本发明的小型转接传输线路的平面图和纵剖视图。如果参照图2A以及图 2B,则除了以中心导体201为中心，在圆周上以等间隔配置接地转接孔202 的点，与图IA以及图IB所示的构造同样。如果为了使印刷电路板中使用的导体层彼此绝缘而使用的绝缘层205与结构参数调整用转接孔203的填 充用介质204相同，则转接传输线路的特性阻抗能用信号波在圆周上的连 10 续的内侧导体边界和外侧导体边界之间前进时使用的众所周知的以下的表 达式（1)近似。

这里，Zr是小型转接传输线路的特性阻抗，Rr=Dr/2是中心导体的中 15 心和构成外侧导体边界的接地转接孔之间的距离，rrod=drod/2是中心导体 的半径，e是绝缘层205的介电常数，绝缘层205的介电常数为1。

在本发明的小型转接传输线路中，填充直径dele的结构参数调整用转 接孔203的填充用介质204的介电常数必须与构成印刷电路板的绝缘层205 的介电常数不同。

20 因此，这时，通过由填充结构参数调整用转接孔203的填充用介质204 的介电常数、印刷电路板的绝缘层205的介电常数双方决定的有效介电常 数计算安装在印刷电路板上的转接传输线路的特性阻抗。

该有效介电常数由已知的逻辑和实验的方法求出。如果填充在小型转 接传输线路的结构参数调整用转接孔中的填充用介质204的介电常数比绝 25 缘层205的介电常数还小时，转接传输线路的有效介电常数比绝缘层205 的介电常数还小。

据此，当比较填充用介质204和绝缘层205的材料相同的转接传输线 路、所述本发明的小型转接传输线路时，2个转接传输线路的特性阻抗相等， 并且填充结构参数调整用转接孔的填充用介质以外的参数相等，本发明的 小型转接传输线路的截面积

is mounted on the multilayer substrate 12 by a conductor layer composed of a layer of FIG.

FIG. 17B is a diagram of a conventional transmission line connection switch mounted on the multilayer substrate layer of a conductive layer 12 composed of a transmission line and a small adapter of the present invention through the simulation coefficient FIG.

FIG. 18A is a diagram showing simulation results for conventional transmission lines connected to switch 10 and the reflection coefficient of the small transit transmission line of the present invention is mounted on the multilayer substrate 12 by a conductor layer composed of a layer of FIG.

FIG. 18B is a diagram of a conventional transmission line connection switch mounted on the multilayer substrate layer of a conductive layer 12 composed of a transmission line and a small adapter of the present invention through the simulation coefficient FIG.

15 The following specific embodiments will be outlined embodiments of the present invention.

Small forwarding the transmission line of the present invention comprises: a transmission line of the boundary of a small adapter inner conductor layers constituting the via hole center signal conductor; arranged around the center conductor, form a compact transmission adapter a plurality of ground conductor via holes of the outer boundary line; a plurality of printed circuit board by a conductive plate of a conductor layer; compact border to the potential at the boundary of the transmission line adapter inner conductor layer 20 and the outer conductor signal propagation layer structural parameters in the high frequency band signal crosstalk is not

比以往的填充用介质204和绝缘层205的材料 相同的转接传输线路的截面积小。

从以上可知，在圆周上配置图2A以及图2B所示的接地转接孔202的 5 小型转接传输线路的特性阻抗由以下的表达式（2)表示。

ZCVT、r ^ 60 广R)) 2 C V Vrod) 这里，ZCVT, r是小型转接传输线路的特性阻抗，e eff是从绝缘层205 和填充结构参数调整用转接孔的填充用介质204的双方决定的有效介电常 数。

从表达式（2)可知，如果填充结构参数调整用转接孔的填充用介质的 介电常数减小，则有效介电常数减小，为了把特性阻抗保持一定，例如50 Q，距离Rr必然减小。该事实提供用于开发小型转接传输线路的设计方针。

为了实现印刷电路板的转接传输线路的小型化，重要的是进行选择，从而 使填充结构参数调整用转接孔的绝缘层的介电常数比把印刷电路板的导体 层绝缘的绝缘材料的介电常数还小。

图3A和图3B是表示为了接地转接孔302分别包围中心导体301而配 置为正方形的印刷电路板中小型转接传输线路的平面图和剖视图。为了简 化说明，与图IA以及图IB同样，表示为小型转接传输线路嵌入印刷电路 板中。

如果构成小型转接传输线路的直径dele的结构参数调整用转接孔303 由与把印刷电路板的导体层绝缘的绝缘层相同的材料填充时，转接传输线 路的特性阻抗能由信号波在正方形的连续的内侧导体边界和外侧导体边界 之间前进时使用的众所周知的以下表达式（3)近似。

r ^sq w 60 • • In .0787 • Rsa) 3 /lv rrod 这里，Zsq是小型转接传输线路的特性阻抗，Rsq=Dsq/2是中心导体的 中心和构成外侧导体边界的接地转接孔中离中心导体最近的接地转接孔之 间的距离，rrod=drod/2是中心导体的半径，e是绝缘层205的介电常数， 绝缘层305的介电常数为1。

electrically isolated via holes adjustment. The structural parameter adjustment as a composite material may be filled with a substance or different substances constituted by a plurality of via holes. As a specific example, there is used in the method of constituting the signal via holes between the center conductor and the ground via hole transfer transmission line formed air holes, adjusting the structural parameters of the printed circuit board.

25 to select the structural parameters of the present invention may be adjusted by filling the via holes filled with a dielectric, so that the size of the printed circuit board, and usually a small transmission line adapter and mounted on a printed circuit board and connected to a small adapter characteristics of the circuit transmission line impedance matching. By filling structural adjustment parameters either one or both of the parameters via holes or air holes in a dielectric material permittivity and permeability of different, to make the printed circuit board miniaturization, it is possible to improve the mounting density. Furthermore, the present invention is the use of an adapter 30 of the transmission line of the printed circuit board can operate in a wide frequency band, can be transmitted to the high-speed digital signals.

The following detailed description of embodiments with reference to the accompanying drawings of the present invention.

In the following examples, primarily on the via holes comprising a small switching signal transmission line will be described, but the present invention is not necessarily limited to the transfer of small transmission lines, in addition, for example, 5 as one pair of signal transduction jack as a signal transmission

为了在印刷电路板上形成小型转接传输线路，重要的是使填充结构参 5 数调整用转接孔303的填充用介质304的介电常数比把印刷电路板的导体 层绝缘的绝缘层305的介电常数小，这时，把图3A以及图3B所示的接地 转接孔配置在正方形上的小型转接传输线路的特性阻抗由以下的表达式 (4) 表示。

Zcv7r «60^ I——^In--si .0787 •足 rrod Ni/ 这里，ZCVT，r是小型转接传输线路的特性阻抗，e eff是从绝缘层305 和填充结构参数调整用转接孔的填充用介质304的双方决定的有效介电常 数。

来自对使用配置在正方形上的接地转接孔的小型转接传输线路的考察 15 的结论与从使用配置在圆周上的接地转接孔的小型转接传输线路的考察取 得的结论是同样的。即通过减小填充结构参数调整用转接孔的填充用介质 的介电常数，能把小型转接传输线路小型化。上述的2个实施例是基于包 围构成信号转接孔的中心导体而形成接地转接孔，并且使填充结构参数调 整用转接孔的填充用介质与把印刷电路板的导体层绝缘的绝缘材料不同的 20 设计思想。

在形成复合介质上特别重要的方法是使用空气孔作为转接孔构造的方 法。这是因为空气的介电常数和相对导磁率实质上为 1，所以使用空气孔的 复合介质适合构成小型转接传输线路。

下面说明使用空气孔形成小型转接传输线路的实施例。图4A和图4B 25 是表示具有分别在构成信号转接孔的中心导体401的周围配置为正方形的 接地转接孔402的小型转接传输线路的平面图以及剖视图。在小型转接传 输线路中，填充结构参数调整用转接孔403的复合绝缘体404中，复合绝缘体404的介电常数比用于把印刷电路板的导体层绝缘的绝缘层405的介 电常数小，设置空气孔，从而在构造上穿过位于结构参数调整用转接孔403 的区域的绝缘层405。这里，关于印刷电路板的导体层配置，与图1以及图 IB所示的构造同样。穿过绝缘层405而设置的空气孔410形成能视为有效 介电常数比印刷电路板405的介电常数还小的结构参数调整用转接孔403

line of any number of printed circuit board mounted on a small transfer of the transmission line can be easily applied. complex, a high density of via holes arranged any number of transmission lines can be used to transfer small connecting planar transmission line or the like connected to any type of internal circuitry. In addition, a small transmission line adapter of the present invention having an arbitrary transmission line for a multilayer printed circuit board can also be applied.

10 Fig. IA and IB is a printed circuit board, a plan view of a small adapter transmission line of the present invention and a longitudinal cross-sectional view. Referring to Fig IA and 1B, the embodiment is designed as a multilayer printed circuit board, represented by a small-sized adapter is formed in the transmission line conductor layer 10 composed of layers 1~10 multilayer printed circuit board of the example. In the multilayer printed circuit board, the insulating layer 105 by the insulating layer 1~10 conductor, a ground line 107, the signal line 108, the power line 109. Small adapter circuit 15 uses the transmission line structure comprises the following parts: a center conductor 101, disposed in the ground via holes 101 around the center conductor 102, conductive layer 106 is formed by a ground plate 106, 104 is filled by the filling medium with a diameter dde structural adjustment parameters via holes 103. Here, the center conductor signal via holes 101 high frequency signals.

In order to meet the size and characteristics of the internal impedance matching circuits both selected structural parameters 20 is filled with dielectric substance 104, for example, one of the dielectric constant or magnetic permeability or both, so that the

5 的复合介质。结构参数调整用转接孔403的复合介质的有效介电常数依存 于由空气孔410占有的体积，能从已知的理论和实验结果求出。使用形成 这样的结构参数调整用转接孔上的复合介质，能一边保持与不使用空气孔 时的转接传输线路的特性阻抗相同的值，一边开发更小型的转接传输线路。

在小型转接传输线路中，使用表示把接地转接孔配置在圆周上或正方形上 10 时的特性阻抗的所述表达式（2) ~表达式（4)，导出该结论。形成空气孔， 使复合介质的有效介电常数减小，能比印刷电路板的绝缘层减小有效损失 系数。

通过由空气孔和印刷电路板的绝缘材料构成的复合介质，能够乘减小 小型转接传输线路的截面积的本发明的小型转接传输线路。此外通过减小 15 有效介电常数和到形成外侧导体边界的距离，在小型转接传输线路中，能 传输高次的谐波成分，据此，能扩大小型转接传输线路的工作频率范围。

安装在印刷电路板上的小型转接传输线路的空气孔使空冷时的空气循环良 好，据此，能改善高密度安装中的散热特性。

在小型转接传输线路中，电磁波中的基本波主要存在于构成信号转接 20 孔的中心导体和构成外侧导体边界的接地转接孔之间，所以在应用上，空 气孔不仅在结构参数调整用转接孔的区域，能在中心导体和接地转接孔之 间的全部区域中形成。

图5A以及图5B是表示具有形成在中心导体和接地转接孔之间的空气 孔，具有形成结构参数调整用转接孔503和印刷电路板的接地层的导体半 25 的小型转接传输线路的平面图和剖视图。穿过结构参数调整用转接孔503 的区域、由导体层507构成的导电板506而在该区域和接地转接孔502之间的区域形成空气孔510。小型转接传输线路的空气孔的截面能采用任意形 状和任意尺寸，但是有必要比在用于把印刷电路板的导体层的绝缘的绝缘 层505中前进的传输信号的波长A还小很多，例如为KX/8。这里，1是 30 空气孔的截面的最大

insulating layer 105 and the structural parameters are different. That is, due to reflection, a part of the energy returned from the transmission line in combination with a small switching circuit of the incident electromagnetic signal at the binding points, but by adjusting the size of a small switching transmission lines, dielectric constant or the permeability of one or both the value of the reflection can be extremely reduced, so that almost no attenuation of the amplitude of the signal, the signal transmission.

25 In addition, when the adapter is formed from the ground outer conductor of the transmission line of the boundary of the via holes quantity via holes to the adjacent ground is less than X / 4 (X is in a given frequency range, when the printed circuit board minimum wavelength of the transmission signals insulating layer) level, can transfer the transmission line as a transmission line inspection sufficiently insulated. Further, the outer side of the boundary contains ground via holes adapter can be used as a transmission line boundary study based on approximate continuous conductor. Can be regarded as part of the coaxial cable-based boundary continuous conductor 30, the signal wave along the border along the approximate calculation of characteristic impedance of the transmission line switching.

To illustrate the transmission line is used to transfer small physical conditions based mounted on a printed circuit board, examining several typical geometrical shape and configuration of the ground via holes.

Figures 2A and 2B is a printed circuit board, showing the grounding via holes arranged in a cross-sectional view of a small adapter on the circumference of the transmission line 5 is a plan view of the present invention and vertical. If

长度，X是在给定的频率范围中，电路板的绝缘层的 中的传输信号的最小波长。

图6A和图6B是在印刷电路板中表示形成圆形并且不同大小的空气孔 的本发明的小型转接传输线路的平面图和剖视图。在图6中，分别直径dal 和da2的圆柱状空气孔配置在中心导体601和用于形成正方形的外侧导体 5 边界的接地转接孔602之间。

图7是表示本发明的形成正方形以及长方形的空气孔的小型转接传输 线路的平面图。在图7中，空气孔710的水平截面形状为正方形以及长方 形，如图所示，在正方形以及长方形中，为不同的大小。在图7中，虽然 未表示纵剖视图，但是与图5B所示的纵剖视图同样。即空气孔710具有水 30 平截面形状为图7所示的正方形以及长方形的柱状的构造。

空气孔按照给定的规则配置，或者也可以不规则地佩兹。图8表示按 照预先决定的规则配置空气孔810的小型转接传输线路的具体例。构成小 型转接传输线路的小型转接传输线路的接地转接孔802配置在圆周上，从 而在中心导体801的周围，离中心导体801的距离相等，配置空气孔810，15 从而在中心导体801的周围，相邻的空气孔彼此的距离相等，此外离中心 导体801的距离相等。

图9是表示在中心导体901和构成外侧导体边界的接地转接孔902之 间不规则地配置空气孔910的小型转接传输线路的平面图。

作为小型转接传输线路的空气孔的形成方法，考虑到用机械形成孔的 20 方法、由激光形成孔的方法等各种方法。

当然为了把印刷电路板的各种内部连接电路结合而使用印刷电路板用 小型转接传输线路，但是在图IOA和图IOB中，表示在12层的多层印刷电 路板中，把小型转接传输线路和作为带状线1011的平面传输线路结合的具 体例。从图IOA和图IOB可知，小型转接传输线路具有中心导体1001、配25 置在正方形上的接地转接孔1002、由构成印刷电路板的导体层构成的接地 板1006、结构参数调整用转接孔1003。

reference to Figures 2A and 2B, the center conductor 201 in addition to the center, circumferentially arranged at equal intervals in the grounding point via holes 202, and FIG. IA and FIG. IB structure shown in the same. If the insulating layer 205 and the structural parameters to the conductor layer of the printed circuit board for use in insulated from each other by using adjustment via holes 203 are filled with the same medium 204, the transfer characteristic impedance of the transmission line can be the signal wave in the circumferential even less well-known expression is advanced between 10 continuous inner conductor and the outer conductor boundary border use of (1) approximation.

Here, Zr is the characteristic impedance of the transmission line mini adapter, Rr = Dr / 2 is the distance between the center of the center conductor 15 to ground via holes and constitute the boundary between the outer conductor, rrod = drod / 2 is the center conductor radius, e is the dielectric constant of the insulating layer 205, the insulating layer 205 is a dielectric constant of 1.

In a small adapter transmission line of the present invention, the structural parameters of adjustment dele diameter filled via holes filled with a dielectric constant media 203 204 must constitute a printed circuit board with a dielectric constant of the insulating layer 205 is different.

Effective dielectric constant

20 Thus, this time, by adjusting the via hole 203 is filled with the filling medium the structural parameters of the dielectric constant of 204, the insulating layer of the printed circuit board 205 of the dielectric constant determined by calculating both installation in the transfer

小型转接传输线路中的复合介质由用于把印刷电路板的导体层绝缘的 绝缘层1005、根据预先决定的规则在小型转接传输线路的中心导体1001和 接地转接孔1002之间形成不同尺寸的空气孔1010构成。这里，4个大的空 30 气孔中，相邻的空气孔彼此的距离相等，并且均等地配置在中心导体1001 的周围，3个小的空气孔在相邻的大的空气孔之间，均等地配置在中心导体 1001的周围。全部空气孔对于带状线1011的水平轴配置为对称。这里，从 图IOA可知，在包含带状线1011的区域中，不存在对应的小的空气孔。小 型转接传输线路的复合介质的有效介电常数比绝缘层1005的介电常数小， 5 因此，一边把带状线1011的特性阻抗保持相同的值，一边能使连接在带状 线1011上的传输线路小型化。

在图IIA和图IIB中表示在12层的多层印刷电路板中，把小型转接传 输线路和作为微波传输带线1112的平面传输线路结合的具体例。从图IIA 和图IIB可知，小型转接传输线路具有中心导体1101、配置在圆周上的接 10 地转接孔1102、由构成印刷电路板的导体层1107构成的接地板1106、结构参数调整用转接孔1103。

小型转接传输线路的复合介质由用于把印刷电路板的导体层绝缘的绝 缘层1105、除了微波传输带线1112的区域而不规则地配置在小型转接传输 线路的中心导体1101和接地转接孔1102之间的空气孔1110构成。小型转 15 接传输线路的复合介质的有效介电常数比绝缘层1105的介电常数小，因此 一边把微波传输带线1112的特性阻抗保持相同的值，一边能使到达微波传 输带线1112的传输线路小型化。

图12表示用于传输差动心好的小型转接传输线路的一例，表示具有高 密度转接孔构造的2个基本单元。这2个基本单元构成信号转接孔对，分 20 别连接在作为平面传输线路的一例的带传输线路对上。小型转接传输线路 由分别由接地转接孔1202包围的2个信号转接孔1201、由导体层构成的接 地层、2个结构参数调整用转接孔1203构成。为了把转接传输线路小型化、

characteristic of the transmission line impedance of the printed circuit board.

The effective dielectric constant determined by a method known in logic and experiment. If you fill in the configuration parameters of the transmission line switching small adjustment in the via holes 204 are filled with a dielectric constant of the medium than the insulating layer 25 must have a dielectric constant of 205 hours, the effective dielectric constant than the insulating transmission line adapter permittivity layer 205 is also small.

Accordingly, when the same comparison is filled with a dielectric material 204 and the insulating layer 205 of switching transmission line, the transmission line at a small adapter of the present invention, the adapter 2 is equal to the characteristic impedance of the transmission line, and fills small structural parameter adjustment via holes are filled with the medium outside the parameters are equal, the small cross-sectional area of the adapter of the present invention, the transmission line is filled with the same medium than the conventional insulating layer 204 and the material 205 is a sectional area of the transmission line switching.

From the above, in the circumferential configuration of FIG. 2A and FIG. 2B 5 small transfer characteristic of the transmission line 202 to ground as shown in the impedance of the via holes (2) represented by the following expression.

ZCVT, r 60 Kwong R)) 2 CV Vrod) Here, ZCVT, r is the characteristic impedance of the transmission line a small adapter, e eff from the filling structure 205 and the insulating layer parameter adjustment via holes are filled with effective dielectric constant media 204 both decisions.

取得小型转接传输线路和带传输线路对的特性阻抗匹配，形成空气孔1210。

图13是表示小型转接传输线路的应用例即SMA(sub-miniature-type-A) 25 连接器的转接孔构造的平面图。通常的SMA连接器的管脚具有信号转接孔 1301和接地转接孔1313。在图13中，再度表示作为平面传输线路构造的 一例的带状线1311和信号转接孔1301的连接。

可是，通常的转接传输线路在高频产生大的辐射和遗漏损失，由于依 存于与接地转接孔1313的距离的高次的激励振荡，受到工作频率范围的限 30 制。

为了实现SMA连接器的良好的转接孔构造，使用本发明的小型转接传 输线路非常有效。在图13中，小型转接传输线路具有：构成信号转接孔的 中心导体1301、配置在圆周上的接地转接孔1302、由印刷电路板的导体层 构成的电源板、接地板等导体板、结构参数调整用转接孔1303。此外，通 5 过在绝缘层穿过空气孔1310，形成复合介质。

决定中心导体1301和接地转接孔1313的距离、空气孔1310的数量和 大小，从而在包含SMA连接器和带状线的内部连接电路中，使特性阻抗最 佳化。而且，在给定的频率范围中，主要采用只传播基本模式的电磁波的 构造。更具体而言，设定为在印刷电路板中传播的电磁波的电场和磁场对 10 于传播方向，是垂直方向，并且电场和磁场彼此正交传播。可是，在传播 实际的印刷电路板中传播的电磁波中，不仅是所述基本模式的电磁波，同 时也包含对于传播方向，电场和磁场从垂直方向偏离，并且电场和磁场彼 此不正交的电磁波。这时，同样能应用本发明。

在所述实施例中，从多层印刷电路板的表面贯通到背面设置中心导体、 15 接地转接孔、结构参数调整用转接孔、填充用介质，但是不一定要贯通， 也可以从多层印刷电路板的表面到到构成多层印刷电路板的内部衬底形成 中心导体、接地转接孔、结构参数调整用转接孔、填充用介质的一部分或 全部。

From the expression (2), if the structure is filled with a dielectric constant parameter adjustment via holes are filled with medium decreases, the effective dielectric constant is reduced, in order to maintain a certain characteristic impedance, for example, 50 Q, distance Rr inevitably reduced. This fact provides for the development of small transit transmission line design guidelines.

In order to realize miniaturization of the printed circuit board switching transmission line, it is important to choose, so that the structural parameters of filling the via holes of the insulating layer is adjusted by the ratio of the dielectric constant of the printed circuit board insulated conductor layer permittivity insulating material is still small.

Figures 3A and 3B is a via hole 302 for grounding the center conductor 301 surrounded respectively configured as a square plan view of a printed circuit board sized adapter and a sectional view of the transmission line. To simplify the explanation, FIG. IA and FIG. IB denotes an adapter for small transmission line embedded in the printed circuit board. with the via hole 303 by the printed circuit board and the conductor insulating layer of the same material as the insulating layer is filled, if the transfer characteristic of the transmission line structure constituting the dele small diameter parameter transfer impedance of the transmission line is adjusted by the energy the following well-known expression between the square wave signal when the continuous inner conductor and the outer conductor boundaries boundary proceeds used (3) approximation. r sq w 60 ◆ ◆ In.0787 ◆ Rsa) 3 / Iv rrod Here, Zsq is the characteristic impedance of the transmission line of a small adapter, Rsq = Dsq / 2 is the center of the center

图14A和图14B是表示在印刷电路板中，分别在圆周上配置接地转接 20 孔1402，从多层印刷电路板的表面到途中形成中心导体1401、接地转接孔 1402、结构参数调整用转接孔1403、填充用介质1401的本发明的小型转接 传输线路的平面图和剖视图。在所述图2A和图2B所示的构造中，从多层 印刷电路板的表面贯通到背面形成中心导体201、接地转接孔202、结构参 数调整用转接孔203、填充用介质204。而在本实施例的图14A和图14B 25 所示的构造中，从最表面层的第1层到第3层形成中心导体1401，从最表 面层的第1层到第4层形成接地转接孔1402、结构参数调整用转接孔1403、 填充用介质1404。

图15A和图15B是表示分别在小型转接传输线路的结构参数调整用转 接孔的区域形成空气孔，从多层印刷电路板的表面到途中形成中心导体 30 1501、接地转接孔1502、结构参数调整用转接孔1503、空气孔1510的本 发明的小型转接传输线路的平面图和剖视图。图15A和图15B所示的本实 施例的构造除了以下的点，与所述图4A和图4B所示的构造类似。在图15A 和图15B所示的本实施例的构造中，从最表面层的第1层到第3层形成中 心导体1501，从最表面层的第1层到第4层形成接地转接孔1502、结构参 5 数调整用转接孔1503、空气孔1510。

通过这样从多层印刷电路板的表面到构成印刷电路板的内部的衬底形 成中心导体、接地转接孔、结构参数调整用转接孔、填充用介质的一部分 或全部，能进一步最优化小型转接传输线路的特性阻抗。

下面为了表示小型转接传输线路的优越性，在包含小型转接传输线路 10 的构造中，说明关于高速信号传输的几个仿真结果。仿真结果表示通过由 差分时间区域（finite-difference time-domain=FDTD)法计算的S参数的大 小表示小型转接传输线路的优越性。该FDTD法在表示内部连接电路的特 征时可以说是最正确、恰当并且多目的的逻辑计算手法。

图16是表示从50 Q的同轴电缆通过小型转接传输线路向其他50 Q的 15 同轴电缆传输时，对于安装在由12层的导体层构成的

conductor and the ground conductor constituting the outer boundary the via holes from the center of the nearest ground conductor via holes between, rrod = drod / 2 is the radius of the center conductor, e is the dielectric constant of the insulating layer 205, the dielectric constant of the insulating layer 305 is 1.

In order to form a compact adapter printed circuit board transmission lines, it is important that structural parameters filled with 5 adjustments via holes filled with a dielectric constant media 303 304 than the printed circuit board conductor layer insulation the dielectric constant of the insulating layer 305 is small, then, to FIG. 3A and 3B shown grounded via holes arranged on the small square of the characteristic impedance of the transmission line adapter (4) represented by the following expression.

Zcv7r ⊘60 I - ln - si.0787 ⊘ Foot rrod Ni / Here, ZCVT, r is the characteristic impedance of the transmission line of a small adapter, e eff is adjusted from 305 and filled with an insulating layer structure parameters via holes are filled with effective dielectric constant media 304 both decisions.

Conclusions from the use of configuration via holes in the ground on the square of a small transit transmission line 15 of investigation and study obtained from the use of the configuration in a small adapter transmission line via holes to ground on the circumference of the conclusion that same. That is, by reducing the structural parameters of adjusting filling the via holes are filled with a dielectric constant of the medium, small adapter transmission line can be miniaturized. 2 embodiment described above is based surrounds a central signal conductor grounded via holes to form via holes, and adjusting structural parameters of the filling via holes filled

多层电路板上的通常 的转接传输线路以及本发明的小型转接传输线路的反射系数（SII参数）的 频率依存性的仿真结果的图。图16B是表示从50Q的同轴电缆通过小型转 接传输线路向其他50Q的同轴电缆传输时，对于安装在由12层的导体层构 成的多层电路板上的通常的转接传输线路以及本发明的小型转接传输线路 20 的透过系数（S12参数）的频率依存性的仿真结果的图。小型转接传输线路 安装在12层的多层印刷电路板上，由中心导体、配置在正方形上的8个接 地转接孔、由导体层构成的电源板、接地板等导体板、8个空气孔和结构参 数调整用转接孔形成。

关于仿真中使用的小型转接传输线路和12层的多层电路板的几何形 25 状，与图6A和图6B所示相同。这里，仿真中使用的中心导体和8个接地 转接孔的大小如下所述。即中心导体的直径drod为0.65mm，配置接地转接 孔的一边长度Rsq=Dsq/2为1.66mm，信号转接孔的焊盘直径为0.95mm， 小型转接传输线路的结构参数调整用转接孔的直径dele为1.65mm，大的空 气孔的直径dal为0.5mm，小的空气孔的直径da2为0.3mm。

30 对于包含小型转接传输线路的内部连接构造的S参数的大小在15GHz 之前由实线表示。此外为了比较，对于安装在相同的印刷电路板上的转接 传输线路，具有同一参数的通常的同轴电缆的S参数由须线表示。在图16A 中，反射系数ISIII越小，传输特性越好。例如在10GHz，通常的转接传输 线路和小型转接传输线路的ISIII的差为6dB左右，但是这在线性刻度中， 5 表示小型转接传输线路的信号的反射量变为通常的转接传输线路的反射量 的一半。

此外，在图16B中，表示透过系数|S21|，但是它表示信号的损失量， 可以说越接近0，传输特性越好。在10GHz，小型转接传输线路的信号损失 为-0.3dB，在线性刻度中，为3%左右，而通常的转接传输线路的信号损失 10 为l.OdB以上，在线性刻度中，为10%。通过由仿真取得的S参数的比较， 关于信号的反射量和损失量，小型转接传输线路对于通常的转接传输线路 的优越性是明显的。

with a dielectric insulating layer and the conductor of the printed circuit board insulating material 20 different design ideas.

In the composite dielectric is formed is particularly important is to use air holes as via holes construction methods. This is because the dielectric constant and the relative permeability of air is substantially 1, so the use of air holes for the composite dielectric transmission line constituting a small adapter.

The following describes the embodiment using a small air hole is formed in the transmission line switching. 4A and 4B 25 is a plan view and a cross-sectional view, respectively, having a signal around the center conductor via holes 401 are configured to square the ground via holes 402 of the adapter compact transmission lines. In a small transmission line switching, adjusting structural parameters fill the via hole 403 of the composite insulator 404, the complex dielectric constant of the insulator 404 is smaller than that used for the printed circuit board, a conductor insulating layer of the dielectric constant of the insulating layer 405, that air holes, via holes adjustment region 403 through an insulating layer 405 is located so that the configuration parameters of the structure. Here, on a printed circuit board conductor layer configuration, and configuration of Figure IB shown in FIG. 1 and the same. Through the air hole 405 and the insulating layer 410 is formed can be provided deemed effective dielectric constant than the dielectric constant of the printed circuit board 405 smaller structural adjustment parameters via holes of the composite dielectric 4035. Structural adjustment parameters via holes 403 of the composite dielectric effective dielectric constant dependent on the volume occupied by the air holes 410, from the known theoretical and

在通常的转接传输线路中，为了减少反射量，考虑调整中心导体和接 地转接孔之间的距离，从而一边把介电常数4.2和中心转接孔导体的直径 15 drod=0.65mm保持一定，一边进行50 Q的特性阻抗匹配。如果按照所述表 达式（3)，则如果把中心导体和接地转接孔的距离增加到图6A和图6B所示的小型转接传输线路的尺寸的约1.5倍，就能实现阻抗匹配，但是通常构 造越大，在更低的频率发生高次频率的不要传播模式，所以可使用的频率 降低。如上所述，能从这些仿真结果理解在把转接传输线路小型化上，使 20 用空气孔是极有效的。

图17A是表示通过小型转接传输线路在50 Q的同轴电缆和50 Q带状线 之间传输信号时，对于安装在由12层的导体层构成的多层电路板上的通常 的转接传输线路以及本发明的小型转接传输线路的反射系数（SII参数）的 频率依存性的仿真结果的图。图17B是表示通过小型转接传输线路在50 Q 25 的同轴电缆和50 Q带状线之间传输信号时，对于安装在由12层的导体层构 成的多层电路板上的通常的转接传输线路以及本发明的小型转接传输线路 的透过系数（SII参数）的频率依存性的仿真结果的图。

小型转接传输线路和带状线如图IOA和图10所示那样安装在12层的 多层电路板上。这里，印刷电路板、信号转接孔、接地转接孔、结构参数 30调整用转接孔、小型转接传输线路、构成小型转接传输线路的空气孔的全 部尺寸与上述的仿真结果时使用的尺寸相同。此外接地转接孔和空气孔的 排列与上述时同样，但是从图IOA以及图IOB可知，一个小的空气孔从配 置带状线1011的区域除外，而设置第3导体层1011。

同轴电缆与配置在印刷电路板底面上的由第12层的导体层形成的小型 5 转接传输线路的信号转接孔连接。对于包含小型转接传输线路、同轴电缆、 带状线的内部连接构造的S参数的大小在15GHz之前由实线表示。

此外为了比较，关于具有相同的内部连接构造，只是不设置空气孔的 点上不同的转接传输线路的S参数由虚线表示。与参照

experimental results obtained. Such a structure is formed using a composite parameter adjustment via holes on the medium can be maintained while the transfer characteristic of the transmission line is not used during the air holes of the same impedance value, while the development of more compact switching transmission lines.

The expression

In a small adapter transmission lines, representing the ground via holes arranged on the circle or square on 10:00 characteristic impedance (2) to the expression (4), export the results. Air hole is formed, so that the effective dielectric constant of the composite dielectric is reduced, it can reduce the effective loss factor than the insulating layer of the printed circuit board.

By composite dielectric insulating material air holes and the printed circuit board composed of a transmission line can take a small adapter small adapter reduce transmission line cross-sectional area of the present invention. Also formed from the outer boundary of the conductor by reducing the effective dielectric constant and to 15, in a small adapter transmission line, can transmit high-order harmonic components, whereby a small adapter to expand the transmission line operating frequency range.

Air holes

mounted on a printed circuit board adapter small transmission line so that the air circulation good air cooling is good, accordingly, can improve the high-density mounting of the heat dissipation characteristics.

In a small adapter transmission lines, electromagnetic wave of the fundamental wave signal transfer between mainly in

图16A和图16B，所 述同样，从图17A以及图17B能理解通过在信号转接孔和接地转接孔之间 10 设置空气孔，改善电特性，并且实现转接传输线路的小型化。

图18A是表示通过小型转接传输线路在50 Q的同轴电缆和50 Q微波传 输带线之间传输信号时，对于安装在由12层的导体层构成的多层电路板上 的通常的转接传输线路以及本发明的小型转接传输线路的反射系数（SII参 数）的频率依存性的仿真结果的图。图18B是表示通过小型转接传输线路 15 在50Q的同轴电缆和50Q微波传输带线之间传输信号时，对于安装在由12 层的导体层构成的多层电路板上的通常的转接传输线路以及本发明的小型 转接传输线路的透过系数（SII参数）的频率依存性的仿真结果的图。

关于图18A以及图18B所示的内部连接构造的全部参数和配置与图 17A以及图17B中讨论的相同，但是不同点仅在于：把图17A以及图17B 20 的带状线置换为形成在衬底表面的第1层的50 Q的微波传输带线。对于包 含小型转接传输线路、同轴电缆、微波传输带线的内部连接构造的S参数 的大小在15GHz之前由实线表示。

此外，为了比较，关于具有相同的内部连接构造，只是不设置空气孔 的点上不同的转接传输线路的S参数由虚线表示。此外，从关于上述2个 25 内部连接构造的仿真结果取得的结论关于图18A以及图18B所示的构造也 同样。即与参照图16A、图16B、图17A和图17B所述同样，从图18A以及 图18B能理解通过在信号转接孔和接地转接孔之间设置空气孔，能改善电 特性，并且实现转接传输线路的小型化。

如上所述，在同轴电缆、引线、LSI的各管脚、平面传输线路等任何种 30 类的内部构造中使用本发明的印刷电路板用小型转接传输线路对于把印刷 电路板小型化，使形成在印刷电路板上的信号布线的工作频率范围稳定、 扩大是有效的。

作为特别的例子，通过在中心导体和小型转接传输线路的外侧导体边 界之间形成多个空气孔，用具有表的介电常数的介质材

the center of 20-hole conductor and grounding via holes constituting the outer conductor boundary structure, so the applications, not only in the air hole structural parameter adjustment region via holes can be formed in the whole area of the center conductor and the ground via holes between.

Figure 5A and 5B show an air vent is formed between the center conductor and the ground via holes, forming a semi-structural parameter adjustment via holes 503 and the printed circuit board ground plane conductor 25 of the small turn pick a plan view and a sectional view of the transmission line. Through structural parameter adjustment region via holes 503, 507 by a conductor layer composed of a conductive plate 506 in the region and the ground region between the adapter hole 502 to form an air hole 510. Small cross-section of the transmission line adapter can preclude the use of the air holes of any shape and any size, but it is necessary for the ratio of the insulating layer of the printed circuit board conductor insulating layer 505 in advance of the transmission signal wavelength A still many small, for example, KX / 8. Here, 1 is the maximum length of the cross section of the air holes 30, X is a given frequency range, the minimum wavelength of the transmission signals in the circuit board of the insulating layer.

Figures 6A and 6B is a printed circuit board and a plan view showing a circular small adapter transmission line different sized air hole of the present invention and a sectional view. In FIG. 6, respectively, and the diameter da2 dal cylindrical air holes 601 arranged in the center conductor and a ground conductor 5 outer square boundary is formed between the hole 602 adapter.

FIG. 7 is a plan view of a compact transmission line adapter of the present

料能取得与填充结 5 构参数调整用转接孔同样的效果。

该空气孔，虽然受到限制：即该空气孔的截面形状的最大长度1、应远 小于在给定频率范围内被设定为印刷电路板绝缘层中传输信号最小波长的 波长X (—般 1<V8)，但是为了实现满足小型转接传输线路的物质的要求 特性，能以任意形状进行任意的配置。

10 作为附加的结果，空气孔不仅能减少转接传输线路的信号损失，而且 能改善空冷用的空气流，据此，能改善高密度安装中的散热特性。此外， 本发明的小型转接传输线路对于安装在印刷电路板上的复杂、高密度的转 接孔构造以及用差动信号传输的转接孔构造的开发和设计，极端有效。

如果是关于印刷电路板用小型转接传输线路及其设计方法的，本发明 15 就能应用，在利用的可能性上，没有任何限定。

与几个实施例关联，说明了本发明，但是这些实施例只是列举实例说 明发明，并不意味着限定。如果读完本说明书，对于业内人士，基于等价 的构成要素和技术的很多变更和置换是容易的，但是这样的变更和置换属 于附加的权利要求书的范围和精神内。

invention is formed of a square and rectangular air hole Fig. In Figure 7, the air hole 710 of the horizontal cross-sectional shape is square and rectangular, as shown, the square and rectangle, for the different sizes. In Figure 7, although not shown in a longitudinal cross-sectional view, but a longitudinal sectional view of the same and shown in Figure 5B. I.e., the air hole 30 having a water level of 710 square cross-sectional shape as shown in FIG. 7 and the rectangular columnar structure. air hole in accordance with a given rule configuration, or may be irregularly Lopez. Figure 8 shows the rules in accordance with a predetermined configuration of small air holes 810 of the transmission line adapter specific examples. Forwarding the transmission line constituting the ground small compact switching transmission lines via holes 802 arranged circumferentially around the center conductor 801 and thus, the distance from the center conductor 801 are equal, the configuration of air holes 810, so that the center conductor 801 15 around the adjacent air holes are equidistant from each other, in addition to the distance from the center conductor 801 of the same.

FIG. 9 is a plan view showing the air hole transfer adapter compact transmission line 910 between the holes 902 are irregularly arranged on the central conductor 901 and the ground conductor constituting the outer boundary.

The method of forming a transmission line switching small air holes, taking into account the various methods using a mechanical method of forming apertures 20, formed by the laser method of hole.

Of course, in order to various internal circuit connected to the printed circuit board is used in conjunction with a small

adapter PCB transmission line, but in Fig. IOA and IOB, indicates 12 layers in a multilayer printed circuit board, the small adapter stripline transmission lines, and as a specific example of a planar transmission line bound 1011. From Fig. IOA and IOB, small transit transmission line having a center conductor 1001, with the ground 25 is set on the square of the via holes 1002, a conductor layer composed of a printed circuit board ground plane 1006, turn adjusting structural parameters jacks 1003.

Small adapter transmission lines in the composite dielectric insulating layer 1005 by a printed circuit board for the insulation of the conductor layer, based on pre-determined via holes 1002 in a small adapter of the transmission line center conductor 1001 and the ground air hole formed between different sizes of 1010 constitution. Here, four large air vent 30, the adjacent air holes are equidistant from each other, and uniformly arranged around the center conductor 1001, three small air holes between the adjacent large air holes, equal arranged around a central conductor 1001. All air holes for the strip line 1011 is configured as a horizontal axis of symmetry. Here, we can see from Figure IOA, in the region including the stripline 1011, there is no corresponding small air holes. Effective dielectric constant of the transmission line transfer small specific dielectric constant of the composite dielectric insulating layer 1005 is small, and therefore 5, 1011 while the characteristic impedance of the stripline remain the same value, while the effect that the connecting striplines 1011 the transmission line can be miniaturized.

In a specific example of the 12-story multi-layer printed circuit board, the small adapter as a transmission line and a microstrip-line planar transmission line bound in 1112 and IIB in FIG IIA. From

FIG IIA and IIB, small adapter 1101 transmission line having a center conductor, arranged on the circumference 10 connected to the via holes 1102, the conductor layer on the printed circuit board 1107 constituting the ground plate 1106, adjusting structural parameters via holes 1103.

Small forwarding by the transmission line is a composite dielectric layer 1105 for insulating the conductor layer of the printed circuit board insulation, in addition to the microstrip line 1112 disposed in the region of small irregularly switching center conductor of the transmission line 1101 air and ground transit hole hole 1102 between 1110 constitution. Small turn connected to the transmission line 15 of the effective dielectric constant than the composite dielectric permittivity of the insulating layer 1105 is small, and therefore the 1112 side microstrip characteristic impedance of the line to maintain the same value, while makes microstrip line reaches 1112 miniaturization of the transmission line.

Figure 12 shows the difference for transmitting tempted good example of a small adapter transmission line, it represents a high density via holes constructed two basic units. These two basic units constitute a signal via holes, minutes 20 respectively connected to the transmission line as an example of a plane with a transmission line pair. Forwarding the transmission line are small by the via holes 1202 by the ground surrounding the via holes of the two signals 1201, a ground plane by a conductive layer constituted by two structural parameters adjusted via holes 1203 configured. In order to divert the miniaturization of the transmission line, the transmission line and made small adapter with a characteristic impedance of the transmission line, forming an air hole 1210.

FIG. 13 shows an application example of the small transit plan view of the transmission line, i.e. SMA (sub-miniature-type-A) 25 of the connector constructed of the via holes. Conventional SMA connector pin having a signal ground via holes 1301 and via holes 1313. In FIG. 13, once again showing the connection as an example of a planar transmission line structure stripline signal via holes 1311 and 1301.

However, the usual transit transmission line produces a large loss in the high frequency radiation and omissions, as stored in the ground by switching from the hole 1313 of the higher excitation oscillation frequency range limit by 30 system.

In order to achieve a good SMA connector adapter hole configurations, the present invention is the use of small transit transmission line is very effective. In Figure 13, the transmission line having a small adapter: 1301 constituting the signal center conductor via holes, circumferentially arranged ground via holes 1302, the power board of a printed circuit board composed of a conductor layer, a conductor such as a ground plate plate structural adjustment parameters via holes 1303. In addition, through 5 over through the air holes in the insulating layer 1310, to form a composite media. determine the center conductor and the ground via holes 1301 1313 from 1310 the number of air holes and size, which contains an internal SMA connector and ribbon cable circuit, so that the characteristic impedance of the best. Moreover, in a given frequency range, mainly preclude the use of an electromagnetic wave propagates only the fundamental mode of construction. More specifically, the electric and magnetic fields is set to an electromagnetic wave propagating in the printed circuit board 10 to the

propagation direction, the vertical direction, and the spread of electric and magnetic fields orthogonal to each other. However, the spread in the actual propagation of electromagnetic waves in a printed circuit board, not only is the basic mode of the electromagnetic wave, while also containing the direction of propagation, the electric and magnetic field deviate from the vertical direction, and the electric and magnetic fields are not orthogonal to each other electromagnetic waves. In this case, the same can be applied to the present invention.

In the described embodiment, from the surface of the multilayer printed circuit board through to the back surface of the center conductor, the grounding via holes 15, the adjusting structural parameters of the via holes filled with a dielectric, but not necessarily through, and It can be formed from the surface of the center conductor to the multilayer printed circuit board into the interior of the substrate constituting the multilayer printed circuit board, the grounding via holes, via holes adjusting structural parameters, filled with a part or all of the media.

FIGS. 14A and 14B shows a printed circuit board, are arranged in the circumferential grounding adapter 20 holes 1402, 1401 are formed from the surface of the center conductor of the multilayer printed circuit board on the way to the ground via holes 1402, structure parameter adjustment 1403, a plan view of a small transit transmission line of the present invention may be filled with a dielectric 1401 and a sectional view of a via hole. In the configuration shown in FIG. 2A and 2B in the drawing, penetrates from the surface of the multilayer printed circuit board to the back surface of the center conductor 201, the ground via hole 202, the adjusting structural parameters of the via holes

203, 204 is filled with a dielectric. In the configuration diagram of the present embodiment 14A and 14B 25 shown, from the first layer to the third layer forming a central conductor 1401 most of the surface layer from the outermost layer of the first layer to form the ground layer 4 switch jacks 1402, structural parameter adjustment via holes 1403, 1404 are filled with media.

Figure 15A and 15B show respectively the transmission line switching structure parameters small air holes are formed by adjusting the area of the via holes, the center conductor 301,501 is formed, from the surface of the ground switching multilayer printed circuit board on the way to the hole 1502, structural adjustment parameter 1503, a plan view of a small air hole transfer transmission line 1510 of the present invention and a cross-sectional view of a via hole. FIG. 15A and the configuration of the present embodiment shown in FIG. 15B except for the following points, similar to the configuration shown in Fig. 4A 4B and FIG. The structure in FIG. 15A and 15B shown embodiment from the first layer to the third layer forming a central conductor 1501 most of the surface layer from the outermost layer of the first layer to the fourth layer is formed on the ground via holes 1502, the number of adjusting structural parameters 5 via holes 1503, 1510 air holes.

By forming the center conductor from the surface of the multilayer printed circuit board into the interior of a substrate constituting a printed circuit board, part or all of the via holes to ground, adjusting structural parameters of the via holes filled with the medium, further small optimized transit transmission line characteristic impedance.

In order to express the following advantages of a small adapter

transmission line, the transmission line structure in a small adapter that contains 10, description of the high-speed signal transmission several simulation results. The simulation results are shown by the difference time domain calculations (finite-difference time-domain = FDTD) method S parameter indicates the superiority of the small size of the adapter transmission line. The FDTD method represents arguably the most correct, appropriate and logical computing technique of multi-purpose internal connection circuit characteristics.

16 shows from 50 Q coaxial cable transmission line through a small adapter to other 15 50 Q coaxial cable transmission for multi-layer circuit board mounted on the conductor layer 12 is generally composed of layers forwarding the transmission line and the reflection coefficient in Fig compact transmission line switching according to the present invention (SII parameter) of the frequency dependency of the simulation results. FIG. 16B is a diagram showing the 50Q coaxial transmission line through a small adapter, to other 50Q coaxial cable transmission, the transmission line for the usual adapter installed in multi-layer circuit board by the conductive layer 12 and the layer composed of forwarding the transmission line of the present invention, a small permeability coefficient (S12 parameter) of the frequency dependency of the simulation results of FIG 20. Small switching transmission lines installed in multi-layer printed circuit board layers 12, from the center conductor to eight via holes in the ground on the square, by the power board conductor layer, then floors conductor plate 8 air holes and structural adjustment parameters for forming via holes.

Transfer on small transmission lines used in the simulation, and 12 layers of the multilayer circuit board geometric shape

25, the same as shown in FIG. 6A and 6B. Here, size 8 and center conductor to ground via holes used in the simulation are as follows. That is the diameter of the central conductor drod is 0.65mm, the configuration of the side length of the grounding via holes Rsq = Dsq / 2 is 1.66mm, signal transfer pad diameter hole is 0.95mm, the structural parameters of the transmission line switching small adjustment switch the diameter of jacks dele 1.65mm, the diameter dal large air hole is 0.5mm, the diameter da2 small air holes is 0.3mm.

Size

30 contained within a small adapter for the transmission line connection structure of S-parameters before 15GHz represented by the solid line. S-parameters generally coaxial Further For comparison, the transmission line adapter installed on the same printed circuit board, with the same parameter is represented by the whiskers. In Figure 16A, the smaller the reflection coefficient ISIII, the transmission characteristics become better. For example, in 10GHz, the difference is usually small adapter transmission lines and switching transmission line ISIII is about 6dB, but in a linear scale, 5 represents a small amount of reflection transmission line switching signal becomes normal transit transmission line half the amount of reflection.

In addition, in FIG. 16B showing permeation coefficient | S21 |, but it represents the amount of signal loss, can be said that the closer to 0, the better the transmission characteristic. At 10GHz, transmission line switching signal loss is small -0.3dB, the linear scale, about 3 percent, while the signal transmission line losses usually adapter 10 is l.OdB more, the linear scale, 10 percent. By comparing the S-parameters obtained by

the simulation, on the reflection loss and the amount of the signal, the transmission line for the transfer of small conventional transmission line switching superiority is obvious. in the conventional transmission line switching, in order to reduce the amount of reflection, considering the central conductor to adjust the distance between the via holes and the ground, so that the dielectric constant of 4.2 while the diameter of the hole and the center conductor of the adapter 15 drod = 0.65 mm constant, while performed 50 Q characteristic impedance. If in accordance with the expression (3), if the distance between the center conductor and the ground via holes increased to about 1.5 times the adapter 6A and small size of the transmission line shown in Fig. 6B, impedance matching can be achieved, However, generally the larger the structure, occurs at lower frequencies do not propagate higher frequency mode, the frequency used can be reduced. As described above, the results from these simulations understanding on the transfer of small transmission line, so that air holes 20 is extremely effective.

FIG. 17A is a transmission line through a small adapter in the transmission of signals between 50 Q and 50 Q stripline coaxial cable for multi-layer circuit board mounted on the conductor layer 12 is generally composed of layers forwarding the transmission line and the reflection coefficient in Fig compact transmission line switching according to the present invention (SII parameter) of the frequency dependency of the simulation results. 17B is a diagram showing the transmission by switching a small signal in the transmission line between the 50 Q 25 50 Q coaxial cable and the stripline, the multi-layer circuit board mounted on the conductor layer 12 is generally composed of layers of rotation permeation coefficient (SII parameters)

frequency dependence of simulation results showing the connections of a transmission line and a small adapter transmission line of the present invention.

Small adapter and stripline transmission lines in Fig. IOA and as mounted on the multilayer circuit board 12 layers in Figure 10. Here, the printed circuit board, signal via holes, the via holes to ground, adjusting structural parameters of the via hole 30, a small switching transmission lines constituting the transmission line transfer of small overall dimensions of the air holes in the above simulation results using the same size. Besides the above-described arrangement of grounding via holes and air holes in the same, but from the diagram in Fig. IOA and IOB shows that a small air hole from the area except for the configuration of the strip line 1011, and provided with a third conductive layer 1011. coaxial cable signal via holes arranged in the bottom surface of the printed circuit board by a conductive layer formed on the first layer 12 small 5-transit transmission line connection. For the small size of the internal adapter comprising a transmission line, a coaxial cable, stripline connection structure parameter S prior to 15GHz as a solid line.

Also for comparison, the internal connections on the same structure, but not a different set of S-parameters of the transmission line switching point of the air hole indicated by dashed lines. With reference to FIG. 16A and FIG. 16B, the same, from FIG. 17A and FIG. 17B can be understood by the via holes between the signal and ground via holes that air holes 10, to improve electrical characteristics, and to achieve a small switching transmission lines of.

FIG. 18A is a transmission line through a small adapter when transmitting signals between 50 Q and 50 Q coaxial

microstrip line, for the installation of the multi-layer circuit board by the conductive layer 12 composed of layers and forwarding the transmission line is generally in FIG small reflection coefficient adapter of the present invention, the transmission line (SII parameter) of the frequency dependency of the simulation results. FIG. 18B is a transmission line through a small adapter 15 when the coaxial cable for transmitting signals between 50Q and 50Q microstrip line, for the installation of the multi-layer circuit board by the conductive layer 12 is generally composed of layers of forwarding permeation coefficient (SII parameters) frequency dependence of a result of simulation and small transmission line switching transmission line of the present invention. on the same parameters and the configuration of the entire FIG. 17A and FIG. 17B, and 18A of the internal connection structure shown in Fig. 18B discussed, but the only difference is: the stripline FIG. 17A and FIG. 17B 20 is replaced by 50 Q formed in the microstrip line of the first layer of the substrate surface. For the small size of the internal adapter containing a transmission line, a coaxial cable, microstrip line connection structure parameter S prior 15GHz as a solid line.

Further, for comparison, the internal connections on the same structure, but not a different set of S-parameters of the transmission line switching point of the air hole indicated by dashed lines. In addition, two conclusions about the internal 25 of the connection structure constructed on the simulation results obtained as shown in FIG. 18A and FIG. 18B likewise. I.e., with reference to FIG. 16A, FIG. 16B, FIG. 17A and 17B of the same, from FIG. 18A and FIG. 18B can be understood by the via holes between the signal and ground via holes that air holes, can improve the electrical characteristics, and to achieve

transmission line switching miniaturization.

As described above, the printed circuit board of the present invention in any kind of internal structure of the 30 categories of coaxial cable, lead, LSI of the pin, and the like planar transmission line transmission line with a small adapter for the printed circuit board small, so that stable signal wiring formed on the printed circuit board of the operating frequency range, the expansion is valid.

As a specific example, through the boundary between the center conductor and the outer conductor of the transmission line mini adapter plurality of air holes are formed with a dielectric material having a dielectric constant can get a table filled with 5 knot configuration parameter adjustment the same effect via holes.

The air hole, despite the restrictions: the maximum length of the cross-sectional shape of the air holes 1, should be much smaller than in the given frequency range is set to be the insulating layer printed circuit board minimum wavelength of the transmission signal wavelength X (- like 1 and lt; V8), but in order to meet the requirements to achieve transfer characteristics of small transmission line material, it can be configured to any arbitrary shape.

10 As an additional result, the air holes not only reduce the signal loss transfer transmission line, but also improve the air-cooling air flow, whereby high-density mounting can improve heat dissipation characteristics. In addition, small adapter for the transmission line of the present invention is mounted on the printed circuit board complexity, high-density configuration via holes and via holes constructed with development and design of the differential signal transmission, extremely effective.

If you are on a printed circuit board using a small adapter transmission line and its design methods of the present invention 15 can apply, on the possibility of using, without any limitation.

Several embodiments associated with examples illustrate the present invention, but these examples are merely illustrative examples, explanation invention and are not meant to be limiting. If reading this specification, for the industry, based on equivalent elements and a lot of technical changes and substitutions are easy, but such changes and substitutions belong in the appended claims and spirit.

Cited by: CN101945537 A ; CN102714917 A ; CN103066040 A ; CN103066040 B ; CN103796424 A ; CN103796424 B ; CN104378912 A ; CN104937767 A ; CN104937767 B ; CN105072800 A ; CN105072800 B ; CN105263255 A ; CN105263255 B ; CN105578714 A ; CN107069354 A ; CN107205308 A ; CN107241857 A ; CN108336593 A ;

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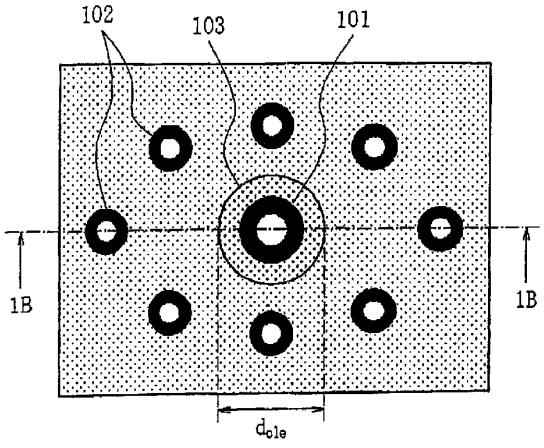
[54] 发明名称

印刷电路板用小型转接传输线路及其设计方法

[57] 摘要

一种印刷电路板用小型转接传输线路及其设计方法，包括：形成小型转接传输线路的内侧导体边界并构成转接孔的中心导体(101)；设置在中心导体的周围形成外侧导体边界的多个接地转接孔(102)；以及由印刷电路板的导体层构成的接地板。并且，在所述内侧导体边界与所述外侧导体边界之间设置结构参数调整用转接孔(103)，在信号转接孔中传播的信号与其他信号在高频信号频带被电性隔离不会产生交扰。实现了具有好的特性阻抗且包含多层印刷电路板的小型化的同时，还能扩大安装在该印刷电路板上的转接孔传输线路的频率范围。



1.一种印刷电路板用小型转接传输线路，其设置在印刷电路板上，包括：

构成所述小型转接传输线路的内侧导体边界，传递信号的中心导体；

构成所述小型转接传输线路的外侧导体边界的多个接地转接孔；

由连接在所述接地转接孔上的所述印刷电路板的导体层构成的接地板；以及

设置在所述内侧导体边界与所述外侧导体边界之间，用于调整所述印刷电路板的结构参数的结构参数调整用转接孔，

所述结构参数调整用转接孔，由具有与构成所述印刷电路板的绝缘层的第1结构参数不同的第二结构参数的一样的介质或复合介质填充。

2.根据权利要求1所述的印刷电路板用小型转接传输线路，其中：

所述印刷电路板是具有多个导体层的多层印刷电路板。

3.根据权利要求1所述的印刷电路板用小型转接传输线路，其中：

所述第1和第2结构参数是介电常数和相对导磁率中的至少任意一个。

4.根据权利要求1所述的印刷电路板用小型转接传输线路，其中：

所述小型转接传输线路，与安装在所述印刷电路板上并连接在所述小型转接传输线路上的内部连接电路取得阻抗匹配。

5.根据权利要求3所述的印刷电路板用小型转接传输线路，其中：

所述第2结构参数的值比所述第1结构参数的值小。

6.一种印刷电路板用小型转接传输线路，其设置在印刷电路板上，包括：

构成所述小型转接传输线路的内侧导体边界，传递信号的中心导体；

构成所述小型转接传输线路的外侧导体边界的多个接地转接孔；

由连接在所述接地转接孔上的所述印刷电路板的导体层构成的接地板；

设置在所述内侧导体边界与所述外侧导体边界之间，用于调整所述印

刷电路板的结构参数的结构参数调整用转接孔；以及

在所述内侧导体边界与所述外侧导体边界之间穿过所述印刷电路板而设置的空气孔。

7. 根据权利要求6所述的印刷电路板用小型转接传输线路，其中：

所述空气孔，设置在所述印刷电路板上，从而调整设置在所述印刷电路板上的转接传输线路与连接在该转接传输线路上的内部连接电路之间的特性阻抗。

8. 根据权利要求6所述的印刷电路板用小型转接传输线路，其中：

所述空气孔，至少包含由2个不同大小的圆形形状构成的所述空气孔。

9. 根据权利要求6所述的印刷电路板用小型转接传输线路，其中：

所述空气孔，不规则地配置在所述内侧导体边界与所述外侧导体边界之间。

10. 根据权利要求6所述的印刷电路板用小型转接传输线路，其中：

所述空气孔，相对于所述信号转接孔配置为对称。

11. 根据权利要求6所述的印刷电路板用小型转接传输线路，其中：

所述空气孔的截面形状的最大长度，是在所述印刷电路板的绝缘层中传播的信号的给定频率范围的最小波长的1/8以下。

12. 根据权利要求1～11中的任意一项所述的印刷电路板用小型转接传输线路，其中：

所述接地转接孔排列在圆周上。

13. 根据权利要求1～11中的任意一项所述的印刷电路板用小型转接传输线路，其中：

所述接地转接孔排列在正方形上。

14. 根据权利要求7所述的印刷电路板用小型转接传输线路，其中：

在所述印刷电路板上传播的主要电磁波的电场和磁场相对于传播方向，是垂直方向，并且电场与磁场彼此正交。

15. 一种印刷电路板用小型转接传输线路，其设置在印刷电路板上，包括：

构成小型转接传输线路的2个内侧导体边界，传播差动信号的2个中心导体；

构成分别配置在2个中心导体的周围的2个外侧导体边界的多个接地转接孔；

由连接在所述接地转接孔上的所述印刷电路板的导体层构成的接地板；以及

设置在所述2个内侧导体边界与所述2个外侧导体边界之间，用于调整所述印刷电路板的结构参数的2个结构参数调整用转接孔，

所述2个结构参数调整用转接孔，分别由具有与构成所述印刷电路板的绝缘层的第1结构参数不同的第二结构参数的一样的介质或复合介质填充。

16.一种印刷电路板用小型转接传输线路的设计方法，该印刷电路板用小型转接传输线路包括：构成设置在印刷电路板上的所述小型转接传输线路的内侧导体边界、传递信号的中心导体；构成所述小型转接传输线路的外侧导体边界的多个接地转接孔；以及由连接在所述接地转接孔上的所述印刷电路板的导体层构成的接地板，其中：

在所述内侧导体边界与所述外侧导体边界之间设置用于调整所述印刷电路板的结构参数的结构参数调整用转接孔，所述结构参数调整用转接孔，分别由具有与构成所述印刷电路板的绝缘层的第1结构参数不同的第二结构参数的一样的介质或复合介质填充。

17.根据权利要求16所述的印刷电路板用小型转接传输线路的设计方法，其中：

所述第二结构参数比所述第一结构参数小。

18.根据权利要求16所述的印刷电路板用小型转接传输线路的设计方法，其中：

所述第1和第2结构参数是介电常数和相对导磁率中的至少任意一个。

19.根据权利要求16所述的印刷电路板用小型转接传输线路的设计方法，其中：

所述小型转接传输线路，与安装在所述印刷电路板上并连接在所述小型转接传输线路上的内部连接电路取得阻抗匹配。

20.一种印刷电路板用小型转接传输线路的设计方法，该印刷电路板

用小型转接传输线路包括：构成设置在印刷电路板上的所述小型转接传输线路的内侧导体边界、传递信号的中心导体；构成所述小型转接传输线路的外侧导体边界的多个接地转接孔；以及由连接在所述接地转接孔上的所述印刷电路板的导体层构成的接地板，其中：

在所述内侧导体边界与所述外侧导体边界之间设置用于调整所述印刷电路板的结构参数的结构参数调整用转接孔，在所述内侧导体边界与所述外侧导体边界之间还形成穿过所述印刷电路板的空气孔。

21. 根据权利要求20所述的印刷电路板用小型转接传输线路的设计方法，其中：

所述空气孔，设置在所述印刷电路板上，从而调整设置在所述印刷电路板上的转接传输线路与连接在该转接传输线路上的内部连接电路之间的特性阻抗。

22. 根据权利要求21所述的印刷电路板用小型转接传输线路的设计方法，其中：

在所述印刷电路板上传播的主要电磁波的电场和磁场对于传播方向，是垂直方向，并且电场与磁场彼此正交。

23. 根据权利要求20所述的印刷电路板用小型转接传输线路的设计方法，其中：

所述空气孔的截面形状的最大长度，是在所述印刷电路板的绝缘层中传播的信号的给定频率范围的最小波长的1/8以下。

印刷电路板用小型转接传输线路及其设计方法

技术领域

本发明涉及印刷电路板用小型转接传输线路(Compact via Transmission Line)及其设计方法，特别是涉及填充构成转接传输线路的结构参数调整用转接孔(via hole)的填充用介质的结构参数与构成印刷电路板的绝缘层的结构参数不同的小型化印刷电路板用小型转接传输线路及其设计方法。

背景技术

为了更充分说明与本发明相关的当前的技术水准，通过在这里参照本申请中引用或特指的专利、专利申请、专利公报、科学论文等的全部，组入它们的全部说明。

印刷电路板的内部连接部，对于数字设备和通信用设备的高速化以及安装密度的提高是非常重要的，对这些设备的电特性带来巨大的影响。在包含多层衬底的印刷电路板中，从以往就广泛使用低成本，并且分别供给接地、电源、信号，把通过绝缘层彼此绝缘的多个导体层相互连接的内部连接技术。这些技术在微波传输带线、带状线、共面线、狭缝线等平面传输线路那样的内部连接电路的开发和设计中特别重要。

以往，提出了在多层衬底中设置与接地板连接的接地用转接孔，抑制漏入偏压图案的高频信号通过由接地板夹着的导电层产生不要传播模式。该以往技术例如在特开平9-321501号公报中记载。

此外，例如在特开平6-104601号公报中记载了在印刷电路板上由金属板、绝缘物、金属栓构成给定的阻抗的同轴线路，高频信号通过这里，从而构成给定阻抗的同轴线路，减小信号衰减的技术。

另外，在特开2001-68596号公报中记载了在四边配置用于遮蔽电磁波的转接孔，从而各转接孔彼此的间隔变为低于有效波长的1/2，不产生共振的技术。

如上述的专利公报所述，作为在垂直于印刷电路板的方向的内部连接部的代表性构造，有转接孔构造。形成在印刷电路板上的单纯的转接孔使构成印刷电路板的绝缘层中产生寄生的共振，从印刷电路板产生不要的电磁辐射。因此，如专利文献3所述，为了避免这样的不要的辐射的影响，进行把接地转接孔作为屏蔽使用的方法。

可是，关于由一个信号转接孔和接地转接孔的屏蔽所构成的复合转接传输线路要正确进行阻抗匹配，在把复合的转接传输线路小型化时是必须的，但是实情是会产生怎么也无法避免的困难的问题。

发明内容

因此，本发明的主要目的在于：实现适合于高密度安装并且具有适合的特性阻抗的小型转接传输线路，扩大包含多层印刷电路板的印刷电路板中的转接传输线路的频率范围。

本发明的其他目的在于：对于构成印刷电路板的小型转接传输线路，让把印刷电路板的导电层间绝缘的绝缘层的结构参数例如介电常数以及相对导磁率与构成小型转接传输线路的结构参数调整用转接孔的填充用介质的结构参数不同，从而实现内部连接线路和印刷电路板的小型化，并且实现所需的特性阻抗。

本发明的第1方面是一种印刷电路板用小型转接传输线路，设置在印刷电路板上，包括：构成所述小型转接传输线路的内侧导体边界，信号传递的中心导体；构成所述小型转接传输线路的外侧导体边界的多个接地转接孔；连接在所述接地转接孔上的所述印刷电路板的导体层构成的接地板；设置在所述内侧导体边界和所述外侧导体边界之间，用于调整所述印刷电路板的结构参数的结构参数调整用转接孔；所述结构参数调整用转接孔由具有与构成所述印刷电路板的绝缘层的第1结构参数不同的第二结构参数的一样的介质或复合介质填充。

所述印刷电路板是具有多个导体层的多层印刷电路板。

所述第1和第2结构参数是介电常数和相对导磁率中的至少任意一个。

所述小型转接传输线路安装在所述印刷电路板上，与连接在所述小型转接传输线路上的内部连接电路取得阻抗匹配。

所述第2结构参数的值比所述第1结构参数的值小。

所述接地转接孔排列在圆周上。此外，所述接地转接孔排列在正方形上。

本发明的第2方面是一种印刷电路板用小型转接传输线路，设置在印刷电路板上，包括：构成所述小型转接传输线路的内侧导体边界，信号传递的中心导体；构成所述小型转接传输线路的外侧导体边界的多个接地转接孔；连接在所述接地转接孔上的所述印刷电路板的导体层构成的接地板；设置在所述内侧导体边界和所述外侧导体边界之间，用于调整所述印刷电路板的结构参数的结构参数调整用转接孔；在所述内侧导体边界和所述外侧导体边界之间穿过所述印刷电路板而设置的空气孔。

所述空气孔设置在所述印刷电路板上，从而调整设置在所述印刷电路板上的转接传输线路和连接在该转接传输线路上的内部连接电路的特性阻抗。

所述空气孔至少包含由2个不同大小的圆形形状构成的所述空气孔。

所述空气孔不规则地配置在所述内侧导体边界和所述外侧导体边界之间。

所述空气孔对于所述信号转接孔配置为对称。

所述空气孔的截面形状的最大长度是在所述印刷电路板的绝缘层中传播的信号的给定频率范围的最小波长的1/8以下(在本申请文件中，“以上”、“以下”均包含本数)。

所述接地转接孔排列在圆周上。此外，所述接地转接孔排列在正方形上。

在所述印刷电路板上传播的主要电磁波的电场和磁场对于传播方向，是垂直方向，并且电场和磁场彼此正交。

本发明的第3方面是一种印刷电路板用小型转接传输线路，设置在印刷电路板上，包括：构成小型转接传输线路的2个内侧导体边界，差动信号传播的2个中心导体；构成分别配置在2个中心导体的周围的2个外侧导体边界的多个接地转接孔；由连接在所述接地转接孔上的所述印刷电路板的导体层构成的接地板；设置在所述2个内侧导体边界和所述2个外侧导体边界之间，用于调整所述印刷电路板的结构参数的2个结构参数调整

用转接孔；所述2个结构参数调整用转接孔分别由具有与构成所述印刷电路板的绝缘层的第1结构参数不同的第二结构参数的一样的介质或复合介质填充。

本发明的第4方面是一种印刷电路板用小型转接传输线路的设计方法，该印刷电路板用小型转接传输线路包括：构成所述小型转接传输线路的内侧导体边界，信号传递的中心导体；构成所述小型转接传输线路的外侧导体边界的多个接地转接孔；连接在所述接地转接孔上的所述印刷电路板的导体层构成的接地板；在所述内侧导体边界和所述外侧导体边界之间设置用于调整所述印刷电路板的结构参数的结构参数调整用转接孔，所述结构参数调整用转接孔分别由具有与构成所述印刷电路板的绝缘层的第1结构参数不同的第二结构参数的一样的介质或复合介质填充。

所述第二结构参数比所述第一结构参数小。

所述第1和第2结构参数是介电常数和相对导磁率中的至少任意一个。

所述小型转接传输线路安装在所述印刷电路板上，与连接在所述小型转接传输线路上的内部连接电路取得阻抗匹配。

本发明的第5方面是一种印刷电路板用小型转接传输线路的设计方法，该印刷电路板用小型转接传输线路包括：构成所述小型转接传输线路的内侧导体边界，信号传递的中心导体；构成所述小型转接传输线路的外侧导体边界的多个接地转接孔；连接在所述接地转接孔上的所述印刷电路板的导体层构成的接地板；在所述内侧导体边界和所述外侧导体边界之间设置用于调整所述印刷电路板的结构参数的结构参数调整用转接孔，在所述外侧导体边界之间穿过所述印刷电路板而形成空气孔。

所述空气孔设置在所述印刷电路板上，从而调整设置在所述印刷电路板上的转接传输线路和连接在该转接传输线路上的内部连接电路的特性阻抗。

在所述印刷电路板上传播的主要电磁波的电场和磁场对于传播方向，是垂直方向，并且电场和磁场彼此正交。

所述空气孔的截面形状的最大长度是在所述印刷电路板的绝缘层中传播的信号的给定频率范围的最小波长的1/8以下。

附图说明

下面简要说明附图。

图1A是在印刷电路板中表示本发明的小型转接传输线路的平面图。

图1B是在印刷电路板中表示本发明的小型转接传输线路的纵剖视图。

图2A是在印刷电路板中表示把接地转接孔配置在圆周上的本发明的小型转接传输线路的平面图。

图2B是在印刷电路板中表示把接地转接孔配置在圆周上的本发明的小型转接传输线路的纵剖视图。

图3A是在印刷电路板中表示把接地转接孔配置在正方形上的本发明的小型转接传输线路的平面图。

图3B是在印刷电路板中表示把接地转接孔配置在正方形上的本发明的小型转接传输线路的纵剖视图。

图4A是在印刷电路板中表示在小型转接传输线路的结构参数调整用转接孔的区域中形成空气孔的本发明的小型转接传输线路的平面图。

图4B是在印刷电路板中表示在小型转接传输线路的结构参数调整用转接孔的区域中形成空气孔的本发明的小型转接传输线路的纵剖视图。

图5A是在印刷电路板中表示具有形成在中心导体和接地转接孔之间的空气孔，具有结构参数调整用转接孔和形成印刷电路板的接地层的导体板的本发明的小型转接传输线路的平面图。

图5B是在印刷电路板中表示具有形成在中心导体和接地转接孔之间的空气孔，具有结构参数调整用转接孔和形成印刷电路板的接地层的导体板的本发明的小型转接传输线路的纵剖视图。

图6A是在印刷电路板中表示形成圆形并且不同大小的空气孔的本发明的小型转接传输线路的平面图。

图6B是在印刷电路板中表示形成圆形并且不同大小的空气孔的本发明的小型转接传输线路的纵剖视图。

图7是表示本发明的形成正方形以及长方形的空气孔的小型转接传输线路的平面图。

图8是表示本发明的按照预先决定的基准，配置空气孔的小型转接传

输线路的平面图。

图9是表示本发明的不规则地配置空气孔的小型转接传输线路的平面图。

图10A是在印刷电路板中表示从本发明的小型转接传输线路到带状线的传输线路的平面图。

图10B是在印刷电路板中表示从本发明的小型转接传输线路到带状线的传输线路的纵剖视图。

图11A是在印刷电路板中表示从本发明的小型转接传输线路到微波传输带线的传输线路的平面图。

图11B是在印刷电路板中表示从本发明的小型转接传输线路到微波传输带线的传输线路的纵剖视图。

图12是在印刷电路板中表示为了传输差动信号而形成小型转接传输线路，并且具有与2个带状线连接的复合转接孔构造的2个基本单元的平面图。

图13是在印刷电路板中表示形成本发明的小型转接传输线路，与带状线连接的SMA连接器的转接孔构造的平面图。

图14A是在印刷电路板中表示在圆周上配置接地转接孔，从多层印刷电路板表面到途中形成中心导体、接地转接孔、结构参数调整用转接孔、填充用介质的本发明的小型转接传输线路的平面图。

图14B是在印刷电路板中表示在圆周上配置接地转接孔，从多层印刷电路板表面到途中形成中心导体、接地转接孔、结构参数调整用转接孔、填充用介质的本发明的小型转接传输线路的纵剖视图。

图15A是表示在小型转接传输线路的结构参数调整用转接孔的区域中形成空气孔，从多层印刷电路板表面到途中形成中心导体、接地转接孔、结构参数调整用转接孔、填充用介质的本发明的小型转接传输线路的平面图。

图15B是表示在小型转接传输线路的结构参数调整用转接孔的区域中形成空气孔，从多层印刷电路板表面到途中形成中心导体、接地转接孔、结构参数调整用转接孔、填充用介质的本发明的小型转接传输线路的纵剖视图。

图16A是表示对安装在由12层的导体层构成的多层衬底上的通常的转接传输线路以及本发明的小型转接传输线路的反射系数的仿真结果的图。

图16B是表示对安装在由12层的导体层构成的多层衬底上的通常的转接传输线路以及本发明的小型转接传输线路的透过系数的仿真结果的图。

图17A是表示对安装在由12层的导体层构成的多层衬底上的通常的转接传输线路以及本发明的小型转接传输线路的反射系数的仿真结果的图。

图17B是表示对安装在由12层的导体层构成的多层衬底上的通常的转接传输线路以及本发明的小型转接传输线路的透过系数的仿真结果的图。

图18A是表示对安装在由12层的导体层构成的多层衬底上的通常的转接传输线路以及本发明的小型转接传输线路的反射系数的仿真结果的图。

图18B是表示对安装在由12层的导体层构成的多层衬底上的通常的转接传输线路以及本发明的小型转接传输线路的透过系数的仿真结果的图。

具体实施方式

下面，说明本发明实施例的概要。

本发明的小型转接传输线路具有：形成所述小型转接传输线路的内侧导体层的边界，构成信号用转接孔的中心导体；配置在中心导体的周围，形成小型转接传输线路的外侧导体边界的多个接地转接孔；由印刷电路板导体层构成的多个导体板；为了在小型转接传输线路的内侧导体层的边界传播的信号与外侧导体层的边界电位在高频信号频带中不串扰而电分离的结构参数调整用转接孔。该结构参数调整用转接孔可以由一样的物质或不同的多个物质构成的复合材料填充。作为特别的例子，有在构成信号用转接孔的中心导体与转接传输线路的接地转接孔之间形成空气孔，调整印刷电路板的结构参数的方法。

选择填充本发明的结构参数调整用转接孔的填充用介质，从而使印刷电路板小型化，并且通常把小型转接传输线路和安装在印刷电路板上并且连接在小型转接传输线路上的电路的特性阻抗匹配。通过把填充结构参数调整用转接孔的介质材料或空气孔的介电常数和导磁率的任意一方或双方的参数选择为不同，能使印刷电路板小型化，所以能提高安装密度。此外，使用本发明的转接传输线路的印刷电路板能在宽阔频带的频率下工作，所

以能传输高速的数字信号。

下面参照附图详细说明本发明实施例。

在以下的实施例中，主要关于包含一个信号转接孔的小型转接传输线路进行说明，但是本发明并不一定局限于小型转接传输线路，此外，例如像1对信号转接孔那样，对安装在印刷电路板上的小型转接传输线路的任意多个信号传输线路，也能容易应用。

复杂、高密度地配置转接孔的任意数量的小型转接传输线路能用于连接平面传输线路等任意种类的内部连接电路。此外，本发明的小型转接传输线路对于具有任意的传输线路的多层印刷电路板，也能应用。

图1A和图1B是在印刷电路板中，表示本发明的小型转接传输线路的平面图以及纵剖视图。如果参照图1A和图1B，则作为多层印刷电路板的设计例，表示形成在由10层的导体层1～10构成的多层印刷电路板上的小型转接传输线路的例子。在多层印刷电路板中，通过由绝缘层105绝缘的导体层1～10，形成接地线107、信号线108、电源线109。小型转接传输线路采用包含以下部分的结构：中心导体101、配置在中心导体101的周围的接地转接孔102、由导体层106形成的接地板106、由填充用介质104填充的直径dcle的结构参数调整用转接孔103。这里，构成信号转接孔的中心导体101传输高频信号。

为了满足小型化和与内部电路的特性阻抗匹配的双方，选择填充用介质104的结构参数例如介电常数或导磁率的一方或双方，从而与绝缘层105的结构参数不同。即从与小型转接传输线路结合的电路入射的电磁波信号的能量在该结合点，由于反射，其一部分返回，但是通过调整小型转接传输线路的尺寸、介电常数或导磁率的一方或双方的值，能极端减小反射，使信号振幅几乎不衰减，进行信号的传输。

此外，当形成转接传输线路的外侧导体边界的接地转接孔的数量多到相邻的接地转接孔之间的距离小于λ/4(λ是在给定频率范围中，印刷电路板的绝缘层的传输信号的最小波长)的程度时，能把该转接传输线路作为充分绝缘的传输线路考察。此外，包含接地转接孔的转接传输线路的外侧边界能作为基于近似连续的导体的边界考察。可以用把基于连续的导体的边界视为同轴电缆的一部分，信号波沿着该边界前进的近似计算转接传

输线路的特性阻抗。

为了说明用于把安装在印刷电路板上的转接传输线路小型化的物理基础条件，考察关于接地转接孔的几个典型的几何学形状和配置。

图2A以及图2B是在印刷电路板中，表示把接地转接孔配置在圆周上的本发明的小型转接传输线路的平面图和纵剖视图。如果参照图2A以及图2B，则除了以中心导体201为中心，在圆周上以等间隔配置接地转接孔202的点，与图1A以及图1B所示的构造同样。如果为了使印刷电路板中使用的导体层彼此绝缘而使用的绝缘层205与结构参数调整用转接孔203的填充用介质204相同，则转接传输线路的特性阻抗能用信号波在圆周上的连续的内侧导体边界和外侧导体边界之间前进时使用的众所周知的以下的表达式(1)近似。

$$Z_r \approx 60 \cdot \sqrt{\frac{1}{\varepsilon}} \cdot \ln\left(\frac{R_r}{r_{rod}}\right) \cdots (1)$$

这里，Zr是小型转接传输线路的特性阻抗，Rr＝Dr/2是中心导体的中心和构成外侧导体边界的接地转接孔之间的距离，rrod＝drod/2是中心导体的半径，ε是绝缘层205的介电常数，绝缘层205的介电常数为1。

在本发明的小型转接传输线路中，填充直径dcle的结构参数调整用转接孔203的填充用介质204的介电常数必须与构成印刷电路板的绝缘层205的介电常数不同。

因此，这时，通过由填充结构参数调整用转接孔203的填充用介质204的介电常数、印刷电路板的绝缘层205的介电常数双方决定的有效介电常数计算安装在印刷电路板上的转接传输线路的特性阻抗。

该有效介电常数由已知的逻辑和实验的方法求出。如果填充在小型转接传输线路的结构参数调整用转接孔中的填充用介质204的介电常数比绝缘层205的介电常数还小时，转接传输线路的有效介电常数比绝缘层205的介电常数还小。

据此，当比较填充用介质204和绝缘层205的材料相同的转接传输线路、所述本发明的小型转接传输线路时，2个转接传输线路的特性阻抗相等，

并且填充结构参数调整用转接孔的填充用介质以外的参数相等，本发明的小型转接传输线路的截面积比以往的填充用介质204和绝缘层205的材料相同的转接传输线路的截面积小。

从以上可知，在圆周上配置图2A以及图2B所示的接地转接孔202的小型转接传输线路的特性阻抗由以下的表达式(2)表示。

$$Z_{CVT,r} \approx 60 \cdot \sqrt{\frac{1}{\varepsilon_{eff}}} \cdot \ln\left(\frac{R_r}{r_{rod}}\right) - - - (2)$$

这里，ZCVT，r是小型转接传输线路的特性阻抗，εeff是从绝缘层205和填充结构参数调整用转接孔的填充用介质204的双方决定的有效介电常数。

从表达式(2)可知，如果填充结构参数调整用转接孔的填充用介质的介电常数减小，则有效介电常数减小，为了把特性阻抗保持一定，例如50Ω，距离Rr必然减小。该事实提供用于开发小型转接传输线路的设计方针。为了实现印刷电路板的转接传输线路的小型化，重要的是进行选择，从而使填充结构参数调整用转接孔的绝缘层的介电常数比把印刷电路板的导体层绝缘的绝缘材料的介电常数还小。

图3A和图3B是表示为了接地转接孔302分别包围中心导体301而配置为正方形的印刷电路板中小型转接传输线路的平面图和剖视图。为了简化说明，与图1A以及图1B同样，表示为小型转接传输线路嵌入印刷电路板中。

如果构成小型转接传输线路的直径dcle的结构参数调整用转接孔303由与把印刷电路板的导体层绝缘的绝缘层相同的材料填充时，转接传输线路的特性阻抗能由信号波在正方形的连续的内侧导体边界和外侧导体边界之间前进时使用的众所周知的以下表达式(3)近似。

$$Z_{sq} \approx 60 \cdot \sqrt{\frac{1}{\varepsilon}} \cdot \ln\left(\frac{1.0787 \cdot R_{sq}}{r_{rod}}\right) - - - (3)$$

这里，Zsq是小型转接传输线路的特性阻抗，Rsq＝Dsq/2是中心导体的

中心和构成外侧导体边界的接地转接孔中离中心导体最近的接地转接孔之间的距离，rrod＝drod/2是中心导体的半径，ε是绝缘层205的介电常数，绝缘层305的介电常数为1。

为了在印刷电路板上形成小型转接传输线路，重要的是使填充结构参数调整用转接孔303的填充用介质304的介电常数比把印刷电路板的导体层绝缘的绝缘层305的介电常数小，这时，把图3A以及图3B所示的接地转接孔配置在正方形上的小型转接传输线路的特性阻抗由以下的表达式(4)表示。

$$Z_{CVT,r} \approx 60 \cdot \sqrt{\frac{1}{\varepsilon_{eff}}} \cdot \ln\left(\frac{1.0787 \cdot R_{sq}}{r_{rod}}\right) \text{---} (4)$$

这里，ZCVT，r是小型转接传输线路的特性阻抗，εeff是从绝缘层305和填充结构参数调整用转接孔的填充用介质304的双方决定的有效介电常数。

来自对使用配置在正方形上的接地转接孔的小型转接传输线路的考察的结论与从使用配置在圆周上的接地转接孔的小型转接传输线路的考察取得的结论是同样的。即通过减小填充结构参数调整用转接孔的填充用介质的介电常数，能把小型转接传输线路小型化。上述的2个实施例是基于包围构成信号转接孔的中心导体而形成接地转接孔，并且使填充结构参数调整用转接孔的填充用介质与把印刷电路板的导体层绝缘的绝缘材料不同的设计思想。

在形成复合介质上特别重要的方法是使用空气孔作为转接孔构造的方法。这是因为空气的介电常数和相对导磁率实质上为1，所以使用空气孔的复合介质适合构成小型转接传输线路。

下面说明使用空气孔形成小型转接传输线路的实施例。图4A和图4B是表示具有分别在构成信号转接孔的中心导体401的周围配置为正方形的接地转接孔402的小型转接传输线路的平面图以及剖视图。在小型转接传输线路中，填充结构参数调整用转接孔403的复合绝缘体404中，复合绝缘体404的介电常数比用于把印刷电路板的导体层绝缘的绝缘层405的介

电常数小，设置空气孔，从而在构造上穿过位于结构参数调整用转接孔403的区域的绝缘层405。这里，关于印刷电路板的导体层配置，与图1以及图1B所示的构造同样。穿过绝缘层405而设置的空气孔410形成能视为有效介电常数比印刷电路板405的介电常数还小的结构参数调整用转接孔403的复合介质。结构参数调整用转接孔403的复合介质的有效介电常数依存于由空气孔410占有的体积，能从已知的理论和实验结果求出。使用形成这样的结构参数调整用转接孔上的复合介质，能一边保持与不使用空气孔时的转接传输线路的特性阻抗相同的值，一边开发更小型的转接传输线路。在小型转接传输线路中，使用表示把接地转接孔配置在圆周上或正方形上时的特性阻抗的所述表达式(2)～表达式(4)，导出该结论。形成空气孔，使复合介质的有效介电常数减小，能比印刷电路板的绝缘层减小有效损失系数。

通过由空气孔和印刷电路板的绝缘材料构成的复合介质，能够乘减小小型转接传输线路的截面积的本发明的小型转接传输线路。此外通过减小有效介电常数和到形成外侧导体边界的距离，在小型转接传输线路中，能传输高次的谐波成分，据此，能扩大小型转接传输线路的工作频率范围。安装在印刷电路板上的小型转接传输线路的空气孔使空冷时的空气循环良好，据此，能改善高密度安装中的散热特性。

在小型转接传输线路中，电磁波中的基本波主要存在于构成信号转接孔的中心导体和构成外侧导体边界的接地转接孔之间，所以在应用上，空气孔不仅在结构参数调整用转接孔的区域，能在中心导体和接地转接孔之间的全部区域中形成。

图5A以及图5B是表示具有形成在中心导体和接地转接孔之间的空气孔，具有形成结构参数调整用转接孔503和印刷电路板的接地层的导体半的小型转接传输线路的平面图和剖视图。穿过结构参数调整用转接孔503的区域、由导体层507构成的导电板506而在该区域和接地转接孔502之间的区域形成空气孔510。小型转接传输线路的空气孔的截面能采用任意形状和任意尺寸，但是有必要比在用于把印刷电路板的导体层的绝缘的绝缘层505中前进的传输信号的波长λ还小很多，例如为$l < \lambda/8$。这里，l是空气孔的截面的最大长度，λ是在给定的频率范围中，电路板的绝缘层的

中的传输信号的最小波长。

图6A和图6B是在印刷电路板中表示形成圆形并且不同大小的空气孔的本发明的小型转接传输线路的平面图和剖视图。在图6中，分别直径da1和da2的圆柱状空气孔配置在中心导体601和用于形成正方形的外侧导体边界的接地转接孔602之间。

图7是表示本发明的形成正方形以及长方形的空气孔的小型转接传输线路的平面图。在图7中，空气孔710的水平截面形状为正方形以及长方形，如图所示，在正方形以及长方形中，为不同的大小。在图7中，虽然未表示纵剖视图，但是与图5B所示的纵剖视图同样。即空气孔710具有水平截面形状为图7所示的正方形以及长方形的柱状的构造。

空气孔按照给定的规则配置，或者也可以不规则地佩兹。图8表示按照预先决定的规则配置空气孔810的小型转接传输线路的具体例。构成小型转接传输线路的小型转接传输线路的接地转接孔802配置在圆周上，从而在中心导体801的周围，离中心导体801的距离相等，配置空气孔810，从而在中心导体801的周围，相邻的空气孔彼此的距离相等，此外离中心导体801的距离相等。

图9是表示在中心导体901和构成外侧导体边界的接地转接孔902之间不规则地配置空气孔910的小型转接传输线路的平面图。

作为小型转接传输线路的空气孔的形成方法，考虑到用机械形成孔的方法、由激光形成孔的方法等各种方法。

当然为了把印刷电路板的各种内部连接电路结合而使用印刷电路板用小型转接传输线路，但是在图10A和图10B中，表示在12层的多层印刷电路板中，把小型转接传输线路和作为带状线1011的平面传输线路结合的具体例。从图10A和图10B可知，小型转接传输线路具有中心导体1001、配置在正方形上的接地转接孔1002、由构成印刷电路板的导体层构成的接地板1006、结构参数调整用转接孔1003。

小型转接传输线路中的复合介质由用于把印刷电路板的导体层绝缘的绝缘层1005、根据预先决定的规则在小型转接传输线路的中心导体1001和接地转接孔1002之间形成不同尺寸的空气孔1010构成。这里，4个大的空气孔中，相邻的空气孔彼此的距离相等，并且均等地配置在中心导体1001

的周围，3个小的空气孔在相邻的大的空气孔之间，均等地配置在中心导体1001的周围。全部空气孔对于带状线1011的水平轴配置为对称。这里，从图10A可知，在包含带状线1011的区域中，不存在对应的小的空气孔。小型转接传输线路的复合介质的有效介电常数比绝缘层1005的介电常数小，因此，一边把带状线1011的特性阻抗保持相同的值，一边能使连接在带状线1011上的传输线路小型化。

在图11A和图11B中表示在12层的多层印刷电路板中，把小型转接传输线路和作为微波传输带线1112的平面传输线路结合的具体例。从图11A和图11B可知，小型转接传输线路具有中心导体1101、配置在圆周上的接地转接孔1102、由构成印刷电路板的导体层1107构成的接地板1106、结构参数调整用转接孔1103。

小型转接传输线路的复合介质由用于把印刷电路板的导体层绝缘的绝缘层1105、除了微波传输带线1112的区域而不规则地配置在小型转接传输线路的中心导体1101和接地转接孔1102之间的空气孔1110构成。小型转接传输线路的复合介质的有效介电常数比绝缘层1105的介电常数小，因此一边把微波传输带线1112的特性阻抗保持相同的值，一边能使到达微波传输带线1112的传输线路小型化。

图12表示用于传输差动心好的小型转接传输线路的一例，表示具有高密度转接孔构造的2个基本单元。这2个基本单元构成信号转接孔对，分别连接在作为平面传输线路的一例的带传输线路对上。小型转接传输线路由分别由接地转接孔1202包围的2个信号转接孔1201、由导体层构成的接地层、2个结构参数调整用转接孔1203构成。为了把转接传输线路小型化、取得小型转接传输线路和带传输线路对的特性阻抗匹配，形成空气孔1210。

图13是表示小型转接传输线路的应用例即SMA(sub-miniature-type-A)连接器的转接孔构造的平面图。通常的SMA连接器的管脚具有信号转接孔1301和接地转接孔1313。在图13中，再度表示作为平面传输线路构造的一例的带状线1311和信号转接孔1301的连接。

可是，通常的转接传输线路在高频产生大的辐射和遗漏损失，由于依存于与接地转接孔1313的距离的高次的激励振荡，受到工作频率范围的限制。

为了实现SMA连接器的良好的转接孔构造，使用本发明的小型转接传输线路非常有效。在图13中，小型转接传输线路具有：构成信号转接孔的中心导体1301、配置在圆周上的接地转接孔1302、由印刷电路板的导体层构成的电源板、接地板等导体板、结构参数调整用转接孔1303。此外，通过在绝缘层穿过空气孔1310，形成复合介质。

决定中心导体1301和接地转接孔1313的距离、空气孔1310的数量和大小，从而在包含SMA连接器和带状线的内部连接电路中，使特性阻抗最佳化。而且，在给定的频率范围中，主要采用只传播基本模式的电磁波的构造。更具体而言，设定为在印刷电路板中传播的电磁波的电场和磁场对于传播方向，是垂直方向，并且电场和磁场彼此正交传播。可是，在传播实际的印刷电路板中传播的电磁波中，不仅是所述基本模式的电磁波，同时也包含对于传播方向，电场和磁场从垂直方向偏离，并且电场和磁场彼此不正交的电磁波。这时，同样能应用本发明。

在所述实施例中，从多层印刷电路板的表面贯通到背面设置中心导体、接地转接孔、结构参数调整用转接孔、填充用介质，但是不一定要贯通，也可以从多层印刷电路板的表面到到构成多层印刷电路板的内部衬底形成中心导体、接地转接孔、结构参数调整用转接孔、填充用介质的一部分或全部。

图14A和图14B是表示在印刷电路板中，分别在圆周上配置接地转接孔1402，从多层印刷电路板的表面到途中形成中心导体1401、接地转接孔1402、结构参数调整用转接孔1403、填充用介质1401的本发明的小型转接传输线路的平面图和剖视图。在所述图2A和图2B所示的构造中，从多层印刷电路板的表面贯通到背面形成中心导体201、接地转接孔202、结构参数调整用转接孔203、填充用介质204。而在本实施例的图14A和图14B所示的构造中，从最表面层的第1层到第3层形成中心导体1401，从最表面层的第1层到第4层形成接地转接孔1402、结构参数调整用转接孔1403、填充用介质1404。

图15A和图15B是表示分别在小型转接传输线路的结构参数调整用转接孔的区域形成空气孔，从多层印刷电路板的表面到途中形成中心导体1501、接地转接孔1502、结构参数调整用转接孔1503、空气孔1510的本

发明的小型转接传输线路的平面图和剖视图。图15A和图15B所示的本实施例的构造除了以下的点，与所述图4A和图4B所示的构造类似。在图15A和图15B所示的本实施例的构造中，从最表面层的第1层到第3层形成中心导体1501，从最表面层的第1层到第4层形成接地转接孔1502、结构参数调整用转接孔1503、空气孔1510。

通过这样从多层印刷电路板的表面到构成印刷电路板的内部的衬底形成中心导体、接地转接孔、结构参数调整用转接孔、填充用介质的一部分或全部，能进一步最优化小型转接传输线路的特性阻抗。

下面为了表示小型转接传输线路的优越性，在包含小型转接传输线路的构造中，说明关于高速信号传输的几个仿真结果。仿真结果表示通过由差分时间区域(finite-difference time-domain＝FDTD)法计算的S参数的大小表示小型转接传输线路的优越性。该FDTD法在表示内部连接电路的特征时可以说是最正确、恰当并且多目的的逻辑计算手法。

图16是表示从50Ω的同轴电缆通过小型转接传输线路向其他50Ω的同轴电缆传输时，对于安装在由12层的导体层构成的多层电路板上的通常的转接传输线路以及本发明的小型转接传输线路的反射系数(S11参数)的频率依存性的仿真结果的图。图16B是表示从50Ω的同轴电缆通过小型转接传输线路向其他50Ω的同轴电缆传输时，对于安装在由12层的导体层构成的多层电路板上的通常的转接传输线路以及本发明的小型转接传输线路的透过系数(S12参数)的频率依存性的仿真结果的图。小型转接传输线路安装在12层的多层印刷电路板上，由中心导体、配置在正方形上的8个接地转接孔、由导体层构成的电源板、接地板等导体板、8个空气孔和结构参数调整用转接孔形成。

关于仿真中使用的小型转接传输线路和12层的多层电路板的几何形状，与图6A和图6B所示相同。这里，仿真中使用的中心导体和8个接地转接孔的大小如下所述。即中心导体的直径drod为0.65mm，配置接地转接孔的一边长度Rsq＝Dsq/2为1.66mm，信号转接孔的焊盘直径为0.95mm，小型转接传输线路的结构参数调整用转接孔的直径dcle为1.65mm，大的空气孔的直径da1为0.5mm，小的空气孔的直径da2为0.3mm。

对于包含小型转接传输线路的内部连接构造的S参数的大小在15GHz

之前由实线表示。此外为了比较，对于安装在相同的印刷电路板上的转接传输线路，具有同一参数的通常的同轴电缆的S参数由须线表示。在图16A中，反射系数|S11|越小，传输特性越好。例如在10GHz，通常的转接传输线路和小型转接传输线路的|S11|的差为6dB左右，但是这在线性刻度中，表示小型转接传输线路的信号的反射量变为通常的转接传输线路的反射量的一半。

此外，在图16B中，表示透过系数|S21|，但是它表示信号的损失量，可以说越接近0，传输特性越好。在10GHz，小型转接传输线路的信号损失为-0.3dB，在线性刻度中，为3％左右，而通常的转接传输线路的信号损失为1.0dB以上，在线性刻度中，为10％。通过由仿真取得的S参数的比较，关于信号的反射量和损失量，小型转接传输线路对于通常的转接传输线路的优越性是明显的。

在通常的转接传输线路中，为了减少反射量，考虑调整中心导体和接地转接孔之间的距离，从而一边把介电常数4.2和中心转接孔导体的直径drod＝0.65mm保持一定，一边进行50Ω的特性阻抗匹配。如果按照所述表达式(3)，则如果把中心导体和接地转接孔的距离增加到图6A和图6B所示的小型转接传输线路的尺寸的约1.5倍，就能实现阻抗匹配，但是通常构造越大，在更低的频率发生高次频率的不要传播模式，所以可使用的频率降低。如上所述，能从这些仿真结果理解在把转接传输线路小型化上，使用空气孔是极有效的。

图17A是表示通过小型转接传输线路在50Ω的同轴电缆和50Ω带状线之间传输信号时，对于安装在由12层的导体层构成的多层电路板上的通常的转接传输线路以及本发明的小型转接传输线路的反射系数(S11参数)的频率依存性的仿真结果的图。图17B是表示通过小型转接传输线路在50Ω的同轴电缆和50Ω带状线之间传输信号时，对于安装在由12层的导体层构成的多层电路板上的通常的转接传输线路以及本发明的小型转接传输线路的透过系数(S11参数)的频率依存性的仿真结果的图。

小型转接传输线路和带状线如图10A和图10所示那样安装在12层的多层电路板上。这里，印刷电路板、信号转接孔、接地转接孔、结构参数调整用转接孔、小型转接传输线路、构成小型转接传输线路的空气孔的全

部尺寸与上述的仿真结果时使用的尺寸相同。此外接地转接孔和空气孔的排列与上述时同样，但是从图10A以及图10B可知，一个小的空气孔从配置带状线1011的区域除外，而设置第3导体层1011。

同轴电缆与配置在印刷电路板底面上的由第12层的导体层形成的小型转接传输线路的信号转接孔连接。对于包含小型转接传输线路、同轴电缆、带状线的内部连接构造的S参数的大小在15GHz之前由实线表示。

此外为了比较，关于具有相同的内部连接构造，只是不设置空气孔的点上不同的转接传输线路的S参数由虚线表示。与参照图16A和图16B，所述同样，从图17A以及图17B能理解通过在信号转接孔和接地转接孔之间设置空气孔，改善电特性，并且实现转接传输线路的小型化。

图18A是表示通过小型转接传输线路在50Ω的同轴电缆和50Ω微波传输带线之间传输信号时，对于安装在由12层的导体层构成的多层电路板上的通常的转接传输线路以及本发明的小型转接传输线路的反射系数(S11参数)的频率依存性的仿真结果的图。图18B是表示通过小型转接传输线路在50Ω的同轴电缆和50Ω微波传输带线之间传输信号时，对于安装在由12层的导体层构成的多层电路板上的通常的转接传输线路以及本发明的小型转接传输线路的透过系数(S11参数)的频率依存性的仿真结果的图。

关于图18A以及图18B所示的内部连接构造的全部参数和配置与图17A以及图17B中讨论的相同，但是不同点仅在于：把图17A以及图17B的带状线置换为形成在衬底表面的第1层的50Ω的微波传输带线。对于包含小型转接传输线路、同轴电缆、微波传输带线的内部连接构造的S参数的大小在15GHz之前由实线表示。

此外，为了比较，关于具有相同的内部连接构造，只是不设置空气孔的点上不同的转接传输线路的S参数由虚线表示。此外，从关于上述2个内部连接构造的仿真结果取得的结论关于图18A以及图18B所示的构造也同样。即与参照图16A、图16B、图17A和图17B所述同样，从图18A以及图18B能理解通过在信号转接孔和接地转接孔之间设置空气孔，能改善电特性，并且实现转接传输线路的小型化。

如上所述，在同轴电缆、引线、LSI的各管脚、平面传输线路等任何种类的内部构造中使用本发明的印刷电路板用小型转接传输线路对于把印刷

电路板小型化，使形成在印刷电路板上的信号布线的工作频率范围稳定、扩大是有效的。

作为特别的例子，通过在中心导体和小型转接传输线路的外侧导体边界之间形成多个空气孔，用具有表的介电常数的介质材料能取得与填充结构参数调整用转接孔同样的效果。

该空气孔，虽然受到限制：即该空气孔的截面形状的最大长度1、应远小于在给定频率范围内被设定为印刷电路板绝缘层中传输信号最小波长的波长λ(一般1＜λ/8)，但是为了实现满足小型转接传输线路的物质的要求特性，能以任意形状进行任意的配置。

作为附加的结果，空气孔不仅能减少转接传输线路的信号损失，而且能改善空冷用的空气流，据此，能改善高密度安装中的散热特性。此外，本发明的小型转接传输线路对于安装在印刷电路板上的复杂、高密度的转接孔构造以及用差动信号传输的转接孔构造的开发和设计，极端有效。

如果是关于印刷电路板用小型转接传输线路及其设计方法的，本发明就能应用，在利用的可能性上，没有任何限定。

与几个实施例关联，说明了本发明，但是这些实施例只是列举实例说明发明，并不意味着限定。如果读完本说明书，对于业内人士，基于等价的构成要素和技术的很多变更和置换是容易的，但是这样的变更和置换属于附加的权利要求书的范围和精神内。

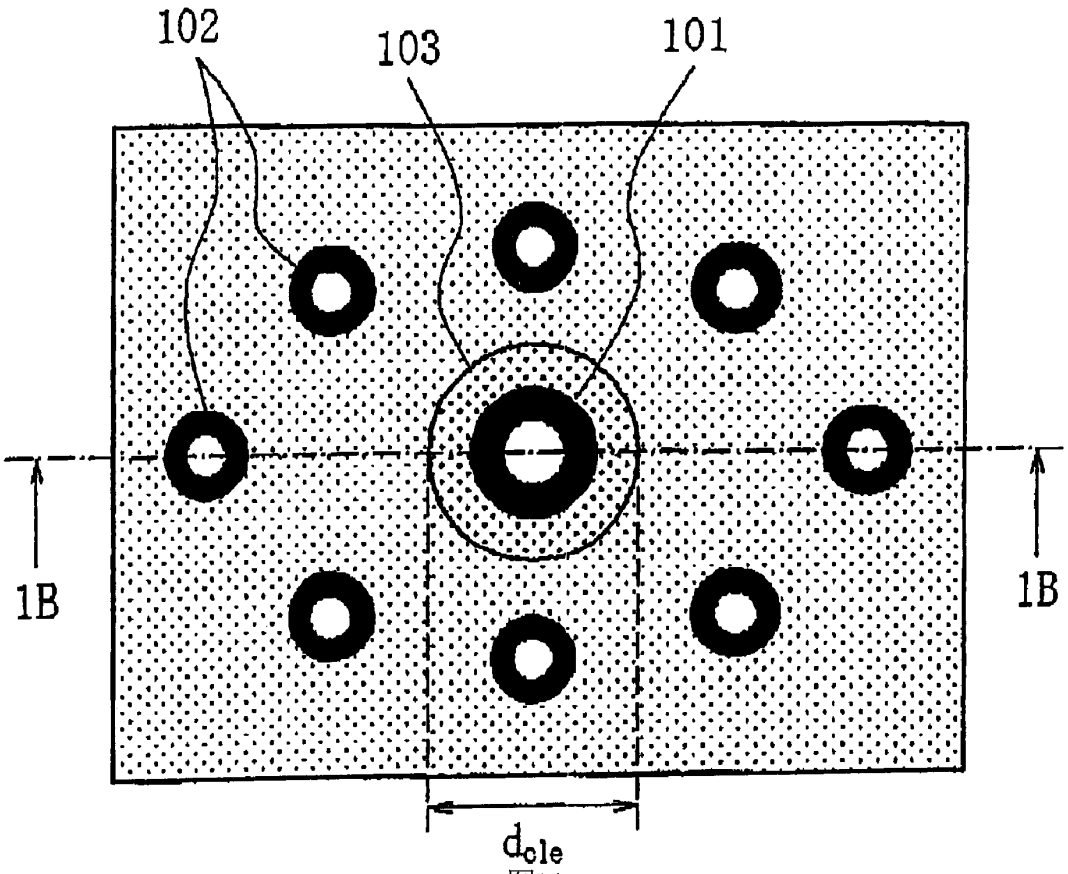


图1A

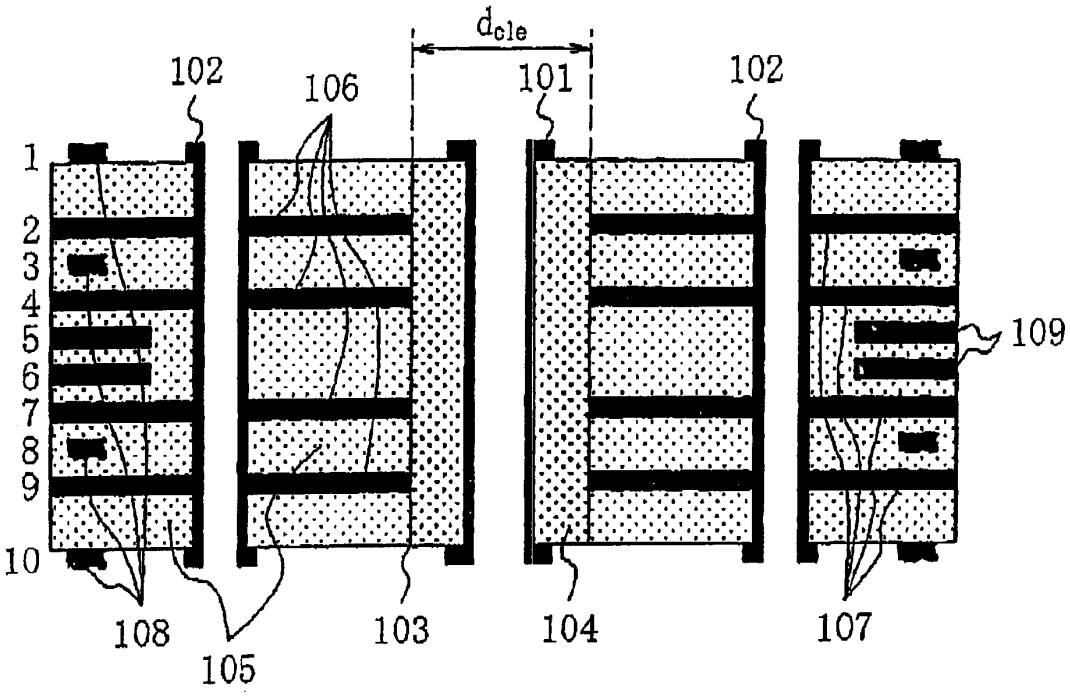


图1B

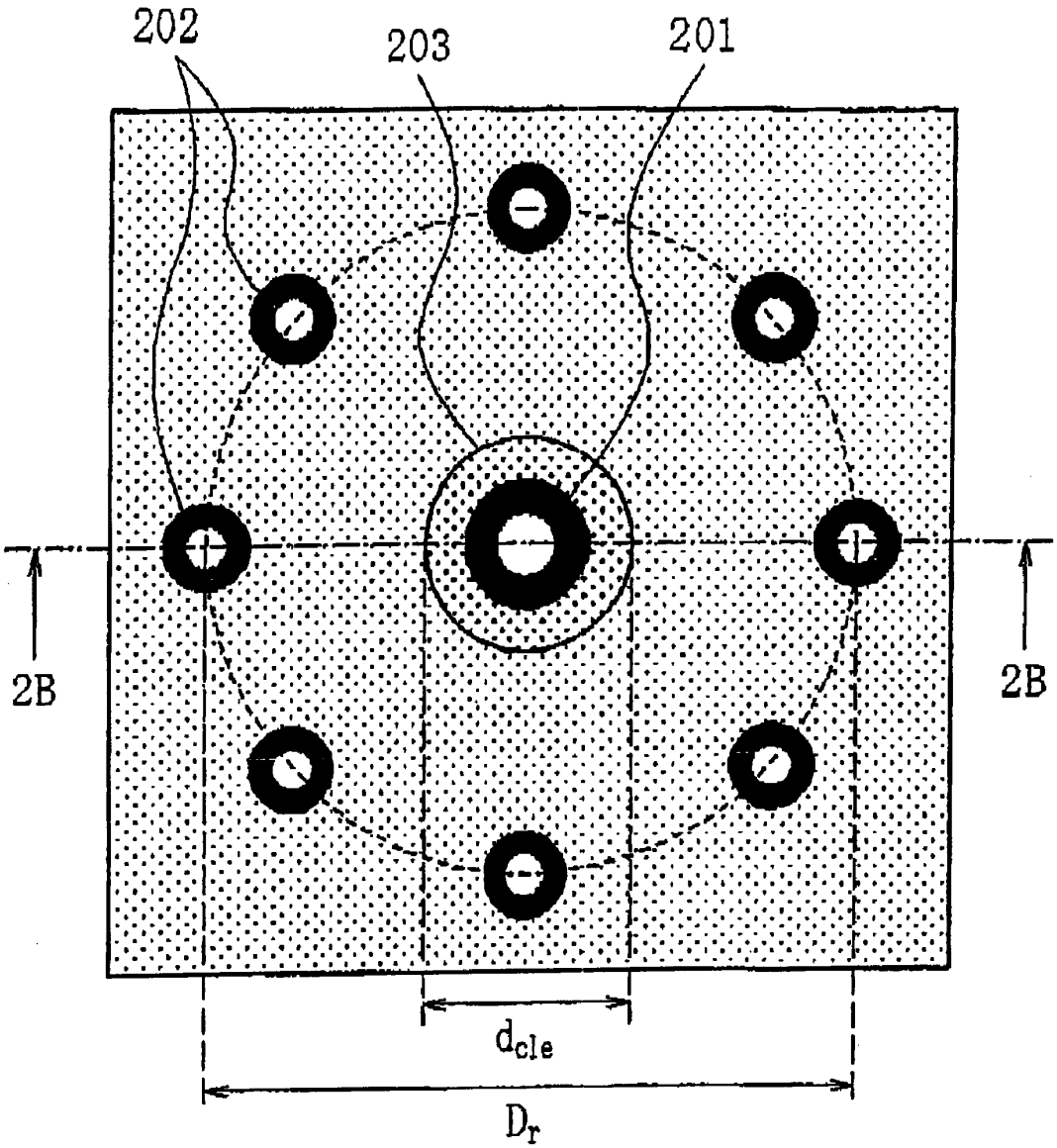


图2A

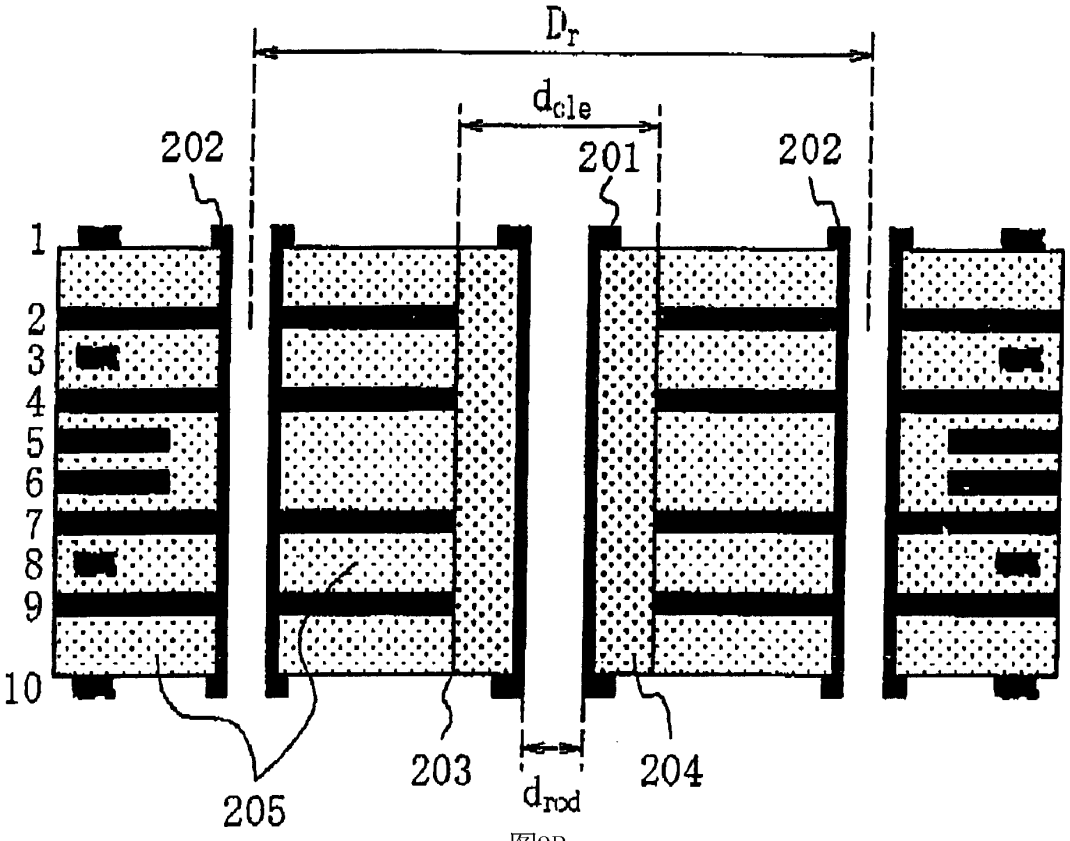


图2B

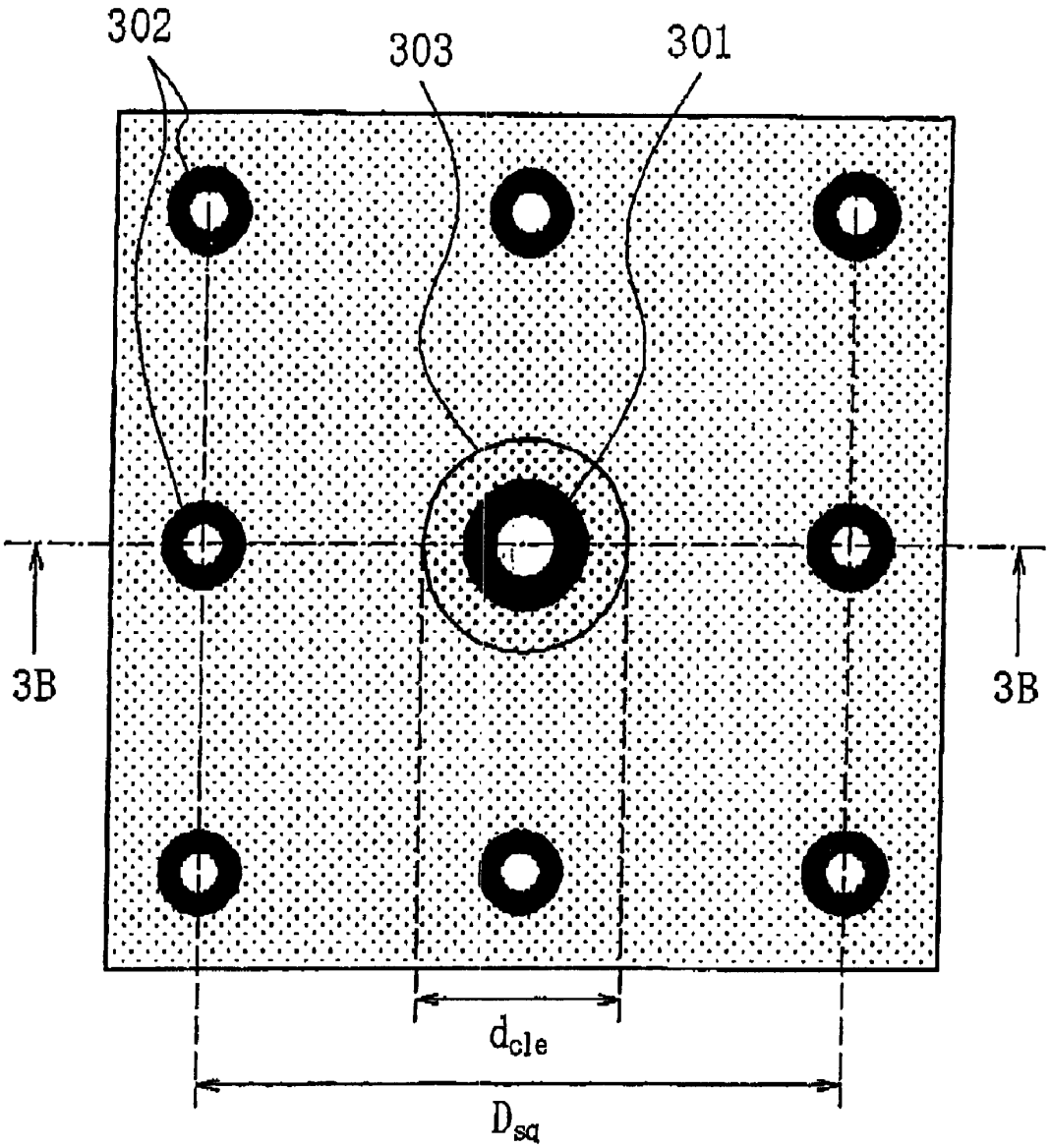


图3A

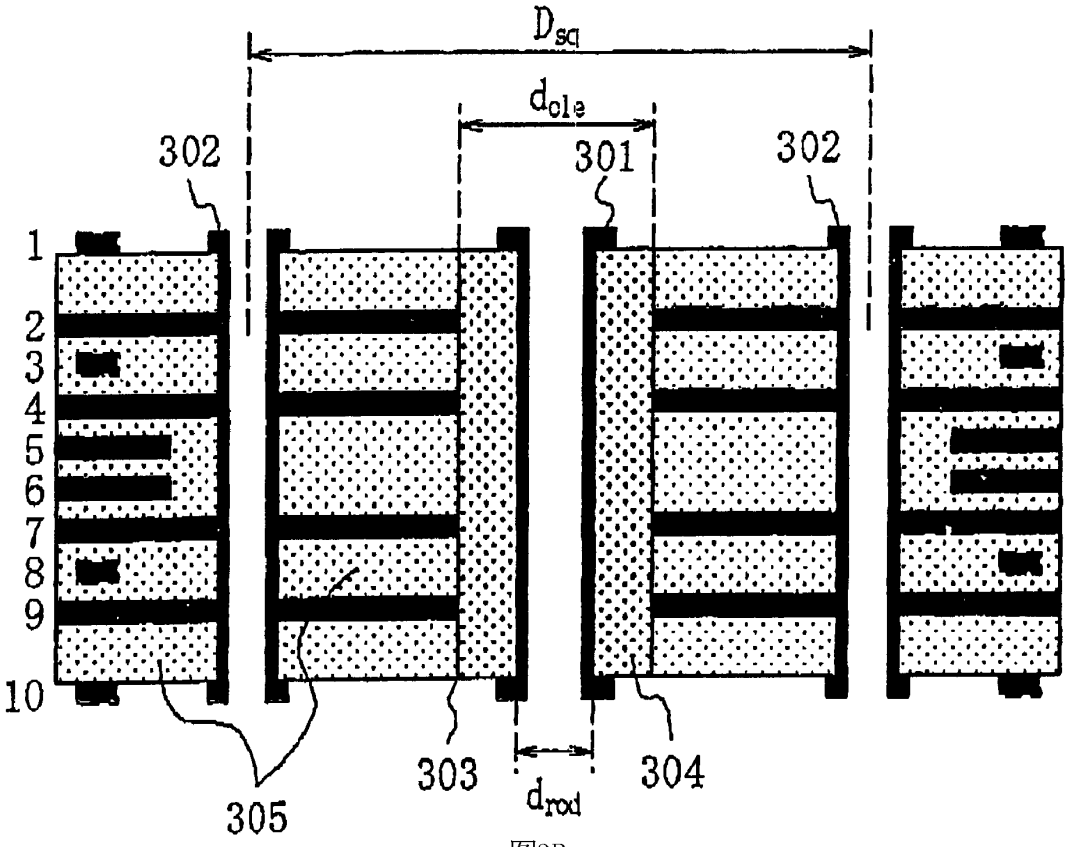


图3B

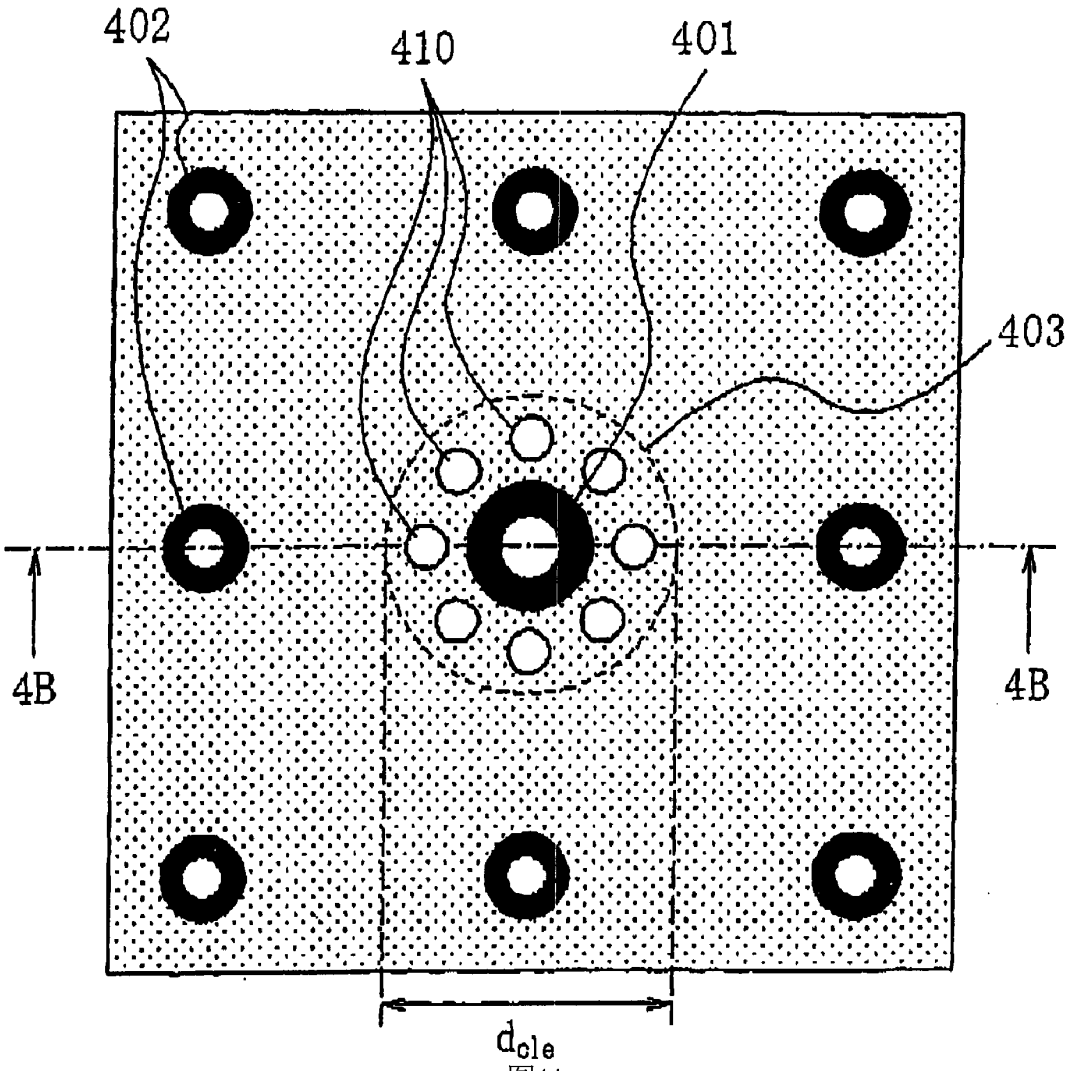


图4A

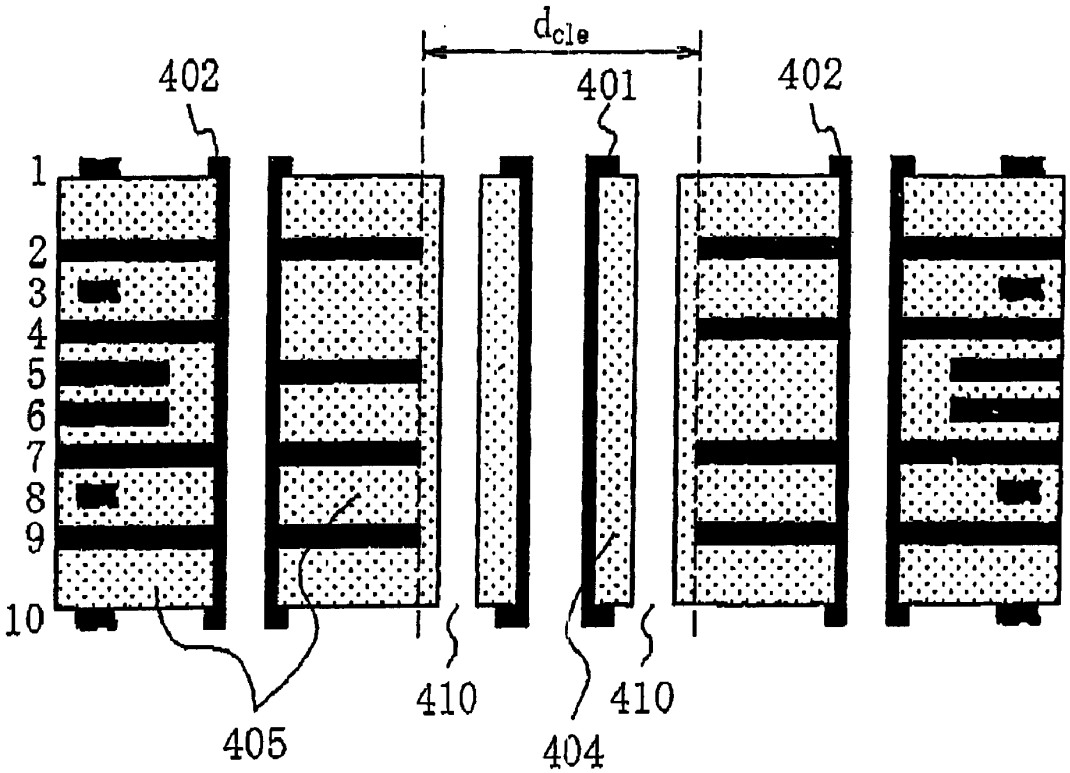


图4B

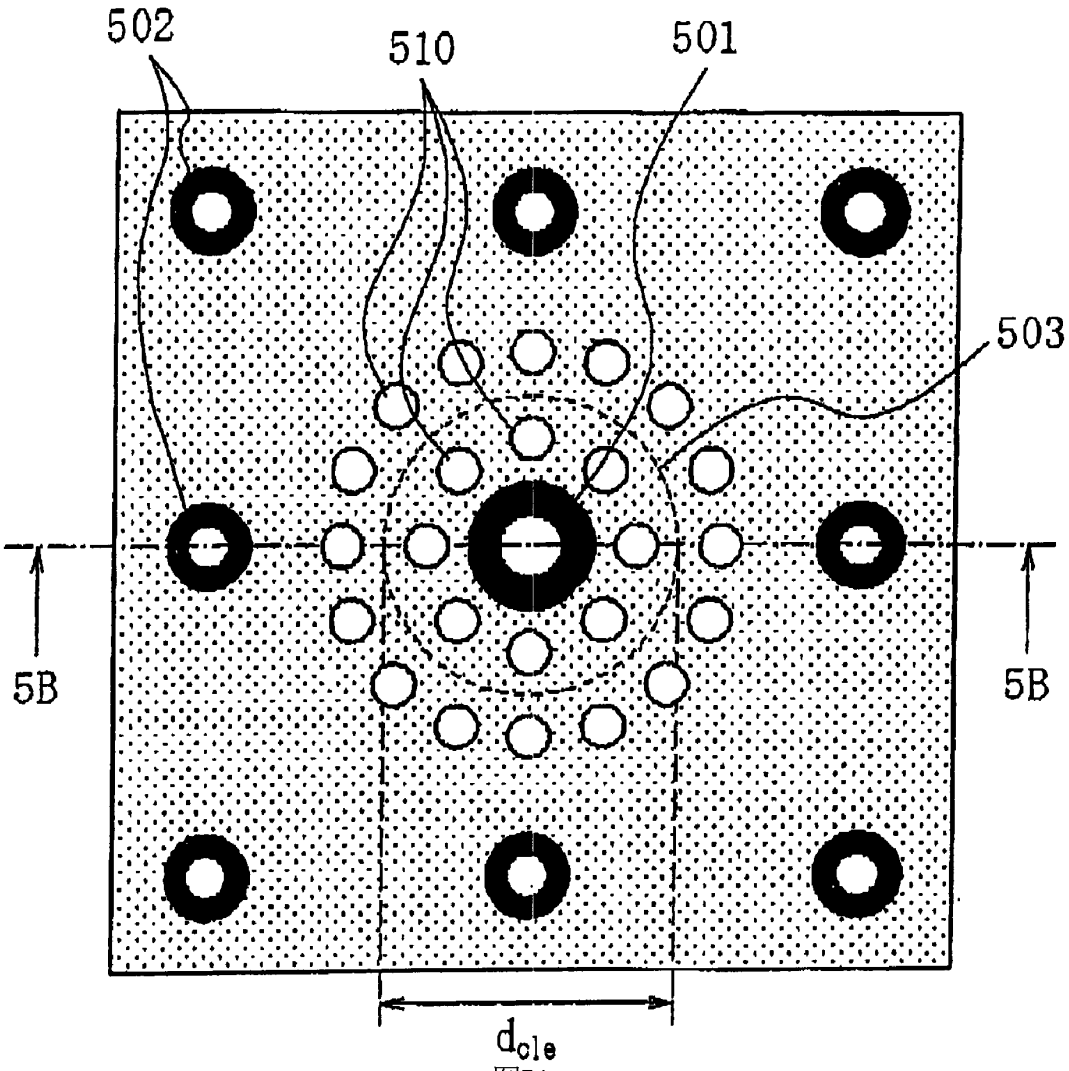


图5A

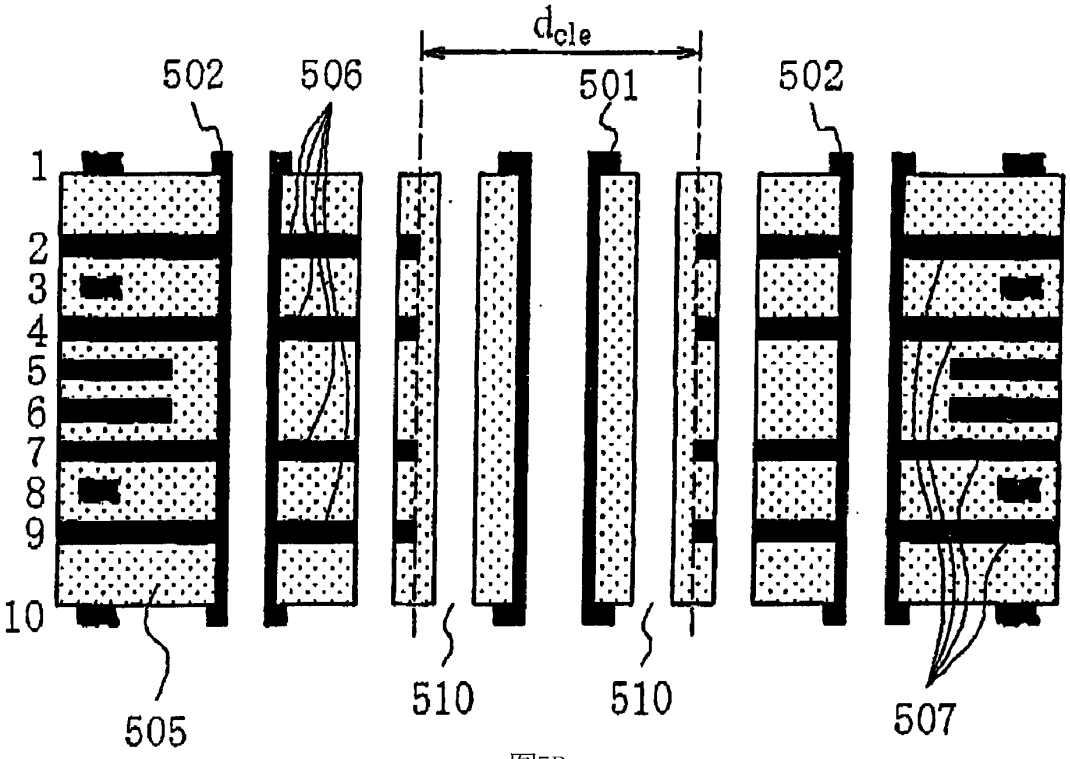


图5B

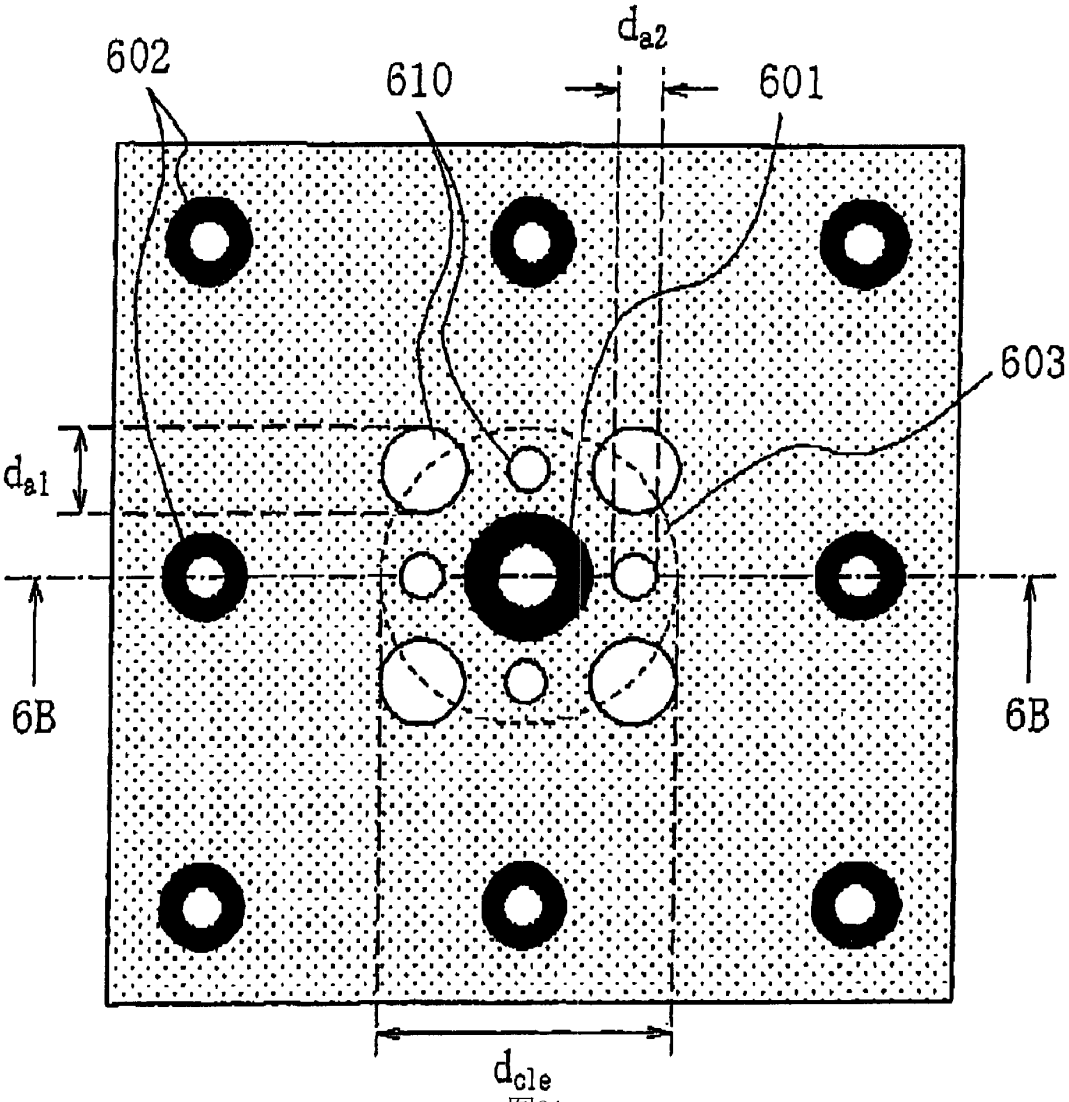


图6A

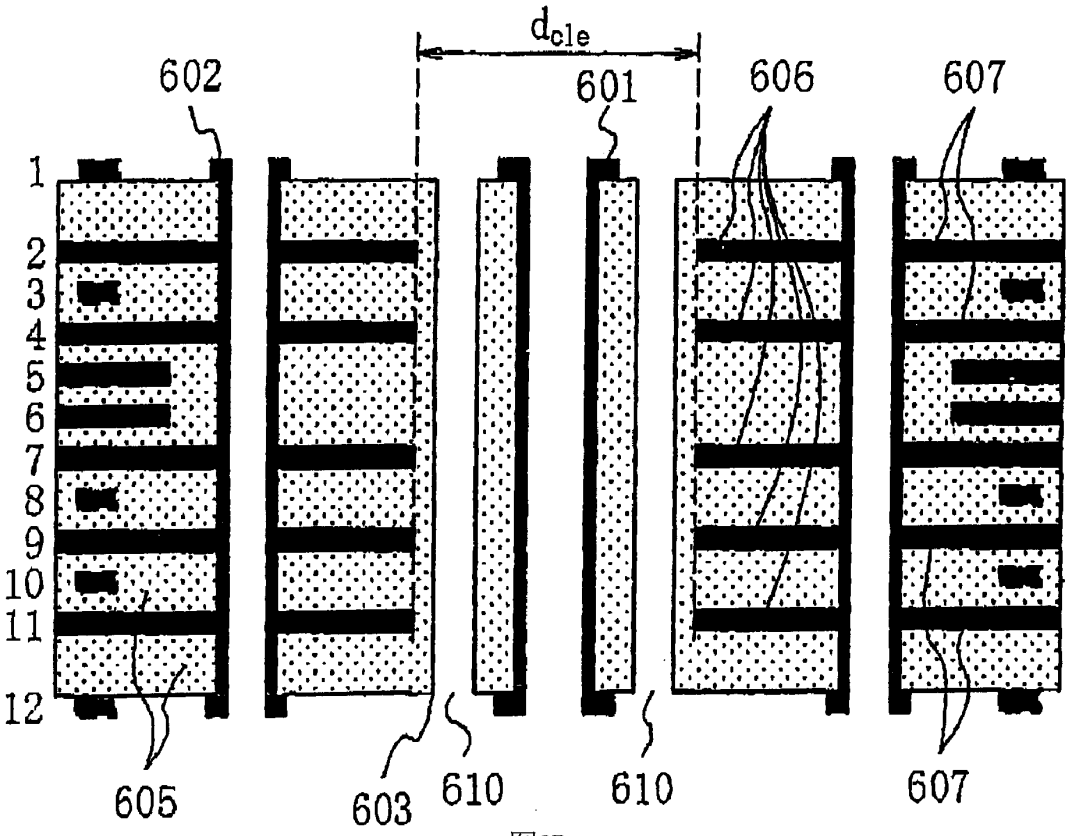


图6B

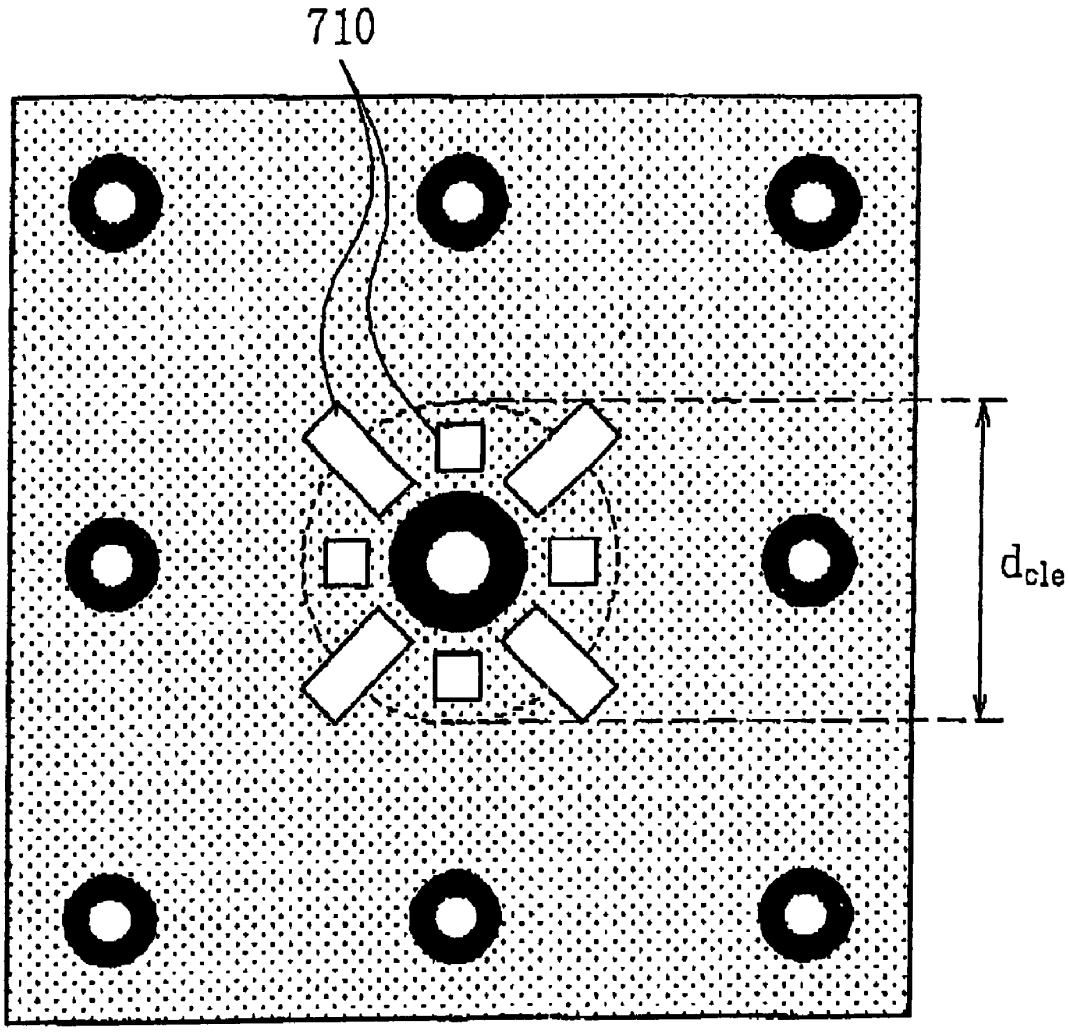


图7

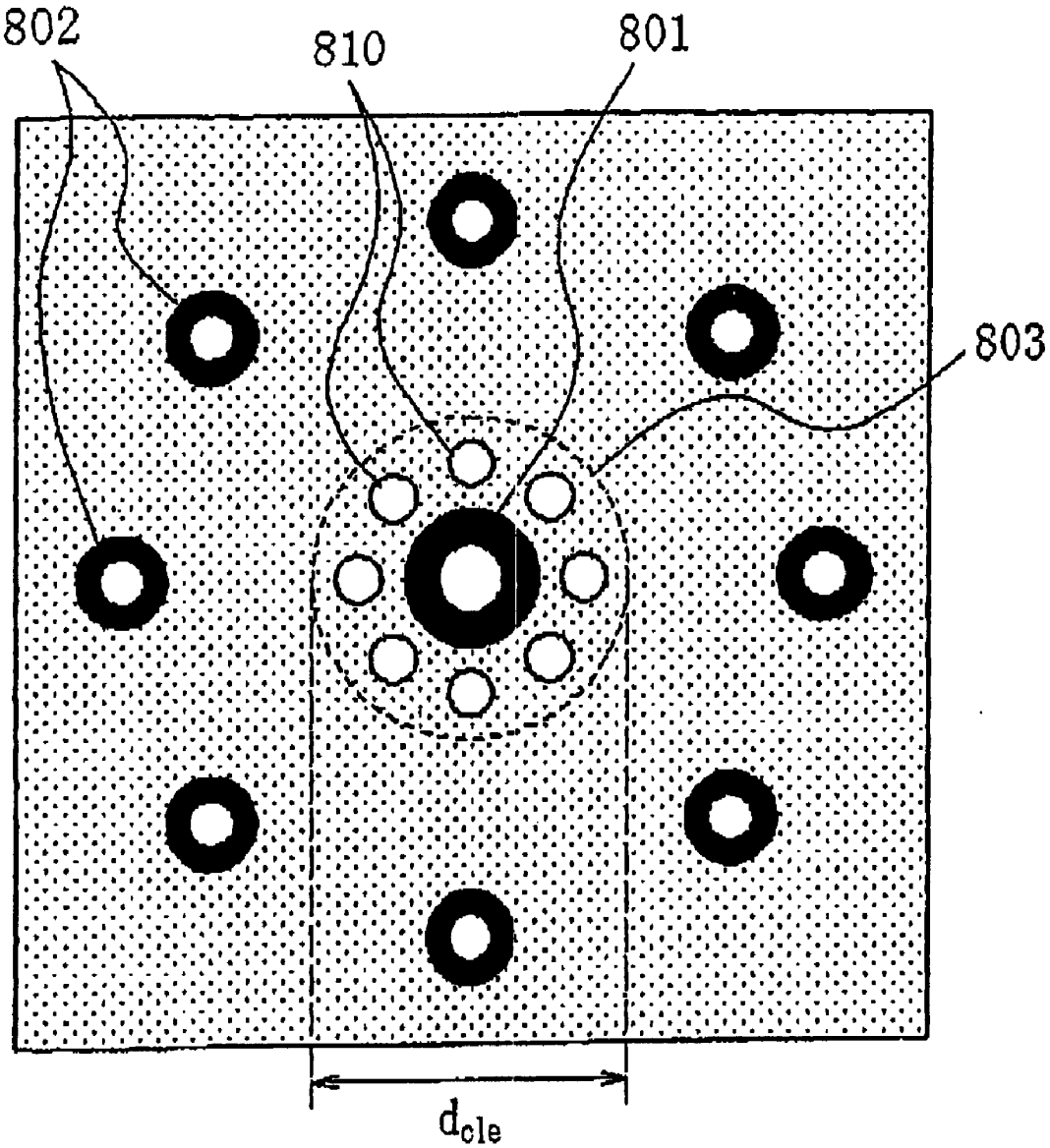


图8

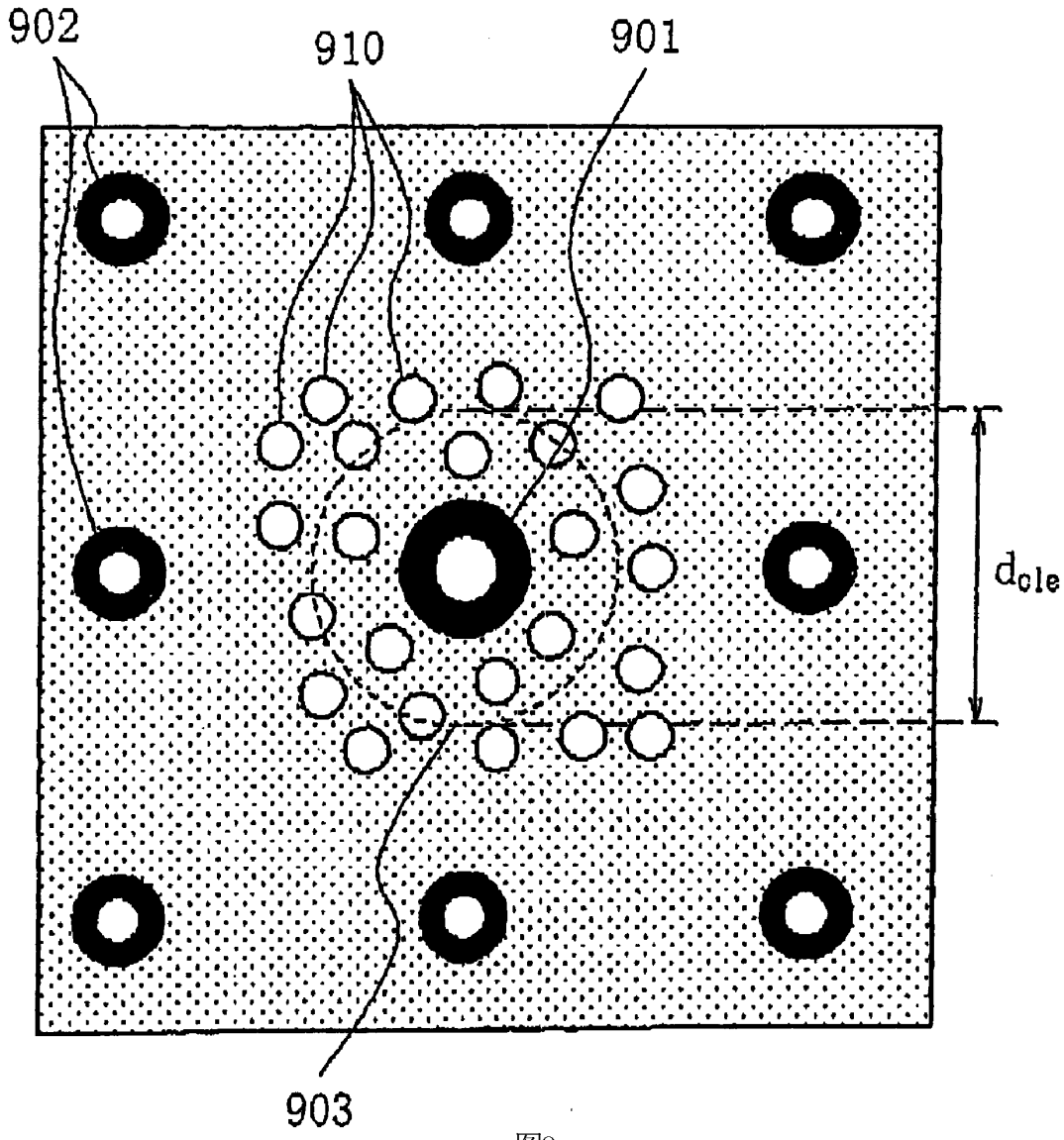


图9

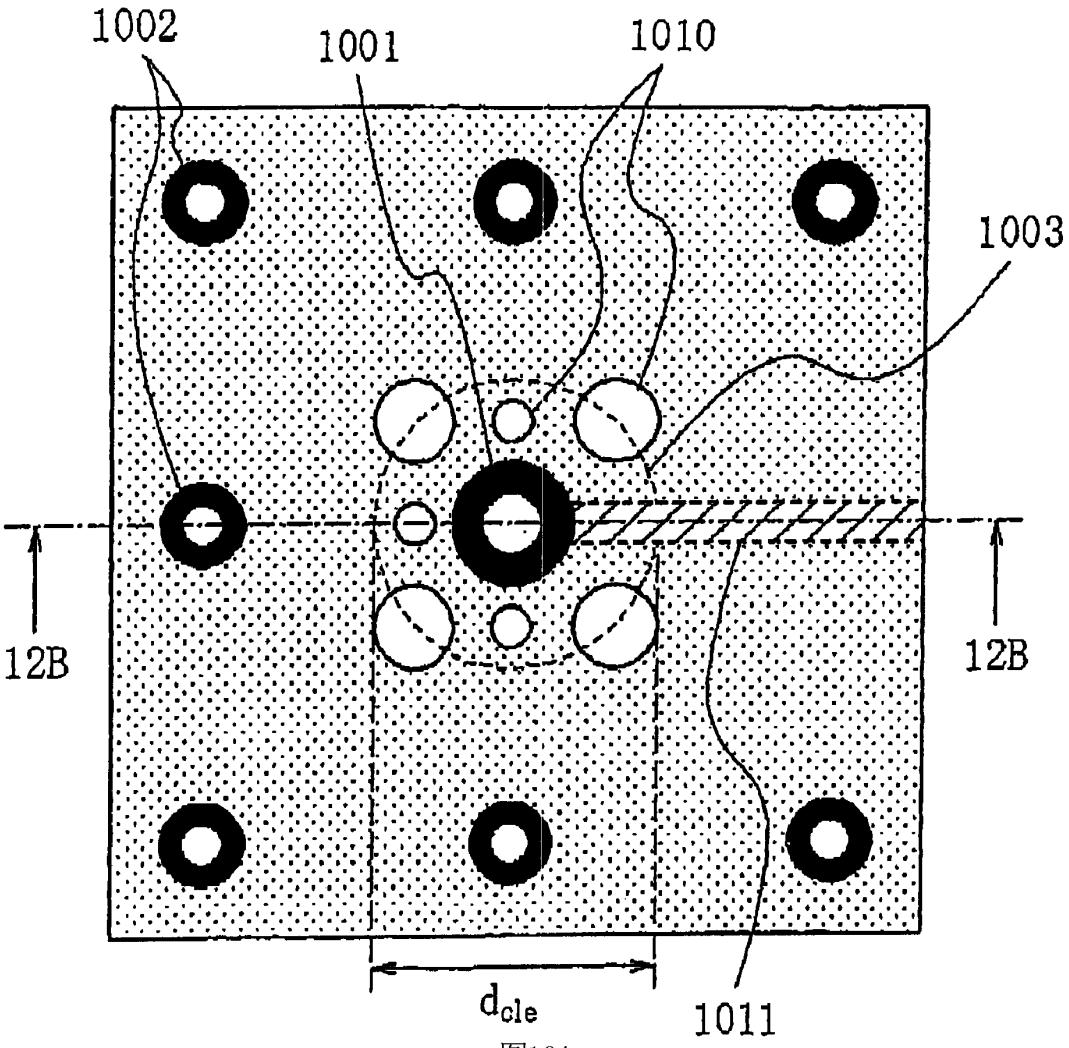


图10A

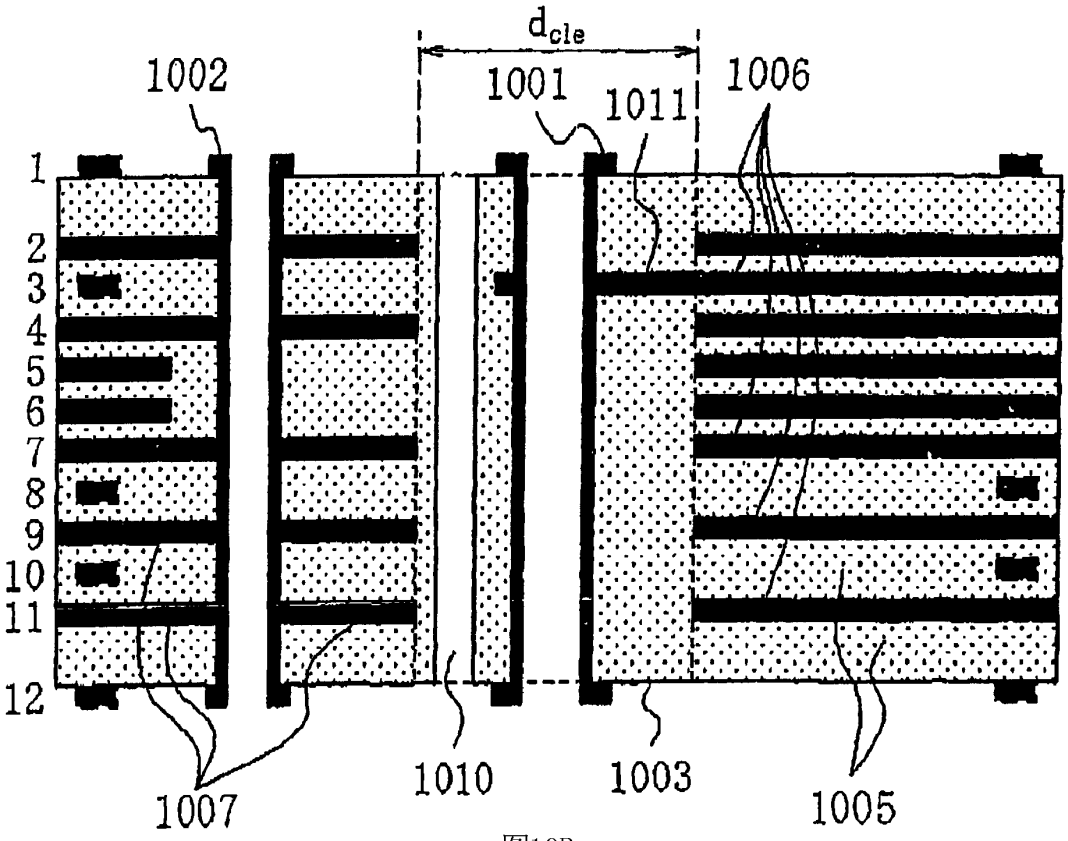


图10B

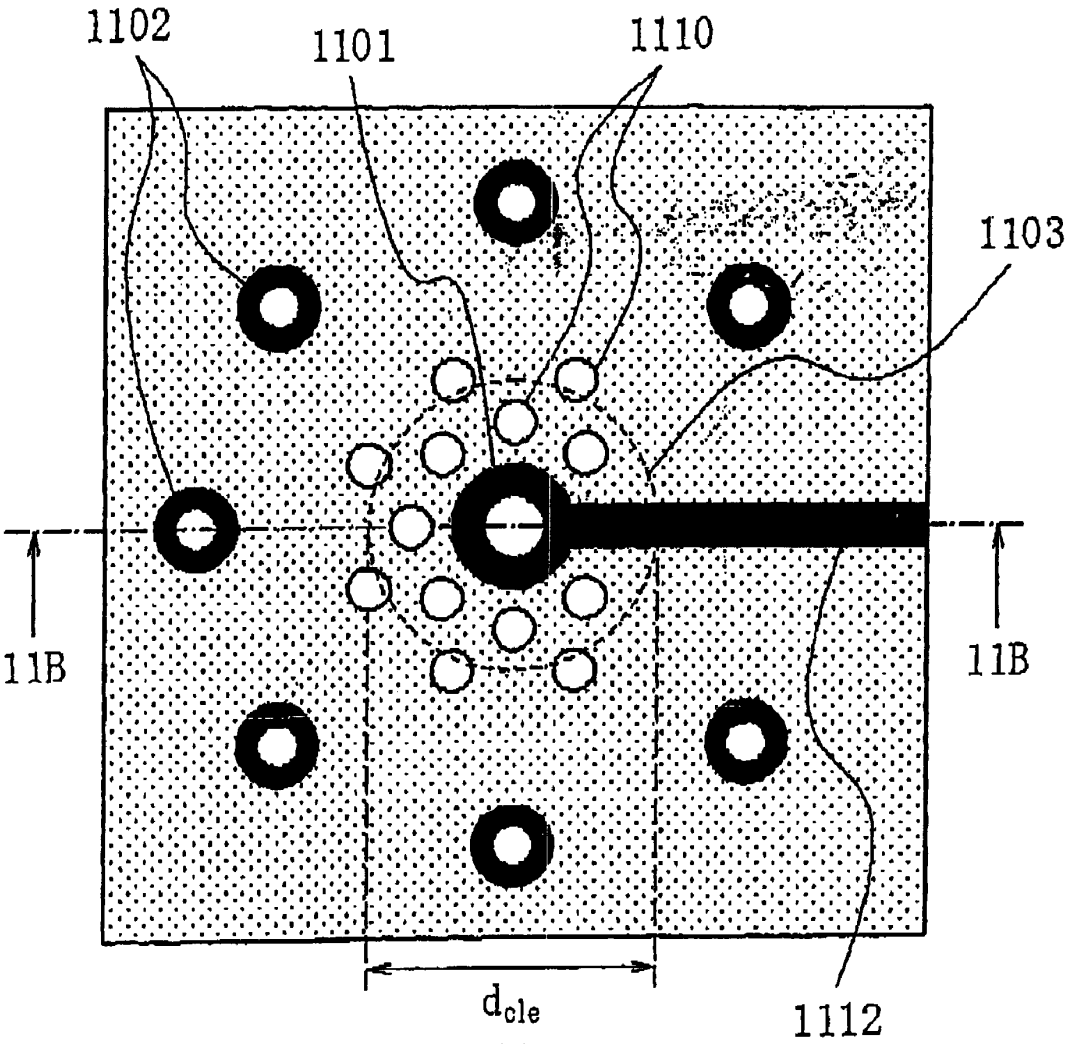


图11A

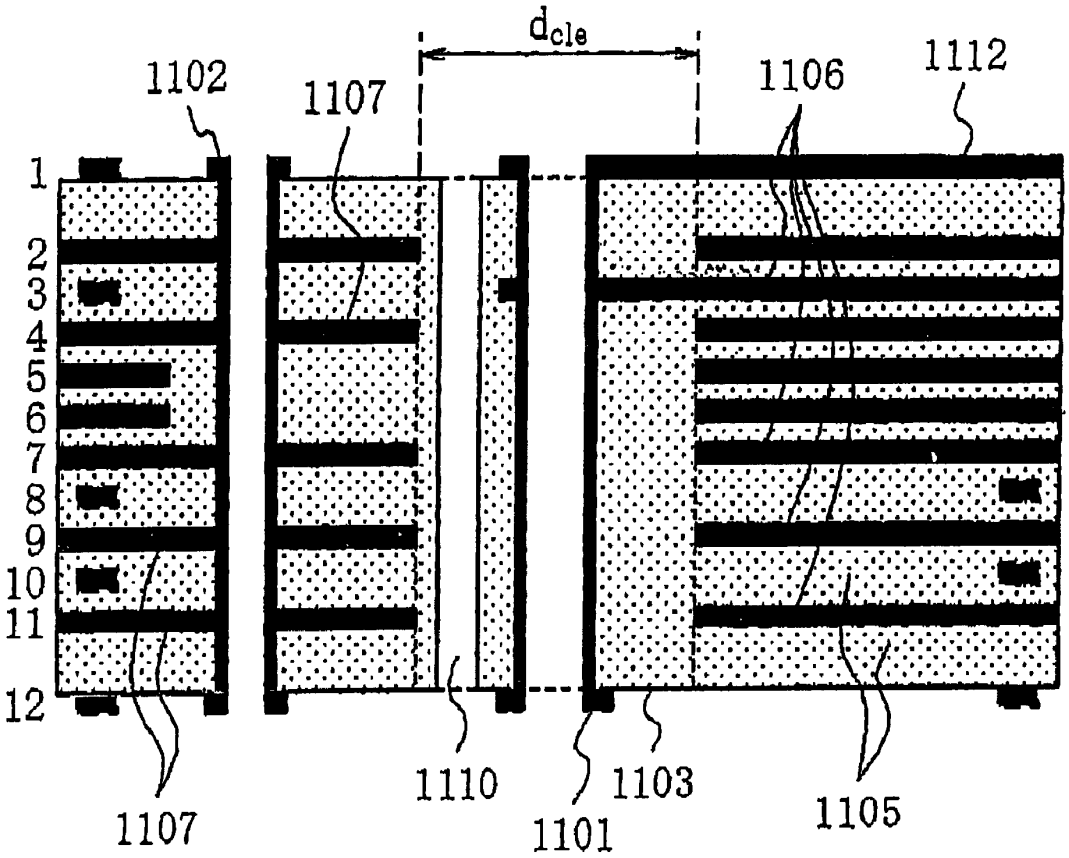


图11B

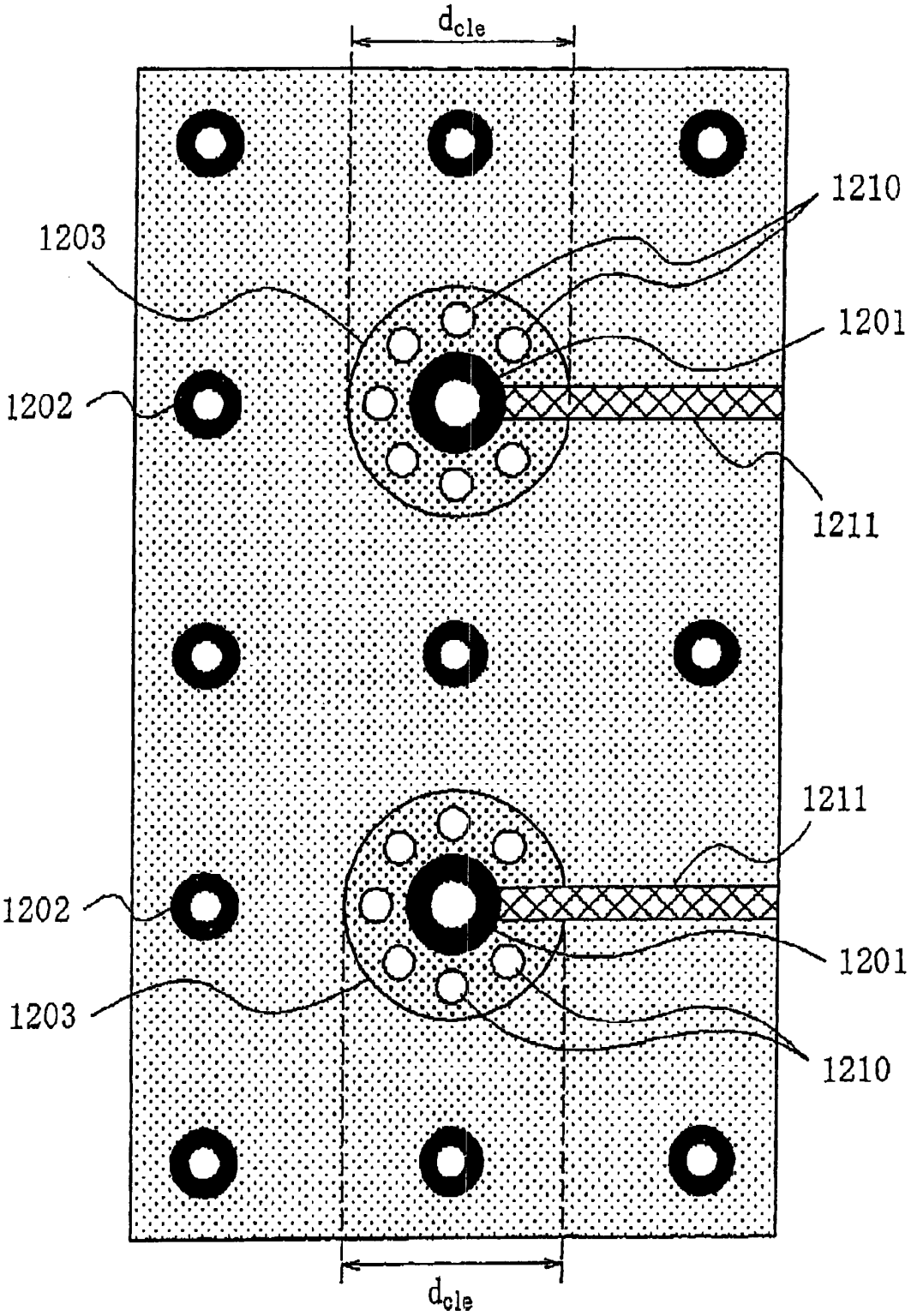


图12

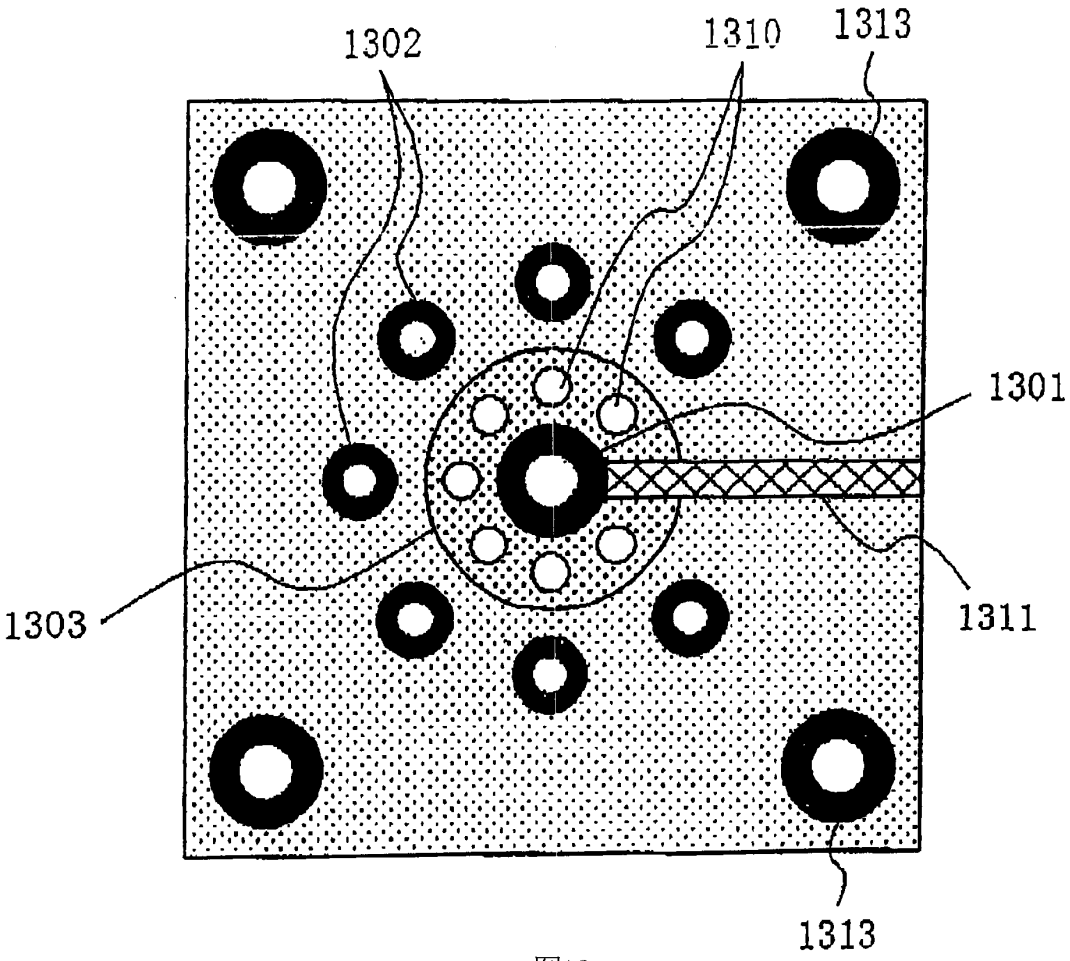


图13

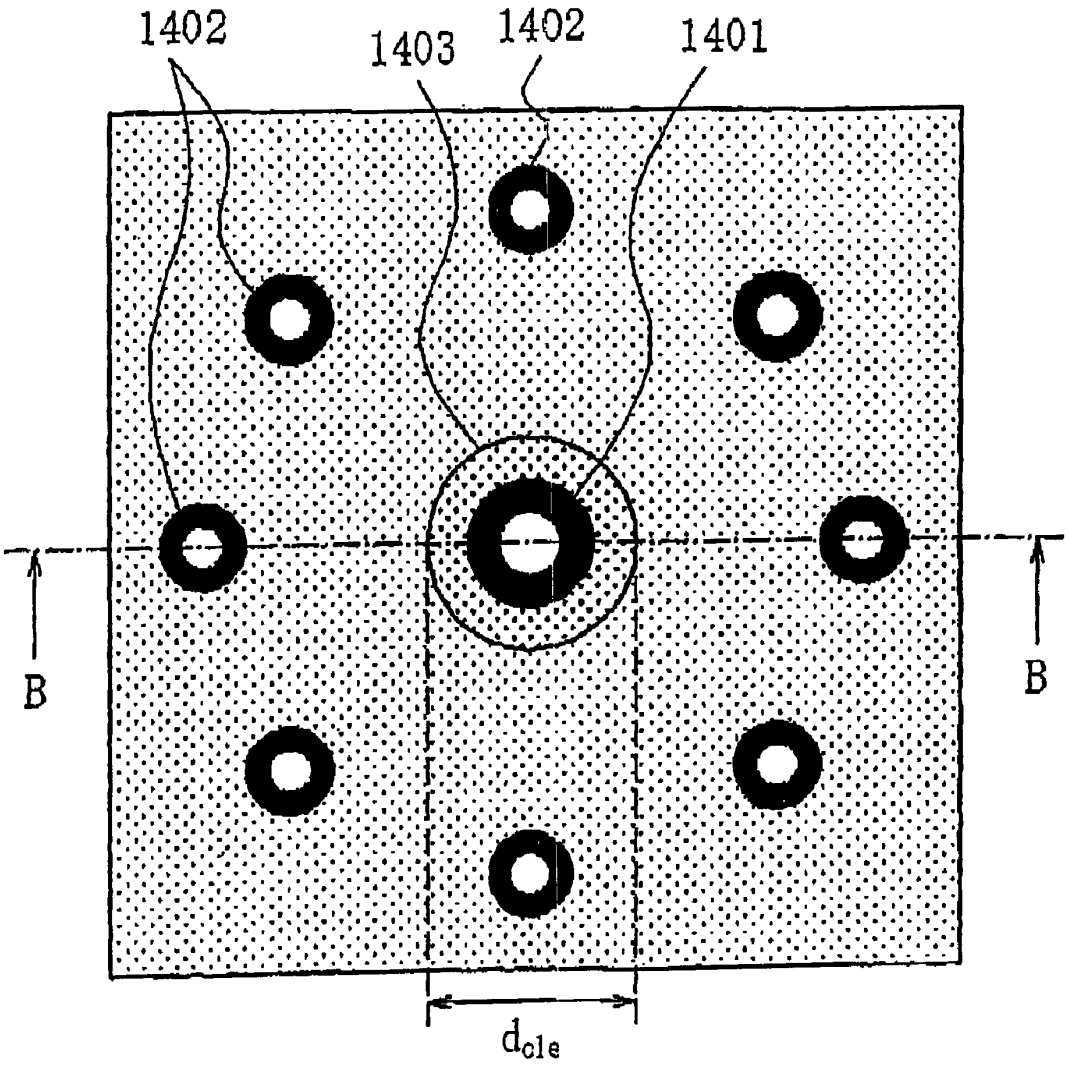


图14A

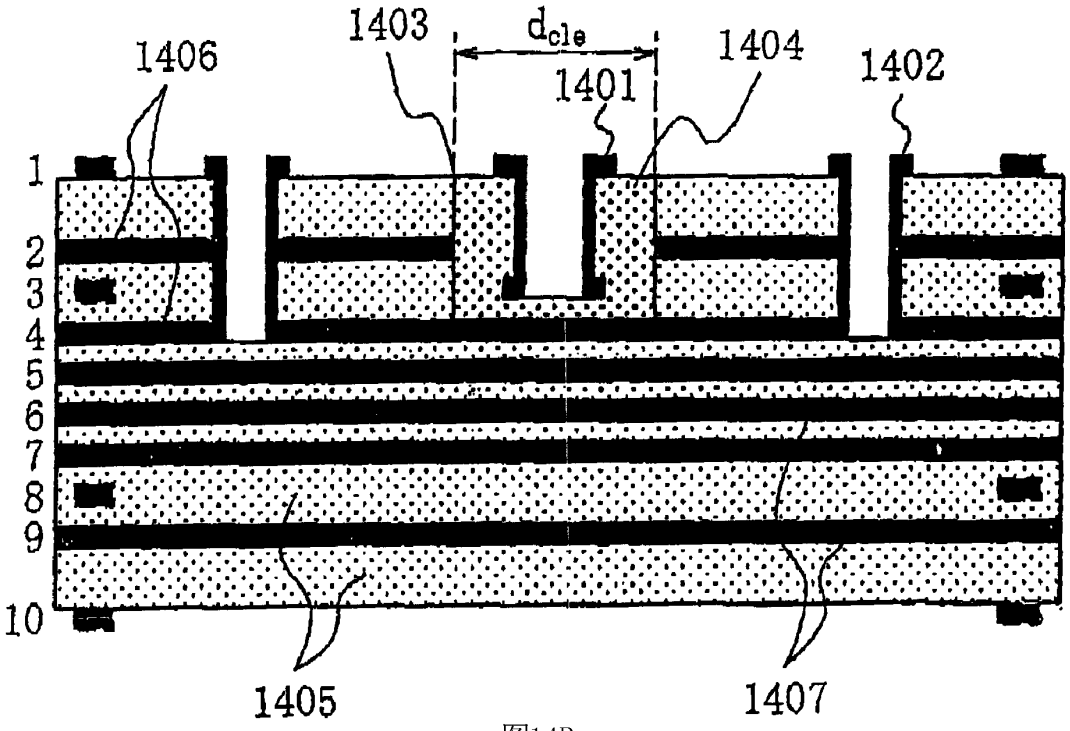


图14B

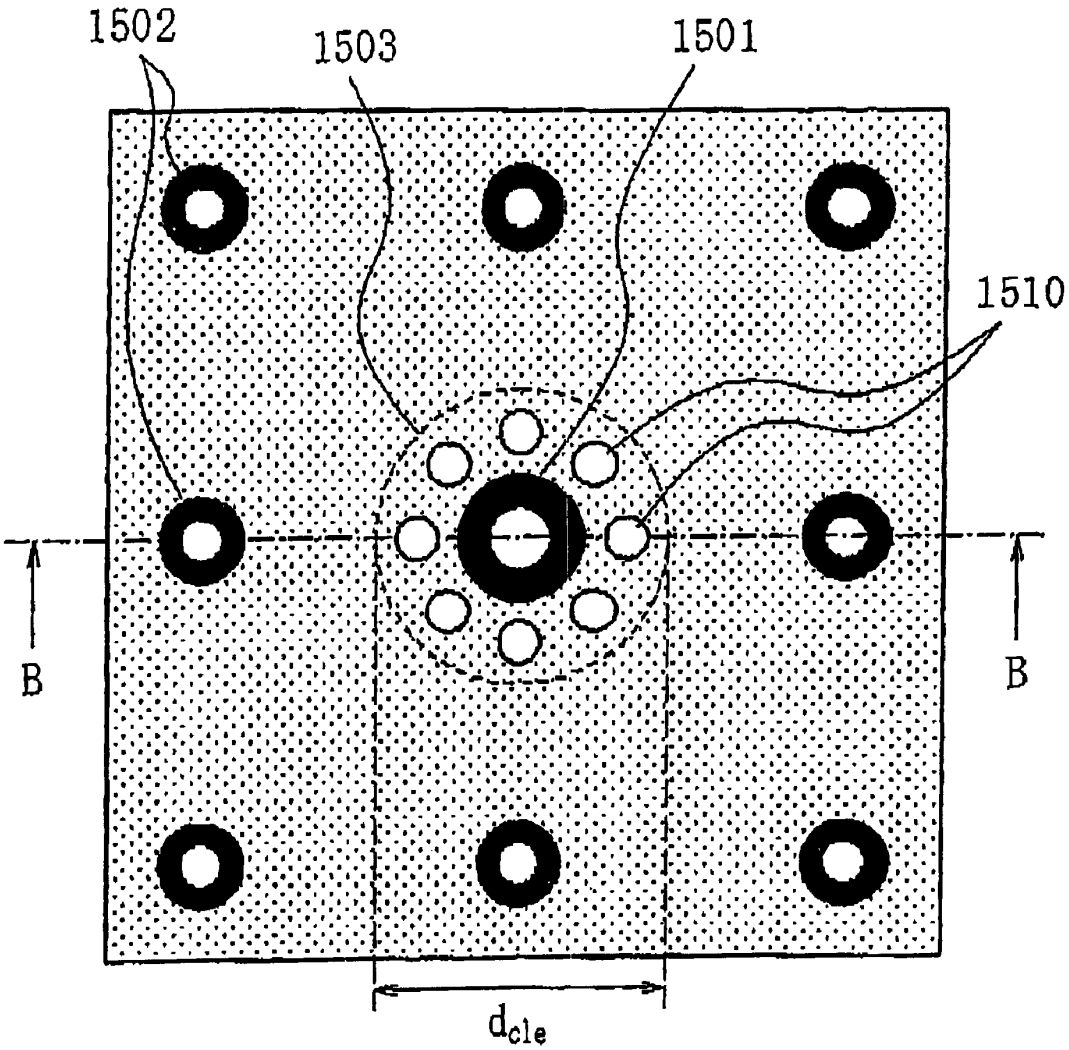


图15A

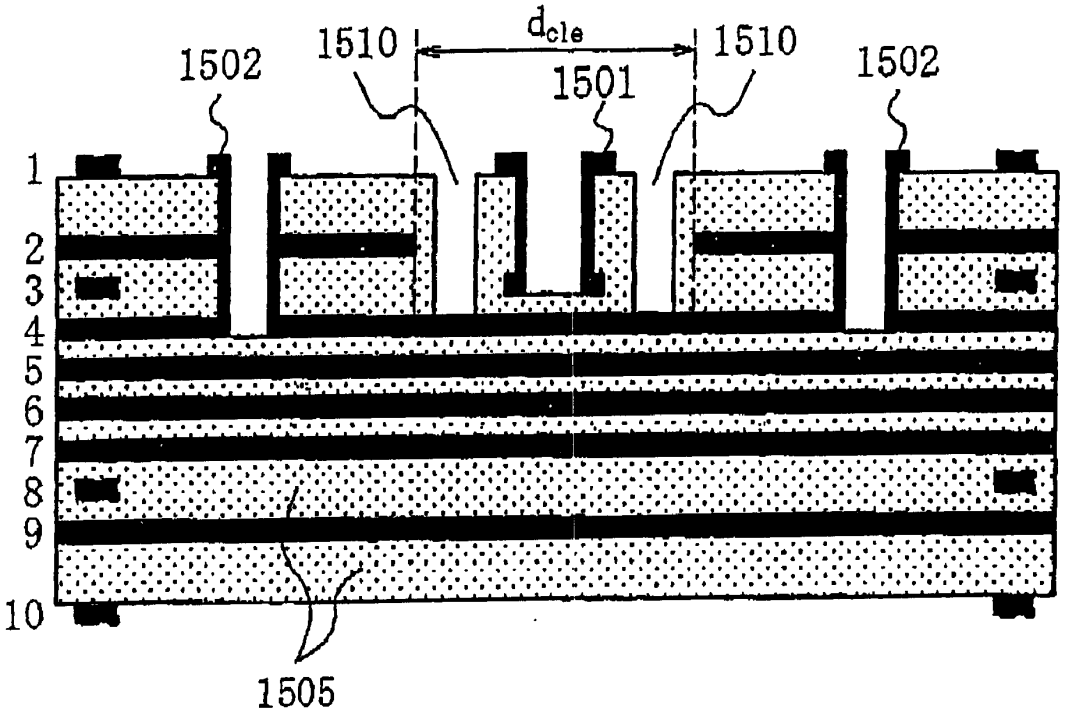


图15B

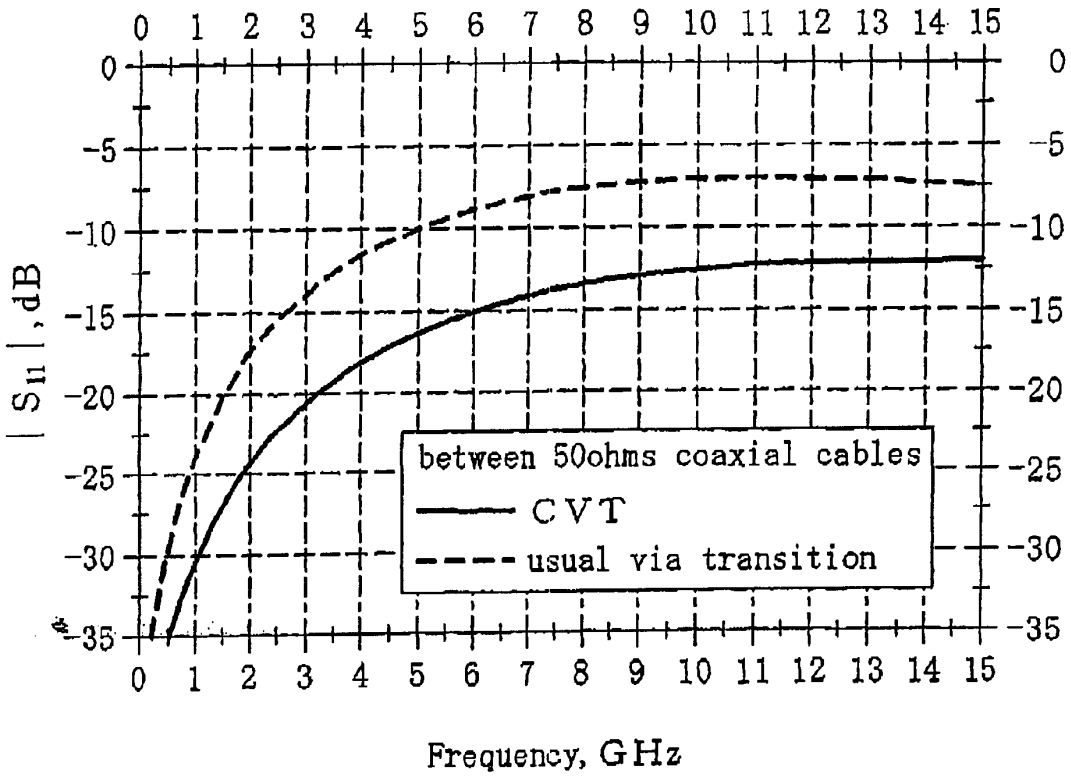


图16A

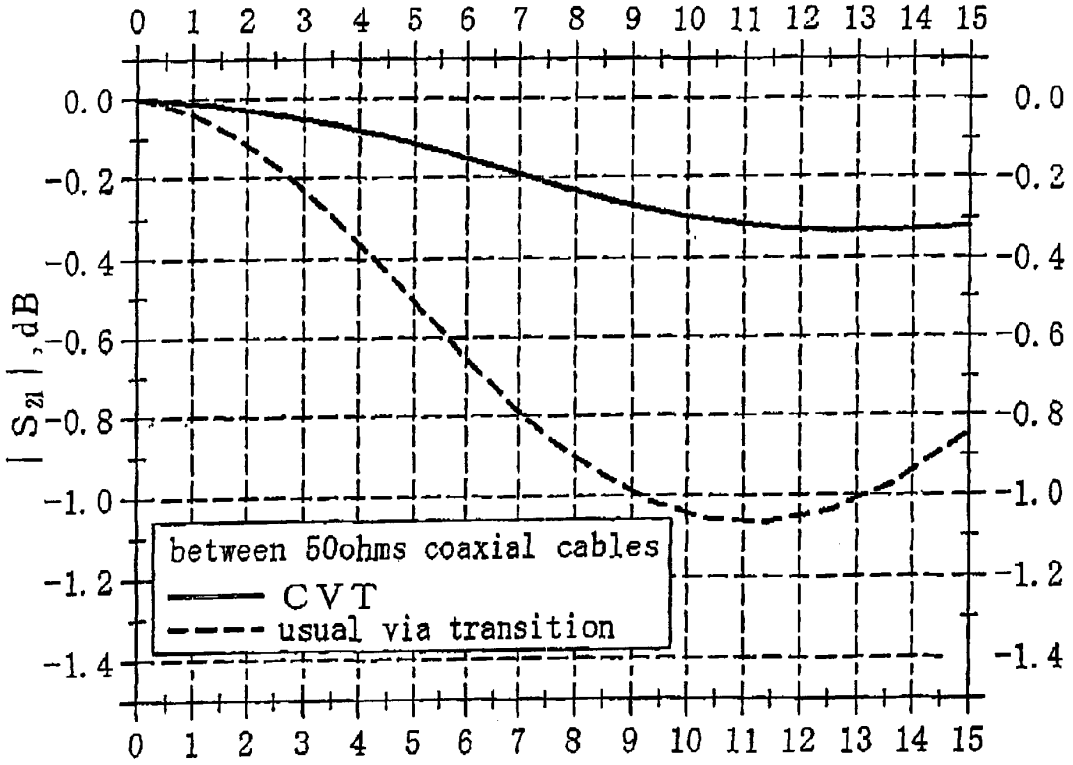


图16B

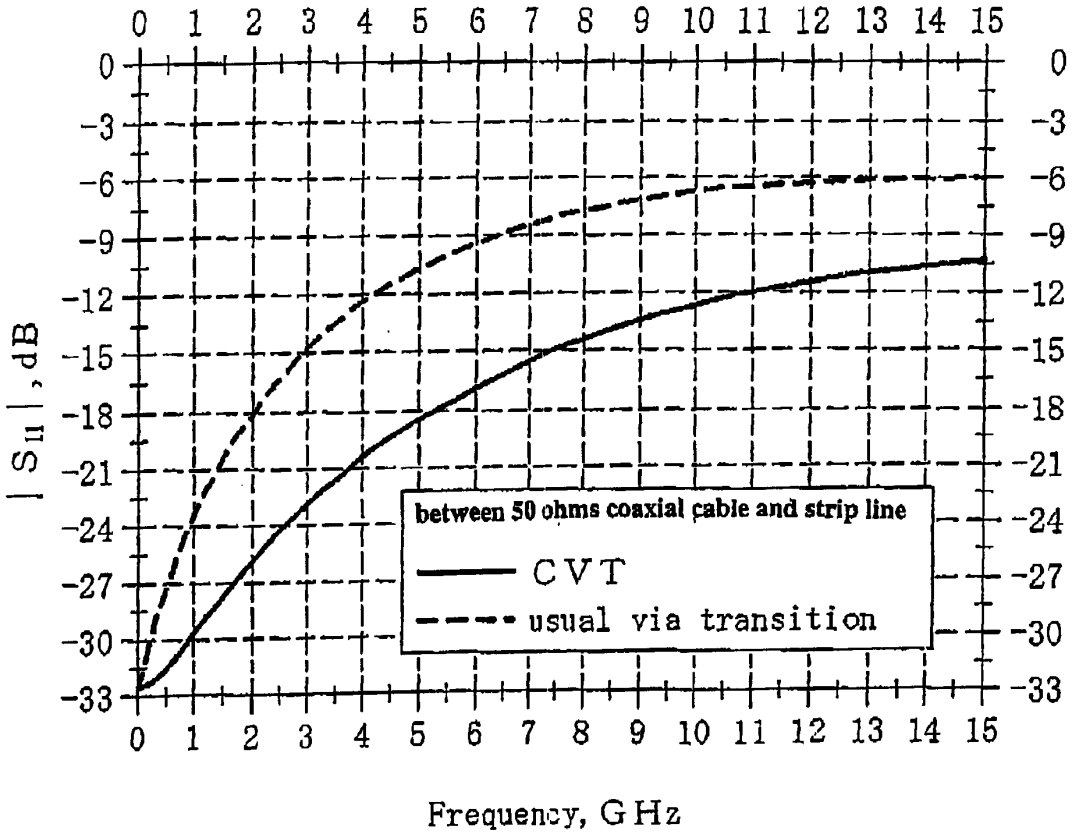


图17A

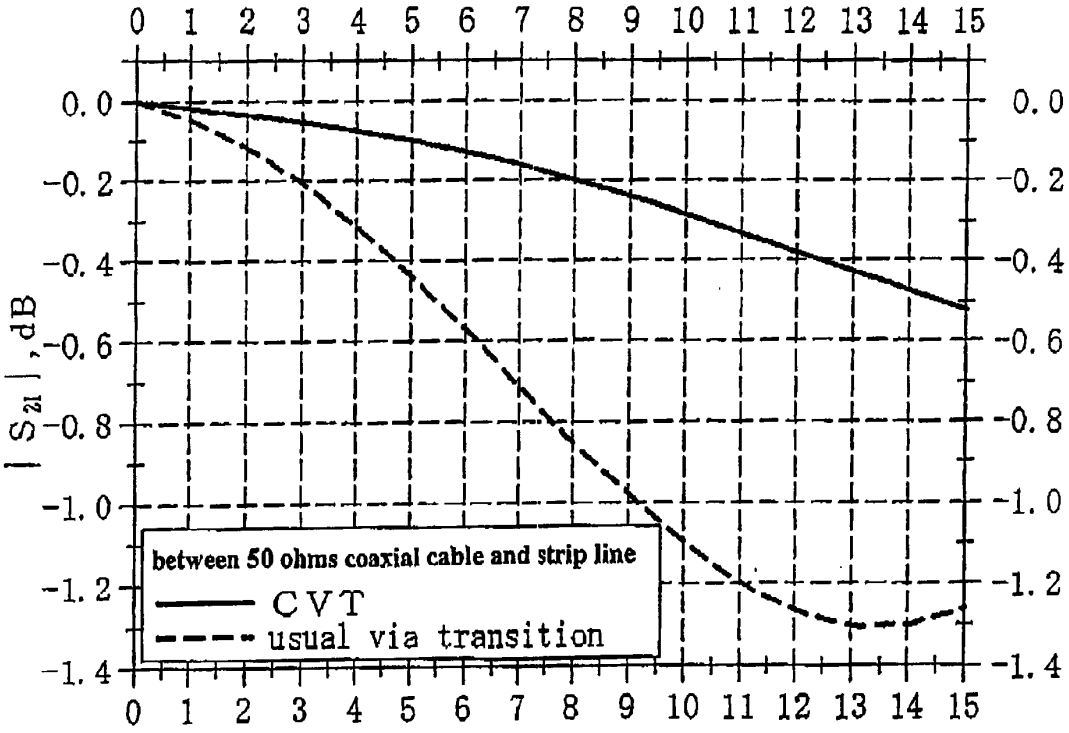


图17B

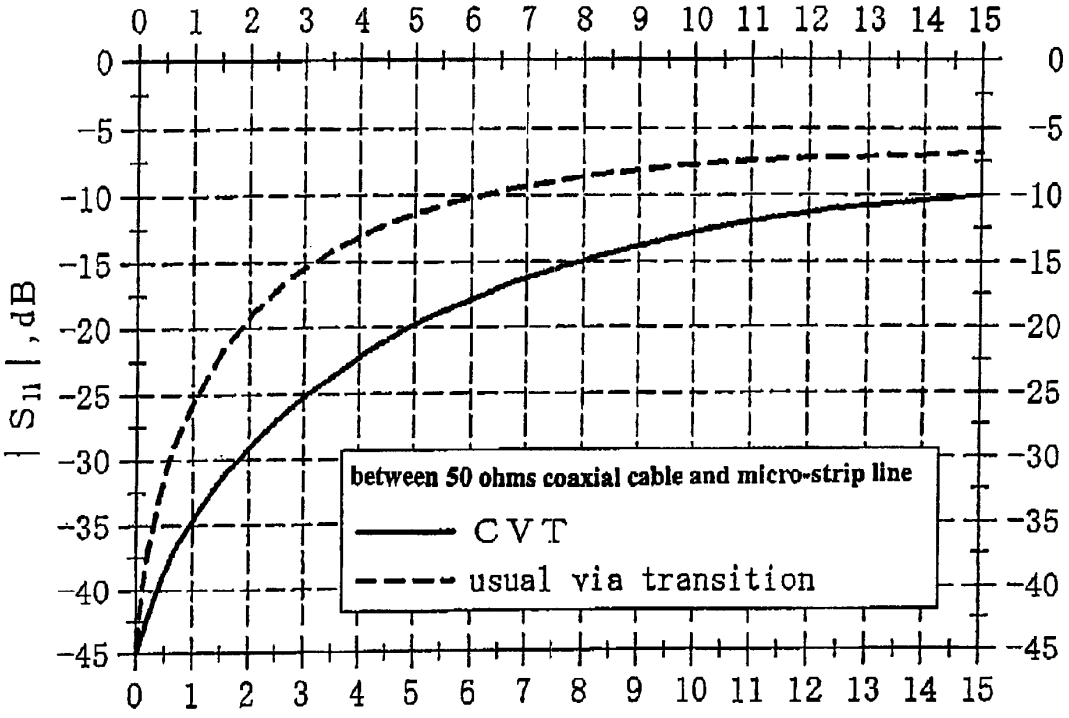
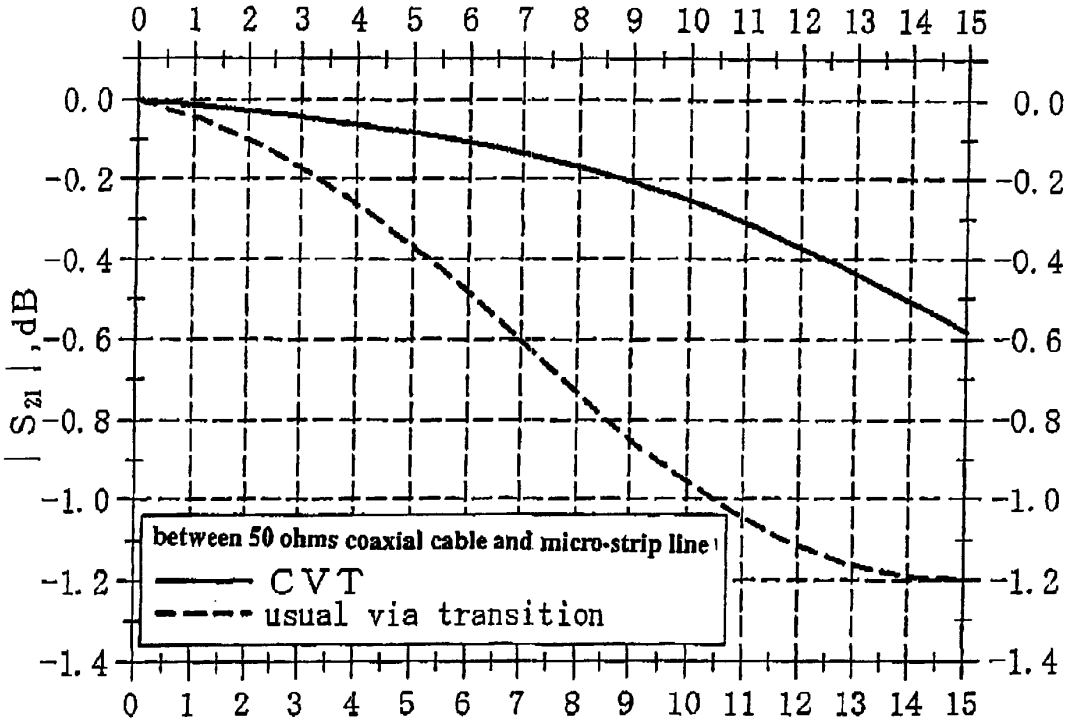


图18A



Frequency, GHz

图18B

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Assignee[std]:	AMPHENOL CORP ;
Inventor[std]:	DUNHAM JOHN R ; GAILUS MARK W ; COHEN THOMAS S ;
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Cooperative Patent class:	H01R12/716 ; H01R12/585 ; H01R12/724 ; H01R12/727 ; H01R13/514 ; H01R13/6474 ; H01R13/6587 ; H01R13/6591 ; H05K1/14 ; H05K7/1445 ; H05K2201/044 ; H05K2201/10189 ; H05K2203/1572 ;
Family members:	CA2592264 AA CA2592270 AA CN101120490 A CN101120490 B CN101120491 A CN101120491 B CN101882717 A CN101882717 B CN101950893 A CN101950893 B DE602005043264 D1 DE602005047978 D1 EP1831970 A2 EP1831970 A4 EP1831970 B1 EP1831971 A2 EP1831971 A4 EP1831971 B1 IL184199 A0 IL184199 A1 IL184200 A0 IL184200 A1 JP2008525972 T2 JP2008526034 T2 US2006024983 AA US2006024984 AA US2006276081 AA US2007149057 AA US2008026638 AA US2009061684 AA US2009298337 AA US2011076860 AA US2011130038 AA US2013112468 AA US2013337665 AA US7094102 BB US7108556 BB US7278886 BB US7422484 BB US7544096 BB US7744415 BB US7811130 BB US8202118 BB US8226438 BB US8444436 BA US9106020 BB WO06071890 A2 WO06071890 A3 WO06071893 A2 WO06071893 A3
Title:	DIFFERENTIAL ELECTRICAL CONNECTOR ASSEMBLY
Title:	差分电连接器组件
Abstract:	

A differential connector has a plurality of rows. Each row includes a plurality of signal conductors provided as differential pairs. Each signal conductor has a first contact end connectable to a printed circuit board, a second contact end, and an intermediate portion having a first width. For each differential pair, one first contact end lies along a first line parallel to the plurality of rows and the other first contact end lies along a second line parallel to and spaced from the first line. The differential connector further includes a plurality of ground conductors, with each ground conductor corresponding to a differential pair. Each ground conductor has a first contact end connectable to the printed circuit board, a second contact end, and an intermediate portion having a second width that is at least twice the first width.

Abstract:

本发明提供了用于最小化电噪声的差分电连接器、组件以及系统。一种差分连接器(400)，包括在多行(330)中的接触(312)。

The present invention provides a differential electrical connector to minimize electrical noise, components, and systems. A differential connector (400), including multi-line contacts (330) in (312).

Description:

差分电连接器组件

[0001] 相关申请的交叉引用

[0002] 本专利申请要求2004年7月1日提交的美国临时专利申请No. 60/584，928以及 2004年12月24日提交的美国临时专利申请No. 60/638，971的优先权。

[0003] 技术领域

[0004] 本发明涉及一种差分电连接器组件。

[0005] 背景技术

[0006] 现代电子系统通常由多个印刷电路板装配而成。这种通常称为“子卡”的印刷电 路板上包含诸如集成电路之类的元件。每一个子卡一般还包括一个或一个以上的连接器， 所述连接器可使子卡上的元件与系统中其它子卡上的元件连通。

Differential electrical connector assembly

[0001] application of the relevant cross-references

[0002] This patent application claims priority to U.S. Provisional Patent July 1, 2004 filed No. 60 / 584,928 and US Provisional Patent December 24, 2004 filed No. 60 / 638,971 of priority.

[0003] TECHNICAL FIELD

[0004] The present invention relates to a differential electrical connector assembly.

[0005] BACKGROUND

[0006] Modern electronic systems are typically assembled from a plurality of printed circuit boards. This is usually referred to as "child card" printed circuit

[0007] -种将电子系统中的子卡互连的方式是利用中平面。中平面是一种通常大于子卡 的印刷电路板，子卡经由在子卡和中平面上的连接器连接到该中平面上，并且该中平面在 其中提供导电通路。也称为“信号迹线”的导电通路，在系统中的子卡之间进行互连并在它 们之间提供通信。正如名称所暗示的那样，中平面在两侧上均提供连接器，可使子卡连接在 中平面的两侧上。中平面可以在连接在中平面同一侧上的子卡之间路由信号，或将中平面 一侧上的子卡与中平面另一侧上的子卡进行交叉连接。

[0008] 为了将连接器连接到中平面上，孔按照惯例是钻穿中平面的。所述也称为“通孔” 的孔电连接到中平面中的信号迹线。通孔的内壁通常镀有导电材料，例如金属，以提供导电 性。连接器配备有接触端头，例如压配合接点尾线或SMT(表面安装技术）接点尾线，用于 与所述通孔连接。

[0009] 因为电子系统已经变得更小、更快且更复杂，这普遍要求中平面在不增大尺寸的 情况下，或是在许多场合下在实际上尺寸减小的同时提供更多通孔和信号迹线。这既在设 计和制造中平面的过程中引起了相当大的困难，也在处理电噪声和其它电特性方面引起了 相当大的困难。电噪声通常被认为是电子系统中任何不希望有的电能量，包括（但不限于） 反射、电磁干扰、模式变换和诸如串话之类的不需要的耦合。

[0010] 更小、更快且更复杂的电子系统的趋势已经要求连接器在更小空间中传送更多更 快的数据信号而不降低信号的电特性。通过在将连接器中的信号导体放置得更靠近，可以 使得连接器在更小的空间中传送更多的信号。将信号导体放置得更靠近的主要困难是，随 着信号导体之间的距离减小和信号速度的增大，信号导体之间的电噪声增大。此外，随着频 率含量增加，能量损耗的可能性会更大。能量损耗可归因于阻抗间断性、模式变换、源于不完美屏蔽的泄漏，或是不希望有的与其它导体的耦合（串话）。因此，设计连接器以便控制 会造成能量损耗的机制。设计构成传输通路的导体以匹配系统阻抗，强制

board components such as integrated circuits contain. Each sub-card typically includes one or more of the connector, the connector components and systems enable the device on the daughter card in the other sub-card communication.

[0007] - kind of the electronic systems daughter card interconnect method is to use the plane. The plane is typically greater than a daughter card printed circuit board, daughter card connected via a connector on the daughter card and in the plane onto the plane, and that the plane in which provides a conductive path. Also referred to as "signal traces" conductive path between the system interconnect daughter card and provides communication between them. As the name implies, the plane on both sides provide a connection that allows the daughter card connector on both sides of the plane. The plane can be connected between the flat side of the daughter card on the same route signals, or the daughter card daughter card on the side of the plane and the plane was on the other side of cross-connect.

[0008] In order to connect to the connector on the plane, the hole is drilled through the customary plane. Also known as the "through-hole" in the hole in the plane is electrically connected to the signal traces. The inner wall of the through hole is usually plated with a conductive material, such as metal, to provide electrical conductivity. Connector with contact ends, such as press fit contacts tails or SMT (surface mount technology) contact tails, for connecting with said through hole.

[0009] Because the electronic systems have become smaller, faster and more complex, which in general requires a plane without increasing the size, or in many cases actually reduced in size while providing More vias and signal

执行一种已知的 能量传递模式，使涡流减到最小，并使交替的传输通路相互绝缘。一个控制能量损耗的实 例是将接地的导体放置为邻近信号接触元件，以确定阻抗并使辐射形式的能量损耗减到最 小。

[0011] 一种控制连接器中的电噪声的方式是利用差分信号。差分信号是由叫做“差分对” 的一对信号导体代表的信号。该对信号导体之间的电压差代表信号。如果电噪声与差分对电磁耦合，那么对该对的每一个信号导体的影响就会是相似的。与单信号导体相比，这给出 了一种对电噪声比较不敏感的差分对。然而，差分连接器的使用，特别是在中平面系统体系 结构中，引起了另外的困难，因为对应于中平面的任一侧上的差分对的通孔必须每一个是 在该中平面中电连接的，并且信号迹线只能在邻近的差分对之间进行路由。

[0012] 因此，所希望的是提供一种中平面和为这样的中平面而设计的差分连接器，以致 力于解决上述困难。

发明内容

[0013] 在根据本发明的中平面的一个实施例中，中平面具有第一侧和与第一侧相对的第 二侧，第一差分连接器的接触端子连接到第一侧，第二差分连接器的接触端子连接到第二 侧。该中平面包括多个从第一侧延伸至第二侧的通孔，所述通孔提供第一侧上的第一信号 激励（signallaimch)和第二侧上的第二信号激励。第一信号激励是在用于电连接到第一 差分连接器的接触端子的多个行中提供的，每一行具有沿着第一条线的第一信号激励和沿 着基本平行于第一条线的第二条线的第一信号激励。沿着第一和第二条线的第一信号激励 是偏移的，从而沿着第一条线的第一信号激励和沿着第二条线的邻近的第一信号激励对应 于第一差分连接器的差分对。第二信号激励是在用于电连接到第二差分连接器的接触端子 的多个列中提供的，每一列具有沿着第三条线的第二信号激励和沿着基本平行于第三条线 的第四条线的第二信号激励。沿着第三和第四条线的第二信号激励是偏移的，从而沿着第 三条线的第二信号激励和沿着第四条线的邻近的第二信号激励对应于第二差分连接器的 差分对。

traces. This not only during the design and manufacture of the plane caused a considerable difficulties, but also dealing with electrical noise, and other electrical characteristics caused considerable difficulties. Electrical noise is usually considered to be any electronic system undesirable electrical energy, including (but not limited to) the reflection, electromagnetic interference, mode change and unwanted coupling, such as crosstalk and the like.

Trend

[0010] smaller, faster and more complex electronic systems already require connectors deliver more data faster signal in a smaller space, without lowering the electrical characteristics of the signal. By the connector is placed closer to the signal conductor, so that the connector can transfer more signals in a smaller space. The signal conductor is placed more near the main difficulty is that with a distance between signal conductors decreases and increases signal speed, electrical noise between the signal conductors is increased. In addition, with the increase of the frequency content, the possibility of energy loss will be even greater. Energy loss attributable to impedance discontinuities, mode change, from the imperfect shield leakage, or do not want some other conductor coupling (crosstalk). Therefore, the design will cause the connector to control energy loss mechanism. Conductor design consists of a transmission path impedance matching system to enforce a known mode of energy transfer in the eddy current is minimized, and an alternate transmission path insulated from each other. A control energy loss instance is placed in the ground near the signal conductor contact elements, in order to determine the impedance and

附图说明

[0014] 附图没有打算按比例来绘制。在附图中，在不同图中举例说明的每一个同样的或 几乎完全相同的部件都是用相似的数字来表示的。为了清楚，不是所有部件都在每一幅图 中被加以标注。在附图中：

[0015] 图1是电子系统的透视图，该系统利用了根据本发明实施例的中平面；

[0016] 图2是根据本发明实施例的差分电连接器组件的部分分解图，该电连接器组件可 以用在图1的电子系统中；

[0017] 图3是图2中所示差分中平面连接器的透视图；

[0018] 图4是透视图，示出了根据本发明实施例的图3中显示的差分中平面连接器的差 分对信号导体和对应接地导体的行；

[0019] 图4A是图4的替换实施例，示出了图3中所示的差分中平面连接器的差分对信号 导体以及对应接地导体的行；

[0020] 图5是底视图，示出了图4中所示差分中平面连接器的差分对信号导体和对应接 地导体的第一接触端子；

[0021] 图6是图2中所示根据本发明实施例的差分子卡连接器的透视图，为了清楚起见， 晶片是与连接器分开的；

[0022] 图7是图6的晶片的分解图，只示出了差分对信号导体和对应接地导体；

[0023] 图8A是图1的中平面一侧的部分的示意性顶视图，表面的一部分被去除以显示接地平面层；

[0024] 图8B是图1的中平面另一侧的部分（与图8A相同的部分）的示意性顶视图，表 面的一部分被去除以显示接地平面层；

[0025] 图9A是穿过传统差分中平面连接器的配合接触区的截面的示意图，该连接器附 着于中平面的一侧；

radiation in the form of reduced energy consumption minimal.

[0011] A method of controlling the electrical connector in the way noise is to use differential signals. A differential signal is a signal "differential pair" in a pair of signal conductors represented by the known. A voltage signal representative of the difference between the signal conductor. If electrical noise is electromagnetically coupled with the differential pair, then the influence of each signal conductor would be similar. Compared with a single signal conductor, which gives a relatively insensitive to electrical noise differential pair. However, the use of differential connection, especially in the flat system architecture, causing additional difficulties, because the through-hole corresponding to the differential pairs on either side of the plane must each be in power in the plane connection and signal traces can be routed between adjacent differential pair.

[0012] Accordingly, it is desirable to provide a mid-plane and is designed such differential midplane connector, so that the force to solve the above problems.

Summary

[0013] In accordance with one of the plane of the embodiment of the present invention, the plane has a first side and a second side opposite the first side, connecting the contact terminal of the first differential connector to the first side, contact terminals connected to the second differential connector to the second side. The midplane includes a plurality extending from a first side to the second side of the through hole, the through-hole providing a first signal excitation (signallaimch) on the first side and a second signal on the second side incentives. The first signal excitation is provided in a plurality of rows for electrically connected to the first

[0026] 图9B是穿过传统差分中平面连接器的配合接触区的截面的示意图，该连接器附 着于图9A中所示中平面的另一侧；

[0027] 图9C和9D是示出了用于图9A和9B的通孔图案的图，所述图案分别用于传统差 分中平面连接器；

[0028] 图IOA是穿过根据本发明实施例的差分中平面连接器的配合接触区的截面的示 意图，该连接器附着于中平面的一侧；

[0029] 图IOB是穿过根据本发明实施例的差分中平面连接器的配合接触区的截面的示 意图，该连接器附着于中平面的另一侧；

[0030] 图IOC和IOD是说明用于图IOA和IOB的通孔图案的图，其分别用于根据本发明 实施例的差分中平面连接器；

[0031] 图IIA是根据本发明实施例的两个差分连接器组件的透视图，这两个组件附着于 中平面的相对侧；以及

[0032] 图IIB是图IIA的示意性侧视图，示出了根据本发明实施例的各自安装在中平面的相对侧上并共享公用通孔的两对信号导体。

具体实施方式

[0033] 本发明在应用时不受限于在下面的说明中阐述的或在附图中示出的结构和元件 布置的细节。该发明能以其它方式加以实施，并能够以不同的手段来实施或实现。而且，在 此使用的措词和术语是为了说明起见，不应当看作限制。在此“包括”、“包含”、“具有”、“含”、 “含有”以及它们的变型，意味着既包含其后所列项目以及它们的等效物又包括其它项目。

[0034] 参考图1，示出了电子系统100的简图，电子系统100利用了根据本发明的中平面 110。该中平面具有第一侧112和第二侧114。子卡120A、120B、120C和120D在第二侧114 上被电连接到中平面110。子卡130A、130B和130C在第一侧112上被电连接到中平面110。 注意，中平面110的第一侧112上的子卡130A-130C

differential connector contact terminals in each row along a first signal having a first line of incentive and a direction substantially parallel to the first strip The first signal line second line of incentives. Along the first and second line of the first excitation signal is shifted, so along a first line of the first excitation signal along a first signal and the second line of the adjacent excitation corresponds to a first differential Connector differential pair. A second plurality of columns of contact terminals excitation signal is used to electrically connected to the second differential connector provided in each column along a third line with a second excitation signal and a direction substantially parallel to the Article the second signal line fourth line incentives. Along the third and fourth lines of the second excitation signal is offset, thus along the third line of the second signal stimulus and incentives along the fourth line of the adjacent second signal corresponding to the second difference Connector differential pair.

Brief Description

[0014] The drawings are not intended to be drawn proportionally. In the drawings, each of the same or nearly identical component illustrated in the different figures are represented by like numbers of. For clarity, not all components are to be marked in each picture. In the drawings:

[0015] FIG. 1 is a perspective view of an electronic system, the system takes advantage of the plane according to an embodiment of the present invention;

[0016] FIG. 2 is a partial exploded view of a differential electrical connector assembly of the embodiment of the present invention, the electrical connector assembly can be used in an electronic system of FIG. 1;

在定向上正交于中平面110的第二侧 114上的子卡120A-120D。体现在本发明中的概念尤其适用于这样的正交体系结构的电子 系统。

[0035] 尽管没有在图1的简图中示出，子卡120A-120D和130A-130C通过电连接器组件 被电连接到中平面110。图2示出了根据本发明的这种电连接器组件200的优选实施例。 中平面110包括在电子系统100的子卡120A-120D和130A-130C之间路由信号的多条信号 迹线。参考图7对中平面110进行了更详细的说明。应当指出的是，第一侧112上显示的 子卡130A-130C的数目和第二侧114上显示的子卡120A-120D的数目仅仅是出于说明性的 目的，连接到中平面110的子卡的实际数目可以依据电子系统的情况而改变。

[0036] 图2示出了可以用来将子卡120A-120D和130A-130C连接到图1的中平面110的 电连接器组件200。电连接器组件200优选地是差分电连接器组件。电连接器组件200包括第一差分电连接器300和第二差分电连接器400，第一差分电连接器300在图示中连接到 中平面110，第二差分电连接器400连接到子卡之一（在图2中参考子卡120A进行图示）。 典型地，一个或一个以上的第二连接器400将被连接在每一个子卡，相应数目的第一连接 器300被连接到中平面110。

[0037] 图3示出了具有外壳302的差分中平面连接器300，外壳302优选地是由绝缘材料 构成。外壳302具有侧壁304、305、端壁307、308以及底部（没有编号）。布置在外壳302 的底部中的是作为差分对提供的多个信号导体310以及多个接地导体320，每一个接地导 体320对应于信号导体310的差分对并且被放置得邻近那里。正如图4、4A和5中更详细 显示的那样，信号导体310和接地导体320是在多行中提供的。仅仅是出于示范的目的，图 4中显示了六行330a-330f，每一行具有六个由信号导体310组成的差分对和六个对应接地 导体320。注意，行数和每一行的信号导体310的数目，以及每一行的接地导体320的数目 可以为任何期望的数目。然而，正如结合图8中的中平面110的说明将

[0017] FIG. 3 is a perspective view of the difference in the plane of the connector shown in Figure 2;

[0018] FIG. 4 is a perspective view showing a view of an embodiment of the invention of differential signal conductors and the corresponding row of 3 difference in ground conductor plane of the connector shown;

[0019] FIG 4A is an alternative embodiment of FIG. 4, it shows the difference in the plane shown in FIG. 3 connector differential pair signal conductors and corresponding ground conductor of the line;

[0020] FIG. 5 is a bottom view showing the differential midplane connector shown in FIG. 4 of the first contact differential signal conductors and ground conductors corresponding to the terminal;

[0021] FIG. 6 is a perspective view shown in Figure 2 the difference between molecules card connector according to an embodiment of the present invention, for clarity, the wafer is separated from the connector;

[0022] FIG. 7 is an exploded view of the wafer of FIG. 6, shows only the corresponding differential pair signal conductors and ground conductors;

[0023] Figure 8A is a schematic top view of the plane side of a portion, part of the surface is removed to reveal a ground plane layer;

[0024] Figure 8B is a side plan view of another portion of Figure 1 (with the same portion of FIG. 8A) is a schematic top view of a portion of the surface is removed to reveal a ground plane layer;

[0025] FIG. 9A is a sectional view taken along the plane of the connector mating contact region through traditional

变得更加显而易见 的那样，优选地的是预先选择行数，每一行的信号导体310的数目，以及每一行的接地导体 320的数目，以确保大致方形的用于连接到中平面110的覆盖区（ footprint)。

[0038] 每一个信号导体310具有可连接到中平面110的第一接触端子312、第二接触端子 314以及在它们之间的中间部分316，中间部分316具有从信号导体310的第一边317到第 二边318测量的第一宽度。每一个接地导体320具有可连接到中平面110的第一接触端子 322、第二接触端子324以及在它们之间的中间部分326，中间部分326具有从接地导体320 的第一边327到第二边328测量的第二宽度。优选地，接地导体320的中间部分326的第 二宽度至少是信号导体310的中间部分316的第一宽度的两倍。这可使接地导体320向对 应的信号导体310的差分对提供足够的对于邻近行中信号导体的电磁效应的屏蔽。

[0039] 在优选实施例中，接地导体320的第一接触端子322包括第一接触臂332和与第 一接触臂332隔开的第二接触臂333。第一和第二接触臂332、333在对应的信号导体310 的差分对的方向上延伸。优选地，第一和第二接触臂332、333延伸超过对应信号导体310 的平面。这可使接触臂332、333向对应的信号导体310的差分对提供足够的对于该行中邻 近信号导体的电磁效应的屏蔽。注意，对于多行330a-330f中的每一行来说，接地导体320 的第一接触臂332最接近并基本平行于邻近接地导体320的第二接触臂333，除了在一行的 末端处。

[0040] 附图将每一个信号导体310的第一接触端子312和每一个接地导体320的第一接触端子322显示为压配合接点尾线。但是，对于本领域普通技术人员来说应当显而易见 的是，第一接触端子312、322可以采用任何已知的形式来连接到中平面110，例如压装式触 点、孔中锡膏（ paste-in-hole)焊料附着、适合于焊接的接点尾线等等。在优选实施例中， 信号导体310的压配合接点尾线被定向在第一方向上，接地导体320的压配合接点尾线被

difference in the connector attached to the side of the plane;

[0026] FIG. 9B is a schematic cross-section through the traditional difference in the plane of the connector mating contact area of the connector attached to the other side as shown in Fig. 9A plane;

[0027] FIG. 9C and 9D are diagrams showing a through-hole pattern for Fig. 9A and 9B of the pattern are used in conventional differential midplane connector;

[0028] FIG IOA is a schematic cross-section through a differential according to an embodiment of the present invention, the plane of the connector mating contact area of the connector is attached to one side of the plane;

[0029] FIG IOB is a schematic cross-section through a differential according to an embodiment of the present invention, the plane of the connector mating contact area of the connector is attached to the other side of the plane;

[0030] FIG IOC and IOD is an explanatory diagram for IOA and IOB through-hole pattern diagram, which are used for example in the differential plane connector according to the present invention;

[0031] FIG IIA is a perspective view of two differential connector assembly according to an embodiment of the present invention, these two components are attached to opposite sides of the plane; and

[0032] FIG FIG IIA IIB is a schematic side view showing the two pairs of signal conductors in accordance with an embodiment of the present invention, each mounted on the opposite side of the plane and share a common through-hole.

定向在基本垂直于第一方向的第二方向上。

[0041] 参考图4和5，一行，例如行330a的信号导体310的每一个差分对，具有一个第一 接触端子312(a)和另一个第一接触端子312(b)，第一接触端子312(a)沿着第一条线350 布置且平行于所述多行，而另一第一接触端子312 (b)沿着第二条线352布置且平行于第一 条线350并与之隔开。对应接地导体320的第一接触端子322优选地沿着第三条线354布 置，第三条线354平行于第一和第二条线350、352且是与它们隔开的。在优选实施例中，第三条线354位于第一和第二条线350、352之间。这种配置，正如参考图8中的中平面110 的描述更具体加以说明的那样，提供了大致方形的用于连接到中平面110的覆盖区。

[0042] 对于一行中的信号导体310的每一个差分对，第二接触端子314沿着第四条线356 布置。第四条线356优选地是平行于所述多行。接地导体320的第二接触端子324沿着平 行于第四条线356并与之隔开的第五条线358布置。

[0043] 现在参考图4A，在那里显示了图4的替换实施例。在这个实施例中，信号导体310 是像图4中示出的那样的。然而，在那里对每一行的信号导体310提供单个第一接地导体 370，而不是如图4中所示那样提供对应于信号导体310的每一个差分对的接地导体320。 第一接地导体370基本上延伸对应行的长度，在图4A中所述行用330a'-330f'来标记。每 一个第一接地导体370具有可连接到第二差分电连接器400的对应接地导体的多个配合接 触端子374。每一个第一接地导体370的配合接触端子374的数目优选地与每一对应行的 信号导体310的差分对的数目相同。在图4A所示的实例中，有对应于信号导体310的六个 差分对的六个配合接触端子374。

[0044] 还提供多个第二接地导体380，每一个第二接地导体380被电连接到每一个第一 接地导体370，并被定向为基本垂直于第一接地导体370。每一个第二接地导体380基本上 延伸多行330a，-330f，的长度，并且每一个第二接地导体380位于每一行330a，_330f，的 邻近的信号导体

DETAILED DESCRIPTION

[0033] The present invention is not limited in the application or in the drawings the structure and arrangement of elements shown in detail in the following description set forth herein. The invention can be implemented in other ways, and can be implemented with different means or be achieved. Also, the phraseology and terminology used herein is for purposes of illustration and should not be regarded as limiting. Here, "comprises", "comprising", "having", "containing", "contains" and variations thereof, means that contains both the items listed thereafter and equivalents thereof also includes other items.

[0034] Referring to Figure 1, there is shown a diagram of an electronic system 100, the electronic system 100 according to the use of the plane 110 of the present invention. The mid-plane having a first side and a second side 114 112. Daughter card 120A, 120B, 120C and 120D on the second side 114 is electrically connected to the midplane 110. Daughter card 130A, 130B and 130C are electrically connected to the first side 112 to 110 in the plane. Note that the first side of the plane 110 daughter card 112 130A-130C in the orientation perpendicular to the daughter card 120A-120D second side 114 on the plane 110. Embodied in the concept of the present invention is particularly suitable for electronic systems such as orthogonal architecture.

[0035] Although not shown in the diagram in Figure 1, the daughter card 120A-120D and 130A-130C is electrically connected to the plane 110 by an electrical connector assembly. Figure 2 shows a preferred such an electrical connector assembly of the present invention embodiment 200. Plane between electronic system 110 includes a

310的差分对之间。第二接地导体380每个配备有可连接到中平面110的 第一接触端子。优选地，每一个第二接地导体380的第一接触端子包括多个接触引脚382， 接触引脚382被定向为垂直于信号导体310的接触引脚312的定向。注意，对于每一行330a，-330f，，邻近信号导体310的每一个差分对具有第二接地导体380的接触引脚382。 并且对于每一行330a，_330f，，该行的接触引脚382沿着第三条线354布置，正如参考图5 说明的那样。对于本领域的普通技术人员来说显而易见的是，信号导体310和接地导体320 的其它适当的配置也可以采用。

[0045] 现在参考图6和7，显示了电连接器组件200的第二差分电连接器400，第二差分 电连接器400在一侧上与第一差分电连接器300配合并在另一侧上电连接到子卡之一（例 如，子卡130C)。第二差分电连接器400包括多个晶片401，所述多个晶片401中的每一个 对应于第一差分电连接器300的所述多行（例如，图4的330a-330f)中的一行。因此，第 二差分电连接器400的晶片401的数目与第一差分电连接器300的行数相同。每一个晶片 401包括优选地由绝缘材料制成的外壳402。作为差分对来提供的多个信号导体410被容 纳在外壳402中，对应的接地导体420被放置为邻近那里。信号导体410和对应的接地导 体420在图7中更详细地示出。注意，在第一差分电连接器300的一行中提供的信号导体 310的差分对的数目与在第二差分电连接器400的对应晶片401中提供的信号导体410的 差分对的数目相同。

[0046] 每一个信号导体410具有可连接到子卡（例如，图1的120A-120D、130A-130C)之 一的第一接触端子412、可连接到第一差分电连接器300的对应信号导体310的第二接触端 子314的第二接触端子414，以及在它们之间的中间部分416。每一个接地导体420具有可 连接到子卡的第一接触端子422、可连接到第一差分电连接器300的对应接地导体320的 第二接触端子324的第二接触端子424，以及在它们之间的中间部分426。附图将每一个信 号导体410的第一接触端子412和接地导体420的第一接触端子422显示为压配合接点

daughter card 100, 120A-120D and 130A-130C plurality of signal traces routed signal. Referring to Figure 7 in more detail in the description of the plane 110. It should be noted that the number of sub-cards 120A-120D on the number of sub-card 130A-130C for 112 on the first side and a second side 114 of the display shows merely for illustrative purposes, is connected to the child in the plane 110 The actual number can be based on the electronic card system is changed.

[0036] FIG. 2 shows a daughter card can be used to 120A-120D and 130A-130C connection to the midplane electrical connector assembly 200 of FIG. 1 110. The electrical connector assembly 200 is preferably a differential electrical connector assembly. The electrical connector assembly 200 includes a first differential electrical connector 300 and a second differential electrical connector 400, a first differential electrical connector 300 is connected to the midplane 110 in the illustration, the second differential electrical connector 400 is connected to a daughter card one (Fig. 2 120A be illustrated with reference to the daughter card). Typically, one or more of the second connector 400 to be connected to each sub-card, a corresponding number of first connector 300 is connected to the midplane 110.

[0037] FIG. 3 shows a housing 302 having a differential midplane connector 300, the housing 302 is preferably formed of an insulating material. Housing 302 has side walls 304, 305, 307, 308 and a bottom end wall (not numbered). Disposed in the bottom of the housing 302 is a plurality of signal conductors as a differential to provide a plurality of ground conductors 310 and 320, each corresponding to a ground conductor 320 in the differential signal conductor 310 is positioned adjacent to and there. As

尾线。然而，对于本领域的普通技术人员来说应当显而易见的是，第一接触端子412、422可以 采取任何的形式来连接到子卡，例如压装式触点、孔中锡膏焊料连接、适合于焊接的接点尾

续寸寸。

[0047] 在优选实施例中，接地导体420是接地屏蔽，向晶片401的对应信号导体410提供 电屏蔽。然而，正如在本领域已知的那样，可以采用多个接地导体而不是单个接地屏蔽。在 接地屏蔽420的第二接触端子424中提供缝隙430。优选地，缝隙430位于邻近的信号导体 410的差分对之间。

[0048] 缝隙430中的每一个被配置来接收并电连接到接地导体440，接地导体440被定向 为垂直于晶片401的接地导体420。注意，接地导体440优选地被配置成接地片，如图6中 所示的那样。每一个接地片440电连接到晶片401的每一个接地导体420。以这种方式，接 地片440将信号导体410的差分对的邻近第二接触端子414电隔离。由接地屏蔽420和接 地片440构成的栅格状的屏蔽图案为信号导体410的差分对提供了有效的电屏蔽（例如， 对电噪声的电屏蔽）。该由接地屏蔽420和接地片440构成的栅格状的屏蔽图案被封装在罩450中，罩450优选地是绝缘的。

[0049] 现在参考图8A，显示了图1的中平面110的第一侧112的部分的顶视图，表面的一 部分被去除以显示接地平面层150。图8B显示了图1的中平面110的第二侧114的部分 (与图8A中的部分相同的部分，并且是从与图8A相同的角度来观察）的顶视图，表面的一 部分被去除以展现接地平面层170。图8A和8B中所示的中平面110的所述部分对应于连 接到中平面110的差分电连接器（例如差分电连接器300)的覆盖区。注意，图8A中所示 中平面110的第一侧112的所述部分提供与图8B中所示中平面110的第二侧114的所述 部分相似的用于差分电连接器的接口。

[0050] 正如本领域所已知的那样，中平面一般是由多层电介质基板构成的多层印刷电路 板，信号迹线或平面形成在电介质层的一层或更多层上。此外，多层印刷电路

shown in Figure 4,4A and 5, as shown in more detail, the signal conductors 310 and grounding conductor 320 is provided in multiple rows. Merely for illustrative purposes, Figure 4 shows the six lines 330a-330f, each row having six composed by the signal conductor 310 and six differential pairs corresponding to the ground conductor 320. Note that the number of signal conductors grounding conductor number of rows and each row 310, and 320 of each line may be any desired number. However, as described in conjunction with FIG. 8 in the plane 110 it will become more apparent from the above, preferably the pre-selected number of rows, the number of signal conductors 310 of each row, each row and the number of grounding conductor 320 to to ensure a substantially square planar for connection to the coverage area (footprint) 110 of.

[0038] each having a signal conductor 310 may be connected to the first contact plane 110 in the terminal 312, the second contact terminal 314 and an intermediate portion 316 therebetween, the intermediate portion 316 has a first signal conductor 310 from 317 to the second side edge of the first width 318 measurements. Each ground conductor 320 having a first contact connected to the terminal 322 in plane 110, a second contact terminal 324, and an intermediate portion 326 therebetween, the intermediate portion 326 having a ground conductor 320 from the first side 327 to the second 328 second edge width measurement. Preferably, the intermediate ground conductor 320 of the second width portion 326 is at least twice the width of the first intermediate signal conductor 310 of the portion 316. This allows the grounding conductor 320 to the differential pair signal conductors 310 should be enough for EME adjacent rows of signal conductors shielded pairs.

板典型地会具 有在电介质层的一层或更多层上形成的接地平面。通孔一般在多层印刷电路板的层之间延 伸。贯穿多层印刷电路板的所有层的通孔有时被称为穿通孔。通孔通常在各层基板形成印 刷电路板之后形成。导电通孔一般与不同层上的信号迹线相交。导电通孔还将安装在印刷 电路板上的元件互连至印刷电路板的内层上的信号迹线。

[0051] 图8A示出了接地平面150，接地平面150是在中平面110的一层电介质层上形成 的。图8B示出了接地平面170，接地平面170是在中平面110的一层电介质层上形成的。 典型地，中平面110会具有一层以上的接地平面，接地平面150、170会是不同的接地平面。 然而，接地平面150、170可以是同一接地平面，而不偏离本发明的范围。中平面110具有从 第一侧112延伸至第二侧114的多个通孔152、154。因此，通孔152、154是穿通孔式通孔。通孔152是信号连接导电通孔，而通孔154则是接地连接导电通孔。注意，中平面110的第 一侧112上的信号连接导电通孔152提供用于连接到第一侧112的差分连接器的差分对的 第一信号激励155，中平面110的第二侧114上的信号连接导电通孔152提供用于连接到第 二侧114的差分连接器的差分对的第二信号激励175。中平面110第一侧112上的接地连 接导电通孔154提供用于连接到第一侧112的差分连接器的差分对的第一接地激励157，中 平面110的第二侧114上的接地连接导电通孔154提供用于连接到第二侧114的差分连接器的差分对的第二接地激励177。

[0052] 第一信号激励155是在用于电连接到差分连接器的多行156a_156f中提供的，如 图8A中所示那样。在图8A的实例中，所示的六行156a-156f对应于图4和5中所示第一 差分电连接器300的信号导体310的差分对的六行330a-330f。对应于一信号导体差分对 的一对中的每一个信号连接导电通孔152与该对中的另一个信号连接导电通孔152电绝 缘。此外，对于与信号导体差分对相对应的每一对信号连接导电通孔152，存在围绕该对信 号连接导电通孔152的区域158，区域158没有接地平面150。该自由区域158有时称为 “反焊盘

[0039] In a preferred embodiment, the ground conductor 320 of the first contact terminal 322 includes a first contact arm 332 and contact arm 332 with the first second contact arm 333 spaced. The first and second contact arm 332 extends in the differential signal corresponding to the direction of conductor 310. Preferably, the first and second contact arms 332, 333 extend beyond the plane of the corresponding signal conductor 310. This allows a signal corresponding to the difference of adequate shielding conductor 310 EME contact arms 332, 333 to provide for the row adjacent signal conductors. Note that for multi-line 330a-330f each row, the ground conductor 332 of the first contact arm 320 and substantially parallel to the closest adjacent ground conductor 320 of the second contact arm 333, in addition to the end of a line.

[0040] drawings will first contact each signal conductor terminals 312 and 310 each of first contact terminal 322 grounding conductor 320 is shown as a press-fit contacts tails. However, those of ordinary skill should be apparent that the first contact terminals 312 and 322 may take any form known in the plane 110 to connect to, e.g., press-fit contacts, Kong Zhongxi cream (paste- in-hole) solder attachment, suitable for welding of the contact tails and so on. In a preferred embodiment, the pressure signal conductor 310 contacts with the tail wire is oriented in a first direction, the ground conductor 320 contacts the end of the press-fitting line is oriented in a second direction substantially perpendicular to the first direction.

[0041] 4 and 5, a line, such as a signal conductor line 330a 310 each differential pair having a first contact terminal 312 (a) and another first contact terminal 312 (b), section a contact terminal 312 (a) 350 disposed along a first line parallel to said

（antipad)”。已发现通过确保围绕该对信号连接导电通孔152的区域没有接地平 面150 (而在邻近对的信号连接导电通孔152之间的区域包括接地平面150)，就会显著改善 信号性能。注意，虽然该发明的优选实施例图示了大致椭圆的反焊盘158，但反焊盘158还 可以采用其它形状。参看，结合于此以供参考的美国专利No. 6，607，402。例如，反焊盘158 可以是大致矩形的或大致是数字8的形状。

[0053] 同第一差分电连接器300的信号导体310的每一个差分对的第一接触端子312的 情况（图4和5) -样，一对中的一个信号连接导电通孔152沿着第一条线160布置，而该对 的另一个信号连接导电通孔152则沿着第二条线162布置，第二条线162平行于第一条线 160并与之隔开。而且，同第一差分电连接器300信号导体310的每一个差分对的第一接触 端子312的情况一样，一对的信号连接导电通孔152是偏移的。优选地，一对的信号连接导 电通孔152是大致与行156a-156f的定向成四十五（45)度角偏移的。注意，由于一对的信 号连接导电通孔152的这种偏移，围绕该对的反焊盘158也优选地被定向为与行156a-156f的定向成四十五（45)度角。

[0054] 第一接地激励157也提供在用于电连接到差分连接器的多行156a_156f中，如图 8A中所示。对于行156a-156f中的每一行，第一接地激励157是沿着线164提供的，线164 邻近并基本平行于第一和第二条线160、162。优选地，该线164隔在第一和第二条线160、 162之间。此外，对于行156a-156f中的每一行，第一接地激励157的数目优选地大于第一 信号激励155的对的数目。在图8A的实例中，行156a-156f的第一接地激励157的数目是 七（7)，而行156a-156f的第一信号激励155的对的数目则是六（6)。

[0055] 现在参考图8B，显示了第二信号激励175，信号激励175是在用于电连接于差分连 接器的多列176a-176f中提供的。在图8B的示范性图示中，所示的六列176a_176f对应于 图4和5中所示的第一差分电连接器300的信号导体310的差分对的六行330a-330f。这 些列176a-176f正交于

plurality of rows, and the other of the first contact terminals 312 (b) are arranged along a second line 352 and parallel to the first line 350 and spaced. Grounding conductor 320 corresponds to a first contact terminal 322 preferably along the third line arrangement 354, third line 354 parallel to the first and second lines 350, 352, and they are separated. In a preferred embodiment, the third line 354 is located between the first and second lines 350,352. This configuration, as the reference plane of FIG. 8 to be described more specifically 110. As described, there is provided a substantially square footprint for connecting to the midplane 110.

[0042] For each row in a differential signal conductors 310 on the second contact terminal 314 356 arranged along the fourth line. The fourth line 356 is preferably parallel to the rows. Grounding conductor 320 of the second contact terminal 324 along a line parallel to the Article 356 and spaced from the fifth line 358 is arranged.

[0043] Referring now to Figure 4A, where FIG. 4 shows an alternative embodiment. In this embodiment, the signal conductor 310 is as shown in Figure 4 as. However, where each row of signal conductors 310 of providing a single first ground conductor 370, rather than as shown in Figure 4 as provided corresponding to the signal conductor 310 of each differential pair of the grounding conductor 320. The first ground conductor 370 extends substantially the length of the corresponding row, in line with the FIG. 4A 330a'-330f 'labeled. Each first ground conductor 370 having a plurality of connectable to the second differential electrical connector 400 of the corresponding ground conductor of the mating contact terminal 374. Differential signal conductors in contact with each of the first ground conductor 370 terminal

图8A的行156a_156f。中平面110的第一侧112上的行156a_156f 相对于中平面100的第二侧114上的列176a-176f的正交性对应并适应第一侧112上的子 卡130A-130C相对于第二侧114上的子卡120A-120D的正交性(参见图1)。

[0056] 与图8A中相同，对应于一信号导体差分对的一对中的每一个信号连接导电通孔 152是与该对中的另一个信号连接导电通孔152电绝缘的。事实上，图8A中所示穿通孔式 信号连接导电通孔152是图8B中所示相同的穿通孔式信号连接导电通孔152。因此，对于 图8A和8B所示的中平面110的该部分，第一信号激励155的数目等于第二信号激励175 的数目。注意，通过设计提供大致方形的用于连接到中平面110的覆盖区的差分电连接器 (例如第一差分电连接器300)，可以提供中平面110，其利用相同的穿通孔式信号连接导电 通孔152来将一差分电连接器连接至第一侧112并将一差分电连接器连接至第二侧114。如此，本发明的中平面设计(1)显著减少了所要求的层和中平面的尺寸，（ii)提供了比较容易的设计和制造中平面的方式，（iii)改善了所传输信号的信号特性，以及（iv)显著减 少了所制造的中平面的材料和成本。

[0057] 对于对应于一信号导体差分对的每一对信号连接导电通孔152，存在一围绕该对 信号连接导电通孔152的区域178，区域178没有接地平面170。反焊盘178与图8A的反焊 盘158相似。已发现通过确保围绕该对信号连接导电通孔152的区域没有接地平面170 (而 在邻近对的信号连接导电通孔152之间的区域包括接地平面170)，就会显著改善信号性 能。注意，虽然该发明的优选实施例图示了大致椭圆的反焊盘178，但反焊盘178还可以采 用其它形状。例如，反焊盘178可以是大致矩形的或大致是数字8的形状。

[0058] 同第一差分电连接器300的信号导体310的每一个差分对的第一接触端子312的 情况（图4和5) -样，一对中的一个信号连接导电通孔152沿着第三条线180布置，而该 对的另一个信号连接导电通孔152则沿着第四条线182布置，第四条线182平行

number 374 is preferably 310 to each corresponding row of the same number. In the example shown in FIG. 4A, the signal conductor 310 corresponding to the six differential pairs of the six mating contact terminals 374.

[0044] further providing a plurality of second ground conductors 380, each of the second ground conductor 380 is electrically connected to each of the first ground conductor 370, and is oriented substantially perpendicular to the first ground conductor 370. Each second ground conductor 380 extends substantially more rows 330a, -330f, length, and each second ground conductor 380 is located in each line 330a, _330f, the adjacent signal conductor 310 between the differential pair. Each second ground conductor 380 is equipped with a terminal connected to the first contact plane 110. Preferably, the first contact terminal of each second ground conductor 380 includes a plurality of contact pins 382, the contact pin 382 is oriented perpendicular orientation to the signal conductor contact pin 312 310. Note that for each row 330a, -330f,, each differential signal conductors 310 adjacent to the contact pin 382 has a second ground conductor 380. And for each line 330a, _330f,, the line contact pins 382 are arranged along the third line 354, as described with reference to FIG. 5. Those of ordinary skill in the art is obvious that other suitable configurations of signal conductors 310 and grounding conductor 320 may also be used.

[0045] Referring now to Figures 6 and 7, showing the electrical connector assembly 200 of the second differential electrical connector 400, a second differential electrical connector 400 on one side of the first differential electrical connector 300 and mating On the other side is electrically connected to one of the sub card (for example, a daughter

于第三条 线180并与之隔开。而且，同第一差分电连接器300的信号导体310的每一个差分对的第 一接触端子312的情况一样，一对的信号连接导电通孔152是偏移的。优选地，一对的信号 连接导电通孔152是大致与列176a-176f的定向成四十五（45)度角偏移的。注意，由于 一对的信号连接导电通孔152的这种偏移，围绕该对的反焊盘178也优选地被定向为与列176a-176f的定向成四十五(45)度角。

[0059] 第二接地激励177也提供在用于电连接到差分连接器的多列176a_176f中，如图 8B中所示。对于列176a-176f中的每一列，第二接地激励177是沿着线184提供的，线184 邻近并基本平行于第三和第四条线180、182。优选地，该线184隔在第三和第四条线180、 182之间。如上所述，第二侧114的列176a-176f正交于第一侧112的行156a_156f。因此 第三和第四条线180、182正交于图8A的第一和第二条线160、162。对于列176a_176f中的 每一列，第二接地激励177的数目优选地大于第二信号激励175的对的数目。在图8B的实 例中，列176a-176f的第二接地激励177的数目是七（7)，而列176a_176f的第二信号激励 175的对的数目则是六（6)。

[0060] 图9A-9D和10A-10D图示了根据本发明实施例与差分中平面连接器300相关联的 偏移接点尾线的优点。图9A图示了在第二接触端子区域附近穿过传统连接器的截面。图 9A显示连接器300具有成对的定向。在此使用时，“成对的”定向表明连接器被设计成具有 适合优先地彼此电耦合的信号导体对。例如，第一接触端子附近的一对中的一个导体例如 312(a)以及第一接触端子附近的所述对中的第二个导体例如312(b)之间的位移方向，提 供所述对的定向。

[0061] 多种设计技术可以用来创建连接器的成对的定向。这些设计技术可以单独地或结 合地使用。在所示的实施例中，使用屏蔽来创建对之间的优先耦合。因为每一对的信号导 体在连接器中加以定向，一对的信号导体在平行于屏蔽的方向上相互偏移，所以创建成对 的定向。

card 130C). The second differential electrical connector 400 includes a plurality of wafer 401, the wafer 401 in the plurality each corresponding to a first differential electrical connector 300 of the plurality of rows (e.g., FIG. 4 330a-330f) in a row. Therefore, the second differential electrical connector number and the first differential electrical connector 400 of the wafer 401 in the same row number 300. Each wafer 401 preferably includes a housing 402 made of insulating material. A plurality of differential pair signal conductors 410 provided in the housing 402 is accommodated in the corresponding ground conductor 420 is disposed adjacent to there. Signal conductor 410 and the corresponding ground conductor 420 is shown in greater detail in Figure 7. Note that the same number of differential signal conductors number provided in a row first differential electrical connector 300 of the differential pair 310 and signal conductors provided in the second differential electrical connector 400 of the wafer 401 corresponding to 410 pairs.

[0046] Each signal conductor 410 has a first contact terminal can be connected to the daughter card (e.g., 120A-120D 1 in FIG, 130A-130C) of 412, may be connected to the first differential electrical connector 300 The second contact 310 corresponds to a signal conductor of the second contact terminal 314 of the terminal 414, and an intermediate portion 416 therebetween. Each ground conductor 420 has a second contact of the first contact terminal can be connected to a daughter card 422, may be connected to the first differential electrical connector 320 of the corresponding ground conductor 300 of the second contact terminal 324 of the terminal 424, and of them intermediate portion 426 between. Brief contact with each of the first signal conductor terminal of the first contact terminals 410 422 412

[0062] 作为创建成对的定向的另一个技术实例，一对的信号导体可以在路径上更靠近彼 此而不是下一个最近的信号导体。

[0063] 对于差分连接器来说成对的定向是理想的，因为它增大了形成一对的导体之间的 耦合并减小了对于形成邻近对的信号导体的耦合。结果，每一个差分信号通路都更不容易 受可能引起噪声的外部电磁场的影响。此外，邻近对之间的耦合减少，从而减少了连接器内

12的串话，使该连接器能够以更卓越的信号完整性来工作。有更卓越的信号完整性，更多的信 号就可以通过该连接器来路由，或者具有更高频率的信就可以通过该连接器。

[0064] 在图9A中，形成差分对的第二接触端子314A和314B是沿着列910A排列的。这 样的排列与如图1中所示的将连接器300安装在表面112上以接收板130A上的连接器相 似，列910A是沿着平行于行330a-330f的轴（在这里显示在ζ轴上）来排列的。

[0065] 图9C示出了如果没有使用偏移的第一接触端子，接收来自如图9A中所示那样安 装的传统连接器中信号导体的第一接触端子所需的通孔图案。图9C示出了具有与图9A中 连接器的信号导体一样的沿着一个轴的排列的孔图案，该轴在这里显示在ζ轴上。

[0066] 图9B显示了连接器的截面，差分对的第二接触端子是沿着行920A排列的。这样 的排列与如图1中所示的将连接器300安装在表面114上以接收板120A上的连接器类似， 行920A是沿着平行于行330a-330f的轴（在这里显示在χ轴上）来排列的。因为板120A 垂直于板130A，所以图9B中连接器的成对的定向和排列正交于图9A中连接器的成对的定 向和排列。

[0067] 图9D示出了如果未使用偏移的第一接触端子，接收来自如图9B中所示那样安装 的传统连接器中信号导体的第一接触端子所需的通孔图案。图9D示出了具有与图9B中连 接器的信号导体一样的沿着一个

and the ground conductor 420 is shown as a press-fit contacts tails. However, those of ordinary skill in the art that should be apparent that the first contact terminal 412, 422 can take any form to connect to the daughter card, such as press-fit contacts, ??? paste solder connection, suitable for solder contacts tail

Continued begins.

[0047] In a preferred embodiment, the ground conductor 420 is a ground shield to the corresponding signal conductors 410 of the wafer 401 to provide electrical shielding. However, as is known in the art as a plurality of ground conductors may be used rather than a single ground shield. Slit 430 provided in the ground shield 420 second contact terminal 424. Preferably, a gap 430 is located between the adjacent signal conductors of the differential pair 410.

[0048] Each of the slits 430 is configured to receive and electrically connected to the ground conductor 440, ground conductor 440 is oriented perpendicular to the wafer 401, ground conductor 420. Note that the ground conductor 440 is preferably configured as a ground sheet, as shown as 6 in FIG. Electrically connecting each ground tab 440 of the wafer 401 to each ground conductor 420. In this way, the ground-chip differential signal conductors 440 410 414 adjacent to the second contact terminal electrically isolated right. By the ground shields 420 and ground plate 440 in a grid-like shielding pattern formed as a differential signal on conductor 410 provides effective electrical shielding (e.g., electrical shielding of electrical noise). The ground shield 420 and the ground plate 440 constituting the grid-like mask pattern is encapsulated in the cover 450, the cover 450 is preferably insulated.

轴的排列的孔图案，该轴在这里显示在χ轴上。

[0068] 当图9C和9D的通孔图案形成在中平面的相对侧上的时候，没有任何通孔图案的 偏移量可使同一对的两个孔都对齐。例如，如果孔930A和940A是对齐的，孔930B和940B 就不能对齐。要使用传统连接器设计来将中平面的一侧上的信号对连接到另一个，需要中 平面内的路由迹线来实现其中安装中平面的相对侧上连接器的通孔之间的连接。

[0069] 图10A-10D图示了可以用根据本发明实施例的偏移接点尾线312(a)、312(b)获得 的优点。图IOA和图IOB显示了沿着与之前在图9A和9B中显示的相同的轴（在这里分别 显示在ζ和1轴上）排列的第二接触端子314A、314B和324A。由于与接点尾线312 (a)、 312(b)的定向关联的从第二接触端子位置的四十五（45)度偏移，对于与每一差分对关联 的孔图案都存在对应的四十五（45)度偏移。因此，图IOC和IOD分别显示了接收来自安装 在图IOA和图IOB中的信号导体310的第一接触端子312(a)和312(b)所需的通孔图案。 图IOC显示了具有沿着轴ζ'的排列的孔图案，轴ζ'与图IOA中所示的第二接触端子314 的排列（在这里显示在ζ轴上）成大约四十五度的角。相似地，图IOD显示了具有沿着轴X'的排列的孔图案，轴X'与图IOB中所示的第二接触端子314的排列（在这里显示在χ轴 上）成大约四十五度的角。结果，即使中平面110的相对侧上的连接器300的配合接触部 分314具有正交的成对的定向和排列，中平面110的相对侧上的差分对的孔也可以具有相 同的图案并可以对齐。如果中平面相对侧上的孔图案对齐，中平面的相对侧中的连接器就 可以被插入相同的通孔中。

[0070] 这种排列在图IIA中示出，图IIA中示出了安装在中平面110的相对侧上的连接器300A和300B。连接器300A与连接器400A配合。连接器300B和连接器400B配合。因 为连接器400A和400B附着于以不同定向安装的印刷电路板上，所以连接器400A和400B的 成对的定向有不同的定向。在图示的实施例中，连接器400A和

[0049] Referring now to Figure 8A, shows a top view of a portion of a first side of the plane of FIG. 1 112 110, a portion of the surface removed to show a ground plane layer 150. 8B shows a plan view of a portion of a second side 114 of the 110 (Fig. 8A and the same parts, and is from the same angle as in Fig. 8A to observe) top view of a portion of the surface is removed to show ground plane layer 170. Portion 8A and 8B shown in plane 110 corresponding to an electrical connector connected to the differential midplane 110 (e.g. a differential electrical connector 300) coverage area. Note that, as shown in Fig. 8A portion of the first side 112 of the plane 110 is provided as shown in FIG. 8B portion of the second side 114 of the plane 110 similar to an electrical connector for differential interface.

[0050] As is known in the art, as the plane is normally provided by a multilayer printed circuit board consisting of a multilayer dielectric substrate, signal traces or plane is formed in one or more layers of dielectric layers. Further, a multilayer printed circuit board will typically have formed on one or more layers of the dielectric layer of the ground plane. Vias generally between layers of the multilayer printed circuit board extends. The through-hole of the multilayered printed circuit board through all layers of the through hole is sometimes called. After the formation of the through-hole is generally formed in a printed circuit board substrate layers. Conductive vias and signal traces are generally different layers intersect. Conductive vias will be installed in the signal trace on the inner component interconnect printed circuit board to a printed circuit board.

[0051] FIG. 8A shows the ground plane 150, ground plane 150 is a plane on the dielectric layer 110 is formed. 8B shows

400B是与彼此正交地安装 的。要与连接器400A和400B配合，连接器300A和300B必须相似地彼此正交地安装。因 此，连接器300A有成对的定向和排列，且连接器300B有成对的定向和排列。

[0071] 尽管连接器300A和300B的成对的定向不同，接点尾线312的偏移图案还是可使 连接器300A和300B的接点尾线312的偏移图案使用一组通孔来安装。此外，连接器300A 中每一对信号导体都可以安装在与连接器300B中的一对信号导体相同的两个通孔中。

[0072] 图IIB是安装在中平面110的相对侧上的连接器300A和300B内的一对信号导体 的侧视图。信号导体有在板的一侧上的定向和排列以及在相对侧上的定向和排列。尽管是 正交的定向，这两个对的接点尾线的偏移还是可使该接点尾线对齐，从而它们可以分别通 过通孔IIIOa和IIIOb来连接。

[0073] 这样，形成一个差分信号的两个信号被一起从中平面110的一侧上的子卡，通过 第一组连接器路由至中平面110，通过中平面110路由到第二组连接器，再路由到第二子 卡。这两个信号导体保持在一起作为一对，从而提供令人满意的信号完整特性。此外，传输 通路可以被优化用于传送差分信号。如上所述，每一个连接器可以构造成具有屏蔽、信号导 体布置或提供成对的定向的其它结构，该成对的定向在传送差分信号的时候增大信号完整 性。

[0074] 在该中平面中，仅仅使用中平面的通孔就可以实现中平面的相对侧上的信号导体 之间的连接以传送信号。不需要中平面内的任何迹线来将差分信号从中平面的一侧传送到 另一侧。在中平面中消除迹线，以及通孔和迹线之间的过渡，意味着在中平面中发生更少的 信号失真，还增大了连接器的信号完整性。此外，图8A和8B图示了差分对周围的接地间隙 可以被构造来进一步提升通过定向为差分对的中平面的信号的完整性。

[0075] 已经描述了本发明的许多优选和替换实施例。然而，对于本领域中普通技术人员 来说显而易见的是，这个发明的各种

the ground plane 170, ground plane 170 is a plane on the dielectric layer 110 is formed. Typically, the plane 110 will have more than one layer of the ground plane, the ground plane 150, 170 would be different ground plane. However, the ground plane 150, 170 may be the same ground plane without departing from the scope of the invention. The plane 110 extending from the first side 112 to a plurality of through holes 114, 152, 154, the second side. Thus, the through hole 152, 154 is a through-hole vias. Through-hole 152 is a signal connection conductive vias, and through-hole 154 is connected to ground conductive vias. Note that the signal 112 on the first side of the plane 110 connecting the conductive vias 152 provided for connection to a first side of the differential connector 112 of the first differential signal pair excitation 155 on the plane of the second side 114 110 signal connecting conductive vias 152 provides a differential connected to the second side of the differential for the connector 114 of the second excitation signal 175. The first side of the ground plane 110 connecting conductive vias 112 154 provides for connection to a first side of the connector 112 of the differential pair of the differential excitation of the first ground 157, the ground plane of the second side 114 of the connector 110 Conductive vias 154 provide for connection to the second side of the differential connector 114 of the second differential pair 177 ground excitation.

[0052] 155 is a first excitation signal for electrically connecting to a differential connector 156a_156f provided in a plurality of rows, as shown in FIG. 8A. In the example of FIG. 8A, six lines 156a-156f correspond shown in Figures 4 and 5, as shown in the first differential electrical connector 310 differential signal conductors 300 on the six lines 330a-330f. Corresponding to a differential pair

修改和改变可以在不偏离本发明的范围和精神的情况 下做出。因此，其它实施例在所附权利要求的范围之内。

of signal conductors in each pair of signal connection conductive vias 152 connected to the signal level of the other insulating conductive vias 152. In addition, for the signal conductors of the differential pair corresponding to each pair of signal connecting conductive vias 152, the existence of an area around the pair of signal connecting conductive vias 152, 158, 158 is no ground plane region 150. The free area 158 is sometimes referred to as "anti-pad (antipad)". It has been found connecting area of conductive vias 152 surrounding the signal by ensuring that there is no ground plane 150 (while the area adjacent to the signal connection between the conductive vias 152 includes a ground plane 150), it will significantly improve signal performance. Note that, although the preferred embodiment of the invention, illustrating the anti-pad 158 is substantially oval, but also the anti-pad 158 may take other shapes. Referring, incorporated herein by reference in U.S. Patent No. 6,607,402. For example, the anti-pad 158 may be generally rectangular or generally figure eight shape.

The first contact each difference

[0053] with the first differential signal conductor electrical connector 300 of the 310 cases of terminal 312 (FIG. 4 and 5) - like a pair of a signal connection conductive vias 152 160 are arranged along a first line, and another signal of the pair of connecting conductive vias 152 are arranged along a second line 162, second line 160 and spaced with 162 parallel to the first line. Also, the first contact 300 each differential signal with a first differential electrical connector 310 of the conductor 312 as a terminal case, a pair of signal connection conductive vias 152 are offset. Preferably, a pair of signal connection conductive vias 152 is approximately the line 156a-156f is

oriented forty-five (45) degrees offset. Note that since the pair of signal connecting conductive vias 152 of this shift, around the pair of anti-pad 158 is also preferably are oriented with the orientation of the rows 156a-156f to forty-five (45) degree angle.

[0054] The first ground excitation 157 is also provided for electrically connecting the connector to a differential 156a_156f multiple rows, as shown in FIG 8A. For lines 156a-156f each row, the first ground excitation 157 is provided along line 164, line 164 adjacent to and substantially parallel to the first and second lines 160,162. Preferably, the line 164 separated in the first and second lines 160, 162 between. In addition, the line 156a-156f each row, the first ground excitation number 157 is preferably greater than the first signal excitation of the number 155. In the example of FIG. 8A, the first ground line 156a-156f incentive 157 number is seven (7), and the first signal line 156a-156f of the number of 155 pairs of excitation is six (6).

[0055] Referring now to Figure 8B, shows a second excitation signal 175, the excitation signal 175 is connected to the plurality of columns 176a-176f are provided for electrically connecting to the differential. In the exemplary illustration 8B, six columns correspond 176a_176f shown in Fig. 5 and 4 in the first differential signal conductor electrical connector 300 of the differential pair of six lines 330a-330f 310's. These columns 176a-176f orthogonal rows 156a_156f in Fig. 8A. Line 156a_156f 112 110 on the first side of the plane relative to the plane of the second side 114 of the column 100 on the corresponding orthogonality 176a-176f and the first side adapted to the daughter card 112 130A-130C relative to the second daughter card side 114 120A-120D are orthogonal (see Figure 1).

[0056] the same as in Fig. 8A, corresponding to a differential pair of signal conductors in each pair of signal connection conductive vias 152 is connected to the other of the pair of electrically conductive vias 152 signal insulation. In fact, as shown in FIG. 8A through-hole signal connecting conductive vias 152 are the same signal in the through-hole connection shown in FIG. 8B conductive vias 152. Thus, for the portion of the plane 110 of FIG. 8A and 8B, the first excitation signal 155 is equal in number to the number of second signal 175 excitation. Note that, by providing a substantially square design for connecting a differential electrical connector to the midplane of the coverage area 110 (e.g., a first differential electrical connector 300) may be provided in the plane 110, which utilizes the same through-hole signal connecting conductive through-hole 152 to be a differential electrical connector connected to the first side 112 and a differential electrical connector to the second side 114. Thus, the graphic design ? present invention significantly reduces required and the plane size layer, (ii) provide a relatively easy design and manufacture of flat manner, (iii) improve the signal characteristics of the transmitted signal, and (iv) a significant reduction in the cost of materials and manufacturing in the plane.

[0057] For a signal conductor corresponding to each pair of the differential pair signal connecting conductive vias 152, around which there is a signal connection region 178 of the conductive vias 152, region 178 no ground plane 170. Anti-pad 178 of FIG. 8A anti-pad 158 is similar. By ensuring that the connection has been found around the area of the signal conductive vias 152 no ground plane 170 (while the area adjacent to the signal connection between the conductive vias 152 includes

a ground plane 170), it will significantly improve signal performance. Note that, although the preferred embodiment of the invention, illustrating the anti-pad 178 is substantially oval, but the anti-pad 178 may also adopt other shapes. For example, the anti-pad 178 may be generally rectangular or generally figure eight shape.

The first contact each difference

[0058] with the first differential signal conductor electrical connector 300 of 310 cases of terminal 312 (FIG. 4 and 5) - like a pair of a signal connection conductive vias 152 180 are arranged along the third line, and the other signal of the pair of connecting conductive vias 152 182 disposed along the fourth line, fourth line 180 and spaced with 182 parallel to the third line. Moreover, with the first differential signal conductor electrical connector 300 of the first contact 310 of each differential terminal case 312, like a pair of signal connection conductive vias 152 are offset. Preferably, a pair of signal connection conductive vias 152 is approximately the columns 176a-176f is oriented forty-five (45) degrees offset. Note that since the pair of signal connecting conductive vias 152 of this shift, around the pair of anti-pad 178 is also preferably are oriented with the orientation of the columns 176a-176f to forty-five (45) degree angle.

[0059] Second excitation 177 is also provided in the ground for electrically connecting to a differential connector 176a_176f multiple columns, as shown in FIG 8B. For columns 176a-176f each column, the second ground excitation 177 is provided along line 184, line 184 adjacent to and substantially parallel to the third and fourth lines 180,182. In the third and fourth lines 180, 182 184 separated Preferably the line. As described above, the column 176a-176f

of the second side 114 is orthogonal to the first side 112 of the line 156a_156f. Thus the third and fourth lines of the first and second lines 180, 182, 160, 162 orthogonal to Fig. 8A. For columns 176a_176f each column, the second ground excitation number 177 is preferably greater than the second signal excitation of the number 175. The number of instances in Fig. 8B, the column 176a-176f of the second ground excitation 177 is seven (7), while the second column 176a_176f excitation signal for the number 175 is six (6).

[0060] FIG. 9A-9D and 10A-10D illustrate the advantages offset the contact tails of cases and the difference in plane associated connector 300 according to embodiments of the present invention. Figure 9A illustrates a terminal area in the vicinity of the second contact through the cross section of the conventional connector. 9A shows a connector 300 having a pair of orientation. When used herein, "a pair of" orientation indicates that the connector is designed to have a suitable electrically coupled to each other preferentially signal conductor pairs. For example, a conductor of the first contact terminal near a pair such as the pair 312 (a) and the first contact terminal near the second conductor such as the direction of displacement 312 (b) between the pair provided orientation.

[0061] a variety of design techniques can be used to create a pair of connector orientation. These design techniques can be used in combination or separately. In the illustrated embodiment, the use of shielded to create priority coupling between pairs. Because each pair of signal conductors to be oriented in the connector, the signal conductor pair offset from each other in a direction parallel to the shield, so creating a pair of orientation.

[0062] As another technique to create pairs of directional instance, the signal conductor pair may be closer to each other on the path rather than the next nearest signal conductors.

[0063] For differential pair connector for orientation is ideal, because it increases the coupling between a pair of conductors and reduces the signal conductor for the formation adjacent to the coupling. As a result, each differential signal path is less susceptible to external noise may be caused by electromagnetic fields. In addition, the coupling between adjacent reduced, thereby reducing the internal connector crosstalk 12, so that the connector can be more excellent signal integrity to work. There are more excellent signal integrity, more signals can be routed through the connector, or a letter of higher frequency can be the connector through.

[0064] In Fig. 9A, forming a differential pair of second contact terminals 314A and 314B are arranged along the columns 910A. Such arrangement of the connector shown in FIG. 1 300 112 is mounted on the surface of the connector receiving plate 130A is similar to the column 910A is parallel to the line 330a-330f of the shaft (shown here in ? axis a) to order.

[0065] Figure 9C shows if no offset first contact terminal, the receiving terminal from a desired first contact as shown in the conventional connector shown 9? installed signal conductor pattern of the through holes. Figure 9C shows a connector with FIG 9? signal conductors are arranged along the same axis of a hole pattern, shown here in the shaft axis ?.

[0066] Figure 9B shows a cross-section of the connector, a second differential pair of contact terminals are arranged along the rows 920?. Such arrangement

of the connector shown in FIG. 1, 300 is mounted on the surface 114 to the connector on the receiving plate 120? Similarly, line 920? along lines 330a-330f in parallel to an axis (shown here in the ? axis a) to order. Because 120? vertical plate to plate 130?, so the connector 9B, paired orthogonal orientation and arrangement of the connector in Figure 9? paired directional and order.

[0067] Figure 9D illustrates If no offset first contact terminal, the first contact from the desired reception terminal as shown in the conventional connector 9B as shown in the installation of the signal conductor pattern of the through holes. 9D shows the signal conductors having a connector of FIG. 9B same hole pattern arranged along an axis, the axis shown here in the ? axis.

When

[0068] FIG. 9C and 9D when the through-hole pattern is formed on the opposite side of the plane, without any offset through-hole pattern allows the two holes are aligned with the same pair. For example, if the hole is aligned 930? and 940? holes 930B and 940B can not be aligned. To use the conventional connector design to the signals on one side of the plane is connected to another, routing plane need traces to connect the connector on opposite sides of the plane of the installation between which the through hole.

[0069] Figure 10A-10D illustrate the advantages may offset the contact tails according to an embodiment of the present invention 312 (a), 312 (b) obtained was. Figure IOA and IOB show along the same axis in Fig. 9A and 9B before displayed (shown here in ? and 1, respectively, the axis) of the second arrangement of contact terminals 314A, 314B and 324A. Due to the contact tails 312 (a), 312 (b) of the directional

association from forty-five (45) a second contact terminal position degree offset for differential pair with each hole patterns are associated with the presence of the corresponding four five (45) degree offset. Thus, Figure IOC and IOD show the first contact terminal 312 receives a signal from the conductor mounted in Figure IOA and IOB 310 (a) and 312 (b) through-hole pattern required. Figure IOC shows have along the axis ? 'arrangement of the hole pattern, axis ?' second contact shown in FIG IOA terminal arrangement 314 (shown here in the ? axis) to be about forty-five degree angle. Similarly, FIG IOD shows 'holes arranged in a pattern, the axis X' along the axis X having a second contact shown in Fig. IOB terminal arrangement 314 (shown here in the ? axis) to about forty-five angle degrees. As a result, even with the opposite side of the plane of the connector 110 of the contact portion 314 has 300 pairs of orthogonal orientation and arrangement of the differential pair of apertures in the opposite side of the plane 110 may also have the same pattern and can alignment. If the hole pattern on the opposite side of the plane is aligned in the opposite side of the plane of the connector can be inserted through the same hole.

[0070] Such an arrangement is shown in FIG IIA, is shown in Fig IIA connector is mounted on the opposite side of the plane 110 300A and 300B. 300A connector mating with the connector 400A. Connector 300B and 400B fit connector. Because connectors 400A and 400B is attached to a printed circuit board installed in a different orientation, the connectors 400A and 400B of the pair have different directional orientation. In the illustrated embodiment, the connector 400A and 400B are mounted orthogonally with each other. To the mating connector 400A and 400B, 300A and 300B connector must similarly

mounted orthogonally to each other. Accordingly, the connector 300A has a pair of orientation and alignment and connector 300B has a pair of orientation and alignment.

[0071] Although the connector 300A and 300B of different pairs of orientation, the contact tails 312 can shift pattern or connectors 300A and 300B of the contact tails 312 offset pattern using a set of through holes installation. In addition, the connector 300A each pair of signal conductors can be installed in the connector 300B in the same two signal conductors of a pair of through holes.

[0072] FIG IIB is mounted on the opposite side of the plane 110 of the connector 300A side view of a pair of signal conductors inside and 300B. Signal conductor has directed and arranged on one side of the plate as well as orientation and arranged on the opposite side. Despite being orthogonal orientation, which two pairs of contacts tails offset or make the contacts tails are aligned so that they can pass through holes respectively IIIOa and IIIOb to connect.

[0073] Thus, the formation of the two signals is a differential signal from the daughter card on one side of the plane 110 along the route by the first group to the mid-plane connector 110, through the midplane 110 to the second set of routing connector, then routed to the second daughter card. The two signal conductors are held together as a pair, so as to provide a satisfactory signal integrity characteristics. In addition, the transmission path can be optimized for transmitting differential signals. As described above, each connector may be configured to have a shield, or to provide a signal conductor disposed pairs of orientation of other structures, oriented in

the paired differential signal transmission when increased signal integrity.

[0074] In the mid-plane, only the use of flat vias can connect the signal conductor to transmit a signal on the opposite side of the plane between. It does not require any trace of the plane to the differential signal transmitted from one side of the plane to the other side. In the plane to eliminate traces of transition, as well as between the vias and traces, which means less signal distortion occurs in the plane, but also increases the signal integrity of the connector. In addition, 8A and 8B illustrate the differential pair of ground clearance can be constructed around further enhance the integrity through oriented in the plane of the differential pair signals.

[0075] have been described and the replacement of the present number of preferred embodiments of the invention. However, this art is apparent to one of ordinary skill that various modifications and variations of this invention can be made without departing from the scope and spirit of the present invention the situation. Accordingly, other embodiments are within the scope of the appended claims.

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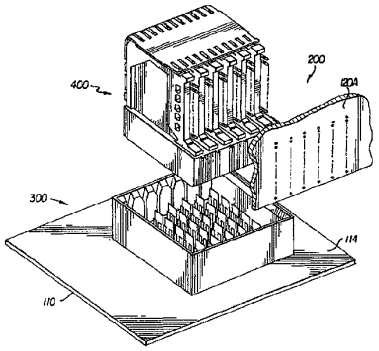
权利要求书 3 页 说明书 10 页 附图 11 页

(54)发明名称

差分电连接器组件

(57)摘要

本发明提供了用于最小化电噪声的差分电连接器、组件以及系统。一种差分连接器(400),包括在多行(330)中的接触(312)。



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1. 一种差分电连接器，具有保持在绝缘外壳中的成多行的差分对，其中所述多行中的每一行包括：

作为差分对提供的多个信号导体，每个信号导体具有可连接到印刷电路板的第一接触端子、第二接触端子以及其间的中间部分，该中间部分具有第一宽度；

差分对的信号导体中的一个的第一接触端子形成平行于所述多行的第一条线，而其它第一接触端子形成平行于第一条线并与之隔开的第二条线；

多个接地导体，每个接地导体对应由信号导体构成的差分对；

每个接地导体具有可连接到印刷电路板的第一接触端子、第二接触端子以及其间的中间部分，该中间部分具有至少为第一宽度的两倍的第二宽度；以及

每个接地导体的第一接触端子沿平行于第一和第二条线并与之隔开的第三条线布置。

2. 如权利要求 1 所述的差分电连接器，其中每个接地导体的第一接触端子还包括第一接触臂和与第一接触臂隔开的第二接触臂，该第一和第二接触臂朝向对应的差分对的信号导体延伸。

3. 如权利要求 2 所述的差分电连接器，其中对于所述多行中的每一行，接地导体的第一接触臂靠近并平行于相邻接地导体的第二接触臂。

4. 如权利要求 2 所述的差分电连接器，其中每个信号导体的第一接触端子包括在第一方向中定向的接触引脚，每个接地导体的第一和第二接触臂各自还包括基本垂直于第一方向定向的接触引脚。

5. 如权利要求 1 所述的差分电连接器，其中所述第三条线位于第一和第二条线之间。

6. 如权利要求 1 所述的差分电连接器，其中对于所述多行中的每一行，信号导体的第二接触端子沿第四条线布置，接地导体的第二接触端子沿平行于第四条线并与之隔开的第五条线布置。

7. 如权利要求 1 所述的差分电连接器，其中行的数目、这些行中每一行的信号导体的数目以及这些行中每一行的接地导体的数目是预先选择的，以确保信号导体和接地导体的第一接触端子形成用于连接到印刷电路板的基本方形的覆盖区。

8. 一种差分电连接器组件，其包括：

第一差分电连接器，具有保持在第一绝缘外壳中成多行的差分对，其中该多行中的每一行包括：

作为差分对提供的多个第一信号导体，每个第一信号导体具有可连接到第一印刷电路板的第一接触端子、第二接触端子以及其间的中间部分；

差分对的第一信号导体中的一个的第一接触端子形成平行于所述多行的第一条线，而其它第一接触端子形成平行于第一条线并与之隔开的第二条线；

多个第一接地导体，每个第一接地导体对应由第一信号导体构成的差分对；

每个第一接地导体具有可连接到第一印刷电路板的第一接触端子、第二接触端子以及其间的中间部分；

每个第一接地导体的第一接触端子沿平行于第一和第二条线并与之隔开的第三条线布置；

第二差分电连接器，具有在多个晶片中提供的差分对，其中该多个晶片中的每一个对应第一差分电连接器的所述多行中的一行，并包括：

第二绝缘外壳；

作为差分对提供并保持在第二绝缘外壳中的多个第二信号导体，每个第二信号导体具有可连接到第二印刷电路板的第一接触端子、可连接到对应的第一信号导体的第二接触端子的第二接触端子、以及其间的中间部分；

第二接地导体，具有可连接到第二印刷电路板的第一接触端子、可连接到对应的第一接地导体的第二接触端子的第二接触端子、以及其间的中间部分；并且

其中第二差分电连接器还包括第三接地导体，该第三接地导体电连接到每个晶片的第二接地导体，该第三接地导体基本垂直于每个晶片的第二接地导体而定向。

9. 如权利要求 8 所述的差分电连接器组件，其中对于第一差分电连接器，每个第一信号导体的中间部分具有第一宽度，每个第一接地导体的中间部分具有至少为第一宽度的两倍的第二宽度。

10. 如权利要求 8 所述的差分电连接器组件，其中对于第一差分电连接器，每个第一接地导体的第一接触端子还包括第一接触臂和与第一接触臂隔开的第二接触臂，该第一和第二接触臂朝向对应的差分对的第一信号导体延伸。

11. 如权利要求 10 所述的差分电连接器组件，其中对于第一差分电连接器，每个第一信号导体的第一接触端子包括在第一方向中定向的接触引脚，每个第一接地导体的第一和第二接触臂各自还包括基本垂直于第一方向定向的接触引脚。

12. 如权利要求 8 所述的差分电连接器组件，其中对于第一差分电连接器，行的数目、这些行中每一行的第一信号导体的数目以及这些行中每一行的第一接地导体的数目是预先选择的，以确保第一信号导体和第一接地导体的第一接触端子形成用于连接到第一印刷电路板的基本方形的覆盖区。

13. 如权利要求 8 所述的差分电连接器组件，其中对于第二差分电连接器，第二接地导体包括接地屏蔽，其为对应晶片的第二信号导体提供电屏蔽，并且第三接地导体包括多个接地片，每个接地片电连接每个晶片的接地屏蔽。

14. 如权利要求 13 所述的差分电连接器组件，其中对于第二差分电连接器，所述多个接地片将由第二信号导体构成的差分对的相邻的第二接触端子电隔离，使得由第二信号导体构成的每个差分对的第二接触端子被接地屏蔽和接地片电屏蔽。

15. 一种差分电互连系统，其包括：

第一差分电连接器，具有保持在第一绝缘外壳中成多行的差分对，其中该多行中的每一行包括：

作为差分对提供的多个第一信号导体，每个第一信号导体具有可连接到中平面电路板的第一侧的第一接触端子、第二接触端子以及其间的中间部分；

差分对的第一信号导体中的一个的第一接触端子形成平行于所述多行的第一条线，而其它第一接触端子形成平行于第一条线并与之隔开的第二条线；

多个第一接地导体，每个第一接地导体对应由第一信号导体构成的差分对；

每个第一接地导体具有可连接到所述中平面电路板的第一侧的第一接触端子、第二接触端子以及其间的中间部分；

其中对于第一差分电连接器，行的数目、这些行中每一行的第一信号导体的数目以及这些行中每一行的第一接地导体的数目是预先选择的，以确保第一信号导体和第一接地导

体的第一接触端子形成用于连接到所述中平面电路板的第一侧的基本方形的覆盖区；

第二差分电连接器，具有保持在第二绝缘外壳中成多列的差分对，其中这些列垂直于第一差分电连接器的所述行而定向，并且该多列中的每一列包括：

作为差分对提供的多个第二信号导体，每个第二信号导体具有可连接到所述中平面电路板的第二侧的第一接触端子、第二接触端子以及其间的中间部分；

对于由第二信号导体构成的每个差分对，一个第一接触端子沿平行于所述多列的第三条线布置，而另一个第一接触端子沿平行于第三条线并与之隔开的第四条线布置；

多个第二接地导体，每个第二接地导体对应由第二信号导体构成的差分对；

每个第二接地导体具有可连接到所述中平面电路板的第二侧的第一接触端子、第二接触端子以及其间的中间部分；

其中对于第二差分电连接器，列的数目、这些列中每一列的第二信号导体的数目以及这些列中每一列的第二接地导体的数目是预先选择的，以确保第二信号导体和第二接地导体的第一接触端子形成用于连接到所述中平面电路板的第二侧的基本方形的覆盖区；并且

所述中平面电路板包括从第一侧向第二侧延伸的多个通孔，这些通孔提供在第一侧上的第一信号激励，用于电连接到第一信号导体和第一接地导体的第一接触端子，并且这些通孔提供在第二侧上的第二信号激励，用于电连接到第二信号导体和第二接地导体的第一接触端子。

16. 如权利要求 15 所述的差分电互连系统，其中第一接地导体和第二接地导体的第一接触端子还包括第一接触臂和与第一接触臂隔开的第二接触臂。

17. 一种差分电连接器，具有保持在外壳中成多行的差分对，其中该差分电连接器包括：

所述多行中的每一行包括：

作为差分对提供的多个信号导体，每个信号导体具有可连接到印刷电路板的第一接触端子；

差分对的信号导体中的一个的第一接触端子形成平行于所述多行的第一条线，而其它第一接触端子形成平行于第一条线并与之隔开的第二条线；

与所述行的多个信号导体对应的第一接地导体，该第一接地导体基本延伸该行的长度；

多个第二接地导体，每个第二接地导体电连接到每行的第一接地导体，并基本垂直于每行的第一接地导体而定向；

每个第二接地导体基本延伸所述多行的长度；并且

每个第二接地导体位于每行中邻近的差分对之间，且每个第二接地导体具有可连接到所述印刷电路板的第一接触端子。

18. 如权利要求 17 所述的差分电连接器，其中每个信号导体的第一接触端子包括在第一方向中定向的接触引脚，每个第二接地导体的第一接触端子包括基本垂直于第一方向定向的多个接触引脚。

19. 如权利要求 18 所述的差分电连接器，其中对于每一行，具有与由信号导体构成的每个差分对邻近的第二接地导体的接触引脚。

20. 如权利要求 19 所述的差分电连接器，其中对于每一行，第二接地导体的接触引脚沿平行于第一和第二条线并与之隔开的第三条线布置。

差分电连接器组件

[0001] 相关申请的交叉引用

[0002] 本专利申请要求 2004 年 7 月 1 日提交的美国临时专利申请 No.60/584,928 以及 2004 年 12 月 24 日提交的美国临时专利申请 No.60/638,971 的优先权。

[0003] 技术领域

[0004] 本发明涉及一种差分电连接器组件。

[0005] 背景技术

[0006] 现代电子系统通常由多个印刷电路板装配而成。这种通常称为“子卡”的印刷电路板上包含诸如集成电路之类的元件。每一个子卡一般还包括一个或一个以上的连接器，所述连接器可使子卡上的元件与系统中其它子卡上的元件连通。

[0007] 一种将电子系统中的子卡互连的方式是利用中平面。中平面是一种通常大于子卡的印刷电路板，子卡经由在子卡和中平面上的连接器连接到该中平面上，并且该中平面在其中提供导电通路。也称为“信号迹线”的导电通路，在系统中的子卡之间进行互连并在它们之间提供通信。正如名称所暗示的那样，中平面在两侧上均提供连接器，可使子卡连接在中平面的两侧上。中平面可以在连接在中平面同一侧上的子卡之间路由信号，或将中平面一侧上的子卡与中平面另一侧上的子卡进行交叉连接。

[0008] 为了将连接器连接到中平面上，孔按照惯例是钻穿中平面的。所述也称为“通孔”的孔电连接到中平面中的信号迹线。通孔的内壁通常镀有导电材料，例如金属，以提供导电性。连接器配备有接触端头，例如压配合接点尾线或 SMT（表面安装技术）接点尾线，用于与所述通孔连接。

[0009] 因为电子系统已经变得更小、更快且更复杂，这普遍要求中平面在不增大尺寸的情况下，或是在许多场合下在实际上尺寸减小的同时提供更多通孔和信号迹线。这既在设计和制造中平面的过程中引起了相当大的困难，也在处理电噪声和其它电特性方面引起了相当大的困难。电噪声通常被认为是电子系统中任何不希望有的电能量，包括（但不限于）反射、电磁干扰、模式变换和诸如串话之类的不需要的耦合。

[0010] 更小、更快且更复杂的电子系统的趋势已经要求连接器在更小空间中传送更多更快的数据信号而不降低信号的电特性。通过在将连接器中的信号导体放置得更靠近，可以使得连接器在更小的空间中传送更多的信号。将信号导体放置得更靠近的主要困难是，随着信号导体之间的距离减小和信号速度的增大，信号导体之间的电噪声增大。此外，随着频率含量增加，能量损耗的可能性会更大。能量损耗可归因于阻抗间断性、模式变换、源于不完美屏蔽的泄漏，或是不希望有的与其它导体的耦合（串话）。因此，设计连接器以便控制会造成能量损耗的机制。设计构成传输通路的导体以匹配系统阻抗，强制执行一种已知的能量传递模式，使涡流减到最小，并使交替的传输通路相互绝缘。一个控制能量损耗的实例是将接地的导体放置为邻近信号接触元件，以确定阻抗并使辐射形式的能量损耗减到最小。

[0011] 一种控制连接器中的电噪声的方式是利用差分信号。差分信号是由叫做“差分对”的一对信号导体代表的信号。该对信号导体之间的电压差代表信号。如果电噪声与差分对

电磁耦合，那么对该对的每一个信号导体的影响就会是相似的。与单信号导体相比，这给出了一种对电噪声比较不敏感的差分对。然而，差分连接器的使用，特别是在中平面系统体系结构中，引起了另外的困难，因为对应于中平面的任一侧上的差分对的通孔必须每一个是在该中平面中电连接的，并且信号迹线只能在邻近的差分对之间进行路由。

[0012] 因此，所希望的是提供一种中平面和为这样的中平面而设计的差分连接器，以致力于解决上述困难。

发明内容

[0013] 在根据本发明的中平面的一个实施例中，中平面具有第一侧和与第一侧相对的第二侧，第一差分连接器的接触端子连接到第一侧，第二差分连接器的接触端子连接到第二侧。该中平面包括多个从第一侧延伸至第二侧的通孔，所述通孔提供第一侧上的第一信号激励（signallaunch）和第二侧上的第二信号激励。第一信号激励是在用于电连接到第一差分连接器的接触端子的多个行中提供的，每一行具有沿着第一条线的第一信号激励和沿着基本平行于第一条线的第二条线的第一信号激励。沿着第一和第二条线的第一信号激励是偏移的，从而沿着第一条线的第一信号激励和沿着第二条线的邻近的第一信号激励对应于第一差分连接器的差分对。第二信号激励是在用于电连接到第二差分连接器的接触端子的多个列中提供的，每一列具有沿着第三条线的第二信号激励和沿着基本平行于第三条线的第四条线的第二信号激励。沿着第三和第四条线的第二信号激励是偏移的，从而沿着第三条线的第二信号激励和沿着第四条线的邻近的第二信号激励对应于第二差分连接器的差分对。

附图说明

[0014] 附图没有打算按比例来绘制。在附图中，在不同图中举例说明的每一个同样的或几乎完全相同的部件都是用相似的数字来表示的。为了清楚，不是所有部件都在每一幅图中被加以标注。在附图中：

[0015] 图 1 是电子系统的透视图，该系统利用了根据本发明实施例的中平面；

[0016] 图 2 是根据本发明实施例的差分电连接器组件的部分分解图，该电连接器组件可以用在图 1 的电子系统中；

[0017] 图 3 是图 2 中所示差分中平面连接器的透视图；

[0018] 图 4 是透视图，示出了根据本发明实施例的图 3 中显示的差分中平面连接器的差分对信号导体和对应接地导体的行；

[0019] 图 4A 是图 4 的替换实施例，示出了图 3 中所示的差分中平面连接器的差分对信号导体以及对应接地导体的行；

[0020] 图 5 是底视图，示出了图 4 中所示差分中平面连接器的差分对信号导体和对应接地导体的第一接触端子；

[0021] 图 6 是图 2 中所示根据本发明实施例的差分子卡连接器的透视图，为了清楚起见，晶片是与连接器分开的；

[0022] 图 7 是图 6 的晶片的分解图，只示出了差分对信号导体和对应接地导体；

[0023] 图 8A 是图 1 的中平面一侧的部分的示意性顶视图，表面的一部分被去除以显示接

地平面层；

[0024] 图 8B 是图 1 的中平面另一侧的部分（与图 8A 相同的部分）的示意性顶视图，表面的一部分被去除以显示接地平面层；

[0025] 图 9A 是穿过传统差分中平面连接器的配合接触区的截面的示意图，该连接器附着于中平面的一侧；

[0026] 图 9B 是穿过传统差分中平面连接器的配合接触区的截面的示意图，该连接器附着于图 9A 中所示中平面的另一侧；

[0027] 图 9C 和 9D 是示出了用于图 9A 和 9B 的通孔图案的图，所述图案分别用于传统差分中平面连接器；

[0028] 图 10A 是穿过根据本发明实施例的差分中平面连接器的配合接触区的截面的示意图，该连接器附着于中平面的一侧；

[0029] 图 10B 是穿过根据本发明实施例的差分中平面连接器的配合接触区的截面的示意图，该连接器附着于中平面的另一侧；

[0030] 图 10C 和 10D 是说明用于图 10A 和 10B 的通孔图案的图，其分别用于根据本发明实施例的差分中平面连接器；

[0031] 图 11A 是根据本发明实施例的两个差分连接器组件的透视图，这两个组件附着于中平面的相对侧；以及

[0032] 图 11B 是图 11A 的示意性侧视图，示出了根据本发明实施例的各自安装在中平面的相对侧上并共享公用通孔的两对信号导体。

具体实施方式

[0033] 本发明在应用时不受限于在下面的说明中阐述的或在附图中示出的结构和元件布置的细节。该发明能以其它方式加以实施，并能够以不同的手段来实施或实现。而且，在此使用的措词和术语是为了说明起见，不应当看作限制。在此“包括”、“包含”、“具有”、“含”、“含有”以及它们的变型，意味着既包含其后所列项目以及它们的等效物又包括其它项目。

[0034] 参考图 1，示出了电子系统 100 的简图，电子系统 100 利用了根据本发明的中平面 110。该中平面具有第一侧 112 和第二侧 114。子卡 120A、120B、120C 和 120D 在第二侧 114 上被电连接到中平面 110。子卡 130A、130B 和 130C 在第一侧 112 上被电连接到中平面 110。注意，中平面 110 的第一侧 112 上的子卡 130A-130C 在定向上正交于中平面 110 的第二侧 114 上的子卡 120A-120D。体现在本发明中的概念尤其适用于这样的正交体系结构的电子系统。

[0035] 尽管没有在图 1 的简图中示出，子卡 120A-120D 和 130A-130C 通过电连接器组件被电连接到中平面 110。图 2 示出了根据本发明的这种电连接器组件 200 的优选实施例。中平面 110 包括在电子系统 100 的子卡 120A-120D 和 130A-130C 之间路由信号的多条信号迹线。参考图 7 对中平面 110 进行了更详细的说明。应当指出的是，第一侧 112 上显示的子卡 130A-130C 的数目和第二侧 114 上显示的子卡 120A-120D 的数目仅仅是出于说明性的目的，连接到中平面 110 的子卡的实际数目可以依据电子系统的情况而改变。

[0036] 图 2 示出了可以用来将子卡 120A-120D 和 130A-130C 连接到图 1 的中平面 110 的电连接器组件 200。电连接器组件 200 优选地是差分电连接器组件。电连接器组件 200 包

括第一差分电连接器300和第二差分电连接器400，第一差分电连接器300在图示中连接到中平面110，第二差分电连接器400连接到子卡之一（在图2中参考子卡120A进行图示）。典型地，一个或一个以上的第二连接器400将被连接在每一个子卡，相应数目的第一连接器300被连接到中平面110。

[0037] 图3示出了具有外壳302的差分中平面连接器300，外壳302优选地是由绝缘材料构成。外壳302具有侧壁304、305、端壁307、308以及底部（没有编号）。布置在外壳302的底部中的是作为差分对提供的多个信号导体310以及多个接地导体320，每一个接地导体320对应于信号导体310的差分对并且被放置得邻近那里。正如图4、4A和5中更详细显示的那样，信号导体310和接地导体320是在多行中提供的。仅仅是出于示范的目的，图4中显示了六行330a-330f，每一行具有六个由信号导体310组成的差分对和六个对应接地导体320。注意，行数和每一行的信号导体310的数目，以及每一行的接地导体320的数目可以为任何期望的数目。然而，正如结合图8中的中平面110的说明将变得更加显而易见的那样，优选地的是预先选择行数，每一行的信号导体310的数目，以及每一行的接地导体320的数目，以确保大致方形的用于连接到中平面110的覆盖区（footprint）。

[0038] 每一个信号导体310具有可连接到中平面110的第一接触端子312、第二接触端子314以及在它们之间的中间部分316，中间部分316具有从信号导体310的第一边317到第二边318测量的第一宽度。每一个接地导体320具有可连接到中平面110的第一接触端子322、第二接触端子324以及在它们之间的中间部分326，中间部分326具有从接地导体320的第一边327到第二边328测量的第二宽度。优选地，接地导体320的中间部分326的第二宽度至少是信号导体310的中间部分316的第一宽度的两倍。这可使接地导体320向对应的信号导体310的差分对提供足够的对于邻近行中信号导体的电磁效应的屏蔽。

[0039] 在优选实施例中，接地导体320的第一接触端子322包括第一接触臂332和与第一接触臂332隔开的第二接触臂333。第一和第二接触臂332、333在对应的信号导体310的差分对的方向上延伸。优选地，第一和第二接触臂332、333延伸超过对应信号导体310的平面。这可使接触臂332、333向对应的信号导体310的差分对提供足够的对于该行中邻近信号导体的电磁效应的屏蔽。注意，对于多行330a-330f中的每一行来说，接地导体320的第一接触臂332最接近并基本平行于邻近接地导体320的第二接触臂333，除了在一行的末端处。

[0040] 附图将每一个信号导体310的第一接触端子312和每一个接地导体320的第一接触端子322显示为压配合接点尾线。但是，对于本领域普通技术人员来说应当显而易见的是，第一接触端子312、322可以采用任何已知的形式来连接到中平面110，例如压装式触点、孔中锡膏（paste-in-hole）焊料附着、适合于焊接的接点尾线等等。在优选实施例中，信号导体310的压配合接点尾线被定向在第一方向上，接地导体320的压配合接点尾线被定向在基本垂直于第一方向的第二方向上。

[0041] 参考图4和5，一行，例如行330a的信号导体310的每一个差分对，具有一个第一接触端子312(a)和另一个第一接触端子312(b)，第一接触端子312(a)沿着第一条线350布置且平行于所述多行，而另一第一接触端子312(b)沿着第二条线352布置且平行于第一条线350并与之隔开。对应接地导体320的第一接触端子322优选地沿着第三条线354布置，第三条线354平行于第一和第二条线350、352且是与它们隔开的。在优选实施例中，第

三条线 354 位于第一和第二条线 350、352 之间。这种配置，正如参考图 8 中的中平面 110 的描述更具体加以说明的那样，提供了大致方形的用于连接到中平面 110 的覆盖区。

[0042] 对于一行中的信号导体 310 的每一个差分对，第二接触端子 314 沿着第四条线 356 布置。第四条线 356 优选地是平行于所述多行。接地导体 320 的第二接触端子 324 沿着平行于第四条线 356 并与之隔开的第五条线 358 布置。

[0043] 现在参考图 4A，在那里显示了图 4 的替换实施例。在这个实施例中，信号导体 310 是像图 4 中示出的那样的。然而，在那里对每一行的信号导体 310 提供单个第一接地导体 370，而不是如图 4 中所示那样提供对应于信号导体 310 的每一个差分对的接地导体 320。第一接地导体 370 基本上延伸对应行的长度，在图 4A 中所述行用 330a'-330f'来标记。每一个第一接地导体 370 具有可连接到第二差分电连接器 400 的对应接地导体的多个配合接触端子 374。每一个第一接地导体 370 的配合接触端子 374 的数目优选地与每一对应行的信号导体 310 的差分对的数目相同。在图 4A 所示的实例中，有对应于信号导体 310 的六个差分对的六个配合接触端子 374。

[0044] 还提供多个第二接地导体 380，每一个第二接地导体 380 被电连接到每一个第一接地导体 370，并被定向为基本垂直于第一接地导体 370。每一个第二接地导体 380 基本上延伸多行 330a'-330f'的长度，并且每一个第二接地导体 380 位于每一行 330a'-330f'的邻近的信号导体 310 的差分对之间。第二接地导体 380 每个配备有可连接到中平面 110 的第一接触端子。优选地，每一个第二接地导体 380 的第一接触端子包括多个接触引脚 382，接触引脚 382 被定向为垂直于信号导体 310 的接触引脚 312 的定向。注意，对于每一行 330a'-330f'，邻近信号导体 310 的每一个差分对具有第二接地导体 380 的接触引脚 382。并且对于每一行 330a'-330f'，该行的接触引脚 382 沿着第三条线 354 布置，正如参考图 5 说明的那样。对于本领域的普通技术人员来说显而易见的是，信号导体 310 和接地导体 320 的其它适当的配置也可以采用。

[0045] 现在参考图 6 和 7，显示了电连接器组件 200 的第二差分电连接器 400，第二差分电连接器 400 在一侧上与第一差分电连接器 300 配合并在另一侧上电连接到子卡之一（例如，子卡 130C）。第二差分电连接器 400 包括多个晶片 401，所述多个晶片 401 中的每一个对应于第一差分电连接器 300 的所述多行（例如，图 4 的 330a-330f）中的一行。因此，第二差分电连接器 400 的晶片 401 的数目与第一差分电连接器 300 的行数相同。每一个晶片 401 包括优选地由绝缘材料制成的外壳 402。作为差分对来提供的多个信号导体 410 被容纳在外壳 402 中，对应的接地导体 420 被放置为邻近那里。信号导体 410 和对应的接地导体 420 在图 7 中更详细地示出。注意，在第一差分电连接器 300 的一行中提供的信号导体 310 的差分对的数目与在第二差分电连接器 400 的对应晶片 401 中提供的信号导体 410 的差分对的数目相同。

[0046] 每一个信号导体 410 具有可连接到子卡（例如，图 1 的 120A-120D、130A-130C）之一的第一接触端子 412、可连接到第一差分电连接器 300 的对应信号导体 310 的第二接触端子 314 的第二接触端子 414，以及在它们之间的中间部分 416。每一个接地导体 420 具有可连接到子卡的第一接触端子 422、可连接到第一差分电连接器 300 的对应接地导体 320 的第二接触端子 324 的第二接触端子 424，以及在它们之间的中间部分 426。附图将每一个信号导体 410 的第一接触端子 412 和接地导体 420 的第一接触端子 422 显示为压配合接点尾

线。然而，对于本领域的普通技术人员来说应当显而易见的是，第一接触端子 412、422 可以采取任何的形式来连接到子卡，例如压装式触点、孔中锡膏焊料连接、适合于焊接的接点尾线等等。

[0047] 在优选实施例中，接地导体 420 是接地屏蔽，向晶片 401 的对应信号导体 410 提供电屏蔽。然而，正如在本领域已知的那样，可以采用多个接地导体而不是单个接地屏蔽。在接地屏蔽 420 的第二接触端子 424 中提供缝隙 430。优选地，缝隙 430 位于邻近的信号导体 410 的差分对之间。

[0048] 缝隙 430 中的每一个被配置来接收并电连接到接地导体 440，接地导体 440 被定向为垂直于晶片 401 的接地导体 420。注意，接地导体 440 优选地被配置成接地片，如图 6 中所示的那样。每一个接地片 440 电连接到晶片 401 的每一个接地导体 420。以这种方式，接地片 440 将信号导体 410 的差分对的邻近第二接触端子 414 电隔离。由接地屏蔽 420 和接地片 440 构成的栅格状的屏蔽图案为信号导体 410 的差分对提供了有效的电屏蔽（例如，对电噪声的电屏蔽）。该由接地屏蔽 420 和接地片 440 构成的栅格状的屏蔽图案被封装在罩 450 中，罩 450 优选地是绝缘的。

[0049] 现在参考图 8A，显示了图 1 的中平面 110 的第一侧 112 的部分的顶视图，表面的一部分被去除以显示接地平面层 150。图 8B 显示了图 1 的中平面 110 的第二侧 114 的部分（与图 8A 中的部分相同的部分，并且是从与图 8A 相同的角度来观察）的顶视图，表面的一部分被去除以展现接地平面层 170。图 8A 和 8B 中所示的中平面 110 的所述部分对应于连接到中平面 110 的差分电连接器（例如差分电连接器 300）的覆盖区。注意，图 8A 中所示中平面 110 的第一侧 112 的所述部分提供与图 8B 中所示中平面 110 的第二侧 114 的所述部分相似的用于差分电连接器的接口。

[0050] 正如本领域所已知的那样，中平面一般是由多层电介质基板构成的多层印刷电路板，信号迹线或平面形成在电介质层的一层或更多层上。此外，多层印刷电路板典型地会具有在电介质层的一层或更多层上形成的接地平面。通孔一般在多层印刷电路板的层之间延伸。贯穿多层印刷电路板的所有层的通孔有时被称为穿通孔。通孔通常在各层基板形成印刷电路板之后形成。导电通孔一般与不同层上的信号迹线相交。导电通孔还将安装在印刷电路板上的元件互连至印刷电路板的内层上的信号迹线。

[0051] 图 8A 示出了接地平面 150，接地平面 150 是在中平面 110 的一层电介质层上形成的。图 8B 示出了接地平面 170，接地平面 170 是在中平面 110 的一层电介质层上形成的。典型地，中平面 110 会具有一层以上的接地平面，接地平面 150、170 会是不同的接地平面。然而，接地平面 150、170 可以是同一接地平面，而不偏离本发明的范围。中平面 110 具有从第一侧 112 延伸至第二侧 114 的多个通孔 152、154。因此，通孔 152、154 是穿通孔式通孔。通孔 152 是信号连接导电通孔，而通孔 154 则是接地连接导电通孔。注意，中平面 110 的第一侧 112 上的信号连接导电通孔 152 提供用于连接到第一侧 112 的差分连接器的差分对的第一信号激励 155，中平面 110 的第二侧 114 上的信号连接导电通孔 152 提供用于连接到第二侧 114 的差分连接器的差分对的第二信号激励 175。中平面 110 第一侧 112 上的接地连接导电通孔 154 提供用于连接到第一侧 112 的差分连接器的差分对的第一接地激励 157，中平面 110 的第二侧 114 上的接地连接导电通孔 154 提供用于连接到第二侧 114 的差分连接器的差分对的第二接地激励 177。

[0052] 第一信号激励 155 是在用于电连接到差分连接器的多行 156a-156f 中提供的，如图 8A 中所示那样。在图 8A 的实例中，所示的六行 156a-156f 对应于图 4 和 5 中所示第一差分电连接器 300 的信号导体 310 的差分对的六行 330a-330f。对应于一信号导体差分对的一对中的每一个信号连接导电通孔 152 与该对中的另一个信号连接导电通孔 152 电绝缘。此外，对于与信号导体差分对相对应的每一对信号连接导电通孔 152，存在围绕该对信号连接导电通孔 152 的区域 158，区域 158 没有接地平面 150。该自由区域 158 有时称为“反焊盘 (antipad)”。已发现通过确保围绕该对信号连接导电通孔 152 的区域没有接地平面 150（而在邻近对的信号连接导电通孔 152 之间的区域包括接地平面 150），就会显著改善信号性能。注意，虽然该发明的优选实施例图示了大致椭圆的反焊盘 158，但反焊盘 158 还可以采用其它形状。参看，结合于此以供参考的美国专利 No. 6,607,402。例如，反焊盘 158 可以是大致矩形的或大致是数字 8 的形状。

[0053] 同第一差分电连接器 300 的信号导体 310 的每一个差分对的第一接触端子 312 的情况（图 4 和 5）一样，一对中的一个信号连接导电通孔 152 沿着第一条线 160 布置，而该对的另一个信号连接导电通孔 152 则沿着第二条线 162 布置，第二条线 162 平行于第一条线 160 并与之隔开。而且，同第一差分电连接器 300 信号导体 310 的每一个差分对的第一接触端子 312 的情况一样，一对的信号连接导电通孔 152 是偏移的。优选地，一对的信号连接导电通孔 152 是大致与行 156a-156f 的定向成四十五 (45) 度角偏移的。注意，由于一对的信号连接导电通孔 152 的这种偏移，围绕该对的反焊盘 158 也优选地被定向为与行 156a-156f 的定向成四十五 (45) 度角。

[0054] 第一接地激励 157 也提供在用于电连接到差分连接器的多行 156a-156f 中，如图 8A 中所示。对于行 156a-156f 中的每一行，第一接地激励 157 是沿着线 164 提供的，线 164 邻近并基本平行于第一和第二条线 160、162。优选地，该线 164 隔在第一和第二条线 160、162 之间。此外，对于行 156a-156f 中的每一行，第一接地激励 157 的数目优选地大于第一信号激励 155 的对的数目。在图 8A 的实例中，行 156a-156f 的第一接地激励 157 的数目是七 (7)，而行 156a-156f 的第一信号激励 155 的对的数目则是六 (6)。

[0055] 现在参考图 8B，显示了第二信号激励 175，信号激励 175 是在用于电连接于差分连接器的多列 176a-176f 中提供的。在图 8B 的示范性图示中，所示的六列 176a-176f 对应于图 4 和 5 中所示的第一差分电连接器 300 的信号导体 310 的差分对的六行 330a-330f。这些列 176a-176f 正交于图 8A 的行 156a-156f。中平面 110 的第一侧 112 上的行 156a-156f 相对于中平面 100 的第二侧 114 上的列 176a-176f 的正交性对应并适应第一侧 112 上的子卡 130A-130C 相对于第二侧 114 上的子卡 120A-120D 的正交性（参见图 1）。

[0056] 与图 8A 中相同，对应于一信号导体差分对的一对中的每一个信号连接导电通孔 152 是与该对中的另一个信号连接导电通孔 152 电绝缘的。事实上，图 8A 中所示穿通孔式信号连接导电通孔 152 是图 8B 中所示相同的穿通孔式信号连接导电通孔 152。因此，对于图 8A 和 8B 所示的中平面 110 的该部分，第一信号激励 155 的数目等于第二信号激励 175 的数目。注意，通过设计提供大致方形的用于连接到中平面 110 的覆盖区的差分电连接器（例如第一差分电连接器 300），可以提供中平面 110，其利用相同的穿通孔式信号连接导电通孔 152 来将一差分电连接器连接至第一侧 112 并将一差分电连接器连接至第二侧 114。如此，本发明的中平面设计 (i) 显著减少了所要求的层和中平面的尺寸，(ii) 提供了比较

容易的设计和制造中平面的方式，(iii) 改善了所传输信号的信号特性，以及 (iv) 显著减少了所制造的中平面的材料和成本。

[0057] 对于对应于一信号导体差分对的每一对信号连接导电通孔 152，存在一围绕该对信号连接导电通孔 152 的区域 178，区域 178 没有接地平面 170。反焊盘 178 与图 8A 的反焊盘 158 相似。已发现通过确保围绕该对信号连接导电通孔 152 的区域没有接地平面 170（而在邻近对的信号连接导电通孔 152 之间的区域包括接地平面 170），就会显著改善信号性能。注意，虽然该发明的优选实施例图示了大致椭圆的反焊盘 178，但反焊盘 178 还可以采用其它形状。例如，反焊盘 178 可以是大致矩形的或大致是数字 8 的形状。

[0058] 同第一差分电连接器 300 的信号导体 310 的每一个差分对的第一接触端子 312 的情况（图 4 和 5）一样，一对中的一个信号连接导电通孔 152 沿着第三条线 180 布置，而该对的另一个信号连接导电通孔 152 则沿着第四条线 182 布置，第四条线 182 平行于第三条线 180 并与之隔开。而且，同第一差分电连接器 300 的信号导体 310 的每一个差分对的第一接触端子 312 的情况一样，一对的信号连接导电通孔 152 是偏移的。优选地，一对的信号连接导电通孔 152 是大致与列 176a-176f 的定向成四十五 (45) 度角偏移的。注意，由于一对的信号连接导电通孔 152 的这种偏移，围绕该对的反焊盘 178 也优选地被定向为与列 176a-176f 的定向成四十五 (45) 度角。

[0059] 第二接地激励 177 也提供在用于电连接到差分连接器的多列 176a-176f 中，如图 8B 中所示。对于列 176a-176f 中的每一列，第二接地激励 177 是沿着线 184 提供的，线 184 邻近并基本平行于第三和第四条线 180、182。优选地，该线 184 隔在第三和第四条线 180、182 之间。如上所述，第二侧 114 的列 176a-176f 正交于第一侧 112 的行 156a-156f。因此第三和第四条线 180、182 正交于图 8A 的第一和第二条线 160、162。对于列 176a-176f 中的每一列，第二接地激励 177 的数目优选地大于第二信号激励 175 的对的数目。在图 8B 的实例中，列 176a-176f 的第二接地激励 177 的数目是七 (7)，而列 176a-176f 的第二信号激励 175 的对的数目则是六 (6)。

[0060] 图 9A-9D 和 10A-10D 图示了根据本发明实施例与差分中平面连接器 300 相关联的偏移接点尾线的优点。图 9A 图示了在第二接触端子区域附近穿过传统连接器的截面。图 9A 显示连接器 300 具有成对的定向。在此使用时，“成对的”定向表明连接器被设计成具有适合优先地彼此电耦合的信号导体对。例如，第一接触端子附近的一对中的一个导体例如 312(a) 以及第一接触端子附近的所述对中的第二个导体例如 312(b) 之间的位移方向，提供所述对的定向。

[0061] 多种设计技术可以用来创建连接器的成对的定向。这些设计技术可以单独地或结合地使用。在所示的实施例中，使用屏蔽来创建对之间的优先耦合。因为每一对的信号导体在连接器中加以定向，一对的信号导体在平行于屏蔽的方向上相互偏移，所以创建成对的定向。

[0062] 作为创建成对的定向的另一个技术实例，一对的信号导体可以在路径上更靠近彼此而不是下一个最近的信号导体。

[0063] 对于差分连接器来说成对的定向是理想的，因为它增大了形成一对的导体之间的耦合并减小了对于形成邻近对的信号导体的耦合。结果，每一个差分信号通路都更不容易受可能引起噪声的外部电磁场的影响。此外，邻近对之间的耦合减少，从而减少了连接器内

的串话，使该连接器能够以更卓越的信号完整性来工作。有更卓越的信号完整性，更多的信号就可以通过该连接器来路由，或者具有更高频率的信就可以通过该连接器。

[0064] 在图 9A 中，形成差分对的第二接触端子 314A 和 314B 是沿着列 910A 排列的。这样的排列与如图 1 中所示的将连接器 300 安装在表面 112 上以接收板 130A 上的连接器相似，列 910A 是沿着平行于行 330a-330f 的轴（在这里显示在 z 轴上）来排列的。

[0065] 图 9C 示出了如果没有使用偏移的第一接触端子，接收来自如图 9A 中所示那样安装的传统连接器中信号导体的第一接触端子所需的通孔图案。图 9C 示出了具有与图 9A 中连接器的信号导体一样的沿着一个轴的排列的孔图案，该轴在这里显示在 z 轴上。

[0066] 图 9B 显示了连接器的截面，差分对的第二接触端子是沿着行 920A 排列的。这样的排列与如图 1 中所示的将连接器 300 安装在表面 114 上以接收板 120A 上的连接器类似，行 920A 是沿着平行于行 330a-330f 的轴（在这里显示在 x 轴上）来排列的。因为板 120A 垂直于板 130A，所以图 9B 中连接器的成对的定向和排列正交于图 9A 中连接器的成对的定向和排列。

[0067] 图 9D 示出了如果未使用偏移的第一接触端子，接收来自如图 9B 中所示那样安装的传统连接器中信号导体的第一接触端子所需的通孔图案。图 9D 示出了具有与图 9B 中连接器的信号导体一样的沿着一个轴的排列的孔图案，该轴在这里显示在 x 轴上。

[0068] 当图 9C 和 9D 的通孔图案形成在中平面的相对侧上的时候，没有任何通孔图案的偏移量可使同一对的两个孔都对齐。例如，如果孔 930A 和 940A 是对齐的，孔 930B 和 940B 就不能对齐。要使用传统连接器设计来将中平面的一侧上的信号对连接到另一个，需要中平面内的路由迹线来实现其中安装中平面的相对侧上连接器的通孔之间的连接。

[0069] 图 10A-10D 图示了可以用根据本发明实施例的偏移接点尾线 312(a)、312(b) 获得的优点。图 10A 和图 10B 显示了沿着与之前在图 9A 和 9B 中显示的相同的轴（在这里分别显示在 z 和 x 轴上）排列的第二接触端子 314A、314B 和 324A。由于与接点尾线 312(a)、312(b) 的定向关联的从第二接触端子位置的四十五 (45) 度偏移，对于与每一差分对关联的孔图案都存在对应的四十五 (45) 度偏移。因此，图 10C 和 10D 分别显示了接收来自安装在图 10A 和图 10B 中的信号导体 310 的第一接触端子 312(a) 和 312(b) 所需的通孔图案。图 10C 显示了具有沿着轴 z' 的排列的孔图案，轴 z' 与图 10A 中所示的第二接触端子 314 的排列（在这里显示在 z 轴上）成大约四十五度的角。相似地，图 10D 显示了具有沿着轴 x' 的排列的孔图案，轴 x' 与图 10B 中所示的第二接触端子 314 的排列（在这里显示在 x 轴上）成大约四十五度的角。结果，即使中平面 110 的相对侧上的连接器 300 的配合接触部分 314 具有正交的成对的定向和排列，中平面 110 的相对侧上的差分对的孔也可以具有相同的图案并可以对齐。如果中平面相对侧上的孔图案对齐，中平面的相对侧中的连接器就可以被插入相同的通孔中。

[0070] 这种排列在图 11A 中示出，图 11A 中示出了安装在中平面 110 的相对侧上的连接器 300A 和 300B。连接器 300A 与连接器 400A 配合。连接器 300B 和连接器 400B 配合。因为连接器 400A 和 400B 附着于以不同定向安装的印刷电路板上，所以连接器 400A 和 400B 的成对的定向有不同的定向。在图示的实施例中，连接器 400A 和 400B 是与彼此正交地安装的。要与连接器 400A 和 400B 配合，连接器 300A 和 300B 必须相似地彼此正交地安装。因此，连接器 300A 有成对的定向和排列，且连接器 300B 有成对的定向和排列。

[0071] 尽管连接器 300A 和 300B 的成对的定向不同，接点尾线 312 的偏移图案还是可使连接器 300A 和 300B 的接点尾线 312 的偏移图案使用一组通孔来安装。此外，连接器 300A 中每一对信号导体都可以安装在与连接器 300B 中的一对信号导体相同的两个通孔中。

[0072] 图 11B 是安装在中平面 110 的相对侧上的连接器 300A 和 300B 内的一对信号导体的侧视图。信号导体有在板的一侧上的定向和排列以及在相对侧上的定向和排列。尽管是正交的定向，这两个对的接点尾线的偏移还是可使该接点尾线对齐，从而它们可以分别通过通孔 1110a 和 1110b 来连接。

[0073] 这样，形成一个差分信号的两个信号被一起从中平面 110 的一侧上的子卡，通过第一组连接器路由至中平面 110，通过中平面 110 路由到第二组连接器，再路由到第二子卡。这两个信号导体保持在一起作为一对，从而提供令人满意的信号完整特性。此外，传输通路可以被优化用于传送差分信号。如上所述，每一个连接器可以构造成具有屏蔽、信号导体布置或提供成对的定向的其它结构，该成对的定向在传送差分信号的时候增大信号完整性。

[0074] 在该中平面中，仅仅使用中平面的通孔就可以实现中平面的相对侧上的信号导体之间的连接以传送信号。不需要中平面内的任何迹线来将差分信号从中平面的一侧传送到另一侧。在中平面中消除迹线，以及通孔和迹线之间的过渡，意味着在中平面中发生更少的信号失真，还增大了连接器的信号完整性。此外，图 8A 和 8B 图示了差分对周围的接地间隙可以被构造来进一步提升通过定向为差分对的中平面的信号的完整性。

[0075] 已经描述了本发明的许多优选和替换实施例。然而，对于本领域中普通技术人员来说显而易见的是，这个发明的各种修改和改变可以在不偏离本发明的范围和精神的情况下做出。因此，其它实施例在所附权利要求的范围之内。

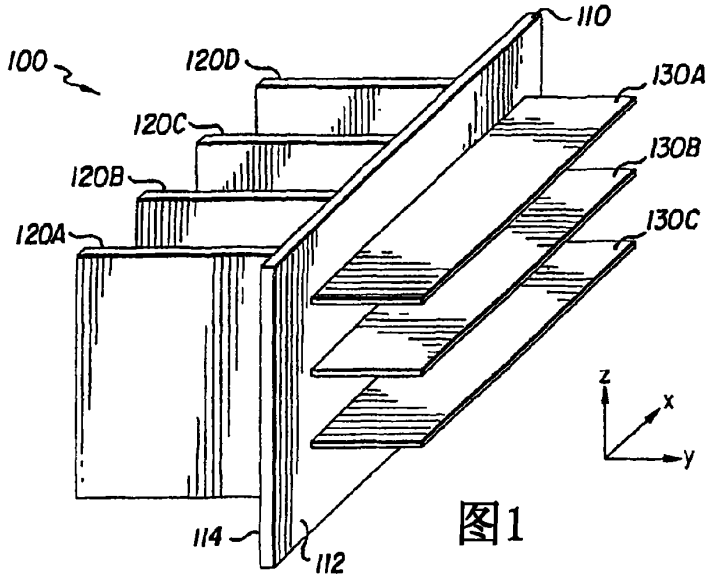

图1

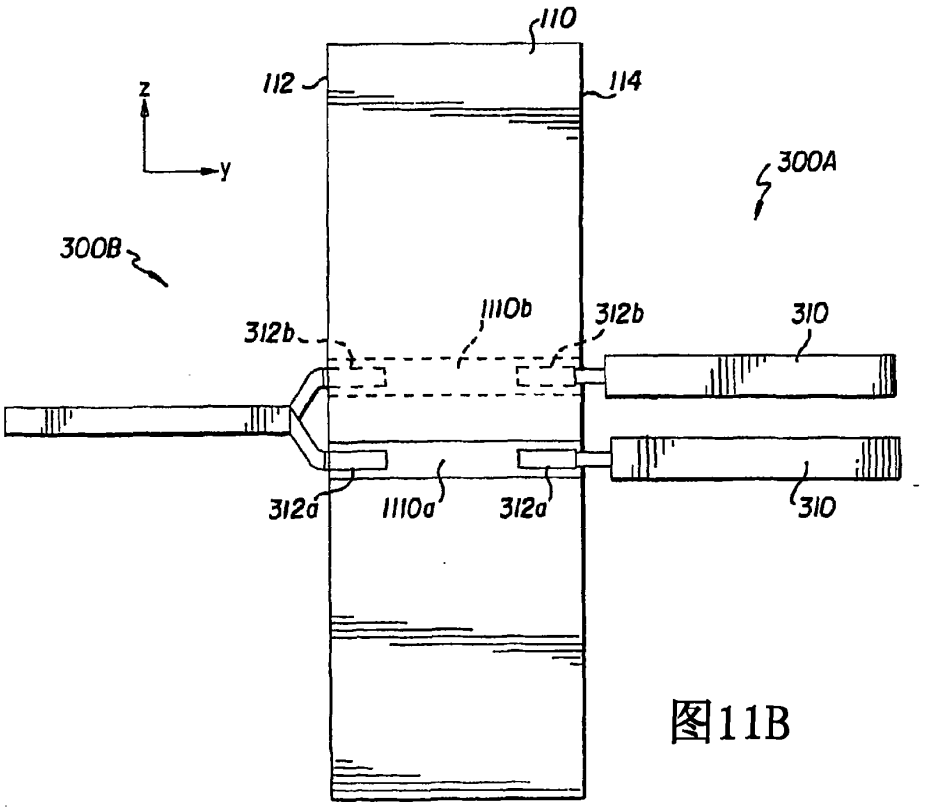

图11B

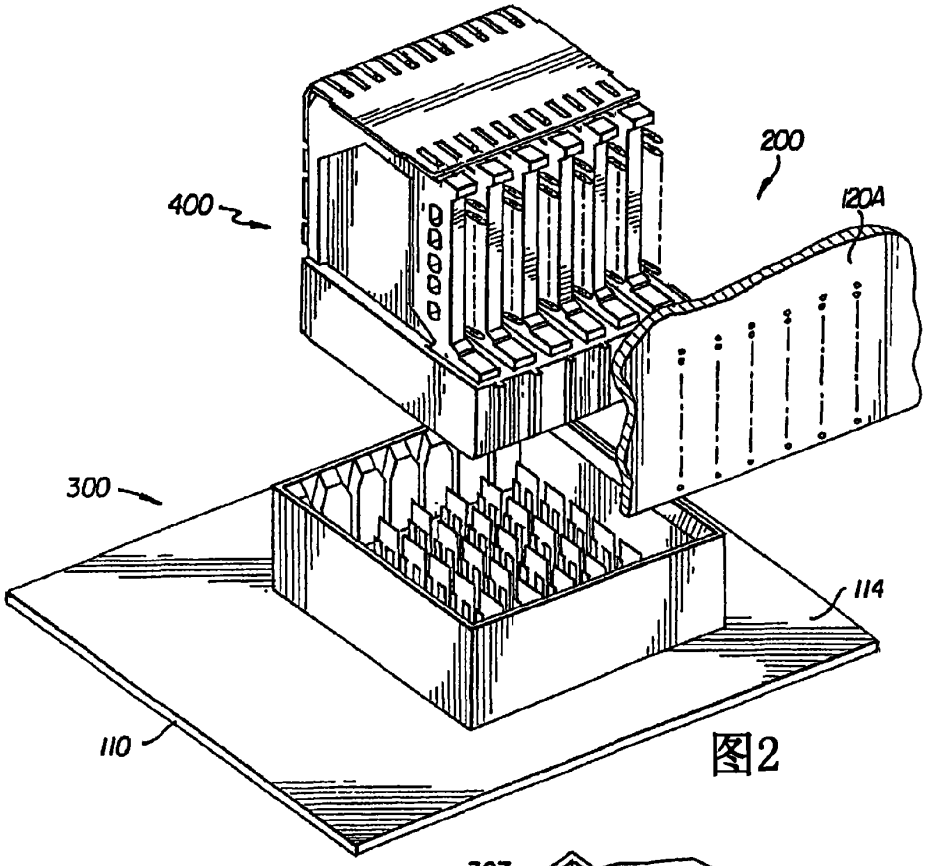

图2

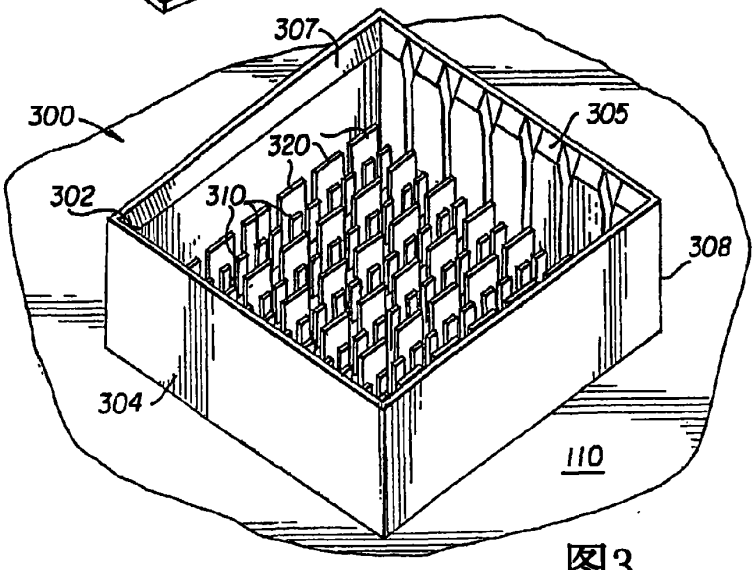

图3

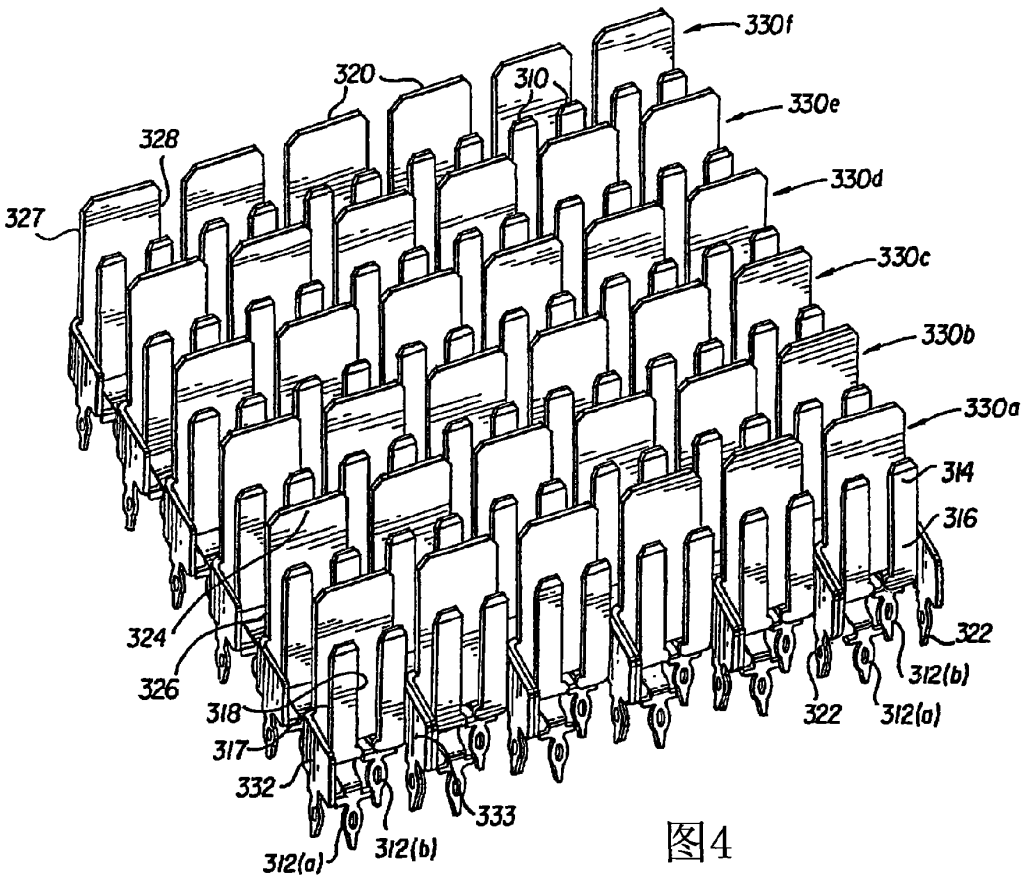

图4

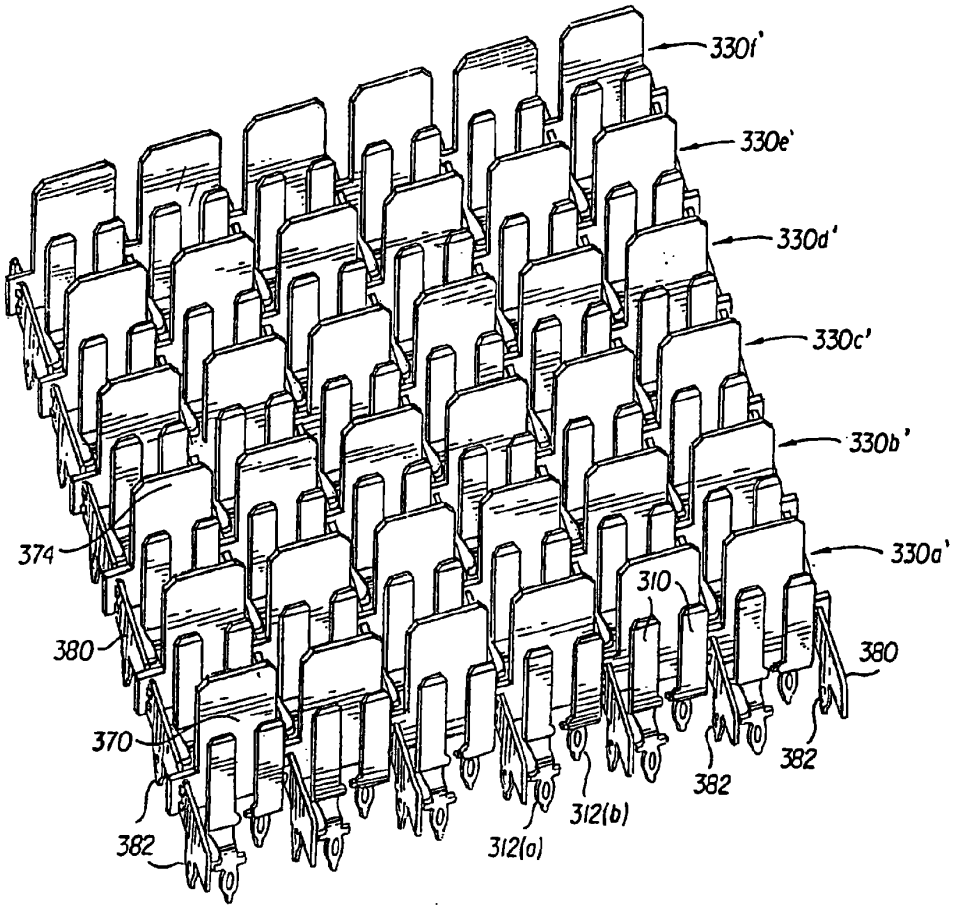

图4A

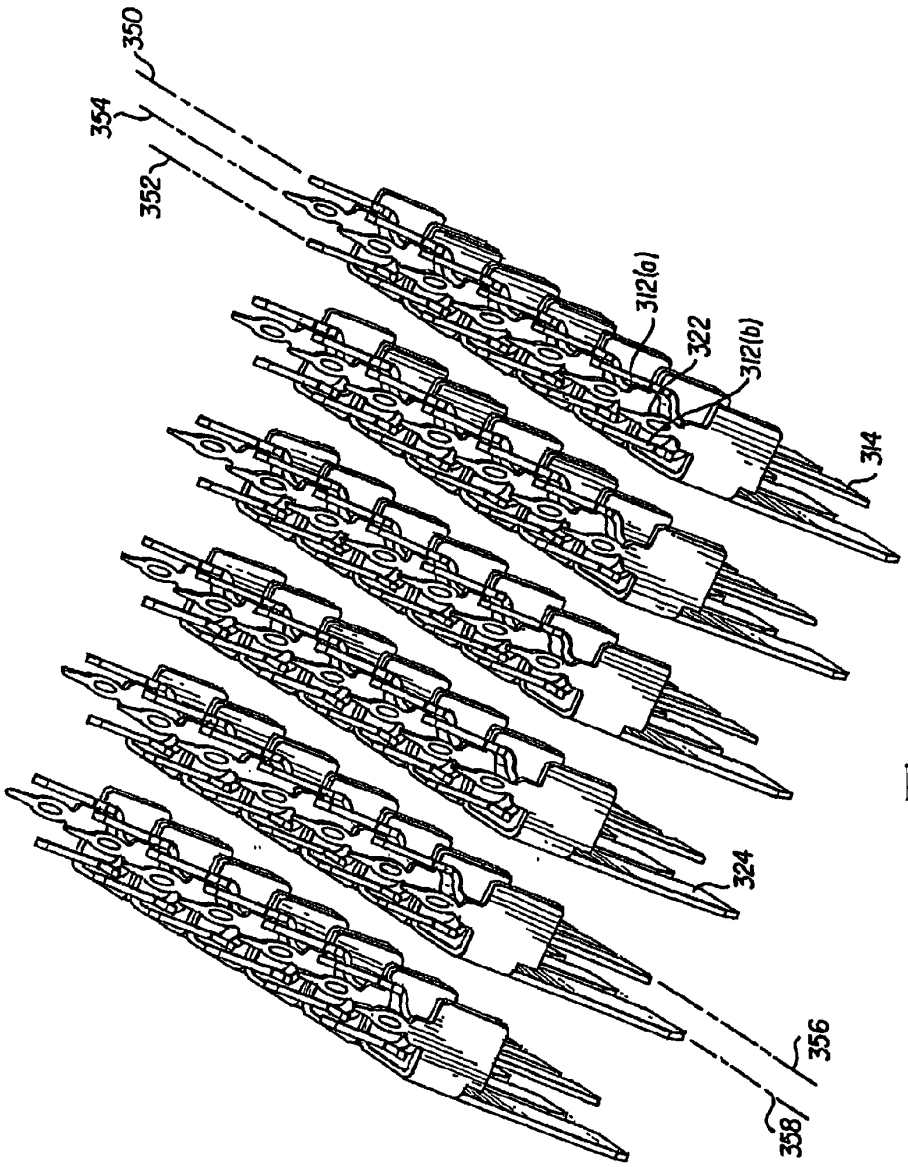

图5

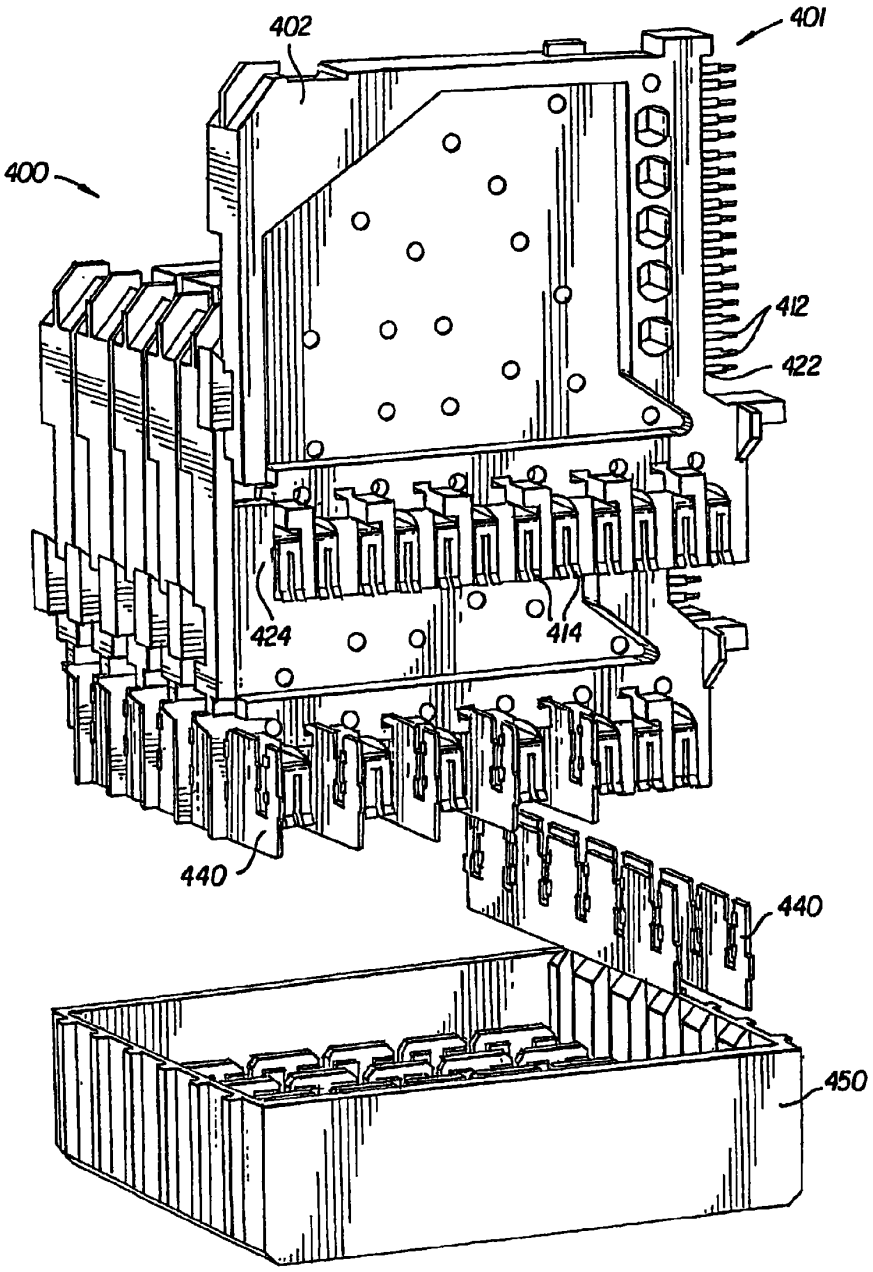

图 6

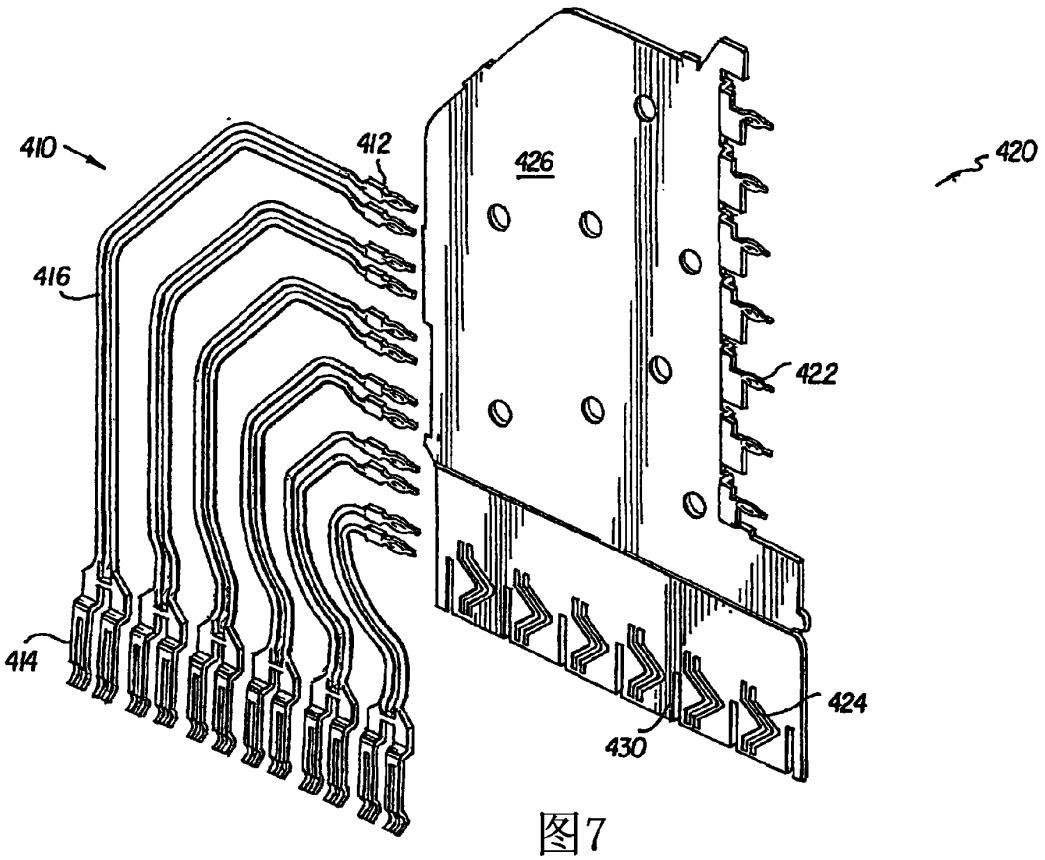

图7

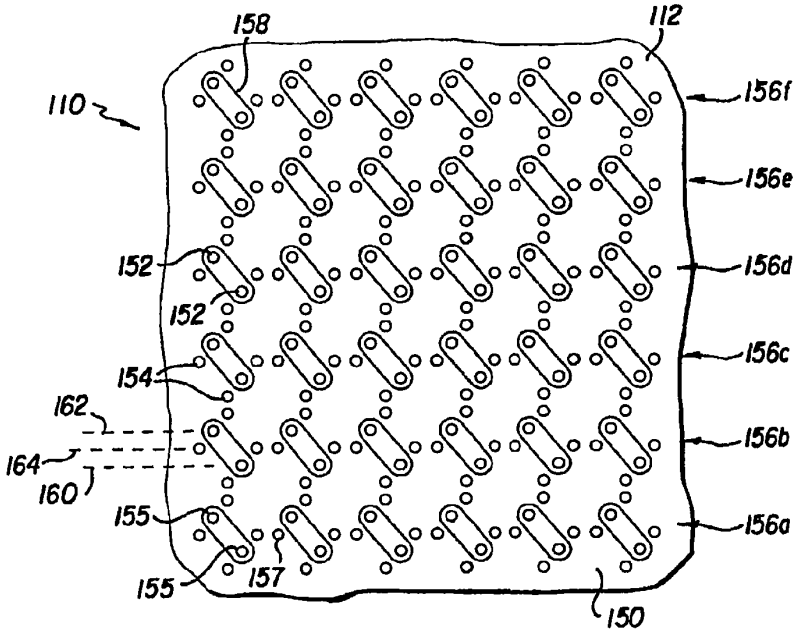

图 8A

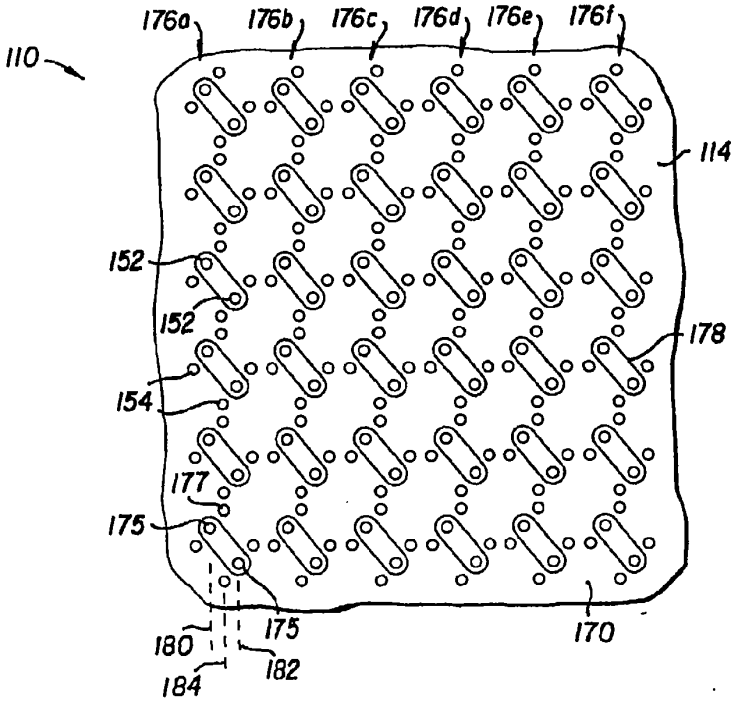

图 8B

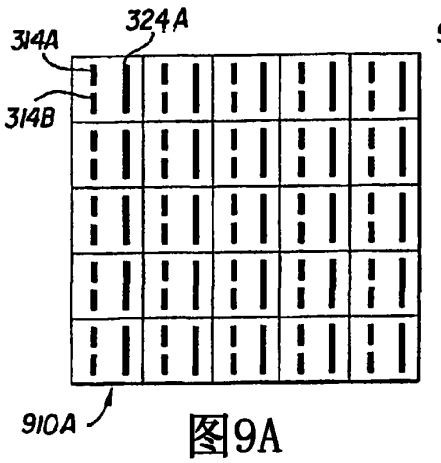

图9A

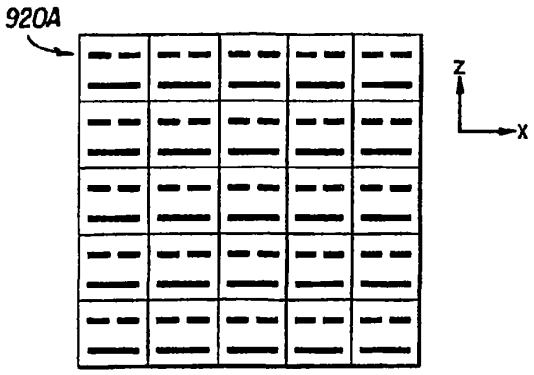

图9B

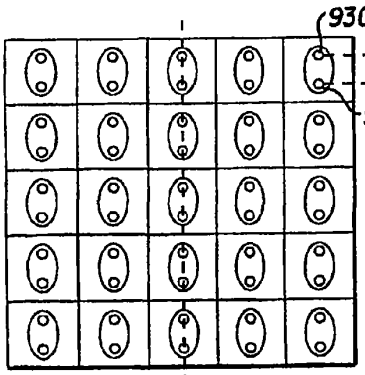

图9C
(现有技术)

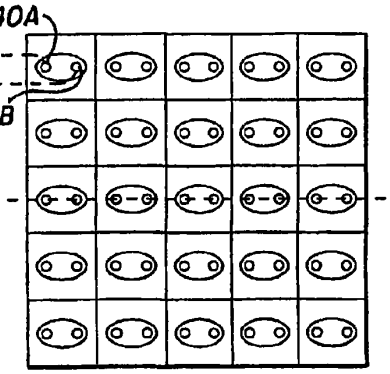

图9D
(现有技术)

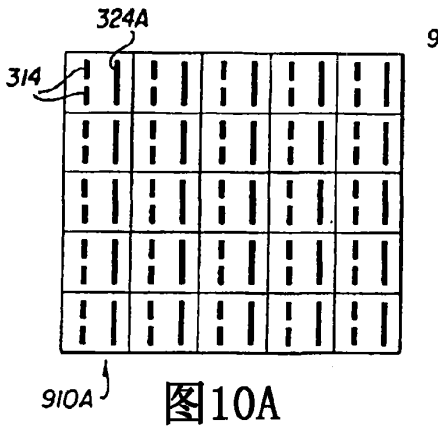

图10A

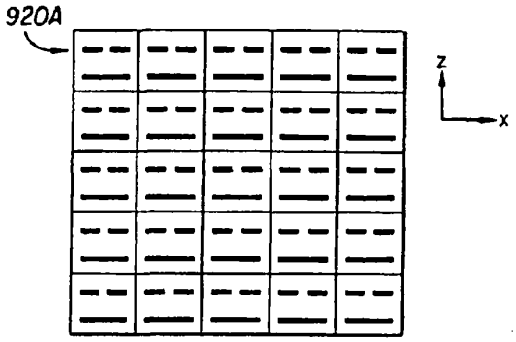

图10B

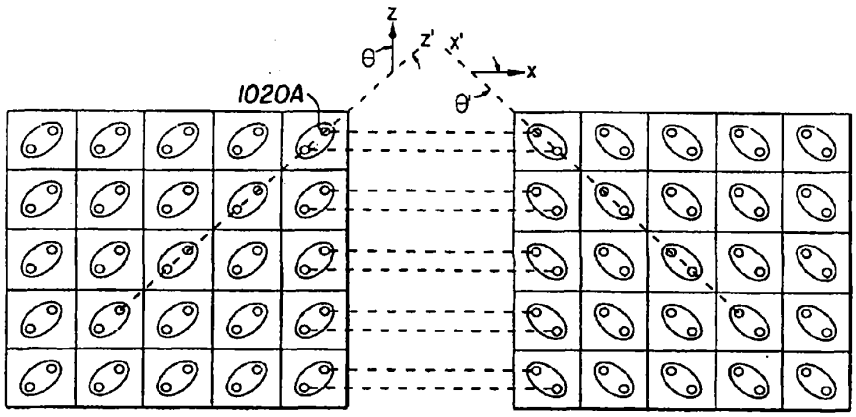

图10C

图10D

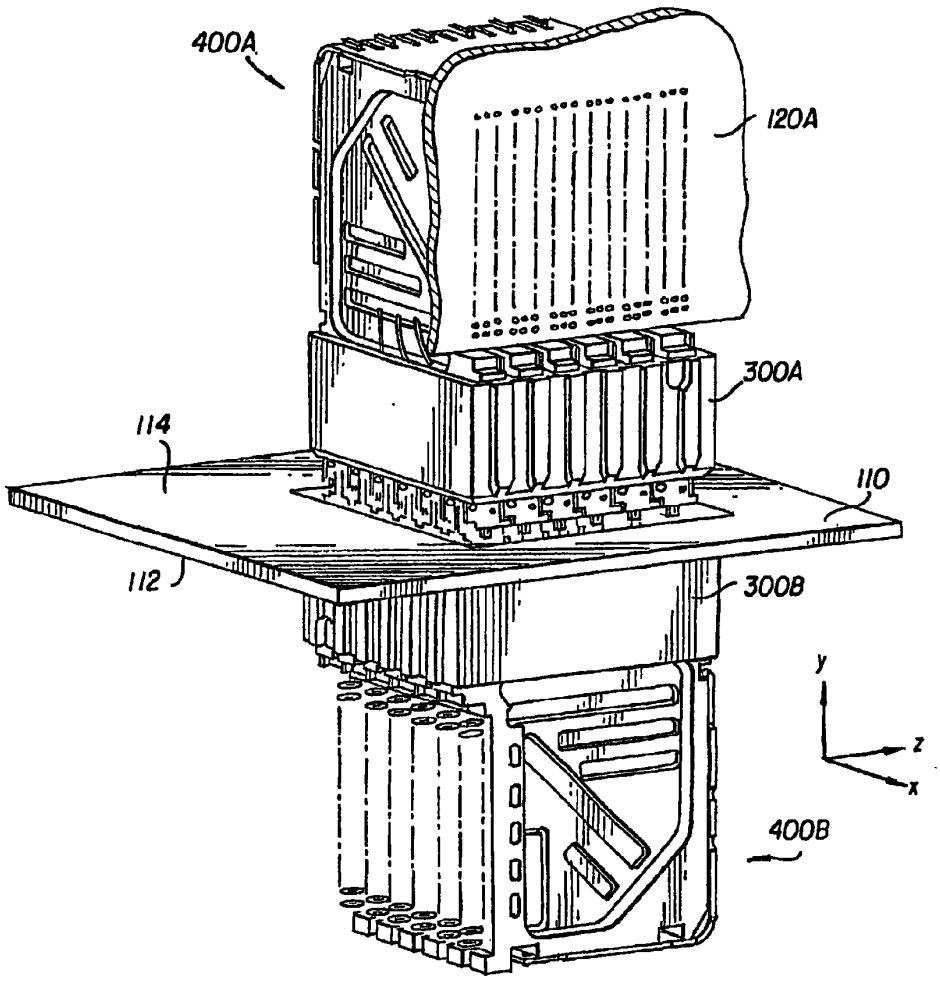

图 11A

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Publication date: 20080507
Application number: CN200680016991
Application date: 20060515
Priority: WO2006US1887020060515WO2006US18870; US20050681325P20050516US20050681325P; US20050266892200511103US20050266892;
Assignee[std]: TERADYNE INC ;
Inventor: BEHZIZ ARASH ;
Inventor[std]: ARASH BEHZIZ ;
International class[8]: H05K1/02;
Cooperative Patent class: H05K1/0251 ; H05K1/0219 ; H05K1/0222 ; H05K1/116 ; H05K2201/09718 ; H05K2201/09727 ;
Family members: CN101176389 A CN101176389 B EP1884145 A1 JP2008541484 T2 JP5199071 B2 KR101329595 B1 KR20080015107 A US2006258187 AA US7492146 BB WO06124864 A1

Title: Impedance controlled via structure

Title: 阻抗受控过孔结构

Abstract:

在一个实施例中，提供了一种用于印刷电路板的过孔结构，该过孔结构包括：信号过孔和与该信号过孔电连接的细长信号导体带。该细长信号导体带与接地导体相邻，而且从导电焊盘基本上延伸到接地导体。该细长信号导体带包括横向地向外延伸的部分，可以配置该部分，以具有建立过孔结构的阻抗的电容。

In one embodiment, there is provided a via structure for a printed circuit board, the via structure comprising: a signal via hole and an elongated signal conductor strip connected to said electrical signal vias. The elongate strip signal conductor adjacent the ground conductor and extending substantially from the conductive pads to a ground conductor. The elongate band portion comprises a signal conductor extending laterally outwardly, the portion may be configured

to have a structure of a via to the impedance of the capacitor.

Claims:

1. 一种用于印刷电路板的过孔结构，包括： 信号过孔；以及 细长信号导体带，与所述信号过孔相连，所述细长信号导体带包 括从所述信号过孔延伸而没有相邻接地导体的分段，其中该分段沿轴 线延伸，而且包括从所述轴线横向地向外凸出的部分。

2.根据权利要求1所述的过孔结构，进一步包括在所述信号过孔 附近并且与所述信号过孔间隔开的接地过孔。

3.根据权利要求1所述的过孔结构，其中，所述凸出部分进一步 包括位于所述轴线的相对侧上的拱形部分。

4.根据权利要求1所述的过孔结构，其中，所述凸出部分至少包 括如下之一：（a)弯曲形；（b)部分多边形；或者（C)锥形。

5.根据权利要求1所述的过孔结构，其中，所述凸出部分位于所 述分段的中点处。

6.根据权利要求1所述的过孔结构，其中，所述凸出部分包括外 围边缘，所述外围边缘从所述轴线横向地向外延伸，在离开所述信号 过孔的方向上靠近所述信号过孔而且向远离所述信号过孔的轴线收 缩。

7.根据权利要求1所述的过孔结构，其中，所述凸出部分具有大 致凸形的外表面。

8.根据权利要求1所述的过孔结构，其中，确定所述凸出部分的 大小，而且沿所述细长信号导体带定位所述凸出部分，以便能够具有 建立所述过孔结构的预定阻抗的电容。

9.根据权利要求1所述的过孔结构，进一步包括：位于所述分段 之外的至少一个接地导体，其中确定所述凸出部分的大小，而且沿所 述细长信号导体带定位所述凸出部分，以便能够与所述至少一个接地 导体电容耦合。

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1 a via structure for a printed circuit board, comprising: a signal vias; and an elongated signal conductor strip connected with the signal via hole, said elongated zone comprising signal conductors the signal vias extending from adjacent segments without the ground conductor, wherein the segment extends along the axis, from said axis and comprising a laterally outwardly projecting portion.

2. Via structure according to claim 1 or claim 2, further comprising in the vicinity of the signal with the signal via hole and via hole interval ? ground vias.

. According via structure according to claim 1, wherein said projecting portion further comprises three arcuate portions located on opposite sides of the axis on.

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4 via structure according to claim 1, wherein said projecting portion comprises at least one of the following: (a) a curved shape; (b) part of a polygon; or (C) cone.

5. According via structure according to claim 1, wherein said projecting portion is located at a midpoint of said segment.

6. Via structure according to claim 1 or claim 2, wherein said projecting portion comprises a peripheral edge, said peripheral edge extending laterally outwardly from said axis, away from the close to the signal vias and away from the axis of the signal vias ? contraction direction of the signal vias.

10.根据权利要求1所述的过孔结构，其中，所述分段包括位于 所述信号过孔与所述凸出部分之间的颈部。

11.根据权利要求1所述的过孔结构，其中，所述分段包括连接 部分，所述连接部分在所述凸出部分与所述信号过孔相反的的一侧处 与所述凸出部分邻接。

12. 一种用于印刷电路板的过孔结构，包括： 信号过孔； 导电焊盘，电连接到所述信号过孔； 至少一个接地导体，定位在离开所述导电焊盘禁区距离处；以及 细长信号导体带，沿轴线从所述导电焊盘纵向地延伸到与所述至 少一个接地导体相邻，而且包括从所述轴线横向地向外凸起的部分， 所述向外凸起部分位于所述禁区距离内。

13.根据权利要求12所述的过孔结构，其中，所述向外凸起部分 至少包括如下之一：（a)弯曲形状；（b)部分多边形；或者（c)锥 形。

14.根据权利要求12所述的过孔结构，其中，所述向外凸起部分 包括位于所述轴线的相对侧上的拱形部分。

15.根据权利要求12所述的过孔结构，其中，所述向外凸起部分 基本上位于所述导电焊盘的外边缘和所述至少一个接地导体的近端边 缘所确定的间隔的中点处。

16.根据权利要求12所述的过孔结构，其中，确定所述向外凸起 部分的大小，而且沿所述细长信号导体带定位所述向外凸起部分，以 便能够具有建立所述过孔结构的预定阻抗的电容。

17.根据权利要求16所述的过孔结构，其中，所述过孔结构的预 定阻抗是如下之一：（a)约33欧姆；（b)约50欧姆；（c)约75 欧姆;或者（d)约100欧姆。

18.根据权利要求12所述的过孔结构，其中，确定所述向外凸起 部分的大小，而且沿所述细长信号导体带定位所述向外凸起部分，以 便能够与所述至少一个接地导体电容耦合。

7. Via structure according to claim 1, wherein said portion having a substantially convex exterior surface protruding.

8. Via structures in accordance with claim 1, wherein determining the size of said projecting portion, and along the elongate signal conductor positioned with the convex portion, to be able to establish a predetermined impedance having a pore structure of the off capacitance.

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9 via structure according to claim 1, further comprising: at least one ground conductor is located outside of the segment, wherein determining the size of said projecting portion, and along the elongate signal conductor positioned with the projecting portion, to enable the at least one ground conductor coupling capacitance.

10. Via structure according to claim 1, wherein said segment comprises a neck portion located between said through hole and said projection signal.

. According via structure according to claim 1, wherein said connecting segment comprises a portion 11, opposite to the connecting portion at the convex portion and the signal vias at the side of the projecting portion abuts

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12 for a printed circuit board via structure, comprising: a signal via hole; conductive pads, electrically connected to the signal via hole; at least one ground conductor, positioned in leaving the conductive pads restricted area at a distance; and an elongated signal conductor strip, along the axis from the conductive pads to at least one longitudinally extending adjacent the ground conductor, and includes a projection laterally outwardly

19.根据权利要求12所述的过孔结构，进一步包括：位于所述信 号过孔附近的接地过孔，而且其中至少一个接地过孔连接到所述至少 一个接地导体，而且定位在如下之一：（a)部分地位于所述禁区距离 内；或者（b)位于所述禁区距离之外。

20.根据权利要求12所述的过孔结构，其中，所述细长信号导体 带包括位于所述信号过孔与所述向外凸起部分之间的颈部。

21.根据权利要求12所述的过孔结构，其中，所述细长信号导体 带包括连接部分，所述连接部分在所述向外凸起部分的与所述信号过 孔相反的一侧处与所述向外凸起部分邻接。

22.根据权利要求12所述的过孔结构，其中，所述导电焊盘和所 述向外凸起部分具有一般泪珠形状，该泪珠形状包括位于所述导电焊 盘与所述向外凸起部分之间的颈部。

23.—种印刷电路板，包括： 第一层，包括第一接地导体； 第二层，包括信号迹线；以及 过孔结构，电连接到所述信号迹线，所述过孔结构包括： 信号过孔，至少部分地延伸通过所述第二层； 导电焊盘，在所述第二层中，所述导电焊盘电连接到所述信号过 孔；以及 细长信号导体带，在所述第二层中，所述细长信号导体带沿轴线 从导电焊盘纵向地延伸，而且包括从所述轴线横向地向外凸起的部分， 配置所述向外凸起部分，以具有建立所述过孔结构的预定阻抗的电容； 以及 至少一个接地过孔，位于所述信号过孔附近，而且定位在离幵所 述信号过孔的禁区距离处，所述至少一个接地过孔电连接到所述第一 接地导体。

24.根据权利要求23所述的印刷电路板，其中，所述向外凸起部 分包括： 第一部分，从所述轴线横向地向外凸起；以及 第二部分，对着所述第一部分，而且从所述轴线横向地向外凸起。

25.根据权利要求23所述的印刷电路板，其中，所述向外凸起部 分至少具有如下之一：（a)弯曲形；（b)部分多边形；或者（c)锥 形。

from the axis from the part of the outward protrusion portion located within the restricted area distance.

. Via structures

13 according to claim 12, wherein said outwardly projecting portion includes at least one of the following: (a) a curved shape; (b) part of the polygon; or (c) a tapered shape.

14. Via structure according to claim according to claim 12, wherein said outwardly projecting portion includes a curved portion on the opposite side of the axis.

15. According via structure according to claim 12, wherein said outwardly projecting portion is substantially located at the outer edge of the conductive pads and said at least one ground conductor the proximal edge determined by the midpoint of the interval.

16. According via structure according to claim 12, wherein, determining the size of the outwardly projecting portion, and along the elongate strip signal conductor positioned outwardly of said raised portions, so as to be able to establish a capacitance having a predetermined impedance through the pore structure of the.

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17 via structure according to claim according to claim 16, wherein said predetermined impedance through the pore structure is one of the following: (a) from about 33 ohms; (b) from about 50 ohm; (c) about 75 ohms; or (d) of about 100 ohms.

18. According via structure according to claim 12, wherein, determining the size of the outwardly projecting portion, and along the elongate strip signal conductor

26.根据权利要求23所述的印刷电路板，其中，所述向外凸起部 分位于所述导电焊盘的外边缘和所述第一接地导体的近端边缘所确定 的间隔的近似中间处理。

27.根据权利要求23所述的印刷电路板，其中，所述信号迹线包 括预定阻抗，而且其中所述过孔结构的预定阻抗近似地等于所述信号 迹线的预定阻抗。

28.根据权利要求23所述的印刷电路板，其中，所述过孔结构的 预定阻抗是如下之一：（a)在约48欧姆到约52欧姆的范围内；（b) 约75欧姆；或者（c)约100欧姆。

29.根据权利要求23所述的印刷电路板，其中，所述信号过孔包 括约0.0125英寸的半径，所述导电焊盘包括约0.0175英寸的外径，而 所述向外凸起部分包括半圆形部分，每一个所述半圆形部分包括约为0.0125英寸的半径。

30.根据权利要求23所述的印刷电路板，其中，所述第一接地导 体是接地面。

31.根据权利要求23所述的印刷电路板，进一步包括：包括第二 接地导体的第三层，所述第二接地导体电连接到所述第一接埤导体， 其中进一步确定所述向外凸起部分的大小，而且沿所述细长信号导体 带定位所述向外凸起部分，以便能够与所述第二接地导体电容耦合。

32.根据权利要求23所述的印刷电路板，其中，所述细长信号导 体带进一步包括位于所述信号过孔与所述向外凸起部分之间的颈部。

33.根据权利要求23所述的印刷电路板，其中，所述细长信号导 体带包括位于所述向外凸起部分与所述信号迹线之间的连接部分。

34. 一种用于测试被测器件的装置，包括： 测试器主机； 测试头，连接到所述测试器主机；以及 印刷电路板，被配置以与所述测试头配合，所述印刷电路板包括： 第一层，包括第一接地导体； 第二层，包括信号迹线；以及 过孔结构，至少

positioned outwardly of said raised portion to allow coupling at least one ground conductor and said capacitor.

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19 via structure according to claim 12, further comprising: a signal ground via the vias nearby, and wherein at least one is connected to the ground via at least a grounding conductor and positioned in one of the following: (a) partially located within the restricted area of the distance; or (b) located outside the restricted area of the distance.

20. Via structure according to claim according to claim 12, wherein the elongate strip comprises a signal conductor located between the portion of the signal through hole and said projection outwardly neck.

21. According via structure according to claim 12, wherein the elongate strip comprises a signal conductor connecting portion, said connecting portion of said outwardly projecting portion and the signal vias at the opposite side of the outwardly convex portion adjacent.

22. Via structure according to claim 12, wherein said conductive pads and said outwardly projecting portion having a generally teardrop shape, which shape comprises a teardrop conductive pads projecting outwardly of said neck portion.

23.- type printed circuit board, comprising: a first layer comprising a first ground conductor; a second layer comprising signal traces; and a via structure electrically connected to the signal trace, the via structure comprising: a signal via hole, extending at least partially through said second layer; conductive pads in the second layer, the conductive pads electrically connected to the signal via hole; and an elongate signal conductor strips in the second

部分地延伸通过所述印刷电路板，而且电连接到 所述信号迹线，所述过孔结构包括： 信号过孔，至少部分地延伸通过所述印刷电路板； 导电焊盘，在所述第二层中，所述导电焊盘电连接到所述信号过孔；以及 细长信号导体带，在所述第二层中，所述细长信号导体带沿轴线 从所述导电焊盘纵向地延伸，而且包括从所述轴线横向地向外凸起的 部分，配置该向外凸起部分，以具有建立所述过孔结构的预定阻抗的 O 35.根据权利要求34所述的装置，其中，所述印刷电路板是如下 之一：（a)器件接口板，（ ID)探测器接口板，或者（ c)处理器接口 板。

36.根据权利要求34所述的装置，其中，所述细长信号导体带包 括位于信号过孔与所述向外凸起部分之间的颈部。

layer, with the elongated signal conductors extending longitudinally along the axis from the conductive pads, and includes an outwardly projecting laterally from said axis portion, configuration said outwardly projecting portion, so as to have a predetermined impedance is established through the pore structure of the capacitor; and at least one ground via, which is located near the signal via hole, and positioned in the signal vias Depart from the restricted area at a distance said at least one ground vias electrically connected to said first ground conductor.

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24 23 According to the printed circuit board of claim, wherein said outwardly projecting portion includes: a first portion projecting laterally outwardly from the axis; and a Second portion against the first portion, and projecting laterally outwardly from said axis.

Part polygon (b); (a) a curved shape;:

25 according to claim 23, wherein the printed circuit board, wherein said outwardly projecting portion having at least one of the following or (c) a tapered shape.

26. 23 in accordance with the printed circuit board of claim, wherein said outwardly projecting portion of the outer edge is located near the conductive pads and said first ground conductor approximate intermediate end edge processing interval determined.

27. 23 in accordance with the printed circuit board of claim, wherein the signal traces includes a predetermined impedance, and wherein said through-hole structure of predetermined impedance is approximately equal to the signal trace predetermined impedance lines.

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23 in accordance with the printed circuit board according to claim, wherein said predetermined impedance through-hole 28 is one of the following structures: (a) from about 48 ohms to about 52 ohms the range; (b) about 75 ohms; or (c) about 100 ohms.

29. 23 in accordance with the printed circuit board of claim, wherein the signal via hole comprises a radius of about 0.0125 inches, the conductive pads comprise an outer diameter of about 0.0175 inches, and said outwardly projecting portion includes a semi-circular portion, each of said arched portion comprises a radius of approximately 0.0125 inches.

30. 23 in accordance with the printed circuit board of claim, wherein said first ground conductor is connected to ground.

31 in accordance with the printed circuit board 23, claim further comprising: a third layer comprising a second ground conductor, said second ground conductor electrically connected to said first terminal Pi conductor, further wherein determining the size of the outwardly projecting portion, and along the elongate strip signal conductor positioned outwardly of said raised portion to allow the second ground conductor coupling capacitance.

32. According to claim 23, wherein the printed circuit board, wherein said elongate strip further comprises a signal conductor of the signal through hole and said projection between the outwardly portions neck.

33. 23 in accordance with the printed circuit board of claim, wherein the elongate strip comprises signal conductors between the outwardly

projecting portion of said signal traces connecting portion.

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34 An apparatus for testing a device under test, comprising: a host testing; test head is connected to the test host; and a printed circuit board is configured to interface with the said test head with said printed circuit board comprises: a first layer comprising a first ground conductor; a second layer comprising signal traces; and via hole structures extending at least partially through the printed circuit board, and electrically connected to the signal trace, the via structure comprising: a signal via hole, extending at least partially through the printed circuit board; conductive pads in the second layer, the conductive pads being electrically connected to the said signal vias; and an elongate signal conductor strips in the second layer, with the elongated signal conductors extending longitudinally along an axis from said conductive pads, and including outwardly projecting laterally from said axis from the section of the outwardly projecting portion configured to have a predetermined impedance over said established cell structure O 35. the apparatus according to claim 34, wherein the printed circuit board is one of the following: (a) device interface board, (ID) sensor interface board, or (c) a processor interface board.

36. The apparatus according to claim 34, wherein the elongate strip comprises a signal conductor located in the signal through hole and projecting outwardly between the neck portion.

Description:

说明书 阻抗受控过孔结构 相关申请的交叉参考 本申请要求Arash Behziz于2005年 Priority

5月16日提交的标题为 "IMPEDANCE CONTROLLED VIA STRUCTURE" 的第 60/681,325 号 美国临时申请的优先权，在此引用该申请的全部内容以供参考。

背景技术 过孔是通常通过多层印刷电路板而且在印刷电路板的层之间提供 电连接的电互连。通常，过孔使印刷电路板的一层中的迹线与印刷电 路板的另一层中的迹线连接。依次地，迹线又连接到电路、电设备、 接触焊盘、连接器等。此外，过孔本身可以包括表面接触焊盘。这样， 电路、电设备、接触焊盘、连接器等通过过孔彼此电连接。

因此，过孔与印刷电路板上的迹线组合提供通过印刷电路板的信 号路径。对于高频信号，该过孔可以呈现出沿信号路径缓慢传播高频 信号的传输线特性，而且可能影响该高频信号的保真度和完整性。鉴 于上述问题，需要改进通过印刷电路板中的过孔传播高频信号的速率。

此外，需要保持通过过孔传播的高频信号的保真度和完整性。

发明内容 在一个实施例中，一种用于印刷电路板的过孔结构包括与细长信 号导体带相连的信号过孔。该细长信号导体带具有延伸离开信号过孔 而没有相邻接地导体的分段，该延伸离开的分段沿轴线延伸，而且它 包括从该轴线横向地向外凸出的部分。

在另一个实施例中，用于印刷电路板的过孔结构包括电连接到导 电焊盘的信号过孔。接地导体定位在离开导电焊盘禁区距离处。细长 信号导体带纵向地沿轴线从导电焊盘延伸到与接地导体相邻。细长信 号导体带包括从该轴线横向地向外凸起的部分，该向外凸起部分位于 禁区距离之内。

在另一个实施例中，一种印刷电路板包括：第一层、第二层、过 孔结构以及至少一个接地过孔。第一层包括接地导体，而第二层包括 信号迹线。该过孔结构电连接到信号迹线，而且该过孔结构包括：信 号过孔，至少一部分延伸通过第二层；导电焊盘，在第二层中。该导 电焊盘电连接到信号过孔和细长信号导体带。该细长信号

Instructions impedance controlled via structures CROSS-REFERENCE TO RELATED APPLICATIONS This application claims Arash Behziz on May 16, 2005 filed entitled "IMPEDANCE CONTROLLED VIA STRUCTURE" No. 60 / 681,325 U.S. Provisional Application, the entire contents of which is hereby incorporated herein by reference.

BACKGROUND typically a via is formed through the multilayered printed circuit board and between the printed circuit board to provide electrical connection layer electrically interconnected. Typically, the through-hole printed circuit board traces another layer of the printed circuit board traces in connection. In turn, connected to the circuit traces and electrical equipment, contact pads, connectors. Moreover, vias may itself comprise a surface contact pads. Thus, circuits, electrical devices, contact pads, connectors, etc. are electrically connected through vias.

So, via a combination of traces of the printed circuit board to provide signal path through the printed circuit board. For the high-frequency signal, the vias can exhibit characteristics of the transmission line along the signal propagation path is slow high-frequency signal, and may affect the fidelity and integrity of the high-frequency signal. Given these problems, the need to improve high-frequency signal propagation through the printed circuit board through-hole rate.

In addition, the need to maintain fidelity and integrity through vias propagating high frequency signals.

SUMMARY In one embodiment, a via structure for a printed circuit board includes a signal through the elongated hole and is connected with a signal conductor. The elongated signal conductor strip extending Depart from signal vias without staging ground

导体带沿轴 线从导电焊盘纵向延伸，而且该细长信号导体带包括从该轴线横向地 向外凸起的部分。配置细长信号导体带的该向外凸起部分，以具有使 过孔结构具有预定阻抗的电容。电连接到第一接地导体的接地过孔位 于信号过孔附近，而且定位在离开该信号过孔的禁区距离之外。

上述一个或者多个实施例具有以下的一个或者多个优点。在阅读 该说明时，存在变得显而易见的其他优点。一个优点是该过孔结构可 以传送高速信号。另一个优点是该过孔结构可以保持高速信号的保真 度。又一个优点是无需显著增加成本或者制造时间，就可以实现该过 孔结构。

附图说明 通过结合附图参考下列描述，更加容易理解本发明的更多特征和 优点。

图1是包括过孔结构的印刷电路板的一个实施例的俯视图。

图2是该过孔结构的一个实施例的方框图。

图3是该过孔结构的一个实施例的方框图。

图4是多层印刷电路板的横截面图。

图5是包括该过孔结构的印刷电路板的一个实施例的横截面图。

图6是包括该过孔结构的印刷电路板的另一个实施例的横截面 图。

图7是包括过孔结构的测试器的一个实施例的方框图。

具体实施方式 图1示出包括过孔结构18的一个实施例的印刷电路板10的俯视 图。过孔结构18包括具有导电焊盘30，信号过孔24延伸通过孔（图 1中未示出）而穿过导电焊盘30。在一些实施例中，导电焊盘30可以 完全包围信号过孔24，以形成环状结构，如图1所示，或它可以仅部 分地包围信号过孔24 (未示出）。信号过孔24至少部分地通过印刷电 路板10，并且具有相关阻抗。

conductor adjacent to leave the extended segment extending along an axis, and which includes the axis projecting laterally outwardly from the part.

In another embodiment, the via structures for printed circuit board comprising electrical vias connecting the signal to the conductive pads. Depart from the ground conductor is positioned at a distance from the area of the conductive pads. Elongated signal conductor strip extends longitudinally adjacent the ground conductor from the conductive pads along the axis. Elongated signal conductor strip ranging from the axis laterally outwardly projecting portion of the convex portion is located outside the restricted area within the distance.

In another embodiment, a printed circuit board comprising: a first layer, the second layer, and at least one via structure ground vias. The first layer comprises a ground conductor, and the second layer comprising signal traces. The via structure electrically connected to the signal traces and the via structures comprising: signal vias, extending through at least a portion of the second layer; conductive pads, the second layer. The conductive pads are electrically connected to the signal vias and an elongated signal conductor strip. The elongated signal conductor strip along a longitudinal axis extending from the conductive pads, and the elongated signal conductor strip comprises outwardly projecting laterally from the axis of the part. Configuring the elongated signal conductor with the outwardly convex portion having the via structure having a predetermined impedance capacitor. Electrically connected to the first grounding grounding conductor vias located near the signal vias and positioned Depart from outside the penalty area from the signal vias.

细长信号导体带17从导电焊盘30延伸，而且包括从细长信号导 体带17横向地凸起的凸出部分20。确定凸出部分20的大小，而且沿 着细长信号导体带17定位凸出部分20，以便能够具有建立过孔结构 18所要求的阻抗的电容。例如，可以对凸出部分20选择电容，以建立 过孔结构18的50欧姆的阻抗。

细长信号导体带17延伸，以形成沿印刷电路板10布线的信号迹 线部分14。信号迹线部分14通常至少具有一个相应的回路或者地线（图 1中未示出）。

可以选择凸出部分20的电容，以便与导电焊盘30和信号过孔24 组合，该过孔结构18具有预定阻抗。例如，过孔结构18的预定阻抗 可以近似为33欧姆、50欧姆、75欧姆、100欧姆等，或所要求的其他 值。信号迹线部分14的阻抗可以近似地与过孔结构18的阻抗相同。

在一些实施例中，使过孔结构18的预定阻抗与信号迹线部分14 的预定阻抗匹配，可以使高频信号（例如，频率高于1 GHz的信号）传播通过过孔结构18，并且可以保持该信号的保真度。因此，信号迹 线部分14可以布线成带状线，与布线成微带的信号迹线部分14相比, 这样可以提高印刷电路板10的布线密度。

印刷电路板10可以包括一个或者多个的通过印刷电路板10的层 12的接地过孔16，该接地过孔16用作印刷电路板10的电接地参考或 者信号返回。如图1中所示，接地过孔16通常位于包围导电焊盘30 的禁区（keep out) 22 (利用假想线所示的）之外，该禁区22可以是基 本上与信号过孔24同中心的圆形区域。接地过孔16位于禁区22之外， 这是因为接地过孔16可能影响信号过孔24的电感或者电容。例如， 在接地过孔16的一个较靠近信号过孔24时，信号过孔24的电容可能 增加。在其他实施例中，可以有一部分接地过孔16在禁区22内部。

选择禁区22的大小，使得感应信号过孔24。例如，对于高频信号，例 如，频率高于IGHz的信号，信号过孔24具有大于容抗的感抗。

One or more of the above-described embodiments having one or more of the following advantages. When reading the instructions, there are other advantages will become apparent. One advantage is that the structure can be transmitted via a high speed signal. Another advantage is that the structure can be maintained via Gao speed signal fidelity. A further advantage is that without a significant increase in manufacturing cost or time, you can achieve this via structures.

BRIEF DESCRIPTION OF THE DRAWINGS The following description easier to understand additional features and advantages of the present invention.

1 is a structure comprising a hole through the printed circuit board is a plan view of the embodiment of FIG.

2 is a block diagram of an embodiment of the through hole feature.

FIG. 3 is a block diagram of an embodiment of the through hole feature.

FIG. 4 is a cross-sectional view of a multilayer printed circuit board.

FIG. 5 is a cross-sectional view through the embodiment of a cell structure of a printed circuit board.

FIG. 6 is a cross-sectional view of a via structure of the printed circuit board to another embodiment. through FIG. 7 is a block diagram of one embodiment includes a test of the pore structure.

DETAILED DESCRIPTION Figure 1 shows a structure 18 includes a hole through one embodiment of a printed circuit board 10 is a plan view of FIG. 18 comprises a via structure having conductive pads 30, signal vias extending through aperture 24 (not shown in FIG. 1) to pass through the conductive pads 30. In some embodiments, the conductive

例如，通过利用金属镀膜/电镀以及蚀刻处理，导电焊盘30、细长 信号导体带17以及信号迹线部分14,或者它们的任意组合可以是形成 在该印刷电路板的层12上的集成导体的各部分。导电焊盘30、细长信 号导体带17以及信号迹线部分14可以由诸如铜的金属组成。例如， 导电焊盘30、细长信号导体带17以及信号迹线部分14可以是印刷电 路板10上的铜箔的一部分。信号过孔24也可以由诸如铜的金属组成。

例如，通过利用金属镀膜/电镀以及蚀刻处理，可以在层12上集 成地形成导电焊盘30和细长信号导体带17。利用钻出贯穿层的孔12， 并且通过利用金属镀膜处理以电镀或者填充该孔，使得信号过孔24电 连接到导电焊盘30，可以形成信号过孔24。

图2示出过孔结构18的一个实施例的方框图。信号过孔24可以 具有半径1^确定的大致圆形。内径q和外径r2可以确定导电焊盘30， 而且导电焊盘30可以具有外径r2确定的外边缘34。禁区22可以具有 由比导电焊盘30的外径1"2大的半径r3确定的大致圆形。例如，禁区22 可以是半径r3确定的圆形，并且具有导电焊盘30的外边缘34和该圆 形之间的距离12。信号过孔24、导电焊盘30以及禁区22基本上是同 心圆，但是不必这样。

在图2所示的实施例中，细长信号导体带17从导电焊盘30延伸， 而且它包括从导电焊盘30的外边缘34延伸到凸出部分20的近端54 的颈部（neck portion) 50。颈部50沿轴线80纵向延伸，而且将信号 过孔24与凸出部分20分离。这样，对于高频信号（例如，频率高于 IGHz的信号），凸出部分20不会显著影响信号过孔24的电容，使得 信号过孔24保持固有电感。在如图2所示的一个实施例中，颈部50 具有沿轴线80的长度I1和垂直于轴线80的宽度W1确定的大致矩形。

长度I1在导电焊盘30的外边缘34和凸出部分20的近端54(假想线中 所示）之间延伸。

在各种实施例中，凸出部分20可以具有从经过颈部50的轴线80 横向地向外凸出和/或者凸起的对称形状。例如，凸出部分20

pads 30 may completely surround the signal vias 24, to form a cyclic structure, shown in Figure 1, or it may only partially surround the signal via hole 24 (not shown). Signal via hole 24 at least partially through the printed circuit board 10, and having an impedance related. elongated signal conductor strip 17 extends from the conductive pads 30, 17 and includes a laterally projecting portion 20 protruding from the elongated signal conductor strip. Determining the size of the projecting portion 20, and along the elongate signal conductor 17 with positioning convex portion 20, so that the structure can have a via to the desired impedance of the capacitor 18. For example, you can choose capacitors bulge portion 20 in order to establish structure 50 via 18 ohm impedance. elongated signal conductor strip 17 extends to the printed circuit board 10 is formed along the signal wiring portion 14 traces. Signal traces 14 typically has at least one portion of the respective circuit or ground (not shown in FIG. 1). can select projecting portion 20 of the capacitor, and the conductive pads 30 to vias 24 and the signal combination, the via structure 18 having a predetermined impedance. For example, via a predetermined impedance structure 18 may be approximately 33 ohms, 50 ohms, 75 ohms, 100 ohms, etc., or other required values. Impedance of the signal trace section 14 may be approximately the same as with the through hole 18 of the impedance of the structure.

In some embodiments, the pore structure so that over a predetermined impedance and a predetermined impedance signal traces 18 of section 14, you can make a high-frequency signal (for example, a signal frequencies above 1 GHz) propagate through via structures 18 and maintain the fidelity of the signal. Thus, the signal trace section 14 can be wired into a strip line, a microstrip wiring

可以具有 拱形凸起，如图2中所示。凸出部分20的拱形凸起可以从一侧到另一 侧延伸距离d,该距离d大于颈部50的宽度Wl。例如，颈部50的宽 度W1可以是0.025英寸，而凸出部分20的距离d可以是0.035英寸。

通过插入在凸出部分20与信号迹线部分14之间的连接部分70，凸出 部分20可以连接到信号迹线部分14 (如图2中所示）。或者，凸出部 分20可以直接连接到信号迹线部分14 (未示出）。在如图2中所示的 一个实施例中，在位于禁区22内的细长信号导体带17的中点，凸出 部分20位于导电焊盘30的外边缘34与禁区22的外边缘r3之间的中 间。

在一些实施例中，凸出部分20具有横向弯曲形状的凸出和/或凸 起。在一些实施例中，可以对着半圆部分的拱形部分横向地从轴线80 向外凸出和/或者凸起，如图2中所示。其他形状的凸起也是可能的。

如图2中所示，在一些实施例中，过孔结构18包括位于禁区22 内、从凸出部分20延伸的连接部分70。在凸出部分20的远端66 (假 想线中所示）与禁区22之间，连接部分70可以具有大致矩形。连接 部分70的宽度可以小于凸出部分20的距离d，而且可以与信号迹线部 分14的宽度W2相同。例如，连接部分70的宽度可以是0.025英寸。

尽管所示的凸出部分20具有大致拱形凸起，但是凸出部分20可 以具有任意几何形状，以便凸出部分20具有建立过孔结构18的预定 阻抗的电容。例如，凸出部分20可以是多边形的，例如菱形的。凸出 部分20的几何形状不需要是对称的，而且可以是非规则形状。此外， 可以利用沿近端54与远端66之间的轴线80延伸的长度和垂直于轴线 80的宽度确定凸出部分20的形状。

图3示出过孔结构318的实施例的方框图。在图3的实施例中， 凸出部分320沿从颈部350延伸的曲线向外凸起距离w3，而在凸出部 分320的远端366收缩到宽度w2。在其他实施例中（未示出），凸出 部分320可以沿直线向外凸起，该直线离开轴线80垂直收缩或者延伸。

compared with a signal trace portion 14, which can improve the wiring density of the printed circuit board 10. the printed circuit board 10 may include a layer or a printed circuit board 10 by a plurality of grounding vias 12 16, which is electrically grounded through the ground signal or the reference hole 16 is used as the printed circuit board 10 is returned. As shown in Figure 1, the ground vias 16 is typically located in the area surrounding the conductive pads (keep out) 22 (shown in phantom lines in use) 30 outside the restricted area 22 may be substantially the same center of the signal via hole 24 circular area. Ground vias 16 are located outside of the box 22, because the ground via 16 may affect the signal vias 24 an inductor or capacitor. For example, in the grounding hole 16 through a through hole 24 closer to the signal, the capacitance of the signal vias 24 may be increased. In other embodiments, there may be some ground vias 16 22 inside the penalty area.

Select the size of the box 22 so that the sensor signal vias 24. For example, for a high-frequency signal, e.g., Gao at IGHz frequency signals each having a through-hole 24 is greater than the capacitance of the inductance.

, for example, by using a metal plating / electroplating and etching treatment, conductive pads 30, 17 with an elongated signal conductors and a signal trace section 14, or any combination thereof may be formed on the printed circuit board 12 on layer the integration of various parts of the conductor. Conductive pads 30, 17 with an elongated signal conductor and a signal trace section 14 may be made of metal, such as copper components. For example, the conductive pads 30, 17 with an elongated signal conductors and a signal trace section 14 may be part of a

如在图2的实施例中，可以改变颈部350的宽度，但是它小于凸出部 分320的距离w3。而且，如在图3中可以看出，可以改变颈部350的 长度，在图2中利用l1表示该长度，而且可以将它缩小到0或者接近0，如图3中所示。如图3中所示，在从凸出部分320的外部观看时，凸 出部分320基本上是凸形的或者具有凸形外表面。

所示的禁区22内的连接部分370将位于远端366的凸出部分320 连接到信号迹线部分314。在其他实施例中，凸出部分320可以延伸到 禁区22的边缘，或者禁区22之外。

在未示出的一些实施例中，导电焊盘和凸出部分通常都具有在导 电焊盘与凸出部分之间形成颈部的隙缝或者其他开槽的泪珠形状。

图4示出多层印刷电路板410的一部分的横截面图。通过利用半 固化片86将各印刷电路板12粘连在一起形成多层印刷电路板410，各 印刷电路板12分别具有芯84和位于芯84的两侧上的相对的导体层82。

在一些实施例中（未示出），如在本技术领域内公知，在邻近的芯84 上的导体层82之间，可以将几层半固化片夹入诸如导电箔的导体层。

其他布置也是可能的。

尽管在图4中仅示出8个导体层82，但是印刷电路板410可以具 有更多或者更少的导体层82。为了说明目的，利用实心层示出导体层 82。导体层82可以包括导体面、迹线、过孔结构等。

图5示出包括根据本发明的可能性实施例的过孔结构518的单芯 584a印刷电路板510的横截面图。印刷电路板510可以是多层板的部 分（图5中未示出）。过孔结构518的信号过孔524通过芯584a，以 通过导电焊盘530、颈部550、凸出部分520以及连接部分570，连接 到信号迹线部分514。

印刷电路板510包括接地导体515，它可以是接地迹线或者接地 面。如图5中所示，

copper foil of the printed circuit board 10 on. Signal vias 24 may be formed of metals such as copper.

, for example, by using a metal plating / etching process and plating, may be formed of conductive pads 30 and 17 with an elongated signal conductors in the layer 12 to be part one. The use of drilled holes 12 through the layer, and by using a metal plating or coating treatment with filling in the pores, so that the signal vias 24 electrically connected to the conductive pads 30, vias 24 may be formed signal.

Figure 2 shows a through-hole 18 is a block diagram showing the structure of an example of embodiment. Signal vias 24 may have a radius substantially circular determined. And the outer diameter of the inner diameter r2 q conductive pads 30 may be determined, and the conductive pads 30 may have an outer edge 34 of an outer diameter r2 is determined. 22 may have a generally circular restricted by the 1 '2 larger radius than the outer diameter of the conductive pads 30 of r3 determined. For example, the area 22 may be determined r3 radius of the circle, and having an outer edge of the conductive pads 34 and 30 of the 12. the distance between the signal through the circular hole 24, the conductive pads 30 and 22 is substantially concentric restricted area, but not necessarily so.

In the embodiment shown in FIG. 2, the elongate strip signal conductor 17 extends from the conductive pads 30, and it comprises the conductive pads extending from the outer edge 34 of the proximal end 30 of the projecting portion 54 of the neck 20 of the portion (neck portion) 50. Neck portion 50 extending along the longitudinal axis 80, and the signal via hole 24 and the projecting portion 20 is disengaged. Thus, the high-frequency signal (e.g., Gao frequency

接地导体515位于禁区522的外部，但是其近端 延伸到禁区522。因此，禁区522表示通常没有接地导体515的区域。

如图5中所示，接地导体515与信号迹线部分514相邻。然而， 连接在信号过孔524与信号迹线部分514之间的信号导体带的分段延 伸通过禁区522，以使信号过孔524与信号迹线部分514相连，而没有 相应邻近的接地导体515。

在一个实施例中，接地导体515是基本上平行于信号迹线部分514 的迹线，而且其图案与信号迹线部分514的图案相同。在另一个实施 例中，接地导体515是接地面。在该实施例中，在印刷电路板510上， 信号迹线部分514与接地导体515组合形成微带信号迹线部分514。

可以确定凸出部分520的大小，而且沿细长信号导体带517定位 凸出部分520，以便能够在凸出部分520与接地导体515之间，g P，通 过边缘电容，实现电容耦合。凸出部分520的电容基于凸出部分520的大小和形状、凸出部分520的材料以及芯584a层（或者未示出的其 他层之间的）的材料。此外，凸出部分520的电容还基于凸出部分520 与信号过孔524之间的距离、禁区距离r3以及相邻接地导体的数量。

在一个实施例中，凸出部分520的电容主要归因于凸出部分520与接 地导体515之间的电容。图5中所示的细长信号导体带517的凸出部 分520基本上位于定位在禁区522处的接地导体515的近端与导电焊盘530的外边缘534之间的中间。

在一个实施例中，信号过孔524包括印刷电路板510的上表面525 上的任选接触焊盘526。接触焊盘526可以提供印刷电路板510与该印 刷电路板510外部的电路之间的接口。这样，可以通过接触焊盘526 在信号过孔524与该电路之间发送信号。例如，印刷电路板510可以 是器件接口板（DIB)、探测器接口板（PIB)或者处理器接口板（HIB) 的一部分。该电路可以包括用于测试半导体器件的装置的弹簧针（pogo pin)或者转接板(interposer)。接触焊盘526可以是用于将信号过孔524 电连

signal to IGHz), the projecting portion 20 does not significantly affect the capacitance of the signal through hole 24, so that the signal vias 24 maintain the inherent inductance. In an embodiment shown in FIG. 2, the neck 50 has a generally rectangular axial length I1 and a vertical axis 80 in the width W1 of 80 determined. length I1 (shown in phantom lines) at the outer edge of the conductive pads 34 and convex portion 20 extending between the proximal end 54 30.

In various embodiments, the projecting portion 20 may have a symmetrical shape from the through axis 50 of the neck portion 80 projecting laterally outwardly and / or projections. For example, the projecting portion 20 may have a convex arcuate, as shown in Fig. Arcuate projections projecting portion 20 may extend a distance d from side to side, the distance d is greater than the width Wl 50 of the neck portion. For example, the neck width W1 50 may be 0.025 inches, and the projecting portion 20 of the distance d can be 0.035 inches. by inserting the projecting portion 20 and 14 is connected between the signal traces portion 70, the projecting portion 20 may be connected to the signal trace portion 14 (shown in Figure 2). Alternatively, the protruding portion 20 can be connected directly to the signal trace section 14 (not shown). In the area located within the elongate signal conductor 22 with the midpoint 17 of the projecting portion 20 at the outer edge of the conductive pads 30 and 34 of the area of the outer edge of the r3 22 is shown in Figure 2. In one embodiment, intermediate between.

In some embodiments, the protruding portion 20 has a convex curved shape of the lateral and / or projections. In some embodiments, may 80 laterally outwardly projecting portion facing the semicircle from the axis and / or projections, as

接到SMT连接器的表面贴装（ SMT)焊盘。

图6示出根据本发明另一个实施例的印刷电路板610的部分的横 截面图。信号过孔结构618具有通过芯684a的信号过孔624，以通过 导电焊盘630、颈部650、凸出部分620以及连接部分670，连接到信号迹线部分614。

在图6所示的实施例中，对细长信号导体带617的信号迹线部分 614设置两个接地导体615和619。接地导体615和619位于禁区622 之外，但是其近端延伸到禁区622。如图6中所示，在两侧具有相对的接地导体615和619的信号迹线部分614有时被称为带线信号导体。

确定凸出部分620的大小，而且沿细长信号导体带617定位凸出 部分620，以便与接地导体615和619具有边缘电容。在各种实施例中' 接地导体615和619可以是如上所述的接地面和/或者接地迹线。在包 括任选接触焊盘626的实施例中，凸出部分620可以与如上所述的接 触焊盘626具有边缘电容。

印刷电路板610可以是多层层叠的印刷电路板的部分（图6中未 示出）。所示的接地过孔616延伸通过芯684a和半固化片686，以电 连接到接地导体615和619。所示的接地过孔616延伸通过芯684a，而 且如果需要，可以延伸到接触其他接地导体（未示出）。其他实施例 也是可能的。

利用三维电路仿真程序，可以对上述的过孔结构和印刷电路板建 模，并模拟它们。这种三维电路仿真程序的实例有Pitsburg, PA的Ansoft Corp., www.ansoft.com市售的高频结构仿真器(HFSS)。

这样，可以确定凸出部分的电容，以根据选择的配置和材料，建 立信号过孔结构的预定阻抗。因此，可以配置凸出部分，以具有对信 号过孔结构提供选择的阻抗的电容。此外，可以将印刷电路板制造为 具有多个信号过孔结构的，每个信号过孔结构分别具有对其相关信号 过孔的特性定制以对每个信号过孔结构形成适当阻抗的凸出部分。

shown in Fig. Other shapes are also possible projections. shown in Figure 2, in some embodiments, includes a through hole 18 located within the box structure 22, the connecting portion 70 projecting from portion 20 extends. The projecting portion 20 of the distal end 66 (shown in phantom line) between the box 22, the connecting portion 70 may have a generally rectangular. The connecting portion 70 may be smaller than the width of the projecting portion 20 of the distance d, and the signal traces can be divided into the same portion of the width W2 14. For example, the width of the connecting portion 70 can be 0.025 inches.

Although shown projecting portion 20 having a substantially arcuate convex, but the protruding portion 20 may have any geometry, to a projecting portion 20 having a via to the structure of the predetermined impedance of the capacitor 18. For example, the projecting portion 20 may be polygonal, e.g. diamond. The geometry of the convex portion 20 need not be symmetrical, but may be non-regular shape. Furthermore, you can use the length and along a vertical axis 66 between the proximal end 54 and distal end 80 of the axis 80 extending in the width of the portion 20 of the convex shape is determined.

Figure 3 shows a block diagram 318 over the pore structure of the embodiment of FIG. In the embodiment of Figure 3, the projecting portion 320 projecting outward distance along the curve w3 extending from the neck 350, and the projections 320 of the distal portion 366 to shrink the width w2. (Not shown), projecting outwardly projecting portion 320 can be a straight line in other embodiments, the linear shrinkage perpendicular to the axis 80 away from or extend.

图7是包括过孔结构（未示出）的测试器700的一个实施例的方 框图。测试器700包括测试器主机702，连接该测试器主机702，以便 与测试头708和与该测试头708相关的接口板706通信，该接口板706 可以连接到测试头708。在图7中所示的实施例中，接口板706是器件 器件接口板。在工作中，接口板706电连接到被测器件（DUT) 704， 用于测试DUT 704。例如，测试器700可以是用于测试集成电路的自 动测试装备（ATE)系统，而DUT 704可以是包括集成电路的半导体 器件。接口板706可以是印刷电路板10 (图1，4，5或者6)或可以 包括印刷电路板10 (图1，4，5或者6)。

测试器主机702包括用于产生测试信号并评估测试信号的电路。

通过测试头708和接口板706，测试器主机702将测试信号发送到DUT 704并从DUT 704接收测试信号。DUT 704可以是包括要被测试的集 成电路的封装芯片。在另一个实施例中，接口板706是探测器接口板， 而DUT 704可以是包括要被测试的集成电路的半导体晶片。

在各种实施例中，接口板706和/或者测试头708可以包括含有如 上所述的信号过孔结构的多层印刷电路板。

在此描述的实施例用于说明本发明。当参考图解描述本发明的这 些实施例时，所描述的方法和/或特定结构的各种修改或者调整对于本 领域内的技术人员变得显而易见。可以认为基于本发明的教导，而且 通过它们这些教导已经改进了该领域的所有这些修改、调整或者改变 均在本发明的精神和范围内。因此，不应该认为这些描述和附图具有 限制性意义，因为应该明白本发明并不仅仅局限于所说明的实施例。

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As in the embodiment of FIG. 2, the width of the neck portion 350 may be varied, but it is projected portion 320 is smaller than the distance w3. Moreover, as can be seen in Figure 3, can change the length of the neck 350, it indicates that the use of the length I1 in Figure 2, but it can be reduced to zero or close to zero, as shown in Fig. As shown in Figure 3, when viewed from the outside projecting portion 320, projecting portion 320 having a substantially convex or convex outer surface.

Connecting portion 370 within the restricted area 22 shown in

will be located in the distal end portion 366 projecting 320 is connected to the signal trace section 314. In other embodiments, the projecting portion 320 can extend to the edge of the box 22, 22 or the prohibited area.

In some embodiments, not shown, the conductive pad and the protruding portions are usually teardrop shape having a slit or slotted in between other conductive pads and forming a projecting portion of the neck.

Figure 4 shows a cross-section of a portion of a multilayer printed circuit board 410 of FIG. By using a prepreg 86 of each of the printed circuit board 12 to stick together to form a multilayer printed circuit board 410, the printed circuit board 12, respectively, each having opposing conductive layers 82 and 84 located on both sides of the core 84 on the core.

(not shown), as known in the art In some embodiments, the core 84 adjacent the conductive layer 82 may be layers such as a semi-conductor layer cured film holder into the conductive foil.

Other arrangements are possible.

Although shown only eight conductor layer 82 in FIG. 4, but the printed circuit board 410 may have more or fewer conductive layer 82. For illustrative purposes, the use of a solid layer conductor layer 82 is shown. Conductive layer 82 may comprise a conductor surface, traces, vias and other structures.

Figure 5 shows a cross-section including the possibility according to an embodiment of the present invention via structures 584a 518 single printed circuit board 510 of FIG. A printed circuit board 510 may be multilayer portion (not shown in FIG. 5). Signal structure 518 via vias 524 through the core 584a, through the conductive pads 530, the neck 550, the projecting portion 520 and a connecting portion 570 connected to the signal trace portion 514. a printed circuit board 510 includes a ground conductor 515, which may be a ground trace or ground plane. Shown in Figure 5, the ground conductor 515 is located outside the area 522, but it extends to the proximal end of the box 522. Therefore, the area 522 represents the area usually no ground conductor 515.

As shown, the ground conductor 515 and the signal trace portion 514 adjacent 5. However, the segment connected between the signal vias 524 and the signal trace section 514 with the signal conductor 522 extends through the area, so that the signal vias 524 and section 514 is connected to the signal traces, but no corresponding adjacent ground conductor 515.

In one embodiment, the ground conductor 515 is substantially parallel to the signal trace trace section 514, and its pattern portion 514 the same signal trace pattern. In another embodiment, the ground conductor 515 is a ground plane. In this embodiment, on the printed circuit board 510, the signal trace section 514

and the ground conductor 515 forming the microstrip combination signal trace portion 514. may determine the size of the projecting portion 520, and signal conductor strip 517 along elongate positioning convex portion 520 to allow the projecting portion 520 between the ground conductor 515, g Jie, through the edge of the capacitor, to achieve the capacitive coupling. Based on the capacitance of the projecting portion 520 projecting portion 520 of the size and shape (or an unillustrated Other layers) material projecting portion 520 and a core material layer 584a. In addition, the protruding portion 520 of the capacitor is also based on projections from the section 520 and the signal vias 524 between the area and the number of distance r3 adjacent ground conductor.

In one embodiment, the projecting portion 520 projecting mainly due to the capacitance 520 and the capacitance portion 515 between the ground conductor. Figure 5 elongate projections shown in the signal conductor 520 with 517 points located substantially positioned in the middle of the ground conductor of the outer edge of the area 522 534 515 530 proximal conductive pads between.

In one embodiment, the optional touch signal vias 524 on the surface 525 includes a printed circuit board 510 on the pad 526. Contact pad 526 may provide a printed circuit board 510 and the printed circuit board 510 to the outside of the interface circuit. Thus, the contact pad 526 can transmit signals between the signal via hole 524 with the circuit. For example, a printed circuit board 510 may be part of the device interface board (DIB), the detector interface board (PIB) or Processor Interface Board (HIB) of. The circuit may include a spring pin device testing semiconductor device (pogo pin) or

adapter plate (interposer). Contact pads 526 may be used to signal vias 524 electrically connected to the surface mount SMT connector (SMT) pads.

Figure 6 shows a cross-sectional view of a portion of the printed circuit board 610 according to another embodiment of the present invention. Signal via structure 618 has a core 684a through the signal vias 624, through the conductive pads 630, 650 and neck protruding portion 620 and a connecting portion 670 connected to the signal trace section 614.

In the embodiment shown in FIG. 6, the pair of elongated signal conductor trace section 614 with signal 617 set two ground conductors 615 and 619. Grounding conductor 622 615 and 619 located outside the restricted area, but it extends to the proximal end of the box 622. As shown in Figure 6, the ground conductor having opposite sides 615 and 619 of signal traces portion 614 is sometimes referred to as stripline signal conductors. determine the size of the protruding portion 620, and along the elongated signal conductor strip 617 positioning convex portion 620, so that the ground conductor 615 and 619 has an edge capacitance. In various embodiments, the '615 and the ground conductor 619 may be a ground plane as described above and / or the ground traces. In includes an optional embodiment of the contact pads 626, the protruding portion 620 as described above with the contact pad 626 has an edge capacitance. the printed circuit board 610 may be part of a multilayer laminated printed circuit board (not shown in FIG. 6). Ground vias 616 shown extending 686, to be electrically connected to the ground conductor 615 and 619 through the core 684a and a prepreg. Ground vias 616 shown extending through the core 684a, and if desired, may be extended to contact with

other ground conductor (not shown). Other embodiments are possible. using three-dimensional circuit simulation program, it can be said through-hole printed circuit board structure and modeling, and simulation them. Examples of such three-dimensional circuit simulation program has Pitsburg, PA of Ansoft Corp., www.ansoft.com commercially available HF Structure Simulator (HFSS).

In this way, the protruding portion of the capacitor can be determined, in accordance with the selected configuration and materials, establish impedance signal over a predetermined pore structure. Therefore, you can configure the protruding portion to have an impedance signal via structure provides the selected capacitor. Further, the printed circuit board can be manufactured with the structure of a plurality of signal vias, each signal via structures each having a projecting portion to be customized for each of the signal via structures formed on its characteristic impedance appropriate correlation signal vias.

FIG. 7 is a structure comprising vias (not shown) of the tester 700 is a block diagram of an example of embodiment. The tester 700 includes a test host 702, is connected to the test host 702 to communicate with the test head 708 and test head 708 associated with the interface board 706, the interface board 706 may be connected to the test head 708. In the embodiment shown in FIG. 7, the device interface board 706 is a device interface board. In operation, the interface board 706 is electrically connected to the device under test (DUT) 704, used to test the DUT 704. For example, the tester 700 may be used to test an integrated circuit automatic test equipment (ATE) systems, and DUT 704 may include a semiconductor integrated

circuit device. Interface board 706 may be a printed circuit board 10 (FIG. 1, 4, 5 or 6) or may include a printed circuit board 10 (FIG. 4, 5, or 6). test host 702 includes means for generating a test signal and the test signal evaluation circuit.

706, the test host 702 sends test signals to the DUT 704 and received from the DUT 704 via the test head 708 and interface board test signal. DUT 704 may include a chip to be tested packaged IC's. In another embodiment, the interface board 706 is a detector interface board, and DUT 704 may include an integrated circuit to be tested is a semiconductor wafer.

In various embodiments, the interface board 706 and / or test head 708 may include a structure containing as signal vias on multilayer printed circuit board said.

In the embodiments described to illustrate the invention. When the reference graphic description of these embodiments of the present invention, the method described and / or specific structures of various modifications or adjustments within the skill in the art will become apparent. Based on the teachings of the present invention it can be considered, but these teachings through them all these modifications have improved in this area, adjusted or changed within the spirit and scope of the invention. Therefore, you should not think that these description and drawings in a limiting sense, because it should be understood that the invention is not limited to the embodiments described. and Pflf H

Cited by: CN102577639 A ; CN104219871 A ; CN104797075 A ; CN104797075 B ; CN108336593 A ; WO15106528 A1 ;

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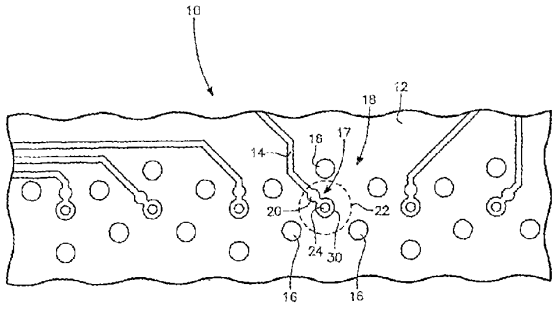
权利要求书 6 页 说明书 10 页 附图 4 页

[54] 发明名称

阻抗受控过孔结构

[57] 摘要

在一个实施例中，提供了一种用于印刷电路板的过孔结构，该过孔结构包括：信号过孔和与该信号过孔电连接的细长信号导体带。该细长信号导体带与接地导体相邻，而且从导电焊盘基本上延伸到接地导体。该细长信号导体带包括横向地向外延伸的部分，可以配置该部分，以具有建立过孔结构的阻抗的电容。



1.一种用于印刷电路板的过孔结构，包括：

信号过孔；以及

细长信号导体带，与所述信号过孔相连，所述细长信号导体带包括从所述信号过孔延伸而没有相邻接地导体的分段，其中该分段沿轴线延伸，而且包括从所述轴线横向地向外凸出的部分。

2.根据权利要求1所述的过孔结构，进一步包括在所述信号过孔附近并且与所述信号过孔间隔开的接地过孔。

3.根据权利要求1所述的过孔结构，其中，所述凸出部分进一步包括位于所述轴线的相对侧上的拱形部分。

4.根据权利要求1所述的过孔结构，其中，所述凸出部分至少包括如下之一：(a)弯曲形；(b)部分多边形；或者(c)锥形。

5.根据权利要求1所述的过孔结构，其中，所述凸出部分位于所述分段的中点处。

6.根据权利要求1所述的过孔结构，其中，所述凸出部分包括外围边缘，所述外围边缘从所述轴线横向地向外延伸，在离开所述信号过孔的方向上靠近所述信号过孔而且向远离所述信号过孔的轴线收缩。

7.根据权利要求1所述的过孔结构，其中，所述凸出部分具有大致凸形的外表面。

8.根据权利要求1所述的过孔结构，其中，确定所述凸出部分的大小，而且沿所述细长信号导体带定位所述凸出部分，以便能够具有

建立所述过孔结构的预定阻抗的电容。

9. 根据权利要求1所述的过孔结构，进一步包括：位于所述分段之外的至少一个接地导体，其中确定所述凸出部分的大小，而且沿所述细长信号导体带定位所述凸出部分，以便能够与所述至少一个接地导体电容耦合。

10. 根据权利要求1所述的过孔结构，其中，所述分段包括位于所述信号过孔与所述凸出部分之间的颈部。

11. 根据权利要求1所述的过孔结构，其中，所述分段包括连接部分，所述连接部分在所述凸出部分与所述信号过孔相反的的一侧处与所述凸出部分邻接。

12. 一种用于印刷电路板的过孔结构，包括：

信号过孔；

导电焊盘，电连接到所述信号过孔；

至少一个接地导体，定位在离开所述导电焊盘禁区距离处；以及

细长信号导体带，沿轴线从所述导电焊盘纵向地延伸到与所述至少一个接地导体相邻，而且包括从所述轴线横向地向外凸起的部分，所述向外凸起部分位于所述禁区距离内。

13. 根据权利要求12所述的过孔结构，其中，所述向外凸起部分至少包括如下之一：(a)弯曲形状；(b)部分多边形；或者(c)锥形。

14. 根据权利要求12所述的过孔结构，其中，所述向外凸起部分包括位于所述轴线的相对侧上的拱形部分。

15. 根据权利要求12所述的过孔结构，其中，所述向外凸起部分

基本上位于所述导电焊盘的外边缘和所述至少一个接地导体的近端边缘所确定的间隔的中点处。

16. 根据权利要求12所述的过孔结构，其中，确定所述向外凸起部分的大小，而且沿所述细长信号导体带定位所述向外凸起部分，以便能够具有建立所述过孔结构的预定阻抗的电容。

17. 根据权利要求16所述的过孔结构，其中，所述过孔结构的预定阻抗是如下之一：(a)约33欧姆；(b)约50欧姆；(c)约75欧姆；或者(d)约100欧姆。

18. 根据权利要求12所述的过孔结构，其中，确定所述向外凸起部分的大小，而且沿所述细长信号导体带定位所述向外凸起部分，以便能够与所述至少一个接地导体电容耦合。

19. 根据权利要求12所述的过孔结构，进一步包括：位于所述信号过孔附近的接地过孔，而且其中至少一个接地过孔连接到所述至少一个接地导体，而且定位在如下之一：(a)部分地位于所述禁区距离内；或者(b)位于所述禁区距离之外。

20. 根据权利要求12所述的过孔结构，其中，所述细长信号导体带包括位于所述信号过孔与所述向外凸起部分之间的颈部。

21. 根据权利要求12所述的过孔结构，其中，所述细长信号导体带包括连接部分，所述连接部分在所述向外凸起部分的与所述信号过孔相反的一侧处与所述向外凸起部分邻接。

22. 根据权利要求12所述的过孔结构，其中，所述导电焊盘和所述向外凸起部分具有一般泪珠形状，该泪珠形状包括位于所述导电焊盘与所述向外凸起部分之间的颈部。

23.一种印刷电路板，包括：

第一层，包括第一接地导体；

第二层，包括信号迹线；以及

过孔结构，电连接到所述信号迹线，所述过孔结构包括：

信号过孔，至少部分地延伸通过所述第二层；

导电焊盘，在所述第二层中，所述导电焊盘电连接到所述信号过孔；以及

细长信号导体带，在所述第二层中，所述细长信号导体带沿轴线从导电焊盘纵向地延伸，而且包括从所述轴线横向地向外凸起的部分，配置所述向外凸起部分，以具有建立所述过孔结构的预定阻抗的电容；以及

至少一个接地过孔，位于所述信号过孔附近，而且定位在离开所述信号过孔的禁区距离处，所述至少一个接地过孔电连接到所述第一接地导体。

24.根据权利要求23所述的印刷电路板，其中，所述向外凸起部分包括：

第一部分，从所述轴线横向地向外凸起；以及

第二部分，对着所述第一部分，而且从所述轴线横向地向外凸起。

25.根据权利要求23所述的印刷电路板，其中，所述向外凸起部分至少具有如下之一：(a)弯曲形；(b)部分多边形；或者(c)锥形。

26.根据权利要求23所述的印刷电路板，其中，所述向外凸起部分位于所述导电焊盘的外边缘和所述第一接地导体的近端边缘所确定的间隔的近似中间处理。

27.根据权利要求23所述的印刷电路板，其中，所述信号迹线包

括预定阻抗，而且其中所述过孔结构的预定阻抗近似地等于所述信号迹线的预定阻抗。

28. 根据权利要求23所述的印刷电路板，其中，所述过孔结构的预定阻抗是如下之一：(a)在约48欧姆到约52欧姆的范围内；(b)约75欧姆；或者(c)约100欧姆。

29. 根据权利要求23所述的印刷电路板，其中，所述信号过孔包括约0.0125英寸的半径，所述导电焊盘包括约0.0175英寸的外径，而所述向外凸起部分包括半圆形部分，每一个所述半圆形部分包括约为0.0125英寸的半径。

30. 根据权利要求23所述的印刷电路板，其中，所述第一接地导体是接地面。

31. 根据权利要求23所述的印刷电路板，进一步包括：包括第二接地导体的第三层，所述第二接地导体电连接到所述第一接地导体，其中进一步确定所述向外凸起部分的大小，而且沿所述细长信号导体带定位所述向外凸起部分，以便能够与所述第二接地导体电容耦合。

32. 根据权利要求23所述的印刷电路板，其中，所述细长信号导体带进一步包括位于所述信号过孔与所述向外凸起部分之间的颈部。

33. 根据权利要求23所述的印刷电路板，其中，所述细长信号导体带包括位于所述向外凸起部分与所述信号迹线之间的连接部分。

34. 一种用于测试被测器件的装置，包括：

测试器主机；

测试头，连接到所述测试器主机；以及

印刷电路板，被配置以与所述测试头配合，所述印刷电路板包括：

第一层，包括第一接地导体；

第二层，包括信号迹线；以及

过孔结构，至少部分地延伸通过所述印刷电路板，而且电连接到所述信号迹线，所述过孔结构包括：

信号过孔，至少部分地延伸通过所述印刷电路板；

导电焊盘，在所述第二层中，所述导电焊盘电连接到所述信号过孔；以及

细长信号导体带，在所述第二层中，所述细长信号导体带沿轴线从所述导电焊盘纵向地延伸，而且包括从所述轴线横向地向外凸起的部分，配置该向外凸起部分，以具有建立所述过孔结构的预定阻抗的电容。

35.根据权利要求34所述的装置，其中，所述印刷电路板是如下之一：(a)器件接口板，(b)探测器接口板，或者(c)处理器接口板。

36.根据权利要求34所述的装置，其中，所述细长信号导体带包括位于信号过孔与所述向外凸起部分之间的颈部。

阻抗受控过孔结构

相关申请的交叉参考

本申请要求Arash Behziz于2005年5月16日提交的标题为“IMPEDANCE CONTROLLED VIA STRUCTURE”的第60/681,325号美国临时申请的优先权，在此引用该申请的全部内容以供参考。

背景技术

过孔是通常通过多层印刷电路板而且在印刷电路板的层之间提供电连接的电互连。通常，过孔使印刷电路板的一层中的迹线与印刷电路板的另一层中的迹线连接。依次地，迹线又连接到电路、电设备、接触焊盘、连接器等。此外，过孔本身可以包括表面接触焊盘。这样，电路、电设备、接触焊盘、连接器等通过过孔彼此电连接。

因此，过孔与印刷电路板上的迹线组合提供通过印刷电路板的信号路径。对于高频信号，该过孔可以呈现出沿信号路径缓慢传播高频信号的传输线特性，而且可能影响该高频信号的保真度和完整性。鉴于上述问题，需要改进通过印刷电路板中的过孔传播高频信号的速率。此外，需要保持通过过孔传播的高频信号的保真度和完整性。

发明内容

在一个实施例中，一种用于印刷电路板的过孔结构包括与细长信号导体带相连的信号过孔。该细长信号导体带具有延伸离开信号过孔而没有相邻接地导体的分段，该延伸离开的分段沿轴线延伸，而且它包括从该轴线横向地向外凸出的部分。

在另一个实施例中，用于印刷电路板的过孔结构包括电连接到导电焊盘的信号过孔。接地导体定位在离开导电焊盘禁区距离处。细长

信号导体带纵向地沿轴线从导电焊盘延伸到与接地导体相邻。细长信号导体带包括从该轴线横向地向外凸起的部分，该向外凸起部分位于禁区距离之内。

在另一个实施例中，一种印刷电路板包括：第一层、第二层、过孔结构以及至少一个接地过孔。第一层包括接地导体，而第二层包括信号迹线。该过孔结构电连接到信号迹线，而且该过孔结构包括：信号过孔，至少一部分延伸通过第二层；导电焊盘，在第二层中。该导电焊盘电连接到信号过孔和细长信号导体带。该细长信号导体带沿轴线从导电焊盘纵向延伸，而且该细长信号导体带包括从该轴线横向地向外凸起的部分。配置细长信号导体带的该向外凸起部分，以具有使过孔结构具有预定阻抗的电容。电连接到第一接地导体的接地过孔位于信号过孔附近，而且定位在离开该信号过孔的禁区距离之外。

上述一个或者多个实施例具有以下的一个或者多个优点。在阅读该说明时，存在变得显而易见的其他优点。一个优点是该过孔结构可以传送高速信号。另一个优点是该过孔结构可以保持高速信号的保真度。又一个优点是无需显著增加成本或者制造时间，就可以实现该过孔结构。

附图说明

通过结合附图参考下列描述，更加容易理解本发明的更多特征和优点。

图1是包括过孔结构的印刷电路板的一个实施例的俯视图。

图2是该过孔结构的一个实施例的方框图。

图3是该过孔结构的一个实施例的方框图。

图4是多层印刷电路板的横截面图。

图5是包括该过孔结构的印刷电路板的一个实施例的横截面图。

图6是包括该过孔结构的印刷电路板的另一个实施例的横截面图。

图7是包括过孔结构的测试器的一个实施例的方框图。

具体实施方式

图1示出包括过孔结构18的一个实施例的印刷电路板10的俯视图。过孔结构18包括具有导电焊盘30，信号过孔24延伸通过孔(图1中未示出)而穿过导电焊盘30。在一些实施例中，导电焊盘30可以完全包围信号过孔24，以形成环状结构，如图1所示，或它可以仅部分地包围信号过孔24(未示出)。信号过孔24至少部分地通过印刷电路板10，并且具有相关阻抗。

细长信号导体带17从导电焊盘30延伸，而且包括从细长信号导体带17横向地凸起的凸出部分20。确定凸出部分20的大小，而且沿着细长信号导体带17定位凸出部分20，以便能够具有建立过孔结构18所要求的阻抗的电容。例如，可以对凸出部分20选择电容，以建立过孔结构18的50欧姆的阻抗。

细长信号导体带17延伸，以形成沿印刷电路板10布线的信号迹线部分14。信号迹线部分14通常至少具有一个相应的回路或者地线(图1中未示出)。

可以选择凸出部分20的电容，以便与导电焊盘30和信号过孔24组合，该过孔结构18具有预定阻抗。例如，过孔结构18的预定阻抗可以近似为33欧姆、50欧姆、75欧姆、100欧姆等，或所要求的其他值。信号迹线部分14的阻抗可以近似地与过孔结构18的阻抗相同。

在一些实施例中，使过孔结构18的预定阻抗与信号迹线部分14的预定阻抗匹配，可以使高频信号(例如，频率高于1GHz的信号)传播通过过孔结构18，并且可以保持该信号的保真度。因此，信号迹线部分14可以布线成带状线，与布线成微带的信号迹线部分14相比，这样可以提高印刷电路板10的布线密度。

印刷电路板10可以包括一个或者多个的通过印刷电路板10的层12的接地过孔16，该接地过孔16用作印刷电路板10的电接地参考或者信号返回。如图1中所示，接地过孔16通常位于包围导电焊盘30的禁区(keep out)22(利用假想线所示的)之外，该禁区22可以是基本上与信号过孔24同中心的圆形区域。接地过孔16位于禁区22之外，这是因为接地过孔16可能影响信号过孔24的电感或者电容。例如，在接地过孔16的一个较靠近信号过孔24时，信号过孔24的电容可能增加。在其他实施例中，可以有一部分接地过孔16在禁区22内部。选择禁区22的大小，使得感应信号过孔24。例如，对于高频信号，例如，频率高于1GHz的信号，信号过孔24具有大于容抗的感抗。

例如，通过利用金属镀膜/电镀以及蚀刻处理，导电焊盘30、细长信号导体带17以及信号迹线部分14，或者它们的任意组合可以是形成在该印刷电路板的层12上的集成导体的各部分。导电焊盘30、细长信号导体带17以及信号迹线部分14可以由诸如铜的金属组成。例如，导电焊盘30、细长信号导体带17以及信号迹线部分14可以是印刷电路板10上的铜箔的一部分。信号过孔24也可以由诸如铜的金属组成。

例如，通过利用金属镀膜/电镀以及蚀刻处理，可以在层12上集成地形成导电焊盘30和细长信号导体带17。利用钻出贯穿层的孔12，并且通过利用金属镀膜处理以电镀或者填充该孔，使得信号过孔24电连接到导电焊盘30，可以形成信号过孔24。

图2示出过孔结构18的一个实施例的方框图。信号过孔24可以具有半径r_1确定的大致圆形。内径r_1和外径r_2可以确定导电焊盘30，而且导电焊盘30可以具有外径r_2确定的外边缘34。禁区22可以具有由比导电焊盘30的外径r_2大的半径r_3确定的大致圆形。例如，禁区22可以是半径r_3确定的圆形，并且具有导电焊盘30的外边缘34和该圆形之间的距离l_2。信号过孔24、导电焊盘30以及禁区22基本上是同

心圆，但是不必这样。

在图2所示的实施例中，细长信号导体带17从导电焊盘30延伸，而且它包括从导电焊盘30的外边缘34延伸到凸出部分20的近端54的颈部(neck portion)50。颈部50沿轴线80纵向延伸，而且将信号过孔24与凸出部分20分离。这样，对于高频信号(例如，频率高于1GHz的信号)，凸出部分20不会显著影响信号过孔24的电容，使得信号过孔24保持固有电感。在如图2所示的一个实施例中，颈部50具有沿轴线80的长度l1和垂直于轴线80的宽度w_1确定的大致矩形。长度l_1在导电焊盘30的外边缘34和凸出部分20的近端54(假想线中所示)之间延伸。

在各种实施例中，凸出部分20可以具有从经过颈部50的轴线80横向地向外凸出和/或者凸起的对称形状。例如，凸出部分20可以具有拱形凸起，如图2中所示。凸出部分20的拱形凸起可以从一侧到另一侧延伸距离d，该距离d大于颈部50的宽度w_1。例如，颈部50的宽度w_1可以是0.025英寸，而凸出部分20的距离d可以是0.035英寸。通过插入在凸出部分20与信号迹线部分14之间的连接部分70，凸出部分20可以连接到信号迹线部分14(如图2中所示)。或者，凸出部分20可以直接连接到信号迹线部分14(未示出)。在如图2中所示的一个实施例中，在位于禁区22内的细长信号导体带17的中点，凸出部分20位于导电焊盘30的外边缘34与禁区22的外边缘r_3之间的中间。

在一些实施例中，凸出部分20具有横向弯曲形状的凸出和/或凸起。在一些实施例中，可以对着半圆部分的拱形部分横向地从轴线80向外凸出和/或者凸起，如图2中所示。其他形状的凸起也是可能的。

如图2中所示，在一些实施例中，过孔结构18包括位于禁区22内、从凸出部分20延伸的连接部分70。在凸出部分20的远端66(假

想线中所示)与禁区22之间，连接部分70可以具有大致矩形。连接部分70的宽度可以小于凸出部分20的距离d，而且可以与信号迹线部分14的宽度w_2相同。例如，连接部分70的宽度可以是0.025英寸。

尽管所示的凸出部分20具有大致拱形凸起，但是凸出部分20可以具有任意几何形状，以便凸出部分20具有建立过孔结构18的预定阻抗的电容。例如，凸出部分20可以是多边形的，例如菱形的。凸出部分20的几何形状不需要是对称的，而且可以是非规则形状。此外，可以利用沿近端54与远端66之间的轴线80延伸的长度和垂直于轴线80的宽度确定凸出部分20的形状。

图3示出过孔结构318的实施例的方框图。在图3的实施例中，凸出部分320沿从颈部350延伸的曲线向外凸起距离w_3，而在凸出部分320的远端366收缩到宽度w_2。在其他实施例中(未示出)，凸出部分320可以沿直线向外凸起，该直线离开轴线80垂直收缩或者延伸。如在图2的实施例中，可以改变颈部350的宽度，但是它小于凸出部分320的距离w_3。而且，如在图3中可以看出，可以改变颈部350的长度，在图2中利用l_1表示该长度，而且可以将它缩小到0或者接近0，如图3中所示。如图3中所示，在从凸出部分320的外部观看时，凸出部分320基本上是凸形的或者具有凸形外表面。

所示的禁区22内的连接部分370将位于远端366的凸出部分320连接到信号迹线部分314。在其他实施例中，凸出部分320可以延伸到禁区22的边缘，或者禁区22之外。

在未示出的一些实施例中，导电焊盘和凸出部分通常都具有在导电焊盘与凸出部分之间形成颈部的隙缝或者其他开槽的泪珠形状。

图4示出多层印刷电路板410的一部分的横截面图。通过利用半固化片86将各印刷电路板12粘连在一起形成多层印刷电路板410，各

印刷电路板12分别具有芯84和位于芯84的两侧上的相对的导体层82。在一些实施例中(未示出)，如在本技术领域内公知，在邻近的芯84上的导体层82之间，可以将几层半固化片夹入诸如导电箔的导体层。其他布置也是可能的。

尽管在图4中仅示出8个导体层82，但是印刷电路板410可以具有更多或者更少的导体层82。为了说明目的，利用实心层示出导体层82。导体层82可以包括导体面、迹线、过孔结构等。

图5示出包括根据本发明的可能性实施例的过孔结构518的单芯584a印刷电路板510的横截面图。印刷电路板510可以是多层板的部分(图5中未示出)。过孔结构518的信号过孔524通过芯5 84a，以通过导电焊盘530、颈部550、凸出部分520以及连接部分570，连接到信号迹线部分514。

印刷电路板510包括接地导体515，它可以是接地迹线或者接地面。如图5中所示，接地导体515位于禁区522的外部，但是其近端延伸到禁区522。因此，禁区522表示通常没有接地导体515的区域。

如图5中所示，接地导体515与信号迹线部分514相邻。然而，连接在信号过孔524与信号迹线部分514之间的信号导体带的分段延伸通过禁区522，以使信号过孔524与信号迹线部分514相连，而没有相应邻近的接地导体515。

在一个实施例中，接地导体515是基本上平行于信号迹线部分514的迹线，而且其图案与信号迹线部分514的图案相同。在另一个实施例中，接地导体515是接地面。在该实施例中，在印刷电路板510上，信号迹线部分514与接地导体515组合形成微带信号迹线部分514。

可以确定凸出部分520的大小，而且沿细长信号导体带517定位

凸出部分520，以便能够在凸出部分520与接地导体515之间，即，通过边缘电容，实现电容耦合。凸出部分520的电容基于凸出部分520的大小和形状、凸出部分520的材料以及芯584a层(或者未示出的其他层之间的)的材料。此外，凸出部分520的电容还基于凸出部分520与信号过孔524之间的距离、禁区距离r_3以及相邻接地导体的数量。在一个实施例中，凸出部分520的电容主要归因于凸出部分520与接地导体515之间的电容。图5中所示的细长信号导体带517的凸出部分520基本上位于定位在禁区522处的接地导体515的近端与导电焊盘530的外边缘534之间的中间。

在一个实施例中，信号过孔524包括印刷电路板510的上表面525上的任选接触焊盘526。接触焊盘526可以提供印刷电路板510与该印刷电路板510外部的电路之间的接口。这样，可以通过接触焊盘526在信号过孔524与该电路之间发送信号。例如，印刷电路板510可以是器件接口板(DIB)、探测器接口板(PIB)或者处理器接口板(HIB)的一部分。该电路可以包括用于测试半导体器件的装置的弹簧针(pogo pin)或者转接板(interposer)。接触焊盘526可以是用于将信号过孔524电连接到SMT连接器的表面贴装(SMT)焊盘。

图6示出根据本发明另一个实施例的印刷电路板610的部分的横截面图。信号过孔结构618具有通过芯684a的信号过孔624，以通过导电焊盘630、颈部650、凸出部分620以及连接部分670，连接到信号迹线部分614。

在图6所示的实施例中，对细长信号导体带617的信号迹线部分614设置两个接地导体615和619。接地导体615和619位于禁区622之外，但是其近端延伸到禁区622。如图6中所示，在两侧具有相对的接地导体615和619的信号迹线部分614有时被称为带线信号导体。

确定凸出部分620的大小，而且沿细长信号导体带617定位凸出

部分620，以便与接地导体615和619具有边缘电容。在各种实施例中，接地导体615和619可以是如上所述的接地面和/或者接地迹线。在包括任选接触焊盘626的实施例中，凸出部分620可以与如上所述的接触焊盘626具有边缘电容。

印刷电路板610可以是多层层叠的印刷电路板的部分(图6中未示出)。所示的接地过孔616延伸通过芯684a和半固化片686，以电连接到接地导体615和619。所示的接地过孔616延伸通过芯684a，而且如果需要，可以延伸到接触其他接地导体(未示出)。其他实施例也是可能的。

利用三维电路仿真程序，可以对上述的过孔结构和印刷电路板建模，并模拟它们。这种三维电路仿真程序的实例有Pitsburg，PA的Ansoft Corp.，www.ansoft.com市售的高频结构仿真器(HFSS)。

这样，可以确定凸出部分的电容，以根据选择的配置和材料，建立信号过孔结构的预定阻抗。因此，可以配置凸出部分，以具有对信号过孔结构提供选择的阻抗的电容。此外，可以将印刷电路板制造为具有多个信号过孔结构的，每个信号过孔结构分别具有对其相关信号过孔的特性定制以对每个信号过孔结构形成适当阻抗的凸出部分。

图7是包括过孔结构(未示出)的测试器700的一个实施例的方框图。测试器700包括测试器主机702，连接该测试器主机702，以便与测试头708和与该测试头708相关的接口板706通信，该接口板706可以连接到测试头708。在图7中所示的实施例中，接口板706是器件器件接口板。在工作中，接口板706电连接到被测器件(DUT)704，用于测试DUT 704。例如，测试器700可以是用于测试集成电路的自动测试装备(ATE)系统，而DUT 704可以是包括集成电路的半导体器件。接口板706可以是印刷电路板10(图1，4，5或者6)或可以包括印刷电路板10(图1，4，5或者6)。

测试器主机702包括用于产生测试信号并评估测试信号的电路。通过测试头708和接口板706，测试器主机702将测试信号发送到DUT 704并从DUT 704接收测试信号。DUT 704可以是包括要被测试的集成电路的封装芯片。在另一个实施例中，接口板706是探测器接口板，而DUT 704可以是包括要被测试的集成电路的半导体晶片。

在各种实施例中，接口板706和/或者测试头708可以包括含有如上所述的信号过孔结构的多层印刷电路板。

在此描述的实施例用于说明本发明。当参考图解描述本发明的这些实施例时，所描述的方法和/或特定结构的各种修改或者调整对于本领域内的技术人员变得显而易见。可以认为基于本发明的教导，而且通过它们这些教导已经改进了该领域的所有这些修改、调整或者改变均在本发明的精神和范围内。因此，不应该认为这些描述和附图具有限制性意义，因为应该明白本发明并不仅仅局限于所说明的实施例。

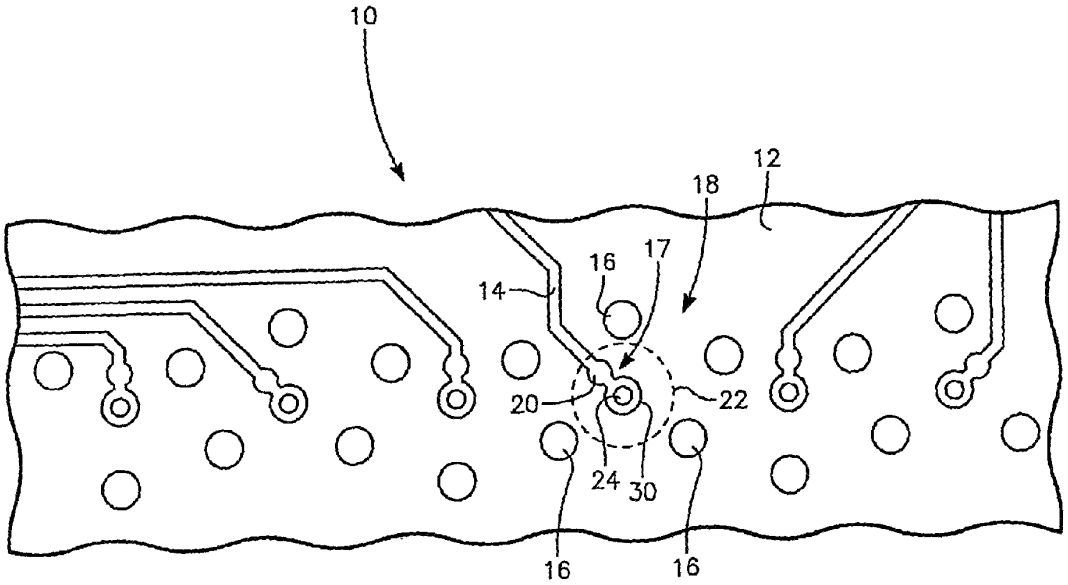


图1

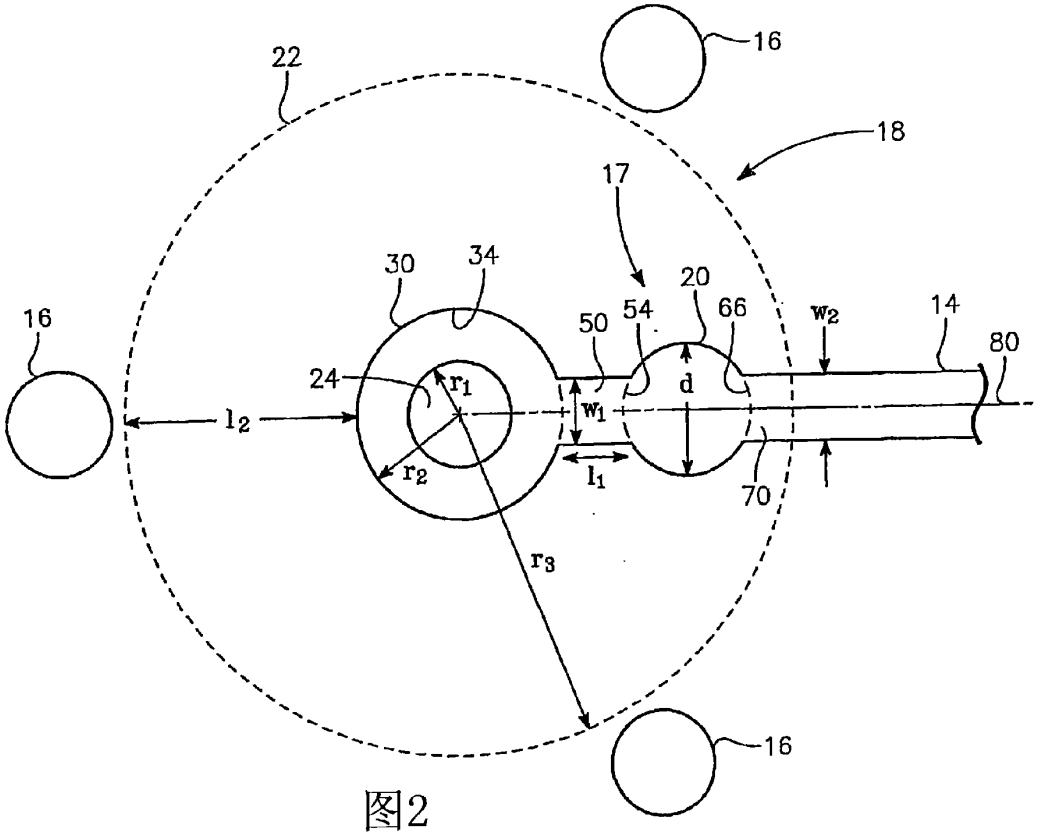


图2

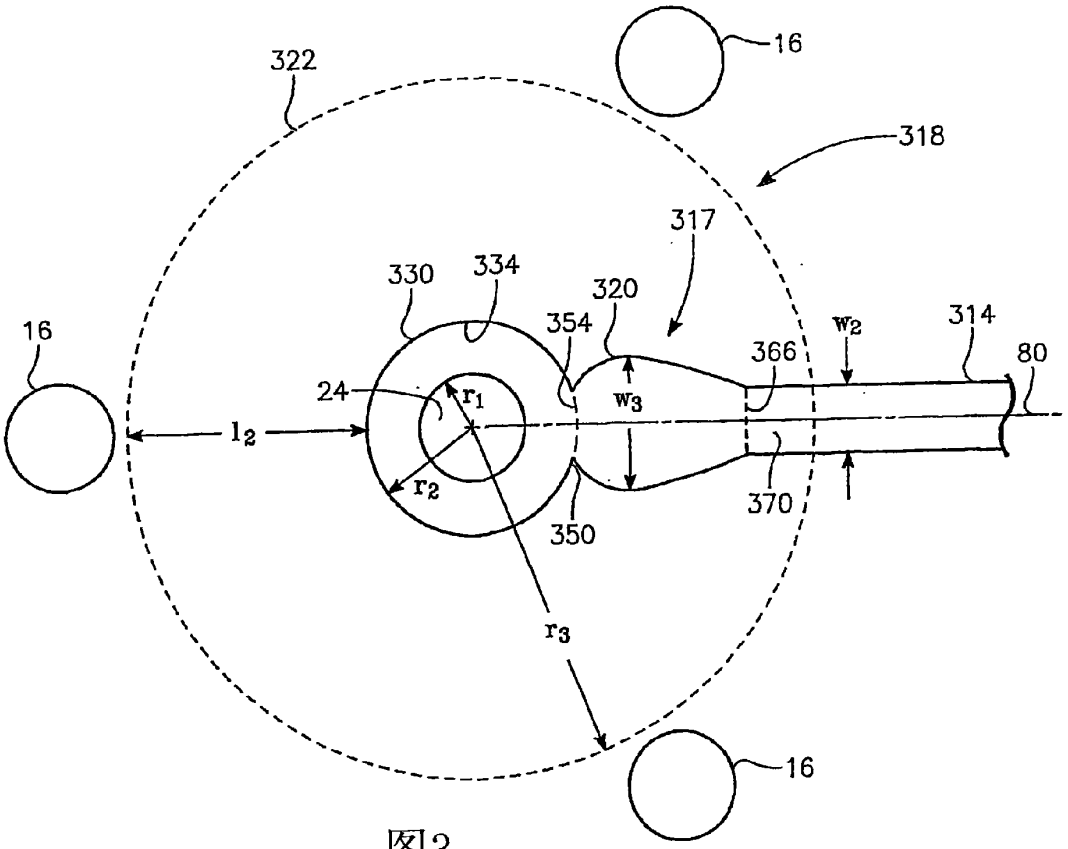


图3

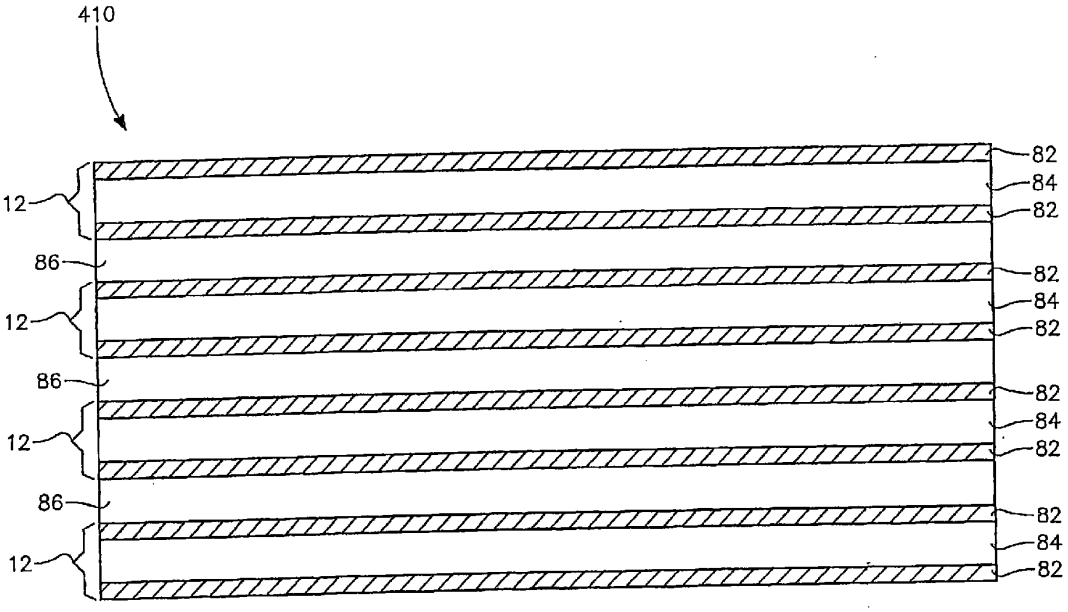


图4

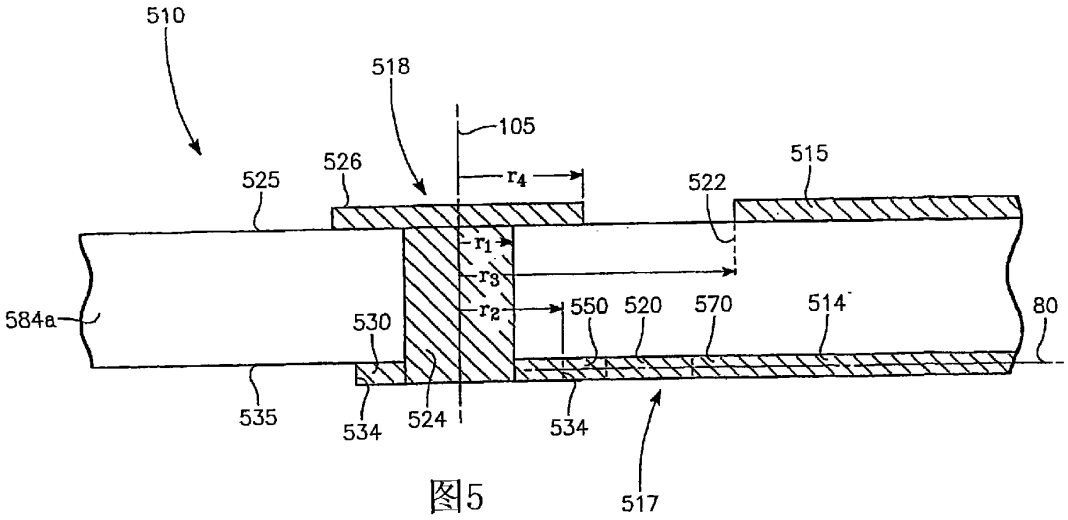


图5

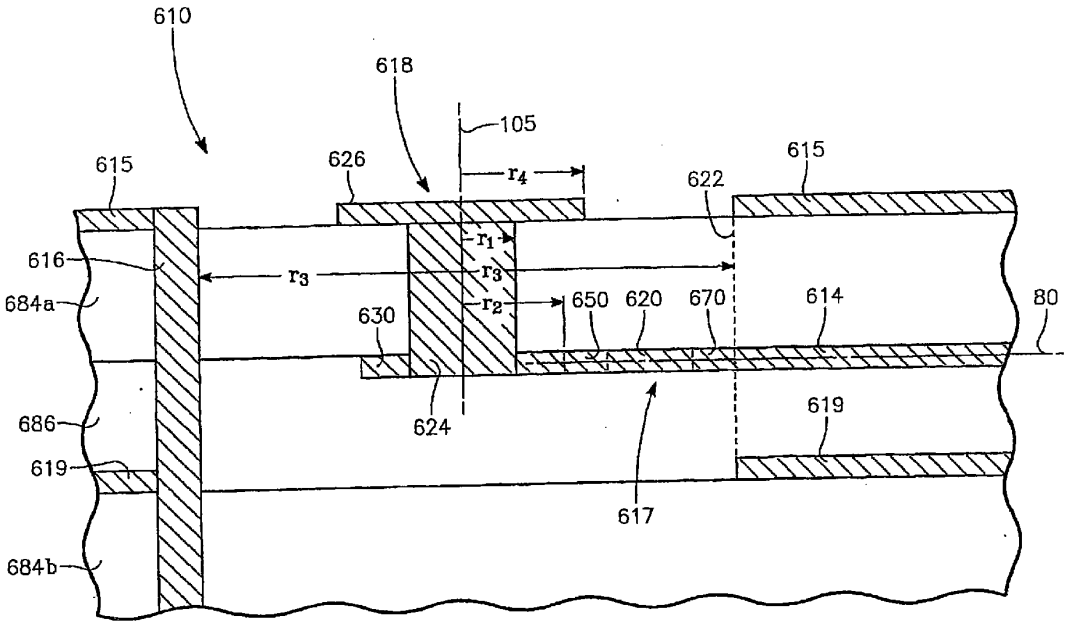


图6

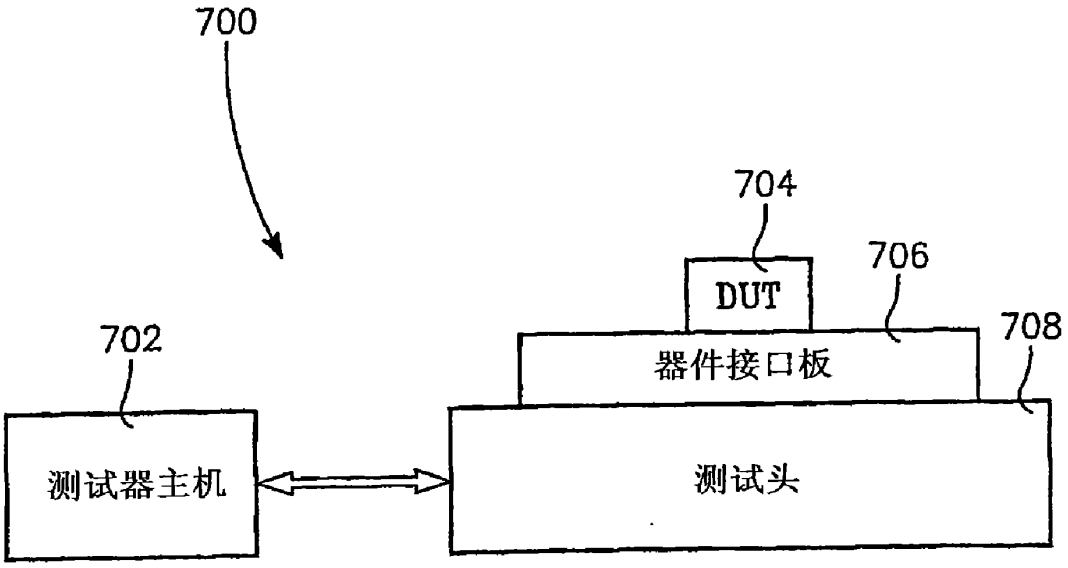


图7

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Family members: CN101600293 A CN101600293 B US2009301768 AA US8077472 BB

Title: Printing circuit board

Title: 印刷电路板

Abstract:

The invention discloses a printing circuit board comprising a board body, a through hole is drilled on the board body, and the printing circuit board is fixedly connected with an earthing element via the through hole; the surface of the printing circuit board around the through hole is provided with a tin coating which is in contact with the earthing element, and the printing circuit board is in electrical conduction with the earthing element; and the periphery of the through hole is provided with solder mask preventing the tin cream of the tin coating from flowing into the through hole. The printing circuit board of the invention has the advantages of short processing time, low cost and anti-electromagnetic interference.

Abstract:

一种印刷电路板，其包括一个板体，板体上开设有一个通孔，印刷电路板通过通孔与接地元件固定连接。该印刷电路板的表面于通孔的周围设有一个镀锡层，镀锡层与接地元件接触且印刷电路板与接地元件保持电性导通。通孔的周围设有用于阻止该镀锡层的锡膏流入该通孔的防焊漆。本发明印刷电路板具有加工时间短、成本低及抗电磁干扰的优点。

A printed circuit board including a board member, the board body set up with a through-hole printed circuit board by means of through-hole and the ground element fixedly connected. The surface of the printed circuit board around the through hole is provided with a layer of tin, tin plating layer in contact with the ground element and the printed circuit board ground element holding electrically conductive. Paste around the through-hole is provided for preventing the tin layer through-hole solder flows into the paint. The present invention is a printed circuit board having a short processing time, low cost and anti-electromagnetic interference advantages.

Claims:

[权利要求1]一种印刷电路板，其包括一个板体，该板体上开设有一个通孔， 该印刷电路板通过该通孔与接地元件固定连接，该印刷电路板的表面于该通孔的周围设有一 个镀锡层，该镀锡层与该接地元件接触且该印刷电路板与该接地元件保持电性导通，其特征 在于:该通孔的周围设有用于阻止该镀锡层的锡宫流入该通孔的防焊漆。

A printed circuit board [Claim 1], which comprises a plate, the opening of the plate member has a through hole through which the printed circuit board through-hole member is fixedly connected to the ground, the surface of the printed circuit board on the periphery of the through hole is provided with a tin layer, the tin layer in contact with the ground element and the printed circuit board to maintain electrical conduction with the ground element, wherein: the periphery of the through hole is provided for blocking the tin layer of tin house flows into the through-hole solder paint.

[权利要求幻如权利要求1所述的印刷电路板，其特征在于:该镀锡层由该防焊 漆隔开为均匀分布于通孔周围的四个扇形区域。

[magic claim 1 wherein the printed circuit board as claimed in claim wherein: the tin layer is made of the solder resist lacquer is evenly spaced in all four fan-shaped area around the through hole.

[权利要求3]如权利要求1所述的印刷电路板，其特征在于:该印刷电路板上还 设有一个螺钉，该螺钉穿过该印刷电路板的通孔并螺合于接地元件上。

[Claim 3] The printed circuit board as claimed in claim wherein: the printed circuit board is also provided with a screw, the screw through the through holes of the printed circuit board and screwed into the ground element.

[权利要求们如权利要求3所述的印刷电路板，其特征在于:该饭体依次包括一 个第一铜箔层、一个第一钢板层、一个接地层、一个第二钢板层及一个第二铜箔层。

[权利要求田如权利要求4所述的印刷电路板，其特征在于:该第一钢板层上设 有多个第一锡盘，该多个第一锡盘贯穿并凸出于该第一铜箔层，该螺钉的帽部与该多个锡盘 接触并与接地层保持电性导通。

[权利要求门如权利要求5所述的印刷电路板，其特征在于:该第二钢板层上设 有多个第二锡盘，该多个第二锡盘贯穿并凸出于该第二铜箔层，该镀锡层覆盖该第二铜箔层 及该多个第二锡盘。

[权利要求7]如权利要求6所述的印刷电路板，其特征在于:该防焊漆涂覆于该 第二铜箔层上。

[权利要求8]如权利要求6所述的印刷电路板，其特征在于:该印刷电路板上还 开设有多个过孔，该第一铜箔层及该第二铜箔层通过过孔内的焊盘与其他板层保持电性导通

[as claimed in claim 3 are printed circuit board according to claim, characterized in that: the food, in order, comprises a first layer of copper, a layer of a first plate, a ground layer, and a second layer of steel a second layer of copper foil.

[Tian claim 4, wherein the printed circuit board as claimed in claim, characterized in that: a plurality of first steel sheet tin plate on the first layer, the plurality of first tin plate and protrude through the the first copper layer, the cap portion of the screw is in contact with the tin plate and a plurality of electrically conductive ground plane.

[door of claim 5, wherein the printed circuit board as claimed in claim, characterized in that: a plurality of second tin plate on the second layer of steel plate, the plurality of second tin plate and protrude through the the second layer of copper foil, the tin foil layer covers the second layer and the second plurality of tin plate.

[Claim 7] The printed circuit board 6 as claimed in claim wherein: the solder resist lacquer is coated on the second copper foil layer.

[Claim 8] The printed circuit board 6 as claimed in claim wherein: the printed circuit board is also formed with a plurality of vias, the first layer and the second copper foil layer is formed by through hole pads and other board layers remain electrically conductive

Description:

印刷电路板 技术领域 本发明涉及一种印刷电路板。

背景技术 印刷电路板在电子行业中有右广泛的应用，印刷电路板在使用时，由于电子组件间的干 扰，往往会由干扰电流产生大量宽频噪声或杂讯，严重影响印刷电路

Printed circuit board TECHNICAL FIELD The present invention relates to a printed circuit board.

BACKGROUND printed circuit board has a right widely used, the printed circuit board is in use, due to the interference

板的功能，一般称这种 现象为电磁干扰 (Eleclro Magnelic Inlerference; EMI) o 为了降低印刷电路板在使用过程中的电磁干扰，通常需要将引起电磁干扰的电流导向大 地。一般情况下，会在印刷电路板上开设一个通孔，将一个螺钉穿过通孔并螺合于一个与大 地保持电性导通的壳体上，以便于将印刷电路板上的干扰电流通过螺钉及壳体导向大地。通 孔的周围在印刷电路板的表面上一般设有一个镀铜层，印刷电路板上的电流流向大地时会经 过该镀铜层，镀铜层容易被空气氧化而不利于将印刷电路板上的电流导出。因此，通常会在通孔周围镀铜层上涂覆一层锡宫，然后经过锡炉使锡宫更好地附着于镀铜层上，然而经过锡 炉时，锡宫容易流入通孔而产生封孔问题。现有技术中为防止封孔问题的产生，在印刷电路 经过锡炉前，先用贴胶带的万式将通孔封住，然而，贴胶带极为浪费时间，通常需要增加人 力，从而增加了生产成本。

发明内容 鉴于上述状况，有必要提供一种加^时间短且成本较低的印刷电路板。

一种印刷电路板，其包括一个板体，该板体上开设有一个通孔，该印刷电路板通过该通 孔与接地元件固定连接。该印刷电路板的表面于通孔的周围设有一个镀锡层，镀锡层与接地 元件接触且印刷电路板与接地元件保持电性导通。通孔的周围设有用于阻止该镀锡层的锡宫 流入该通孔的防焊漆。

与现有技术相比，印刷电路板的通孔周围设有防焊锡，印刷电路板经过锡炉时，防焊漆 可阻止镀锡层的锡宫流入印刷电路板的通孔中，防止了封孔问题的产生。在通孔周围涂覆防 焊锡操作简单，可有效缩短加^时间，从而降低了生产成本。

附图说明 图1是本发明较佳实施例的印刷电路板的局部俯视图。

图2是本发明较佳实施例的印刷电路板的局部仰视图。

书 明 说 图3是图1所示的印刷电路板沿1_I11线的局部剖视图。

between electronic components, tends to produce a lot of noise from the broadband noise or interference currents in the electronics industry, seriously affecting the printed circuit board function, generally referred to this phenomenon as electromagnetic interference (Eleclro Magnelic Inlerference; EMI) o In order to reduce the printed circuit board in the course of electromagnetic interference, and often need to guide electromagnetic interference caused by the current land. Under normal circumstances, it will open a through hole in the printed circuit board, a screw through the through holes and screwed into the earth on a holding electrically conductive housing, in order to interfere with the current printed circuit board through screw and guide housing earth. Around the through hole on the surface of the printed circuit board generally has a copper layer, printed circuit board when the current flows through the copper layer of the earth will, copper plating layer is easily oxidized by air to the detriment of the printed circuit board Current export. Therefore, usually coated with a layer of tin around the palace in the through-hole copper plating layer, and tin after tin stove palace to better adhere to the copper layer, but after a while tin stove, tin palace easily flow through holes and produce Sealing problems. The prior art is to prevent plugging problems in the printed circuit through tin stove, first with the taping of the square sealed through-hole type, however, taping extremely waste of time, usually we need to increase manpower, thereby increasing production cost.

In view of the above circumstances, it is necessary to provide an add short time and low cost of the printed circuit board.

A printed wiring board, which comprises a plate, the opening of the plate member has a through hole, the printed circuit

图4是图1所示的印刷电路板沿IV-IV线的局部剖视图。

图5是图1所示的印刷电路板与电子装置的壳体固定连接后的局部示意图。

具体实施万式 下面将结合附图及较佳实施例对本发明的印刷电路板作进一步的详细说明。

请参见图1与图2，本发明较佳实施例的印刷电路板10包括一个板体12以及开设于板体 12上的圆形通?L14与多个过?L16，多个过?L16均匀分布于的通?L14周围。印刷电路板10可通 过通?L14与电子装置的接地元件固定连接，而使印刷电路板10与大地保持电性导通。

板体12包括一个第一表面122及一个与第一表面122相对的第二表面124。通孔14的周围 于板体12^f^q第一表面122±设有多个第一锡盘18及一个第一铜箔层20，多个第一锡盘18均匀 分布于通孔14的周围。多个第一锡盘18与多个过?L16相互交钳地均匀分布于通孔14的周围。

板体12^f^q第二表面124于通孔14的附近涂覆有一个镀锡层22，通孔14的周围于通?L14与镀锡 层22之间设有防焊漆24 (Solder mask Or Solder Resisl)，且镀锡层22由防焊漆24隔开为 四个均匀分布于通?L14周围的扇形区域，而阻止镀锡层_」fiq锡宫流入通?L14中。防焊漆24一 般称为"绿漆"，为便于肉眼对印刷电路板10的检查，在主漆中多加入对眼睛有帮助的绿色颜 料，防焊漆24除了为绿色之外还可为黄色、白色、黑色或其它颜色。防焊漆24可阻止锡宫流 过防焊漆24所在的E域。

可以理解，通孔14的周围设有防焊漆24，且镀锡层22由防焊漆24隔开为四个E域，这样 当印刷电路板经过锡炉时，防焊漆24可有效阻止镀锡层_」_q锡宫流入通孔14，从而避免了封 孔问题的产生。镀锡层22还可被防焊漆24隔开为两个、三个或四个以上的E域，镀锡层22也 可不被隔开，而仅在镀锡层22与通?L14之间设有防焊漆24。通?L14不限于圆形，还可为万形 或其他形状。

board with a through hole through which the ground element is fixedly connected. The surface of the printed circuit board around the through hole is provided with a tin layer, tin plating layer in contact with the ground element and the printed circuit board and the ground element holding electrically conductive. Around the through-hole is provided for preventing the tin layer of tin palace flowing into the through-hole solder paint.

Compared with the prior art, the printed circuit board around the through-hole with anti-solder, printed circuit board passes through the furnace, paint can prevent solder tin tin layer printed circuit boards Palace inflow through holes, preventing the generation of sealing problem. Around the through-hole solder coating Anti simple, can effectively shorten add time, thereby reducing production costs.

BRIEF DESCRIPTION OF DRAWINGS FIG. 1 is a partial top plan view of a printed circuit board of the preferred embodiment of the present invention.

2 is a partial bottom view of a preferred embodiment of a printed circuit board of the present invention.

Shuming said FIG. 3 is a partial cross-sectional view of the printed circuit board shown in Figure 1 along 1_ I11 lines.

Figure 4 is a partial cross-sectional view of the printed circuit board shown in Figure 1 along the line IV-IV.

FIG. 5 is a partial schematic view of the printed circuit board shown in FIG. 1 and the electronic device housing fixedly connected after.

DETAILED DESCRIPTION square formula below in conjunction with the accompanying drawings and the preferred embodiment of the printed circuit board of the present invention will

请一并参见图3与图4，印刷电路板10的板体12由多个板层组成。板体12各板层从第一表 面122到第二表面_4^fiq顺序分别为:第一铜箔层20、第一钢板层28、接地层30、第二钢板层 32及第二铜箔层26。过?L16内还设有多个焊盘(图未示)，多个焊盘分别位于板体12」fiq不同 板层上，从而使得第一铜箔层20及第二铜箔层26通过过?L16内的焊盘与其他板层保持电性导 通。

多个第一锡盘18位于第一钢板层28±，其贯穿并凸出于第一铜箔层20，多个第一锡盘 18与第一钢板层28保持电性导通。接地层30与大地保持电性导通，其与第一钢板层28及第二 钢板层32间为非电性导通。第二钢板层32±也设有均匀分布于通?L14周围的多个第二锡盘34 书 明 说 ，多个第二锡盘34贯穿并凸出于第二铜箔层26，其与第二钢板层32保持电性导通。镀锡层22 覆盖于第二铜箔层26及多个第二锡盘34±，防焊漆24涂覆于该第二铜箔层26±阻止镀锡层22 的锡宫流入通?L14。可以理解，板体12^f^q板层结构不限于本实施例中所列举的情形，只需在 层与层之间建立导电通道即可。

请参见图5，下面对本发明较佳实施例的印刷电路板10抗电磁干扰的^作原理作详细说 明。

印刷电路板10±还设有一个螺钉36，组装时，印刷电路板10通过螺钉36与电子装置的壳 体38固定连接，螺钉36包括帽部362和杆部364，杆部364在远离帽部362的一端设有螺纹，螺 钉36^f^q杆部364穿过印刷电路板10的通?L14并螺合于壳体38±。螺钉_」^帽部362与多个第一 锡盘18相接触，印刷电路板10的镀锡层22与壳体38相接触。印刷电路板10的各板层与螺钉 36保持电性导通。在本实施例中，因为多个第一锡盘18及镀锡层22被隔开的四个扇形区域均 匀分布在通孔14的周围，所以印刷电路板10与螺钉_」^帽部362间以及印刷电路板10与壳体 38间均具有较佳且均匀分布的接触面，有利于将引起杂讯的电流导出。可以理解，依实际需 要，印刷电路板10可与电子装置上任意的接地元件连接。

be described in further detail. see Figure 1 and Figure 2, the preferred embodiment of the invention the printed circuit board 10 includes a plate member 12 and the opening in the upper plate member 12 of circular through? L14 with a plurality of through? L16, a plurality of through? L16 evenly distributed in the pass? L14 around. Printed circuit board 10 can pass through? L14 ground element fixedly connected with the electronic device, leaving the printed circuit board 10 remains electrically conducting earth. plate member 12 includes a first surface 122 and a surface 122 opposing the first surface 124 of the second. Around the through hole 14 in plate 12 f q of the first surface 122 plus or minus 18 tin plate has a plurality of first and a first copper layer 20, a first plurality of evenly distributed in the tin plate 18 through hole 14 around. A plurality of first tin plate 18 with a plurality of through? L16 mutually cross-clamp evenly distributed around the through hole 14 in. plate member 12 f q of the second surface 124 in the vicinity of the through-hole 14 is coated with a tin layer 22, on through? 22 is provided between the solder resist lacquer around the through hole 14 and the tin plating layer L14 24 (Solder mask Or Solder Resisl), and tin solder resist layer 22 is made up of 24 separated into four evenly distributed in the paint through? L14 fan-shaped area around the tin layer is prevented _ "fiq Tin Palace inflows through? L14 in. Solder Mask 24 generally known as "masking", in order to facilitate visually inspect the printed circuit board 10, the main paint added more helpful eyes green paint, solder resist 24 except for the addition of green paint but also for yellow, white, black or other colors. Paint tin solder 24 can prevent flow through the E domain Palace solder lacquer 24 is located.

It will be appreciated around the through hole 14 is provided with solder lacquer 24

印刷电路板10±引起杂讯的电流流向大地的路径有多种，比如一条路径为螺钉_」^帽部 362^(第一锡盘1^(第一钢板层28^(螺钉_」^杆部364^(接地层30^(大地，此路径的阻抗较低，电 流优先从该路径流向大地:另一条路径为螺钉_」^帽部362^(第一锡盘1^(第一钢板层28^(螺钉 _」^杆部364^(壳体38^(大地。在本实施例中，第一铜箔层20及第二铜箔层26通过过?L16内的焊盘与其他板层保持电性导通，印刷电路板10的各板层与螺钉36保持电性导通，同时印刷电 路板10的镀锡层22与壳体38保持电性导通，因此，电流的流经路径不限于以上列举的两种， 这样在印刷电路板10与大地间建立了多个电流通道，从而能有效地将印刷电路板10±引起杂 讯的电流导向大地，降低电磁干扰。

在本实施例中，通孔14的周围于镀锡层22与通?L14之间设有防焊漆24，而不用采用贴胶 带的方式将通孔14封住，印刷电路板10经过锡炉时，由于防焊漆24」fiq隔阻，镀锡层22」fiq锡富 不会流入通?L14中，在通?L14周围涂覆防焊锡操作简单，可有效缩短加^时间，从而降低了 生产成本。此外，因为防焊漆24将镀锡层22隔开为四个均匀分布于通?L14周围的E域，印刷 电路板10与电子装置的壳体38固定连接后，镀锡层22与壳体38接触使得印刷电路板10与壳体 38间具有较好的接触面，有利于将印刷电路板10±引起杂讯的电流导向大地，从而达到抗电 磁干扰的目的。

另外，本领域技术人员还可在本发明精神内做其它变化，当然，这些依据本发明精神所 做的变化，都应包含在本发明所要求保护的范围内。

and 24 are separated by a tin solder layer 22 paint four E domains, such as a printed circuit board passes through the furnace, solder paint 24 can effectively prevent the tin layer _ "_ q Tin Palace inflow through hole 14, thus avoiding the problem of sealing. Solder Mask 22 may also be two, three or four or more E domains, tin plating layer 22 may not be separated by 24 separated, but only in the tin plating layer 22 and the via? L14 between the tin coating 24 has solder paint. Through? L14 is not limited to circular, but also for the million-shaped or other shapes.

Please also refer to FIG. 3 and FIG. 4, the plate member 12 of the printed circuit board 10 by a plurality of sheet layers. Each lamellar plate 12 from the first surface 122 to the second surface _4 fiq order are: a first copper foil layer 20, a first steel layer 28, ground layer 30, a second steel layer 32 and the second copper foil layer 26. Through? L16 also has a plurality of inner pads (not shown), a plurality of pads 12 are located on the 'fiq different lamellar plate, so that the first layer 20 and the second copper foil layer 26 by over-? pad L16 is kept electrically conductive layer and the other plate. tin plate a plurality of first layer 18 located between the first plate 28 plus or minus, which runs through and projecting from the first copper foil layer 20, a plurality of first plate 18 and the tin layer 28 of the first sheet holding electrically conductive. Ground layer 30 remains electrically conductive and the earth, with the first steel layer 28 and the second plate layer 32 is non-electrically conductive. The second steel layer 32 plus or minus also has uniformly distributed through? Multiple L14 around 34 books confessed second tin plate, tin plate 34 through a plurality of second and protruding from the second copper foil layer 26, with the second steel layer 32 remains electrically conductive. Tin layer

22 covers the second copper foil layer 26 and a plurality of second tin plate 34 plus or minus, solder coating paint 24 to the second copper foil layer 26 plus or minus 22 tin tin coating prevents inflow through the palace? L14. Will be appreciated, the plate member 12 f q lamellar structure is not limited to the present embodiment in the case exemplified embodiment, can simply establish a conductive path between the layers.

Refer to Figure 5, the present invention below the printed circuit board 10 against electromagnetic interference as a preferred embodiment of the principle of detailed instructions. the printed circuit board is also provided with a screw 10 plus or minus 36, when assembled, the printed circuit board 10 by screws 36 and 38 fixedly connected to the housing of the electronic device, the screw 36 includes a cap portion 362 and lever portions 364, 364 in the lever portion away from the cap portion 362 is provided with a threaded end, a screw 36 f q rod portion 364 passes through the through the printed circuit board 10? L14 and screwed to the housing 38 plus or minus. Screw _ " cap portion 362 with a plurality of first contact with the tin plate 18, 22 tinned layer contacting the printed circuit board 10 with the housing 38. Each plate layer printed circuit board 10 with the screw 36 to maintain electrical conduction. In this embodiment, since a plurality of first tin plate 18 and 22 are separated by four quadrants region tin layer evenly distributed around the through hole 14, so that the printed circuit board 10 with screws _ " cap portion 362 and a printed circuit board 10 and the housing 38 have a better and uniform distribution of the contact surface is conducive to export the current noise of the cause. It is appreciated that, according to the actual needs, the printed circuit board 10 may be connected to any ground element on the electronic device.

earth current flowing path of the printed circuit board 10 plus or minus There are many causes of noise, such a path is a screw _ " cap portion 362 (first tin plate 1 (a first steel layer 28 (screw _ " rod section 364 (a ground layer 30 (earth, low impedance path, current flows from the path priority land: another path to screw _" cap portion 362 (first tin plate 1 (Article A sheet layer 28 (_ screw "stem portion 364 (38 housing (earth. In the present embodiment, the first layer 20 and the copper foil layer 26 by a second over? pads inside and L16 Other board layer remains electrically conductive, each board layer printed circuit board 10 with the screw 36 to maintain electrical conduction, while tin layer printed circuit board 10 and 22 remains electrically conductive housing 38, therefore, the current flow path is not limited to two listed above, so that between the printed circuit board 10 and the ground to establish a plurality of current channels, which can be effectively printed circuit board 10 plus or minus guide earth current causing noise, reduce electromagnetic interference.

In this embodiment, in the tin layer 22 and pass? Provided around the through hole 14 between the solder lacquer L14 24, instead of using taped sealed manner through hole 14, a printed circuit board 10 past the furnace, because the solder paint 24 "fiq deadening, tin layer 22 'fiq tin rich does not flow through? L14, the pass? simple anti-solder coating operation around L14, can effectively reduce the increase time, thereby reducing production costs. Further, since the tin solder resist lacquer layer 24 into four 22 spaced evenly distributed through? 10 fixedly coupled around the E field L14, the printed circuit board and the electronic device housing 38, the tin layer 22 and the housing 38 makes contact with the printed circuit board 10 and the housing 38 has a better contact surface,

is conducive to the printed circuit board 10 plus or minus caused by the noise of the current guide the earth, so as to achieve the purpose of anti-electromagnetic interference.

In addition, the skilled staff can do other variations within the spirit of the present invention, of course, these are made in accordance with the spirit of the present invention, the change should be included within the protection scope of the invention as claimed.

Cited by: CN103167721 A ; CN103167723 A ; CN106163245 A ; CN108336593 A ; GB2543987 A1 ; TWI459873 B ; WO16026161 A1 ; WO17008510 A1 ;

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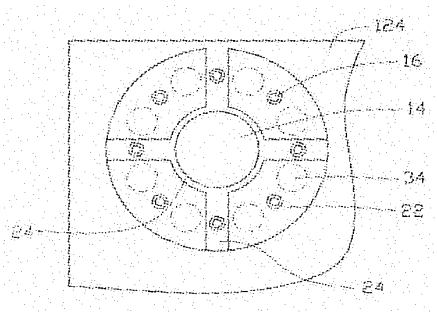
权利要求书 1 页 说明书 4 页 附图 3 页

[54] 发明名称

印刷电路板

[57] 摘要

一种印刷电路板，其包括一个板体，板体上开设有一个通孔，印刷电路板通过通孔与接地元件固定连接。 该印刷电路板的表面于通孔的周围设有一个镀锡层，镀锡层与接地元件接触且印刷电路板与接地元件保持电性导通。 通孔的周围设有用于阻止该镀锡层的锡膏流入该通孔的防焊漆。 本发明印刷电路板具有加工时间短、成本低及抗电磁干扰的优点。



【权利要求1】一种印刷电路板，其包括一个板体，该板体上开设有一个通孔，该印刷电路板通过该通孔与接地元件固定连接，该印刷电路板的表面于该通孔的周围设有一个镀锡层，该镀锡层与该接地元件接触且该印刷电路板与该接地元件保持电性导通，其特征在于：该通孔的周围设有用于阻止该镀锡层的锡膏流入该通孔的防焊漆。

【权利要求2】如权利要求1所述的印刷电路板，其特征在于：该镀锡层由该防焊漆隔开为均匀分布于通孔周围的四个扇形区域。

【权利要求3】如权利要求1所述的印刷电路板，其特征在于：该印刷电路板上还设有一个螺钉，该螺钉穿过该印刷电路板的通孔并螺合于接地元件上。

【权利要求4】如权利要求3所述的印刷电路板，其特征在于：该板体依次包括一个第一铜箔层、一个第一钢板层、一个接地层、一个第二钢板层及一个第二铜箔层。

【权利要求5】如权利要求4所述的印刷电路板，其特征在于：该第一钢板层上设有多个第一锡盘，该多个第一锡盘贯穿并凸出于该第一铜箔层，该螺钉的帽部与该多个锡盘接触并与接地层保持电性导通。

【权利要求6】如权利要求5所述的印刷电路板，其特征在于：该第二钢板层上设有多个第二锡盘，该多个第二锡盘贯穿并凸出于该第二铜箔层，该镀锡层覆盖该第二铜箔层及该多个第二锡盘。

【权利要求7】如权利要求6所述的印刷电路板，其特征在于：该防焊漆涂覆于该第二铜箔层上。

【权利要求8】如权利要求6所述的印刷电路板，其特征在于：该印刷电路板上还开设有多个过孔，该第一铜箔层及该第二铜箔层通过过孔内的焊盘与其他板层保持电性导通

印刷电路板

技术领域

本发明涉及一种印刷电路板。

背景技术

印刷电路板在电子行业中有着广泛的应用，印刷电路板在使用时，由于电子组件间的干扰，往往会由干扰电流产生大量宽频噪声或杂讯，严重影响印刷电路板的功能，一般称这种现象为电磁干扰（Electro Magnetic Interference; EMI）。

为了降低印刷电路板在使用过程中的电磁干扰，通常需要将引起电磁干扰的电流导向大地。一般情况下，会在印刷电路板上开设一个通孔，将一个螺钉穿过通孔并螺合于一个与大地保持电性导通的壳体上，以便于将印刷电路板上的干扰电流通过螺钉及壳体导向大地。通孔的周围在印刷电路板的表面上一般设有一个镀铜层，印刷电路板上的电流流向大地时会经过该镀铜层，镀铜层容易被空气氧化而不利于将印刷电路板上的电流导出。因此，通常会在通孔周围镀铜层上涂覆一层锡膏，然后经过锡炉使锡膏更好地附着于镀铜层上，然而经过锡炉时，锡膏容易流入通孔而产生封孔问题。现有技术中为防止封孔问题的产生，在印刷电路经过锡炉前，先用贴胶带的方式将通孔封住，然而，贴胶带极为浪费时间，通常需要增加人力，从而增加了生产成本。

发明内容

鉴于上述状况，有必要提供一种加工时间短且成本较低的印刷电路板。

一种印刷电路板，其包括一个板体，该板体上开设有一个通孔，该印刷电路板通过该通孔与接地元件固定连接。该印刷电路板的表面于通孔的周围设有一个镀锡层，镀锡层与接地元件接触且印刷电路板与接地元件保持电性导通。通孔的周围设有用于阻止该镀锡层的锡膏流入该通孔的防焊漆。

与现有技术相比，印刷电路板的通孔周围设有防焊锡，印刷电路板经过锡炉时，防焊漆可阻止镀锡层的锡膏流入印刷电路板的通孔中，防止了封孔问题的产生。在通孔周围涂覆防焊锡操作简单，可有效缩短加工时间，从而降低了生产成本。

附图说明

图1是本发明较佳实施例的印刷电路板的局部俯视图。

图2是本发明较佳实施例的印刷电路板的局部仰视图。

图3是图1所示的印刷电路板沿III-III线的局部剖视图。

图4是图1所示的印刷电路板沿IV-IV线的局部剖视图。

图5是图1所示的印刷电路板与电子装置的壳体固定连接后的局部示意图。

具体实施方式

下面将结合附图及较佳实施例对本发明的印刷电路板作进一步的详细说明。

请参见图1与图2，本发明较佳实施例的印刷电路板10包括一个板体12以及开设于板体12上的圆形通孔14与多个过孔16，多个过孔16均匀分布于的通孔14周围。印刷电路板10可通过通孔14与电子装置的接地元件固定连接，而使印刷电路板10与大地保持电性导通。

板体12包括一个第一表面122及一个与第一表面122相对的第二表面124。通孔14的周围于板体12的第一表面122上设有多个第一锡盘18及一个第一铜箔层20，多个第一锡盘18均匀分布于通孔14的周围。多个第一锡盘18与多个过孔16相互交错地均匀分布于通孔14的周围。板体12的第二表面124于通孔14的附近涂覆有一个镀锡层22，通孔14的周围于通孔14与镀锡层22之间设有防焊漆24 (Solder mask or Solder Resist)，且镀锡层22由防焊漆24隔开为四个均匀分布于通孔14周围的扇形区域，而阻止镀锡层22的锡膏流入通孔14中。防焊漆24一般称为"绿漆"，为便于肉眼对印刷电路板10的检查，在主漆中多加入对眼睛有帮助的绿色颜料，防焊漆24除了为绿色之外还可为黄色、白色、黑色或其它颜色。防焊漆24可阻止锡膏流过防焊漆24所在的区域。

可以理解，通孔14的周围设有防焊漆24，且镀锡层22由防焊漆24隔开为四个区域，这样当印刷电路板经过锡炉时，防焊漆24可有效阻止镀锡层22的锡膏流入通孔14，从而避免了封孔问题的产生。镀锡层22还可被防焊漆24隔开为两个、三个或四个以上的区域，镀锡层22也可不被隔开，而仅在镀锡层22与通孔14之间设有防焊漆24。通孔14不限于圆形，还可为方形或其他形状。

请一并参见图3与图4，印刷电路板10的板体12由多个板层组成。板体12各板层从第一表面122到第二表面124的顺序分别为：第一铜箔层20、第一钢板层28、接地层30、第二钢板层32及第二铜箔层26。过孔16内还设有多个焊盘（图未示），多个焊盘分别位于板体12的不同板层上，从而使得第一铜箔层20及第二铜箔层26通过过孔16内的焊盘与其他板层保持电性导通。

多个第一锡盘18位于第一钢板层28上，其贯穿并凸出于第一铜箔层20，多个第一锡盘18与第一钢板层28保持电性导通。接地层30与大地保持电性导通，其与第一钢板层28及第二钢板层32间为非电性导通。第二钢板层32上也设有均匀分布于通孔14周围的多个第二锡盘34

，多个第二锡盘34贯穿并凸出于第二铜箔层26，其与第二钢板层32保持电性导通。镀锡层22覆盖于第二铜箔层26及多个第二锡盘34上，防焊漆24涂覆于该第二铜箔层26上阻止镀锡层22的锡膏流入通孔14。可以理解，板体12的板层结构不限于本实施例中所列举的情形，只需在层与层之间建立导电通道即可。

请参见图5，下面对本发明较佳实施例的印刷电路板10抗电磁干扰的工作原理作详细说明。

印刷电路板10上还设有一个螺钉36，组装时，印刷电路板10通过螺钉36与电子装置的壳体38固定连接，螺钉36包括帽部362和杆部364，杆部364在远离帽部362的一端设有螺纹，螺钉36的杆部364穿过印刷电路板10的通孔14并螺合于壳体38上。螺钉36的帽部362与多个第一锡盘18相接触，印刷电路板10的镀锡层22与壳体38相接触。印刷电路板10的各板层与螺钉36保持电性导通。在本实施例中，因为多个第一锡盘18及镀锡层22被隔开的四个扇形区域均匀分布在通孔14的周围，所以印刷电路板10与螺钉36的帽部362间以及印刷电路板10与壳体38间均具有较佳且均匀分布的接触面，有利于将引起杂讯的电流导出。可以理解，依实际需要，印刷电路板10可与电子装置上任意的接地元件连接。

印刷电路板10上引起杂讯的电流流向大地的路径有多种，比如一条路径为螺钉36的帽部362(第一锡盘18(第一钢板层28(螺钉36的杆部364(接地层30(大地，此路径的阻抗较低，电流优先从该路径流向大地；另一条路径为螺钉36的帽部362(第一锡盘18(第一钢板层28(螺钉36的杆部364(壳体38(大地。在本实施例中，第一铜箔层20及第二铜箔层26通过过孔16内的焊盘与其他板层保持电性导通，印刷电路板10的各板层与螺钉36保持电性导通，同时印刷电路板10的镀锡层22与壳体38保持电性导通，因此，电流的流经路径不限于以上列举的两种，这样在印刷电路板10与大地间建立了多个电流通道，从而能有效地将印刷电路板10上引起杂讯的电流导向大地，降低电磁干扰。

在本实施例中，通孔14的周围于镀锡层22与通孔14之间设有防焊漆24，而不用采用贴胶带的方式将通孔14封住，印刷电路板10经过锡炉时，由于防焊漆24的隔阻，镀锡层22的锡膏不会流入通孔14中，在通孔14周围涂覆防焊锡操作简单，可有效缩短加工时间，从而降低了生产成本。此外，因为防焊漆24将镀锡层22隔开为四个均匀分布于通孔14周围的区域，印刷电路板10与电子装置的壳体38固定连接后，镀锡层22与壳体38接触使得印刷电路板10与壳体38间具有较好的接触面，有利于将印刷电路板10上引起杂讯的电流导向大地，从而达到抗电磁干扰的目的。

另外，本领域技术人员还可在本发明精神内做其它变化，当然，这些依据本发明精神所

做的变化，都应包含在本发明所要求保护的范围内。

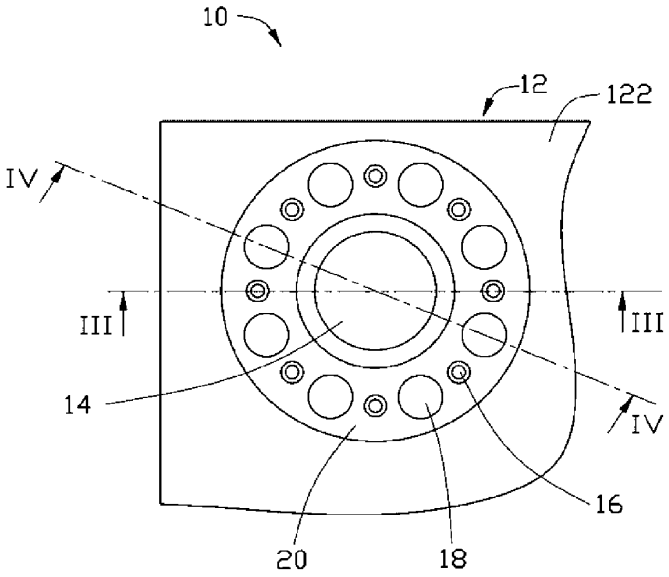


图 1

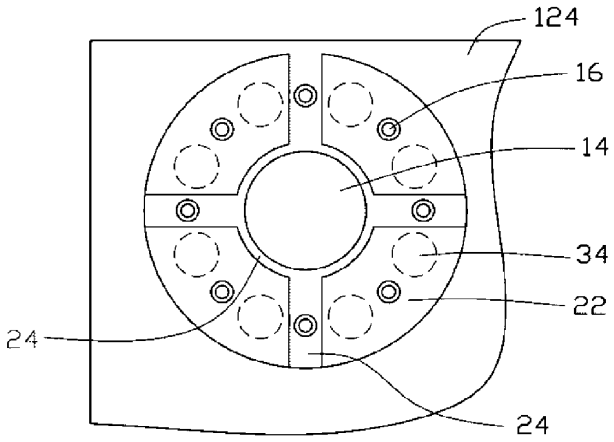


图 2

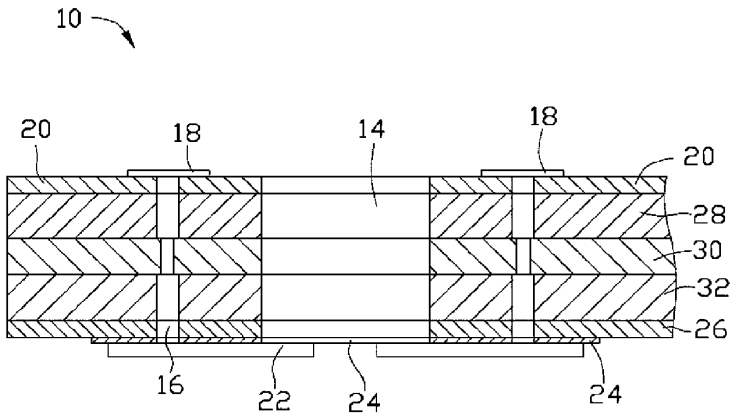


图 3

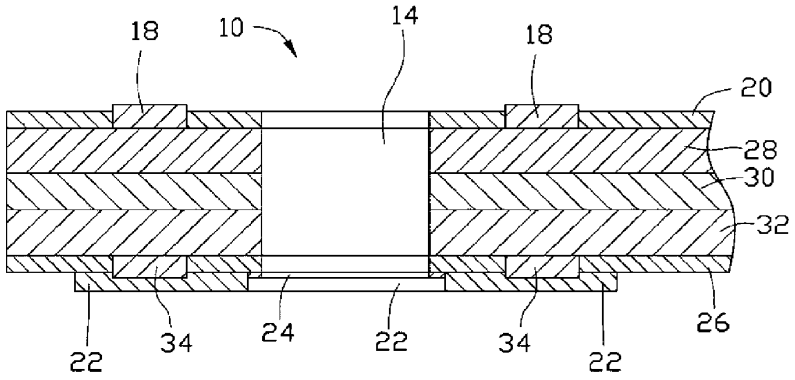


图 4

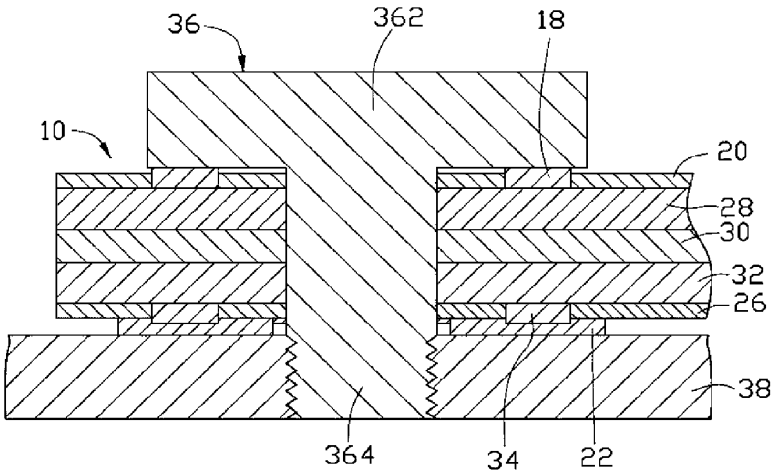


图 5

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Inventor: LIU SHUZI ;
Inventor[std]: SHUZI LIU ;
International class[8]: H05K1/02; H05K1/11; H05K9/00;
Cooperative Patent class: H05K3/0094 ; H05K1/0215 ; H05K1/05 ; H05K1/116 ; H05K3/3452 ; H05K3/3484 ; H05K2201/099 ; H05K2201/09909 ; H05K2201/10409 ; H05K2203/043 ;
Family members: CN101600293 A CN101600293 B US2009301768 AA US8077472 BB
Title: Printing circuit board
Title: 印刷电路板

Abstract:

The invention discloses a printing circuit board comprising a board body. A through hole is drilled on the board body, and the printing circuit board is fixedly connected with an earthing element via the through hole. The surface of the printing circuit board is provided with a tin coating around the through hole. The tin coating is in contact with the earthing element, and the printing circuit board is in electrical conduction with the earthing element. The board body includes a first copper foil layer, a first steel plate layer, an earthing layer, a second steel plate layer and a second copper foil layer in turn. The first steel plate layer is provided with a plurality of tin plates which cross and protrude the first copper foil layer. The second steel plate is provided with a plurality of second tin plates which cross and protrude the second copper foil layer. The tin coating covers the second copper foil layer and the plurality of tin plates. The periphery of the through hole is provided with solder mask preventing the tin cream of the tin coating from flowing into the

through hole. The printing circuit board of the invention has the advantages of short processing time, low cost and anti-electromagnetic interference.

Abstract:

一种印刷电路板，其包括一个板体，板体上开设有一个通孔，印刷电路板通过通孔与接地元件固定连接。该印刷电路板的表面于通孔的周围设有一个镀锡层，镀锡层与接地元件接触且印刷电路板与接地元件保持电性导通。板体依次包括第一铜箔层、第一钢板层、接地层、第二钢板层及第二铜箔层。第一钢板层上设有多个第一锡盘，多个第一锡盘贯穿并凸出于第一铜箔层。第二钢板层上设有多个第二锡盘，多个第二锡盘贯穿并凸出于第二铜箔层，镀锡层覆盖第二铜箔层及多个第二锡盘。通孔的周围设有用于阻止该镀锡层的锡膏流入该通孔的防焊漆。本发明印刷电路板具有加工时间短、成本低及抗电磁干扰的优点。

A printed circuit board including a board member, the board body set up with a through-hole printed circuit board by means of through-hole and the ground element fixedly connected. The surface of the printed circuit board around the through hole is provided with a tin layer, tin plating layer in contact with the ground element and the printed circuit board and the ground element holding electrically conductive. The plate member includes a first copper foil layer successively, a first plate layer, a ground layer, a second steel layer and the second copper foil layer. A plurality of first layer of tin plate on the first plate, a plurality of first through tin plate and projecting from the first copper layer. The second layer has a plurality of second plate tin plate, a plurality of second tin plate and projecting through the second copper foil layer, tinned copper layer covering the second layer and a plurality of second tin plate. It is provided around the through-hole solder paste used to prevent the tin layer through-hole solder flows into the paint. The present invention is a printed circuit board having a short processing time, low cost, and anti-electromagnetic interference advantages.

Claims:

1. 一种印刷电路板，其包括一个板体，该板体上开设有一个通孔，该印刷电路板通过该通孔与接地元件固定连接，该印刷电路板的表面于该通孔的周围设有一个镀锡层，该镀锡层与该接地元件接触且该印刷电路板与该接地元件保持电性导通，其特征在于：该板体依次包括一个第一铜箔层、一个第一钢板层、一个接地层、一个

1. A printed circuit board, which comprises a plate, the opening of the plate member has a through hole, the printed circuit board through the through hole is fixedly connected with the ground element, the surface of the printed circuit board at the periphery of the through hole is provided with a tin layer, the tin plating

第二钢板层及一个第二铜箔层，该第一钢板层上设有多个第一锡盘，该多个第一锡盘贯穿并凸出于该第一铜箔层，该第二钢板层上设有多个第二锡盘，该多个第二锡盘贯穿并凸出于该第二铜箔层，该镀锡层覆盖该第二铜箔层及该多个第二锡盘，该通孔的周围设有用于阻止该镀锡层的锡膏流入该通孔的防焊漆。

2.如权利要求1所述的印刷电路板，其特征在于：该镀锡层由该防焊漆隔开为均匀分布于通孔周围的四个扇形区域。

3.如权利要求1所述的印刷电路板，其特征在于：该印刷电路板上还设有一个螺钉，该螺钉穿过该印刷电路板的通孔并螺合于接地元件上。

4.如权利要求3所述的印刷电路板，其特征在于：该螺钉的帽部与该多个锡盘接触并与接地层保持电性导通。

5.如权利要求1所述的印刷电路板，其特征在于：该防焊漆涂覆于该第二铜箔层上。

6.如权利要求5所述的印刷电路板，其特征在于：该印刷电路板上还开设有多个过孔， 该第一铜箔层及该第二铜箔层通过过孔内的焊盘与其他板层保持电性导通。

layer in contact with the ground element and the printed circuit board to maintain the electrically conductive ground member, characterized in that: the plate body in turn comprises a first copper foil layer, a first steel layer, a ground layer, a second steel layer and a second layer of copper, which has a plurality of first layer of tin plate on the first plate, tin plate through the plurality of first and projecting from the first copper layer, a plurality of second tin plate steel on the second floor, the plurality of second tin plate and protrude through the second copper foil layer, the tin layer covering the the second copper foil layer and the plurality of second tin plate, is provided around the through-hole solder paste used to prevent the tin layer through-hole solder flows into the paint.

.

2 as claimed in any one of the printed circuit board, characterized in that: the tin plating layer made of the solder resist lacquer spaced evenly distributed in the four quadrants of the area around the through-hole.

.

3 claim 1, wherein the printed circuit board, characterized in that: the printed circuit board also has a screw, the screw through the through-hole printed circuit board and screwed to the grounding element.

.

4 claim 3, wherein the printed circuit board, characterized in that: the screw cap portion in contact with the plurality of tin plate and keep the ground layer is electrically conductive.

.

5 according to claim 1 wherein the printed circuit board, characterized in that: the solder resist lacquer is coated on the second copper foil layer.

.

6 Claim 5, wherein the printed circuit board, characterized in that: the printed circuit board has a plurality of through holes opened, the first and the second copper foil layer copper layer is formed by a pad over the hole to keep electrical conduction with the other board layers.

Description:

印刷电路板

PCB

技术领域

FIELD

[0001] 本发明涉及一种印刷电路板。 背景技术

[0001] The present invention relates to a printed circuit board. BACKGROUND

[0002] 印刷电路板在电子行业中有着广泛的应用，印刷电路板在使用时，由于电子组件间的干扰，往往会由干扰电流产生大量宽频噪声或杂讯，严重影响印刷电路板的功能，一般称这种现象为电磁干扰（Electro Magnetic Interference;EMI)。

[0002] printed circuit boards in the electronics industry has a wide range of applications, the printed circuit board is in use, due to the interference between electronic components, tends to produce a lot of noise from the broadband noise or interference current, seriously affecting the printed circuit board function, generally referred to this phenomenon as electromagnetic interference (Electro Magnetic Interference; EMI).

Current

[0003] 为了降低印刷电路板在使用过程中的电磁干扰，通常需要将引起电磁干扰的电流导向大地。一般情况下，会在印刷电路板上开设一个通孔，将一个螺钉穿过通孔并螺合于一个与大地保持电性导通的壳体上，以便于将印刷电路板上的干扰电流通过螺钉及壳体导向大地。通孔的周围在印刷电路板的表面上一般设有一个镀铜层，印刷电路板上的电流流向大地时会经过该镀铜层，镀铜层容易被空气氧化而不利于将印刷电路板上的电流导出。因此，通常会在通孔周围镀铜层上涂覆一层锡膏，然后经过锡炉使锡膏更好地附着于镀铜层上，然而经过锡炉时，锡膏容易流入通孔而产生封孔问题。现有技术中为防止封孔问题的产生，在印刷电路经过锡炉前，先用贴胶带的方式将通孔封住，然

[0003] In order to reduce the printed circuit board in the course of electromagnetic interference, usually caused by electromagnetic interference needs to guide the earth. Under normal circumstances, it will open a through hole in the printed circuit board, a screw through the through holes and screwed into the earth on a holding electrically conductive housing, in order to interfere with the current printed circuit board

而，贴胶带极为浪费时间，通常需要增加人力，从而增加了生产成本。

发明内容

[0004] 鉴于上述状况，有必要提供一种加工时间短且成本较低的印刷电路板。

[0005] 一种印刷电路板，其包括一个板体，该板体上开设有一个通孔，该印刷电路板通过该通孔与接地元件固定连接。该印刷电路板的表面于通孔的周围设有一个镀锡层，镀锡层与接地元件接触且印刷电路板与接地元件保持电性导通。板体依次包括一个第一铜箔层、 一个第一钢板层、一个接地层、一个第二钢板层及一个第二铜箔层。第一钢板层上设有多个第一锡盘，多个第一锡盘贯穿并凸出于第一铜箔层。第二钢板层上设有多个第二锡盘，多个第二锡盘贯穿并凸出于第二铜箔层，镀锡层覆盖第二铜箔层及多个第二锡盘。通孔的周围设有用于阻止该镀锡层的锡膏流入该通孔的防焊漆。

[0006] 与现有技术相比，印刷电路板的通孔周围设有防焊锡，印刷电路板经过锡炉时，防焊漆可阻止镀锡层的锡膏流入印刷电路板的通孔中，防止了封孔问题的产生。在通孔周围涂覆防焊锡操作简单，可有效缩短加工时间，从而降低了生产成本。

附图说明

[0007] 图1是本发明较佳实施例的印刷电路板的局部俯视图。

[0008] 图2是本发明较佳实施例的印刷电路板的局部仰视图。

[0009] 图3是图1所示的印刷电路板沿III-III线的局部剖视图。

[0010] 图4是图1所示的印刷电路板沿IV-IV线的局部剖视图。

[0011] 图5是图1所示的印刷电路板与电子装置的壳体固定连接后的局部示意图。具体实施方式

through screw and guide housing earth. Around the through hole on the surface of the printed circuit board generally has a copper layer, printed circuit board when the current flows through the copper layer of the earth will, copper plating layer is easily oxidized by air to the detriment of the printed circuit board Current export. Therefore, usually around the through-hole plating layer is coated with a paste, and then after the solder has better furnace attached to the copper layer, but after furnace, the solder easily flows into the through-hole and produce Sealing problems. The prior art is to prevent plugging problems in the printed circuit through tin stove, first with the taping of the way through holes sealed, however, taping extremely waste of time, usually we need to increase manpower, thereby increasing the cost of production.

Summary

[0004] In view of the above circumstances, it is necessary to provide a short processing time and low cost of the printed circuit board.

[0005] A printed wiring board, which comprises a plate, the opening of the plate member has a through hole, the printed circuit board with a through hole through which the ground element is fixedly connected. The surface of the printed circuit board around the through hole is provided with a tin layer, tin plating layer in contact with the ground element and the printed circuit board and the ground element holding electrically conductive. Plate successively comprises a first copper layer, a layer of a first plate, a ground layer, a second steel layer, and a second copper foil layer. A plurality of first layer of tin plate on the first plate, a plurality of first through tin plate and projecting from the first copper layer. The second layer has a plurality of second plate tin plate, a plurality of second tin

[0012] 下面将结合附图及较佳实施例对本发明的印刷电路板作进一步的详细说明。

[0013] 请参见图1与图2，本发明较佳实施例的印刷电路板10包括一个板体12以及开设于板体12上的圆形通孔14与多个过孔16，多个过孔16均匀分布于的通孔14周围。印刷电路板10可通过通孔14与电子装置的接地元件固定连接，而使印刷电路板10与大地保持电性导通。

[0014] 板体12包括一个第一表面122及一个与第一表面122相对的第二表面124。通孔 14的周围于板体12的第一表面122上设有多个第一锡盘18及一个第一铜箔层20，多个第一锡盘18均匀分布于通孔14的周围。多个第一锡盘18与多个过孔16相互交错地均匀分布于通孔14的周围。板体12的第二表面IM于通孔14的附近涂覆有一个镀锡层22，通孔 14的周围于通孔14与镀锡层22之间设有防焊漆M (Solder mask or Solder Resist)，且镀锡层22由防焊漆对隔开为四个均匀分布于通孔14周围的扇形区域，而阻止镀锡层22的锡膏流入通孔14中。防焊漆M-般称为〃绿漆〃，为便于肉眼对印刷电路板10的检查， 在主漆中多加入对眼睛有帮助的绿色颜料，防焊漆M除了为绿色之外还可为黄色、白色、 黑色或其它颜色。防焊漆M可阻止锡膏流过防焊漆M所在的区域。

[0015] 可以理解，通孔14的周围设有防焊漆24，且镀锡层22由防焊漆M隔开为四个区域，这样当印刷电路板经过锡炉时，防焊漆M可有效阻止镀锡层22的锡膏流入通孔14，从而避免了封孔问题的产生。镀锡层22还可被防焊漆M隔开为两个、三个或四个以上的区域，镀锡层22也可不被隔开，而仅在镀锡层22与通孔14之间设有防焊漆M。通孔14不限于圆形，还可为方形或其他形状。

[0016] 请一并参见图3与图4，印刷电路板10的板体12由多个板层组成。板体12各板层从第一表面122到第二表面124的顺序分别为：第一铜箔层20、第一钢板层观、接地层 30、第二钢板层32及第二铜箔层沈。过孔16内还设有多个焊盘（图未示），多个焊盘分别位于板体12的不同板层上，从而使得第一铜箔层20及第二铜箔

plate and projecting through the second copper foil layer, tinned copper layer covering the second layer and a plurality of second tin plate. It is provided around the through-hole solder paste used to prevent the tin layer through-hole solder flows into the paint.

[0006] Compared with the prior art, the through-hole printed circuit board around with anti-solder, printed circuit board passes through the furnace, paint can prevent tin plating solder paste flow into the printed circuit board through hole, preventing the generation of sealing problem. Simple prevention around the through-hole solder coating operation, can effectively shorten the processing time, thereby reducing production costs.

Brief Description

[0007] FIG. 1 is a partial top plan view of a printed circuit board of the preferred embodiment of the present invention.

[0008] FIG. 2 is a partial bottom view of a preferred embodiment of a printed circuit board of the present invention.

[0009] FIG. 3 is a partial cross-sectional view of the printed circuit board shown in FIG. 1 along the line III-III.

[0010] FIG. 4 is a partial cross-sectional view of the printed circuit board shown in FIG. 1 along the line IV-IV.

[0011] FIG. 5 is a partial schematic view of the printed circuit board shown in FIG. 1 and the electronic device housing fixedly connected after. DETAILED DESCRIPTION

[0012] in conjunction with the accompanying drawings and the following preferred embodiments of the printed circuit board of the present invention will be described in further detail.

层沈通过过孔16内的焊盘与其他板层保持电性导通。

[0017] 多个第一锡盘18位于第一钢板层观上，其贯穿并凸出于第一铜箔层20，多个第一锡盘18与第一钢板层观保持电性导通。接地层30与大地保持电性导通，其与第一钢板层 28及第二钢板层32间为非电性导通。第二钢板层32上也设有均匀分布于通孔14周围的多个第二锡盘34，多个第二锡盘34贯穿并凸出于第二铜箔层沈，其与第二钢板层32保持电性导通。镀锡层22覆盖于第二铜箔层沈及多个第二锡盘34上，防焊漆M涂覆于该第二铜箔层沈上阻止镀锡层22的锡膏流入通孔14。可以理解，板体12的板层结构不限于本实施例中所列举的情形，只需在层与层之间建立导电通道即可。

[0018] 请参见图5，下面对本发明较佳实施例的印刷电路板10抗电磁干扰的工作原理作详细说明。

[0019] 印刷电路板10上还设有一个螺钉36，组装时，印刷电路板10通过螺钉36与电子装置的壳体38固定连接，螺钉36包括帽部362和杆部364，杆部364在远离帽部362的一端设有螺纹，螺钉36的杆部364穿过印刷电路板10的通孔14并螺合于壳体38上。螺钉 36的帽部362与多个第一锡盘18相接触，印刷电路板10的镀锡层22与壳体38相接触。印刷电路板10的各板层与螺钉36保持电性导通。在本实施例中，因为多个第一锡盘18及镀锡层22被隔开的四个扇形区域均匀分布在通孔14的周围，所以印刷电路板10与螺钉36 的帽部362间以及印刷电路板10与壳体38间均具有较佳且均匀分布的接触面，有利于将引起杂讯的电流导出。可以理解，依实际需要，印刷电路板10可与电子装置上任意的接地元件连接。

[0020] 印刷电路板10上引起杂讯的电流流向大地的路径有多种，比如一条路径为螺钉 36的帽部362 -第一锡盘18 -第一钢板层28 -螺钉36的杆部364 -接地层30 -大地，此路径的阻抗较低，电流优先从该路径流向大地；另一条路径为螺钉36的帽部362 -第一锡盘18 -第一钢板层28 -螺钉36的杆部364 -壳体38 -大地。在本实施例中，第

[0013] See Figure 1 and Figure 2, the preferred embodiment of the printed circuit board 10 includes a body 12 and a plate 14 with a plurality of through holes on the circular through hole 12 opened in the plate member 16 of the present invention, a plurality of through holes 14 around the through hole 16 in a uniformly distributed. 10 may be fixedly connected to the printed circuit board 14 through the through hole and the ground element of the electronic device, leaving the printed circuit board 10 remains electrically conductive and earth.

[0014] a first plate member 12 includes a first surface 122 and a second surface 122 opposing surface 124. Surrounding the through hole 14 in the plate around the first plurality of tin plate 18 and a first copper layer 20, a first plurality of evenly distributed in the tin plate 18 through hole 14 of the 12 on the first surface 122 is provided. A plurality of first tin plate 18 with a plurality of through holes 16 evenly distributed around the staggered manner in the through-hole 14. The second surface 12 of the IM-coated plate in the vicinity of the through hole 14 has a tin plating layer 22, around the through hole 14 in the through hole 14 is provided between the tin layer 22 and the solder resist lacquer M (Solder mask or Solder Resist), and paint tin solder layer 22 is comprised of four spaced evenly distributed around the through-hole 14 of the fan-shaped area, and prevent 14 tin solder layer 22 flows into the through-hole. Solder masking paint M- ? ? as called for ease of visually checking the printed circuit board 10, the main paint added more helpful eyes green pigment, Solder Mask M in addition to green outside but also for yellow, white, black or other colors. Solder Mask M can prevent the flow area through the solder paste paint M is located.

一铜箔层20及第二铜箔层沈通过过孔16内的焊盘与其他板层保持电性导通，印刷电路板10的各板层与螺钉36保持电性导通，同时印刷电路板10的镀锡层22与壳体38保持电性导通， 因此，电流的流经路径不限于以上列举的两种，这样在印刷电路板10与大地间建立了多个电流通道，从而能有效地将印刷电路板10上引起杂讯的电流导向大地，降低电磁干扰。

[0021] 在本实施例中，通孔14的周围于镀锡层22与通孔14之间设有防焊漆M，而不用采用贴胶带的方式将通孔14封住，印刷电路板10经过锡炉时，由于防焊漆M的隔阻，镀锡层22的锡膏不会流入通孔14中，在通孔14周围涂覆防焊锡操作简单，可有效缩短加工时间，从而降低了生产成本。此外，因为防焊漆对将镀锡层22隔开为四个均匀分布于通孔14 周围的区域，印刷电路板10与电子装置的壳体38固定连接后，镀锡层22与壳体38接触使得印刷电路板10与壳体38间具有较好的接触面，有利于将印刷电路板10上引起杂讯的电流导向大地，从而达到抗电磁干扰的目的。

[0022] 另外，本领域技术人员还可在本发明精神内做其它变化，当然，这些依据本发明精神所做的变化，都应包含在本发明所要求保护的范围内。

[0015] It will be appreciated around the through hole 14 is provided with solder lacquer 24, and the tin layer 22 is made of solder paint M separated into four regions, so that when the printed circuit board passes through the furnace, solder M paint tin plating layer can effectively prevent the paste 22 flows into the through hole 14, thus avoiding plugging problems. Tin solder resist lacquer layer 22 may also be separated M is two, three or four or more regions, 22 tinned layer may not be separated, but only between the tin plating layer 22 is provided with a through hole 14 There Solder Mask M. Through hole 14 is not limited to a circular, square or other shapes may also be.

[0016] Please refer to FIG. 3 in conjunction with FIG. 4, the plate member 12 of the printed circuit board 10 by a plurality of sheet layers. Each plate layer board member 12 from the first surface 122 to the second surface 124 of the order are: first copper layer 20, the first steel layer concept, the ground layer 30, a second steel layer 32 and the second copper foil layer Shen. The through-hole 16 is also provided with a plurality of pads (not shown), a plurality of pads are located on different lamellar plate 12, so that the first layer 20 and the second copper foil layer through vias sink pad 16 is kept electrically conductive with the other board layers.

[0017] a plurality of first tin plate 18 is located on the first steel layer concept, which runs through and projecting from the first copper layer 20, a plurality of first tin plate 18 remains electrically with the first steel layer concept conduction. Ground layer 30 remains electrically conductive and the earth, with the first steel layer 28 and the second plate layer 32 is non-electrically conductive. The second steel layer 32 also has a plurality of through holes uniformly distributed

around the 14 second tin plate 34, a plurality of second tin plate 34 and protrude through the second copper foil layer sink with a second steel layer 32 remains electrically conductive. Tin layer 22 covering the copper layer on the second sink and a plurality of second tin plate 34, the solder paste paint M coating prevents tin layer 22 flows into the through hole 14 on the second layer of heavy foil. It will be appreciated lamellar plate structure 12 is not limited to the present embodiment in the case exemplified embodiment, can simply establish a conductive path between the layers.

[0018] Refer to Figure 5, the working principle of the present invention, the following example of a printed circuit board 10 against electromagnetic interference preferred embodiment described in detail.

[0019] on the printed circuit board 10 is also provided with a screw 36, when assembled, the printed circuit board 10 is fixedly connected with the electronic device 36 of the housing 38 by screws, screw 36 includes a cap portion 362 and the rod 364, the lever portion 364 at an end remote from the cap portion 362 is provided with threads 364 of the screw shaft portion 36 through the through hole 14 of the printed circuit board 10 and is screwed to the housing 38. 36 screw cap portion 362 with a plurality of first contact 18 tin plate, tin plating layer 22 in contact with the printed circuit board 10 of the housing 38. Each plate layer printed circuit board 10 with the screw 36 to maintain electrical conduction. In the present embodiment, since the plate 18 and a plurality of first solder 22 are spaced four fan-shaped area in the tin plating layer uniformly distributed around the through hole 14, so that between the screw 10 and the printed circuit board 36 and the cap portion 362 printed circuit

board 10 and the housing 38 have a better and uniform distribution of the contact surface is conducive to export the current noise of the cause. It is appreciated that, according to the actual needs, the printed circuit board 10 may be connected to any ground element on the electronic device.

Current flow path of the earth

[0020] 10 cause noise on the printed circuit board are many, such a path is a screw cap 362 36 - the first tin plate 18 - the first steel layer 28 - 36 screws lever unit 364 - Ground floor 30-- earth, low impedance path, current flows from the path priority land; the other path is a screw cap 36 362 - First tin plate 18 - the first steel layer 28 - 36 screws The rod portion 364-- housing 38 - Mother Earth. In the present embodiment, the first copper foil layer 20 and the second copper foil layer through pad sink through the retaining hole 16 of each lamellar electrically conductive screw, the printed circuit board 10 and the other plate layer 36 electrically of conduction, while tin plating layer 22 of the printed circuit board 10 holding the housing 38 electrically conductive, and therefore, the two current flow path is not limited to the above exemplified, so that between the printed circuit board 10 and ground to establish a a plurality of current paths, which can effectively guide the current noise caused by the land 10 of printed circuit boards, to reduce electromagnetic interference.

[0021] In the present embodiment, the through-hole in the tin layer 22 is provided around the through hole 14 between 14 and solder paint M, instead of using the taping manner through hole 14 sealed, printing circuit board 10 passes furnace, since the solder paste paint M deadening, tin layer 22 does not flow into the through hole 14, the

through-hole 14 anti-solder coating around simple, can effectively shorten the processing time, thereby reducing production costs. Further, since the solder resist lacquer 10 is fixedly connected after the tin plating layer 22 are separated into four evenly distributed around the through-hole region 14, a printed circuit board and the electronic device housing 38, the housing 22 and the tin plating layer 38 makes contact with the printed circuit board 10 and the housing 38 has a better contact surface, facilitates the cause noise on the current guide land 10 of the printed circuit board, so as to achieve the purpose of anti-electromagnetic interference.

[0022] In addition, the skilled staff can do other variations within the spirit of the present invention, of course, vary depending on the spirit of the present invention made these should be included within the protection scope of the invention as claimed.

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审查员 刘乐

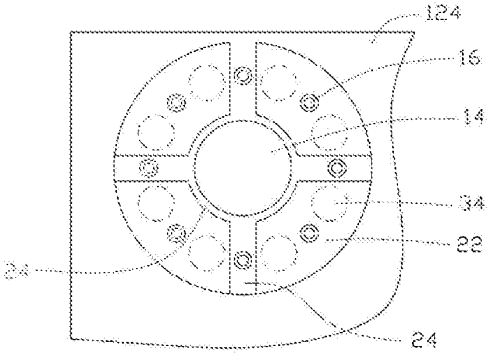
权利要求书 1 页 说明书 3 页 附图 3 页

(54)发明名称

印刷电路板

(57)摘要

一种印刷电路板，其包括一个板体，板体上开设有一个通孔，印刷电路板通过通孔与接地元件固定连接。该印刷电路板的表面于通孔的周围设有一个镀锡层，镀锡层与接地元件接触且印刷电路板与接地元件保持电性导通。板体依次包括第一铜箔层、第一钢板层、接地层、第二钢板层及第二铜箔层。第一钢板层上设有多个第一锡盘，多个第一锡盘贯穿并凸出于第一铜箔层。第二钢板层上设有多个第二锡盘，多个第二锡盘贯穿并凸出于第二铜箔层，镀锡层覆盖第二铜箔层及多个第二锡盘。通孔的周围设有用于阻止该镀锡层的锡膏流入该通孔的防焊漆。本发明印刷电路板具有加工时间短、成本低及抗电磁干扰的优点。



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1. 一种印刷电路板，其包括一个板体，该板体上开设有一个通孔，该印刷电路板通过该通孔与接地元件固定连接，该印刷电路板的表面于该通孔的周围设有一个镀锡层，该镀锡层与该接地元件接触且该印刷电路板与该接地元件保持电性导通，其特征在于：该板体依次包括一个第一铜箔层、一个第一钢板层、一个接地层、一个第二钢板层及一个第二铜箔层，该第一钢板层上设有多个第一锡盘，该多个第一锡盘贯穿并凸出于该第一铜箔层，该第二钢板层上设有多个第二锡盘，该多个第二锡盘贯穿并凸出于该第二铜箔层，该镀锡层覆盖该第二铜箔层及该多个第二锡盘，该通孔的周围设有用于阻止该镀锡层的锡膏流入该通孔的防焊漆。

2. 如权利要求 1 所述的印刷电路板，其特征在于：该镀锡层由该防焊漆隔开为均匀分布于通孔周围的四个扇形区域。

3. 如权利要求 1 所述的印刷电路板，其特征在于：该印刷电路板上还设有一个螺钉，该螺钉穿过该印刷电路板的通孔并螺合于接地元件上。

4. 如权利要求 3 所述的印刷电路板，其特征在于：该螺钉的帽部与该多个锡盘接触并与接地层保持电性导通。

5. 如权利要求 1 所述的印刷电路板，其特征在于：该防焊漆涂覆于该第二铜箔层上。

6. 如权利要求 5 所述的印刷电路板，其特征在于：该印刷电路板上还开设有多个过孔，该第一铜箔层及该第二铜箔层通过过孔内的焊盘与其他板层保持电性导通。

印刷电路板

技术领域

[0001] 本发明涉及一种印刷电路板。

背景技术

[0002] 印刷电路板在电子行业中有着广泛的应用，印刷电路板在使用时，由于电子组件间的干扰，往往会由干扰电流产生大量宽频噪声或杂讯，严重影响印刷电路板的功能，一般称这种现象为电磁干扰 (Electro Magnetic Interference ;EMI)。

[0003] 为了降低印刷电路板在使用过程中的电磁干扰，通常需要将引起电磁干扰的电流导向大地。一般情况下，会在印刷电路板上开设一个通孔，将一个螺钉穿过通孔并螺合于一个与大地保持电性导通的壳体上，以便于将印刷电路板上的干扰电流通过螺钉及壳体导向大地。通孔的周围在印刷电路板的表面上一般设有一个镀铜层，印刷电路板上的电流流向大地时会经过该镀铜层，镀铜层容易被空气氧化而不利于将印刷电路板上的电流导出。因此，通常会在通孔周围镀铜层上涂覆一层锡膏，然后经过锡炉使锡膏更好地附着于镀铜层上，然而经过锡炉时，锡膏容易流入通孔而产生封孔问题。现有技术中为防止封孔问题的产生，在印刷电路经过锡炉前，先用贴胶带的方式将通孔封住，然而，贴胶带极为浪费时间，通常需要增加人力，从而增加了生产成本。

发明内容

[0004] 鉴于上述状况，有必要提供一种加工时间短且成本较低的印刷电路板。

[0005] 一种印刷电路板，其包括一个板体，该板体上开设有一个通孔，该印刷电路板通过该通孔与接地元件固定连接。该印刷电路板的表面于通孔的周围设有一个镀锡层，镀锡层与接地元件接触且印刷电路板与接地元件保持电性导通。板体依次包括一个第一铜箔层、一个第一钢板层、一个接地层、一个第二钢板层及一个第二铜箔层。第一钢板层上设有多个第一锡盘，多个第一锡盘贯穿并凸出于第一铜箔层。第二钢板层上设有多个第二锡盘，多个第二锡盘贯穿并凸出于第二铜箔层，镀锡层覆盖第二铜箔层及多个第二锡盘。通孔的周围设有用于阻止该镀锡层的锡膏流入该通孔的防焊漆。

[0006] 与现有技术相比，印刷电路板的通孔周围设有防焊锡，印刷电路板经过锡炉时，防焊漆可阻止镀锡层的锡膏流入印刷电路板的通孔中，防止了封孔问题的产生。在通孔周围涂覆防焊锡操作简单，可有效缩短加工时间，从而降低了生产成本。

附图说明

[0007] 图 1 是本发明较佳实施例的印刷电路板的局部俯视图。

[0008] 图 2 是本发明较佳实施例的印刷电路板的局部仰视图。

[0009] 图 3 是图 1 所示的印刷电路板沿 III-III 线的局部剖视图。

[0010] 图 4 是图 1 所示的印刷电路板沿 IV-IV 线的局部剖视图。

[0011] 图 5 是图 1 所示的印刷电路板与电子装置的壳体固定连接后的局部示意图。

具体实施方式

[0012] 下面将结合附图及较佳实施例对本发明的印刷电路板作进一步的详细说明。

[0013] 请参见图 1 与图 2，本发明较佳实施例的印刷电路板 10 包括一个板体 12 以及开设于板体 12 上的圆形通孔 14 与多个过孔 16，多个过孔 16 均匀分布于的通孔 14 周围。印刷电路板 10 可通过通孔 14 与电子装置的接地元件固定连接，而使印刷电路板 10 与大地保持电性导通。

[0014] 板体 12 包括一个第一表面 122 及一个与第一表面 122 相对的第二表面 124。通孔 14 的周围于板体 12 的第一表面 122 上设有多个第一锡盘 18 及一个第一铜箔层 20，多个第一锡盘 18 均匀分布于通孔 14 的周围。多个第一锡盘 18 与多个过孔 16 相互交错地均匀分布于通孔 14 的周围。板体 12 的第二表面 124 于通孔 14 的附近涂覆有一个镀锡层 22，通孔 14 的周围于通孔 14 与镀锡层 22 之间设有防焊漆 24(Solder mask or Solder Resist)，且镀锡层 22 由防焊漆 24 隔开为四个均匀分布于通孔 14 周围的扇形区域，而阻止镀锡层 22 的锡膏流入通孔 14 中。防焊漆 24 一般称为″绿漆″，为便于肉眼对印刷电路板 10 的检查，在主漆中多加入对眼睛有帮助的绿色颜料，防焊漆 24 除了为绿色之外还可为黄色、白色、黑色或其它颜色。防焊漆 24 可阻止锡膏流过防焊漆 24 所在的区域。

[0015] 可以理解，通孔 14 的周围设有防焊漆 24，且镀锡层 22 由防焊漆 24 隔开为四个区域，这样当印刷电路板经过锡炉时，防焊漆 24 可有效阻止镀锡层 22 的锡膏流入通孔 14，从而避免了封孔问题的产生。镀锡层 22 还可被防焊漆 24 隔开为两个、三个或四个以上的区域，镀锡层 22 也可不被隔开，而仅在镀锡层 22 与通孔 14 之间设有防焊漆 24。通孔 14 不限于圆形，还可为方形或其他形状。

[0016] 请一并参见图 3 与图 4，印刷电路板 10 的板体 12 由多个板层组成。板体 12 各板层从第一表面 122 到第二表面 124 的顺序分别为：第一铜箔层 20、第一钢板层 28、接地层 30、第二钢板层 32 及第二铜箔层 26。过孔 16 内还设有多个焊盘（图未示），多个焊盘分别位于板体 12 的不同板层上，从而使得第一铜箔层 20 及第二铜箔层 26 通过过孔 16 内的焊盘与其他板层保持电性导通。

[0017] 多个第一锡盘 18 位于第一钢板层 28 上，其贯穿并凸出于第一铜箔层 20，多个第一锡盘 18 与第一钢板层 28 保持电性导通。接地层 30 与大地保持电性导通，其与第一钢板层 28 及第二钢板层 32 间为非电性导通。第二钢板层 32 上也设有均匀分布于通孔 14 周围的多个第二锡盘 34，多个第二锡盘 34 贯穿并凸出于第二铜箔层 26，其与第二钢板层 32 保持电性导通。镀锡层 22 覆盖于第二铜箔层 26 及多个第二锡盘 34 上，防焊漆 24 涂覆于该第二铜箔层 26 上阻止镀锡层 22 的锡膏流入通孔 14。可以理解，板体 12 的板层结构不限于本实施例中所列举的情形，只需在层与层之间建立导电通道即可。

[0018] 请参见图 5，下面对本发明较佳实施例的印刷电路板 10 抗电磁干扰的工作原理作详细说明。

[0019] 印刷电路板 10 上还设有一个螺钉 36，组装时，印刷电路板 10 通过螺钉 36 与电子装置的壳体 38 固定连接，螺钉 36 包括帽部 362 和杆部 364，杆部 364 在远离帽部 362 的一端设有螺纹，螺钉 36 的杆部 364 穿过印刷电路板 10 的通孔 14 并螺合于壳体 38 上。螺钉 36 的帽部 362 与多个第一锡盘 18 相接触，印刷电路板 10 的镀锡层 22 与壳体 38 相接触。

印刷电路板 10 的各板层与螺钉 36 保持电性导通。在本实施例中，因为多个第一锡盘 18 及镀锡层 22 被隔开的四个扇形区域均匀分布在通孔 14 的周围，所以印刷电路板 10 与螺钉 36 的帽部 362 间以及印刷电路板 10 与壳体 38 间均具有较佳且均匀分布的接触面，有利于将引起杂讯的电流导出。可以理解，依实际需要，印刷电路板 10 可与电子装置上任意的接地元件连接。

[0020] 印刷电路板 10 上引起杂讯的电流流向大地的路径有多种，比如一条路径为螺钉 36 的帽部 362 →第一锡盘 18 →第一钢板层 28 →螺钉 36 的杆部 364 →接地层 30 →大地，此路径的阻抗较低，电流优先从该路径流向大地；另一条路径为螺钉 36 的帽部 362 →第一锡盘 18 →第一钢板层 28 →螺钉 36 的杆部 364 →壳体 38 →大地。在本实施例中，第一铜箔层 20 及第二铜箔层 26 通过过孔 16 内的焊盘与其他板层保持电性导通，印刷电路板 10 的各板层与螺钉 36 保持电性导通，同时印刷电路板 10 的镀锡层 22 与壳体 38 保持电性导通，因此，电流的流经路径不限于以上列举的两种，这样在印刷电路板 10 与大地间建立了多个电流通道，从而能有效地将印刷电路板 10 上引起杂讯的电流导向大地，降低电磁干扰。

[0021] 在本实施例中，通孔 14 的周围于镀锡层 22 与通孔 14 之间设有防焊漆 24，而不用采用贴胶带的方式将通孔 14 封住，印刷电路板 10 经过锡炉时，由于防焊漆 24 的隔阻，镀锡层 22 的锡膏不会流入通孔 14 中，在通孔 14 周围涂覆防焊锡操作简单，可有效缩短加工时间，从而降低了生产成本。此外，因为防焊漆 24 将镀锡层 22 隔开为四个均匀分布于通孔 14 周围的区域，印刷电路板 10 与电子装置的壳体 38 固定连接后，镀锡层 22 与壳体 38 接触使得印刷电路板 10 与壳体 38 间具有较好的接触面，有利于将印刷电路板 10 上引起杂讯的电流导向大地，从而达到抗电磁干扰的目的。

[0022] 另外，本领域技术人员还可在本发明精神内做其它变化，当然，这些依据本发明精神所做的变化，都应包含在本发明所要求保护的范围内。

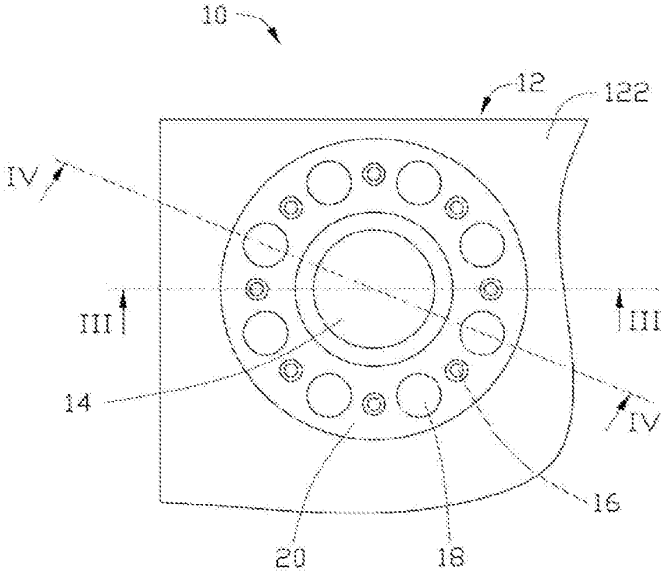

图 1

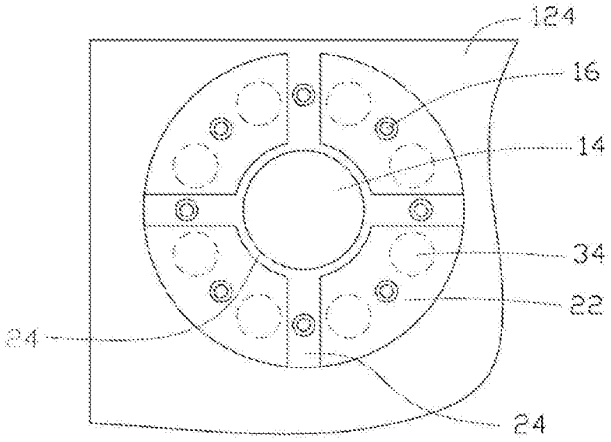

图 2

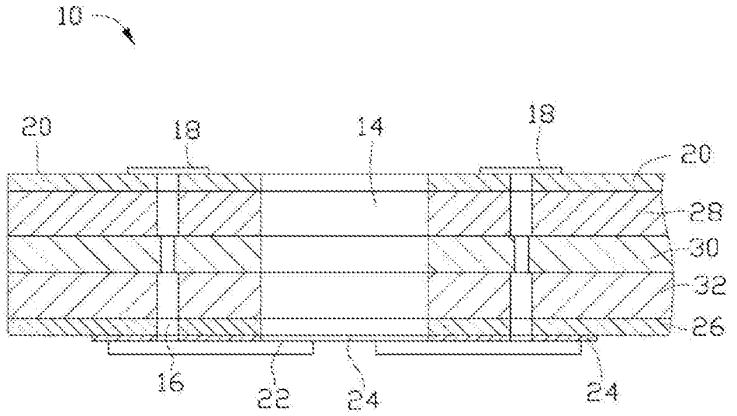

图 3

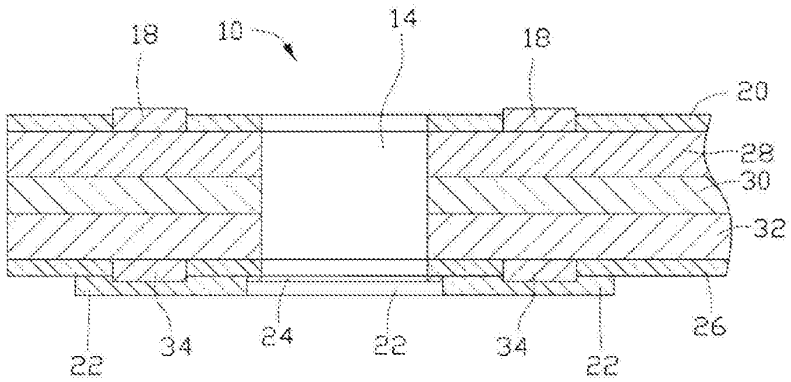

图 4

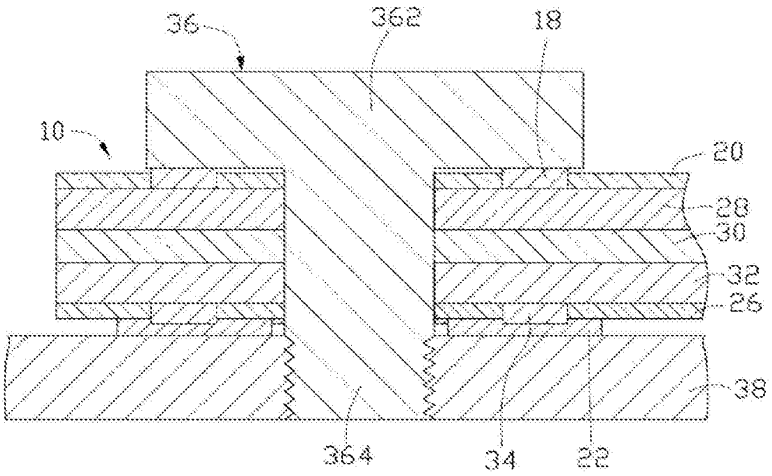

图 5

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Assignee[std]: MOLEX INC ;
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Title: HIGH-DATE RATE CONNECTOR SYSTEM AND CIRCUIT BOARD THEREOF

Title: 高数据速率连接器系统及其电路板

Abstract:

The utility model provides a high-date rate connector system which comprises a connector and a circuit board component, wherein the component comprises a terminal arranged in the connector, and the terminal is arranged in a through hole on the circuit board. Therefore, a signal and a grounding terminal are coupled to a signal path wire and an earth wire layer on the circuit board. In order to help to improve the electric performance of a joint between the terminal in the connector and the signal path wire on the circuit board, the other pin through holes which are aligned at grounding through hole can be arranged on the circuit board. A signal ring leads the signal path wire to be separated from each other, a wire is distributed around the two different sides of the through hole before the signal path wire is jointed again, the close electric vicinity is kept at the

same time, and the electric coupling which is relatively continuous is arranged between the pair of path wires.

Abstract:

高数据速率连接器系统，其包括连接器和电路板组件，该组件包括位于连接器内的端子，端子被安装到电路板上的通孔中。信号和接地端子由此耦接至电路板上的信号迹线和地线层。为了帮助改善连接器内的端子和电路板上的信号迹线之间的接口处的电性能，可以在电路板上设置与接地通孔对齐的其它引脚通孔。信号环使信号迹线分开，并在重新接合前围绕通孔的两不同侧布线，同时保持亲密的电邻近，其在所述一对信号迹线的迹线之间提供相对持续的电耦合。

High data rate connector system comprising a connector and a circuit board assembly that includes a terminal, the terminal is located within the connector is mounted to the through holes in the circuit board. Whereby the signal and ground terminal coupled to the signal traces on the circuit board and the ground plane. To help improve the electrical properties of the interface signal traces on the circuit board terminals and connectors between the inside, you can set other pin through-hole ground vias aligned with the circuit board. Signal loop the signal traces separated and re-engaged around the through hole before two different sides of the wiring, while maintaining a close adjacent electricity, which provides a relatively constant electrical coupling between the pair of signal traces trace.

Description:

说明书 7/7 页 高数据速率连接器系统及其电路板 技术领域 [0001] 本实用新型涉及连接器技术领域，更特别地涉及一种适用于高频信号传递的连接 O 背景技术 [0002] 高速连接器是高性能数字系统中广泛应用的主要产品。一般说来，连接器将不同 的元件连接在一起，由此这些元件可以以高数据速率通讯。例如，现在10-15Gbps的数据速 率正被使用于和/或被设计用于系统中，并且未来的系统可期望向每数据通道17_25Gbps 发展。另外，连接器被制作得愈加紧凑，这使得提供较低数据速率具有挑战性，更不用说系 统可能从中获益且在将来被期望的较高数据速率。

Instructions 7/7 high data rate and circuit board connector system TECHNICAL FIELD

[0001] The utility model relates to the technical field of connectors, and more particularly to a high-frequency signal transmission is suitable for connection O BACKGROUND

[0002] The high-speed connectors are the main products of high-performance digital systems widely used. In general, different connector elements are connected together, whereby these elements can be at a high data rate

[0003] 连接器可被配置成提供需要的性能水平，同时连接器作为通常包括电路板（例如 PCB)的通讯系统的一部分。因此，对于安装于电路板上的元件而言，可能的通信路径可能包 括将触头上的信号插入第一电路板上的第一组迹线。第一电路板上的第一组迹线从所述元 件延伸至连接器的触头，通过该第一连接器延伸至第二匹配连接器，然后延伸至第二电路 板上的迹线，进而至第二元件上。已经确定的是，在欲提供高数据速率的系统中存在的一个 重要问题是电路板和连接器之间的接口。因为通常有两个这种接口，所以这个问题对系统 的整体性能具有实质影响。因此，连接器和电路板接口的改进是值得重视的。

实用新型内容 [0004] 为了解决上述问题，本实用新型提供一种高数据速率连接器系统，包括： [0005] 连接器，其包括具有安装表面和配合表面的壳体，所述壳体被配置成支撑多个端 子，所述多个端子分别包括通孔尾部、对接部以及在通孔尾部和配合部之间延伸的主体 部，所述多个端子包括第一信号对和第二信号对以及至少一个接地端子，第一和第二信号 对分别从所述安装表面延伸到所述配合表面，并被配置成在所述安装表面和配合表面之间 提供差分信号路径，所述至少一个接地端子布置在第一和第二信号对之间，从而将第一信号对与第二对端子电屏蔽开；以及 [0006] 电路板，其包括顶层、具有地线层的接地层以及信号层，所述电路板包括与所述第一信号对的尾部耦接的第一对信号通孔以及与所述第二信号对的尾部耦接的第二对信号 通孔，所述信号通孔中的每一个耦接到信号层上的迹线并与地线层隔离，所述电路板还包 括从顶层延伸到接地层并延伸穿过信号层的接地通孔，所述接地通孔耦接至所述至少一个 接地端子的尾部，并进一步耦接至所述地线层， [0007] 所述电路板还包括从顶层延伸穿过信号层并耦接到所述地线层的引脚通孔，所述 引脚通孔邻近所述接地通孔布置，其中在所述接地通孔和所述引脚通孔之间所画虚线位于 第一和第二对信号通孔之间。

communications. For example, the data rate 10-15Gbps now is being used in and / or designed for the system, and future systems can be expected to each data channel 17_25Gbps development. Further, the connector must be made even more compact, which provides a lower data rate such that challenging, not to mention the system and in the future may benefit from a higher data rate is desired.

[0003] the connector may be configured to provide the required level of performance, at the same time as part of the connector generally includes a circuit board (e.g. PCB) of the communication system. Thus, the element mounted on the circuit board, the possible communication paths may include the signal into the first set of contacts on the first circuit board trace. The first set of traces from the first circuit board to the connector element extends contacts, extending through the first connector to the second mating connector, then extending to the second circuit board traces, and then to the second element. It has been determined that an important issue to provide high data rates in the desire is present in the system interface circuit board and the connector between. Because usually there are two such interfaces, so this problem have a substantial impact on the overall performance of the system. Thus, the connector interface and improved circuit board is worthy of attention.

Utility Model Content

[0004] In order to solve the above problems, the present utility model provides a high data rate connector system, comprising:

[0005] The connector includes a mounting surface and the mating surface of the housing, said housing body is configured to support a plurality of

[0008] 进一步地，所述接地通孔和引脚通孔被配置成将信号层上的第一对信号通孔与第 二对信号通孔屏蔽开。

5 CN [0009] 进一步地，所述引脚通孔是第一引脚通孔，并且所述电路板还包括第二引脚通孔， 第一和第二引脚通孔被配置成第一和第二引脚通孔以及所述接地通孔的组合在所述信号 层上的第一对信号通孔和第二对信号通孔之间有效地形成屏蔽。

[0010] 进一步地，所述接地通孔位于第一和第二引脚通孔之间。

[0011] 进一步地，第一和第二引脚通孔被配置成使得在第一和第二引脚通孔之间延伸的 虚线与所述接地通孔相交。

[0012] 进一步地，第一和第二引脚通孔在直径上小于所述接地通孔。

[0013] 进一步地，第一引脚通孔在直径上小于所述接地通孔。

[0014] 进一步地，所述连接器被配置为以大于15Gbps的数据速率运行。

[0015] 根据本实用新型的另一个方面，本实用新型提供一种电路板，包括： [0016] 顶层； [0017] 接地层； [0018] 信号层，其位于所述顶层和所述接地层之间； [0019] 第一对信号通孔，其从所述顶层延伸至所述接地层，并耦接至所述信号层上的第 一对信号迹线，第一对信号通孔与所述接地层电隔离，且每个信号通孔被配置成接收端子 尾部； [0020] 第二对信号通孔，其从所述顶层延伸至所述接地层，并耦接至所述信号层上的第 二对信号迹线，第二对信号通孔与所述接地层电隔离，且每个信号通孔被配置成接收端子 尾部； [0021] 第一接地通孔，其在所述顶层和所述接地层之间延伸，并电耦接至所述接地层，所 述接地通孔被配置成接收端子尾部；以及 [0022] 引脚通孔，其邻近所述接地通孔布置，并在所述顶层和所述接地层之间延伸，并且 电耦接至所述接地层，其特征在于，在运行中，所述引脚通孔未被配置成接收端子尾部，以 及介于所述引脚通孔和所述接地通孔之间的虚线位于第一和第二对信号通孔之间。

terminals, said plurality of terminals respectively include a through hole tail, and the butt portion between the body portion and the through-hole tail portion extending mating, said plurality of terminals comprising a first and a second signal signal and at least one ground terminal, the first and second signals, respectively, extending from the mounting surface to the mating surface, and configured to provide a differential signal path between the mounting surface and the mating surface of said at least a ground terminal disposed between the first and second signals, so that the first signal and the second pair of terminals electrically shielded; and

[0006] circuit board, which comprises a top layer, a ground layer having a ground plane, and signal layer, said circuit board comprises a first pair of signal vias and the tail of the first signal and the second pair of coupled signal via said second signal coupled to the tail, the signal via Each layer is coupled to the signal trace and the ground plane on the isolation, the circuit board further comprises a layer extending from the top to the ground and ground vias extending through the signal layers, the grounding vias coupled to the at least one rear ground terminal and further coupled to the ground plane,

[0007] The circuit board also includes extending through the signal from the top layer and coupled to the pin through the ground plane hole, the pin through-hole vias disposed adjacent the ground, where the ground between the through hole and the pin through holes dotted line drawn between the first and second pairs of signal vias.

[0008] Further, the ground vias and pin through-hole is configured to signal via a first signal layer and the second pair of signal via shielded ?.

5 CN

[0023] 进一步地，所述引脚通孔为布置在所述接地通孔的第一侧上的第一引脚通孔，所 述电路板进一步包括位于所述接地通孔的第二侧上的第二引脚通孔，所述第一和第二引脚 通孔设置成与所述接地通孔结合以在第一和第二对信号通孔之间形成有效的屏蔽。

[0024] 进一步地，第二引脚通孔被布置成使得在第一引脚通孔和第二引脚通孔之间的虚 线与所述接地通孔相交。

[0025] 进一步地，所述接地通孔具有第一直径，所述引脚通孔具有第二直径，第二直径小 于第一直径。

[0026] 进一步地，所述接地通孔和信号通孔具有大致相同的直径。

[0027] 进一步地，第一对信号迹线布置成使得每个信号迹线围绕所述接地通孔和所述引 脚通孔中的一个的相对两侧延伸，所述电路板进一步包括信号环，所述信号环围绕所述接 地通孔和所述引脚通孔中的一个延伸，并与所述接地通孔和引脚通孔中的一个电隔离。

[0028] 根据本实用新型的又一个方面，本实用新型提供一种电路板，包括： [0029] 顶层； [0030] 接地层，该接地层包括地线层； [0031] 信号层，其位于所述顶层和所述接地层之间； 6 CN [0032] 一对信号通孔，其从所述顶层延伸至所述接地层，并耦接至所述信号层上的一对 信号迹线，该对信号通孔与所述接地层电隔离，且每个通孔被配置成接收端子尾部； [0033] 其特征在于，所述电路板还包括： [0034] 通孔，其在所述顶层和所述接地层之间延伸，并电耦接至所述地线层； [0035] 信号环，其围绕所述通孔延伸，且位于所述信号层上，所述信号环不与所述通孔直 接电连通，其中该对信号迹线的每个信号迹线围绕所述信号环的相对两侧延伸。

[0036] 进一步地，所述通孔为被配置成接收端子尾部的接地通孔和被配置为不接收端子 尾部的引脚通孔中的一个。

[0037] 进一步地，该对信号线中的迹线被配置成通过使用所述信号环将两迹线耦合

[0009] Further, the pin through-hole is the first pin through-hole, and the circuit board further comprises a second pin through-hole, the first and second pin through hole is configured a combination of the first and second pin through hole and through hole in the ground on the signal layer formed between the first pair of effective signal vias and a second pair of signal via shielded.

[0010] Further, the ground vias between the first and second pin through holes.

[0011] Further, the first and second pin through-holes are arranged so that a dotted line between the first and second pin through hole extending through holes intersect with the ground.

[0012] Further, the first and second pin through hole smaller in diameter than the ground vias.

[0013] Further, the first pin through hole smaller in diameter than the ground vias.

[0014] Further, the connector is configured to operate at data rates greater than 15Gbps.

[0015] According to another aspect of the utility model, the utility model provides a circuit board comprising:

[0016] the top;

[0017] The ground layer;

[0018] a signal layer, which is located in the top and the between said ground layer;

[0019] a first pair of signal through holes extending from the top floor to the ground floor, and is coupled to the first pair of signal traces on the signal layer, a first pair of signal through hole and said ground plane is electrically isolated, and

在一 起来在运行时保持较近的电耦合，所述信号环用于在沿围绕所述通孔的路径上的多个点处 降低两信号迹线之间的有效电隔离。

[0038] 进一步地，该电路板包括在所述顶层和所述接地层之间延伸的第一引脚通孔，该 第一引脚通孔与一接地通孔相邻设置，其中在所述接地通孔与第一引脚通孔之间所画虚线 位于所述一对信号通孔的一侧。

[0039] 进一步地，该电路板包括与接地通孔相邻设置的第二引脚通孔，第一和第二引脚 通孔位于接地通孔的相对两侧上。

[0040] 电路板包括两对信号通孔和位于该两对信号通孔之间的接地通孔。所述信号通孔 与电路板的信号层上的迹线耦接。接地通孔与电路板的地线层耦接。所述接地通孔和信号 通孔都被配置成接收安装到电路板上的连接器的端子尾部。一个或多个引脚通孔（pinning via)可以与接地通孔相邻设置，并且也与所述地线层耦接，但不接收所述连接器的端子尾 部。所述接地通孔和一个或多个引脚通孔结合，用来帮助提供电屏蔽，从而帮助防止两对信 号通孔之间的串扰。

[0041] 在一个实施例中，连接器可以安装到电路板上，使得所述成对的信号端子尾部布 置在信号通孔内，接地端子尾部布置在接地通孔内。电路板和连接器的组合可以提供彼此 屏蔽的成对的信号通道，并且引脚通孔可以提供延伸穿过所述尾部和信号迹线之间的接口 的屏蔽。

[0042] 在一个实施例中，信号迹线可以从两个信号通孔布置在电路板上，使得信号迹线 以差分的方式耦合。信号可以围绕通孔的相对侧延伸，该通孔可以为接地通孔，并且信号环 (signal collar)可用于帮助将信号迹线之间的任何电隔离最小化，该电隔离可能是由于 两信号迹线之间的通孔引起的物理隔离的增加而造成的。

附图说明 [0043] 本实用新型借助于实例进行说明，但不限于所附附图，在所附附图中，相同的附图 标记表示类似的元件，其

each signal via being configured to receive a terminal tail;

[0020] the second pair of signal vias extending from said top layer to said ground plane, and coupled to the a second pair of signal traces on the signal layer, a second pair of signal vias and the ground layer is electrically isolated, and each signal via the terminal is configured to receive the tail;

[0021] The first ground vias, which in the extending between said top layer and the ground layer and electrically coupled to said ground plane, said ground vias is configured to receive a terminal tail; and

[0022] the through-hole pins, which are arranged adjacent to the ground vias and between the top layer and the ground layer extends, and electrically coupled to said ground layer, characterized in that, in operation, the pin is not a through hole configured to receive a terminal tails, as well as between dashed through the pin hole and the ground through holes located between the first and second pairs of signal vias.

[0023] Further, the pin through-hole of the first pin through holes are arranged on a first side of the ground through holes of the circuit board further comprises the ground via a first second pin through hole on the second side, said first and second pin through holes arranged in conjunction with the ground through holes in between the first and second pairs of signal vias formed an effective shield.

[0024] Further, the second pin through-holes are arranged such that the first pin in dashed through hole and the second pin through holes intersect the ground vias.

[0025] Further, the grounding through holes having a first diameter, said pin through hole having a second diameter,

中： [0044] 图1示出了连接器和电路板组件的一个实施例的透视图。

[0045] 图Ia示出了连接器和电路板组件的另一个实施例的透视图。

[0046] 图2示出了图1中描述的组件的局部透视图。

[0047] 图3示出了连接器端子和电路板之间的接口的一个实施例的透视图。

[0048] 图4示出了图3中描述的接口的简化透视图。

7 CN [0049] 图5示出了电路板的一个实施例的俯视图。

[0050] 图6示出了电路板的另一实施例的俯视图。

[0051] 图7示出了图5中描述的实施例的其它特征。

[0052] 图8示出了图6中描述的实施例的其它特征。

[0053] 图9示出了电路板的可选实施例的俯视图。

[0054] 图10示出了包括多个层的电路板的实施例的透视图。

[0055] 图11示出了图10中描述的实施例的透视图，其中省略了多个层。

[0056] 图12示出了图11中描述的实施例的俯视图。

[0057] 图13示出了轨迹结构的实施例的俯视图。

具体实施方式 [0058] 本申请要求于2009年3月25日提交的美国临时申请号为61/163，315的申请的 优先权，在此以引用的方式整体并入本文中。

[0059] 下面的详细说明描述了示例性实施例，但并不是限于明确公开的组合。因此，除非 另有说明，这里公开的特征可以

the second diameter smaller than the first diameter.

[0026] Further, the ground vias and signal vias having substantially the same diameter.

[0027] Further, the first pair of signal traces are arranged such that each of the signal traces extending around opposite sides of the grounding through holes and the pins of one of the through holes, the circuit board further including the signal loop, the signal ring around the ground through hole and the pin through hole extending, and with the ground via and pin through hole in one of the electrical isolation.

[0028] According to the present utility model to yet another aspect, the present utility model provides a circuit board comprising:

[0029] the top;

[0030] the ground floor, the ground floor comprises a ground plane;

[0031] signal layer which is located between the top layer and the ground layer; 6 CN

[0032] a pair of signal through holes extending from the top floor to the ground floor, and is coupled to a signal on the signal layer traces, the signal through hole and the ground plane is electrically isolated, and each through-hole is configured to receive a terminal tail;

[0033] wherein said circuit board further comprises:

[0034] a through hole, in which extending between the top layer and the ground layer and electrically coupled to the ground plane;

被组合在一起构成其它组合，这些组合出于简洁的目的而 未另外示出。

[0060] 将连接器耦接至电路板（例如印刷电路板）的系统有时使用已知的通孔结构。特 别地，连接器内的端子包括尾部，这些尾部被配置为插入到电路板上的通孔内，然后被焊接 在适当的位置。这些通孔由此将连接器内的端子耦接到电路板上的信号迹线。这种系统提 供了良好的机械性能，并且允许宽范围的连接器都能够被电路板支撑。虽然存在许多连接 器设计，但是电路板的接口往往比较类似。一般来说，某些通孔用于传输信号（通常以差分信号的结构），并用于将电路板上的信号迹线耦接至连接器的信号端子。其它通孔用于将连 接器的接地端子耦接至地线层（例如电路板的接地层）。众所周知，一个设计差的连接器会 把信号端子上的信号噪声引入其它电相邻的信号端子。可能较少被重视的是连接器和电路 板之间的接口对整个系统的影响。

[0061] 图1示出了连接器和电路板组件10的实施例，为了说明目的，连接器20部分未进 行组装。可以看出，端子触头31位于安装表面24内（所示安装表面为卡槽结构），并且部 分端子延伸到电路板50，如所示，薄片状针座22用于在所希望的方向上支撑多个端子。可 以看出，这些针座彼此毗邻设置。因此，不仅在连接器内，而且在连接器20和电路板50之 间的接口内都需要注意信号。

[0062] 图IA示出了组件的另一实施例，其包括通过连接器组件210、211连接在一起的电 路板250、251、252。可以看出，虽然电路板251上的一些通孔可以被电路板251的两侧上 的端子使用（例如，它们是共用通孔），但是有些通孔并不共用，因此电路板251上（有时 被称为中间面）的信号迹线需要布线到其它通孔。可以看出，基于中间面的组件，例如图 IA所示，可以包括多个类似的连接器组件，且位于中间面一侧上的一个连接器组件的一些 端子可以通过使用迹线被布线到位于中间面另一侧上的不同的连接器组件。因此，中间面 设计可以提供重要的灵活性。然而，对于比较简单的设计而言，连接器组件可

[0035] Signal ring which extends around the through hole, and is located on said signal layer, said signal ring not with direct electrical communication with said through hole, wherein the signal trace for each signal trace around opposite sides of the ring signal extends

[0036] Further, the through-hole is configured to receive a terminal tail of ground vias, and is configured to receive the pin through holes in the rear of a terminal.

[0037] Further, the pair of signal lines trace is configured to use the signal loop of two traces are coupled together to keep the electrically coupled close at runtime, the signal loop for at various points along the path around the through-hole to reduce the effective electrical isolation between the two signal traces.

[0038] Further, the circuit board includes a first pin through hole between the top layer and the ground layer extending to the first pin and a through hole disposed adjacent ground vias, wherein in the The painting above ground vias between the first pin through hole on one side of the dotted line of a signal via said.

[0039] Further, the circuit board includes a second pin through-hole ground vias disposed adjacent the first and second pins through holes located on opposite sides of the grounding through holes.

[0040] The circuit board includes two pairs of signal vias and ground vias located between the signal via the two pairs. The trace signal layer signal vias on the circuit board is coupled. Ground vias of the circuit board ground plane coupling. The ground vias and signal vias are configured to receive terminal tail attached to the connector on the circuit board. One or more pins through holes (pinning via) may be provided adjacent to the through hole and the ground, and is

以将两个电路 板（或电缆和电路板）耦接在一起。一般来说，连接器可以包括图1中示出的安装表面和 配合表面，尽管配合表面和安装表面可能会有许多变化。

8 CN [0063] 图2示出了图1中描述的连接器组件10的特征。可以看出，端子30包括信号端 子34和接地端子33a、33b。每个端子具有接触部30a、尾部30b和在它们之间延伸的主体 部30c。在一个实施例中，两个信号端子34将被配置作为一个信号对，并在操作中耦合在 一起以提供一个差分信号路径。接地端子，例如接地端子33b将帮助相互屏蔽位于连接器 10主体内的两个不同的差分信号对。在一个实施例中，如所示，接地端子可以宽于信号端子，以帮助在作为差分信号对的端子对之间提供更大的屏蔽。可以看出，一般地，将接地端 子设置在两个不同的信号端子对之间有助于降低信号对之间的串扰，并且有助于信号对在 较高的频率下运行以达到所希望的噪声水平（因此允许有更高的数据速率）。例如，因为 针座允许信号端子之间的可控宽边耦合，并且桥接件25 (其可以由任意合适的导电材料制 成，且具有任意适当的形状）被间隔开以帮助确保接地端子33所提供的接地结构在所关 心的频率上基本无谐振，图2所示连接器可配置成在大于IOGHz的奈奎斯特频率（Nyquist frequency)下运行。因此，这种连接器可以考虑被配置为在大于16Gps的数据速率下运行， 并且甚至在大于20Gps的数据速率下运行。

[0064] 如所示，连接器10包括共用结构和有用的电气间隔，该共用结构将接地端子耦接 在一起。虽然共用结构可以采用多种形式且并非必需的，但是对于更高速的运行而言，已 经确定的是这种接地的共用对于降低电谐振是有益的，否则电谐振将会向信号中引入不希 望的噪声。对于许多连接器而言，当奈奎斯特频率接近或者超过8GHz时，这种共用的性价 比利益也更加有益，然而更大的连接器甚至在较低的奈奎斯特频率下也受益于这种共用结 构。

[0065] 图3和4示出了连接器内的端子和电路板上的通孔之间的接口。接地通孔52配置成收容接地或屏蔽端子33a、33b的尾

also coupled to the ground plane, but does not receive the connector terminal tail. The ground vias, and one or more pins through holes combine to help provide electrical shielding to help prevent crosstalk between two pairs of signal vias of.

Signal terminal tail

[0041] In one embodiment, the connector may be mounted to a circuit board, such that the pair of through holes arranged in the signal, the ground terminal tail is arranged in the grounding through holes. A combination of circuit board and the connector shield can provide another pair of signal channels, and pin through-hole extending through the interface can provide the shield of the tail and signal traces between.

[0042] In one embodiment, signal traces from two signal vias disposed on a circuit board, so that the signal traces coupled to a differential manner. Signal may surround the opposite side of the through hole extends, the through hole vias may be grounded, and the ring signal (signal collar) may be used to assist any electrical isolation between the signal traces to minimize, the electrical isolation may be due to the two signal increase physical separation between the traces vias caused caused.

BRIEF DESCRIPTION

[0043] The present utility model will be described by way of example, but not limited to the accompanying drawings, in the accompanying drawings, the same reference numerals indicate similar elements and in which:

[0044] Figure 1 It shows a perspective view of a connector and a circuit board assembly embodiment.

A perspective view of a

部，而信号通孔54配置成收容信号端子34、35的尾 部。如所示，接地端子比信号端子更宽。如所示，一排信号对设置有介于信号对之间的接地 端子。在一个实施例中，信号对可以宽边耦合在连接器中，然后在尾部改变为边缘耦合，应 当注意，在一个实施例中边缘耦合可以使端子根据图5中所示布局排成一列，或者在一实 施例中根据图6中所示的布局偏移。因此，成对的信号通孔54可以沿着与针座的纵轴一致 的直线布置，或者它们可以沿着与针座的纵轴成一定角度的直线布置。虽然从性能的角度。

两者相当，但是信号端子沿着与纵轴一致的直线布置的好处是可以简化布线。相对于纵轴 成一定角度的优势是，针座内的端子在制造过程中不需要形成和前者一样多。

[0066] 可以进一步看出，设置有多个引脚通孔55，但是这些引脚通孔55并不收容端子的 尾部。引脚通孔的尺寸可以与其它通孔相似，或者它们可以比其它通孔更小，因为它们不用 收容端子尾部，并且小尺寸具有允许更加紧凑的接口的优点（并且潜在地降低接口内的阻 抗不连续，这种不连续可能是由于接口变得相对来说呈容性而引起的）。引脚通孔55与接 地通孔52相邻，并如所示位于接地通孔52的相对两侧。因此，从图4-9可以看出，引脚通 孔可以在电路板表面和接地层之间延伸的信号对之间有效地形成栅栏或屏蔽。

[0067] 可以看出，对于连接器结构，其中两个单独的针座分别提供构成所述信号对的端 子中的一个端子，该端子可以设置为许多结构。例如在图5中，信号端子形成一条直线，该 直线与针座对齐。在图6中，信号端子形成一条直线，该直线与针座成一定角度。在具有两 个引脚通孔的实施例中，连接两个引脚通孔的虚线可以与接地通孔相交（由此形成一直栅 栏结构）。应当注意，如果设置有两个引脚通孔，它们可以布置在相对两侧上（如图4-8所 9 CN 示），或者相同一侧上（接地通孔相对于信号通孔更偏斜）。中心结构的优点是存在于信号 端子和接地端子之间的共用模式可以更容易保持。不论信号通孔

[0045] Figure Ia shows a connector and a circuit board assembly to another embodiment.

[0046] FIG. 2 shows a partial perspective view of the assembly of Figure 1 is described.

[0047] FIG. 3 shows a perspective view of one embodiment of the interface connector terminal and the circuit board.

[0048] FIG. 4 shows a simplified perspective view of the interface 3 described in FIG.

7 CN

[0049] FIG. 5 shows a circuit board of an embodiment of a top view.

[0050] FIG. 6 shows a top view of another embodiment of a circuit board.

[0051] FIG. 7 shows a further embodiment of the feature described in FIG.

[0052] FIG. 8 shows a further embodiment of the feature described in FIG. 6.

[0053] Figure 9 shows an alternative plan view of a circuit board of the embodiment.

[0054] FIG. 10 shows an embodiment comprising a plurality of layers is a perspective view of a circuit board.

[0055] FIG. 11 shows a perspective view of the embodiment described in FIG. 10, in which a plurality of layers is omitted.

[0056] FIG. 12 shows a top view of the embodiment described in FIG. 11.

[0057] FIG. 13 shows a top view of the embodiment of the track structure.

DETAILED DESCRIPTION

的方位，由接地通孔和多 个引脚通孔构成的栅栏（或虚线）可以设置在信号通孔对之间。

[0068] 然而，从图9可以看出，也可以使用一个引脚通孔。这种结构允许电路板上有更紧 密的空间，因此可帮助在相对紧凑的连接器内提供良好的电绝缘。应当注意到，虽然所示两 个引脚通孔与一个接地通孔相关，但是也可以根据需要使用其他的引脚通孔（在实施中或 者将栅栏柱移动地更近，或者延长栅栏的长度）。大量的引脚通孔带来的一个问题是在信 号层上布置信号迹线变得更加困难。因此，对于某些应用而言，可以优选一个或两个引脚通孔，因为每个接地通孔具有三个或更多相关的引脚通孔将会使得以理想的方式布置信号迹 线变得基本上不可能。

[0069] 图10-12示出了电路板的一个实施例的特征。一般来说，多层电路板包括顶层82、 信号层81和接地层80 (其包括一地线层）。虽然图10中描述了其它层用于显示可以使用 多个层，但是总的层数通常为偶数，因为电路板通常具有偶数个层数以确保对称（由此将 扭曲的可能性降低到最小）。因此，虽然可以设置其它层，如果设置了接地层、信号层和顶 层，通常在电路板的相对侧设置至少三个与接地层、信号层和和顶层相同模式的其它层。应 当注意，虽然所示结构中顺序是顶层、信号层和接地层，但是接地层还可以布置在信号层和 顶层之间。假定电路板是普通的对称层设计，那么在接地层和顶层之间设置信号层的好处 是电路板的两半部分上的迹线可以彼此屏蔽。

[0070] 不管接地层和信号层的方位如何，信号通孔通常包括在接地层围绕它们的隔离 盘72 (如所示，用于每个信号端子的隔离盘是独立的正方形形状，其可以实现紧凑排列，但 是也可以设想其它构造，例如用于两个信号端子的单个隔离盘，或者一些其它形状的隔离 盘），如果信号通孔穿过隔离盘能够将信号通孔与接地层上的接地平面电隔离。从图11、12 中可以看出，信号迹线61、62由此设置在除接地层以外的不同平面内，并且均电耦合至信 号通孔。信号迹线通常布置成它们保持彼此

[0058] This application claims priority to U.S. Provisional Application No. 25 March 2009 filed priority 61 / 163,315 application, the manner herein by reference in their entirety herein.

[0059] The following detailed description of exemplary embodiments described, but is not limited to the specifically disclosed combinations. Therefore, unless otherwise indicated, the features disclosed herein may be combined together to form other combinations, these combinations the sake of brevity without additionally shows.

[0060] The connector is coupled to the circuit board (e.g. printed circuit board) using a known system sometimes via structure. In particular, the terminals within the connector comprises a tail, the tail is configured to be inserted into the through hole of the circuit board and then soldered in place. These vias thereby terminal coupled within the connector is connected to signal traces on the circuit board. This system provides a good mechanical properties, and allows a wide range of connector circuit boards can be supported. Although there are many connector design, but the board is often more similar interfaces. In general, some of the through holes for transmitting a signal (differential signal structure generally), and for the signal traces on the circuit board is coupled to the signal terminals of the connector. Other through-holes for the ground terminal of the connector is coupled to the ground plane (e.g., a circuit board ground plane). As we all know, signal noise will signal connector terminals on a poorly designed introduce other electrical adjacent signal terminals. Less likely to be seriously affecting the connector and circuit board interface for the entire system.

[0061] Figure 1 illustrates an embodiment of a connector and a circuit board

接近（以确保存在于两个差分信号传递之间的 差分模式的连续性）。

[0071] 在过去已经引起问题的事情是需要围绕通孔布线，例如延伸通过信号层的引脚通 孔或接地通孔。图13示出了一实施例，该实施例允许信号环163围绕通孔152延伸。信号 环163与通孔152电隔离，通孔152可以耦合到地线层，并且可以是接地或引脚通孔。信号 迹线161、162间隔开一距离164，该距离可以保持信号迹线路径，从而确保构成所述信号迹 线对的两迹线之间的相对持续的耦合。如所示，信号迹线161、162围绕通孔152的相对两 侧布线。通常所产生的电隔离将会对电特性具有显著的影响。然而，信号迹线之间的有效 电间隔被基本保持着，因为信号环163降低了信号迹线61、62之间的电隔离。因此，在剩余 的信号迹线路径上，信号迹线将电隔离设置成接近于距离165的两倍（相对接近于当信号 迹线间隔开距离164存在的电隔离）。因此，所示结构允许以一种方便的形式从端子尾部与 收容通孔之间的接口布置信号迹线，同时仍能实现紧凑的封脚。因此，这种结构在具有紧凑 间隔的同时还具有良好的电性能，尤其是在更高的信号频率时，例如大于IOGHz的奈奎斯 特频率。

[0072] 可以看出，本文描述的各种特征可以单独使用，也可以根据需要组合使用。因此， 电路板可以包括与一个或多个接地通孔相关联的一个或多个引脚通孔，和/或电路板可以 10 CN 包括一个或多个信号环以帮助改善电路板的布线性能。此外，连接器可以安装到包括一个 或多个上述特征的电路板上。

[0073] 根据优选和示范实施例已经描述了本实用新型。在理解本实用新型的基础上，本 领域的普通技术人员将会想到落入附属权利要求范围和精神内的许多其它的实施例、修改 和变化。

11 H . “"250 252 图IA CN 50 图 12 3!J 图 2 图3 1

assembly 10, for purposes of illustration, not part of the connector 20 is assembled. As can be seen, the terminal contact 31 is located in the inner mounting surface 24 (surface mounting slot structure shown), and the portion of the terminal extending into the circuit board 50, as shown, a sheet-shaped hub 22 is used in the desired direction supports a plurality of terminals. As can be seen, these hub adjacent to each other setting. Therefore, not only within the connector, and in the interface between the connector 50 and the circuit board 20 need to pay attention signal.

[0062] Figure IA shows another embodiment of the assembly, which includes a connector assembly 210, 211 is connected through the circuit board together 250,251,252. As can be seen, although the through holes on the circuit board 251 may be the terminal to use on the both sides of the circuit board 251 (e.g., through-holes are common), but some do not share the through hole, and therefore the circuit board 251 (sometimes are called intermediate surface) of the signal traces to be routed to the other through hole. As can be seen, based on the intermediate surface component, e.g., as shown in FIG. IA, may comprise a plurality of similar connector assembly, and is located a number of terminals of the connector assembly on the side of the intermediate surface by using a wiring traces are located Different intermediate connector assembly on the other side. Therefore, the intermediate surface design can provide important flexibility. However, for relatively simple designs, the connector assembly may be two circuit boards (or cables and circuit boards) are coupled together. Generally, the connector may comprise in Figure 1 and the mating surface of the surface mounting illustrated, although mating surface and

the mounting surface may have many variations.

8 CN

[0063] FIG. 2 shows a feature connector assembly depicted in Figure 1 10. As can be seen, the terminal 30 includes signal terminals 34 and ground terminals 33a, 33b. Each terminal has a contact portion 30a, 30b and the rear body portion 30c extending therebetween. In one embodiment, the two signal terminals 34 is configured as a signal and coupled together to provide a differential signal path in operation. Ground terminal, e.g., the ground terminal shield 33b will help each of two different differential signal pairs 10 located within the body of the connector. In one embodiment, as shown, the ground terminal can be wider than the signal terminals, to help as a differential signal between the terminals of the pairs provide greater shielding. As can be seen, in general, the ground terminal is provided between the two different signal terminals to help reduce cross-talk between signals and helps signals at a higher frequency operation to achieve the desired noise level (thus allowing for a higher data rate). For example, because the needle hub allows controlled broadside coupling between the signal terminals and the bridge piece 25 (which may be made of any suitable conductive material and have any suitable shape) are spaced apart to help ensure that the ground terminal 33 ground structure provided in the frequency of interest almost no resonance connector shown in Figure 2 can be configured to run in more than IOGHz Nyquist frequency (Nyquist frequency) lower. Thus, the connector can be configured to be considered greater than the data rate 16Gps run, and even greater than the data rate 20Gps the run.

[0064] As shown, the connector 10 includes a common structure and useful electrical interval, the common ground terminal structures coupled together. Although the common structure can take many forms and is not necessary, but for higher speed operation, it has been determined that such a common ground for reducing the electrical resonance is useful, otherwise the electrical resonance signals will be introduced to the undesirable noise. For many connectors, when the Nyquist frequency is close to or exceeds 8GHz, this cost-effective and more beneficial to the common interests, but even greater in the lower connector Nyquist frequency also benefit from this species common structure.

Interface

[0065] Figures 3 and 4 shows a through-hole terminals and circuit board within the connector between. Ground vias 52 arranged housing grounding or shielding terminals 33a, 33b of the tail, and the signal via the rear housing 54 is configured to signal terminals 34,35. As shown, the ground terminal is wider than the signal terminals. As shown, a row of signal ground terminal is provided between the signal pairs. In one embodiment, the signal can broadside coupling connector, then change to the edge at the end of the coupling, it should be noted that in one embodiment may be coupled to the edge of the terminal according to the layout shown in Figure 5 in a row, or In one embodiment, the offset according to the layout shown in Figure 6. Accordingly, the pair of signal vias 54 may be along the longitudinal axis of the needle holder consistent linear arrangement, or they may be arranged along a straight line with the longitudinal axis of the needle holder angled. Although from a performance perspective.

Both pretty, but the signal terminals along the longitudinal axis of the linear arrangement of the same benefits can be simplified wiring. With respect to the longitudinal axis of the angled advantage is that the terminal does not need to be formed within the needle hub and as much as the former in the manufacturing process.

[0066] can further be seen, the pin is provided with a plurality of through-holes 55, but these pins through holes 55 is not receiving terminal tail. Size pin through hole vias may be similar to other, or they may be smaller than the other through holes, as they are not receiving terminal tails, and a small size has the advantage to allow more compact interface (and potentially reduce the impedance of the interface within the discontinuous, this discontinuity may be due to the interface becomes relatively speaking was caused by capacitive). Pin through-hole 55 and the adjacent ground vias 52, and as shown on opposite sides of the ground through-hole 52. Thus, it can be seen from Figure 4-9, effectively formed between the pin through holes may be between the circuit board and the ground plane surfaces extending barrier or shield for the signal.

[0067] As can be seen, the connector structure in which two separate hub respectively constituting the signal terminals of a terminal, which can be set to many structures. For example, in FIG. 5, the signal terminal forming a straight line, the straight line is aligned with the needle hub. In Figure 6, the signal terminals are formed a straight line, the straight line and angled needle holder. In embodiments having two pins through holes connecting two pins through holes dotted line may intersect with the ground vias (thereby forming has been fences structure). It should be noted that if provided with two pins through holes,

they can be disposed on opposite sides (shown in Figure 4-8 9 CN), or on the same side (ground vias with respect to the signal via more skewed). Advantages of the central structure is present between the signal and ground terminals of the common mode can be more easily maintained. Regardless of the orientation signal via fence by the ground vias and a plurality of pins through holes formed (or dotted line) may be provided between the signal through-hole pair.

[0068] However, it can be seen from Figure 9, you can use a pin through hole. This structure allows a circuit board space more closely, it can help to provide good electrical insulation in a relatively compact connector. It should be noted that, although shown with a two-pin through-hole ground vias relevant, but you can use other pins through holes as needed (in the implementation of the fence posts or move closer to, or extend the length of the fence). One problem to bring a large number of through-holes of the pin arrangement of signal traces is more difficult on the signal layer. Thus, for some applications, it may be preferable to one or two pins through holes, since each ground vias having three or more pins through holes will be arranged in a manner such that an ideal signal traces change It was basically impossible.

[0069] Figure 10-12 shows features of an embodiment of a circuit board. In general, the top layer 82 comprises a multilayer circuit board, signal layers 81 and the ground layer 80 (which includes a ground plane). Although FIG. 10 describes other layers can be used for displaying a plurality of layers, but the total number of layers is even often, as the circuit board usually has an even number of layers to ensure symmetry (thereby reducing to a minimum the possibility of distortions). Therefore, although you can set other

layer, if you set the ground floor, and the top signal layer, usually opposite side of the circuit board at least three other layers and ground layers, and the top signal layer and in the same pattern. It should be noted that although the structure shown in the order is the top level, the signal layer and the ground layer, but the ground layer may also be disposed between the signal layer and the top layer. Assume the board is normal symmetrical layer design, then set the signal layer between the ground floor and the top benefit is trace the two halves of the circuit board can be shielded from each other.

[0070] regardless of the orientation of the ground layer and signal layers how the signal vias are typically included in the ground floor around their isolation plate 72 (as shown, each signal terminal isolation plate for an independent square shape, which can achieve a compact arrangement, but other configurations may be contemplated, for example, for the isolation of two signals single terminal plate, or some other shape isolation plate), if the signal via the signal can be passed through the partition plate through hole and the ground layer on the ground plane electrically isolated. As it can be seen from FIG. 11, 12, whereby the signal traces 61, 62 disposed in different planes other than the ground layer, and are electrically coupled to signal vias. Signal traces are usually arranged so that they remain close to each other (in order to ensure continuity exists between the two differential signal transmission in differential mode).

[0071] In the events of the past has caused problems around the through hole wiring is required, such as pins extending through the signal layer vias or ground vias. Figure 13 shows an embodiment, this embodiment allows the signal loop 163 extending around the

through hole 152. Signal loop 163 and the through hole 152 is electrically isolated from the through hole 152 may be coupled to the ground plane, and may be grounded or pin through hole.? signal traces 161, 162 spaced a distance 164, the distance between the signal trace path can be maintained, thereby ensuring a relatively constant coupling constituting the pair of signal traces between the two traces. As shown, the signal traces 161, 162 on opposite sides of the wiring around the through-hole 152. Galvanic isolation is typically generated will have a significant impact on the electrical characteristics. However, the effective electrical spacing between signal traces is substantially maintained, since the signal loop 163 to reduce the electrical isolation between the signal traces 61 and 62. Therefore, in the remainder of the signal trace path, the signal traces electrically isolated arranged close to twice the distance of 165 (as opposed to close when the signal traces 164 spaced apart from the presence of electrical isolation). Thus, the structure shown in a convenient form allows the interface layout from the signal traces and the receiving terminal tails between through-holes, while still achieving a compact closure foot. Therefore, this structure has a compact interval while also having good electrical properties, especially at higher signal frequencies, e.g., greater than IOGHz Nyquist frequency.

[0072] As can be seen, the various features described herein may be used alone, it can also be used in combination as required. Therefore, the circuit board may include one or more of a ground vias associated with a plurality of pins or vias, and / or circuit board 10 CN may include one or more signal ring to help improve the performance of the circuit board wiring. In addition, the connector may be mounted to include one or more of the features described above a circuit board.

[0073] According to a preferred and demonstration of the utility model has been described embodiment. In this new understanding on the basis of practical, one of ordinary skill in the art would expect the scope of the appended claims fall within a number of other embodiments, modifications and variations within the spirit and.

11 H. '"' 250 252 Figure IA CN 50 Figure 12 3! J Figure 2 Figure 3 1

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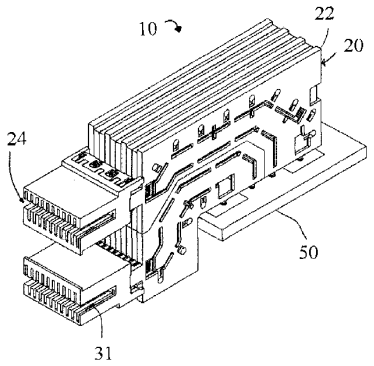
(54)实用新型名称

高数据速率连接器系统及其电路板

(57)摘要

高数据速率连接器系统，其包括连接器和电路板组件，该组件包括位于连接器内的端子，端子被安装到电路板上的通孔中。信号和接地端子由此耦接至电路板上的信号迹线和地线层。为了帮助改善连接器内的端子和电路板上的信号迹线之间的接口处的电性能，可以在电路板上设置与接地通孔对齐的其它引脚通孔。信号环使信号迹线分开，并在重新接合前围绕通孔的两不同侧布线，同时保持亲密的电邻近，其在所述一对信号迹线的迹线之间提供相对持续的电耦合。



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1. 一种高数据速率连接器系统，包括 ：

连接器，其包括具有安装表面和配合表面的壳体，所述壳体被配置成支撑多个端子，所述多个端子分别包括通孔尾部、对接部以及在通孔尾部和配合部之间延伸的主体部，所述多个端子包括第一信号对和第二信号对以及至少一个接地端子，第一和第二信号对分别从所述安装表面延伸到所述配合表面，并被配置成在所述安装表面和配合表面之间提供差分信号路径，所述至少一个接地端子布置在第一和第二信号对之间，从而将第一信号对与第二对端子电屏蔽开 ；以及

电路板，其包括顶层、具有地线层的接地层以及信号层，所述电路板包括与所述第一信号对的尾部耦接的第一对信号通孔以及与所述第二信号对的尾部耦接的第二对信号通孔，所述信号通孔中的每一个耦接到信号层上的迹线并与地线层隔离，所述电路板还包括从顶层延伸到接地层并延伸穿过信号层的接地通孔，所述接地通孔耦接至所述至少一个接地端子的尾部，并进一步耦接至所述地线层，

其特征在于，所述电路板还包括从顶层延伸穿过信号层并耦接到所述地线层的引脚通孔，所述引脚通孔邻近所述接地通孔布置，其中在所述接地通孔和所述引脚通孔之间所画虚线位于第一和第二对信号通孔之间。

2. 根据权利要求 1 所述的高数据速率连接器系统，其特征在于，所述接地通孔和引脚通孔被配置成将信号层上的第一对信号通孔与第二对信号通孔屏蔽开。

3. 根据权利要求 1 所述的高数据速率连接器系统，其特征在于，所述引脚通孔是第一引脚通孔，并且所述电路板还包括第二引脚通孔，第一和第二引脚通孔被配置成第一和第二引脚通孔以及所述接地通孔的组合在所述信号层上的第一对信号通孔和第二对信号通孔之间有效地形成屏蔽。

4. 根据权利要求 3 所述的高数据速率连接器系统，其特征在于，所述接地通孔位于第一和第二引脚通孔之间。

5. 根据权利要求 4 所述的高数据速率连接器系统，其特征在于，第 一和第二引脚通孔被配置成使得在第一和第二引脚通孔之间延伸的虚线与所述接地通孔相交。

6. 根据权利要求 4 所述的高数据速率连接器系统，其特征在于，第一和第二引脚通孔在直径上小于所述接地通孔。

7. 根据权利要求 1 所述的高数据速率连接器系统，其特征在于，第一引脚通孔在直径上小于所述接地通孔。

8. 根据权利要求 1 所述的高数据速率连接器系统，其特征在于，所述连接器被配置为以大于 15Gbps 的数据速率运行。

9. 一种电路板，包括 ：

顶层 ；

接地层 ；

信号层，其位于所述顶层和所述接地层之间 ；

第一对信号通孔，其从所述顶层延伸至所述接地层，并耦接至所述信号层上的第一对信号迹线，第一对信号通孔与所述接地层电隔离，且每个信号通孔被配置成接收端子尾部 ；

第二对信号通孔，其从所述顶层延伸至所述接地层，并耦接至所述信号层上的第二

对信号迹线，第二对信号通孔与所述接地层电隔离，且每个信号通孔被配置成接收端子尾部；

第一接地通孔，其在所述顶层和所述接地层之间延伸，并电耦接至所述接地层，所述接地通孔被配置成接收端子尾部；以及

引脚通孔，其邻近所述接地通孔布置，并在所述顶层和所述接地层之间延伸，并且电耦接至所述接地层，其特征在于，在运行中，所述引脚通孔未被配置成接收端子尾部，以及介于所述引脚通孔和所述接地通孔之间的虚线位于第一和第二对信号通孔之间。

10. 根据权利要求 9 所述的电路板，其特征在于，所述引脚通孔为布置在所述接地通孔的第一侧上的第一引脚通孔，所述电路板进一步包括位于所述接地通孔的第二侧上的第二引脚通孔，所述第一和第二引脚通孔设置成与所述接地通孔结合以在第一和第二对信号通孔之间形成有效的屏蔽。

11. 根据权利要求 10 所述的电路板，其特征在于，第二引脚通孔被 布置成使得在第一引脚通孔和第二引脚通孔之间的虚线与所述接地通孔相交。

12. 根据权利要求 9 所述的电路板，其特征在于，所述接地通孔具有第一直径，所述引脚通孔具有第二直径，第二直径小于第一直径。

13. 根据权利要求 12 所述的电路板，其特征在于，所述接地通孔和信号通孔具有大致相同的直径。

14. 根据权利要求 9 所述的电路板，其特征在于，第一对信号迹线布置成使得每个信号迹线围绕所述接地通孔和所述引脚通孔中的一个的相对两侧延伸，所述电路板进一步包括信号环，所述信号环围绕所述接地通孔和所述引脚通孔中的一个延伸，并与所述接地通孔和引脚通孔中的一个电隔离。

15. 一种电路板，包括：

顶层；

接地层，该接地层包括地线层；

信号层，其位于所述顶层和所述接地层之间；

一对信号通孔，其从所述顶层延伸至所述接地层，并耦接至所述信号层上的一对信号迹线，该对信号通孔与所述接地层电隔离，且每个通孔被配置成接收端子尾部；

其特征在于，所述电路板还包括：

通孔，其在所述顶层和所述接地层之间延伸，并电耦接至所述地线层；

信号环，其围绕所述通孔延伸，且位于所述信号层上，所述信号环不与所述通孔直接电连通，其中该对信号迹线的每个信号迹线围绕所述信号环的相对两侧延伸。

16. 根据权利要求 15 所述的电路板，其特征在于，所述通孔为被配置成接收端子尾部的接地通孔和被配置为不接收端子尾部的引脚通孔中的一个。

17. 根据权利要求 16 所述的电路板，其特征在于，该对信号线中的迹线被配置成通过使用所述信号环将两迹线耦合在一起来在运行时保持较近的电耦合，所述信号环用于在沿围绕所述通孔的路径上的多个点处 降低两信号迹线之间的有效电隔离。

18. 根据权利要求 15 所述的电路板，其特征在于，该电路板包括在所述顶层和所述接地层之间延伸的第一引脚通孔，该第一引脚通孔与一接地通孔相邻设置，其中在所述接地通孔与第一引脚通孔之间所画虚线位于所述一对信号通孔的一侧。

19. 根据权利要求 18 所述的电路板，其特征在于，进一步包括与接地通孔相邻设置的第二引脚通孔，第一和第二引脚通孔位于接地通孔的相对两侧上。

高数据速率连接器系统及其电路板

技术领域

[0001] 本实用新型涉及连接器技术领域，更特别地涉及一种适用于高频信号传递的连接器。

背景技术

[0002] 高速连接器是高性能数字系统中广泛应用的主要产品。一般说来，连接器将不同的元件连接在一起，由此这些元件可以以高数据速率通讯。例如，现在 10-15Gbps 的数据速率正被使用于和 / 或被设计用于系统中，并且未来的系统可期望向每数据通道 17-25Gbps 发展。另外，连接器被制作得愈加紧凑，这使得提供较低数据速率具有挑战性，更不用说系统可能从中获益且在将来被期望的较高数据速率。

[0003] 连接器可被配置成提供需要的性能水平，同时连接器作为通常包括电路板（例如 PCB）的通讯系统的一部分。因此，对于安装于电路板上的元件而言，可能的通信路径可能包括将触头上的信号插入第一电路板上的第一组迹线。第一电路板上的第一组迹线从所述元件延伸至连接器的触头，通过该第一连接器延伸至第二匹配连接器，然后延伸至第二电路板上的迹线，进而至第二元件上。已经确定的是，在欲提供高数据速率的系统中存在的一个重要问题是电路板和连接器之间的接口。因为通常有两个这种接口，所以这个问题对系统的整体性能具有实质影响。因此，连接器和电路板接口的改进是值得重视的。

实用新型内容

[0004] 为了解决上述问题，本实用新型提供一种高数据速率连接器系统，包括：

[0005] 连接器，其包括具有安装表面和配合表面的壳体，所述壳体被配置成支撑多个端子，所述多个端子分别包括通孔尾部、对接部以及在通孔 尾部和配合部之间延伸的主体部，所述多个端子包括第一信号对和第二信号对以及至少一个接地端子，第一和第二信号对分别从所述安装表面延伸到所述配合表面，并被配置成在所述安装表面和配合表面之间提供差分信号路径，所述至少一个接地端子布置在第一和第二信号对之间，从而将第一信号对与第二对端子电屏蔽开；以及

[0006] 电路板，其包括顶层、具有地线层的接地层以及信号层，所述电路板包括与所述第一信号对的尾部耦接的第一对信号通孔以及与所述第二信号对的尾部耦接的第二对信号通孔，所述信号通孔中的每一个耦接到信号层上的迹线并与地线层隔离，所述电路板还包括从顶层延伸到接地层并延伸穿过信号层的接地通孔，所述接地通孔耦接至所述至少一个接地端子的尾部，并进一步耦接至所述地线层，

[0007] 所述电路板还包括从顶层延伸穿过信号层并耦接到所述地线层的引脚通孔，所述引脚通孔邻近所述接地通孔布置，其中在所述接地通孔和所述引脚通孔之间所画虚线位于第一和第二对信号通孔之间。

[0008] 进一步地，所述接地通孔和引脚通孔被配置成将信号层上的第一对信号通孔与第二对信号通孔屏蔽开。

[0009] 进一步地，所述引脚通孔是第一引脚通孔，并且所述电路板还包括第二引脚通孔，第一和第二引脚通孔被配置成第一和第二引脚通孔以及所述接地通孔的组合在所述信号层上的第一对信号通孔和第二对信号通孔之间有效地形成屏蔽。

[0010] 进一步地，所述接地通孔位于第一和第二引脚通孔之间。

[0011] 进一步地，第一和第二引脚通孔被配置成使得在第一和第二引脚通孔之间延伸的虚线与所述接地通孔相交。

[0012] 进一步地，第一和第二引脚通孔在直径上小于所述接地通孔。

[0013] 进一步地，第一引脚通孔在直径上小于所述接地通孔。

[0014] 进一步地，所述连接器被配置为以大于 15Gbps 的数据速率运行。

[0015] 根据本实用新型的另一个方面，本实用新型提供一种电路板，包括：

[0016] 顶层；

[0017] 接地层；

[0018] 信号层，其位于所述顶层和所述接地层之间；

[0019] 第一对信号通孔，其从所述顶层延伸至所述接地层，并耦接至所述信号层上的第一对信号迹线，第一对信号通孔与所述接地层电隔离，且每个信号通孔被配置成接收端子尾部；

[0020] 第二对信号通孔，其从所述顶层延伸至所述接地层，并耦接至所述信号层上的第二对信号迹线，第二对信号通孔与所述接地层电隔离，且每个信号通孔被配置成接收端子尾部；

[0021] 第一接地通孔，其在所述顶层和所述接地层之间延伸，并电耦接至所述接地层，所述接地通孔被配置成接收端子尾部；以及

[0022] 引脚通孔，其邻近所述接地通孔布置，并在所述顶层和所述接地层之间延伸，并且电耦接至所述接地层，其特征在于，在运行中，所述引脚通孔未被配置成接收端子尾部，以及介于所述引脚通孔和所述接地通孔之间的虚线位于第一和第二对信号通孔之间。

[0023] 进一步地，所述引脚通孔为布置在所述接地通孔的第一侧上的第一引脚通孔，所述电路板进一步包括位于所述接地通孔的第二侧上的第二引脚通孔，所述第一和第二引脚通孔设置成与所述接地通孔结合以在第一和第二对信号通孔之间形成有效的屏蔽。

[0024] 进一步地，第二引脚通孔被布置成使得在第一引脚通孔和第二引脚通孔之间的虚线与所述接地通孔相交。

[0025] 进一步地，所述接地通孔具有第一直径，所述引脚通孔具有第二直径，第二直径小于第一直径。

[0026] 进一步地，所述接地通孔和信号通孔具有大致相同的直径。

[0027] 进一步地，第一对信号迹线布置成使得每个信号迹线围绕所述接地通孔和所述引脚通孔中的一个的相对两侧延伸，所述电路板进一步包括信号环，所述信号环围绕所述接地通孔和所述引脚通孔中的一个延伸，并与所述接地通孔和引脚通孔中的一个电隔离。

[0028] 根据本实用新型的又一个方面，本实用新型提供一种电路板，包括：

[0029] 顶层；

[0030] 接地层，该接地层包括地线层；

[0031] 信号层，其位于所述顶层和所述接地层之间；

[0032] 一对信号通孔，其从所述顶层延伸至所述接地层，并耦接至所述信 号层上的一对信号迹线，该对信号通孔与所述接地层电隔离，且每个通孔被配置成接收端子尾部；

[0033] 其特征在于，所述电路板还包括：

[0034] 通孔，其在所述顶层和所述接地层之间延伸，并电耦接至所述地线层；

[0035] 信号环，其围绕所述通孔延伸，且位于所述信号层上，所述信号环不与所述通孔直接电连通，其中该对信号迹线的每个信号迹线围绕所述信号环的相对两侧延伸。

[0036] 进一步地，所述通孔为被配置成接收端子尾部的接地通孔和被配置为不接收端子尾部的引脚通孔中的一个。

[0037] 进一步地，该对信号线中的迹线被配置成通过使用所述信号环将两迹线耦合在一起来在运行时保持较近的电耦合，所述信号环用于在沿围绕所述通孔的路径上的多个点处降低两信号迹线之间的有效电隔离。

[0038] 进一步地，该电路板包括在所述顶层和所述接地层之间延伸的第一引脚通孔，该第一引脚通孔与一接地通孔相邻设置，其中在所述接地通孔与第一引脚通孔之间所画虚线位于所述一对信号通孔的一侧。

[0039] 进一步地，该电路板包括与接地通孔相邻设置的第二引脚通孔，第一和第二引脚通孔位于接地通孔的相对两侧上。

[0040] 电路板包括两对信号通孔和位于该两对信号通孔之间的接地通孔。所述信号通孔与电路板的信号层上的迹线耦接。接地通孔与电路板的地线层耦接。所述接地通孔和信号通孔都被配置成接收安装到电路板上的连接器的端子尾部。一个或多个引脚通孔(pinning via)可以与接地通孔相邻设置，并且也与所述地线层耦接，但不接收所述连接器的端子尾部。所述接地通孔和一个或多个引脚通孔结合，用来帮助提供电屏蔽，从而帮助防止两对信号通孔之间的串扰。

[0041] 在一个实施例中，连接器可以安装到电路板上，使得所述成对的信号端子尾部布置在信号通孔内，接地端子尾部布置在接地通孔内。电路板和连接器的组合可以提供彼此屏蔽的成对的信号通道，并且引脚通孔可以提供延伸穿过所述尾部和信号迹线之间的接口的屏蔽。

[0042] 在一个实施例中，信号迹线可以从两个信号通孔布置在电路板上， 使得信号迹线以差分的方式耦合。信号可以围绕通孔的相对侧延伸，该通孔可以为接地通孔，并且信号环(signal collar)可用于帮助将信号迹线之间的任何电隔离最小化，该电隔离可能是由于两信号迹线之间的通孔引起的物理隔离的增加而造成的。

附图说明

[0043] 本实用新型借助于实例进行说明，但不限于所附附图，在所附附图中，相同的附图标记表示类似的元件，其中：

[0044] 图 1 示出了连接器和电路板组件的一个实施例的透视图。

[0045] 图 1a 示出了连接器和电路板组件的另一个实施例的透视图。

[0046] 图 2 示出了图 1 中描述的组件的局部透视图。

[0047] 图 3 示出了连接器端子和电路板之间的接口的一个实施例的透视图。

[0048] 图 4 示出了图 3 中描述的接口的简化透视图。

[0049] 图 5 示出了电路板的一个实施例的俯视图。

[0050] 图 6 示出了电路板的另一实施例的俯视图。

[0051] 图 7 示出了图 5 中描述的实施例的其它特征。

[0052] 图 8 示出了图 6 中描述的实施例的其它特征。

[0053] 图 9 示出了电路板的可选实施例的俯视图。

[0054] 图 10 示出了包括多个层的电路板的实施例的透视图。

[0055] 图 11 示出了图 10 中描述的实施例的透视图，其中省略了多个层。

[0056] 图 12 示出了图 11 中描述的实施例的俯视图。

[0057] 图 13 示出了轨迹结构的实施例的俯视图。

具体实施方式

[0058] 本申请要求于 2009 年 3 月 25 日提交的美国临时申请号为 61/163,315 的申请的优先权，在此以引用的方式整体并入本文中。

[0059] 下面的详细说明描述了示例性实施例，但并不是限于明确公开的组合。因此，除非另有说明，这里公开的特征可以被组合在一起构成其它组合，这些组合出于简洁的目的而未另外示出。

[0060] 将连接器耦接至电路板（例如印刷电路板）的系统有时使用已知的 通孔结构。特别地，连接器内的端子包括尾部，这些尾部被配置为插入到电路板上的通孔内，然后被焊接在适当的位置。这些通孔由此将连接器内的端子耦接到电路板上的信号迹线。这种系统提供了良好的机械性能，并且允许宽范围的连接器都能够被电路板支撑。虽然存在许多连接器设计，但是电路板的接口往往比较类似。一般来说，某些通孔用于传输信号（通常以差分信号的结构），并用于将电路板上的信号迹线耦接至连接器的信号端子。其它通孔用于将连接器的接地端子耦接至地线层（例如电路板的接地层）。众所周知，一个设计差的连接器会把信号端子上的信号噪声引入其它电相邻的信号端子。可能较少被重视的是连接器和电路板之间的接口对整个系统的影响。

[0061] 图 1 示出了连接器和电路板组件 10 的实施例，为了说明目的，连接器 20 部分未进行组装。可以看出，端子触头 31 位于安装表面 24 内（所示安装表面为卡槽结构），并且部分端子延伸到电路板 50，如所示，薄片状针座 22 用于在所希望的方向上支撑多个端子。可以看出，这些针座彼此毗邻设置。因此，不仅在连接器内，而且在连接器 20 和电路板 50 之间的接口内都需要注意信号。

[0062] 图 1A 示出了组件的另一实施例，其包括通过连接器组件 210、211 连接在一起的电路板 250、251、252。可以看出，虽然电路板 251 上的一些通孔可以被电路板 251 的两侧上的端子使用（例如，它们是共用通孔），但是有些通孔并不共用，因此电路板 251 上（有时被称为中间面）的信号迹线需要布线到其它通孔。可以看出，基于中间面的组件，例如图 1A 所示，可以包括多个类似的连接器组件，且位于中间面一侧上的一个连接器组件的一些端子可以通过使用迹线被布线到位于中间面另一侧上的不同的连接器组件。因此，中间面设计可以提供重要的灵活性。然而，对于比较简单的设计而言，连接器组件可以将两个电路板（或电缆和电路板）耦接在一起。一般来说，连接器可以包括图 1 中示出的安装表面和配合表面，尽管配合表面和安装表面可能会有许多变化。

[0063] 图 2 示出了图 1 中描述的连接器组件 10 的特征。可以看出，端子 30 包括信号端子 34 和接地端子 33a、33b。每个端子具有接触部 30a、尾部 30b 和在它们之间延伸的主体部 30c。在一个实施例中，两个信号端子 34 将被配置作为一个信号对，并在操作中耦合在一起以提供一个差分信号路径。接地端子，例如接地端子 33b 将帮助相互屏蔽位于连接器 10 主体内的两个不同的差分信号对。在一个实施例中，如所示，接地端子可以宽于信号端子，以帮助在作为差分信号对的端子对之间提供更大的屏蔽。可以看出，一般地，将接地端子设置在两个不同的信号端子对之间有助于降低信号对之间的串扰，并且有助于信号对在较高的频率下运行以达到所希望的噪声水平（因此允许有更高的数据速率）。例如，因为针座允许信号端子之间的可控宽边耦合，并且桥接件 25（其可以由任意合适的导电材料制成，且具有任意适当的形状）被间隔开以帮助确保接地端子 33 所提供的接地结构在所关心的频率上基本无谐振，图 2 所示连接器可配置成在大于 10GHz 的奈奎斯特频率 (Nyquist frequency) 下运行。因此，这种连接器可以考虑被配置为在大于 16Gps 的数据速率下运行，并且甚至在大于 20Gps 的数据速率下运行。

[0064] 如所示，连接器 10 包括共用结构和有用的电气间隔，该共用结构将接地端子耦接在一起。虽然共用结构可以采用多种形式且并非必需的，但是对于更高速的运行而言，已经确定的是这种接地的共用对于降低电谐振是有益的，否则电谐振将会向信号中引入不希望的噪声。对于许多连接器而言，当奈奎斯特频率接近或者超过 8GHz 时，这种共用的性价比利益也更加有益，然而更大的连接器甚至在较低的奈奎斯特频率下也受益于这种共用结构。

[0065] 图 3 和 4 示出了连接器内的端子和电路板上的通孔之间的接口。接地通孔 52 配置成收容接地或屏蔽端子 33a、33b 的尾部，而信号通孔 54 配置成收容信号端子 34、35 的尾部。如所示，接地端子比信号端子更宽。如所示，一排信号对设置有介于信号对之间的接地端子。在一个实施例中，信号对可以宽边耦合在连接器中，然后在尾部改变为边缘耦合，应当注意，在一个实施例中边缘耦合可以使端子根据图 5 中所示布局排成一列，或者在一实施例中根据图 6 中所示的布局偏移。因此，成对的信号通孔 54 可以沿着与针座的纵轴一致的直线布置，或者它们可以沿着与针座的纵轴成一定角度的直线布置。虽然从性能的角度。两者相当，但是信号端子沿着与纵轴一致的直线布置的好处是可以简化布线。相对于纵 轴成一定角度的优势是，针座内的端子在制造过程中不需要形成和前者一样多。

[0066] 可以进一步看出，设置有多个引脚通孔 55，但是这些引脚通孔 55 并不收容端子的尾部。引脚通孔的尺寸可以与其它通孔相似，或者它们可以比其它通孔更小，因为它们不用收容端子尾部，并且小尺寸具有允许更加紧凑的接口的优点（并且潜在地降低接口内的阻抗不连续，这种不连续可能是由于接口变得相对来说呈容性而引起的）。引脚通孔 55 与接地通孔 52 相邻，并如所示位于接地通孔 52 的相对两侧。因此，从图 4-9 可以看出，引脚通孔可以在电路板表面和接地层之间延伸的信号对之间有效地形成栅栏或屏蔽。

[0067] 可以看出，对于连接器结构，其中两个单独的针座分别提供构成所述信号对的端子中的一个端子，该端子可以设置为许多结构。例如在图 5 中，信号端子形成一条直线，该直线与针座对齐。在图 6 中，信号端子形成一条直线，该直线与针座成一定角度。在具有两个引脚通孔的实施例中，连接两个引脚通孔的虚线可以与接地通孔相交（由此形成一直栅栏结构）。应当注意，如果设置有两个引脚通孔，它们可以布置在相对两侧上（如图 4-8 所

示），或者相同一侧上（接地通孔相对于信号通孔更偏斜）。中心结构的优点是存在于信号端子和接地端子之间的共用模式可以更容易保持。不论信号通孔的方位，由接地通孔和多个引脚通孔构成的栅栏（或虚线）可以设置在信号通孔对之间。

[0068] 然而，从图 9 可以看出，也可以使用一个引脚通孔。这种结构允许电路板上有更紧密的空间，因此可帮助在相对紧凑的连接器内提供良好的电绝缘。应当注意到，虽然所示两个引脚通孔与一个接地通孔相关，但是也可以根据需要使用其他的引脚通孔（在实施中或者将栅栏柱移动地更近，或者延长栅栏的长度）。大量的引脚通孔带来的一个问题是在信号层上布置信号迹线变得更加困难。因此，对于某些应用而言，可以优选一个或两个引脚通孔，因为每个接地通孔具有三个或更多相关的引脚通孔将会使得以理想的方式布置信号迹线变得基本上不可能。

[0069] 图 10-12 示出了电路板的一个实施例的特征。一般来说，多层电路板包括顶层 82、信号层 81 和接地层 80（其包括一地线层）。虽然图 10 中描述了其它层用于显示可以使用多个层，但是总的层数通常为偶数，因为电路板通常具有偶数个层数以确保对称（由此将扭曲的可能性降低到最小）。因此，虽然可以设置其它层，如果设置了接地层、信号层和顶层，通常在电路板的相对侧设置至少三个与接地层、信号层和和顶层相同模式的其它层。应当注意，虽然所示结构中顺序是顶层、信号层和接地层，但是接地层还可以布置在信号层和顶层之间。假定电路板是普通的对称层设计，那么在接地层和顶层之间设置信号层的好处是电路板的两半部分上的迹线可以彼此屏蔽。

[0070] 不管接地层和信号层的方位如何，信号通孔通常包括在接地层围绕它们的隔离盘 72（如所示，用于每个信号端子的隔离盘是独立的正方形形状，其可以实现紧凑排列，但是也可以设想其它构造，例如用于两个信号端子的单个隔离盘，或者一些其它形状的隔离盘），如果信号通孔穿过隔离盘能够将信号通孔与接地层上的接地平面电隔离。从图 11、12 中可以看出，信号迹线 61、62 由此设置在除接地层以外的不同平面内，并且均电耦合至信号通孔。信号迹线通常布置成它们保持彼此接近（以确保存在于两个差分信号传递之间的差分模式的连续性）。

[0071] 在过去已经引起问题的事情是需要围绕通孔布线，例如延伸通过信号层的引脚通孔或接地通孔。图 13 示出了一实施例，该实施例允许信号环 163 围绕通孔 152 延伸。信号环 163 与通孔 152 电隔离，通孔 152 可以耦合到地线层，并且可以是接地或引脚通孔。信号迹线 161、162 间隔开一距离 164，该距离可以保持信号迹线路径，从而确保构成所述信号迹线对的两迹线之间的相对持续的耦合。如所示，信号迹线 161、162 围绕通孔 152 的相对两侧布线。通常所产生的电隔离将会对电特性具有显著的影响。然而，信号迹线之间的有效电间隔被基本保持着，因为信号环 163 降低了信号迹线 61、62 之间的电隔离。因此，在剩余的信号迹线路径上，信号迹线将电隔离设置成接近于距离 165 的两倍（相对接近于当信号迹线间隔开距离 164 存在的电隔离）。因此，所示结构允许以一种方便的形式从端子尾部与收容通孔之间的接口布置信号迹线，同时仍能实现紧凑的封脚。因此，这种结构在具有紧凑间隔的同时还具有良好的电性能，尤其是在更高的信号频率时，例如大于 10GHz 的奈奎斯特频 率。

[0072] 可以看出，本文描述的各种特征可以单独使用，也可以根据需要组合使用。因此，电路板可以包括与一个或多个接地通孔相关联的一个或多个引脚通孔，和 / 或电路板可以

包括一个或多个信号环以帮助改善电路板的布线性能。此外，连接器可以安装到包括一个或多个上述特征的电路板上。

[0073] 根据优选和示范实施例已经描述了本实用新型。在理解本实用新型的基础上，本领域的普通技术人员将会想到落入附属权利要求范围和精神内的许多其它的实施例、修改和变化。

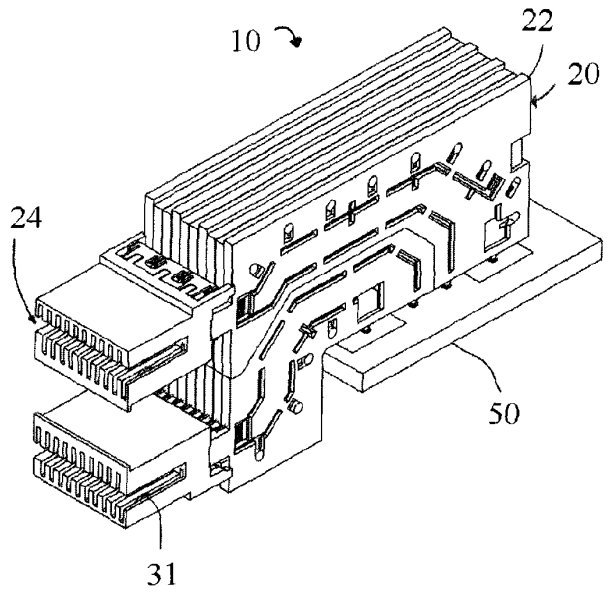

图 1

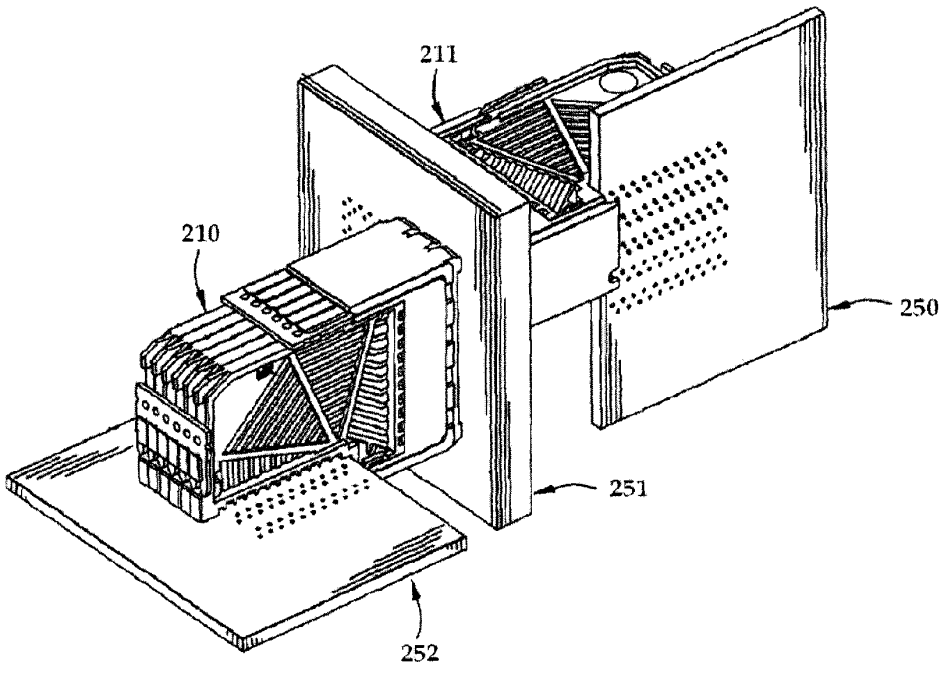

图 1A

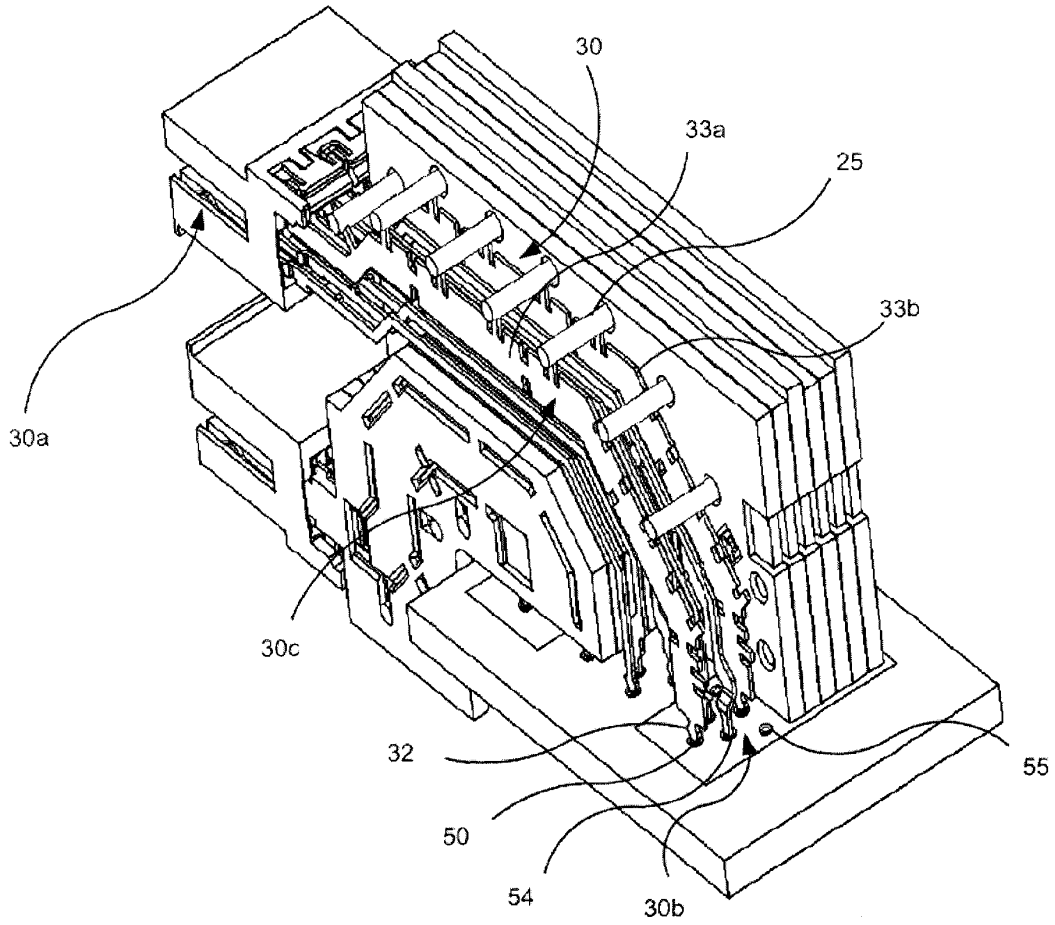

图 2

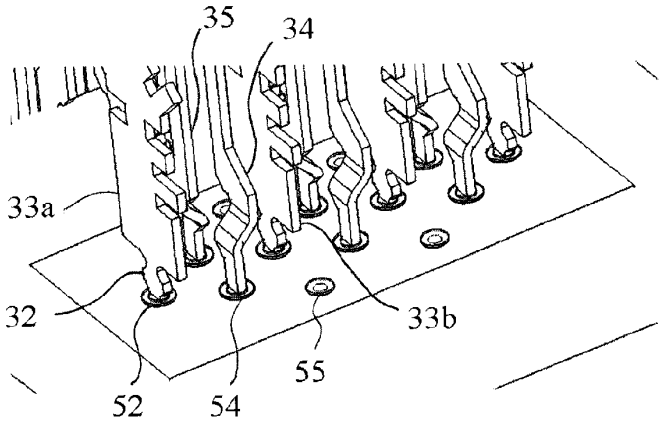

图 3

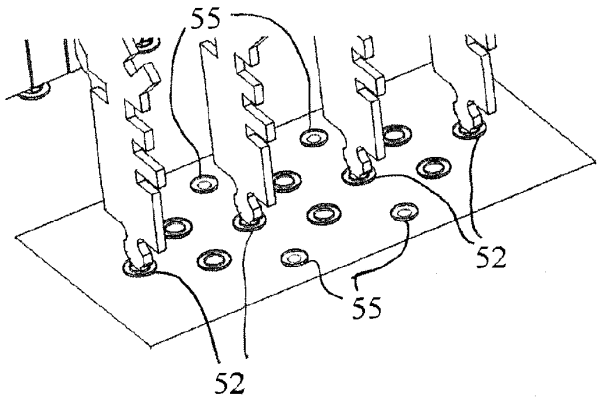

图 4

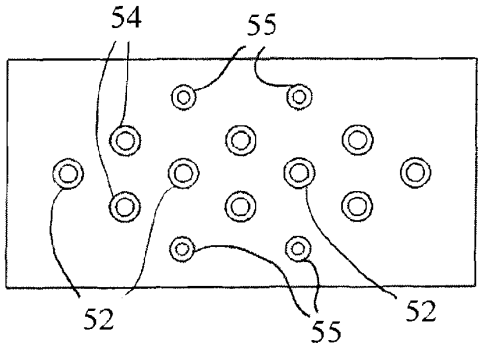

图 5

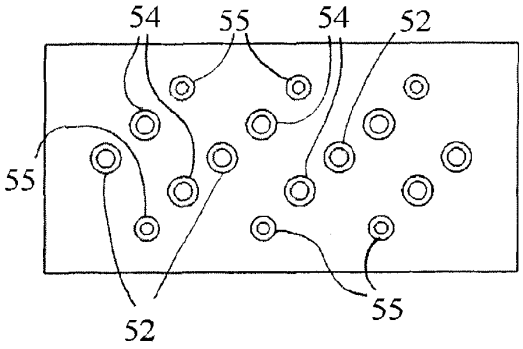

图 6

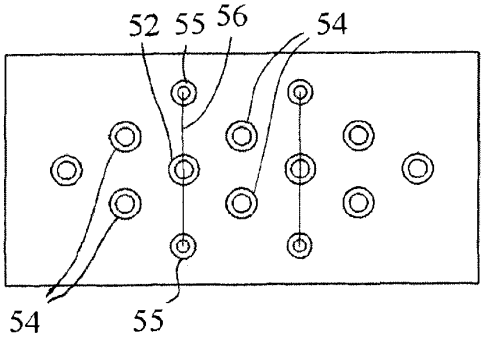

图 7

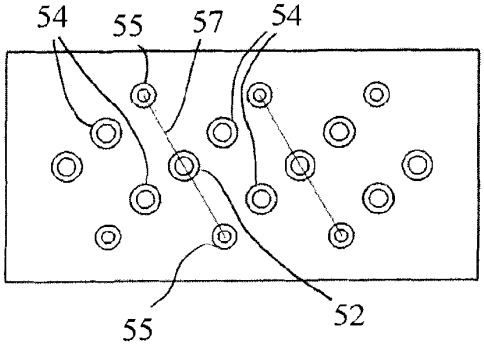

图 8

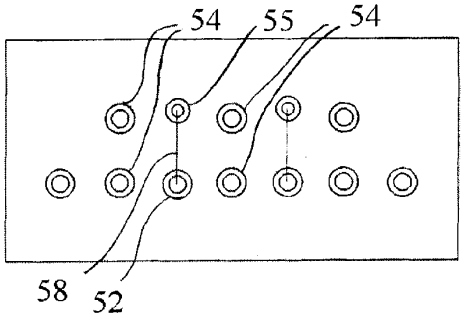

图 9

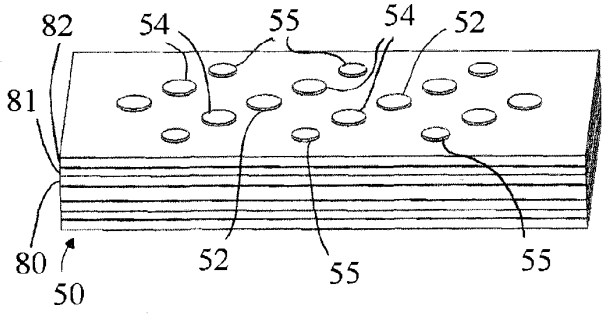

图 10

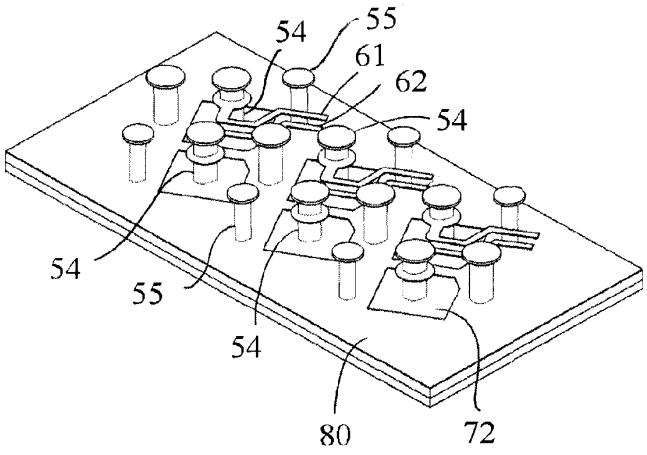

图 11

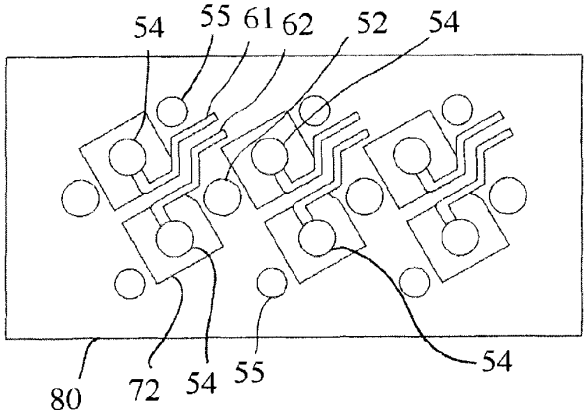

图 12

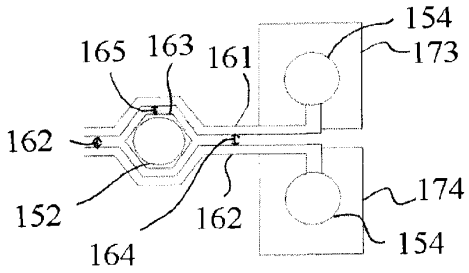

图 13

Espacenet

Bibliographic data: DE60216728 (T2) — 2007-11-08

CONNECTOR MOLDING METHOD AND SHIELDED WAFERIZED CONNECTOR MADE THEREFROM

Inventor(s): ASTBURY L [US]; COHEN S [US] ± (ASTBURY, L, ; COHEN, S)

Applicant(s): AMPHENOL CORP [US] ± (AMPHENOL CORP)

Classification: - international: ***H01R13/514; H01R13/658;*** *H01R12/50*
- cooperative: **H01R13/6587**

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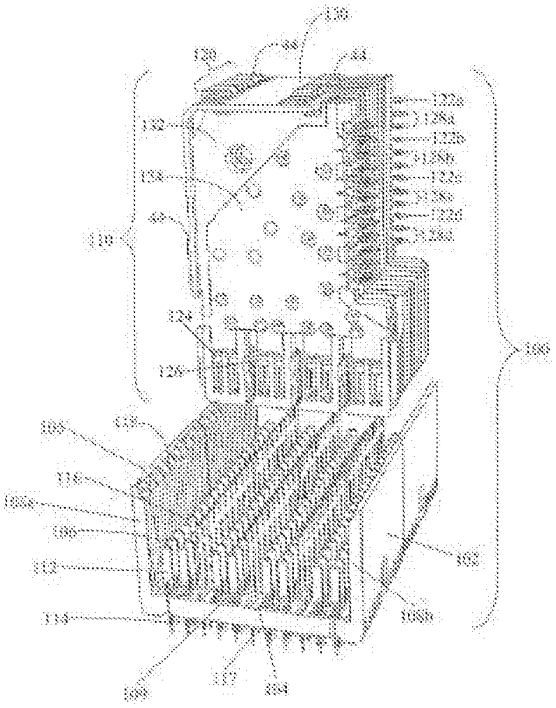
Abstract not available for DE60216728 (T2)
Abstract of corresponding document: US6409543 (B1)

A high speed, high density electrical connector. The connector is assembled from wafers. Each wafer is formed by molding a first dielectric housing over a shield plate. Signal contacts are inserted into the first dielectric housing and a second housing is overmolded on the first housing. Features are employed to lock the first and second housings together with the shield plate to provide a mechanically robust subassembly. The connector as formed has a good electrical properties, including precise impedance control and low cross talk.



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H01R 12/20 (2006.01)
H01R 13/514 (2006.01)

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(74) Vertreter:
derzeit kein Vertreter bestellt

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(54) Bezeichnung: **Verbinderformverfahren und davon abgeschirmter Verbinder in Plattenbauweise**

Beschreibung

[0001] Diese Erfindung betrifft im Allgemeinen elektrische Schaltverbindungen und spezieller elektrische Hochleistungsverbinder hoher Packungsdichte, die verwendet werden, um Leiterplatten zu verbinden.

[0002] Eine moderne elektronische Schaltung wird oftmals auf Leiterplatten aufgebaut. Die Leiterplatten werden danach verbunden, um ein vollständiges System zu bilden, wie beispielsweise eine Computer-Workstation oder einen Router für ein Kommunikationsnetz. Elektrische Verbinder werden oftmals verwendet, um die Schaltverbindungen herzustellen. Im Allgemeinen kommen die Verbinder in zwei Teilen, mit einem Teil auf jeder Platte. Die Verbinderteile passen zusammen, um Signalwege zwischen den Platten zu liefern.

[0003] Das WO 00/10233 offenbart einen Buchsenverbinder mit Mehrfachmodulen für ein Einsetzen in ein Buchsengehäuse. Vertikale Abschirmungen und horizontale Endabschirmungen bilden eine Abschirmung um Signalleiter.

[0004] Das U.S.Patent 5993259 offenbart einen Hochleistungsverbinder hoher Packungsdichte, der aus Platten hergestellt wird, wobei jede Erdungsfläche und senkrechte Signalreihe in die Bauteile gespritzt werden, die eine Platte bilden, wenn sie kombiniert werden.

[0005] Ein guter Verbinder muss eine Kombination von mehreren Eigenschaften aufweisen. Er muss Signalwege mit geeigneten elektrischen Eigenschaften bereitstellen, so dass die Signale nicht übermäßig verzerrt werden, während sie sich zwischen den Platten bewegen. Außerdem muss der Verbinder sichern, dass die Teile leicht und zuverlässig zueinanderpassen. Außerdem muss der Verbinder stabil sein, so dass er bei Handhabung der Leiterplatten nicht beschädigt wird. In vielen Systemen ist es ebenfalls wichtig, dass die Verbinder eine hohe Packungsdichte aufweisen, was bedeutet, dass sie eine große Anzahl von elektrischen Signalen pro Längeneinheit führen können.

[0006] Beispiele für sehr erfolgreiche elektrische Hochleistungsverbinder hoher Packungsdichte sind die VHDM™- und VHDM-HSD™-Verbinder, die von der Teradyne Connection Systems of Nashua, New Hampshire, USA, verkauft werden.

[0007] Es wäre jedoch wünschenswert, einen noch besseren elektrischen Verbinder bereitzustellen. Es ist ebenfalls wünschenswert, vereinfachte Verfahren zur Herstellung von Verbindern bereitzustellen.

[0008] Die Erfindung stellt ein Verfahren nach Patentanspruch 1 zur Herstellung einer Platte für eine Verwendung in einem Verbinder und einen elektrischen Verbinder nach Patentanspruch 10 bereit.

[0009] Die Erfindung kann einen verbesserten elektrischen Hochleistungsverbinder hoher Packungsdichte bereitstellen.

[0010] Bei der bevorzugten Ausführung wird ein Isolator um die Abschirmung geformt, wobei Zwischenräume verbleiben, um Signalkontakte aufzunehmen. Die Signalkontakte werden danach in den Zwischenräumen angeordnet, und es wird ein zweiter Formvorgang durchgeführt, wobei ein verriegeltes Formgehäuse zurückbleibt.

[0011] Entsprechend weiteren charakteristischen Merkmalen der bevorzugten Ausführung sind die Abschirmung und das Kunststoffgehäuse so geformt, dass eine mechanische Integrität für die Platten bewirkt wird.

KURZE BESCHREIBUNG DER ZEICHNUNGEN

[0012] Die vorangegangenen und weiteren Ziele, charakteristischen Merkmale und Vorteile der Erfindung werden aus der folgenden spezielleren Beschreibung eines abgeschirmten Verbinders in Plattenbauweise ersichtlich werden, wie er in den als Anlage beigefügten Zeichnungen veranschaulicht wird, bei denen gleiche Bezugszeichen die gleichen Teile durchgängig bei den verschiedenen Ansichten betreffen. Für die Deutlichkeit und Leichtigkeit der Beschreibung müssen die Zeichnungen nicht maßstabgetreu gezeichnet werden, wobei anstelle dessen die Betonung auf der Veranschaulichung der Prinzipien der Erfindung liegt.

[0013] Es zeigen:

[0014] Fig. 1 eine grafische Darstellung eines zweiteiligen modularen elektrischen Verbinders;

[0015] Fig. 2 eine grafische Darstellung einer Platte aus Fig. 1, die entsprechend einer Ausführung der Erfindung zusammengebaut ist;

[0016] Fig. 3 eine grafische Darstellung einer Abschirmplatte;

[0017] Fig. 4 eine grafische Darstellung einer Plattenunterbaugruppe, die die Abschirmplatte aus Fig. 3 umfasst;

[0018] Fig. 5 eine grafische Darstellung eines Signalleitungsrahmens;

[0019] Fig. 6 eine grafische Darstellung des Signalleitungsrahmens aus Fig. 5, der auf der Plattenunterbaugruppe aus Fig. 4 positioniert ist;

[0020] Fig. 7 die Baugruppe aus Fig. 6, nachdem die Befestigungsstreifen des Signalleitungsrahmenträgerstreifens durchgetrennt wurden;

[0021] Fig. 8 eine grafische Darstellung, die die Platten zeigt, die mit dem Basisverbinder zusammenpassen;

[0022] Fig. 9 die Platten, die mit dem Basisverbinder zusammenpassen, vom umgekehrten Winkel; und

[0023] Fig. 10 eine auseinandergezogene Darstellung der alternativen Ausführung des Basisverbinders.

DETAILLIERTE BESCHREIBUNG DER ERFINDUNG

[0024] Mit Bezugnahme auf Fig. 1 wird ein zweiteiliger elektrischer Verbinder **100** gezeigt, der einen Basisverbinder **105** und einen Tochterleiterplattenverbinder **110** umfasst. Der Basisverbinder **105** umfasst eine Basisabdeckung **102** und eine Vielzahl von Signalkontakten **112**, die hier in einer Anordnung von differentiellen Signalpaaren angeordnet sind. Eine einseitige Konfiguration der Signalkontakte **112** wird ebenfalls in Betracht gezogen. Bei der veranschaulichten Ausführung wird die Basisabdeckung **102** aus einem dielektrischen Material geformt, wie beispielsweise einem Flüssigkristallpolymer (LCP), einem Polyphenylinsulfid (PPS) oder einem hochtemperaturbeständigen Nylon.

[0025] Die Signalkontakte **112** erstrecken sich durch einen Boden **104** der Basisabdeckung **102**, wobei eine Kontaktfläche sowohl oberhalb als auch unterhalb des Bodens **104** der Abdeckung **102** bereitgestellt wird. Hierbei liegt die Kontaktfläche der Signalkontakte **112** über dem Abdeckungsboden **104** in der Form eines Messerkontaktes **106** vor. Die Kontaktfläche des Endabschnittes **114** des Signalkontaktes **112**, die sich unterhalb des Abdeckungsbodens **104** erstreckt, liegt hierbei in der Form eines eine Presspassung aufweisenden als „Nadelöhr" ausgebildeten nachgiebigen Kontaktes vor. Andere Konfigurationen sind jedoch ebenfalls geeignet, wie beispielsweise Oberflächenmontageelemente, Federkontakte, lötbare Stifte, usw. Bei einer typischen Konfiguration passt der Basisverbinder **105** mit dem Tochterleiterplattenverbinder **110** an den Messerkontakten **106** zusammen und verbindet sich mit Signalleiterbahnen in einer Trägerplatte (nicht gezeigt) durch die Endabschnitte **114**, die in die durchkontaktierten Löcher in der Trägerplatte gepresst werden.

[0026] Die Basisabdeckung **102** umfasst außerdem Seitenwände **108a**, **108b**, die sich entlang der Länge der entgegengesetzten Seiten der Basisabdeckung **102** erstrecken. Die Seitenwände **108a**, **108b** umfassen Nuten **118**, die vertikal längs einer Innenfläche der Seitenwände **108a**, **108b** verlaufen. Die Nuten **118** dienen dazu, den Tochterleiterplattenverbinder **110** in die geeignete Position in der Abdeckung **102** zu führen. Parallel zu den Seitenwänden **108a**, **108b** verläuft eine Vielzahl von Abschirmplatten **116**, die hierbei zwischen Reihen der Paare von Signalkontakten **112** angeordnet sind. Bei einer gegenwärtig bevorzugten einseitigen Konfiguration würde die Vielzahl der Abschirmplatten **116** zwischen den Reihen der Signalkontakte **112** angeordnet. Andere Abschirmungskonfigurationen könnten jedoch gebildet werden, einschließlich der, die die man Abschirmplatten **116** aufweisen, die zwischen den Wanden der Abdeckungen quer zur veranschaulichten Richtung verlaufen.

[0027] Jede Abschirmplatte **116** umfasst einen Endabschnitt **117**, der sich durch die Abdeckungsbasis **104** erstreckt. Hierbei wird der Endabschnitt **117** als ein als „Nadelöhr" ausgebildeter nachgiebiger Kontakt gebildet, der in die Trägerplatte mittels Presspassung gebracht wird; es sind jedoch andere Konfigurationen ebenfalls geeignet, wie beispielsweise Oberflächenmontageelemente, Federkontakte, lötbare Stifte, usw.

[0028] Es wird gezeigt, dass der Tochterleiterplattenverbinder **110** eine Vielzahl von Modulen oder Platten **120** umfasst, die mittels einer Versteifung **130** gestützt werden. Jede Platte **120** umfasst charakteristische Merkmale **44**, die in Öffnungen (nicht nummeriert) in der Versteifung eingesetzt werden, um jede Platte **120** mit Bezugnahme zueinander anzuordnen und weiter, um eine Drehung der Platte **120** zu verhindern.

[0029] Mit Bezugnahme auf Fig. 2 wird eine einzelne Platte gezeigt. Es wird gezeigt, dass die Platte **120** ein dielektrisches Gehäuse **132**, **134** umfasst, das um sowohl eine Tochterleiterplattenabschirmplatte **10** (Fig. 3) als auch einen Signalleitungsrahmen **60** (Fig. 5) gebildet wird. Eine bevorzugte Art und Weise des Bildens des dielektrischen Gehäuses um die Abschirmplatte **10** und den Signalleitungsrahmen **60** wird detailliert in Verbindung mit Fig. 3 bis Fig. 9 diskutiert.

[0030] Von einem ersten Rand einer jeden Platte **120** erstreckt sich eine Vielzahl von Signalkontaktlötenden **128a-128d**, die sich vom Signalleitungsrahmen **60** erstrecken, und eine Vielzahl von Erdungskontaktlötenden **122a-122d**, die sich von einem ersten Rand der Abschirmplatte **10** erstrecken. Bei der bevorzugten Ausführung werden die Vielzahl der Signalkontaktlötenden **128a-128d** und die Vielzahl der Erdungskontaktlötenden **122a-122d** in einer einzelnen Ebene angeordnet.

[0031] Hierbei liegen sowohl die Signalkontaktlöten-

den **128a-128d** als auch die Erdungskontaktlötenden **122a-122d** in der Form von eine Presspassung aufweisenden als „Nadelöhr" ausgebildete nachgiebige Kontakte vor, die in durchkontaktierte Löcher gepresst werden, die in einer Leiterplatte (nicht gezeigt) angeordnet sind. Andere Konfigurationen für die Signalkontaktlötenden **128a-128d** und die Erdungskontaktlötenden **122a-122d** sind ebenfalls geeignet, wie beispielsweise Oberflächenmontageelemente, Federkontakte, lötbare Stifte, usw. Hierbei sind die Signalkontaktlötenden **128** so ausgebildet, dass sie ein differentielles Signal liefern, und sie sind dazu in Paaren **128a-128d** angeordnet.

[0032] Nahe eines zweiten Randes einer jeden Platte **120** sind Gegenkontaktbereiche **124** der Signalkontakte vorhanden, die zu den Signalkontakten **112** des Basisverbinders **105** passen. Hierbei sind die Gegenkontaktbereiche **124** in der Form von Doppelanschlussbrücken vorhanden, um mit dem Ende des Messerkontaktes **106** der Trägerplattensignalkontakte **112** in Eingriff zu kommen. Die Gegenkontaktbereiche sind innerhalb von Öffnungen im dielektrischen Gehäuse **132** positioniert, um die Kontakte zu schützen. Öffnungen in der Eingriffsfläche der Platte gestatten, dass die Signalkontakte **112** ebenfalls in jene Öffnungen gelangen, um ein Eingreifen der Tochterleiterplatte und der Trägerplattensignalkontakte zu gestatten.

[0033] Um ein differentielles Signal zu führen, sind die Anschlussbrücken **124** in Paaren **124a-124d**, **124a'-124d'** ausgebildet. Bei einer einseitigen Konfiguration sind die Anschlussbrücken **124** nicht in Paaren vorhanden.

[0034] Zwischen den Paaren der Doppelanschlussbrückenkontakte **124** und ebenfalls in der Nähe des zweiten Randes der Platte sind Abschirmanschlussbrückenkontakte **126a-126c** vorhanden. Abschirmanschlussbrückenkontakte werden mit der Tochterleiterplattenabschirmplatte **10** verbunden und werden vorzugsweise aus der gleichen Metallplatte geformt, wie sie verwendet wird, um die Abschirmplatte **10** zu formen. Abschirmanschlussbrückenkontakte **126a**...**126c** kommen mit einem oberen Rand der Basisabschirmplatte **116** in Eingriff, wenn der Tochterleiterplattenverbinder **110** und der Basisverbinder **105** in Eingriff gebracht werden. Bei einer alternativen Ausführung (nicht gezeigt) ist der Anschlussbrückenkontakt auf der Basisabschirmplatte **116** vorhanden, und es wird ein Messer auf der Tochterleiterplattenabschirmplatte **10** zwischen den Paaren der Doppelanschlussbrückenkontakte **124** bereitgestellt. Daher ist die spezifische Form des Abschirmkontaktes für die Erfindung nicht kritisch.

[0035] Wie es vorangehend erwähnt wird, umfassen die Platten ein dielektrisches Gehäuse **132**, **134**. Die Platten **120** werden bei der bevorzugten Ausführung mittels eines Zweistufenformverfahrens hergestellt. Das erste Gehäuse **132** aus dielektrischem Material wird über der oberen Fläche der Tochterleiterplattenabschirmung **10** gebildet. Der Signalleitungsrahmen **60** (Fig. 5) wird auf der Oberfläche des ersten Gehäuses **132** angeordnet, und das zweite dielektrische Gehäuse **134** wird über dem Signalleitungsrahmen **60** gebildet, wobei der Signalleitungsrahmen **60** zwischen dem ersten und dem zweiten dielektrischen Gehäuse **132**, **134** eingekapselt wird. Das Zweistufenformverfahren wird detaillierter in Verbindung mit Fig. 3 bis Fig. 9 beschrieben.

[0036] Mit Bezugnahme auf Fig. 3 wird eine Tochterleiterplattenabschirmung **10** gezeigt, die an einem Trägerstreifen **12** befestigt ist. Typischerweise ist eine Vielzahl von Tochterleiterplattenabschirmungen auf einem Trägerstreifen **12** vorhanden, der in die Montageanlage geführt werden kann. Es wird gezeigt, dass der Trägerstreifen **12** eine Reihe von Öffnungen umfasst. Hierbei werden die Öffnungen, die an jedem Ende des Trägerstreifens angeordnet sind, als Ausrichtungslöcher **13** benutzt. Bei einer bevorzugten Ausführung werden die Vielzahl der Abschirmungen und der Trägerstreifen aus einer langen Metallplatte gestanzt und geformt.

[0037] Bei der veranschaulichten Ausführung ist die Tochterleiterplattenabschirmung **10** am Trägerstreifen **12** an zwei Stellen befestigt, auf die man sich im Allgemeinen als Befestigungsstreifen **14a**, **14b** bezieht. Benachbarte Abschirmungen **10** sind an Stellen angebracht, die durch Trägerstreifen **30a** und **30b** angezeigt werden. Die Trägerstreifen **12** und **30** werden an Ort und Stelle belassen, um eine mechanische Halterung zu liefern, und um bei der Handhabung der Platte während der Herstellung zu unterstützen, werden aber zu einen zweckmäßigen Zeitpunkt getrennt, bevor der Tochterleiterplattenverbinder **110** (Fig. 1) montiert wird.

[0038] Verschiedene charakteristische Merkmale sind in der Tochterleiterplattenabschirmung **10** ausgebildet. Wie es vorangehend beschrieben wird, ist das dielektrische Gehäuse **132** auf der oberen Fläche der Abschirmung **10** geformt. Eine Vielzahl von Nasen **18** und **21** ist in der Abschirmung **10** ausgebildet und über der oberen Fläche gebogen. Wem das dielektrische Gehäuse **132** auf dieser Fläche der Abschirmplatte **10** geformt wird, werden die Nasen **18** und **21** im dielektrischen Gehäuse eingebettet und sichern die Abschirmung **10** am dielektrischen Gehäuse **132**. Auf diese Weise verbessern diese charakteristischen Merkmale die mechanische Integrität der Platte **120**.

[0039] Eine zweite Gruppe von Nasen **320** wird ebenfalls auf der oberen Fläche der Abschirmung **10** gebildet. Wie in Verbindung mit Fig. 4 deutlicher gezeigt wird, werden die Nasen **320** im dielektrischen

Gehäuse **134** eingebettet und begünstigen weiter die mechanische Integrität der Platte **120**, indem gesichert wird, dass die Abschirmung und beide dielektrischen Gehäuse miteinander gesichert werden.

[0040] Zusätzlich werden Nasen **318** aus der Platte heraus gebildet. Die Nasen **318** dienen mehreren Zwecken. Wie bei den Nasen **18**, **21** und **320** unterstützen die Nasen **318** das Sichern der Platte **10** am dielektrischen Gehäuse. Zusätzlich dienen die Nasen **318** als Befestigungspunkt für die Kontaktlötenden **122a**...**122d**. Weil die Nasen **318** über der Ebene der Abschirmung **10** gebogen sind, richten sich die Kontaktlötenden **122a**...**122d** mit den Signalkontaktlötenden **128a**...**128d** aus, um eine einzelne senkrechte Reihe von Kontaktlötenden für jede Platte zu bilden. Als weiterer Vorteil positionieren die Nasen **318** die Kontaktlötenden **122a**...**122d** innerhalb des dielektrischen Gehäuses und machen sie für ein Biegen weniger empfänglich, wenn die Kontaktlötenden **122a**...**122d** in eine Leiterplatte gepresst werden. Im Ergebnis dessen ist der Verbinder robuster.

[0041] Der Ring **16** ist ein Beispiel für ein Ausrichtungsmerkmal, das während der Herstellung der Verbinderelemente benutzt werden kann. In verschiedenen Stufen bei der Herstellung des Verbinders müssen die Bauteile relativ zu den Werkzeugen oder zueinander ausgerichtet werden. Beispielsweise muss die Abschirmung **10** relativ zu der Form oder zu den Werkzeugen ausgerichtet werden, wenn eine selektive Metallisierung der Kontaktbereiche auf der Abschirmplatte erforderlich ist. Der Ring **16** befindet sich außerhalb des Weges der Signalkontakte und hat daher einen geringen Einfluss auf den Abschirmwirkungsgrad der Abschirmung **10** und wird vorzugsweise abgetrennt, wenn er nicht mehr für die Ausrichtung benötigt wird. Der Ring **16** umfasst Nasen (nicht nummeriert), die im Gehäuse eingebettet werden, um den Ring **16** an Ort und Stelle zu halten, nachdem er getrennt ist, wodurch der Ring **16** davor bewahrt wird, die Funktion des Verbinders zu stören.

[0042] Die Abschirmung **10** enthält zusätzliche charakteristische Merkmale. Löcher **22** sind in der Abschirmplatte **10** eingeschlossen, um einen Zugang zu den inneren Abschnitten der Platte **120** bei späteren Schritten des Herstellungsvorganges zu gestatten. Ihre Verwendung wird in Verbindung mit Fig. 7 beschrieben.

[0043] Der vordere Rand der Abschirmplatte **10** umfasst Schlitze **332**. Jeder der Schlitze **332** nimmt eine Basisabschirmung **116** auf, wenn die Verbinderteile in Eingriff gebracht werden. Ebenfalls wird der Metallausschnitt, um den Schlitz **332** zu bilden, zum Abschirmanschlussbrückenkontakt **126** geformt.

[0044] Weil das Schneiden der Schlitze **332** die mechanische Integrität der Vorderseite der Abschirmung **10** verringert, können erhabene Abschnitte **330** und erhabene Rippen **333** in der Nähe des vorderen Randes der Abschirmung **332** gebildet werden. Das Bilden der erhabenen Abschnitte erhöht die Steifigkeit der Abschirmung in diesem Bereich. Die erhabenen Abschnitte bewegen ebenfalls die Abschirmplatte **10** der einen Platte weg von der benachbarten Platte und bilden einen vertieften Bereich. Während des Formens wird der vertiefte Bereich mit Formmaterial gefällt, um einen dielektrischen Bereich zu erzeugen (Element **912**, Fig. 9). Wie in Fig. 1 gezeigt wird, werden Signalkontakte **124** auf der Oberseite der Platte freigelegt. Wenn die Tochterleiterplatte und die Basisverbinder in Eingriff kommen, werden die Messer **106** die Signalkontakte **124** pressen, um sie nach oben oder in Richtung der Abschirmplatte der benachbarten Platte vorzuspannen. Der dielektrische Bereich **912** verhindert, dass Signalkontakte auf einer Platte die Abschirmplatte der benachbarten Platte kontaktieren.

[0045] Bei der veranschaulichten Ausführung erstreckt sich der Schlitz **332** nicht über die gesamte Länge der erhabenen Abschnitte **330**. Es ist ein flacher Bereich **331** über jedem Schlitz **332** vorhanden. Der flache Bereich **331** ist für ein Eingreifen eines Basisverbinders eingeschlossen, der einen verzahnten oberen Rand aufweist, wie in Fig. 1 gezeigt wird.

[0046] Löcher **26** sind ebenfalls in der Platte in den erhabenen Abschnitten **330** eingeschlossen. Während das dielektrische Gehäuse **132** auf die Abschirmung **10** geformt wird, wird dielektrisches Material durch Löcher **26** fließen, wodurch das Dielektrikum an der Abschirmung **10** sicher gehalten wird, was eine größere Steifigkeit am vorderen Ende des Verbinders bewirkt. Löcher **24** sind ebenfalls in der Abschirmung **10** eingeschlossen. Die Löcher **24**, wie die Löcher **26**, werden verwendet, um die Teile des Verbinders sicher zusammenzuhalten. Löcher **24** werden gefüllt, wenn das dielektrische Gehäuse **134** geformt wird, wodurch das dielektrische Gehäuse an der Abschirmung **10** sicher gehalten wird.

[0047] Die Abschirmung **10** kann ebenfalls charakteristische Merkmale umfassen, um die Signalintegrität des Verbinders zu erhöhen. Vorsprünge **28a** und **28b** sind eingeschlossen, um eine Abschirmung um die Endreihenkontakte zu bewirken. Wenn die Verbinderhälften in Eingriff gebracht werden, werden die inneren Gegenkontaktbereiche **124b** und **124c** jeweils zwischen den Abschirmplatten **116** vom Basisverbinder sein. Die äußeren Gegenkontaktbereiche **124a** und **124d** werden jedoch jeweils eine Abschirmplatte **116** vom Basisverbinder auf nur einer Seite aufweisen. Weil der Abstand und die Form der Erdungsleiter um einen Leiter die Signalführungseigenschaften jenes Leiters beeinflussen, ist es manchmal wünschenswert, geerdete Leiter auf allen Seiten eines Leiters zu haben, insbesondere im Gegenkon-

taktbereich.

[0048] Für die inneren Gegenkontaktbereiche **124b** und **124c** liefern die Abschirmung **10** der Platte **120**, in der die Signalkontakte angebracht sind, und die Abschirmung **10** der benachbarten Platte eine Erdungsebene auf zwei Seiten der Gegenkontakte. Die anderen zwei Seiten werden durch zwei der Basisabschirmungen **116** abgeschirmt, um ein geerdetes Gehäuse um die Eingriffsabschnitte der Signalleiter zu bilden. Für die äußeren Gegenkontaktabschnitte wird ein geerdetes Gehäuse um die Eingriffsabschnitte ebenfalls gebildet, wobei die vier Seiten aus den Abschirmungen **10** von zwei benachbarten Platten **120**, einer Basisabschirmung **116** und einem der Vorsprünge **28a** oder **28b** gebildet werden. Daher haben die äußeren Gegenkontaktabschnitte **124a** und **124d** einen Vorteil aus den Erdungsleitern an allen vier Seiten. Insgesamt ist es wünschenswert, dass alle Signalleiter eine symmetrische Abschirmung aufweisen, die für alle Paare von Leitern gleich ist.

[0049] In Fig. 4 wird jetzt eine Platte beim nächsten Herstellungsschritt gezeigt. In dieser Fig. wird das dielektrische Gehäuse **132** gezeigt, das über einer Abschirmung **10** geformt ist. Das Zweistufen-Spritzgießen ist auf dem Gebiet bekannt und wird in der Verbindertechnik angewandt, um Leiter innerhalb eines dielektrischen Gehäuses zu Tiefem. Im Gegensatz zu Verbindern nach dem bisherigen Stand der Technik wird das dielektrische Material über den größten Teil der Fläche der Abschirmung **10** geformt. Außerdem ist das Dielektrikum in großem Umfang auf der oberen Fläche der Abschirmung vorhanden, wobei die untere Fläche der Abschirmung freigelegt verbleibt.

[0050] Die Nasen **18**, **318** und **20** sind in Fig. 4 nicht sichtbar. Die Nasen **18**, **318** und **21** sind im dielektrischen Gehäuse **132** eingebettet. Die Nasen **322** sind sichtbar, weil das dielektrische Gehäuse **132** geformt ist, um Ausschnitte **424** um die Nasen **322** zu belassen. Gleichfalls sind die Löcher **22** und **24** sichtbar, weil kein dielektrisches Gehäuse um sie herum geformt wurde. Die Löcher **26** sind jedoch nicht sichtbar, weil das dielektrische Gehäuse **132** geformt wurde, um jene Löcher zu Pillen, und um die offenen Zwischenräume hinter den erhabenen Abschnitten **330** zu füllen.

[0051] Verschiedene charakteristische Merkmale werden in das dielektrische Gehäuse **132** geformt. Ein Hohlraum **450**, der durch die Wände **452** begrenzt wird, wird im Allgemeinen in den mittleren Abschnitten des Gehäuses **132** belassen. Kanäle **422** werden im Boden des Hohlraumes **450** gebildet, indem eng beabstandete vorstehende Abschnitte des dielektrischen Gehäuses bereitgestellt werden. Wie deutlicher in Fig. 6 gezeigt wird, werden Kanäle **422** benutzt, um Signalleiter zu positionieren. Ebenfalls werden Öffnungen **426** geformt, um einen Gegenkontaktbereich für jeden Signalkontakt zu gestatten. Die vordere Fläche des dielektrischen Gehäuses **132** bildet die Eingriffsfläche des Verbinders und enthält Löcher, um die Messer **106** vom Basisverbinder aufzunehmen, wie im Fachgebiet bekannt ist. Die Wände der Öffnung **426** schützen den Gegenkontaktbereich.

[0052] Bei der veranschaulichten Ausführung weist der Boden der Öffnung **426** eine Vertiefung **454** auf, die darin ausgebildet ist. Die Abschirmplatte **10** ist durch die Vertiefung **454** sichtbar. Wenn die Verbinderteile in Eingriff gebracht werden, gelangt ein Messer **106** in die Öfnnung **426** durch die vorderen Eingriffsfläche und wird gegen den Boden der Öffnung **426** durch einen Signalkontakt **124** gepresst. Daher wird eine Vertiefung **454** zwischen dem Messer **106** und der Abschirmung vorhanden sein, wobei ein Luftraum verbleibt. Der durch die Vertiefung **454** gebildete Luftraum erhöht die Impedanz des Signalweges in der Nähe der Eingriffsfläche, die anderenfalls ein Abschnitt des Signalweges mit niedriger Impedanz ist. Es ist wünschenswert, dass die Impedanz des Signalweges durchgängig gleichmäßig ist.

[0053] Die Schlitze **410** werden geformt, um die Schlitze **332** und die Abschirmanschlussbrückenkontakte **126** freizulegen. Die Schlitze **410** nehmen Abschirmplatten **116** vom Basisverbinder auf, was eine elektrische Verbindung zu den Abschirmanschlussbrückenkontakten **126** herstellt. Die Schlitze **410** weisen jeweils eine kegelförmige Fläche **412** entgegengesetzt dem Abschirmanschlussbrückenkontakt **126** auf. Während der Basis- und Tochterleiterplattenverbinder in Eingriff kommen, wird eine Abschirmplatte **116** in einen Schlitz **410** gelangen. Die Abschirmplatte **116** könnte in Richtung der kegelförmigen Fläche **412** durch die Federwirkung der Abschirmanschlussbrückenkontakte **126** gepresst werden. Die Konizität der kegelförmigen Fläche **412** fahrt die Vorderkante der Basisabschirmplatte **116** in eine Position am entfernten Ende des Schlitzes **410**, wodurch ein Stoßen der Abschirmplatte während des Eingriffes der Verbinder verhindert wird.

[0054] Das Loch **430** wird im dielektrischen Gehäuse **132** belassen, um einen Zugang zum Ring **16** für den Zweck des Trennens des Befestigungsstreifens **14a** von der Abschirmplatte **10** zu gestatten. Das Trennen der Befestigungsstreifen nahe der Signal- und Erdungskontakte verringert die Stümpfe, die an den Signal- und Erdungselementen haften. Die Stümpfe sind manchmal bei hohen Frequenzen unerwünscht, weil sie die elektrischen Eigenschaften des Bauelementes verändern.

[0055] In Fig. 5 wird ein Signalkontaktrohling **510** gezeigt. Der Signalkontaktrohling **510** wird aus einer langen Metallplatte gestanzt und geformt. Zahlreiche

Signalkontaktrohlinge werden aus einer Metallplatte gebildet, wobei die Signalkontaktrohlinge auf Trägerstreifen **512** zusammengehalten werden. Die Trägerstreifen **512** können Löcher für das Weiterschalten umfassen, oder um anderweitig die Handhabung bei den Trägerstreifen zu erleichtern.

[0056] Wie in Fig. 5 gesehen werden kann, wird jeder der Signalkontakte gestanzt und geformt, um den erforderlichen Gegenkontaktbereich **124** und das Kontaktlötende **128** aufzuweisen. Außerdem weist jeder Signalkontakt einen Zwischenabschnitt **518** auf, der den Kontaktbereich und das Kontaktlötende verbindet.

[0057] Wie sie anfangs gebildet werden, werden die Signalkontakte mit Befestigungsstreifen **516** zusammengehalten und an den Trägerstreifen mit den Befestigungsstreifen **514** gehalten. Diese Befestigungsstreifen liefern eine mechanische Stabilität für den Signalkontaktrohling, während der Verbinder zusammengebaut wird. Sie müssen jedoch abgetrennt werden, bevor der Verbinder verwendet wird. Anderenfalls würden sie die Signalkontakte kurzschließen. Ein Verfahren zum Abtrennen der Befestigungsstreifen wird in Verbindung mit Fig. 7 gezeigt.

[0058] Der Signalkontaktrohling **510** wird vorzugsweise aus Metall gestanzt. Ein Metall, das traditionell beim Verbinder verwendet wird, wird bevorzugt, wobei auf Kupfer basierende Berylliumlegierungen und Phosphorbronze geeignete Metalle sind. Abschnitte der Signalkontakte, insbesondere der Kontaktbereich, können mit Gold beschichtet werden, wenn es gewünscht wird, um die Oxidation zu verringern und die Zuverlässigkeit der elektrischen Verbindungen zu verbessern.

[0059] Die Signalkontakte umfassen ebenfalls Vorsprünge **520**. Wie es vorangehend beschrieben wird, werden die Signalkontakte in Kanälen **422** im dielektrischen Gehäuse **132** angeordnet. Die Vorsprünge **520** ergreifen die Wände der Kanäle **422**, um die Signalkontakte an Ort und Stelle zu halten.

[0060] Beim nächsten Schritt des Herstellungsvorganges wird der Signalkontaktrohling **510** über das dielektrische Gehäuse **132** gelegt, wie in Fig. 4 gezeigt wird. Die Platte **120** in diesem Herstellungszustand wird in Fig. 6 gezeigt. Man beachte, dass die Löcher in den Trägerstreifen **12** und **512** benutzt werden, um die Signalkontakte mit den Trägerstreifen für die Abschirmung **10** auszurichten. Weil der Formvorgang, der das dielektrische Gehäuse **132** über der Abschirmung **10** formte, ebenfalls auf den Löchern im Trägerstreifen **12** basierte, wird eine genaue Ausrichtung aller Teile des Verbinders bewirkt. Die Werkzeuge, um die Signalkontakte in die Kanäle **422** zu pressen, können ebenfalls jene Löcher für das Positionieren verwenden.

[0061] In Fig. 7 wird das Abtrennen der Befestigungsstreifen veranschaulicht. Jene Befestigungsstreifen **514**, die sich über das dielektrische Gehäuse **132** hinaus erstrecken, können leicht an einer Stelle außerhalb des Gehäuses **132** abgeschert werden. Vorzugsweise werden sie so nahe am Gehäuse wie möglich abgeschert.

[0062] Jeder der Befestigungsstreifen **516**, der intern zum dielektrischen Gehäuse **132** ist, gelangt über ein Loch **22**. Ein Werkzeug kann durch das Loch eingesetzt werden, wodurch die Befestigungsstreifen **516** abgetrennt werden.

[0063] Danach wird die Platte einem zweiten Formvorgang unterworfen. Bei diesem Vorgang wird der Hohlraum **450** gefüllt, um ein dielektrisches Gehäuse **134** zu bilden (Fig. 2). Die Öffnungen **426** werden jedoch nicht gefüllt, um zu gestatten, dass sich die Gegenkontaktbereiche **124** ungehindert bewegen und die erforderliche Eingriffskraft liefern.

[0064] Fig. 8 zeigt die Platten **120**, die in einem Verbinder montiert sind, der mit einem Basisverbinder in Eingriff ist. Die Messer **106** kommen mit den Signalkontakten **124** in Eingriff. Die Basisabschirmplatten **116** sind innerhalb der Schlitze **410** und kommen mit Abschirmanschlussbrückenkontakten **126** in Eingriff.

[0065] Bei der veranschaulichten Ausführung weisen die Abschirmplatten **116** eine Vielzahl von Schlitzen **812** auf, um längs der oberen Ränder der Abschirmplatten **116** Verzahnungen zu bilden. Jeder der Schlitze **812** kommt mit einem flachen Bereich **331** in Eingriff (Fig. 3), der im Schlitz **410** freigelegt bleibt (Fig. 4), wenn das Gehäuse **132** geformt wird. Die Schlitze **812** verringern die erforderliche Tiefe der Schlitze **332**, die in der Abschirmplatte **10** (Fig. 3) gebildet werden, gestatten aber, dass die Abschirmplatten **116** in den Bereichen länger sind, wo sie mit den Abschirmanschlussbrückenkontakten **126** in Eingriff kommen. Das Verringern der erforderlichen Tiefe der Schlitze **332** verbessert die mechanische Integrität der Platte. Das Zulassen von längeren Abschirmplatten verstärkt den Grad des „vorverlegten Eingriffes", was wünschenswert sein kann. Der vorverlegte Eingriff betrifft den Abstand zwischen der Stelle, wo die Erdungskontakte in Eingriff kommen und die Signalkontakte in Eingriff kommen, während die Tochterleiterplatten- und Basisverbinder während des Eingriffes des Verbinders zusammengedrückt werden.

[0066] In Fig. 9 wird eine in Eingriff gekommene Platte **120** von der Abschirmseite gezeigt. Wie es vorangehend beschrieben wird, wird das dielektrische Gehäuse **132** auf die obere Fläche der Abschirmung **10** geformt. Daher ist auf der Seite der Platte **120**, die in Fig. 9 sichtbar ist, die untere Fläche **910** der Abschirmung **10** sichtbar. Erhabene Abschnitte **330** (Fig. 3) und erhabene Rippen **333** (Fig. 3) auf der

oberen Fläche der Abschirmung **10** bilden Vertiefungen auf der unteren Fläche **910**. Diese Vertiefungen werden während des Formens des dielektrischen Gehäuses **132** mit Dielektrikum gefüllt, wobei dielektrische Bereiche **912** verbleiben. Die dielektrischen Bereiche **912** dienen mehreren Zwecken. Sie wirken mit dem Kunststoff zusammen, der die Löcher **26** gefüllt hat (Fig. 3), um das dielektrische Gehäuse **132** mit der Abschirmplatte **10** entlang des oberen Randes der Platte **120** sicher zu halten. Sie isolieren ebenfalls die Abschirmplatte **10** von den Signalkontakten **124** in einer benachbarten Platte. Daher verringern sie die Wahrscheinlichkeit, dass die Signalkontakte gegen Erde kurzgeschlossen werden.

[0067] In Fig. 10 wird eine alternative Ausführung des Basisverbinders gezeigt. Bei dieser Ausführung wird die Abdeckung **1002** aus einem leitenden Material gebildet. Bei der bevorzugten Ausführung ist das leitende Material ein Metall, wie beispielsweise Zinkdruckguss. Möglicherweise ist das Metall mit Chromat oder Nickel beschichtet, um eine anodische Oxidation zu verhindern.

[0068] Um zu verhindern, dass die Messer an der leitenden Abdeckung kurzgeschlossen werden, können dielektrische Distanzstücke in die Abdeckung **1002** eingesetzt werden, und danach können die Messer **106** in die Distanzstücke eingesetzt werden. Bei der bevorzugten Ausführung werden die dielektrischen Streifen in die Löcher **1012** im Boden der Abdeckung **1002** gedrückt. Jeder dielektrische Streifen ist aus Kunststoff geformt und umfasst Stopfen **1014** auf der unteren Fläche, um eine Presspassung mit den Löchern **1012** zu bewirken. Die Löcher **1016** in den dielektrischen Streifen **1010** nehmen die Messer **106** auf. Die dielektrischen Streifen **1010** vereinfachen die Herstellung im Vergleich zu den traditionellen dielektrischen Distanzstücken.

[0069] Es gibt mehrere Vorteile bei einem Verbinder, der so hergestellt wird, wie es vorangehend beschrieben wird. Ein Vorteil ergibt sich aus dem mehrstufigen Formverfahren. Der Abstand zwischen den Signalkontakten und der Erdungsfläche, die durch die Abschirmung **10** gebildet wird, wird sehr gründlich kontrolliert. Der kontrollierte Abstand führt zu einer besseren Impedanzsteuerung, die wünschenswert ist.

[0070] Als ein weiterer Vorteil verringert das Formen des dielektrischen Gehäuses auf die Abschirmplatte **10** die Gesamtdicke der Platten, wodurch ein Verbinder mit höherer Packungsdichte hergestellt werden kann.

[0071] Ebenfalls gestattet das Formen von dielektrischem Material über dielektrischem Material Vorteile während der Herstellung des Verbinders. Der Umfang des zweiten dielektrischen Gehäuses **134** überdeckt Stellen, wo das erste dielektrische Gehäuse **132** bereits geformt ist. Der Umfang des dielektrischen Gehäuses **134** wird geformt, wo eine Wand einer Form den Fluss des Kunststoffmaterials während des Formvorganges absperrt. Wenn das zweite dielektrische Gehäuse **132** geformt wird, wird daher die Form nach unten auf das dielektrische Gehäuse **132** festgeklemmt. Eine geringere Genauigkeit ist beim Formvorgang erforderlich, und es kann ebenfalls eine größere Formlebensdauer erwartet werden, wenn die Form unten auf dem Kunststoff festklemmt, wie es der Fall ist, wenn das zweite dielektrische Gehäuse **134** geformt wird.

[0072] Ein weiterer Vorteil ist, dass die Herstellung von Platten mittels eines Vorganges des Darüberformens gestattet, dass eine Gruppe von Verbindern bei unterschiedlichen Abständen zwischen den senkrechten Reihen von Kontakten billig hergestellt werden kann. Der Abstand zwischen den senkrechten Reihen kann verändert werden, indem die Dicke des darübergeformten Teils **134** verändert wird. Eine Vergrößerung des Abstandes könnte beispielsweise erfolgen, um ein Übersprechen zu reduzieren, und um dadurch die Geschwindigkeit des Verbinders zu vergrößern. Es könnte ebenfalls wünschenswert sein, den Abstand zu vergrößern, um zu gestatten, dass Leiterbahnen von 0,25 mm (10 mil) eher zum Verbinder geführt werden können als die normaleren 0,2 mm (8 mil) Leiterbahnen. Während die Arbeitsgeschwindigkeiten größer werden, sind manchmal dickere Leiterbahnen erforderlich. Bei Verwendung der offenbarten Konstruktion können die gleichen Werkzeuge verwendet werden, um das Gehäuse **132**, die Abschirmungen **10** und den Signalkontaktrohling **510** zu formen, ungeachtet der Dicke der Platte. Ebenfalls könnten die gleichen Montagewerkzeuge verwendet werden. Es ist ein wichtiger Vorteil, dass so viel betreffs des Herstellungsverfahrens und der Werkzeuge für Verbinder bei unterschiedlichen Abständen gemeinsam ist.

[0073] Außerdem hält der Zweistufenformvorgang die Kontaktlötenden im isolierenden Gehäuse für sowohl die Abschirm- als auch Signalkontakte sicher. Das sichere Halten der Kontaktlötenden im Gehäuse ist besonders für Verbinder wichtig, die mit Presspassungskontakten hergestellt werden. Die Kontakte nehmen eine sehr hohe Kraft auf, wenn der Verbinder auf eine Leiterplatte montiert wird. Wenn die Lötenden nicht sicher im isolierenden Gehäuse gehalten werden, besteht eine erhöhte Gefahr, dass sich die Kontakte verbiegen oder zerbröckeln, was eine angemessene Verbindung des Verbinders mit der Leiterplatte verhindert.

[0074] Während diese Erfindung speziell mit Hinweis auf deren bevorzugten Ausführungen gezeigt und beschrieben wird, werden jene Fachleute verstehen, dass darin verschiedene Veränderungen hin-

sichtlich der Form und Details vorgenommen werden können, ohne dass man vom Bereich der Erfindung abweicht, der von den als Anhang beigefügten Patentansprüchen eingeschlossen wird.

[0075] Beispielsweise wird die Erfindung beschrieben, wie sie bei einem rechtwinkeligen Basisverbinder zur Anwendung kommt. Die Erfindung könnte bei Verbindern in anderen Konfigurationen angewandt werden, wie beispielsweise Mezzanin- oder Stapelverbindern, die Leiterplatten verbinden, die parallel zueinander sind. Die Erfindung könnte ebenfalls zur Anwendung gebracht werden, um Kabelverbinder herzustellen. Um einen Kabelverbinder herzustellen, würden die Kontaktlötenden, die verwendet werden, um den Verbinder zu befestigen, durch Kabel ersetzt werden. Oftmals werden Kabel abgeschirmt und die Abschirmungen der Kabel an den Abschirmungen der Verbinder angebracht. Oftmals biegen sich die Signalkontakte der Stromverbinder nicht unter rechten Winkeln. Die Eingriffsfläche eines Stromverbinders ist jedoch im Allgemeinen die gleiche wie die Eingriffsfläche des rechtwinkeligen Tochterleiterplattenverbinders. Infolge der gleichen Anschlussfläche wird gestattet, dass der Stromverbinder in den gleichen Basisverbinder gesteckt wird wie der Tochterleiterplattenverbinder.

[0076] Als ein weiteres Beispiel könnte die Reihenfolge der verschiedenen Herstellungsschritte ausgetauscht werden. Die Reihenfolge, in der die Befestigungsstreifen **514** und **516** abgetrennt werden, ist für die Herstellung des Verbinders nicht kritisch. Die Befestigungsstreifen **514** könnten zuerst abgetrennt werden, und danach könnten die Trägerstreifen **512** entfernt werden, bevor das dielektrische Gehäuse **134** geformt wird. Auf diese Weise können die Befestigungsstreifen entfernt werden, wenn die Trägerstreifen **512** entfernt werden.

[0077] Gleichfalls könnten die Trägerstreifen **516** abgetrennt werden, um die Signalkontakte in einen Signalkontaktrohling zu trennen, bevor das dielektrische Gehäuse **134** geformt wird. Wenn die Trägerstreifen **516** nach dem Formvorgang abgetrennt werden, bleiben die Löcher **22** freigelegt.

[0078] Es sollte außerdem erkannt werden, dass die spezifischen Formen der Kontaktelemente erläuternd sind. Verschiedene Formen, Größen und Positionen für die Kontaktelemente wären in einem Verbinder entsprechend der Erfindung geeignet. Beispielsweise muss das Abschirmelement nicht eine einzelne Platte sein, sondern könnte statt dessen aus einer Vielzahl von Abschirmsegmenten gebildet werden. Außerdem könnten Schlitze in der Abschirmplatte gebildet werden, um die Resonanz in der Platte zu verringern.

[0079] Als ein weiteres Beispiel sollte erkannt werden, dass die Nasen, wie beispielsweise **18** und **322**, als Befestigungsmerkmale gezeigt werden, die dazu dienen, die dielektrischen Gehäuse an der Abschirmplatte **10** zu befestigen. Die Löcher **26** sind ebenfalls Veranschaulichungen der Befestigungsmerkmale. Die Nasen könnten gegen Löcher ausgetauscht werden. Alternativ könnten Befestigungsmerkmale mit anderen Formen zur Anwendung gebracht werden.

[0080] Es könnte ebenfalls thermoplastisches Material im Allgemeinen für das Spritzgießen verwendet werden, das für die Formschritte zur Anwendung gebracht werden kann. Andere Arten des Formens könnten zur Anwendung gebracht werden. Außerdem könnte das dielektrische Gehäuse **134** nicht durch Formen hergestellt werden. Es könnte eher durch Füllen des Hohlraumes **450** mit einem Epoxid oder einem anderen abbindbaren Material hergestellt werden.

[0081] Noch weitere Abwandlungen sind möglich. Bei der vorangehend beschriebenen Ausführung wird eine Metallversteifung gezeigt. Andere Verfahren des Befestigens der Platten sind möglich, einschließlich des Befestigens dieser an Kunststoffstützstrukturen oder des anderweitigen Sicherns der Platten miteinander.

[0082] Außerdem weist der Verbinder, der als ein Beispiel der bevorzugten Ausführung verwendet wird, Kontakte in Paaren auf, um einen Differentialverbinder zu bilden. Für Hochleistungsdifferentialverbinder, insbesondere Verbinder, die Signale über Gbits pro Sekunde führen, kann ein Bitversatz (d.h., eine Differenz bei den Laufzeiten) zwischen den Leitungen im Paar eine bedeutende Signalverzerrung hervorrufen. Im U.S.Patent 6379188 wird ein Verfahren zur Eliminierung des Bitversatzes gezeigt. Der Bitversatz wird durch selektives Anordnen von Ausschnitten für Luft um die Signalkontakte herum ausgeglichen. Weil sich die Ausbreitungsgeschwindigkeit des Signals in Luft verändert, verringert das Anordnen von Luft um nur einen der Kontakte in einem Paar den Bitversatz. Die Ausschnitte, wie sie im vorangehend erwähnten Patent gezeigt werden, können leicht hergestellt werden, indem Vertiefungen im Boden des Hohlraumes belassen werden, der die Zwischenabschnitte der Signalkontakte aufnimmt. Ausschnitte könnten ebenfalls belassen werden, wenn das zweite isolierende Gehäuse geformt wird.

[0083] Es sollte ebenfalls erkannt werden, dass alle beschriebenen aufgelisteten charakteristischen Merkmale und Vorteile gleichzeitig vorhanden sein müssen, um einen Vorteil aus der Erfindung zu ziehen.

Patentansprüche

1. Verfahren zur Herstellung einer Platte für eine

Verwendung in einem elektrischen Verbinder, das die folgenden Schritte aufweist:
a) Bereitstellen einer Abschirmplatte (**10**) mit einer oberen Fläche und einer unteren Fläche, wobei die Abschirmplatte (**10**) eine Vielzahl von Kontaktlötenden (**122**) aufweist, die sich von dort erstrecken, wobei die Kontaktlötenden (**122**) mit der Abschirmplatte (**10**) durch einen Abschnitt (**318**) verbunden werden, der gebogen ist, um das Kontaktlötende (**122**) über die Ebene der Abschirmplatte (**10**) anzuheben;
b) Formen eines ersten dielektrischen Gehäuses (**132**) auf der Abschirmplatte (**10**), wobei das erste dielektrische Gehäuse (**132**) einen Hohlraum (**450**) und eine Vielzahl von Öffnungen (**426**) aufweist, die sich vom Hohlraum (**450**) erstrecken, und wobei das erste dielektrische Gehäuse (**132**) ebenfalls die gebogenen Abschnitte (**318**) einschließt, die die Kontaktlötenden (**122**) an der Abschirmplatte (**10**) befestigen;
c) Bereitstellen einer Vielzahl von Signalkontakten (**124**), wobei ein jeder der Signalkontakte ein Kontaktlötende (**128**), einen Kontaktbereich (**124a**-d) und einen Zwischenabschnitt (**518**) aufweist, der das Kontaktlötende (**128**) und den Kontaktbereich (**124a**-d) verbindet;
d) Einsetzen der Vielzahl von Signalkontakten (**124**) in das erste dielektrische Gehäuse (**132**) mit den Zwischenabschnitten (**518**) in den Hohlraum (**450**), den Kontaktbereichen (**124a**-d) in eine der Vielzahl von Öffnungen (**426**), und wobei sich die Kontaktlötenden (**128**) vom ersten dielektrischen Gehäuse (**132**) erstrecken; und
e) Formen eines zweiten dielektrischen Gehäuses (**134**) im Wesentlichen über dem Hohlraum (**450**), wodurch die Abschirmung (**10**), das erste dielektrische Gehäuse (**132**) und die Signalkontakte (**124**) zusammen als eine Platte gesichert werden, wodurch die Kontaktlötenden (**128**) der Abschirmplatte (**10**) und die Signalkontakte (**124**) gesichert werden.

2. Verfahren nach Anspruch 1, bei dem die Abschirmplatte (**10**) eine erste Vielzahl von Nasen (**18**) aufweist, die über die obere Fläche der Abschirmplatte (**10**) gebogen sind, wobei die Nasen (**18**) im ersten dielektrischen Gehäuse (**132**) eingeschlossen sind.

3. Verfahren nach Anspruch 2, das außerdem die folgenden Schritte aufweist: Bereitstellen einer zweiten Vielzahl von Nasen (**320**) auf der oberen Fläche der Abschirmplatte (**10**); und Formen des ersten dielektrischen Gehäuses (**132**), um einen Ausschnitt (**424**) um die zweite Vielzahl von Nasen (**320**) bereitzustellen, und um die zweite Vielzahl von Nasen (**320**) im zweiten dielektrischen Gehäuse (**134**) einzuschließen.

4. Verfahren nach Anspruch 1, bei dem das Formen Bereiche (**426**) im Hohlraum (**450**) des ersten dielektrischen Gehäuses (**132**) bereitstellt, um die Kontaktbereiche (**124a**-d) der Signalkontakte (**124**) aufzunehmen.

5. Verfahren nach Anspruch 1, das außerdem das Bereitstellen eines erhabenen Abschnittes (**330**) auf der Abschirmplatte (**10**) aufweist, der eine Vertiefung unterhalb der oberen Fläche bildet, wobei der erhabene Abschnitt (**330**) darin ein Loch (**26**) aufweist, und bei dem das Formen des ersten dielektrischen Gehäuses (**132**) einen ersten Abschnitt des ersten dielektrischen Gehäuses (**132**) über dem erhabenen Abschnitt (**330**) und einen zweiten Abschnitt des ersten dielektrischen Gehäuses (**132**) in der Vertiefung und im Loch (**26**) bereitstellt.

6. Verfahren nach Anspruch 1, bei dem die Abschirmplatte (**10**) einen erhabenen Abschnitt (**330**) aufweist und das erste dielektrische Gehäuse (**132**) vertiefte Bereiche (**454**) im Boden des Hohlraumes umfasst, wodurch Lufträume zwischen den Signalkontakten und dem erhabenen Abschnitt (**330**) der Abschirmplatte (**10**) bereitgestellt werden.

7. Verfahren nach Anspruch 1, bei dem das Einsetzen der Vielzahl von Signalkontakten (**124**) das Pressen der Signalkontakte (**124**) in Kanäle (**422**) im ersten dielektrischen Gehäuse (**132**) aufweist.

8. Elektrischer Verbinder, der aus Platten montiert wird, wobei die Platten aufweisen:
a) eine Abschirmplatte (**10**) mit einer oberen Fläche und einer unteren Fläche, wobei die Abschirmplatte (**10**) eine Vielzahl von Kontaktlötenden (**122**) aufweist, die sich von dort erstrecken, wobei die Kontaktlötenden (**122**) mit der Abschirmplatte (**10**) durch einen Abschnitt (**318**) verbunden werden, der gebogen ist, um das Kontaktlötende (**122**) über die Ebene der Abschirmplatte (**10**) anzuheben;
b) ein erstes dielektrisches Gehäuse (**132**), das auf der Abschirmplatte (**10**) geformt wird, wobei das erste dielektrische Gehäuse (**132**) einen Hohlraum (**450**) und eine Vielzahl von Öffnungen (**426**) aufweist, die sich vom Hohlraum (**450**) erstrecken, und wobei das erste dielektrische Gehäuse (**132**) ebenfalls die gebogenen Abschnitte (**318**) einschließt, die die Kontaktlötenden (**122**) an der Abschirmplatte (**10**) befestigen;
c) eine Vielzahl von Signalkontakten (**124**), wobei ein jeder der Signalkontakte ein Kontaktlötende (**128**), einen Kontaktbereich (**124a**-d) und einen Zwischenabschnitt (**518**) aufweist, der das Kontaktlötende (**128**) und den Kontaktbereich (**124a**-d) verbindet, wobei die Vielzahl von Signalkontakten (**124**) in das erste dielektrische Gehäuse (**132**) eingesetzt wird, mit den Zwischenabschnitten (**518**) in den Hohlraum (**450**), den Kontaktbereichen (**124a**-d) in eine der Vielzahl von Öffnungen (**426**) und wobei sich die Kontaktlötenden (**128**) vom ersten dielektrischen Gehäuse (**132**) erstrecken; und
d) ein zweites dielektrisches Gehäuse (**134**), das im Wesentlichen über dem Hohlraum (**450**) geformt wird, wodurch die Abschirmung (**10**), das erste dielektrische Gehäuse (**132**) und die Signalkontakte

(**124**) zusammen als eine Platte gesichert werden, wodurch die Kontaktlötenden (**122**) der Abschirmplatte (**10**) und die Signalkontakte (**124**) gesichert werden.

9. Elektrischer Verbinder nach Anspruch 8, bei dem die Abschirmplatte (**10**) einen erhabenen Abschnitt (**330**) aufweist, der eine Vertiefung unterhalb der oberen Fläche bildet, wobei der erhabene Abschnitt darin ein Loch (**26**) aufweist, und bei dem ein erster Abschnitt des ersten dielektrischen Gehäuses (**132**) über dem erhabenen Abschnitt bereitgestellt wird, und bei dem ein zweiter Abschnitt des ersten dielektrischen Gehäuses (**132**) in der Vertiefung und im Loch (**26**) bereitgestellt wird.

10. Elektrischer Verbinder nach Anspruch 9, bei dem der Verbinder eine Fläche aufweist, die so ausgeführt ist, dass sie zu einem zweiten Verbinder passt, und bei dem der erhabene Abschnitt (**330**) längs des Randes der Abschirmplatte (**10**) an der Fläche verläuft.

11. Elektrischer Verbinder nach Anspruch 8, bei dem die Abschirmplatte (**10**) einen erhabenen Abschnitt (**330**) aufweist und das erste dielektrische Gehäuse (**132**) vertiefte Bereiche (**454**) im Boden des Hohlraumes umfasst, wodurch Lufträume zwischen den Signalkontakten (**124**) und dem erhabenen Abschnitt (**330**) der Abschirmplatte (**10**) bereitgestellt werden.

12. Elektrischer Verbinder nach Anspruch 8, bei dem der Verbinder eine Fläche aufweist, die so ausgeführt ist, dass sie zu einem zweiten Verbinder passt und die Abschirmplatte (**10**) eine Vielzahl von Schlitzen (**332**) in denn Rand benachbart zu der Fläche aufweist.

Es folgen 10 Blatt Zeichnungen

Anhängende Zeichnungen

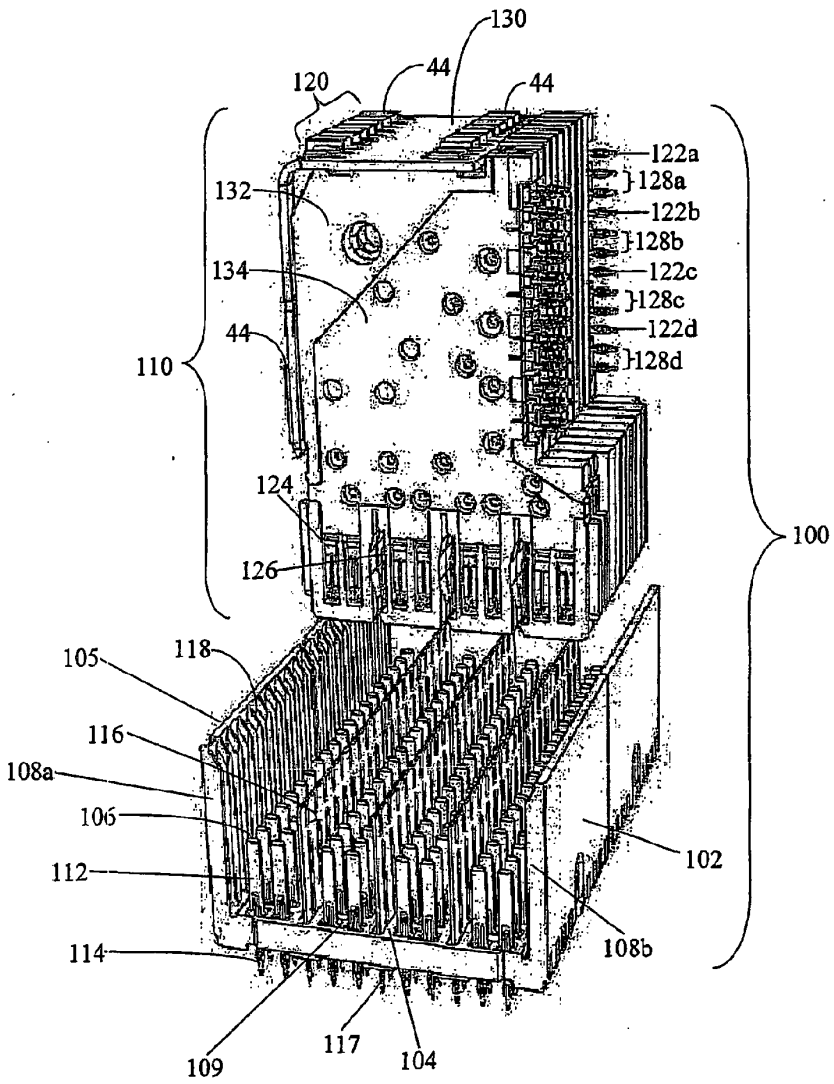

FIG. 1

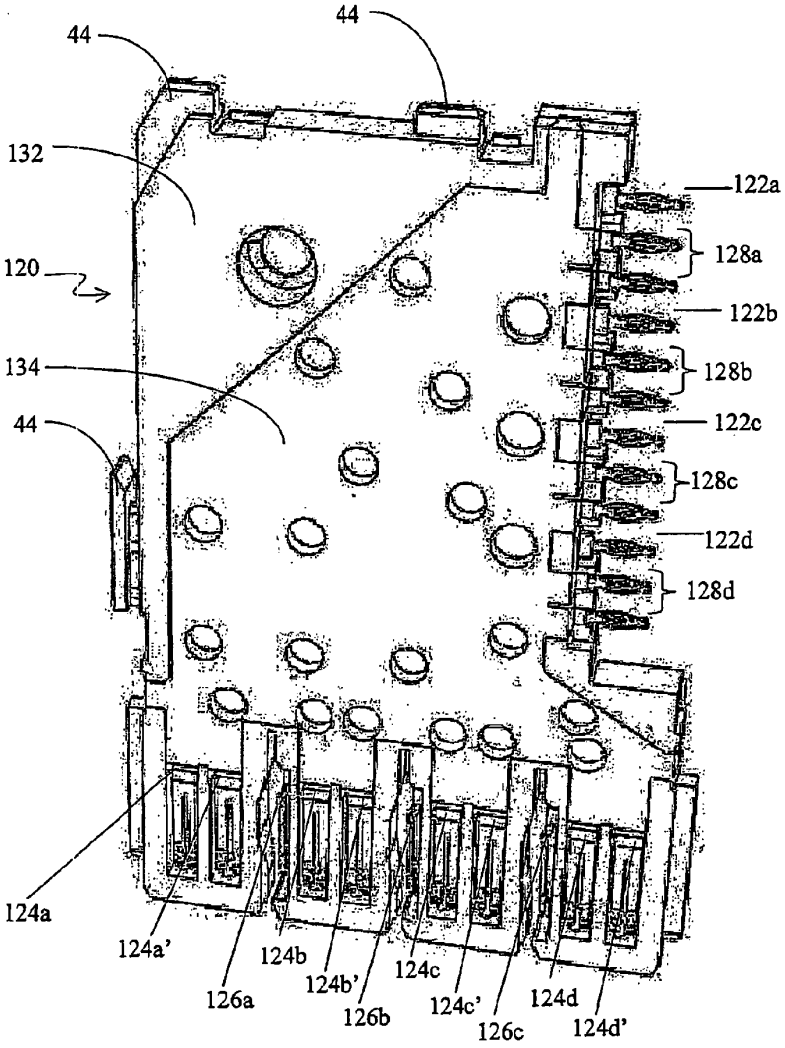
44
44
132
120
134
44
122a
128a
122b
128b
122c
128c
122d
128d
124a
124a'
126a
124b
124b'
126b
124c
124c'
126c
124d
124d'

FIG. 2

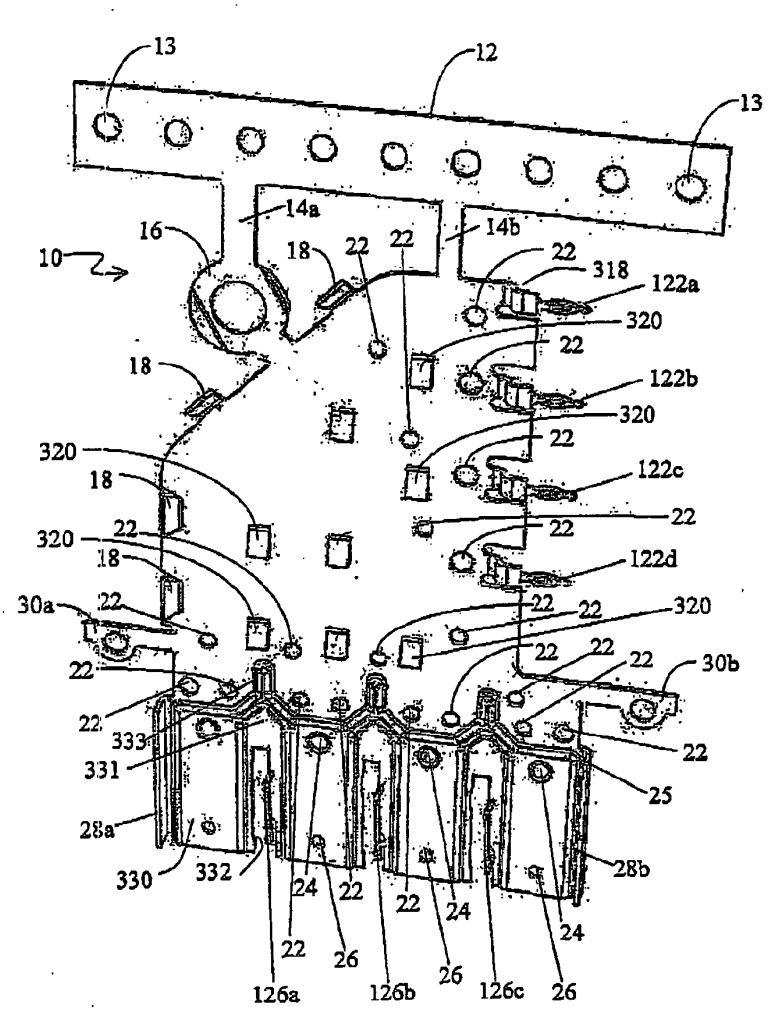
13
12
13
14a
14b
16
10
18
22
22
22
318
122a
320
22
18
122b
320
22
320
18
122c
22
22
320
18
22
22
122d
30a
22
22
22
320
22
22
22
30b
22
22
333
331
22
25
28a
28b
330
332
24
22
22
24
24
22
26
26
26
126a
126b
126c

FIG. 3

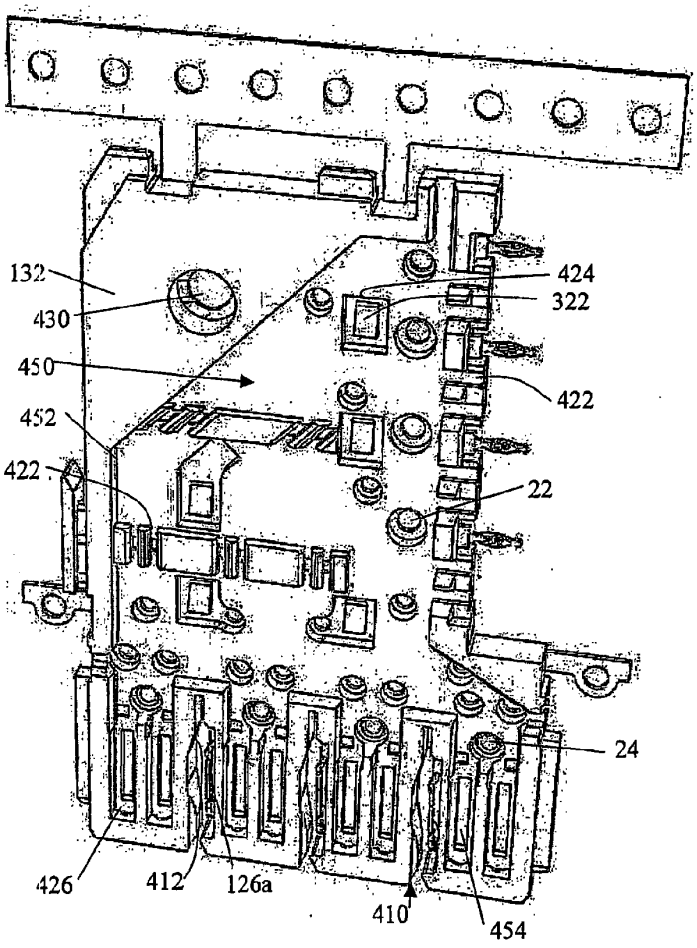

FIG. 4

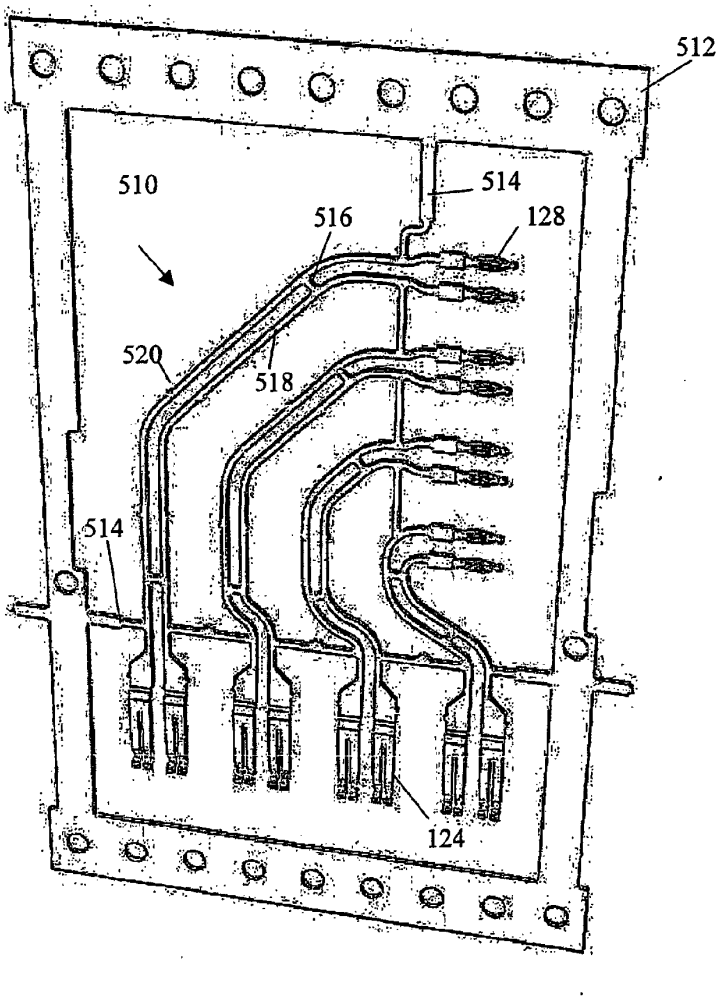

FIG. 5

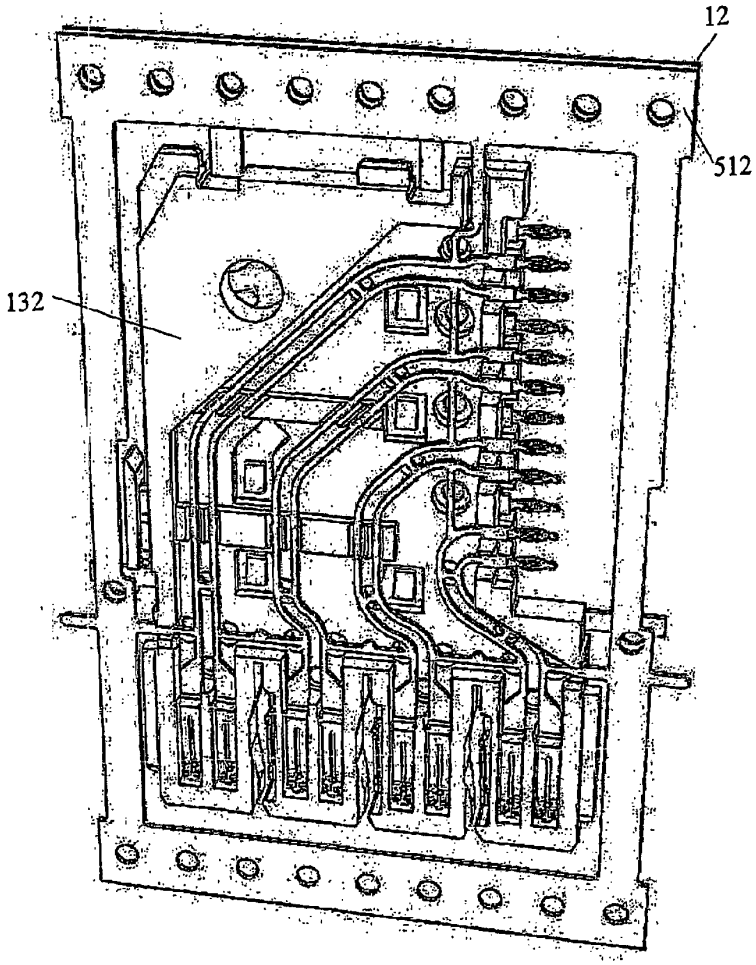

FIG. 6

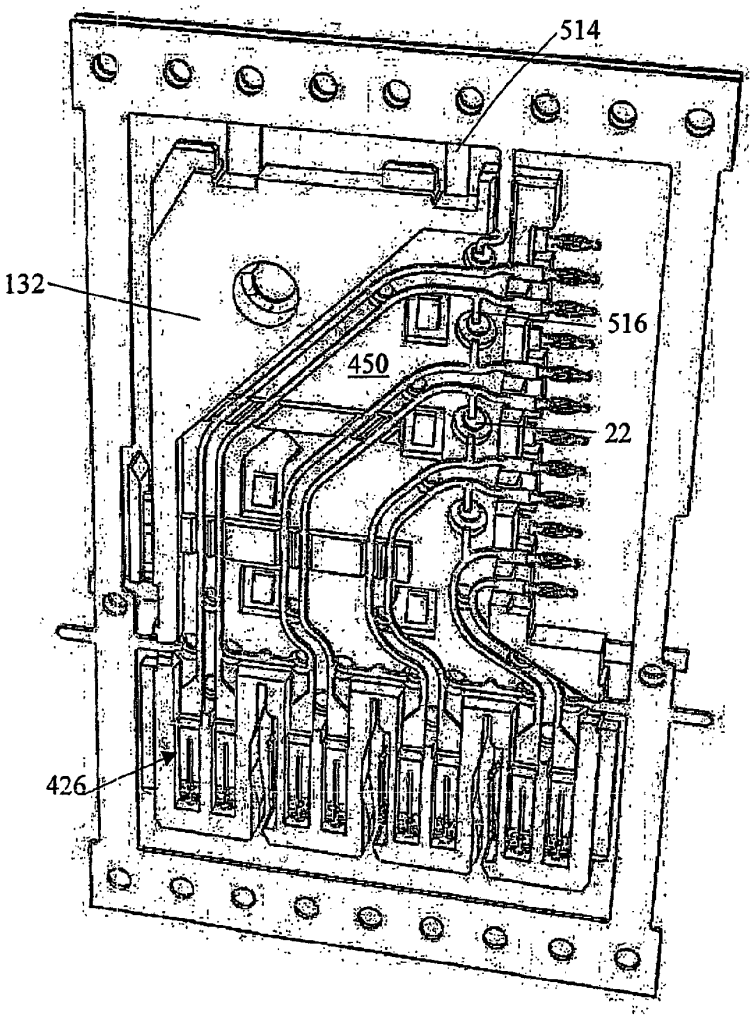

FIG. 7

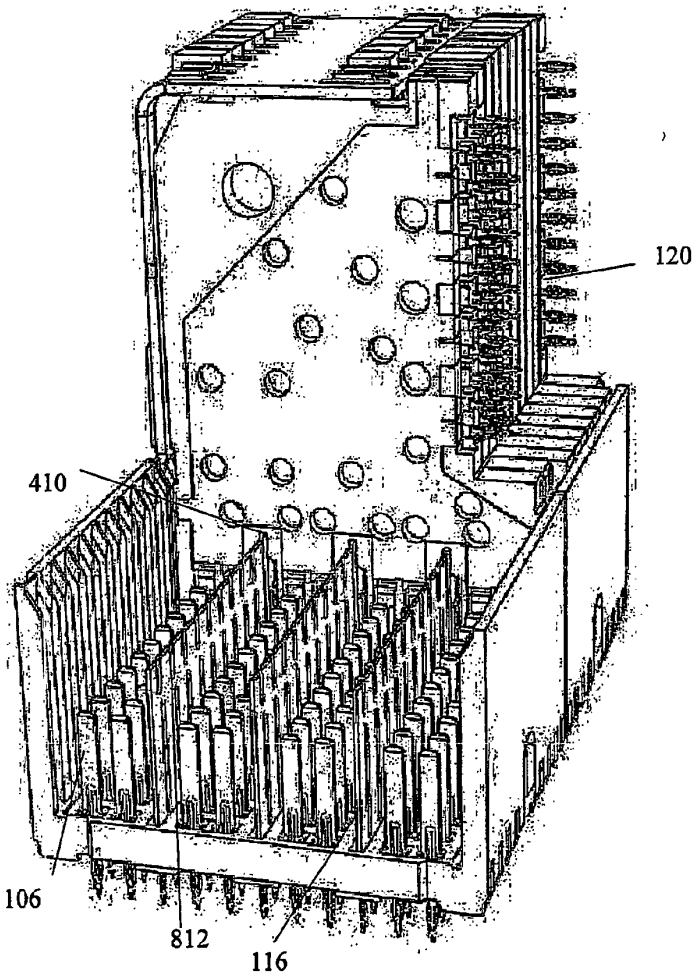

FIG. 8

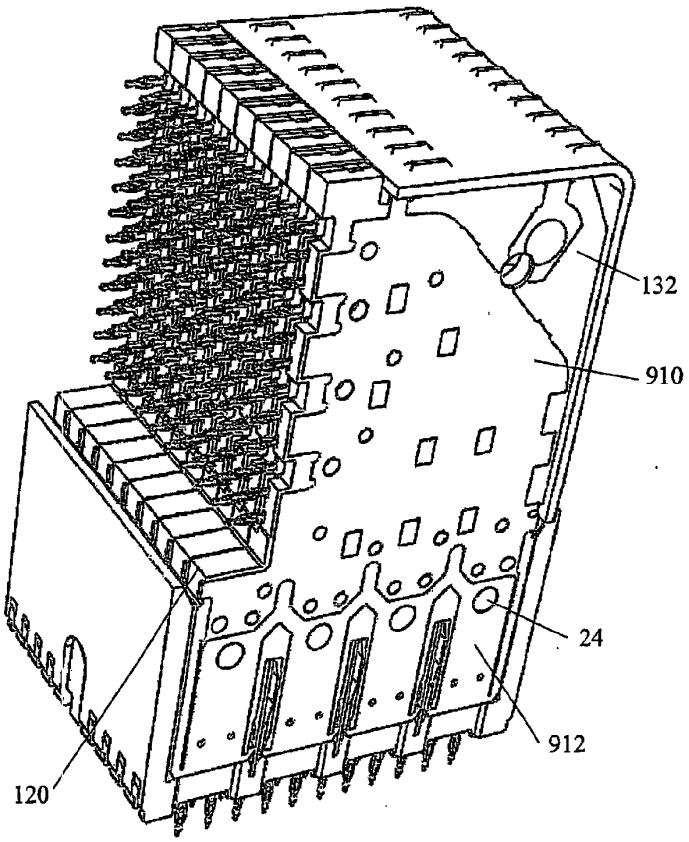

FIG. 9

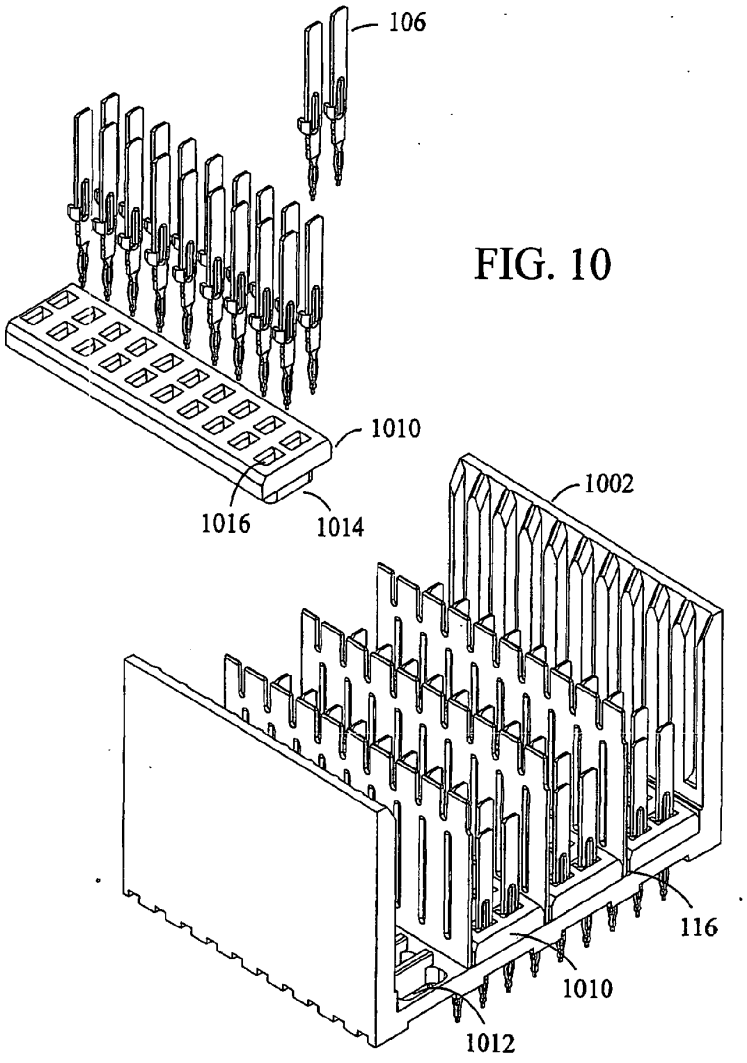

FIG. 10

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(54) **Shielded connectors and method for making the same**

(57) Methods and apparatus are disclosed for manufacturing and for providing electrical connectors having maximum shielding from electronic interference. Maximum shielding is inexpensively achieved by manufacturing a shield structure from a single piece of material in a manner yielding individual channels for shielding a contact terminal from the receptacle area to the tail area. Contact terminals are integrated into the shield structure via insertion molding to form a column connector module. A plurality of column connector modules are then inserted into an appropriately formed front housing. As described by the method of this invention, shielding from electronic interference occurs not only between adjacent terminals within a column structure, but also, between terminals contained in adjacent column connector modules.

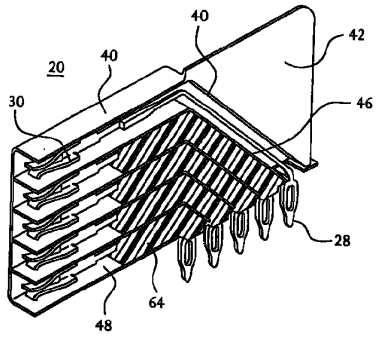


FIG. 6

EP 1 018 784 A1

Description

Related Applications

[0001] The present invention is related by subject matter to the invention disclosed in European application No._____, filed concurrently herewith on _____, 2000, entitled "Shielded Connector and Method for Manufacturing Same".

Field of the Invention

[0002] The present invention relates to electrical connectors and more particularly to shielded connectors and to a method of making connectors such that the connectors provide optimum shielding from electronic interference.

Background of the Invention

[0003] The transition from analog electronics to digital electronics has caused sweeping technological changes within telecommunications and electronic instrumentation industries. For example, as clock-speeds in digital circuitry increase, so do the challenges in maintaining signal integrity with respect to adjacent signals interfering with one another. Other driving forces, that have also created technical challenges, are the demand for miniaturization of electronic devices and the demand for increasing the number of discrete functions associated with each electronic device. The latter two driving forces results in the packing of multiple electronic functions within a smaller cabinet volume, i.e., within a smaller surface space on a printed circuit board (PCB) within the cabinet dimensions. The limited PCB surface space requires closer component spacing that can result in components electrically interfering with or being influenced by neighboring components. For example, the phenomenon of antenna and receiver (crosstalk) is well known in the art.

[0004] More specifically, older connector designs were based on the use of low frequency signals using relatively high voltage and steady state current levels in which the flow of the energy was evenly distributed over the total cross-section of a conductor. A result of the effective impedance to the flow of such energy was electrical resistance. By contrast, contemporary digital signals operate at much higher frequencies with signal amplitudes in the micro-volt level. With such high frequency signals, transmission of energy migrates to the outer "skin" of the conductor and can be transmitted. Consequently, the impedance of the interconnect becomes an important design parameter.

[0005] In recent years, equipment designers and users have become more sensitive to the problems raised by increases in clock speed (frequency) and miniaturization. To alleviate these problems, there has been a gradual design shift towards coaxial or pseudo-coaxial shielded components.

[0006] New connector designs provide shielded interconnects with characteristics that allow propagation of high speed signals while reducing cross talk. In such interconnects, the electronic signal element, i.e., the connector terminal path, is preferably enclosed by an equi-spaced air annulus bounded by a metal shield, air being a preferred dielectric.

[0007] Optimum coaxial performance is achieved by a cylindrically shaped connector having a minimum of cross-section change over the length of the interconnect. In such a connector, the distance between the center conductor and the shield preferably will be uniform over the length of the connector. Unfortunately, round, coaxial connectors are typically machine-turned and expensive to manufacture.

[0008] Other types of shielded connectors, are substantially rectangular in shape, as a result of stamping. Connectors assembled with stamped components are easier and more cost-effective to manufacture. Generally such stamped structures typically include rectangular-shaped internal contact terminals.

[0009] Shielding such rectangular components requires an equi-spaced dielectric annulus. By the very fact that the shield structure is rectangular, rather than circular, there is a natural deviation with respect to ideal coaxial shielding. The performance of such shielding is less optimal than that of the ideal coaxial shielding and is, therefore, referred to as pseudo-coaxial.

[0010] Right angle or horizontal connectors are commonly used for many backplane applications. Not uncommonly, such right angle connectors, are designed to be press-fit to a printed circuit board and contain multiple rows and columns. In manufacturing such connectors, the contact terminals are stitched into a housing after which the back end of the terminal, known as the tail, is bent. Such bending is usually done row by row. The disparity in tail length between each row causes a difference in the impedance path for adjacent terminals. The resultant cross-talk from the tail section of such a connector is approximately 30 to 35% of the total cross-talk for the mated connector. A significant part of the cross-talk is attributed to the close spacing of the contact terminals.

[0011] Hence, there still exists a need to design a right-angle connecter having reduced size without sacrificing shielding performance for high frequency signals.

Summary of the Invention

[0012] The above described problems are resolved and other advantages are achieved in a shielded electrical connector constructed by forming a shield from sheet material, fixing stamped terminals to the shield such that the terminals are positioned equal annular distances from the shield, whereby the terminals and the connector shield define a column connector module,

and by inserting a plurality of the shielded connector modules into an appropriately formed housing.

[0013] According to one aspect of the invention, the step of forming a shield is performed by first forming the sheet material into a planar portion and a leg portion wherein the leg portion is defined by a plurality of legs having a first position lying in the same plane as the planar portion and that extend from the planar portion. Next the legs are bent so that they are perpendicular to the first position thereby defining a second position. Then, the legs are bent again from the second position over and onto the planar portion thereby defining a third position, forming a plurality of channels having a receptacle receiving portion and a tail receiving portion.

[0014] In preferred embodiments of the invention, the sheet material is metal and the plurality of legs are secured to the planar portion of the stamped piece of sheet material.

[0015] In yet another embodiment of the invention, the plurality of legs have a plurality of protrusions and the planar portion of the stamped piece of sheet material has a plurality of apertures designed to cooperate with and matingly receive the plurality of protrusions. In such an embodiment, the step of bending the legs includes bending the legs so that they are perpendicular to the first position of the leg portion defining a second position and bending the legs from the second position over and onto the planar portion defining a third position whereby the apertures in the planar portion of the stamped flat piece of sheet material matingly receive the protrusions thereby forming a plurality of channels.

[0016] According to another aspect of the invention a terminal is provided within each channel, wherein each terminal is formed to receive a mating pin and wherein each terminal defines a tail portion that protrudes beyond the angular tail section. In such an embodiment, the terminals and channels are fixed to one another by an insert-molding process. In such an embodiment it is preferred to insert-mold in only the tail receiving portion. It is especially preferred for the insert-molding material to be a dielectric material.

[0017] In yet another embodiment of the invention, a lobe is formed on the planar portion of the sheet material, preferably by pressing the sheet material.

Detailed Description of the Drawings

[0018] The present invention will be better understood and its numerous objects and advantages will become apparent by reference to the following detailed description of the invention when taken in conjunction with the following drawings, in which:

Figure 1 is a perspective, partial section view of an electrical connector according to the invention;
Figure 1A is a flow chart of the processes by which the electrical connector of Figure 1 is made;
Figure 2 is a top planar view of a pattern formed in a flat piece of sheet metal;
Figures 3A-C show a connector housing made according to the method of the invention;
Figure 4A is a top planar view of a stamped and formed terminal for a five row module showing it's original pitch and still mounted on a carrier frame;
Figure 4B is a cross sectional view of the terminal of Figure 4A taken through line A-A of Figure 4A;
Figure 4C is a top planar view of the cut out terminal of Figure 4A after the pitch has been translated;
Figure 4D is a cross sectional view of the terminals of Figure 4C taken through line B-B of Figure 4C;
Figure 4E is a side planar view of the terminals of Figure 4C;
Figure 5A is a top planar view of the conductor housing fitted with terminals, defining a connector column;
Figure 5B is a vertical frontal view of the connector column of Figure 5A;
Figure 6 is a three-dimensional view of a connector column described in Figures 5A-B;
Figure 7 is a cross-sectional view of an electrical connector showing the connector column of Figure 6A inserted into a front housing; and
Figure 8 is a rear view of the electrical connector of Figure 7 showing a plurality of connector columns inserted into the front housing that comprises the electrical connector.

Detailed Description of Preferred Embodiments

[0019] A right-angled shielded connector and method of making the same, according to the present invention, will now be described with reference to the Figures. It will be appreciated that the description given herein with respect to the Figures is for exemplary purposes only and is not intended in any way to limit the scope of the invention. For example, the Figures describe a right-angled shielded connector and a method for making the same. However, the concepts disclosed herein have a much broader application to a much wider variety of connectors. The concepts disclosed with reference to this connector could also be employed, for example, with a straight connector.

[0020] Figure 1 shows a connector 10 constructed in accordance with the invention. Connector 10 comprises a front housing 12, wherein front housing 12 includes a front face 13 having a plurality of receptacle openings 14, and a plurality of connector columns 20 (only one is shown). Each connector column 20 includes a conductor shield 24 and terminals 26 for conducting electrical signals. Each conductor shield 24 includes a side spring 16 and an optional press-fit ground pin 18. Each terminal 26 also includes a press fit tail 28 and a receptacle portion 30. The plurality of the receptacle portions in the final assembled connector 10 are arranged in rows (horizontally) and in columns (vertically) to correspond to openings 14.

[0021] Figure 1A is a flow chart of the processes for making connector 10 of Figure 1. Processes A, B, and C are performed independently from each other, however, the products of processes B and C are required in process A as indicated by the dotted lines. In describing the processes for manufacturing connector 10, reference will also be made to Figures 2 through 5, wherein there is shown a series of top, plan and perspective views of connector 10 during various stages of manufacture.

[0022] As shown in Figure 1A, the process starts with a flat piece of sheet material 32 that is formed into a pattern 34 (Step 100). Preferably, the sheet material is metal. The pattern 34 is formed by cutting, stamping, or the like, into the shape as shown in Figure 2. At this stage, leg portion 37 lies in the same plane as planar portion 36.

[0023] Pattern 34 is then pressed at 110 to form desired three-dimensional characteristics the function of which will become readily apparent from the description herein. Figure 3A shows that, as a result of steps 100 and 110, the pressed sheet material pattern now comprises planar portion 36, a raised offset portion 40 (shown more clearly in Figure 6), a leg portion 37 consisting of a plurality of legs 38, and an extended portion shown as lobe 42.

[0024] As indicated in Figure 1A, legs 38 of conductor shield are bent at 120 first along axis y-y so that legs 38 are perpendicular to planar portion 36. Referring now to Figures 3a-c, two substantially 45 degree bends, B1 (Figure 3A) and B2 (Figure 3B), are then made in legs 38. In Figure 3C, legs 38 are finally bent over axis x-x and into contact with the planar portion 36 thus creating a plurality of equidistant channels 44 whose bottom portion is defined by planar portion 36 and whose walls comprise legs 38. The resulting angles of bends B1 and B2 are selected to create the desired equidistant channels. As a result of bends B1 and B2, channels 44 also define tail receiving portion 46 and a receptacle receiving portion 48.

[0025] Legs 38 are secured to planar portion 36 in order to more positively ensure that legs 38 are parallel to each other over their entire length, from tail receiving portion 46 to the receptacle receiving portion 48 thereby maintaining conformity in annular space within each channel. Such parallelism and conformity may be further assured in a particularly effective manner shown in Figure 3B. As shown in Figure 3B, planar portion 36 includes apertures 50, while legs 38 have protrusions 52 formed thereon. Apertures 50 and protrusions 52 are selectively located so that protrusions 52 will matingly cooperate with apertures 50 when legs 38 are bent around axis x-x onto planar portion 36. Preferably, protrusions 52 are adapted to be press-fit into apertures 50.

[0026] Lobe 42 can be used as a gripping or grasping section to hold a fully constructed connector column 20 (Figure 5A) during the assembly process for either fitting column 20 into an appropriately formed front housing 12 or for press-fit mass insertion into a PCB. The use of the grasping section allows for easy manipulation of column 20 and permits the column to withstand relatively high assembly forces.

[0027] Lobe 42 may also have attached side springs 16 (shown in Figure 1). If formed of electrically conductive material, side springs 16 operate to establish an electrical contact with an adjacent lobe thereby forming a continuous path across the plurality of lobes. This path, when utilized in conjunction with an optional press fit ground pin connector 18 (also shown in Figure 1) at the base of lobe 16, forms a ground through connector 10 to the PCB.

[0028] Referring to Figures 4A-4E, terminals 26 are depicted. Terminals 26 are preferably formed in any manner from conductive material, such as metal, at step 210 in the manufacturing process in Figure 1A. Figure 4B depicts preferred terminals 26 as stamped from sheet metal having a thickness "e" about 0.15 mm such that, when laying on a flat surface, the distance "f" from the flat surface to an upper most surface of the stamped terminal 26 is about 0.47 mm. The bend represented by distance f is incorporated into the terminal structure 26 specifically to center the receptacle 30 with respect to the other terminal components 56, 58, and 28 to maximize the equidistant relationship of the terminal from the walls of conductor shield 24, once terminals 26 are integrated into conductor shield 24.

[0029] Other conductive material may be used to form terminals 26 such as metalized plastic. The number of stamped terminals 26 will preferably correspond to the number of rows in the final connector product.

[0030] As shown in Figures 4C and 4E, terminals 26 include a U-shaped receptacle 30 for receiving a plug pin, a straight portion 56, a tail portion 58, and a press-fit portion 28 for PCB insertion. The initial receptacle pitch "c" (Figure 4A) of the stamped terminals 26 will be limited by the manufacturing process, for example, to approximately 2.54 mm. The initial pitch "g" (Figure 4A) of press-fit tail portion 28 is less limited by the manufacturing process and will be about 2.0 mm. To reduce the initial receptacle pitch "c" to a desired pitch, bends 60 are made in the portion of the stamped terminals 26 between press-fit portions 28 and the carrier frame 62 at manufacturing step 230 (Fig. 1A). Bends 60 are formed after portions of carrier frame 36 adjacent to receptacle portions 30 have been removed at step 220.

[0031] For example, to reduce the receptacle pitch from about 2.54 mm to a new receptacle pitch "d" of about 2.0 mm, a series of stamps (bends 60) need to be made at different degrees as shown in Figure 4D such that "h" is about 0.6 mm, "i" is about 0.87 mm, "j" is about 1.14 mm, "k" is about 1.41 mm, and "g," which represents "f" from Figure 4B, is adjusted to about 0.32 mm.

[0032] Referring to Figures 5A-B and 6, stamped

terminals 26 are laid within the conductor shield 24 at equal annular distances from conductor shield 24 at step 130 (Fig.1A). At least part of the space between terminals 26 and the channels comprised of planar portion 36 and legs 38 is filled with an insulator. Preferably, an insert molding process is used to integrate terminals 26 and conductor shield 24 into one article. More preferably, molding material 64 is filled only in tail portion 46. In such an embodiment, the bodies of insulative plastic material are inserted in the channels in surrounding relationship to the tail portions of the terminals. This integrated unit defines the shielded connector column 20.

[0033] Once terminals 26 are integrated with conductor shield 24, the remainder of carrier frame 62 is removed from press-fit portion 28 of terminals 26. It is noted that removal of carrier frame 62 also involves removal of bends 60 previously formed therein.

[0034] Referring to Figures 7-8, shielded connector column structure 20 is inserted into an appropriately formed front housing 12 to form connector 10 with the desired number of receptacle positions 14 at step 140 (Fig.1A). Preferably, the front part of the shielded connector column 20 is inserted into a short recess slot 66 at the rear of the front housing 12. As can be seen in Figure 7, a number of slots are formed in front housing 12 thereby forming a number of fingers 70. Each finger 70 is sized to fit around receptacle portion 30 and within channel 44. After insertion, a plurality of shielded connector column modules are positioned adjacent to each other and terminals 26 are shielded from electronic interferences for the entire length of contact area 48 through tail portion 46. The terminals 26 will also be shielded from electronic interferences between all adjacent terminals - both vertically (between columns) and horizontally (between rows).

[0035] Front housing 12 can be made by molding plastic or plastic that is selectively metalized to establish and maintain a ground connection between a plug 68 and receptacle 30 (step 300).

[0036] While the present invention has been described in connection with the various figures, it is to be understood that other embodiments may be used or modifications and additions may be made to the described embodiment for performing the same function of the present invention without deviating therefrom. Therefore, the present invention should not be limited to any single embodiment, but rather construed in breadth and scope in accordance with the recitation of the appended claims.

Claims

1. A method for making an electrical connector comprising the steps of:

   forming a shield from sheet material;
   fixing stamped terminals to the shield such that the terminals are positioned equal annular distances from the shield whereby the terminals and the connector shield define a column connector module; and
   inserting a plurality of the shielded connector modules into an appropriately formed housing.

2. The method of making an electrical connector according to claim 1, wherein the step of forming a shield further comprises the steps of:

   forming said sheet material into a planar portion and a leg portion wherein said leg portion is defined by a plurality of legs having a first position lying in the same plane as the planar portion that extend from the planar portion
   bending the legs so that they are perpendicular to the first position thereby defining a second position, and
   bending the legs from the second position over and onto the planar portion thereby defining a third position forming a plurality of channels having a receptacle receiving portion and an tail receiving portion whereby the horizontal portion and the angular tail portion are defined on the planar portion of the sheet material.

3. The method of making an electrical connector according to claim 2, wherein said sheet material is metal.

4. The method of making an electrical connector according to claim 2, wherein the plurality of legs are secured to the planar portion of the stamped piece of sheet material.

5. The method of making an electrical connector according to claim 2, wherein the plurality of legs have a plurality of protrusions and the planar portion of the stamped piece of sheet material has a plurality of apertures designed to cooperate with and matingly receive the plurality of protrusions, wherein the steps of bending the legs comprises:

   bending the legs so that they are perpendicular to the first position of the leg portion defining a second position; and
   bending the legs from the second position over and onto the planar portion defining a third position whereby the apertures in the planar portion of the stamped flat piece of sheet material matingly receive the protrusions thereby forming a plurality of channels.

6. The method according to claim 2 further comprising the step of providing a terminal within each channel, wherein each terminal is formed to receive a mating pin and wherein each terminal defines a tail

portion that protrudes beyond the angular tail section.

7. The method according to claim 6 further comprising the step of fixing relative to one another the connector shield and the terminals at least in part by an insert-molding process.

8. The method according to claim 7 wherein the step of fixing the connector shield and the terminals comprises insert-molding in a tail portion.

9. The method according to claim 7 wherein the step of fixing the connector shield and the terminals comprises insert-molding a dielectric material in a tail portion.

10. The method for making an electrical connector of claim 1 further comprising the step of forming a lobe portion on the planar portion of the sheet material.

11. The method of claim 10 wherein the step of forming said lobe portion comprises the step of pressing the sheet material.

12. An electrical connector, comprising:

a plurality of column connector modules, wherein each column connector module comprises a shield having channels having a receptacle receiving portion and a tail receiving portion and a plurality of conductive terminals, wherein each conductive terminal is positioned within a channel of the shield wherein the conductive terminals are spaced at substantially equal annular distances from the shield, wherein the conductive terminals each comprise a press-fit tail portion and a receptacle portion; and
a housing having a plurality of openings defining a receptacle grid on a front portion thereof and a plurality of recess slots in a rear portion wherein the plurality of recess slots matingly receive the plurality of column connector modules such that the tail receiving portion and the lobe portion of the shield remains outside of the housing and the plurality of column connector modules are adjacent to each other thereby shielding the terminals throughout the entire length of the channels.

13. The connector of Claim 12, wherein said shield is formed from a single piece of material.

14. The connector of Claim 12, further comprising insulative insert material, wherein said conductive terminals are fixed to said shield by said material.

15. The connector of Claim 14, wherein said material is only present in the tail receiving portion of said channels.

16. The connector of Claim 15, wherein the recess slots in the housing define a plurality of fingers, wherein each finger is inserted into the receptacle receiving portion of the channel.

17. The electrical connector of claim 12, further comprising a lobe portion attached to said shield.

18. The electrical connector of claim 17, further comprising a side spring attached to each lobe portion, wherein the side spring is in contact with an adjacent lobe portion.

19. The electrical connector of claim 17, further comprising a press-fit pin attached to one end of the lobe portion of the connector shield.

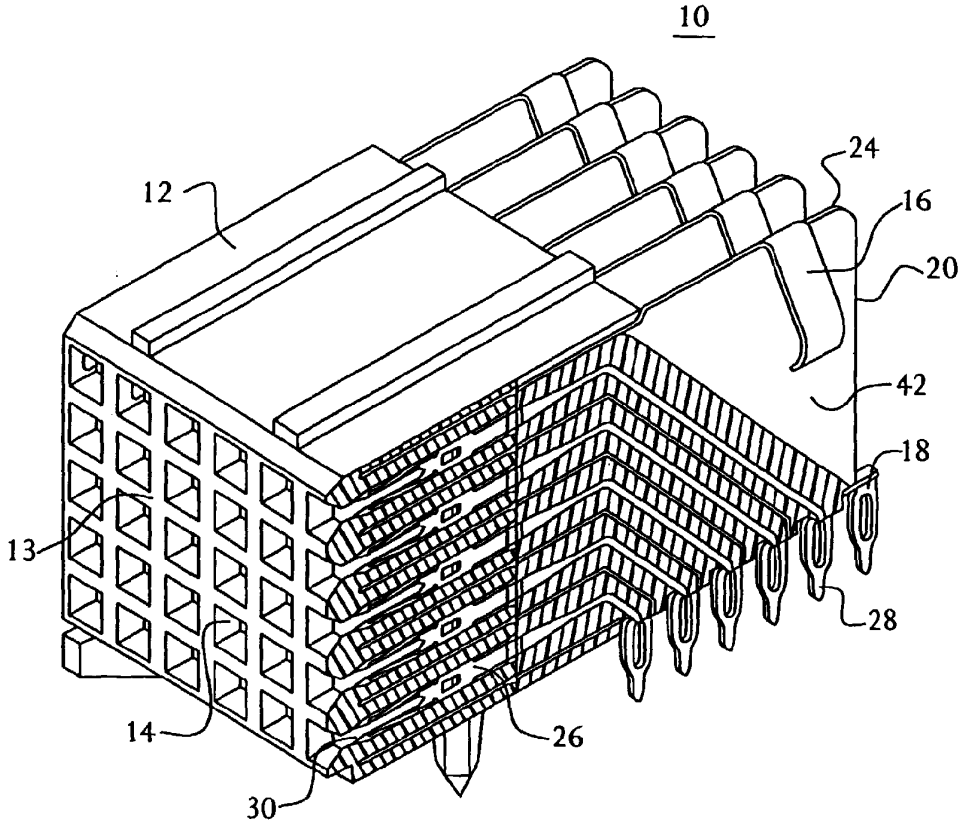


FIG. 1

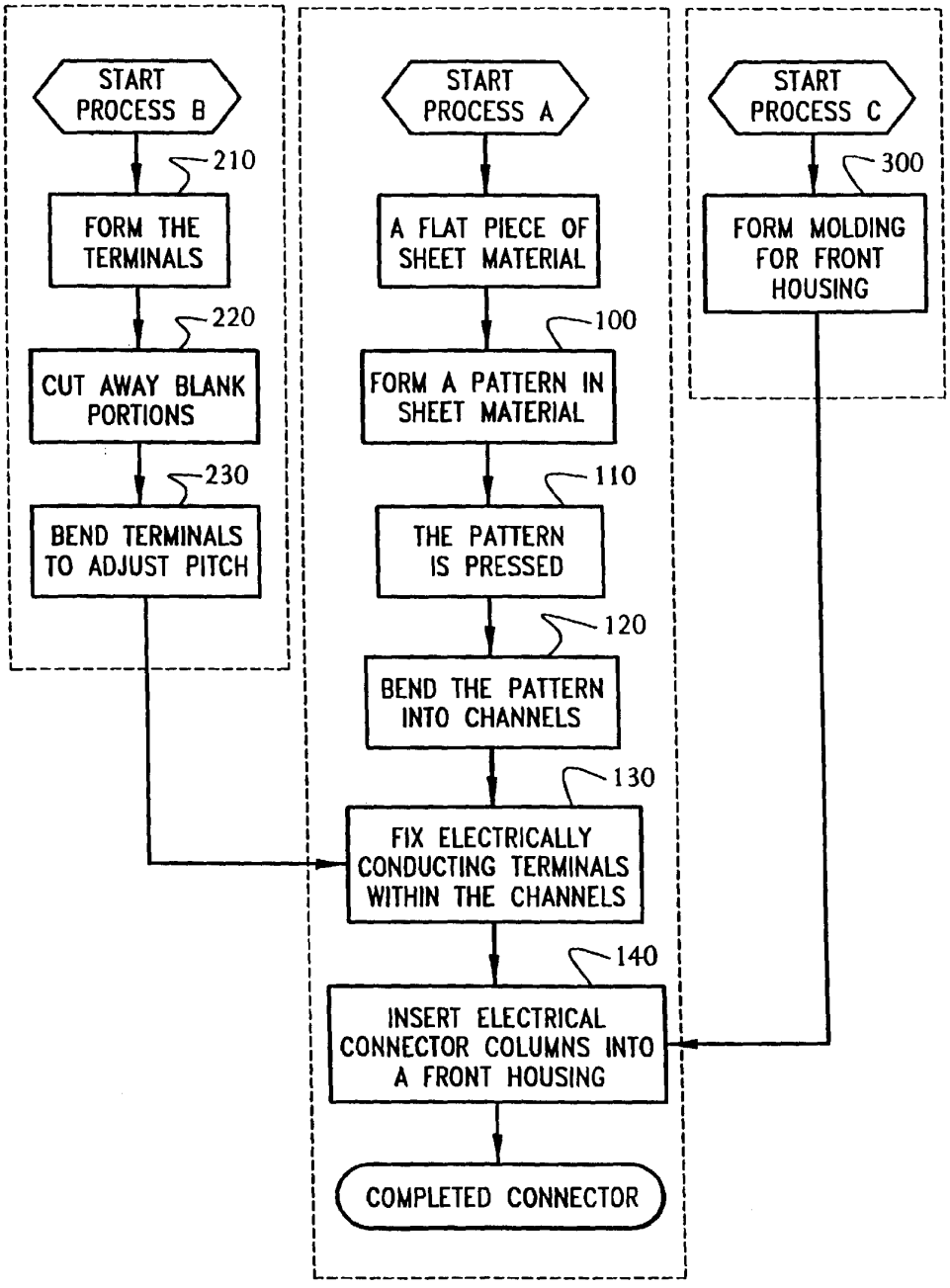

START PROCESS B
210
FORM THE TERMINALS
220
CUT AWAY BLANK PORTIONS
230
BEND TERMINALS TO ADJUST PITCH
START PROCESS A
A FLAT PIECE OF SHEET MATERIAL
100
FORM A PATTERN IN SHEET MATERIAL
110
THE PATTERN IS PRESSED
120
BEND THE PATTERN INTO CHANNELS
130
FIX ELECTRICALLY CONDUCTING TERMINALS WITHIN THE CHANNELS
140
INSERT ELECTRICAL CONNECTOR COLUMNS INTO A FRONT HOUSING
COMPLETED CONNECTOR
START PROCESS C
300
FORM MOLDING FOR FRONT HOUSING

FIG. 1A

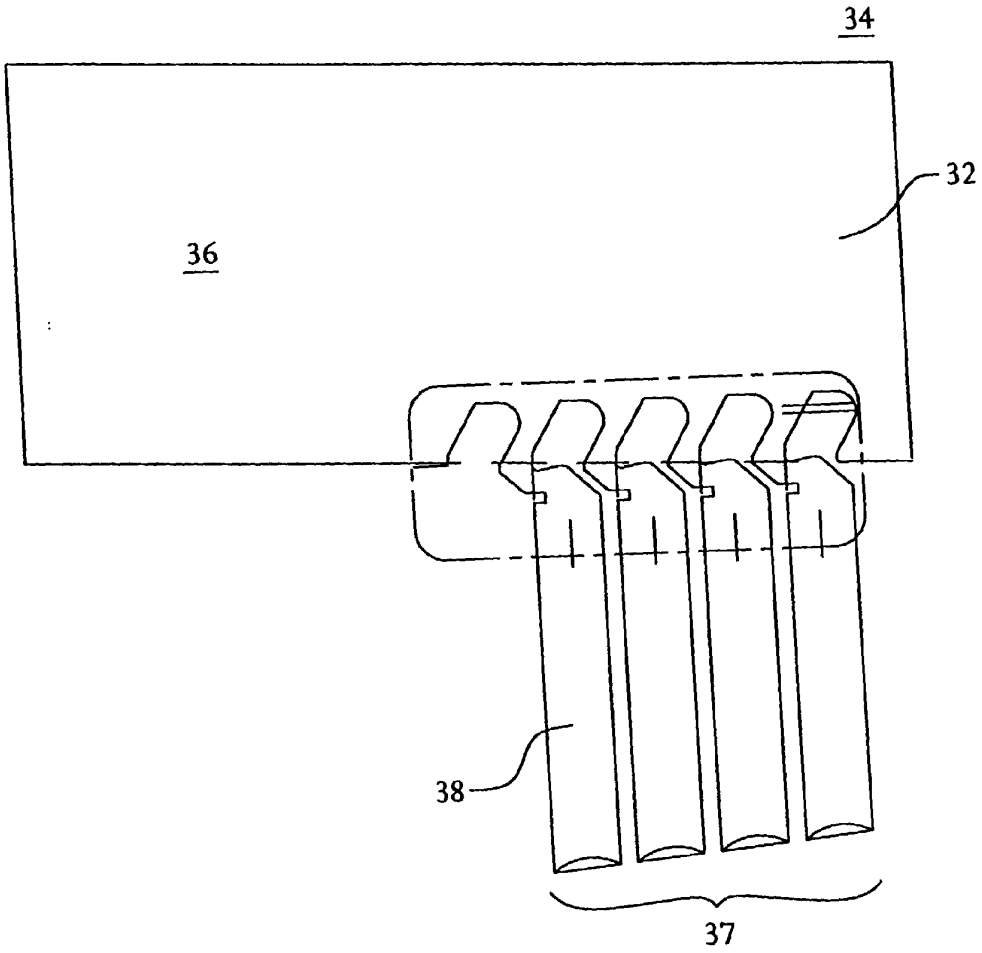
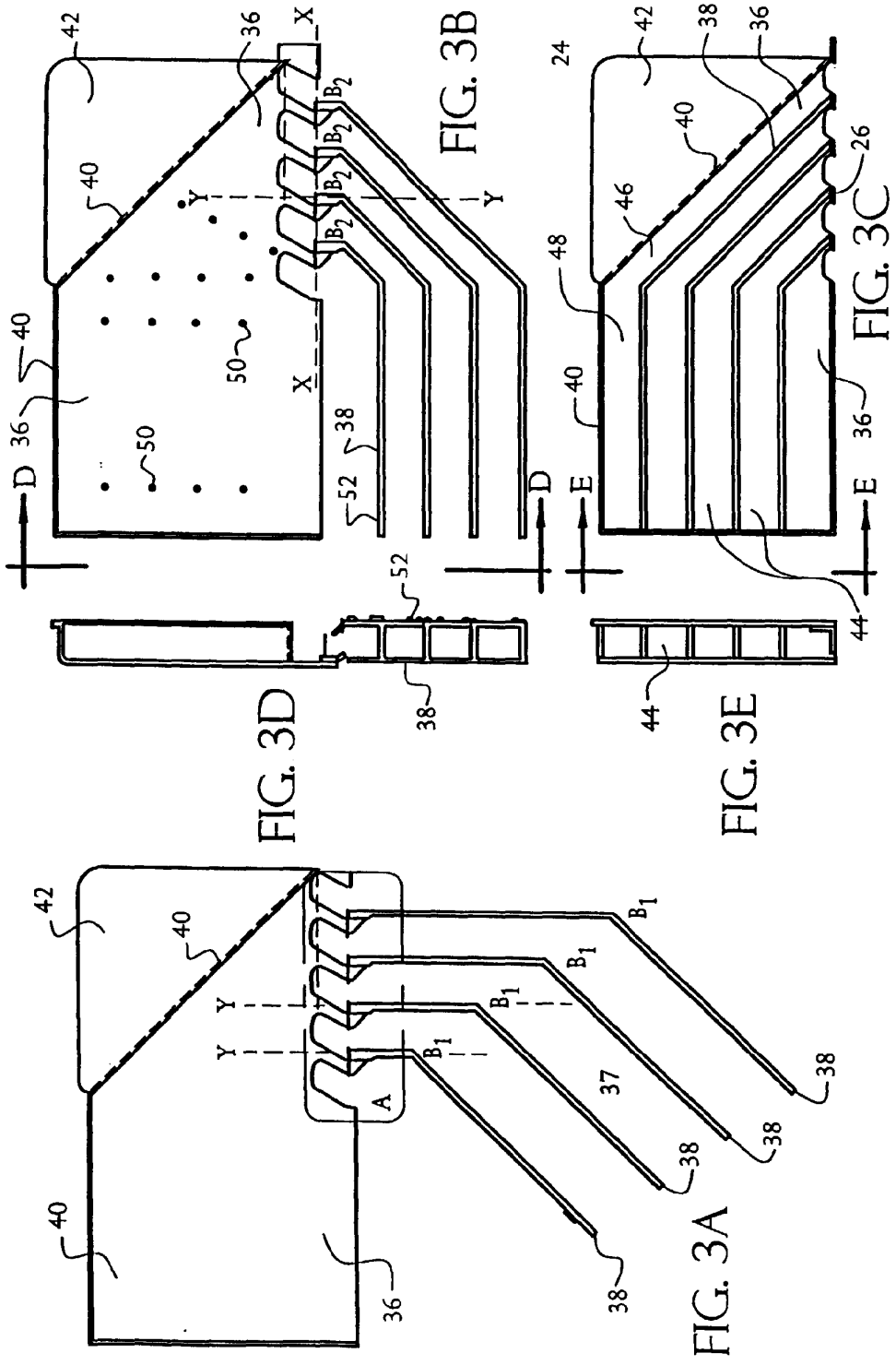
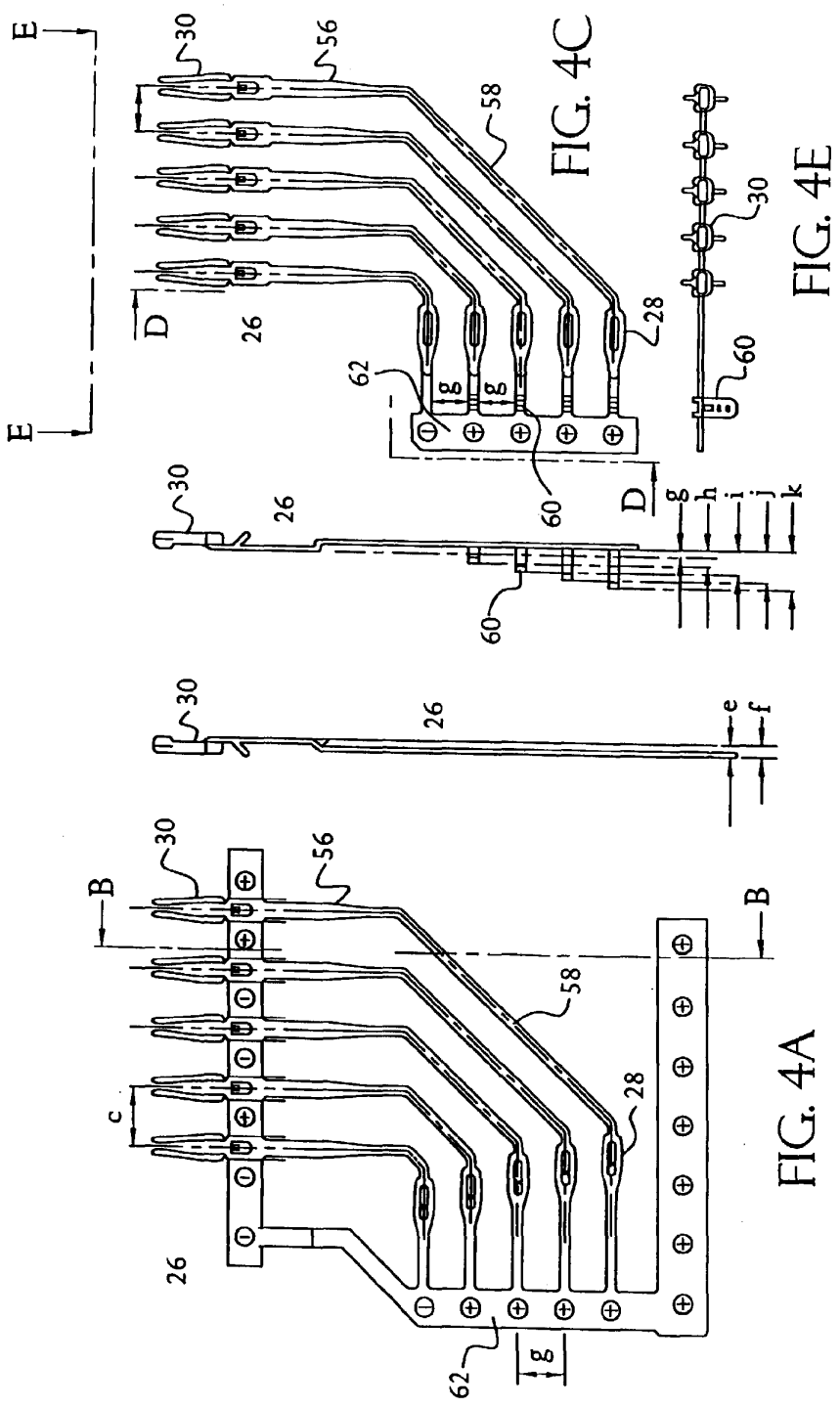


FIG. 2




E
E
30
56
58
D
26
62
g
g
28
60
30
60
FIG. 4C
FIG. 4E
30
26
60
D
g
h
i
j
k
30
26
e
f
FIG. 4B
FIG. 4D
B
30
56
B
58
c
28
26
62
g
FIG. 4A

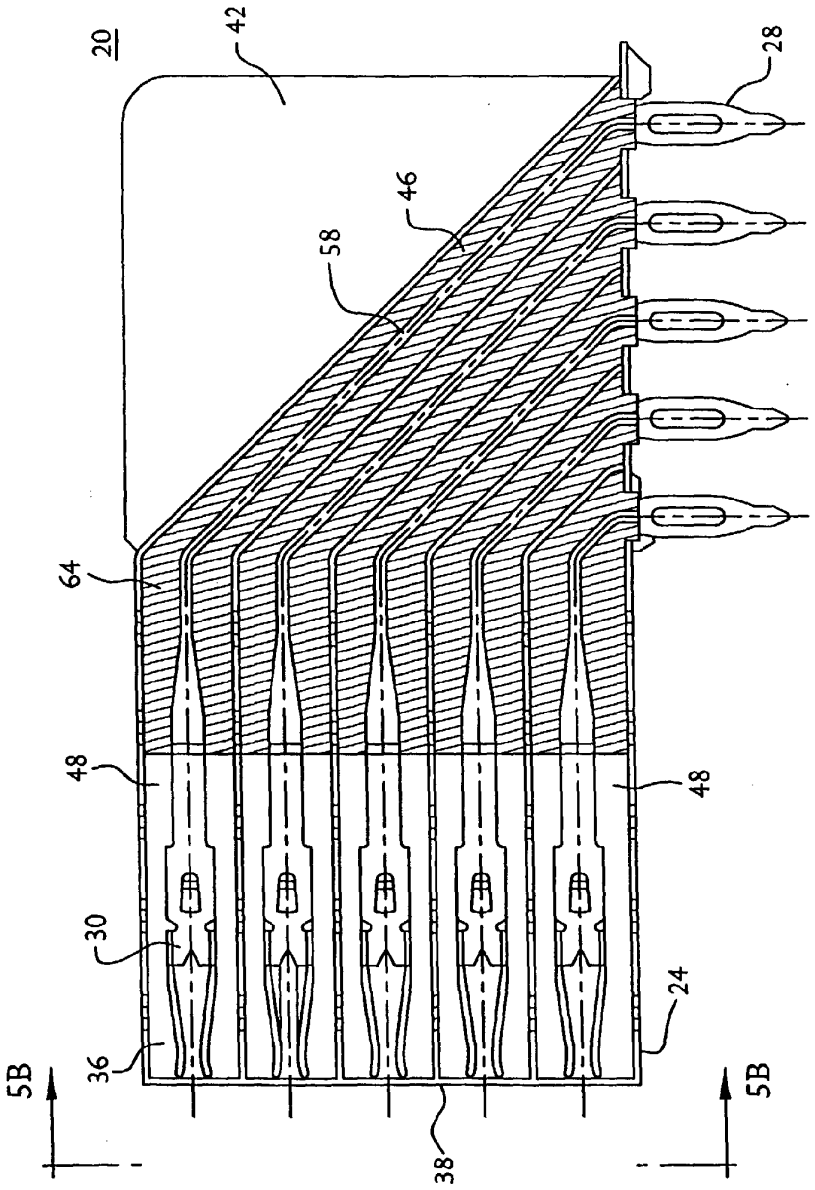


FIG. 5A

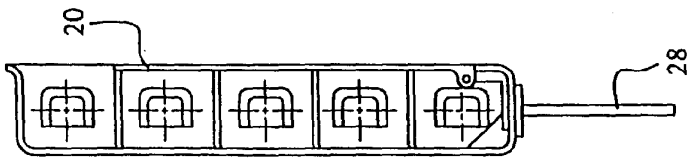


FIG. 5B

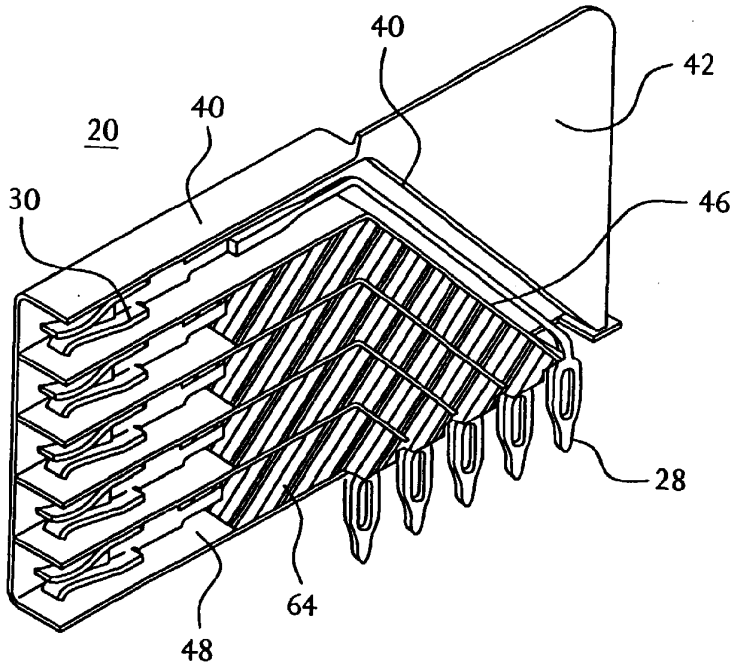


FIG. 6

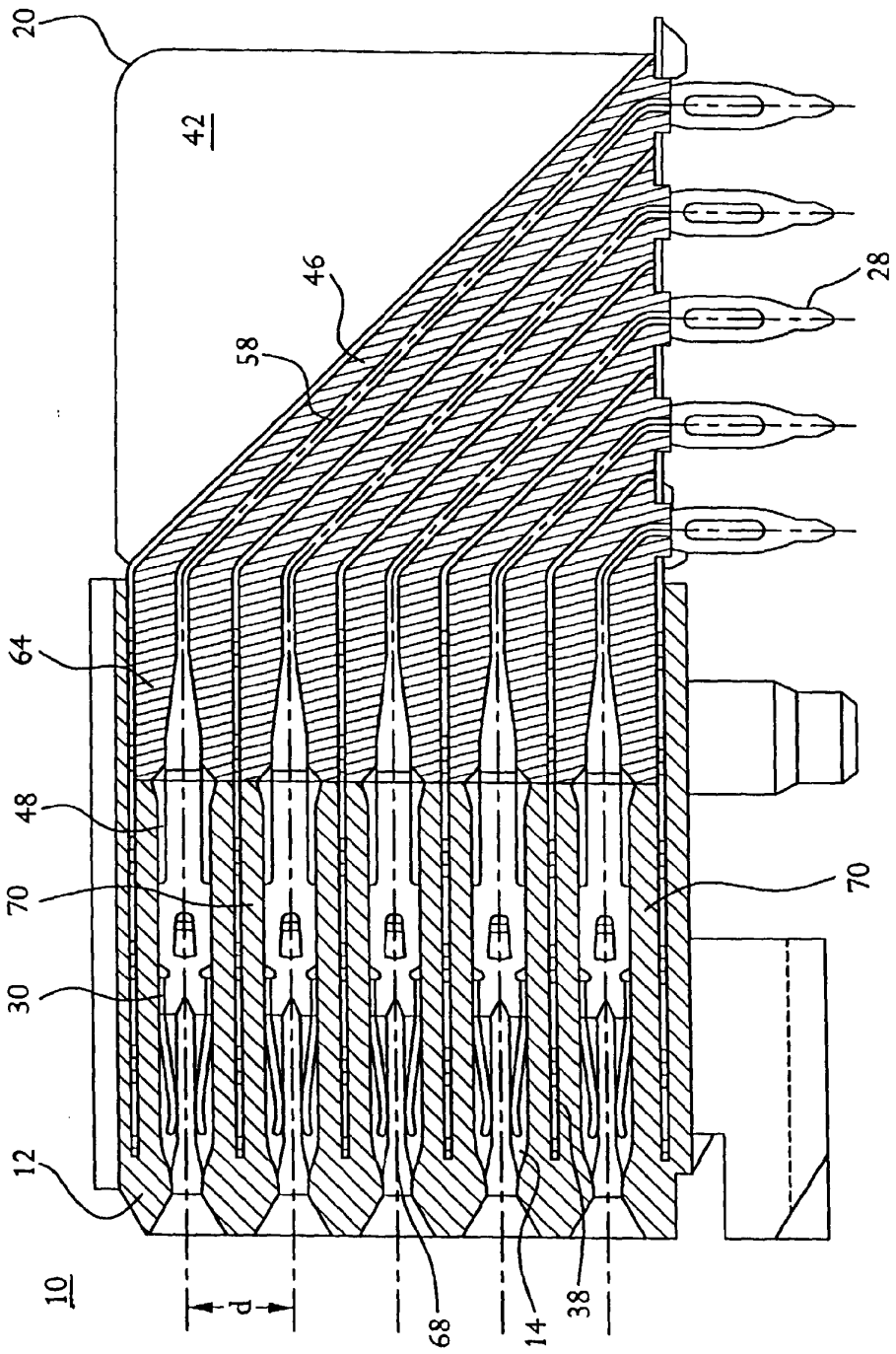


FIG. 7

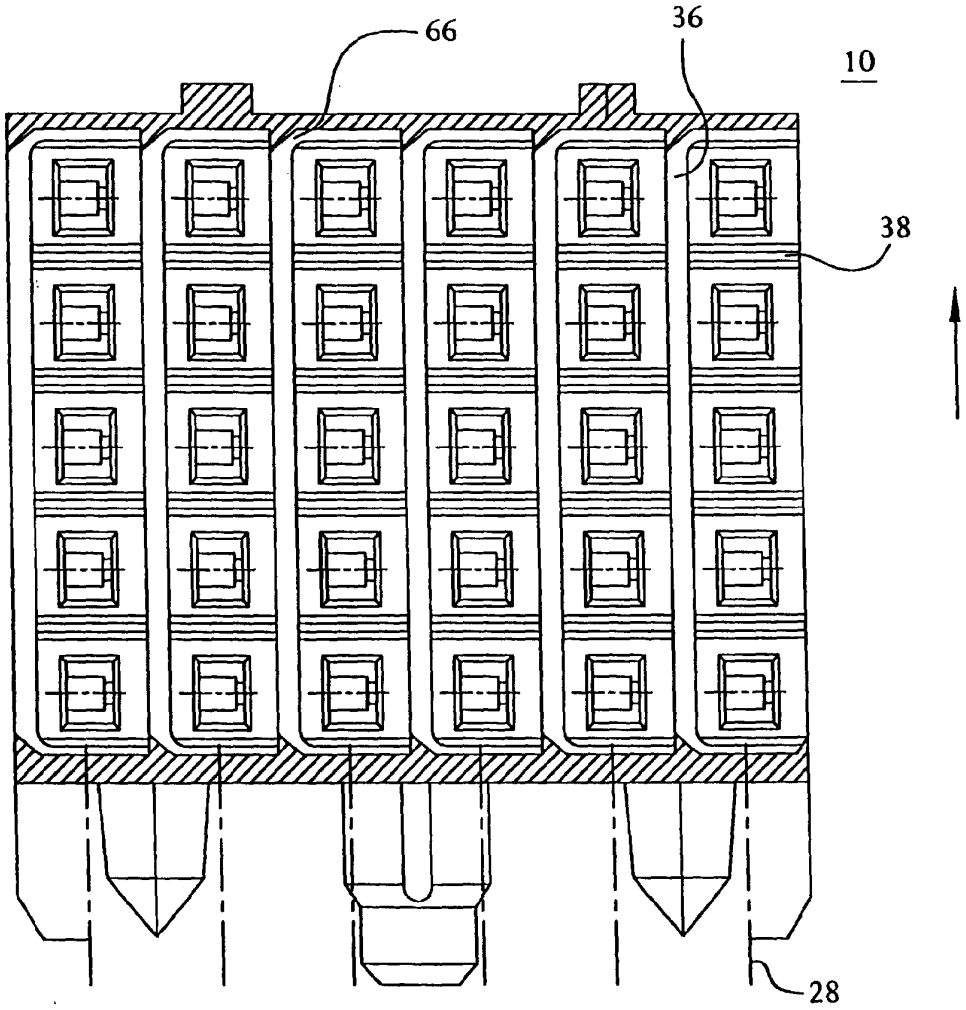


FIG. 8

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 00 20 0018

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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	9 March 2000	Alexatos, G

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
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D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 00 20 0018

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09-03-2000

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Espacenet

Bibliographic data: JP2001510627 (A) — 2001-07-31

HIGH SPEED, HIGH DENSITY ELECTRICAL CONNECTOR

Inventor(s):

Applicant(s):

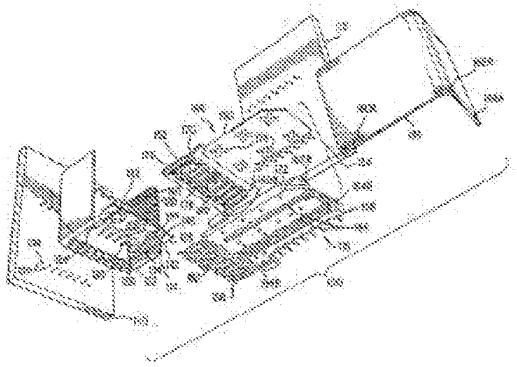
Classification: **- international:** ***H01R12/50; H01R13/514;*** *H01R43/16;* (IPC1-7): H01R12/16
- cooperative: **H01R13/514; H01R13/6476; H01R13/6586;** H01R12/716; H01R12/724; H01R13/6587; H01R43/16

Application number: JP19980534683 19980115

Priority number(s): US19970797537 19970207 ; WO1998US01168 19980115

Also published as: CA2280173 (A1) CA2280173 (C) DE69814123 (T2) EP1021854 (A1) EP1021854 (B1) KR100517158 (B1) KR20000070884 (A) US2002111068 (A1) US5993259 (A) US6238245 (B1) US6379188 (B1) US6554647 (B1) US6607402 (B2) WO9835409 (A1) less

Abstract not available for JP2001510627 (A)
Abstract of corresponding document: WO9835409 (A1)



A high speed, high density electrical connector for use with printed circuit boards. The connector is in two pieces with one piece having pins and shield plates and the other having socket type signal contacts and shield plates. The shields have a grounding arrangement which is adapted to control the electromagnetic fields, for various system architectures, simultaneous switching configurations and signal speeds, allowing all of the socket type signal contacts to be used for signal transmission. Additionally, at least one piece of the connector is manufactured from wafers, with each ground plane and signal column

injection molded into components which, when combined, form a wafer. This construction allows very close spacing between adjacent columns of signal contacts as well as tightly controlled spacing between the signal contacts and the shields. It also allows for easy and flexible manufacture, such as a connector that has wafers intermixed in a configuration to accommodate single ended, point to point and differential applications

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(51)Int.Cl.[7]	識別記号	ＦＩ		ﾃｰﾏｺｰﾄﾞ(参考)
Ｈ０１Ｒ　12/16		Ｈ０１Ｒ　23/68	３０３Ｇ	

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(87)国際公開番号　ＷＯ９８／３５４０９
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(31)優先権主張番号　０８／７９７，５３７
(32)優先日　平成９年２月７日(1997.2.7)
(33)優先権主張国　米国（ＵＳ）
(81)指定国　ＥＰ(ＡＴ，ＢＥ，ＣＨ，ＤＥ，ＤＫ，ＥＳ，ＦＩ，ＦＲ，ＧＢ，ＧＲ，ＩＥ，ＩＴ，ＬＵ，ＭＣ，ＮＬ，ＰＴ，ＳＥ)，ＣＡ，ＪＰ，ＫＲ，ＭＸ

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(74)代理人　弁理士　社本　一夫　（外４名）

最終頁に続く

(54)【発明の名称】　高速、高密度電気コネクタ

(57)【要約】
印刷回路板に使用される高速、高密度電気コネクタ。コネクタは２つの片から成り、一方の片にピンとシールドとを有し、他方の片にソケットタイプの信号接触子及びシールド板とを有している。該シールドは接地構成を有しており、該接地構成は様々な装置の構築のための電磁界、同時スイッチ構成及び信号速度制御するようにされており、あらゆるソケットタイプの信号接触子を利用して信号伝送が可能なようにされている。更に、少なくともワンピースのコネクタがウェファーから製造され、かく接地平面及び信号コラムが各部品に射出成形され、該各部品は組み合わされると、ウェファーを形成する。この構造により、信号接触子を備えた複数のコラム間の間隔が非常に緊密なものにされると共に、信号接触子とシールドとの間の間隔を厳しく制御することが可能になる。更に、ウェファーを混在した構成によりシングルエンドアプリケーション、ポイントーポイントアプリケーション及び差動アプリケーション等に利用可能なコネクタの製造が容易にされると共に柔軟性のあるものとなる。

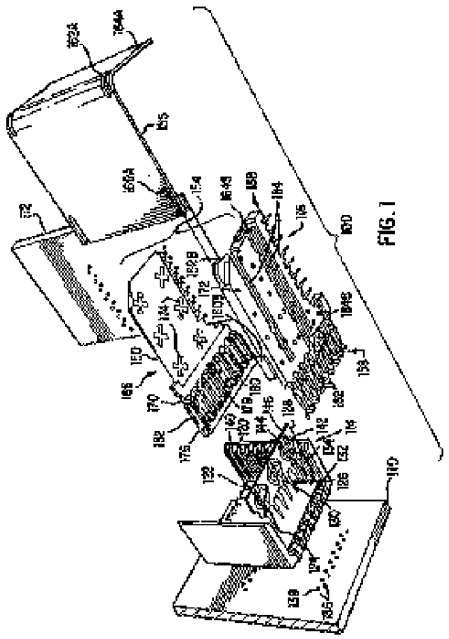
FIG. 1

【特許請求の範囲】

１．　ａ）ピンヘッダであって、

ｉ）絶縁性のベース、

ii）該絶縁性のベースに取り付けられた、ピンを備えた複数のコラム、及び

iii）前記絶縁性のベースに取り付けられた第１の複数の板であって、各板が隣接したピンを備えたコラムの間に配置されると共に、複数の捩じり接触子が内部に形成されている第１の複数の板を備えたピンヘッダと、

ｂ）ドーターカードコネクタであって、

ｉ）前記ピンヘッダの前記絶縁性のベースと嵌合する形状にされた絶縁性のベース、

ii）レセプタクルを備えた複数のコラムであって、各コラムが、前記複数のピンの１つに嵌合するように配置された複数のレセプタクルを有しているレセプタクルを備えた複数のコラム、及び

iii）第２の複数の板であって、各板が隣接するレセプタクルを備えたコラムの間に配置されると共に、前記ピンヘッダの前記複数の板の１つの上の複数の捩じり接触子に係合するように配置されている第２の複数の板を備えたドーターカードコネクタとを備えていることを特徴とする電気コネクタ。

２．　ａ）前記ピンを備えた複数のコラムの各々が、第１の数のピンを含み、且つ、

ｂ）前記ピンヘッダの前記第１の複数の板の各々が、該板から伸長する第２の数の接触子テールを有しており、該第２の数が前記第１の数と同等か、または、前記第１の数から１を引いた数より大きいことを特徴とする請求項１に記載の電気コネクタ。

３．　前記捩じり接触子の各々が、前記第１の複数の板の１つから打ち抜かれた少なくとも１つのアームを備えており、該アームが、前記板に２つの点で接続されると共に、該板の平面から逸脱するように屈曲されていることを特徴とする請求項１に記載の電気コネクタ。

４． 前記撓じり接触子の各々が、前記第１の複数の板の１つから打ち抜かれた少なくとも１つのアームを備えており、該アームの厚さが、前記板の厚さより薄いことを特徴とする請求項１に記載の電気コネクタ。

５． 前記同一のコラム内の隣接したレセプタクルが２ｍｍ以下の間隔で隔置され、且つ、レセプタクルを備えた隣接したコラムが、２．２５ｍｍ以下の間隔で隔置されていることを特徴とする請求項１に記載の電気コネクタ。

６． 前記撓じり接触子の各々が、アームを有し、該アームが曲がりくねった形状を有していることを特徴とする請求項１に記載の電気コネクタ。

７． 前記ドーターカードコネクタが、複数のモジュールを備え、前記コネクタが、更に、前記複数のモジュールの各々が取り付けられる金属製の補強体を備えていることを特徴とする請求項１に記載の電気コネクタ。

８． バックプレーンと、少なくとも１つのドーターカードとを備えたバックプレーン組立体に組み込まれる電気コネクタにおいて、

ａ）第１のコネクタ片であって、

ｉ）複数のピン状の形状をした信号接触子であって、各信号接触子が、前記バックプレーンに取り付けられたテール部を有し、前記ピンの形状をした信号接触子が複数の平行なコラム内に配置されている複数のピンの形状をした信号接触子、及び、

ii）第１の複数のシールド板であって、各シールド板が、信号接触子を備えた隣接したコラムの間に配置されると共に、該板から伸長すると共に前記バックプレーンに取り付けられた複数のテール部を有し、各シールド板の各テール部が、信号接触子を備えた前記同一コラム内で、隣接する信号接触子を備えたテール部の間に配置され、各シールド板に対して、信号接触子を備えた隣接したコラムの各対の隣接した信号接触子間に配置されたテール部が１つある第１の複数のシールド板を有する第１のコネクタ片と、

ｂ）第２のコネクタ片であって、

ｉ）、複数のレセプタクル信号接触子であって、該複数の信号接触子が、複数の平行なコラム内に、各レセプタクルがピンの形状をした信号接触子と係合するように配置された複数のレセプタクル信号接触子、及び、

ii) 第２の複数のシールド板であって、各シールド板がレセプタクル信号接触子を備えた隣接したコラムの間に配置され、前記第２の複数のシールド板の各々が前記第１の複数のシールド板の１つと機械的に係合し、接触子アームが前記第１又は第２の複数のシールド板の１つ２つの点において取り付けられている第２の複数のシールド板を有している第２のコネクタ片とを備えていることを特徴とする電気コネクタ。

９． 信号接触子を備えた各コラムが、少なくとも６つの信号接触子を有していることを特徴とする請求項８に記載の電気コネクタ。

１０． 更に、所定のピンの形状をした信号接触子がその他のピンの形状をした信号接触子を横断しない時に、帰電流路を提供する手段を備え、該手段が、前記第１の複数のシールド板と、前記第２のシールド板とを含んでいることを特徴とする請求項８に記載の電気コネクタ。

１１． 前記信号接触子の前記テール部及び前記板の前記テール部が圧嵌テールであり、前記信号接触子の前記テール部が前記板の前記テール部に直角にされていることを特徴とする請求項８に記載の電気コネクタ。

１２． 前記第１の複数の板の一部にスロットが形成され、前記板が、該スロットに対して垂直なラインに沿って湾曲部を有し、該湾曲部に一方の側の前記板の前記一部がテール領域を形成し、該湾曲部の他方の側の前記板の前記一部がシールド領域を形成し、前記テール領域及びシールド領域が平行であり、前記テール部が前記板の前記テール領域に結合されていることを特徴とする請求項８に記載の電気コネクタ。

１３． 前記第１の複数の板の前記テール部が、バックプレーンに接地されていることを特徴とする請求項８に記載の電気コネクタ。

１４． ２つのイナマテブル（ｉｎｅｒｍａｔｅａｂｌｅ）片を有するタイプの電気コネクタにおいて、各片が、コラム内に配置されて信号接触子領域をお画成する複数の信号接触子を有し、前記コネクタが、更に、信号接触子を備えた隣接したコラムの間に配置された、信号接触子を備えたコラム内の信号接触子の各々に帰電流路を提供する複数の手段を備え、該帰電流路が前記信号接触子の領域内にあり、帰電流路を提供する各手段が複数の、複数の点において互いに電気的に

係合した平行な板を備えており、前記板が、該板より伸長した複数の接触子テールを有し、該接触子テールが隣接した接触子の中間に配置されていることを特徴とする２つイナマテブル片を有するタイプの電気コネクタ。

１５．　前記板の各々の上の接触子テールの数が各コラムの信号接触子の数から１を引いたもの以上であることを特徴とする請求項１４に記載のコネクタ。

１６．　平行な板の各対の該板の一方が、少なくとも２つの端部を有し且つ２つの点で前記板に取り付けられた複数のアームを打ち抜いてあることを特徴とする請求項１５に記載のコネクタ。

１７．　前記アームの各々が、圧印加工されて前記板の厚さより薄くされていることを特徴とする請求項１６に記載のコネクタ。

１８．　前記アームの各々が、曲がりくねった形状を有していることを特徴とする請求項１７に記載のコネクタ。

１９．　前記信号接触子が、リニアインチ当たり少なくとも実信号密度１００及び立ち上がり時間が５００ｐｓｅｃで５％未満のクロストークとなるように隔置されていることを特徴とうする請求項１４に記載のコネクタ。

２０．　前記各コラム内の信号接触子の数が８であることを特徴とする請求項１９に記載のコネクタ。

【発明の詳細な説明】

高速、高密度電気コネクタ

本発明は、全体として、印刷回路板を相互連結するのに使用する電気コネクタに関し、より詳細には数多くの高速信号を搬送するようにされた前記電気コネクタに関する。

電気コネクタは多くの電気装置に使用されている。１つの装置をいつかの印刷回路板上に分けて作製しておき、後で電気コネクタを用いて斯かる印刷回路板を一体に接合して斯かる１つの装置を作製するのは簡単であり且つコスト的にも高効率であると言える。幾つかの印刷回路板を接合する伝統的な構成は、１つの印刷回路板をバックプレーンとして機能させることである。その他の印刷回路板はドーターボードと呼ばれ、バックプレーンを介して連結される。

従来のバックプレーンは多数のコネクタを備えた印刷回路板である。印刷回路板の導体トレースがコネクタの信号ピンに接続して、信号進路がコネクタに画成される。その他の印刷回路板は「ドーターボード（ｄａｕｇｈｔｅｒ　ｂｏａｒｄ）」と呼ばれ、同様にコネクタを備えており、該コネクタはバックプレーンのコネクタに差し込まれる。このように、信号はバックプレーンを介してドーターボード間で送信されるようにされている。ドーターカードはしばしばバックプレーンに直角に差し込まれることがある。このような用途にしようされるコネクタは直角の曲がりを備えており、しばしば「直角コネクタ」と呼ばれることがある。

コネクタは、また、印刷回路板を相互連結するその他の構成にも使用され、ケーブルを印刷回路板に接続するのにも使用される。時には、１つ以上の小型の印刷回路板が別の大型の印刷回路版に接続される場合がある。大型の印刷回路版は「マザーボード（ｍｏｔｈｅｒ　ｂｏａｒｄ）」と呼ばれ、該ボードに差し込まれる印刷回路板はドーターボードと呼ばれる。また、同サイズのボードが平行に整列される場合がある。このような用途に使用されるコネクタは時々「積層コネクタ（ｓｔａｃｋｉｎｇ　ｃｏｎｎｅｃｔｏｒ）」または「メザニンコネクタ（ｍｅｚｚａｎｉｎｅ　ｃｏｎｎｅｃｔｏｒ）」と呼ばれる。

正確な用途とは関係なく、電気コネクタのデザインは電子産業界の傾向を写し

ていると言える。電子装置は全体的に小型化及び高速化が進んでいる。また、電子装置の取り扱うデータも数年前に製造された装置に比べると数段多くなっている。これらの傾向は、電気コネクタがより多くのデータ信号を信号の低下をさせることなくより狭い空間内でより高速で搬送しなくてはならないことを意味している。

コネクタ内での信号接触子をより緊密にすればより狭い空間内でより多くの信号を搬送できるようにコネクタを製造することは可能である。斯かるコネクタは「高密度コネクタ」と呼ばれる。信号接触子をより緊密に配置することに関しての難点は信号接触子間には電磁的結合が存在することである。信号接触子が緊密に配置されるようになれば、電磁的結合が増大する。電磁的結合は、また、信号速度が高くなるに連れて増大する。

コネクタにおいては、電磁的結合量はコネクタの「漏話即ちクロストーク（ｃｒｏｓｓ　ｔａｌｋ）」を測定して表示するようにしている。クロストークは一般に１つの信号を１つ以上の信号接触子上に配置且つ別の信号接触子に連結された信号量を測定して測定される。どの信号接触子を他の信号接触子への結合のみならずクロストーク測定に使用するかの選択はクロストーク測定の数値に影響を与える。しかしながら、信頼性の高いクロストークの測定の結果、クロストークは信号速度が増大し且つ信号接触子がより緊密に配置されるようになると増大することが分かっている。

クロストークを低減するための従来の方法は、信号ピンのフィールド内で信号ピンを接地させることである。この方法の欠点は、コネクタの密度の有効信号密度を低下させてしまうことである。

高速及び高密度双方を満たすコネクタを作製するために、コネクタのデザイナー達は信号接触子間に遮蔽部材即ちシールドを挿入した。該シールドは信号接触子間の電磁的結合を低減させ、以ってより緊密な間隔及び高周波信号に対応しようとしたものである。適切に構成されれば、斯かる遮蔽によりコネクタを通る信号路のインピーダンスを制御することが可能であり、これにより該コネクタにより搬送される信号の保全性即ちインテグリティを向上させることが可能となる。

遮蔽の初期の利用が１９７４年２月１５日付けの富士通株式会社による特許公

開広報昭４９－６５４３に開示されている。双方ともＡＴ＆Ｔベル研究所（ＡＴ＆Ｔ　Ｂｅｌｌ　Ｌａｂｏｒａｔｏｒｉｅｓ）に譲渡された米国特許第４，６３２，４７６号及び第４，８０６，１０７号にはシールドを信号接触子のコラムの間に使用したコネクタデザインが開示されている。これらの特許はシールドがドーターボード及びバックプレーンコネクタの双方を貫通して信号接触子に平行に伸長しているコネクタが記載されている。片持ち梁状ビームが使用されて、シールドとバックプレーンコネクタとの間の電気接触を画成している。すべてがファラマトム・コネクタズ・インターナショナル（Ｆａｒａｍａｔｏｍｅ　Ｃｏｎｎｅｃｔｏｒｓ　Ｉｎｔｅｒｎａｔｉｏｎａｌ）に譲渡されている特許第５，４３３，６１７号、第５，４２９，５２１号、第５，４２９，５２０号及び第５，４３３，６１８号には同様な構成のものが開示されている。しかしながら、バックプレーンとシールドとの間の電気接続は、スプリング式の接触子を使用してなされている。

その他のコネクタではシールド板がドーターカードコネクタ内のみで使用されている。斯かるコネクタデザインの例としては、全てがＡＭＰ社（ＡＭＰ，　Ｉｎｃ．）に譲渡された特許第４，８４６，７２７号、第４，９７５，０８４号、第５，４９６，１８３号及び第５，０６６，２３６号に開示されているものがある。ドーターボードコネクタ内にのみシールドを備えた別のコネクタがテラダイン社（Ｔｅｒａｄｙｎｅ，　Ｉｎｃ．）に譲渡された米国特許第５，４８４，３１０号に開示されている。

クロストークを低減するために遮蔽を使用したコネクタを記載した特許数から、シールドを配置すると共にそれによる接続がコネクタの電気的性能に多大な影響を与えることが理解できる。遮蔽を特定の構成にすることもコネクタの機械的特性に著しい影響をあたえる。例えば、シールドとの電気的接続を如何にするかは、コネクタを嵌合させた時に「スタッビング（ｓｔｕｂｂｉｎｇ）」の存否に影響を及ぼす。スタッビングは、一方の接触子が別の接触子に引っかかることである。スタッビングがある時には、接触子の一方が常に損傷を受けて、接触子の修理又は交換が必要となる。

信号接触子間のクロストークの低減に著しく効果のあるシールド構成を有する

ことが強く望まれる。遮蔽構成が機械的に強固であることが強く望まれる。更に、斯かるコネクタの製造が容易であることが強く望まれる。更に、シールドのジオメトリ及び信号接触子を調整して信号反射を調整して接続を合致させるインピーダンスを得る事が望まれている。

発明の概要

上記の背景を念頭において、本発明の目的は、高速、高密度のコネクタを提供することである。

本発明の別の目的は、全ての信号接触子を使用して信号を搬送するようにされた高性能のコネクタを提供することである。

本発明の更に別の目的は、機械的強度のある電気コネクタを提供することである。

本発明の更に別の目的は、製造が簡単なコネクタを提供することである。

上記及びその他の目的は、ドーターボード及びバックプレーンコネクタの双方の信号接触子列の間にシールドを有する電気コネクタで達成される。バックプレーンコネクタのシールド板は捩じり接触子を有している。捩じり接触子はスタッビングの発生する機会を著しく低減する。捩じり接触子は、また、シールドを通る非常に望ましい電気流のパターンを画成し、これにより信号接触子間の誘導結合の低下従ってクロストークの低下に著しく効果を発揮する。

図面の簡単な説明

本発明は、以下の詳細な説明及び添付図面を参照するとより良く理解されるものであり、添付図面中、

図１は、本発明により作製したコネクタの分解図であり、

図２は、図１のコネクタに使用されているシールド板の素材板即ちブランクであり、

図３は、図２のシールド板ブランクがハウジング要素にインサート成形された後の図であり、

図４は、図１のコネクタに使用されている信号接触子ブランクであり、

図５は、図４の信号接触子ブランクがハウジング要素にインサート成形された

後の図であり、

図６は、差動モジュールを作製するのに適した図４の信号接触子ブランクの代替の実施例であり、

図７Ａ－７Ｃは、従来のコネクタの作動図であり、

図８Ａ－８Ｃは、図１のコネクタの同様の作動図であり、

図９Ａ及び９Ｂは、本発明の、それぞれ、シングルエンド及び差動実施例用のバックプレーン穴及び信号トレースの図であり、

図１０は、本発明の代替実施例の図であり、

図１１Ａは、図１の板１２８の代替実施例であり、

図１１Ｂは、図１１Ａの線Ｂ－Ｂに沿った横断面図であり、及び

図１２は、本発明によるコネクタの等角投影図である。

好適な実施例の説明

図１は、バックプレーン組立体１００の分解図である。バックプレーン１００は、該バックプレーンに取り付けられたピンヘッダ１１４を有している。ドーターカード１１２は、該ドーターカードに取り付けられたドーターカードコネクタ１１６を有している。該ドーターカードコネクタ１１６はピンヘッダ１１４に嵌め合わせてコネクタを形成する。バックっプレーン組立体にも同様に多数のその他のピンヘッダが取り付けられており、多数のドーターカードを接続できるようにされている。更に、多数のピンヘッダを端－端で整列させ、多数のピンヘッダを使用して１つのドーターカードへ接続できるようにされている。しかしながら、明白にするために、バックプレーン組立体の一部及び唯一のドーターカード１１２を図示する。

ピンヘッダ１１４は囲い板から形成される。囲い板１２０はプラスチック、ポリエステル又はその他の適当な絶縁材料から射出成形されるのが好適である。囲い板１２０はピンヘッダ１１４のベースとして機能する。

囲い板１２０の床（符号なし）は数列の穴１２６を含んでいる。ピン１２２は該穴１２６に挿入され、該ピンのテール１２４が囲い板１２０の下部表面を貫通して伸長している。該テール１２４は信号穴１３６内へ圧入される。穴１３６は

バックプレーン１１０に設けためっきした貫通穴であり、ピン１２２をバックプレーン１１０上のトレース（図示なし）に電気的に接続する機能を果たしている。明瞭に図示するため、ピン１２２は１本のみを図示している。しかしながら、ピンヘッダ１１４は多数の平行なピン列即ちコラムを含んでいる。好適な実施例では、ピンコラム毎に８本のピンが並ぶ。

各ピンコラム間の間隔は然して問題ではない。しかしながら、ピンを密接に配置して高密度コネクタを形成するのが本発明の目的である。例として、各コラム内のピンは２．２５ミリメートルの間隔で隔置し、ピンコラムは２ミリメートルの間隔で隔置する。ピン１２２は０．４ミリメートル厚の銅合金から打ち抜いて形成することが可能である。

囲い板１２０は溝１３２を含んでおり、該溝は床に形成され穴１２６のコラムと平行に伸長している。囲い板１２０の側壁には溝１３４が形成されている。シールド板１２８は溝１３２及び１３４に嵌合する。テール１３０は溝１３２の底部の穴（図示なし）を貫通して伸長する。テール１３０はバックプレーン１１０の接地穴１３８に係合する。該接地穴１３８はめっきした貫通穴であり、バックＰレート１１０の接地トレースへ接続される。

例示の実施例では、シールド板１２８は７つのテール１３０を有している。各テール１３０は２つの隣接したピン１２２の間に挟まる。シールド１２８のテール１３０が各品１２２に可能な限り接近するのが望ましい。しかしながら、隣接したピンの中間にテール１３０を配置すればシールド１２８と信号ピン１２２のコラム間の空間を低減することが可能となる。

シールド板１２８には幾つかの撓じりビーム接触子１４２が形成されている。各接触子１４２はシールド板１２８にアーム１４４及び１４６を打ち抜いて形成される。次いで、アーム１４４及び１４６がシールド板１２８の平面から逸脱するように折り曲げられる。アーム１４４及び１４６は十分な長さを有していて、シールド板１２８の平面に押し戻されると、撓むようにされている。アーム１４４及び１４６は十分な弾性を有しており、シールド１２８の平面に押し戻されるとばね力が生じるようにされている。アーム１４４及び１４６により生じたばね

力がアーム１４４または１４６と板１５０との間に接点が生成される。生成されたばね力は、ドーターカードコネクタ１１６が何度となく繰り返しピンヘッダ１１４に嵌め合わされたり外されたりした後でも上記の接触を確実なものにしておくのに十分なものでなくてはならない。

アーム１４４及び１４６は製造中に圧印加工される。斯かる圧印加工即ちコインイングは材料の厚さを薄くし、シールド板１２８を弱体化させずにビームのコンプライアンスを増大させる。

電気性能を向上させるためには、アーム１４４及び１４６は可能な限り短く且つ真っ直ぐであるのが望ましい。したがって、アームは必要以上の長さにすることなく所望のばね力を発生させる。更に、電気性能のためには、１方のアーム１４４又は１４６ができる限り各ピン１２２に接近しているのが望ましい。１つのアーム１４４及び１４６が各ピン１２２毎にあるのが理想的である。コラム毎に８本のピン１２２を備えた例示の実施例では、アーム１４４又は１４６が８本あって合計４つの釣り合いの取れた撚じりビーム接触子１４２を構成するのが理想的である。しかしながら、３つの釣り合いの取れた撚じりビーム接触子１４２のみを図示している。この構成は必要なばね力と所望の電気特性の間の妥協点を表している。

囲い板１２０上の溝１４０はドーターカードコネクタ１１６をピンヘッダ１１４に整列させるのためのものである。タブ１５２が溝１４０に嵌合して整列をさせると共に、ドーターカードコネクタ１１６がピンヘッダ１１４に対して側－側に移動するのを防止する。

ドーターカードコネクタ１１６はウェファー１５４から形成される。明瞭に例示するためにウェファー１５４は１つのみを図示するが、好適な実施例では、ドーターカードコネクタ１１６は幾つかのウェファーが横に並んで積層される。各ウェファー１５４はレセプタクルを１列含んでいる。各レセプタクル１５８は、ピンヘッダ１１４とドーターカードコネクタ１１６とが嵌め合うとピン１２２に係合する。したがって、ドーターカードコネクタ１１６はぴんヘッダ１１４のピンのコラム数と同数のウェファーから形成される。

ウェファー１５４は補強体１５６上に支持されている。該補強体１５６は金属

ストリップから打ち抜き形成されるのが好適である。該補強体はウェファー１５４を回転させずに所望の位置に保持する特徴を備えて打ち抜かれ、従って、３つの取り付け点を含んでいる。補強体１５６には前縁に沿ってスロット１６０Ａが形成されている。タブ１６０Ｂがスロット１６４Ａに嵌合する。補強体１５６はまた穴１６２Ａ及び１６４Ａを含んでいる。ハブ１６２Ｂ及び１６４Ｂが穴１６２Ａ及び１６４Ａに嵌合する。ハブ１６２Ｂ及び１６４Ｂは穴１６２Ａ及び１６４Ａに締まり嵌めするようなサイズにされている。

図１には明瞭性を確保するために、２、３個のスロット１６０及び１６２及び穴１６２のみを図示している。スロット及び穴のパターンは補強体１５６の全長に沿ってウェファー１５４が取り付けられる各点において繰り返される。

例示した実施例では、ウェファー１５４はシールド片１６６及び信号片１６８の２片に形成されている。シールド片１６６はシールド１５０の前部の周りでハウジング１７０にインサート成形される。信号片１６８は接触子４１０Ａ…４１０Ｈの周りでハウジング１７２にインサート成形される（図４）。

信号片１６８及びシールド片１６６は該２つの片を互いに一体に保持する特徴を有している。信号片１６８にはハブ５１２（図５）が一方の表面に形成されている。ハブはシールド１５０に食い込んだクリップ１７４へ整列すると共に該クリップ内へ挿入される。クリップ１７４はハブ５１２に係合し且つ信号片１６８に対してシールド板１５０をしっかりと保持する。

ハウジング１７０にはキャビティ１７６が形成されている。各キャビティ１７６はレセプタクルの１つを収容するような形状にされている。各キャビティ１７６は底部にプラットホーム１７８を有している。プラットホーム１７８には貫通穴１８０が形成されている。穴１８０は、ドーターカードコネクタ１１６がピンヘッダ１１４と嵌め合う時にピン１２２を収容するように成っている。従って、ピン１２２がレセプタクル１５８と嵌め合い、コネクタを通る信号路が形成される。

レセプタクル１５８には２つの脚１８２が形成される。該脚１８２は、レセプタクル１５８がキャビティ１７６内へ挿入される時に、プラットホーム１７８の対向する側部に嵌まる。レセプタクル１５８は脚１８２間の間隔がプラットフォ

ーム１７８の幅より狭くなるように形成されている。従って、レセプタクル１５８をキャビティ内へ収容するには、脚１８２を広げる工具の使用が必要となってくる。

レセプタクルは事前に装填される接触子即ちプレロード接触子として公知のものを構成する。プレロード接触子は従来よりレセプタクルをピラミッド形状のプラットホームに押圧することで形成されていた。レセプタクルがプラットホーム上に押圧されてくるに従いプラットホームの頂点が脚を広げる。斯かる接触片は低挿入力のみを必要とし、２つのコネクタが嵌め合うときに、ピンに引っかかりが生じることはほとんどない。本発明のレセプタクルは同様の効果を発揮するが、レセプタクルをピラミッドに押圧するよりは寧ろ側部から挿入することで前記の効果を得るようにしたものである。

ハウジング１７２には溝１８４が形成されている。上記に説明した如く、ハブ５１２（図５）はシールド板１５０を貫通して伸長する。２つのウェファーが横に並んで積層されると、一方のウェファー１５４からのハブ５１２が隣接するウェファーの溝１８４内へ突出する。ハブ５１２及び溝１８４は隣接するウェファーを一体に保持して１つのローラが隣接する次のウェファーに対して回動するのを防止するのを助けるようにされている。補強体１５６と共にこれらの特徴によりウェファーを保持する別体の箱またはハウジングが不要となり、コネクタの簡素化を図っている。

ハウジング１７０および１７２には多くの穴（符号なし）が形成されており、そのように図示されている。これらの穴は本発明の重要な要素ではない。斯かる穴は「ピンチホール（ｐｉｎｃｈ　ｈｏｌｅ）」と呼ばれ、シールド板１５０またはレセプタクル接触子４１０を射出成形中に保持するのに使用される。シールド板やレセプタクル接触子を射出成形中に保持して、最終製品におけるシールド板及びレセプタクル接触子間の間隔を均一にいじするのが望ましいことである。

図２はシールド板１５０を作製するのに使用するブランクをより詳細に図示している。好適な実施例では、シールド板１５０はロールに巻かれた金属から打ち抜かれる。該板はキャリアストリップ２１０上に保持されて取り扱いが容易にされている。板１５０を射出成形してシールド片１６６とした後でキャリアストリ

ップが切断される。

板１５０は穴２１２を含んでいる。穴２１２はハウジング７０からのプラスチックで充填されて、ハウジング１７０で板１５０を係止するようにされている。

板１５０は、また、スロット２１４を含んでいる。スロット２１４はレセプタクル１５８の間に挟まるように位置決めされている。スロット２１４は板１５０のキャパシタンスを制御する機能を果たし、該キャパシタンスによりコネクタのインピーダンスが総体的に上昇される。スロットはまた、レセプタクル１５８近傍の板内を流れる電流を流す機能も果たし、信号路となる。信号路近傍において帰路電流が高くなるとクロストークが低減される。

スロット２１６はスロット２１４と類似しているが、より大型であって、シールド板１５０がハウジング１７０に成形される時に、フィンガー３１６（図３）がシールド板１５０を通過できるようにしている。フィンガー３１６は絶縁材料から形成された小型のフィンガーであり、板１５０に対して板１２８を保持するのを助けるようにされている。図１において、中央の２つのキャビティ１７６の中間壁が一部取り除かれているのに留意したい。隣接したウェファー１５４（図示なし）からのフィンガー３１６がこの空間に嵌合して前記２つの中央キャビティ間の壁を埋める。フィンガー３１６はハウジング１７０を超えて伸長して隣接したウェファー（図示なし）のスロット１８４Ｂに嵌合することとなる。

スロット２１８は、所望の場合に、テール領域２２２がシールド板１５０の平面から逸脱して屈曲されるのを可能にしている。図９Ａは印刷回路板上のトレースを図示しており、該トレースは、本発明のコネクタを取り付けるのに使用する穴の間に進路を形成している。図９Ａは信号穴１８６のコラムの一部及び接接触子１８８のコラムの一部を図示している。コネクタを使用してシングルエンド信号を搬送する場合には、トレース９１０及び９１２が可能な限り最大の接地により分離されているのが望ましい。したがって、接地穴１８８が信号穴１８６のコラム間の中央に配置されて、信号トレース９１０及び９１２が信号穴１８６と接地穴１８８との間で信号の進路を形成するのが望ましい。一方、図９Ｂは差動対信号用の好適な進路を図示している。差動対信号では、トレースが可能な限り一体に接近して進路を形成するのが望まれる。トレース９１４及び９１６が一体に

接近するのを可能にするためには、接地穴１８８が信号穴１８６のコラムの中央に配置されないようにする。寧ろ、接地穴はオフセットして信号接触子１８６の１列に可能な限り接近できるようにする。斯かる配置により双方の信号トレース９１４及び９１６が接地穴１８８と信号穴１８６のコラムとの間に進路を形成できるようにされている。シングルエンドの構成では、テール領域２２２はシールド板１５０の平面から逸脱するように屈曲される。差動構成では、テール領域の屈曲はない。

シールド板１２８（図１）は、所望であれば、テール領域で同様に屈曲させることができる。好適な実施例では、板１２８はシングルエンド信号に対しては屈曲されておらず、差動信号に対しては屈曲されている点に注意したい。

タブ２２０はハウジング１７０を射出成形する前に板１５０の平面から逸脱するように屈曲される。タブ２２０は穴１８０間に巻き付く（図１）。タブ２２０は板１５０を確実にハウジング１７０に接着するの助ける。タブはまた、ハウジング１７０の前面即ちピンヘッダ１１４に面した表面を補強する。

図３はハウジング１７０内へインサート成形されて接地部１６６を形成した後のシールド板１５０を図示している。図３は、ハウジング１７０がピラミッド形状の突起３１０をシールド片１６６の前面に含んでいるのを図示している。マッチング凹部（図示なし）がぴんヘッダ１１４の床に含まれている。突起３１０及びマッチング凹部は捩じりビーム接触子１４２のばね力が、ドーターカードコネクタ１１６がピンヘッダ１１４内に挿入される時に、隣接したウェファー１５４を広げるのを防止する。

図４はレセプタクル接触子ブランク４００を図示している。レセプタクル接触子ブランクは、金属シートから打ち抜かれるのが好適である。数多くの斯かるブランクがロール状に打ち抜かれる。好適な実施例では、８つのレセプタクル４１０Ａ…４１０Ｈを使用している。レセプタクル接触子４１０は搬送ストリップ４１２、４１４、４１６、４１８及び４２２上に一体に保持される。これらの搬送ストリップは、分断されて、ハウジング１７２が接触子の周りに成形された後で、接触子４１０Ａ…４１０Ｈを分離するの助ける。搬送トリップは製造作業の大半において保持しておきレセプタクル部１６８の取り扱いを容易にすることがで

き

る。

レセプタクル接触子４１０Ａ…４１０Ｈの各々は２つの脚１８２を含んでいる。該脚１８２は折り曲げられると共に屈曲されてレセプタクル１５８を形成する。

各レセプタクル接触子４１０Ａ…４１０Ｈはまた伝送領域４２４及びテール領域４２６を含んでいる。図４は等間隔に隔置された伝送領域４２４を図示している。この構成は、接触子間の間隔が最大になることからシングルエンド信号には好適なものとなる。

図４はテール領域がめっきを施した貫通穴に嵌合するのに適していることを図示したものである。その他のタイプのテール領域も使用することが可能である。例えば、はんだテールを代わりに使用することも可能である。

図５は、レセプタクル接触子ブランク４００を図示しており、ハウジング１７２がその周りに既に成形されている。

図６は、本発明の代替実施例に使用するのに適したレセプタクル接触子ブランク６００を図示している。レセプタクル６１０Ａ…６１０Ｈは対にグループ分けされている。即ち、（６１０Ａと６１０Ｂ）、（６１０Ｃと６１０Ｄ）、（６１０Ｅと６１０Ｆ）及び（６１０Ｇと６１０Ｈ）である。各対の伝送領域６２４は差動インピーダンスを維持しつつ、でき得る限り一体に接近させる。これにより隣接する対の間の間隔が増大する。この構成は差動信号の信号保全性即ちインテグリティを改善する。

テール領域６２６及びレセプタクル接触子ブランク４００及び６００は同一である。該テール領域はレセプタクル接触子４１０及び６１０のハウジング１７２から伸長する部分である。したがって、外面的にはシングルエンド信号でも差動信号でも信号部１６８は同一である。これによりシングルエンド信号ウェファー及び差動信号ウェファーがドーターカードコネクタと混合するのが可能となる。

図７Ａは本発明の改良された性能を説明する一助とする従来の技術によるコネクタを例示している。図７Ａはシールド板７１０を図示しており、該シールド板

には片持ち梁状のビーム７１２が形成されている。接点にはＸの標識が付けてある。ブレード７１４は点７２２でバックプレーン（図示なし）に接続してある。

信号は信号ピン７１６及び７１８を介してシールド板の近傍を流れて伝送される。板７１０及びブレード７１４が信号リターンとして作用する。信号路７２０はこれらの要素を通っており、それをループとして図示している。信号路７２０はピン７１８を通り抜けている点に注意したい。公知の如く、導体を通過するループ内を流れる信号は誘導的に導体に結合する。従って図７Ａの構成ではピン７１６から７１８まで比較的高い結合又はクロストークが発生することになる。

図７Ｂは図７Ａの構成の側面図である。片持ち梁状のビーム７１２がブレード７１４の間隔はｄ２であって、こちらの方が大きい。高周波信号を伝送する時には信号路と接地との間の距離により信号路のインピーダンスが決定される。距離が変化すればインピーダンスが変化し、インピーダンスが変化すれば信号反射が変化し、望ましいことではない。

図７Ｃは同一構成のものが嵌め合いを完了した時の図である。ブレード７１４は片持ち梁状ビーム７１２の下を滑動しなければならない。挿入が正しくなされなければ、ブレード７１４が片持ち梁状ビーム７１２の端部に衝突せざるを得ず、この現象を「スタッビング」と呼んでいる。これによりコネクタが破損することがあり、コネクタには甚だ望ましくないことである。

反対に、ず８は本発明により作製したコネクタの要素の略図である。シールド板１２８及び１５０は重なり合う。撓じりビーム１４６上のＸマークをした点で接触がなされる。信号路８２０は、信号ピン１２２を通過していた１５０を通って接点Ｘまで戻り、アーム１４６、板１２８及び板１３０を通過して流れる。信号路８２０はバックプレーン（図８には図示なし）を通って完了する。信号路８２０は隣接する信号ピン１２２を通り抜けていないことに留意したい。このように、クロストークが従来の技術に比較して著しく低減される。

図８Ｂはドーターカードコネクタ１１６をぴんヘッダ１１４に嵌め合わせる前のシールド板１２８及び１５０の略図である。図８Ｂの斜視図では、アーム１４６が板１２８の平面から逸脱して屈曲されているのが図示されている。板１５０

及び１２８が嵌め合い中に互いに沿って滑動すると、アーム１４６が板１２８の平面に戻される。

図８Ｃは板１２８及び１５０が嵌合した構成を図示している。ディムプル８１０がアーム１４６内に圧入されて板１５０に接触しているのが図示されている。

アーム１４６を板１２８の平面に戻すことにより生じる捩じりばね力が電気接触を確実なものとしている。板１２８または１５０と隣接する信号接触子との間隔は図７Ｂに図示した不連続となるものほど大きくはない。これによりコネクタの電気性能が向上する。

図８Ｂから図８Ｃの構成に移る時には、スタッビングを起こすほどの表面の唐突さなない。従って、捩じり接触子を用いれば、コネクタの機械的強度が従来の技術のものより改善される。

図１０はウェファー１５４(図１)の代替実施例である。図１０の実施例では、搬送ストリップ１０１０上のシールドブランクが射出成形により絶縁性ハウジング１０７０内に封入される。シールドテール１０３０はハウジング１０７０から伸長している如く図示されている。ハウジング１０７０はキャビティ１０１６、１０１７、１０１８及び１０９０を含む。シールドブランクは切断屈曲されてキャビティ１０１６、１０１７、１０１８及び１０９０内に接触子を形成する。

キャビティ１０１６、１０１７、１０１８及び１０９０には床に穴１０２２が形成されている。ピンヘッダからのピンが嵌合中にこれらの穴を介して挿入され、ピン及び接触子のばね力を介して係合してシールドへの電気的接続が確実にされる。

図１０の実施例では、信号接触子は別個に打ち抜かれる。接触子の伝送ライン部分はキャビティ１０２６内に施設される。信号接触子のレセプタクル部分はキャビティ１０２４内に挿入される。

各コラムに使用する信号接触子の数は任意であることを図１０のウェーファーは例示している。図１０では、４つの信号接触子が各コラムに使用されているのが図示されている。また、板１２８に代わりピンを使用することも可能であることも同図によりわかる。しかしながら、電気性能上は相違があると考えられる。

図１０の構成では板が使用される。斯かる場合にはキャビティ１０１６、１０１７、１０１８及び１０９０内の一連の別個の穴１０２２に代わって、スロットがキャビティを通るようにすることが可能である。

図１１Ａは板１２８上の接触子１４２の代替実施例を図示している。板１１２８は一連の捩じり接触子１１４６を含んでいる。各接触子は板１１２８からアーム１１４６を打ち抜いて作製されている。ここで、アームは曲がりくねった形状を有している。上記に説明した如く、アーム１４６は十分な長さにされて良好な柔軟性を有するのが望ましい。しかしながら、電流は信号ピン１２２を通る電流の流れに垂直な方向に可能な限り狭い領域内で接触し１４２を通って流れるのが望ましい。上記２つのゴールを達成するためにはアーム１１４６は曲がりくねった形状に打ち抜かれる。

図１１Ｂは図１Ａの線Ｂ－Ｂに沿った板１２８の横断面図である。図示の如く、アーム１１４６は板１１２８の平面から逸脱して屈曲されている。コネクタの半体との嵌合中に、アームは押し戻されて板１１２８の平面内に戻り、これにより捩じり力が発生する。

図１２はコネクタ１００の追加の図である。図１２はドーターカードコネクタ１１６の表面１２１０を図示している。ピンヘッダ１１４の下部表面もまた見える。この図においては、板１２８の圧嵌めテール１２４の向きが信号ピン１２２の圧嵌めテール１３０の向きと直角になっている。

例

本発明により作製したコネクタを試験した。試験はシングルエンドの構成のものに就いてなされ、１０本の近接したラインから成る１本の信号ラインに就いてなされた。信号の立ち上がり時間が５００ｐｓの場合のクロストークは４．９％であった。前方へのクロストークは３．２％であった。反射は測定に値しないくらい小さなものであった。コネクタの実信号密度は１リニアインチ当たり１０１であった。

１つの実施例に就いて説明してきたが、多くの代替実施例又は修正を施すことが可能である。例えば、コネクタのサイズを説明したものから増減することが可

能である。また、コネクタを形成する材料は説明説明に使用したもの以外の材料を使用することが可能である。

説明した特定の構造に様々な変更を加えることは可能である。例えば、クリップ１７４が全体として対照に図示されている。クリップ１７４を細長くして、長軸を信号片１６８中の信号接触子と平行に伸長するようにし、それと垂直となる

短軸を可能な限り短くすればシールド板１５０の効果を増大することが可能である。

また、製造技術も変更することが可能である。例えば、複数のウェファーを補強体上に載せてドーターカードコネクタを形成すると説明したが、複数のシールド片及び信号レセプタクルを形成したハウジング内に挿入して同等の構造体を形成することも可能である。

従って、本発明は、添付の請求項の趣旨及び範囲にのみ限定されるものである。

【図１】

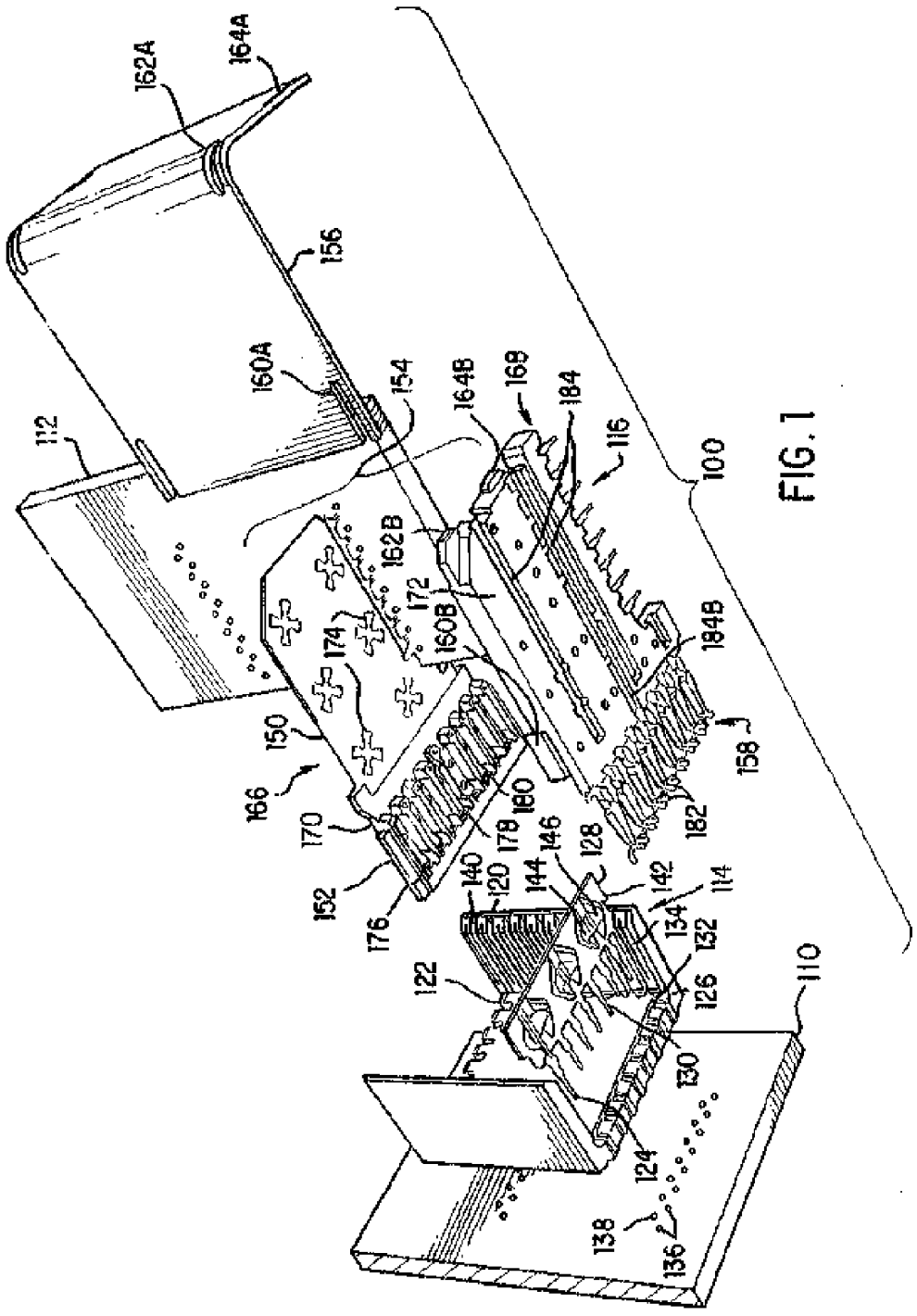
162A
164A
156
160A
154
112
164B
168
184
116
100
162B
172
160B
174
184B
150
158
166
180
170
178
182
146
128
152
140
120
144
142
114
176
134
132
122
126
110
130
124
138
136

FIG. 1

【図２】

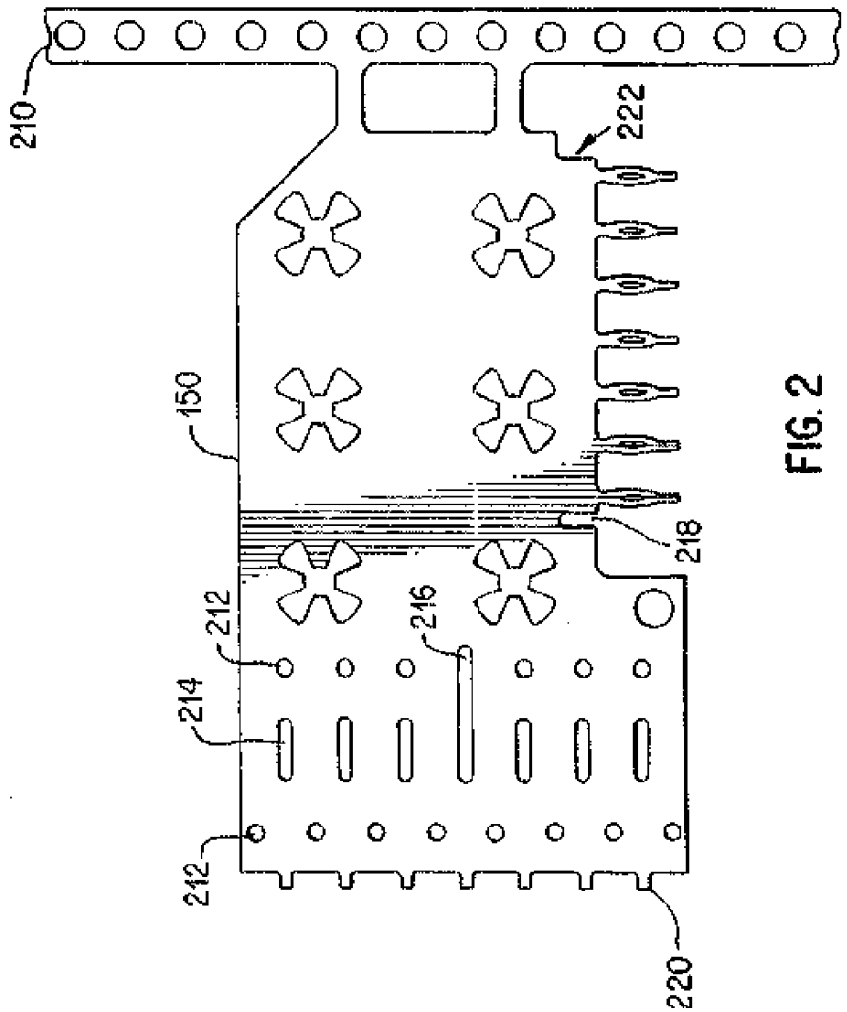

FIG. 2

【図３】

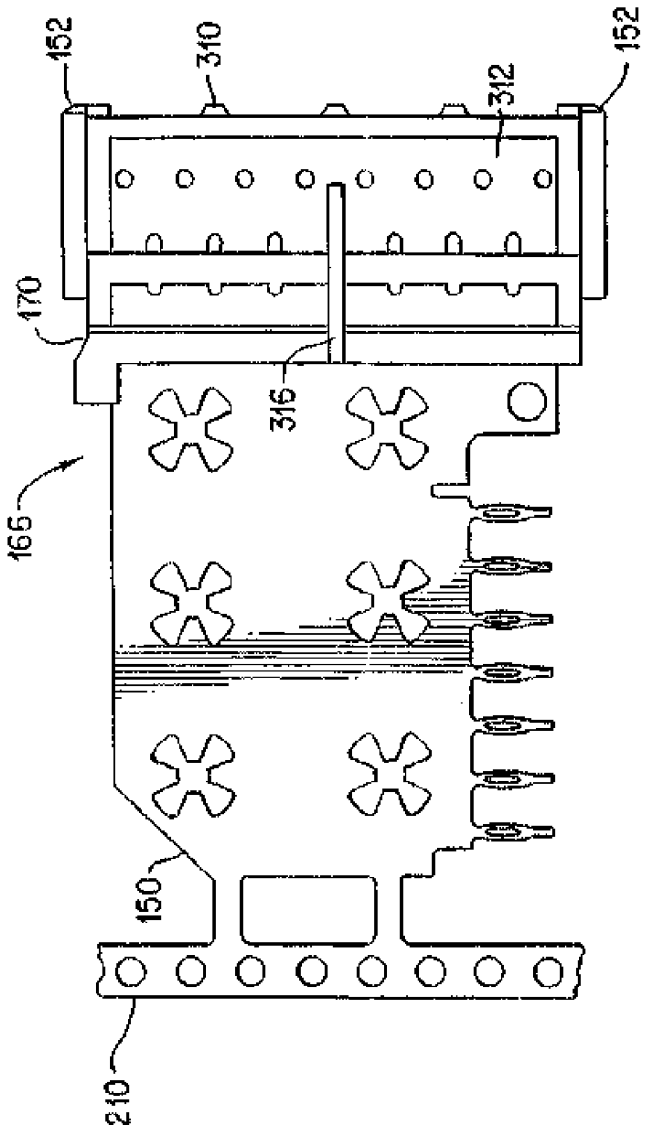

FIG. 3

【図４】

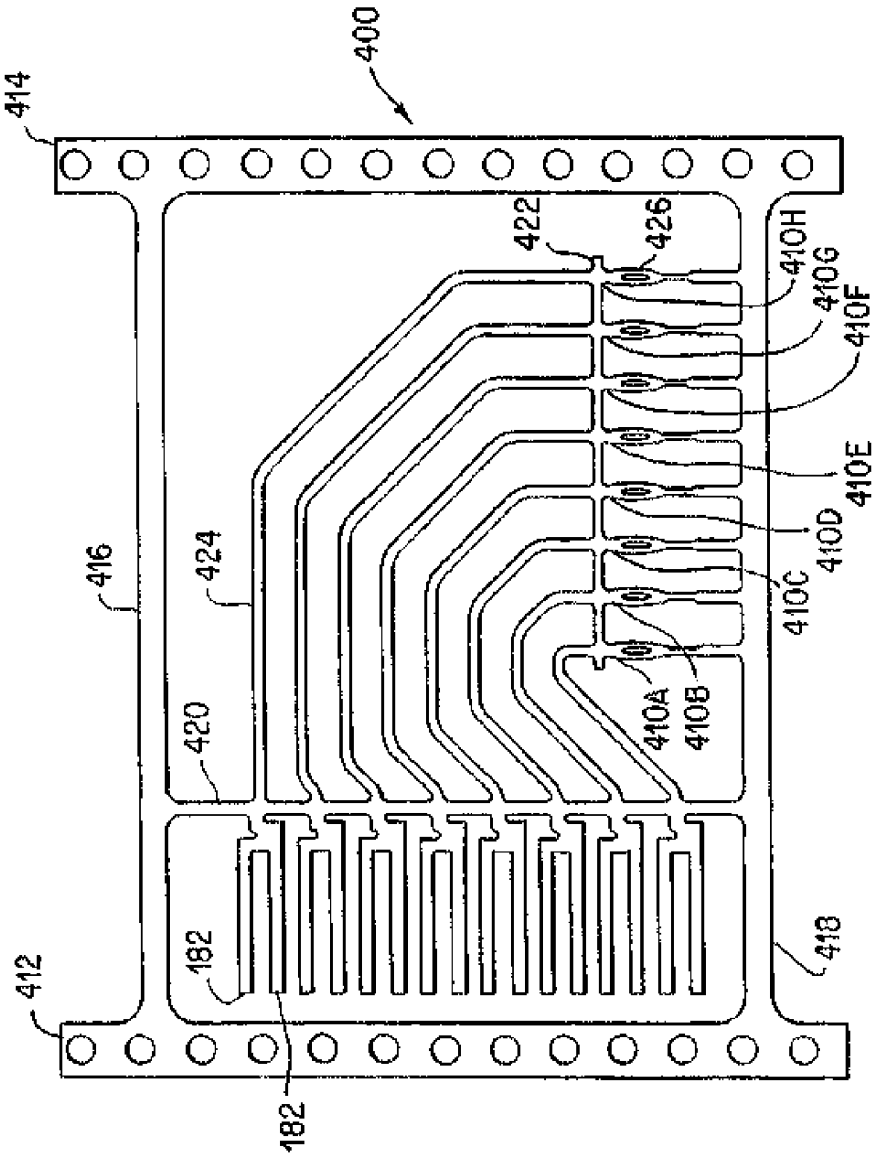
400
414
422
426
410H
410G
410F
410E
410D
410C
410A
410B
416
424
420
182
412
413
182

FIG. 4

【図５】

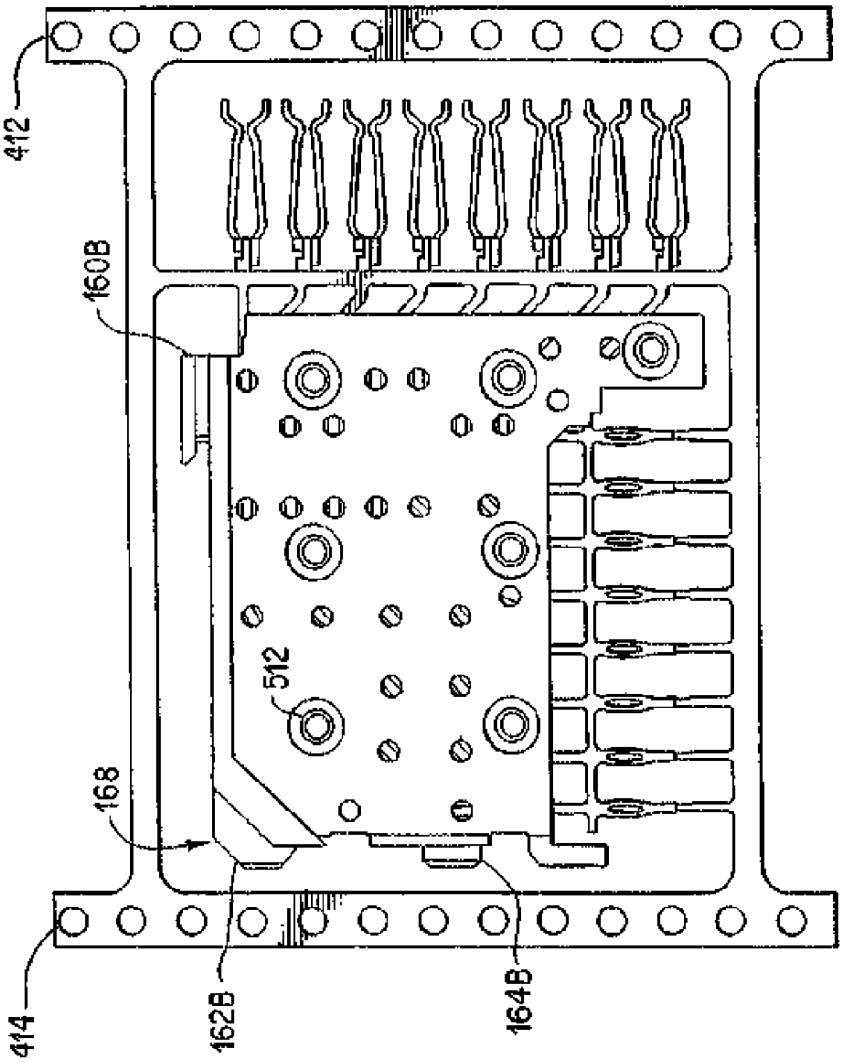

FIG.5

【図６】

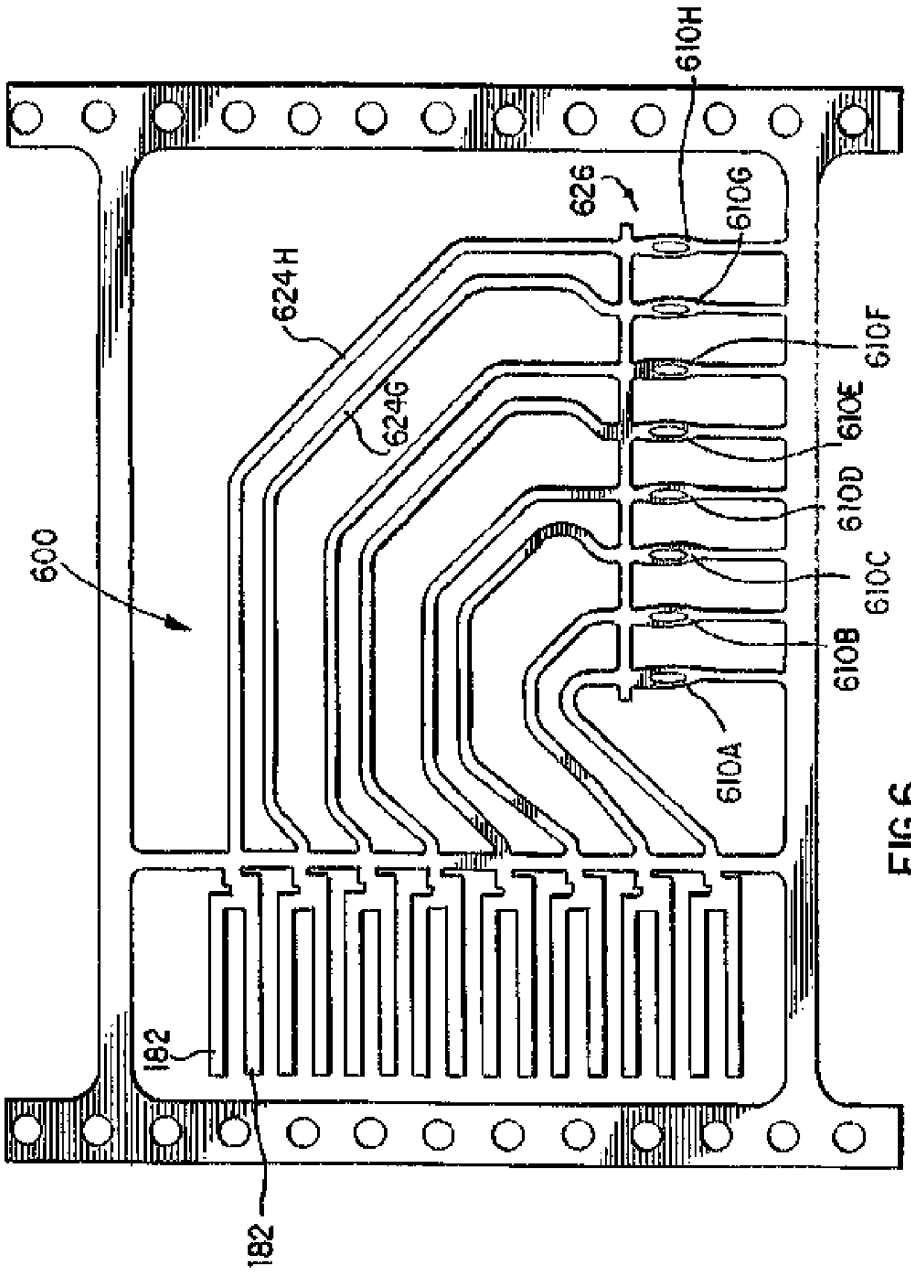
610H
626
610G
624H
610F
624G
610E
610D
600
610C
610B
610A
182
182

FIG.6

【図７】

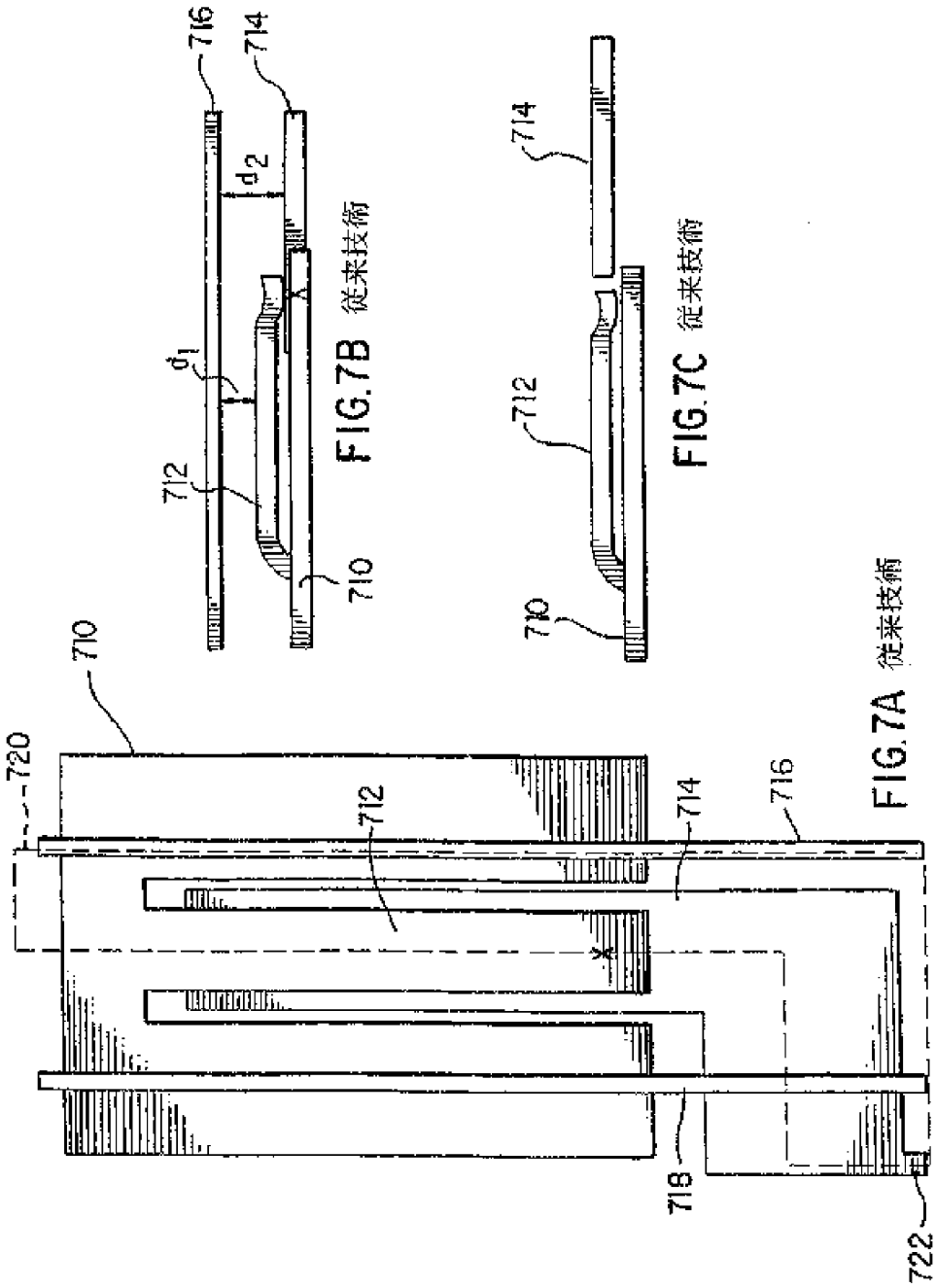

FIG.7B 従来技術

FIG.7C 従来技術

FIG.7A 従来技術

【図８】

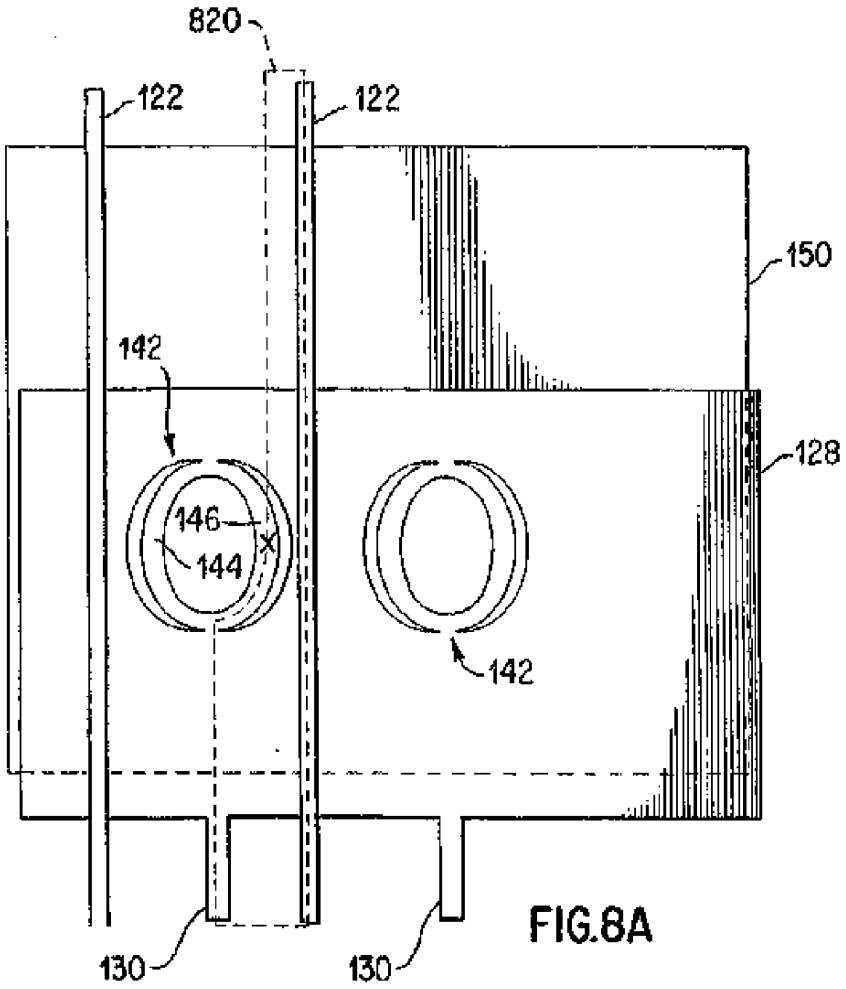

FIG.8A

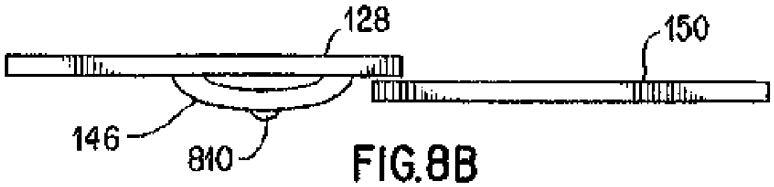

FIG.8B

FIG.8C

【図９】

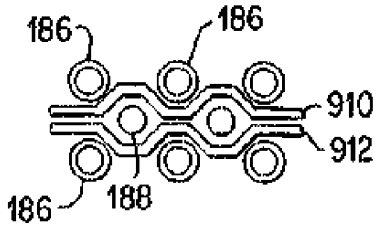

FIG.9A

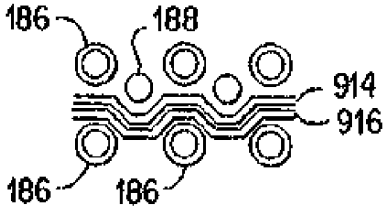

FIG.9B

【図１０】

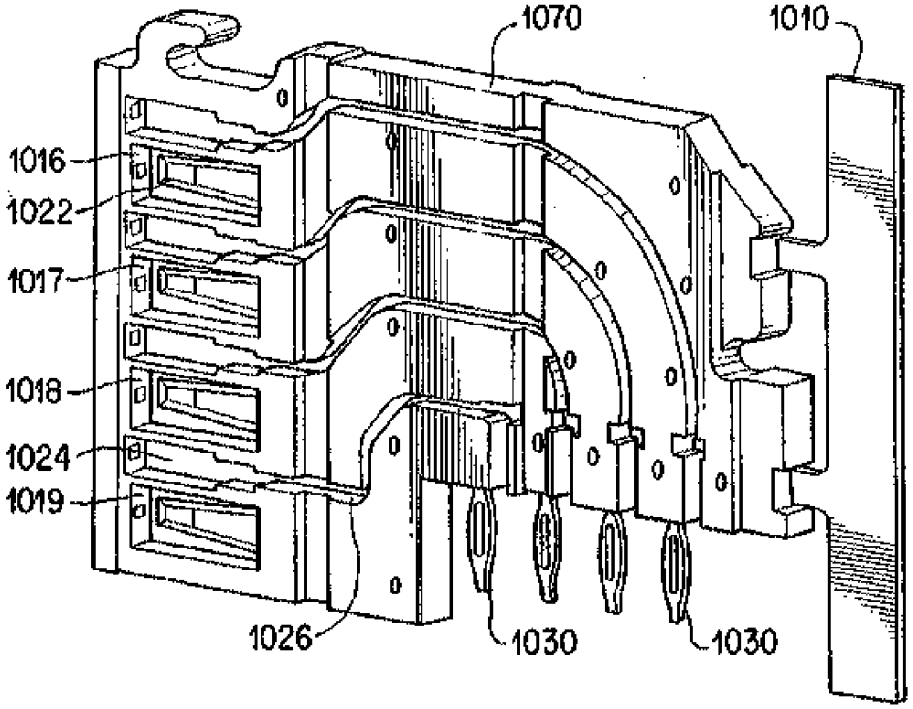

FIG.10

【図１１】

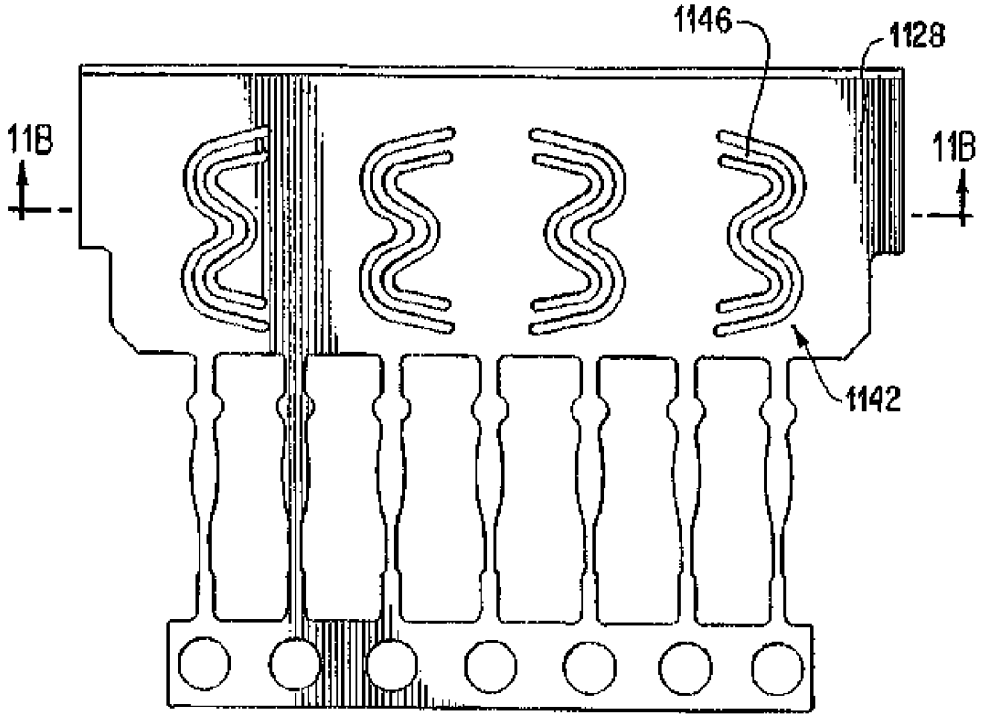

FIG.11A

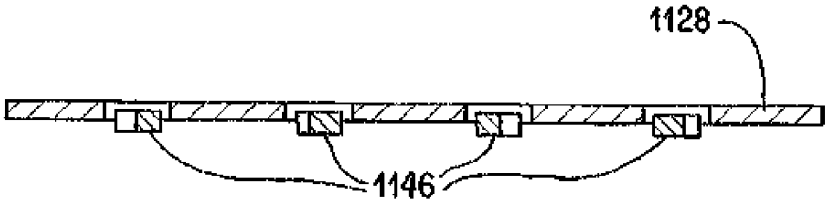

FIG.11B

【図１２】

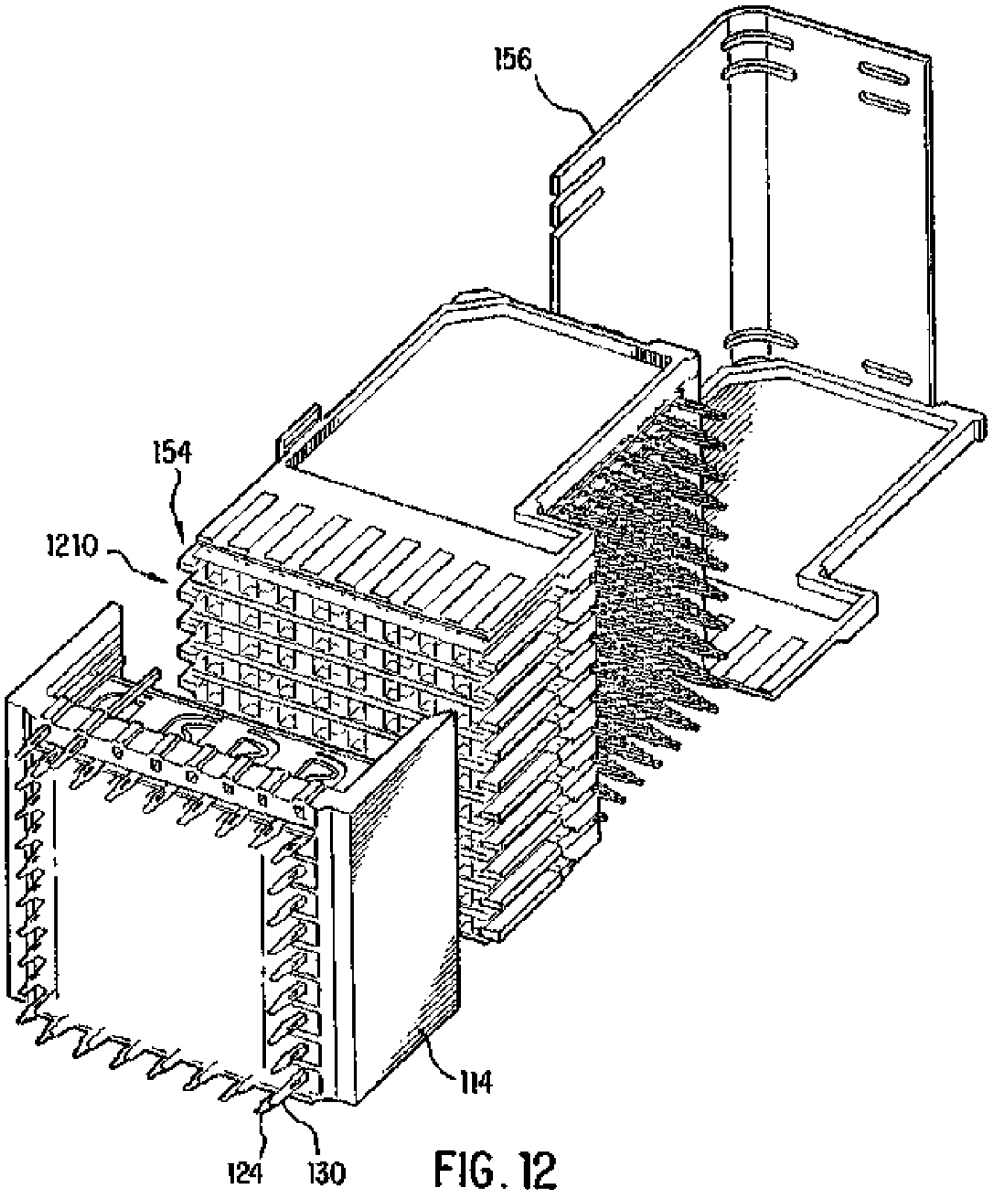

FIG. 12

【国際調査報告】

INTERNATIONAL SEARCH REPORT

Int. Appl. No PCT/US 98/01168

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01R23/68

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01R

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0 492 944 A (AMP INC) 1 July 1992 see column 3, line 28 - column 6, line 12 see column 7, line 13 - line 48 see figures 1-15	1,3,6, 8-14,16
A	DE 195 46 932 C (INOVAN STROEBE) 30 January 1997 see column 4, line 22 - column 5, line 19 see figures 1,2	1,3,6,8, 16-18
P,A	US 5 645 436 A (SHIMIZU MANABU ET AL) 8 July 1997 see column 5, line 54 - column 6, line 57 see column 8, line 34 - column 9, line 20 see figure 9	1,8,9,14

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
31 March 1998	22.04.98

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax (+31-70) 340-3016	Stirn, J-P

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

In ...ational Application No
PCT/US 98/01168

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0492944 A	01-07-92	US 5046960 A	10-09-91
		DE 69117703 D	11-04-96
		DE 69117703 T	19-09-96
		JP 4294076 A	19-10-92
		KR 9704221 B	26-03-97
DE 19546932 C	30-01-97	NONE	
US 5645436 A	08-07-97	JP 6243936 A	02-09-94

Form PCT/ISA/210 (patent family annex) (July 1992)

フロントページの続き

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03062、ナシュア、カバーフィールド・ドライブ 22

【公報種別】特許法第１７条の２の規定による補正の掲載
【部門区分】第７部門第１区分
【発行日】平成17年8月11日(2005.8.11)

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【公表日】平成13年7月31日(2001.7.31)
【出願番号】特願平10-534683
【国際特許分類第７版】
　Ｈ０１Ｒ　12/16
【ＦＩ】
　Ｈ０１Ｒ　23/68　　３０３Ｇ

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【提出日】平成16年12月1日(2004.12.1)
【手続補正１】
【補正対象書類名】明細書
【補正対象項目名】補正の内容のとおり
【補正方法】変更
【補正の内容】

手 続 補 正 書

平成１６年１２月 １日

特許庁長官 殿

１．事件の表示

平成１０年特許願第５３４６８３号

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氏 名 （８９７０） 弁理士 社 本 一 夫

住 所 同 所

担当者氏名 （７６６９） 弁理士 増 井 忠 弐

４．補正により増加する請求項の数 3

５．補正対象書類名

請求の範囲

６．補正対象項目名

請求の範囲

７．補正の内容

（１）請求の範囲を別紙の通り補正する。

方式審査

請求の範囲

1. a）ピンヘッダであって、

ｉ）絶縁性のベース、

ii）該絶縁性のベースに取り付けられた、ピンを備えた複数のコラム、及び

iii）前記絶縁性のベースに取り付けられた第１の複数の導電性板であって、各導電性板が隣接したピンを備えたコラムの間に配置されると共に、複数の撓じり接触子が内部に形成されている前記第１の複数の導電性板を備えたピンヘッダと、

b）ドーターカードコネクタであって、

ｉ）前記ピンヘッダの前記絶縁性のベースと嵌合する形状にされた絶縁性のベース、

ii）レセプタクルを備えた複数のコラムであって、各コラムが、前記複数のピンの１つに嵌合するように配置された複数のレセプタクルを有しているレセプタクルを備えた複数のコラム、及び

iii）第２の複数の導電性板であって、各導電性板が隣接するレセプタクルを備えたコラムの間に配置されると共に、前記ピンヘッダの前記複数の導電性板の１つの上の複数の撓じり接触子に係合するように配置されている前記第２の複数の導電性板を備えたドーターカードコネクタとを備えていることを特徴とする電気コネクタ。

2. a）前記ピンを備えた複数のコラムの各々が、第１の数のピンを含み、且つ、

b）前記ピンヘッダの前記第１の複数の導電性板の各々が、該導電性板から伸長する第２の数の接触子テールを有しており、該第２の数が前記第１の数と同等か、または、前記第１の数から１を引いた数より大きいことを特徴とする請求項１に記載の電気コネクタ。

3. 前記撓じり接触子の各々が、前記第１の複数の導電性板の１つから打ち抜かれた少なくとも１つのアームを備えており、該アームが、前記導電性板に２つ

の点で接続されると共に、該板の平面から逸脱するように屈曲されていることを特徴とする請求項１に記載の電気コネクタ。

４．　前記撚じり接触子の各々が、前記第１の複数の導電性板の１つから打ち抜かれた少なくとも１つのアームを備えており、該アームの厚さが、前記導電性板の厚さより薄いことを特徴とする請求項１に記載の電気コネクタ。

５．　前記同一のコラム内の隣接したレセプタクルが２mm以下の間隔で離置され、且つ、レセプタクルを備えた隣接したコラムが、２．２５mm以下の間隔で隔置されていることを特徴とする請求項１に記載の電気コネクタ。

６．　前記撚じり接触子の各々が、アームを有し、該アームが曲がりくねった形状を有していることを特徴とする請求項１に記載の電気コネクタ。

７．　前記ドーターカードコネクタが、複数のモジュールを備え、前記コネクタが、更に、前記複数のモジュールの各々が取り付けられる金属製の補強体を備えていることを特徴とする請求項１に記載の電気コネクタ。

８．　バックプレーンと、少なくとも１つのドーターカードとを備えたバックプレーン組立体に組み込まれる電気コネクタにおいて、

ａ）第１のコネクタ片であって、

ｉ）複数のピン状の形状をした信号接触子であって、各信号接触子が、前記バックプレーンに取り付けられたテール部を有し，前記ピンの形状をした信号接触子が複数の平行なコラム内に配置されている複数のピンの形状をした信号接触子，及び、

ii）第１の複数のシールド板であって，各シールド板が、信号接触子を備えた隣接したコラムの間に配置されると共に、該板から伸長すると共に前記バックプレーンに取り付けられた複数のテール部を有し，各シールド板の各テール部が、信号接触子を備えた前記同一コラム内で、隣接する信号接触子を備えたテール部の間に配置され、各シールド板に対して、信号接触子を備えた隣接したコラムの各対の隣接した信号接触子間に配置されたテール部が１つある第１の複数のシールド板を有する第１のコネクタ片と、

ｂ）第２のコネクタ片であって、

ｉ），複数のレセプタクル信号接触子であって、該複数の信号接触子

が、複数の平行なコラム内に、各レセプタクルがピンの形状をした信号接触子と係合するように配置された複数のレセプタクル信号接触子、及び、

ii）第２の複数のシールド板であって、各シールド板がレセプタクル信号接触子を備えた隣接したコラムの間に配置され、前記第２の複数のシールド板の各々が前記第１の複数のシールド板の１つと機械的に係合し、接触子アームが前記第１又は第２の複数のシールド板の１つ２つの点において取り付けられている第２の複数のシールド板を有している第２のコネクタ片とを備えていることを特徴とする電気コネクタ。

９．　信号接触子を備えた各コラムが、少なくとも６つの信号接触子を有していることを特徴とする請求項８に記載の電気コネクタ。

１０．　更に、所定のピンの形状をした信号接触子がその他のピンの形状をした信号接触子を横断しない時に、帰電流路を提供する手段を備え、該手段が、前記第１の複数のシールド板と、前記第２のシールド板とを含んでいることを特徴とする請求項８に記載の電気コネクタ。

１１．　前記信号接触子の前記テール部及び前記板の前記テール部が圧嵌テールであり、前記信号接触子の前記テール部が前記板の前記テール部に直角にされていることを特徴とする請求項８に記載の電気コネクタ。

１２．　前記第１の複数の板の一部にスロットが形成され、前記板が、該スロットに対して垂直なラインに沿って湾曲部を有し、該湾曲部に一方の側の前記板の前記一部がテール領域を形成し、該湾曲部の他方の側の前記板の前記一部がシールド領域を形成し、前記テール領域及びシールド領域が平行であり、前記テール部が前記板の前記テール領域に結合されていることを特徴とする請求項８に記載の電気コネクタ。

１３．　前記第１の複数の板の前記テール部が、バックプレーンに接地されていることを特徴とする請求項８に記載の電気コネクタ。

１４．　複数の信号接触子のコラムを有する第１のコネクタ片及び該第１のコネクタ片と第２のコネクタ片とが嵌合した時前記信号接触子に嵌合するようにした複数の信号接触子のコラムを有する第２のコネクタ片を備え、さらに下記の構成を有することを特徴とする電気コネクタ：

a）前記第１のコネクタ片の信号接触子の隣接する列同士の間に各々が配置された第１の複数のシールド板、

b）前記第２のコネクタ片の信号接触子の隣接する列同士の間に各々が配置された第２の複数のシールド板、

c）前記第１の複数のシールド板上または前記第２の複数のシールド板上にあって、前記第１のコネクタ片と第２のコネクタ片とが嵌合した時前記第１の複数のシールド板の各々が前記第２の複数のシールド板の一と平行になると共に複数の点で接触させられる複数の接触子。

１５．　前記第１のコネクタ片が、２つの側壁とそれぞれに形成されたスロットを備えたシュラウドに複数列の信号ピンを設けてなり、前記第１の複数のシールド板が前記側壁の前記スロットに係合するピンヘッダからなることを特徴とする請求項１４に記載の電気コネクタ。

１６．　前記第１または第２の複数のシールド板上に設けられた複数の接触子の各々が２つの点で該シールド板に取付けられ該シールド板の平面から折り曲げられたアームからなることを特徴とする請求項１５に記載の電気コネクタ。

１７．　前記シールド板の幅にわたって複数のアームを設けてなることを特徴とする請求項１６に記載の電気コネクタ。

１８．　複数の信号接触子の各々がテール部を有し、前記シールド板の各々が隣り合った信号接触子のテール部の間に複数のテール部を配置してなることを特徴とする請求項１４に記載の電気コネクタ。

１９．　前記第２コネクタ片が前記第２の複数のシールド板の各々と平行に整列した複数のウェファーからなり、前記第２のシールド板の各々に前記各ウェファーの側部から接近可能になされており、さらに前記ウェファーは前記第１のコネクタ片及び第２のコネクタ片が嵌合した時前記第１の複数のシールド板が隣接するウェファー間に嵌合して前記第２の複数のシールド板のうちの一と接触させられるようにしたことを特徴とする請求項１４に記載の電気コネクタ。

２０．　a）補強体、

b）前面が前記第１のコネクタ片に向き合い後部が前記補強体に取付けられたウェファーであって、隣接したウェファーの前面同士の間に

スロットを残置し、前記第１の複数のシールド板が該スロットに挿入されるようにしてなる複数のウェファー、

をさらに備えたことを特徴とする請求項１４に記載の電気コネクタ。

２１．　前記ウェファーの各々がハウジング内に固定された信号接触子の一のカラムを含むことを特徴とする請求項１９に記載の電子コネクタ。

２２．　前記第２のコネクタ片の信号接触子がレセプクル接触子からなることを特徴とする請求項１４に記載の電気コネクタ。

２３．　前記第１のコネクタ片がバックプレーンに取付けられ、前記第２のコネクタ片がドーターカードに取付けられていることを特徴とする請求項１４に記載の電気コネクタ。

13. (MXPA/a/1999/007324) HIGH SPEED, HIGH DENSITY ELECTRICAL CONNECTOR

Application Number: PA/a/1999/007324 **Application Date:** 09.08.1999

Publication Number: PA/a/1999/007324 **Publication Date:** 01.08.2000

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Applicants: TERADYNE, INC.

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Agents: HEDWIG A. LINDNER LOPEZ.

Priority Data: 08797537 07.02.1997 US

Title: **(EN)** HIGH SPEED, HIGH DENSITY ELECTRICAL CONNECTOR
(ES) CONECTOR ELECTRICO DE ALTA VELOCIDAD Y ALTA DENSIDAD

Abstract: **(EN)** A high speed, high density electrical connector for use with printed circuit boards. The connector is in two pieces with one piece having pins and shield plates and the other having socket type signal contacts and shield plates. The shields have a grounding arrangement which is adapted to control the electromagnetic fields, for various system architectures, simultaneous switching configurations and signal speeds, allowing all of the socket type signal contacts to be used for signal transmission. Additionally, at least one piece of the connector is manufactured from wafers, with each ground plane and signal column injection molded into components which, when combined, form a wafer. This construction allows very close spacing between adjacent columns of signal contacts as well as tightly controlled spacing between the signal contacts and the shields. It also allows for easy and flexible manufacture, such as a connector that has wafers intermixed in a configuration to accommodate single ended, point to point and differential applications.
(ES) Un conector eléctrico de alta densidad y alta velocidad que se utiliza con tableros de circuito impreso. El conector es de dos piezas, una de las piezas tiene patillas y placas de blindaje y la otra pieza tiene contactos de señal de tipo receptáculo y placas de blindaje. Los blindajes tienen un arreglo de tierra que estáadaptado para controlar los campos electromagnéticos, para varios sistemas de arquitecturas, configuraciones de conmutación simultáneas y velocidades de señal, permitiendo que todos los contactos de señal tipo receptáculo se utilicen para transmisión de señal. Adicionalmente, por lo menos una pieza del conector estáfabricada a partir de plaquitas, con cada plano de tierra y columna de señal moldeado por inyección en los componentes que, cuando se combinan, forman una plaquita. Esta construcción permite una separación muy estrecha entre columnas adyacentes de contactos de señal asícomo el control rígido de la separación entre los contactos de señal y los blindajes. También permite la manufactura fácil y flexible, de manera que un conector que tiene plaquitas intermezcladas en una configuración para acomodar aplicaciones de un solo extremo, punto a punto y de tipo diferencial.

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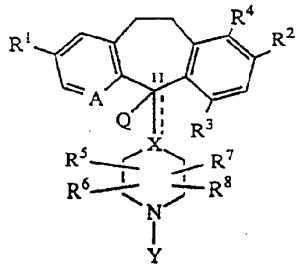

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(57) Abstract

Novel phenyl–substituted tricyclic compounds of formula (1.0) and pharmaceutical compositions are disclosed which are inhibitors of the enzyme, farnesyl protein transferase. Also disclosed is a method of inhibiting Ras function and therefore inhibiting the abnormal growth of cells. The method comprises administering the novel halo–N–substituted urea compound to a biological system. In particular, the method inhibits the abnormal growth of cells in a mammal such as a human.

CONECTOR ELÉCTRICO DE ALTA VELOCIDAD Y ALTA DENSIDAD

CAMPO DE LA INVENCIÓN

Esta invención se relaciona en general con conectores eléctricos que se utilizan para interconectar tableros de circuito impreso y, más específicamente, conectores diseñados para llevar muchas señales de alta velocidad.

ANTECEDENTES DE LA INVENCIÓN

Los conectores eléctricos se utilizan en muchos sistemas electrónicos. En general es más fácil y más económico elaborar un sistema sobre varios tableros de circuito impreso que van a unirse entre sí con conectores eléctricos. Un arreglo tradicional para varios tableros de circuito impreso es que un tablero de circuito impreso sirva como un plano trasero. Otros tableros de circuito impreso, llamados tableros secundarios, se conectan a través del plano trasero.

Un plano trasero tradicional es un tablero de circuito impreso que tiene muchos conectores. Los trazos conductores en el tablero de circuito impreso se conectan a las patillas de señal en los conectores, de manera que las señales podrán enrutarse entre los conectores. Otros tableros de circuito impreso denominados "tableros

secundarios" contienen también conectores que se conectan a los conectores del plano trasero. De esta manera, las señales son enrutadas entre los tableros secundarios a través del plano trasero. Las tarjetas secundarias normalmente se enchufan al plano trasero en un ángulo recto. Los conectores que se utilizan para estas aplicaciones contienen un doblez en ángulo recto y normalmente se denominan "conectores de ángulo recto".

Los conectores se utilizan también en otras configuraciones para interconectar tableros de circuito impreso e incluso para conectar cables a los tableros de circuito impreso. Algunas veces, uno o más tableros de circuito impreso pequeños están conectados a otro tablero de circuito impreso más grande. El tablero de circuito impreso grande recibe el nombre de "tablero madre" y el tablero de circuito impreso que se enchufa a éste se denomina tablero secundario. También, los tableros del mismo tamaño algunas veces se alinean en paralelo. Los conectores utilizados en estas aplicaciones algunas veces se denominan "conectores de apilación" o "conectores mezzanine".

Sin importar la aplicación exacta, los diseños de conectores eléctricos en general se han necesitado para reflejar las tendencias de la industria electrónica. Los sistemas electrónicos en general se han hecho más pequeños

y más rápidos. También manejan mucho más datos que los sistemas construidos hace solo algunos años. Estas tendencias nos señalan que los conectores eléctricos deben llevar más señales de datos y en forma más rápida en un espacio más corto sin degradar la señal.

Los conectores pueden elaborarse para que lleven más señales en menos espacio colocando los contactos de señal en el conector más cercanos entre sí. Estos conectores se denominan "conectores de alta densidad". La dificultad de colocar los contactos de señal más cercanos entre sí es que hay un acoplamiento electromagnético entre los contactos de señal. A medida que los contactos de señal se colocan más cercanos entre sí, el acoplamiento electromagnético aumenta. El acoplamiento electromagnético también aumenta a medida que la velocidad de las señales aumenta.

En un conductor, la cantidad de acoplamiento electromagnético se indica midiendo la "interferencia" del conector. La interferencia en general se mide colocando una señal en uno o más contactos de señal y midiendo la cantidad señal acoplada a otro contacto de señal. La elección de cuáles contactos de señal se utilizan para las mediciones de interferencia así como las conexiones a los otros contactos de señal influirán en el valor numérico de la medición de la interferencia. Sin embargo, cualquier

medida confiable de interferencia debe mostrar que la interferencia aumenta a medida que la velocidad de las señales aumenta y también que los contactos de señal se colocan más cercanos entre sí.

Un método tradicional para reducir la interferencia es poner a tierra las patillas de señal dentro del campo de las patillas de señal. La desventaja de este planteamiento es que reduce la densidad de señal efectiva de la densidad del conector.

Para hacer que el conector sea tanto de alta densidad como de alta velocidad, los diseñadores de conectores han insertado miembros de blindaje entre los contactos de señal. Los blindajes reducen el acoplamiento electromagnético entre los contactos de señal contrarrestando así el efecto de la poca separación o de la alta frecuencia de las señales. El blindaje, si se configura adecuadamente, también puede controlar la impedancia de las trayectorias de señal a través del conector, que también puede mejorar la integridad de las señales llevadas por el conector.

Un uso temprano del blindaje se muestra en la exposición de la patente Japonesa 49-6543 de Fujitsu, Ltd. de fecha 15 de febrero de 1974. Las patentes de los Estados Unidos 4,632,476 y 4,806,107, ambas cedidas a AT&T Bell Laboratories, muestran diseños de conector en los que

los blindajes se utilizan entre las columnas de los contactos de señal. Estas patentes describen conectores en los que los blindajes corren en forma paralela a los contactos de señal a través tanto del tablero secundario como de los conectores del plano trasero. Se utilizan vigas en voladizo para hacer los contactos eléctricos entre el blindaje y los conectores del plano trasero. Las Patentes 5,433,617; 5,429,521; 5,429,520 y 5,433,618, todas cedidas a Framatome Connectors International, muestran un arreglo similar. La conexión eléctrica entre el plano trasero y el blindaje se elabora, sin embargo, con un contacto tipo resorte.

Otros conectores tienen a la placa de blindaje solamente dentro del conector de la tarjeta secundaria. Los ejemplos de estos diseños conectores pueden encontrarse en las patentes 4,846,727; 4,975,084; 5,496,183; 5,066,236, todas ellas cedidas a AMP, Inc. Otro conector con blindaje solamente dentro del conector del tablero secundario se muestra en la patente de los Estados Unidos 5,484,310, cedida a Teradyne, Inc.

A partir de varias de las patentes que describen conectores que utilizan blindajes para reducir la interferencia, se apreciará que la colocación y conexión de los blindajes puede ocasionar un gran efecto sobre el desempeño eléctrico del conector. La configuración

específica del blindaje también puede tener un impacto considerable sobre las propiedades mecánicas del conector. Por ejemplo, la manera en la que se hace la conexión eléctrica con el blindaje puede influir en que haya o no "anclaje" cuando se acoplan los conectores. Anclaje (stubbing) significa que un contacto queda atrapado en otro contacto. Cuando hay anclaje, uno de los contactos normalmente queda dañado, requiriendo que el conector sea reparado o reemplazado.

Sería muy deseable contar con un arreglo de blindaje que sea altamente eficaz para reducir la interferencia entre contactos de señal. También sería bastante deseable si el arreglo de blindaje fuera mecánicamente resistente (robusto). También sería deseable que el conector fuera de fácil manufactura. También es bastante deseable controlar reflexiones de señal al controlar la geometría del blindaje y de los contactos de señal en el acoplamiento de impedancia de la conexión.

SUMARIO DE LA INVENCIÓN

Con los anteriores antecedentes en menta, un objeto de la invención es proporcionar un conector de alta densidad y alta velocidad.

Otro objeto de la presente invención es proporcionar un conector de alto desempeño que permita que

todos estos contactos de señal se utilicen para llevar a cabo las señales.

También un objeto de la presente es un conector eléctrico que sea mecánicamente resistente (robusto).

Otro objeto de la invención es proporcionar un conector de fácil manufactura.

Los objetos anteriores y otros se logran en un conector eléctrico que tiene placas de blindaje entre hileras de los contactos de señal tanto en los conectores del tablero secundario como en los conectores del plano trasero. Las placas de blindaje en el conector del plano trasero tienen contactos torsionales. Los contactos torsionales reducen significativamente la posibilidad de anclaje. También proporcionan un patrón altamente deseable de flujo de corriente a través de los blindajes, lo que aumenta su efectividad para reducir el acoplamiento inductivo entre contactos de señal y la interferencia resultante.

BREVE DESCRIPCIÓN DE LOS DIBUJOS

La invención se comprenderá mejor en relación a la siguiente descripción más detallada y a los dibujos que se acompañan, en donde:

la Figura 1 es una vista en despiece de un conector elaborado de acuerdo a la invención;

la Figura 2 es un modelo de placa de blindaje utilizado en el conector de la Figura 1;

la Figura 3 es una vista del modelo de placa de blindaje de la Figura 2 después de que se inserta por moldeo en un elemento de alojamiento;

la Figura 4 es un modelo de contacto de señal utilizado en el conector de la Figura 1;

la Figura 5 es una vista del modelo de contacto de señal de la Figura 4 después de que se ha insertado por moldeado dentro de un elemento de alojamiento;

la Figura 6 es una modalidad alternativa del modelo de contacto de señal de la Figura 4, adecuado para utilizarse en la elaboración de un módulo diferencial;

las Figuras 7A-7C son vistas operacionales de un conector de la técnica anterior;

las Figuras 8A-8C son vistas operacionales similares del conector de la Figura 1;

las Figuras 9A y 9B son patrones de trazo de señal y orificio de plano trasero para las modalidades de un solo extremo y diferencial de la invención, respectivamente; y

la Figura 10 es una vista de una modalidad alternativa de la invención;

la Figura 11A es una modalidad alternativa de la placa 128 de la Figura 1;

la Figura 11B es una vista en sección transversal tomada a través de la línea B-B de la Figura 11A;

la Figura 12 es una vista isométrica de un conector de acuerdo a la invención.

DESCRIPCIÓN DE LA MODALIDAD PREFERIDA

La Figura 1 muestra una vista en despiece de la unidad de plano trasero 100. El plano trasero 110 tiene un cabezal de patilla 114 unido a éste. La tarjeta secundaria 112 tiene un conector 116 de tarjeta secundaria unido a la misma. El conector 116 de tarjeta secundaria puede acoplarse con el cabezal 114 de la patilla para formar un conector. La unidad de plano trasero igualmente tiene muchos otros cabezales de patilla unidos a la misma de manera que pueden conectarse a ésta varias tarjetas secundarias. Además muchos cabezales de patilla pueden estar alineados extremo con extremo, de manera que puedan utilizarse muchos cabezales de patilla para conectarse a una tarjeta secundaria. Sin embargo, por claridad, solo se muestra una porción de la unidad de plano trasero y una sola tarjeta secundaria 112.

El cabezal de patilla 114 se forma a partir de la gualdera 120. La gualdera 120 de preferencia se moldea por inyección a partir de un plástico, poliéster u otro material aislante adecuado. La gualdera 120 sirve como la

base para el cabezal 114 de patilla.

El piso (que no lleva número) de la gualdera 120 contiene columnas de orificio 126. Las patillas 122 están insertadas dentro de los orificios 126 con sus colas 124 extendiéndose a través de la superficie inferior de la gualdera 120. Las colas 124 se colocan a presión dentro de los orificios 136 de señal. Los orificios 136 son orificios pasantes chapados en la placa trasera 110 y sirven para conectar eléctricamente las patillas 122 a los trazos (no mostrados) en el plano trasero 110. Por claridad de ilustración, solo se muestra una patilla 122. sin embargo, el cabezal 114 de patilla contiene muchas columnas paralelas de patillas. En una modalidad preferida, hay ocho hileras de patillas en cada columna.

La separación entre cada columna de patillas no es crítica. Sin embargo, un objeto de la invención es permitir que las patillas se coloquen estrechamente cercanas entre sí, de manera que pueda formarse un conector de alta densidad. A vía de ejemplo, las patillas dentro de cada columna pueden estar separadas en 2.25 mm y las columnas de las patillas pueden estar separadas en 2 mm. Las patillas 122 pudieran elaborarse por estampado de aleación de cobre con 0.4 mm de espesor.

La gualdera 120 contiene una ranura 132 formada en su piso que corre en sentido paralelo a la columna de

orificio 126. La gualdera 120 también tiene ranuras 134 formadas en sus paredes laterales. La placa de gualdera 128 se ajusta dentro de las ranuras 132 y 134. Las colas 130 se proyectan a través de los orificios (no visibles) en el fondo de la ranura 132. Las colas 130 se acoplan a los orificios de tierra 138 en el plano trasero 110. Los orificios de tierra 138 son orificios pasantes chapados que se conectan a los trazos de tierra en el plano trasero 110.

En la modalidad ilustrada, la placa 128 tiene siete colas 130. Cada cola 130 cae entre dos patillas adyacentes 122. Sería deseable que el blindaje 128 tuviera una cola 130 lo más cercana posible a cada patilla 122. Sin embargo, el centrado de las colas 130 entre las patillas de señal adyacente 122 permitan que se reduzca la separación entre el blindaje 128 y una columna de patillas de señal 122.

La placa de blindaje 128 tiene varios contactos 142 de viga torsional, formados en la misma. Cada contacto 142 se forma por brazos de estampado 144 y 146 en la placa 128. Los brazos 144 y 146 se doblan entonces hacia fuera de la placa 128 del plano. Los brazos 144 y 146 son lo suficientemente largos para que se flexionen cuando se presionan hacia atrás hacia el interior del plano de la placa 128. Los brazos 144 y 148 son suficientemente resilientes para proporcionar una fuerza de resorte cuando

se presionan hacia el plano de la placa 128. La fuerza de resorte generada por los brazos 144 y 146 crea un punto de contacto entre cada brazo 144 o 146 y la placa 150. La fuerza de resorte generada debe ser suficiente para asegurar este contacto, incluso después de que el conector 116 de la tarjeta secundaria se haya acoplado y desacoplado repetidamente del cabezal 114 de patilla.

Durante la manufactura, los brazos 144 y 146 están acuñados. El acuñamiento reduce el espesor del material y aumenta la flexibilidad de las vigas sin debilitar la placa 128.

Para un mejor desempeño eléctrico se desea que los brazos 144 y 146 sean lo más corto y recto posibles. Por lo tanto, se elaboran solo de la longitud que se requiera para proporcionar la fuerza de resorte requerida. Además, para el desempeño eléctrico, se desea que haya un brazo 144 ó 146 lo más cercano posible a cada patilla 122 de señal. Idealmente, tendría que haber un brazo 144 y 146 para cada patilla 122 de señal. Para la modalidad ilustrada con las ocho patillas de señal 122 por columna, habría idealmente ocho brazos 144 ó 146, haciendo un total de cuatro contractos 142 de viga torsional equilibrados. Sin embrago, solo tres contactos 142 de viga torsional equilibrados se muestran. Esta configuración representa un compromiso entre la fuerza de resorte requerida y las

propiedades eléctricas deseadas.

Las ranuras 140 sobre el blindaje 120 tienen la función de alinear el conector 116 de tarjeta secundaria con el cabezal 114 de la patilla. Las lengüetas 152 se ajustan dentro de la ranura 140 para el alineamiento y para evitar el movimiento lateral del conector 116 de la tarjeta secundaria en relación al cabezal 114 de la patilla.

El conector 116 de la tarjeta secundaria se elabora de plaquitas 154. Solo una plaquita 154 se muestra con claridad, pero el conector 116 de la tarjeta secundaria tiene, en una modalidad preferida, varias plaquitas apiladas lado a lado. Cada plaquita 154 contiene una columna de receptáculo 158. Cada receptáculo 158 se acopla con una patilla 122 cuando el cabezal 114 de patilla y el conector 116 de la tarjeta secundaria se acoplan. De esta manera, el conector 116 de la tarjeta secundaria se elabora de tantas plaquitas como columnas de patilla hay en el cabezal 114 de patilla.

Las plaquitas 154 están soportadas en un rigidizador 156. El rigidizador 156 de preferencia se forma por estampado de una tira metálica. Se estampa con características para sostener la plaquita 154 en una posición requerida sin rotación y por lo tanto incluye de preferencia tres puntos de unión. El rigidizador 156 tiene la ranura 160A formada a lo largo de su borde frontal. La

lengüeta 160B se acopla dentro de la ranura 160A. El rigidizador 156 incluye también orificios 162A y 164A. Los bornes 162B y 164B se ajustan dentro de los orificios 162A y 164A. Los bornes 162B y 164B están dimensionados para proporcionar un ajuste de interfaz en los orificios 162A y 164A.

La Figura 1 muestra solo unas cuantas de las ranuras 160A y los orificios 162A y 164A, por claridad. El patrón de ranuras y orificios se repite a lo largo de la longitud del rigidizador 156 en cada punto en donde va a unirse una plaquita 156.

En la modalidad ilustrada, la plaquita 154 se elabora de dos piezas, la pieza de blindaje 166 y una pieza de señal 168. La pieza de blindaje 166 se forma insertando el alojamiento de moldeo 170 alrededor de la porción frontal del blindaje 150. La pieza de señal 168 se elabora insertando el alojamiento de moldeo 172 alrededor de los contactos 410A...410H (Figura 4).

La pieza de señal 168 y la pieza de blindaje 166 tienen características que mantienen a las dos piezas juntas. La pieza de señal 168 tiene los bornes 512 (Figura 5) formado sobre una superficie. Los bornes se alinean con las pinzas 174 y se insertan dentro de las mismas, estando estas cortadas dentro de los blindajes 150. Las pinzas 174 acoplan a los bornes 512 y sostienen a la placa 150

firmemente contra la pieza de señal 168.

El alojamiento 170 tiene cavidades 176 formadas en el mismo. Cada cavidad 176 está conformada para recibir uno de los receptáculos 158. Cada cavidad 176 tiene a la plataforma 178 en su fondo. La plataforma 178 tiene un orificio 180 formado a través de la misma. El orificio 180 recibe a una patilla 122 cuando el conector 116 de tarjeta secundaria se acopla con el cabezal 114 de patilla. Por lo tanto, las patillas 122 se acoplan con los receptáculos 158, proporcionando una trayectoria de señal a través del conector.

Los receptáculos 158 se forman con dos patas 182. Las patas 182 se ajustan en lados opuestos de la plataforma 178 cuando los receptáculos 158 se insertan dentro de las cavidades 176.

Los receptáculos 158 se forman de manera que la separación entre las patas 182 sea más pequeña que la anchura de la plataforma 178. Para insertar los receptáculos 158 dentro de la cavidad 176 es por lo tanto necesario utilizar una herramienta para separar las patas 182.

Los receptáculos forman lo que se conoce como un contacto precargado. Los contactos precargados que se forman tradicionalmente presionando al receptáculo contra una plataforma en forma de pirámide. El vértice de la

plataforma abre las patas a medida que el receptáculo es empujado hacia abajo sobre éstas. Este contacto tiene una fuerza de inserción menor y es menos probable que produzca anclaje sobre la patilla cuando se acoplan los dos conectores. Los receptáculos de la invención proporcionan las mismas ventajas pero estas se logran insertando los receptáculos desde un lado y no presionándolos contra una pirámide.

El alojamiento 172 tiene las ranuras 184 formadas en el mismo. Como se describió antes, los bornes 512 (Figura 5) se proyectan a través de la placa 150. Cuando las dos plaquitas se apilan lado con lado, los bornes 512 de una plaquita 154 se proyectarán dentro de las ranuras 184 de una plaquita adyacente. Los bornes 512 y las ranuras 184 ayudan a sostener a las plaquitas adyacentes juntas y evitar la rotación de la plaquita respecto a la siguiente plaquita. Estas características, junto con el rigidizador 156 eliminan la necesidad de una caja o alojamiento separado para sujetar a las plaquitas, simplificando así el conector.

Los alojamientos 170 y 172 se muestran con varios orificios (que no tienen número). Estos orificios no son críticos para la invención. Son "orificios de apriete" utilizados para sujetar las placas 150 o los contactos de receptáculo 410 durante el moldeo por inyección. Se desea

sujetar estas piezas durante el moldeo por inyección para conservar una separación uniforme entre las placas y los contactos de receptáculo en el producto terminado.

La Figura 2 muestra con mayor detalle el modelo o blanco utilizado para elaborar la placa 150. En una modalidad preferida, las placas 150 se estampan a partir de un rollo de metal. Las placas se retienen sobre la tira portadora 210 para facilitar el manejo. Después de que la placa 150 se moldea por inyección para formar una pieza de blindaje 166, la tira portadora puede cortarse.

Las placas 150 incluyen orificios 212. Los orificios 212 se llenan con plástico a partir del alojamiento 170, de esta manera traban la placa 150 en el alojamiento 170.

La placa 150 incluye también ranuras 214. Las ranuras 214 se colocan para que queden entre los receptáculos 158. Las ranuras 214 sirven para controlar la capacitancia de la placa 150, que puede elevar o disminuir en forma global la impedancia del conector. También pueden canalizar el flujo de corriente en la placa cerca de los receptáculos 158, que son trayectorias de señal. Mientras más alto es el flujo de corriente de retorno cerca de las trayectorias de señal se reduce más la interferencia.

La ranura 216 es similar a las ranuras 214 pero es más grande para permitir que un dedo 316 (Figura 3) pase

a través de la placa 150 cuando ésta se moldea para dar un alojamiento 170. El dedo 316 es un dedo pequeño de material aislante que pudiera ayudar a sostener una placa 128 contra la placa 150. El dedo 316 es opcional y pudiera omitirse. Obsérvese en la Figura 1 que las dos cavidades centrales 176 tienen su pared intermedia retirada parcialmente. El dedo 316 de una plaquita adyacente 154 (no mostrada) se ajustaría dentro de este espacio para completar la pared entre las dos cavidades centrales. El dedo 316 se extendería más allá del alojamiento 170 y se ajustaría dentro de una ranura 184B de una plaquita adyacente (no mostrada).

La ranura 218 permite que la región de cola 222 se doble hacia fuera del plano de la placa 150, si se desea. La Figura 9A muestra trazos 910 y 912 sobre un tablero de circuito impreso dirigidos entre los orificios utilizados para montar un conector de acuerdo a la invención. La Figura 9A muestra porciones de una columna de orificios de señal 186 y porciones de una columna de contactos de tierra 188. Cuando el conector se utiliza para llevar señales de un solo extremo, se desea que los trazos 910 y 912 estén separados por tierra en el mayor grado posible. Por lo tanto, se desea que los orificios de tierra 188 estén centrados entre la columna de orificios de señal 186 de manera que los trazos de señal 910 y 912

puedan dirigirse entre los orificios de señal 186 y los orificios de tierra 188. Por otra parte, la Figura 9B muestra el enrutamiento preferido para las señales de par diferencial. Para las señales de par diferencial se desea que los trazos sean dirigidos lo más cercanos posibles. Para permitir que los trazos 914 y 916 se cierren entre sí, los orificios de tierra 188 no están centrados entre las columnas de los orificios de señal 186. Por el contrario, están desplazados para estar lo más cerca posible de la hilera de contactos de señal 186. Esta colocación permite que los dos trazos de señal 914 y 916 se enruten entre los orificios de tierra 188 y una columna de orificios de señal 186. En la configuración de un solo extremo, la región de cola 222 se dobla hacia fuera del plano de la placa 150. Para la configuración diferencial, ésta no se dobla.

También debe observarse que la placa 128 (Figura 1) puede similarmente doblarse en su región de cola, si se desea. En la modalidad preferida, aunque la placa 128 no esté doblada para las señales de un solo extremo y esté doblada para las señales diferenciales.

Las lengüetas 220 están dobladas fuera del plano de la placa 150 antes del moldeo por inyección del alojamiento 170. Las lengüetas 220 se enrollarán entre los orificios 180 (Figura 1). Las lengüetas 220 ayudan a asegurar que la placa 150 se adhiera al alojamiento 170.

También refuerzan al alojamiento 170 a través de su cara, es decir, la superficie orientada hacia el cabezal 114 de las patillas.

La Figura 3 muestra al blindaje 150 después de que ha sido insertado por moldeo dentro del alojamiento 170 para formar la porción de tierra 166. La Figura 3 muestra que el alojamiento 170 incluye las proyecciones 310 en forma de pirámide sobre la cara de la pieza 166 del blindaje. Los rebajes acoplantes (no mostrados) están incluidos en el piso del cabezal 114 de patilla. Las proyecciones 310 y los rebajes acoplantes sirven para evitar que la fuerza de resorte de los contactos 142 de viga torsional separen a las plaquitas adyacentes 154 cuando el conector 116 de tarjeta secundaria se inserta dentro del cabezal 114 de patilla.

La Figura 4 muestra un blanco o modelo 400 para el contacto de receptáculo. El blanco modelo para contacto de receptáculo de preferencia se estampa de una hoja de metal. Varios blancos se estampan en un rollo. En la modalidad preferida, hay ocho contactos de receptáculo 410A...410H. Los contactos de receptáculo 410 se mantienen juntos sobre las tiras portadoras 412, 414, 416, 418 y 422. Estas tiras portadoras se seccionan para contactos separados 410A...410H después de que el alojamiento 172 se ha moldeado alrededor de los contactos. Las tiras

portadoras pueden retenerse durante la mayor parte de la operación de manufactura para el fácil manejo de las porciones de receptáculo 168.

Cada uno de los contactos de receptáculo 410A...410H incluye dos patas 182. Las patas 182 se pliegan y doblan para formar el receptáculo 158.

Cada contacto de receptáculo 410A...410H incluye también una región de transmisión 424 y una región de cola 426. La Figura 4 muestra que las regiones de transmisión 424 están separadas equidistantemente. Este arreglo se prefiere para señales de un solo extremo, ya que da por resultado la máxima separación entre los contactos.

La Figura 4 muestra que las regiones de cola son adecuadas para ajustarse a presión dentro de los orificios pasantes chapados. Otros tipos de regiones de cola pudieran utilizarse. Por ejemplo, las colas de soldadura pudieran utilizarse.

La Figura 5 muestra blancos o modelos 400 para el contacto de receptáculo después de que el alojamiento 172 sea moldeado alrededor de éste.

La Figura 6 muestra un blanco 600 de contacto de receptáculo adecuado para utilizarse en una modalidad alternativa de la invención. Los contactos de receptáculo 610A...610H están agrupados en pares: (610A y 610B), (610C y 610D), (610E y 610F) y (610G y 610H). Las regiones de

transmisión 624 de cada par están lo más cercanas posibles entre sí mientras que se conserva la impedancia diferencial. Esto aumenta la separación entre pares adyacentes. Esta configuración mejora la integridad de señal para señales diferenciales.

La región de cola 626 y los receptáculos del blanco 400 y 600 de los contactos de receptáculo son idénticos. Estas son las únicas porciones de los contactos de receptáculo 410 y 610 que se extienden desde el alojamiento 172. Por lo tanto, la porción de señal 168 es externamente la misma ya sea para las señales diferenciales o para las señales de un solo extremo. Esto permite que las plaquitas de señal diferencial y de un solo extremo se mezclen en un solo conector de tarjeta secundaria.

La Figura 7A ilustra un conector de la técnica anterior como auxiliar para explicar el desempeño mejorado de la invención. La Figura 7A muestra una placa de blindaje 710 con una viga en voladizo 712 formada en la misma. La viga en voladiza 712 se acopla con una hoja 714 del cabezal de patilla. El punto de contacto se marca como X. La hoja 714 está conectada a un plano trasero (no mostrado) en el punto 722.

Las señales se transmiten a través de las patillas de señal 716 y 718 que corren adyacentes a la placa de blindaje. La placa 710 y la placa 714 actúan como

la señal de retorno. La ruta de señal 720 a través de estos elementos se muestra como un ciclo. Debe observarse que la ruta de señal 720 se corta a través de la patilla 718. Como es bien sabido, una señal que viaja en un ciclo que pasa a través de un conductor se acoplará inductivamente al conductor. Por lo tanto, el arreglo de la Figura 7A tendrá un acoplamiento o interferencia relativamente alto de las patillas 716 a 718.

La Figura 7B muestra una vista lateral del arreglo de la Figura 7A. Como la viga en voladizo 712 está por arriba de la hoja 714, su distancia desde la patilla 716 es d_1. En contraste, la hoja 714 tiene una separación d_2, que es más grande. En la transmisión de las señales de alta frecuencia, la distancia entre la trayectoria de señal y la tierra dictan la impedancia de la trayectoria o ruta de la señal. Los cambios en distancia significan cambios en impedancia. Los cambios en impedancia ocasionan reflexiones de la señal, lo cual no es deseable.

La Figura 7C muestra el mismo arreglo durante el acoplamiento. La hoja 714 debe deslizarse bajo la viga en voladizo 712. Si no se inserta correctamente, la hoja 714 puede topar contra el extremo de la viga 712 en voladizo. Este fenómeno se llama "anclaje". Este fenómeno es muy poco deseable en un conector ya que puede romper el conector.

En contraste, la Figura 8 muestra en sentido esquemático los componentes de un conector fabricado de acuerdo a la invención. Las placas de blindaje 128 y 150 se traslapan. El contacto se hace en el punto marcado con una X en la viga torsional 146. La ruta de señal 820 se muestra que pasa a través de una patilla de señal 122, regresan a la placa pasante 150 hacia el punto de contacto X, pasa a través del brazo 146, a través de la placa 128 y a través de la cola 130. La trayectoria o ruta de señal 820 se completa entonces a través del plano trasero (no mostrado en la Figura 8). Significativamente, la ruta de señal 820 no se corta a través de ninguna patilla 122 de señal que esté adyacente. En esta forma, la interferencia se reduce significativamente con respecto a la técnica anterior.

La Figura 8B ilustra en forma esquemática a las placas 128 y 150 antes de acoplarse con el conector 116 de tarjeta secundaria al cabezal 114 de patilla. En la perspectiva de la Figura 8B, el brazo 146 se muestra doblado hacia afuera del plano de la placa 128. A medida que las placas 150 y 128 se deslizan una a lo largo de la otra durante el acoplamiento, el brazo 146 se presiona hacia el plano de la placa 128.

La Figura 8C muestra las placas 128 y 150 en la configuración acoplada. La depresión 810 que se hace en el

brazo 146 se muestra al tocar la placa 150. La fuerza de resorte torsional generada al presionar el brazo 146 hacia el plano de la placa 128 asegura un buen contacto eléctrico. Debe observarse que la separación entre las placas 128 ó 150 y un contacto de señal adyacente no tiene una discontinuidad tan grande como la que se muestra en la Figura 7B. Esta mejora reforzará el desempeño eléctrico del conector.

También debe observarse que al moverse de la configuración de la Figura 8B a la de la Figura 8C no hay una superficie abrupta que pudiera originar el anclaje. Por lo tanto, con contactos torsionales, la resistencia mecánica del conector debe mejorarse en comparación con la técnica anterior.

La Figura 10 muestra una modalidad alternativa de una plaquita 154 (Figura 1). En la modalidad de la Figura 10 un blanco de blindaje sobre la tira portadora 1010 está encapsulado en un alojamiento aislante 1070 a través de moldeo por inyección. Las colas del blindaje 1030 se muestran extendiéndose desde el alojamiento 1070. El alojamiento 1070 incluye cavidades 1016, 1017, 1018 y 1019. El blanco de blindaje se corta y se dobla para hacer los contactos 1020 dentro de las cavidades 1016, 1017, 1018 y 1019.

Las cavidades 1016, 1017, 1018 y 1019 tienen

orificios 1022 formados en sus pisos. Las patillas de los cabezales de patilla se insertan a través de los orificios durante el acoplamiento y unión, a través de la propiedad de resorte de la patilla, así como de los contactos 1020 que aseguran la conexión eléctrica al blindaje.

En la modalidad de la Figura 10, los contactos de señal se estampan en forma separada. La sección de línea de transmisión de los contactos se tiende en las cavidades 1026. Las porciones de receptáculo de los contactos de señal se insertan dentro de las cavidades 1024.

Una plaquita como se ilustra en la Figura 10 muestra que pueden utilizarse cualquier número de contactos de señal por columna. En la Figura 10, se muestran cuatro contactos de señal por columna. Esa figura también ilustra que las patillas pudieran utilizarse en lugar de una placa 128. Sin embargo, pudiera haber diferencias en el desempeño eléctrico. Pudiera utilizarse una placa junto con la configuración de la Figura 10. En ese caso, en lugar de una serie de orificios separados 1022 en las cavidades 1016, 1017, 1018 y 1019, se cortaría una ranura a través de las cavidades.

La Figura 11A muestra una modalidad alternativa para los contactos 142 sobre la placa 128. La placa 1128 incluye una serie de contactos torsionales 142. Cada contacto está hecho de un estampado sobre el brazo 1146 a

partir de la placa 1128. Aquí, los brazos tienen una forma generalmente en serpentina. Como se describe antes, es deseable que los brazos 146 sean lo suficientemente largos para proporcionar buena flexibilidad. Sin embargo, también se desea que la corriente fluya a través de los contactos 1142 en un área que es lo más angosta posible en una dirección perpendicular al flujo de corriente a través de las patillas de señal 122. Para lograr estos dos objetivos, los brazos 1146 se estampan en una forma de serpentina.

La Figura 11B muestra a la placa 1128 en sección transversal a través de la línea indicada como B-B en la Figura 1A. Como se muestra, los brazos 1146 se doblan fuera del plano de la placa 1128. Durante este acoplamiento de la mitad del conector, se presionan hacia el plano de la placa 1128, generando así una fuerza torsional.

La Figura 12 muestra una vista adicional del conector 100. La Figura 12 muestra la cara 1210 del conector 116 de tarjeta secundaria. La superficie inferior del cabezal 114 de patilla también es visible. En esta vista, puede observarse que las colas 124 de ajuste a presión de la placa 128 tienen una orientación que está en ángulo recto a la orientación de las colas 130 de ajuste a presión de las patillas de señal 122.

EJEMPLO

Se elaboró y probó un conector de acuerdo a la presente invención. Las pruebas se hicieron con la configuración de un solo extremo y las mediciones se hicieron en una línea de señal activada con las diez líneas más cercanas. Para tiempos de elevación de señal de 500ps, la interferencia en retroceso fue de 4.9%. La interferencia en avance fue de 3.2%. La reflexión fue muy pequeña para poder medirse. El conector proporcionó una densidad de señal real de 101 pulgadas por línea.

Habiendo descrito una modalidad, podrán visualizarse varias modalidades alternativas o variaciones. Por ejemplo, el tamaño de conector pudiera aumentarse o disminuirse en relación a lo mostrado. También, es posible que los materiales diferentes a los expresamente mencionados puedan utilizarse para construir el conector.

Pueden también hacerse varios cambios en las estructuras específicas. Por ejemplo, las pinzas 174 se muestran en general como radialmente simétricas. Pudieran mejorar la efectividad de una placa 150 de blindaje si las pinzas 174 se alargaran con un eje mayor corriendo en sentido paralelo a los contactos de señal en las piezas de señal 168 y un eje menor perpendicular, lo más corto posible.

También, las técnicas de manufactura pudieran

variar. Por ejemplo, se desea que el conector 116 de la tarjeta secundaria se forme organizando una pluralidad de plaquitas sobre un rigidizador. También es posible que una estructura equivalente pueda formarse insertando una pluralidad de piezas de blindaje y receptáculos de señal dentro de un alojamiento moldeado.

Por lo tanto, la invención debe limitarse solamente por el espíritu y alcance de las reivindicaciones anexas.

REIVINDICACIONES:

1. Un conector eléctrico que comprende:

a) un cabezal de patilla que comprende:

i) una base aislante;

ii) una pluralidad de columnas de patillas unidas a la base aislante, cada columna tiene una pluralidad de patillas;

iii) una primera pluralidad de placas unida a la base aislante, cada placa está colocada entre una columna adyacente a las patillas y cada placa tiene formada dentro de la misma una pluralidad de contactos torsionales;

b) un conector de tarjeta secundaria que comprende:

i) una base aislante conformada para acoplarse con la base aislante del cabezal de patilla;

ii) una pluralidad de columnas de receptáculos, cada columna tiene una pluralidad de receptáculos dispuestos para acoplar una patilla de la pluralidad de patillas;

iii) una segunda pluralidad de placas, cada placa está dispuesta entre una columna adyacente de receptáculos y está colocada para acoplar a la pluralidad de contactos torsionales de una placa de la pluralidad de placas en el cabezal de patilla.

2. El conector eléctrico según la

reivindicación 1, en donde:

a) cada una de la pluralidad de columnas de patillas incluye un primer número de patillas; y

b) cada una de la primera pluralidad de placas en el cabezal de patilla tiene un segundo número de colas de contacto que se extienden desde la misma, el segundo número es igual o mayor al primer número, menos uno.

3. El conector eléctrico según la reivindicación 1, en donde cada uno de los contactos torsionales comprende por lo menos un brazo estampado a partir de una placa de la primera pluralidad de placas, y el brazo está conectado a la placa en dos puntos y se dobla fuera del plano de la placa.

4. El conector eléctrico según la reivindicación 1, en donde cada uno de los contactos torsionales comprende un brazo estampado fuera de una placa de la primera pluralidad de placas, el brazo tiene un espesor que es menor al espesor de la placa.

5. El conector eléctrico según la reivindicación 1, en donde los receptáculos adyacentes dentro de la misma columna están separados por una cantidad menor o igual a 2 mm y las columnas adyacentes de receptáculos están separadas en una cantidad menor o igual a 2.25 mm.

6. El conector eléctrico según la

reivindicación 1, en donde cada uno de los contactos torsionales contiene un brazo y el brazo tiene una forma de serpentina.

7. El conector eléctrico según la reivindicación 1, en donde el conector de tarjeta secundaria comprende una pluralidad de módulos, el conector comprende adicionalmente un rigidizador metálico al cual cada una de la pluralidad de módulos está unido.

8. Un conector eléctrico incorporado dentro de una unidad de plano trasero con un plano trasero y por lo menos una tarjeta secundaria, el conector eléctrico comprende:

a) una primera pieza conectora que tiene:

i) una pluralidad de contactos de señal en forma de patilla, cada contacto de señal tiene una porción de cola unida al plano trasero, los contactos de señal en forma de patilla están colocados en una pluralidad de columnas paralelas;

ii) una primera pluralidad de placas de blindaje, cada placa de blindaje está colocada entre columnas adyacentes de los contactos de señal y cada una tiene una pluralidad de porciones de cola que se extienden desde la misma y están unidas al plano trasero, cada porción de cola de cada placa de blindaje está colocada entre las porciones de cola de los contactos de señal

adyacentes dentro de la misma columna de contactos de señal, en donde para cada placa de blindaje, hay una porción de cola entre cada par de contactos de señal adyacentes en una columna adyacente de los contactos de señal;

b) una segunda pieza conectora que tiene:

i) una pluralidad de contactos de señal de receptáculo, la pluralidad de contactos de señal de receptáculo está colocada en una pluralidad de columnas paralelas, donde cada receptáculo está colocado para acoplar un contacto de señal en forma de patilla;

ii) una segunda pluralidad de placas de blindaje, cada placa de blindaje está colocada entre columnas adyacentes de contactos de señal de receptáculo, en donde cada placa de blindaje de la segunda pluralidad de placas de blindaje se acopla mecánicamente con una placa de blindaje de la primera pluralidad de placas de blindaje, con los brazos de contacto unidos a una de las placas de blindaje de la primera o segunda pluralidad de placas de blindaje, en dos puntos.

9. El conector eléctrico según la reivindicación 8, en donde cada columna de contactos de señal tiene por lo menos seis contactos de señal.

10. El conector eléctrico según la reivindicación 8, que comprende adicionalmente un medio

para proporcionar una trayectoria de corriente de retorno para que cualquier contacto de señal en forma de patilla, específico, no cruce a ningún otro contacto de señal en forma de patilla, en donde el medio incluye la primera pluralidad de placas de blindaje y la segunda pluralidad de placas de blindaje.

11. El conector eléctrico según la reivindicación 8, en donde las porciones de cola de los contactos de señal y las porciones de cola de las placas son colas de ajuste a presión y las porciones de cola de los contactos de señal están en ángulo recto respecto a las porciones de cola de las placas.

12. El conector eléctrico según la reivindicación 8, en donde una porción de la primera pluralidad de placas tiene una ranura cortada en la misma y la placa tiene un doblez a lo largo de una línea perpendicular a la ranura, la porción de la placa en un lado del doblez forma una región de cola y la porción de la placa en el otro lado del doblez forma una región de blindaje, la región de cola y la región de blindaje son paralelas y las porciones de cola están conectadas a la región de cola de la placa.

13. El conector eléctrico según la reivindicación 8, en donde las porciones de cola de la primera pluralidad de placas están puestas a tierra en el

plano trasero.

14. Un conector eléctrico del tipo que tiene dos piezas interacoplables, cada pieza tiene una pluralidad de contactos de señal colocados en columnas para definir un campo de contactos de señal, el conector comprende adicionalmente una pluralidad de medios, colocados entre columnas adyacentes de contactos de señal, para proporcionar una trayectoria de corriente de retorno para cada uno de los contactos de señal dentro de una columna de contactos de señal, las trayectorias de corriente de retorno quedan dentro del campo de los contactos de señal, en donde cada medio para proporcionar una trayectoria de corriente de retorno comprende un par de placas paralelas que se acoplan eléctricamente una a otra, en una pluralidad de puntos, las placas tienen una pluralidad de colas de contacto que se extienden desde las mismas, las colas de contacto se colocan en forma intermedia a los contactos de señal adyacentes.

15. El conector según la reivindicación 14, en donde el número de colas de contacto en cada una de las placas es mayor o igual al número de contactos de señal en cada una de las columnas, menos uno.

16. El conector según la reivindicación 15, en donde una de las placas en cada par de placas paralelas tiene estampada en la misma una pluralidad de brazos que

tienen por lo menos dos extremos y que están unidos a la placa en los dos extremos.

17. El conector según la reivindicación 16, en donde cada uno de los brazos está acuñado para tener un espesor ... que el espesor de la placa.

18. El conector según la reivindicación 17, en donde cada uno de los brazos tiene una forma de serpentina.

19. El conector según la reivindicación 14, en donde los contactos de señal están separados para proporcionar una densidad de señal real de por lo menos 100 por pulgada lineal y una interferencia en retroceso menor a 5% a un tiempo de elevación de 500 pseg.

20. El conector según la reivindicación 19, en donde el número de contactos de señal en cada columna es de ocho.

RESUMEN DE LA INVENCIÓN

Un conector eléctrico de alta densidad y alta velocidad que se utiliza con tableros de circuito impreso. El conector es de dos piezas, una de las piezas tiene patillas y placas de blindaje y la otra pieza tiene contactos de señal de tipo receptáculo y placas de blindaje. Los blindajes tienen un arreglo de tierra que está adaptado para controlar los campos electromagnéticos, para varios sistemas de arquitecturas, configuraciones de conmutación simultáneas y velocidades de señal, permitiendo que todos los contactos de señal tipo receptáculo se utilicen para transmisión de señal. Adicionalmente, por lo menos una pieza del conector está fabricada a partir de plaquitas, con cada plano de tierra y columna de señal moldeado por inyección en los componentes que, cuando se combinan, forman una plaquita. Esta construcción permite una separación muy estrecha entre columnas adyacentes de contactos de señal así como el control rígido de la separación entre los contactos de señal y los blindajes. También permite la manufactura fácil y flexible, de manera que un conector que tiene plaquitas intermezcladas en una configuración para acomodar aplicaciones de un solo extremo, punto a punto y de tipo diferencial.

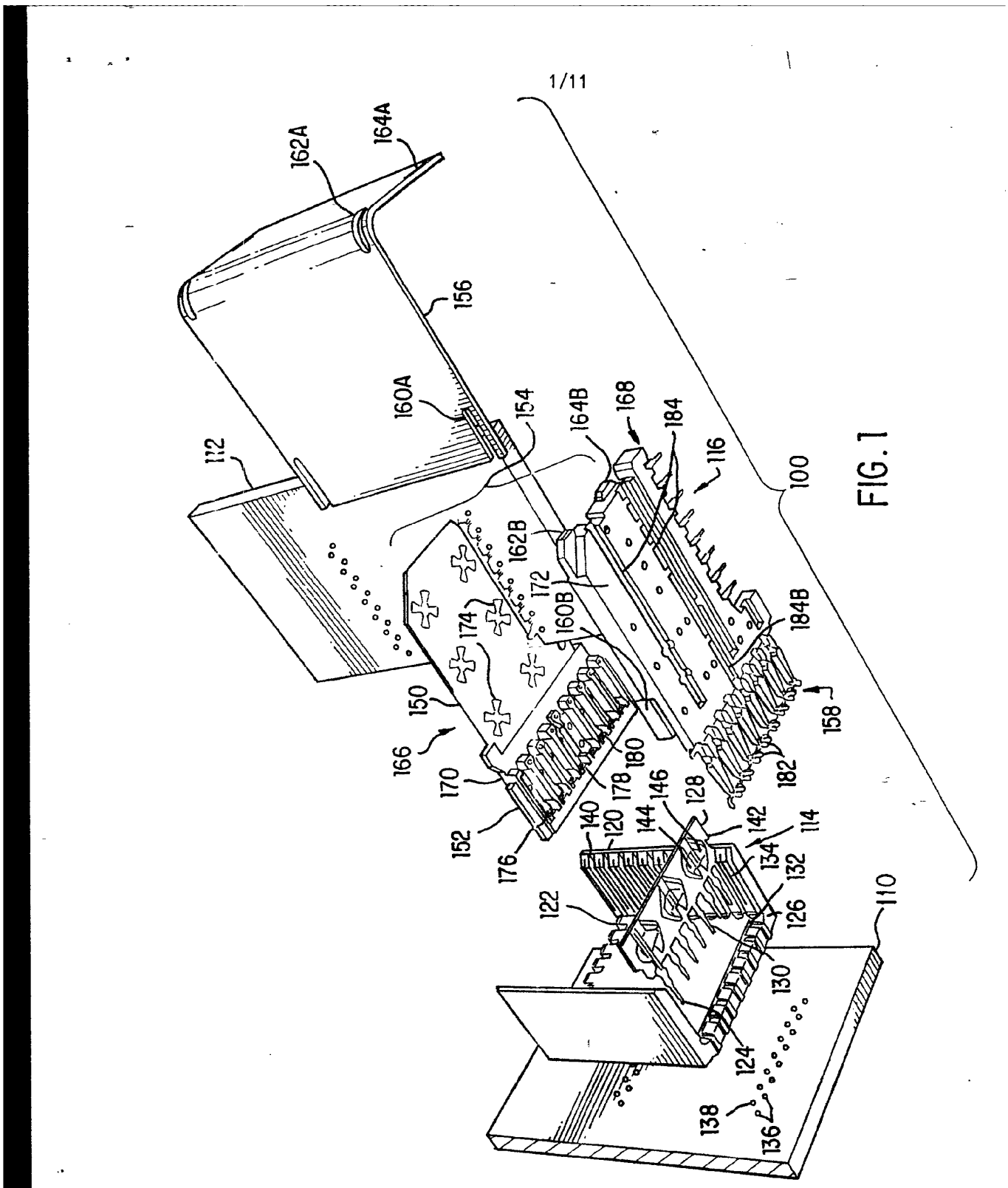
1/11
162A
164A
156
160A
154
164B
168
184
116
100
112
162B
172
160B
174
184B
158
150
166
180
170
178
182
146
128
152
140
120
144
142
114
176
134
132
122
126
110
130
124
138
136

FIG. 1

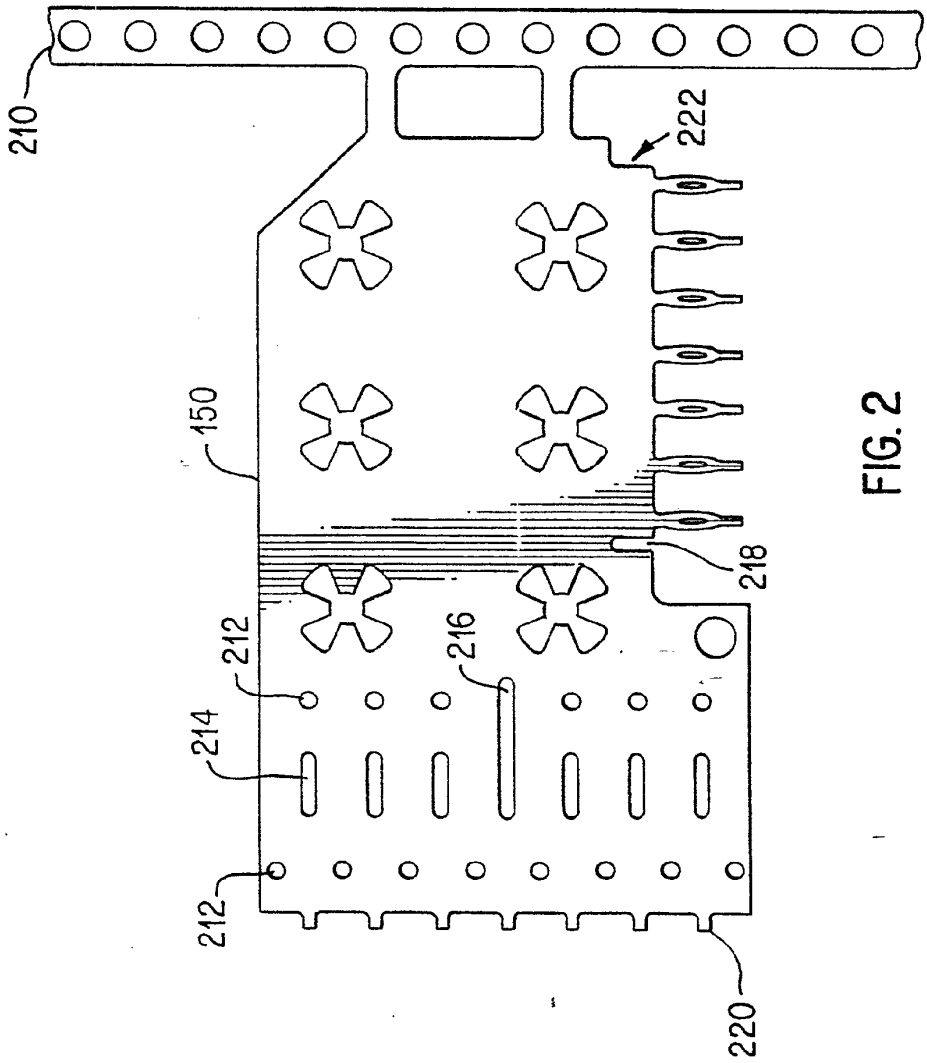

FIG. 2

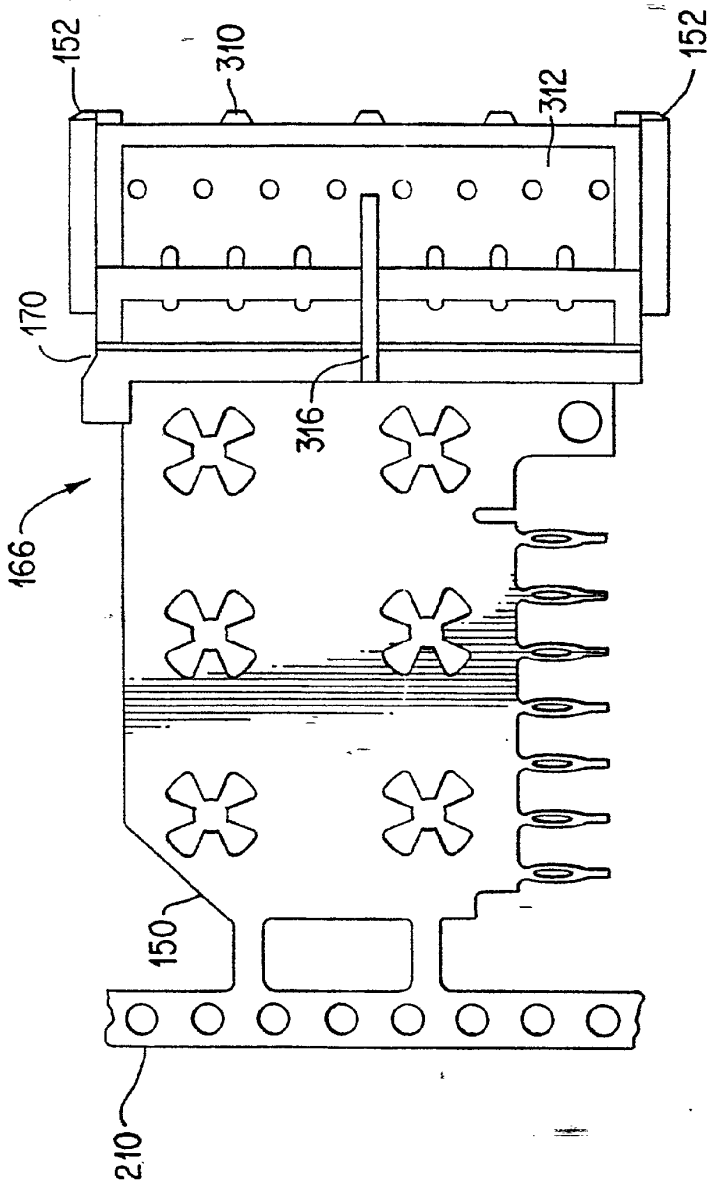

FIG. 3

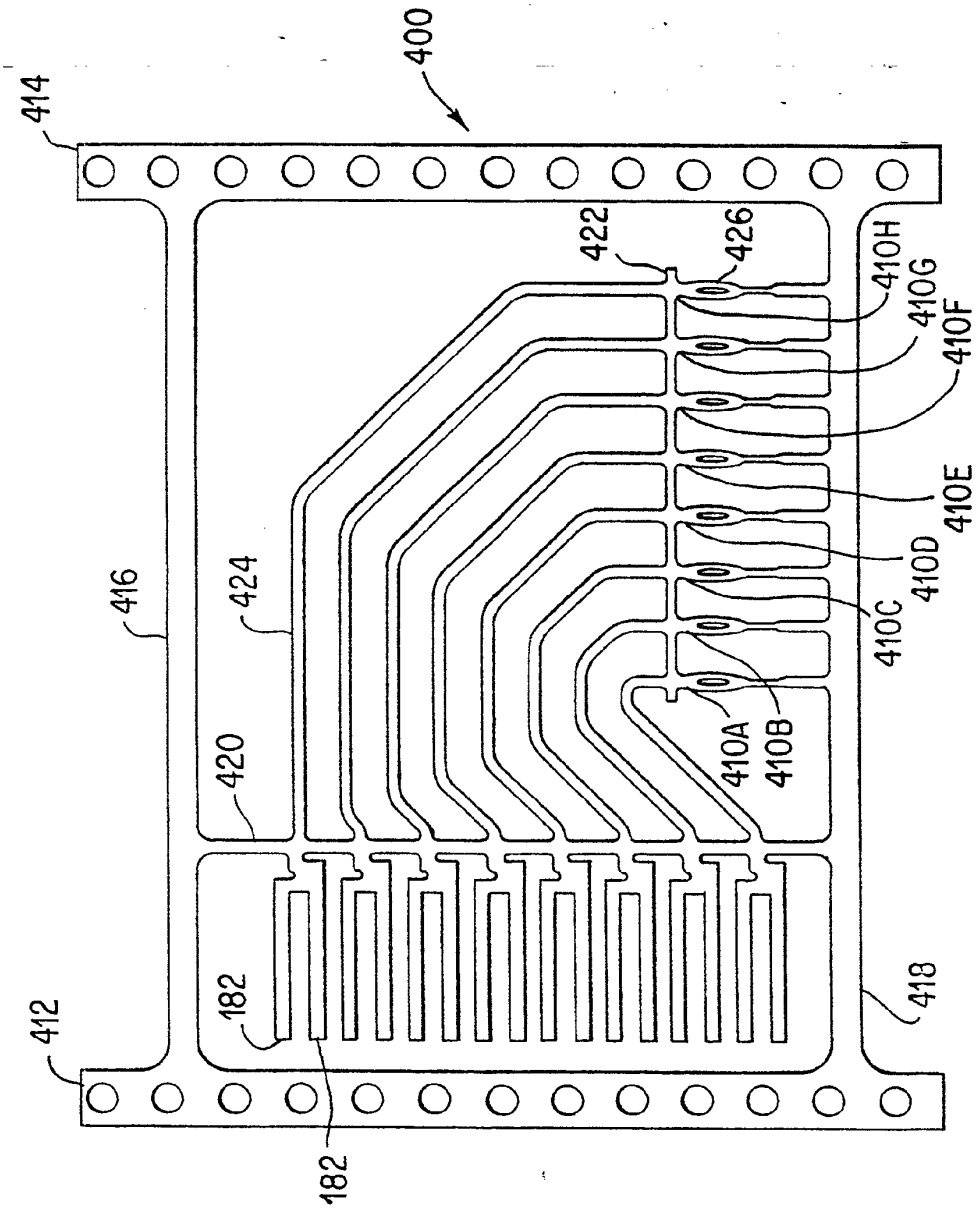
400
414
422
426
410H
410G
410F
410E
410D
410C
410A
410B
416
424
420
182
412
418
182

FIG. 4

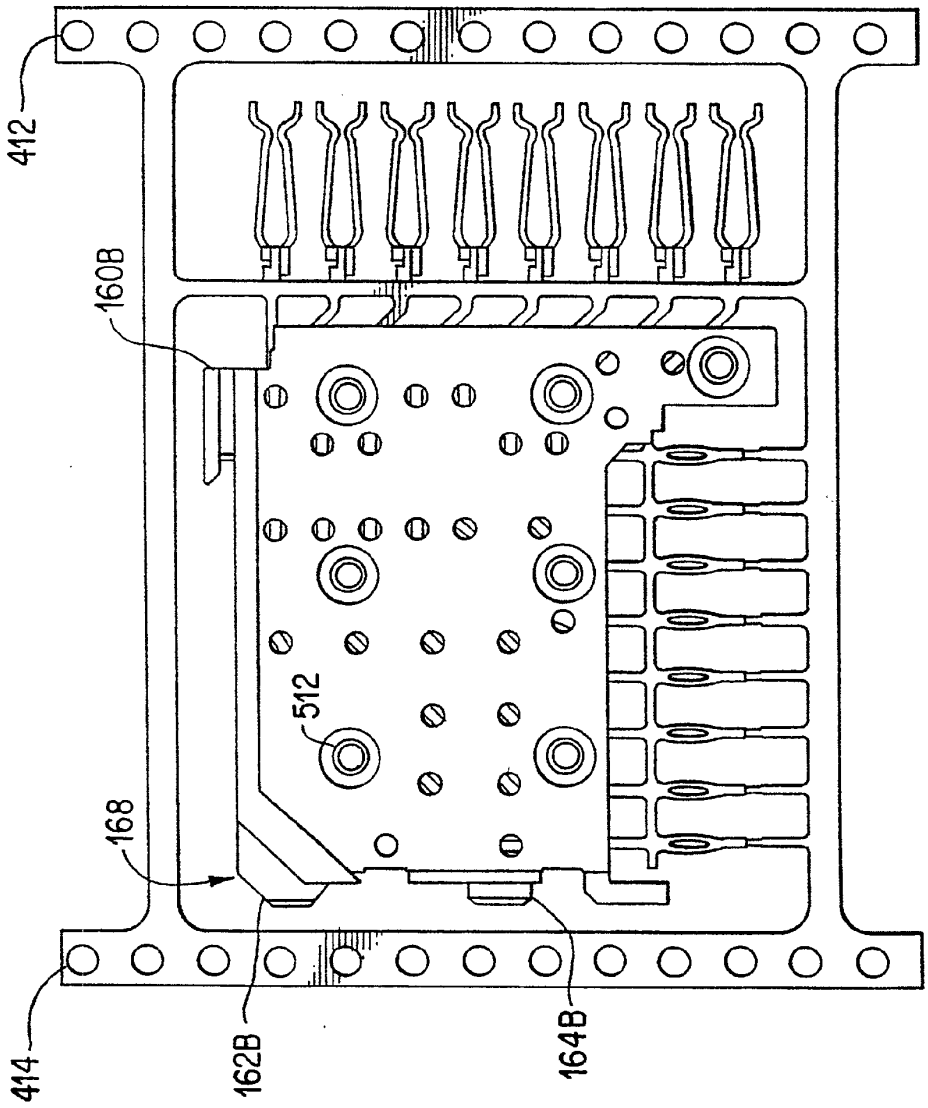

FIG.5

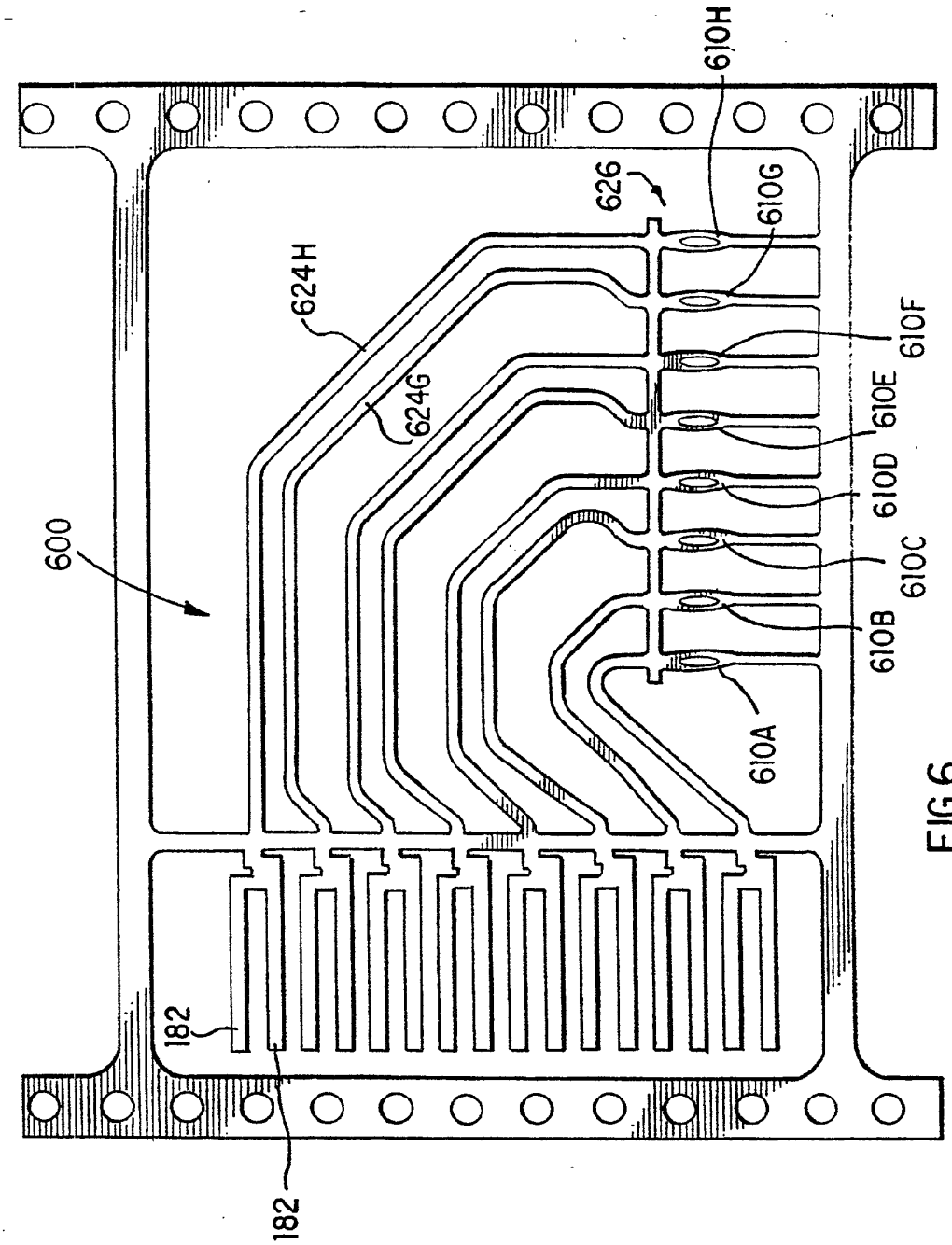
610H
626
610G
624H
610F
624G
610E
610D
600
610C
610B
610A
182
182

FIG.6

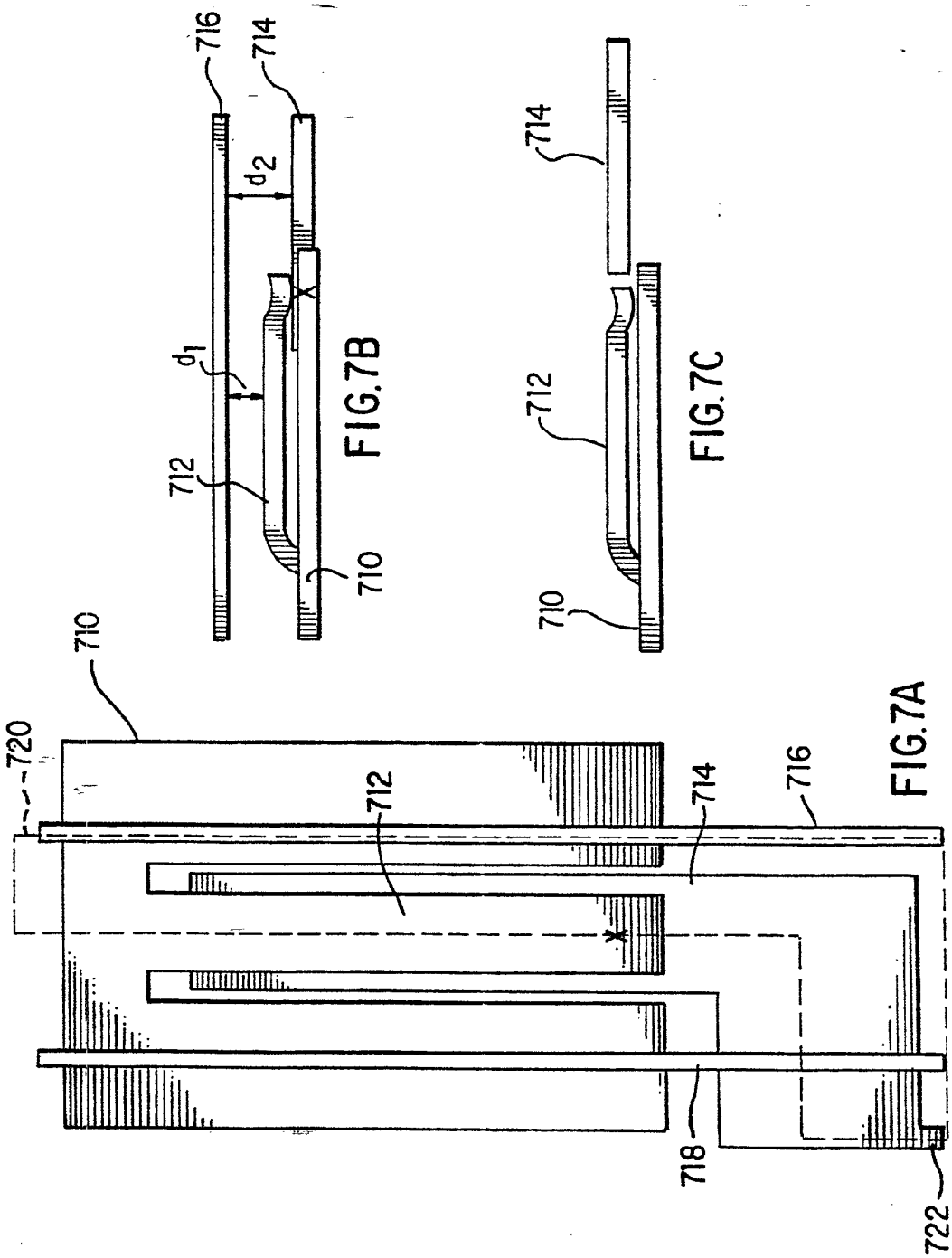

FIG.7B

FIG.7C

FIG.7A

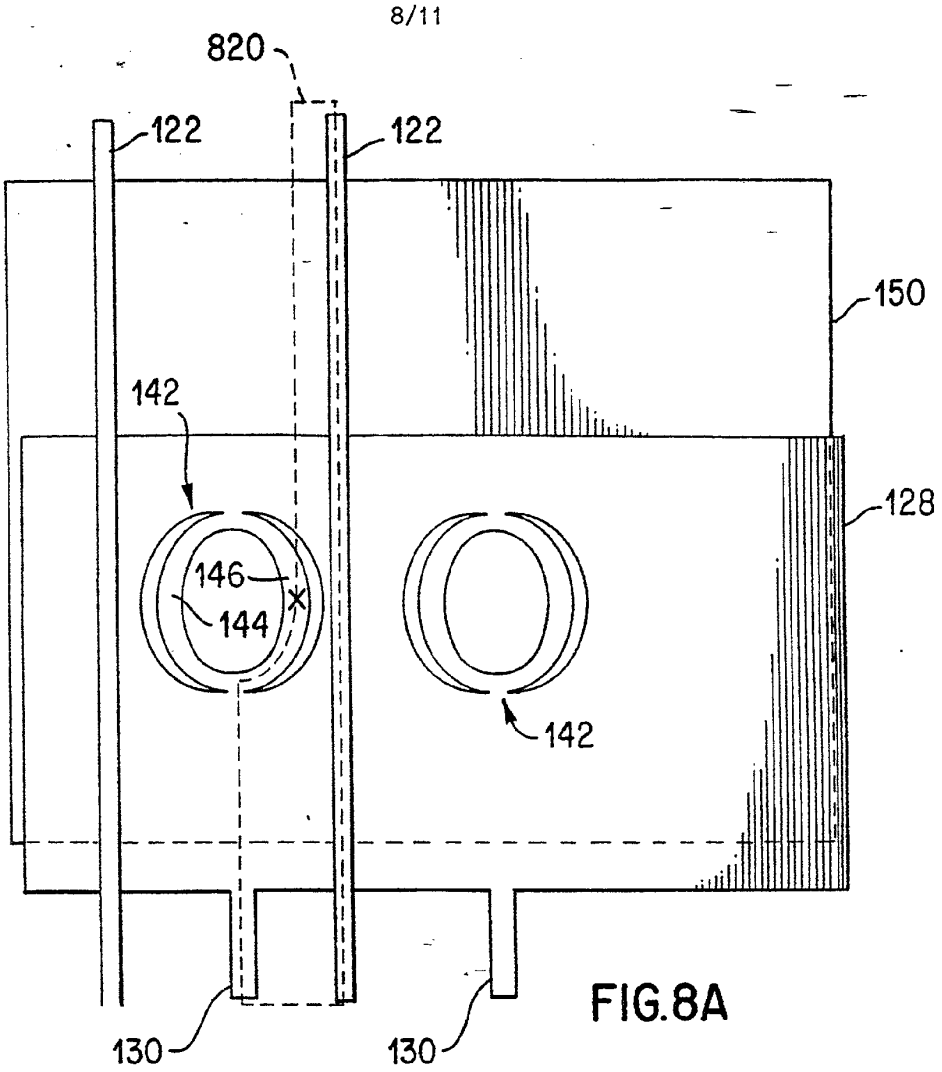

FIG.8A

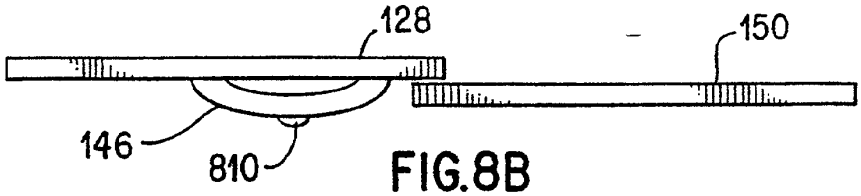

FIG.8B

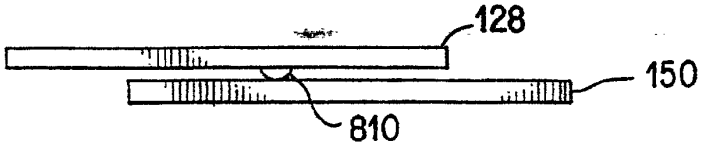

FIG.8C

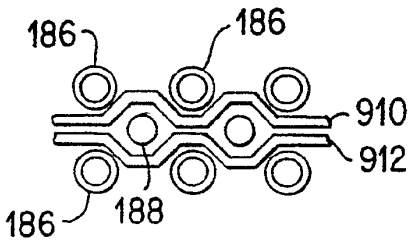

FIG. 9A

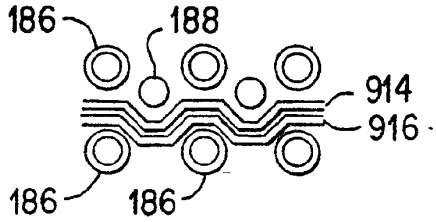

FIG. 9B

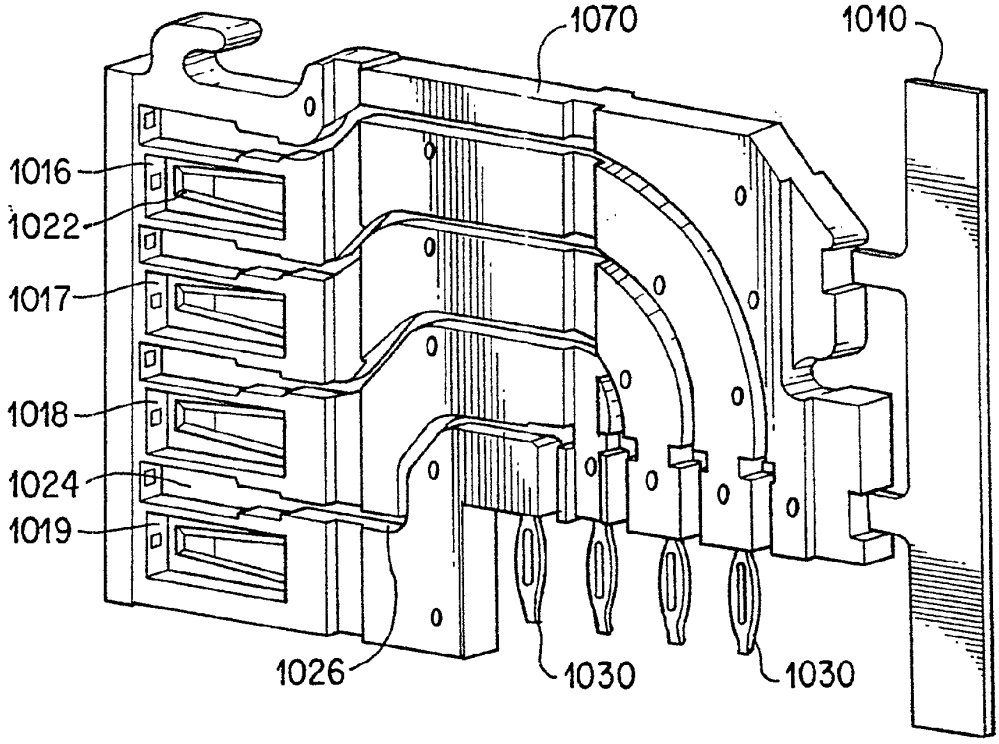

FIG. 10

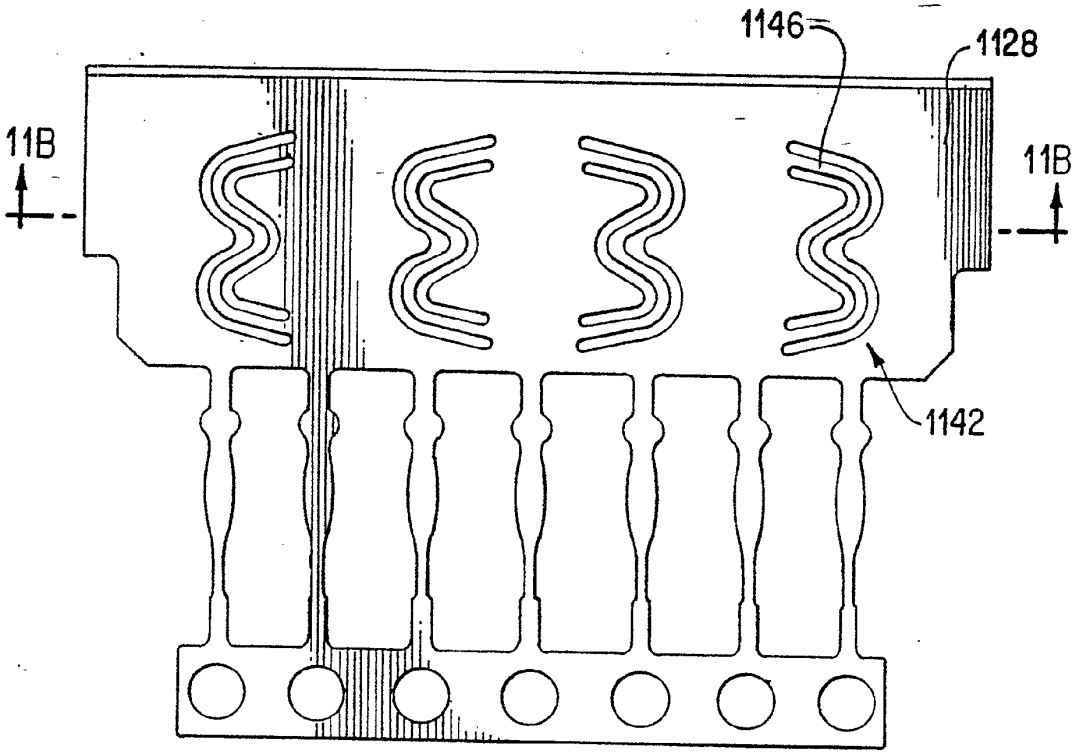

FIG.11A

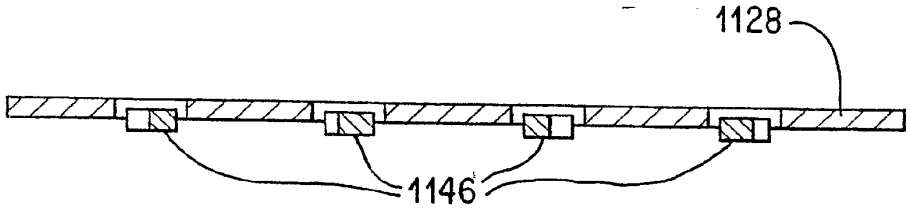

FIG.11B

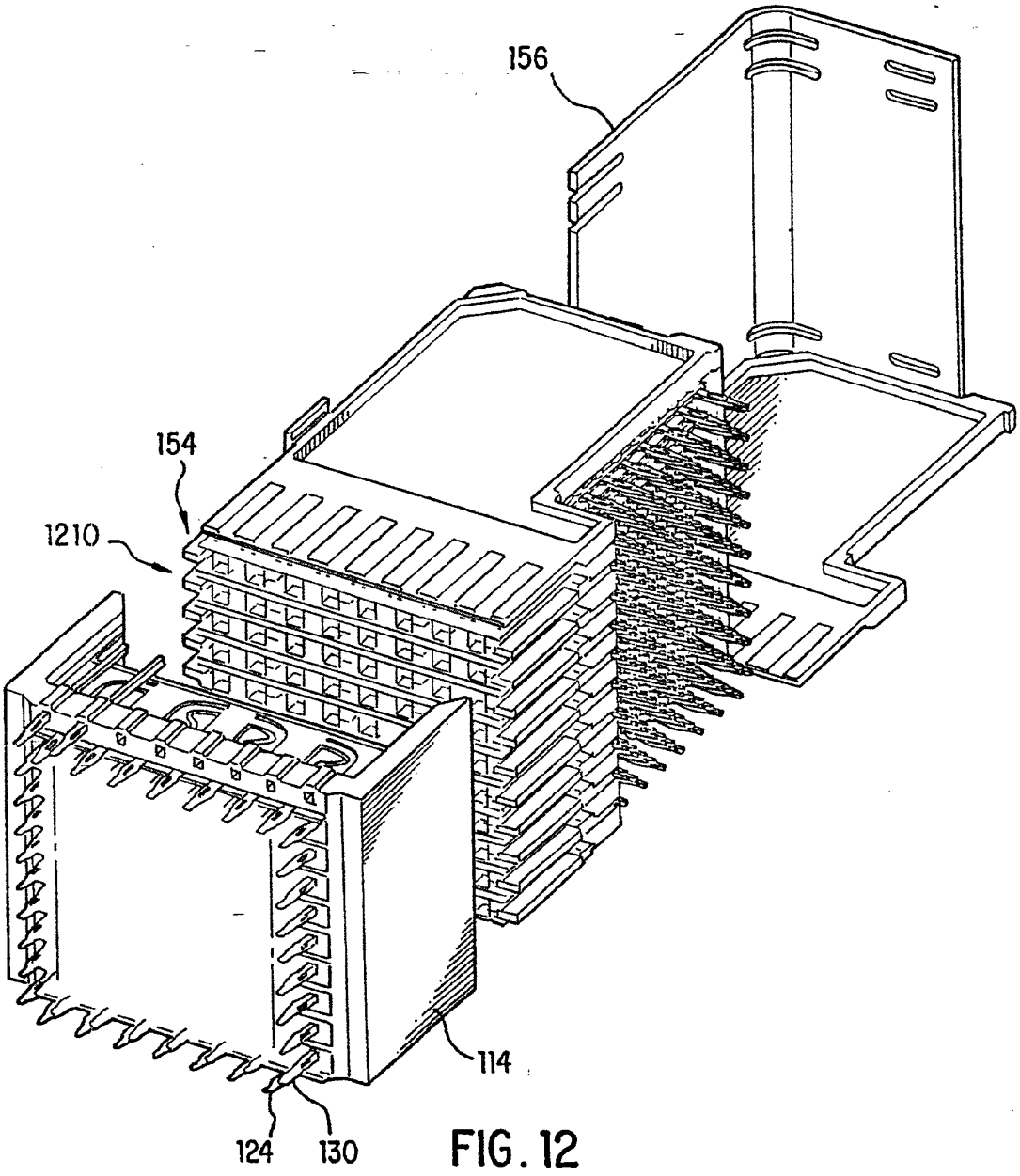

FIG. 12

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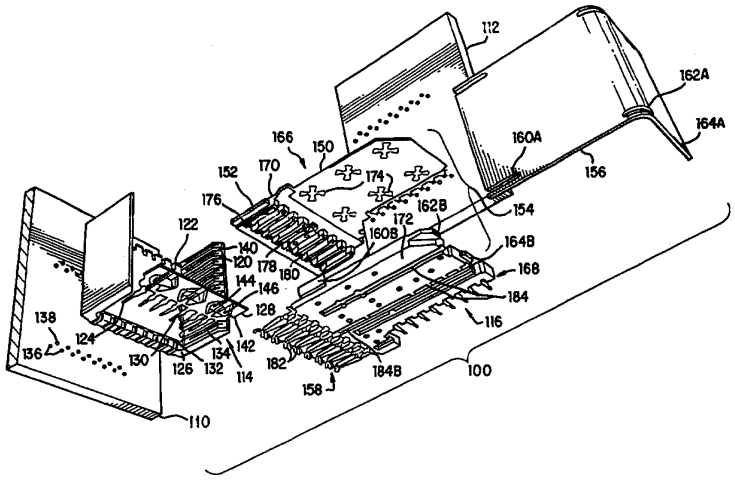

(57) Abstract

A high speed, high density electrical connector for use with printed circuit boards. The connector is in two pieces with one piece having pins and shield plates and the other having socket type signal contacts and shield plates. The shields have a grounding arrangement which is adapted to control the electromagnetic fields, for various system architectures, simultaneous switching configurations and signal speeds, allowing all of the socket type signal contacts to be used for signal transmission. Additionally, at least one piece of the connector is manufactured from wafers, with each ground plane and signal column injection molded into components which, when combined, form a wafer. This construction allows very close spacing between adjacent columns of signal contacts as well as tightly controlled spacing between the signal contacts and the shields. It also allows for easy and flexible manufacture, such as a connector that has wafers intermixed in a configuration to accommodate single ended, point to point and differential applications.

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HIGH SPEED, HIGH DENSITY ELECTRICAL CONNECTOR

This invention relates generally to electrical connectors used to interconnect printed circuit boards and more specifically to such connectors designed to carry many high speed signals.

Electrical connectors are used in many electronic systems. It is generally easier and more cost effective to manufacture a system on several printed circuit boards which are then joined together with electrical connectors. A traditional arrangement for joining several printed circuit boards is to have one printed circuit board serve as a backplane. Other printed circuit boards, called daughter boards, are connected through the backplane.

A traditional backplane is a printed circuit board with many connectors. Conducting traces in the printed circuit board connect to signal pins in the connectors so that signals may be routed between the connectors. Other printed circuit boards, called "daughter boards" also contain connectors that are plugged into the connectors on the backplane. In this way, signals are routed among the daughter boards through the backplane. The daughter cards often plug into the backplane at a right angle. The connectors used for these applications contain a right angle bend and are often called "right angle connectors."

Connectors are also used in other configurations for interconnecting printed circuit boards, and even for connecting cables to printed circuit boards. Sometimes, one or more small printed circuit boards are connected to another larger printed circuit board. The larger printed circuit board is called a "mother board" and the printed circuit boards plugged into it are called daughter boards. Also, boards of the same size are sometimes aligned in parallel. Connectors used in these

applications are sometimes called "stacking connectors" or "mezzanine connectors."

Regardless of the exact application, electrical connector designs have generally needed to mirror trends in the electronics industry. Electronic systems generally have gotten smaller and faster. They also handle much more data than systems built just a few years ago. These trends mean that electrical connectors must carry more and faster data signals in a smaller space without degrading the signal.

Connectors can be made to carry more signals in less space by placing the signal contacts in the connector closer together. Such connectors are called "high density connectors." The difficulty with placing signal contacts closer together is that there is electromagnetic coupling between the signal contacts. As the signal contacts are placed closer together, the electromagnetic coupling increases. Electromagnetic coupling also increases as the speed of the signals increase.

In a conductor, the amount of electromagnetic coupling is indicated by measuring the "cross talk" of the connector. Cross talk is generally measured by placing a signal on one or more signal contacts and measuring the amount of signal coupled to another signal contact. The choice of which signal contacts are used for the cross talk measurement as well as the connections to the other signal contacts will influence the numerical value of the cross talk measurement. However, any reliable measure of cross talk should show that the cross talk increases as the speed of the signals increases and also as the signal contacts are placed closer together.

A traditional method of reducing cross talk is to ground signal pins within the field of signal pins. The disadvantage of this approach is that it reduces the effective signal density of the density of the connector.

To make both a high speed and high density connector, connector designers have inserted shield members between signal contacts. The shields reduce the electromagnetic coupling between signal contacts, thus countering the effect of closer spacing or higher frequency signals. Shielding, if appropriately configured, can also control the impedance of the signal paths through the connector, which can also improve the integrity of signals carried by the connector.

An early use of shielding is shown in Japanese patent disclosure 49-6543 by Fujitsu, Ltd. dated February 15, 1974. US patents 4,632,476 and 4,806,107 - both assigned to AT&T Bell Laboratories - show connector designs in which shields are used between columns of signal contacts. These patents describe connectors in which the shields run parallel to the signal contacts through both the daughter board and the backplane connectors. Cantilevered beams are used to make electrical contact between the shield and the backplane connectors. Patents 5,433,617; 5,429,521; 5,429,520 and 5,433,618 - all assigned to Framatome Connectors International - show a similar arrangement. The electrical connection between the backplane and shield is, however, made with a spring type contact.

Other connectors have the shield plate within only the daughter card connector. Examples of such connector designs can be found in patents 4,846,727; 4,975,084; 5,496,183; 5,066,236 - all assigned to AMP, Inc. An other connector with shields only within the daughter board connector is shown in US patent 5,484,310, assigned to Teradyne, Inc.

From the number of patents that describe connectors using shielding to reduce cross talk, it will be appreciated that the placement and connection of the shields can have a great effect on the electrical performance of the connector. The specific configuration

of the shielding can also have a significant impact on the mechanical properties of the connector. For example, the manner in which the electrical connection is made to the shield can influence whether there is "stubbing" when the connectors are mated. Stubbing means that one contact gets caught on another contact. When there is stubbing, one of the contacts is usually damaged, requiring that the connector be repaired or replaced.

It would be highly desirable to have a shield arrangement that is highly effective at reducing the cross talk between signal contacts. It would be also highly desirable if the shielding arrangement were mechanically robust. It would also be desirable if that connector were easy to manufacture. It would further be highly desirable to control signal reflections by controlling the geometry of the shields and signal contacts for impedance matching the connection.

SUMMARY OF THE INVENTION

With the foregoing background in mind, it is an object of the invention to provide a high speed, high density connector.

It is a further object to provide a high performance connector that allows all of its signal contacts to be used for carrying signals.

It is also an object to provide an electrical connector that is mechanically robust.

It is a further object to provide a connector that is easy to manufacture.

The foregoing and other objects are achieved in an electrical connector having shield plates between rows of signal contacts in both the daughter board and backplane connectors. The shield plates in the backplane connector have torsional contacts. The torsional contacts significantly reduce the chance of stubbing. They also provide a highly desirable pattern of current flow through the shields, which increases their effectiveness at reducing inductive coupling between signal contacts and the resulting cross talk.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be better understood by reference to the following more detailed description and accompanying drawings in which

FIG. 1 is an exploded view of a connector made in accordance with the invention;

FIG. 2 is a shield plate blank used in the connector of FIG. 1;

FIG. 3 is a view of the shield plate blank of FIG. 2 after it is insert molded into a housing element;

FIG. 4 is a signal contact blank used in the connector of FIG. 1;

FIG. 5 is a view of the signal contact blank of FIG. 4 after it is insert molded into a housing element;

FIG. 6 is an alternative embodiment of the signal contact blank of FIG. 4 suitable for use in making a differential module;

FIGs. 7A-7C are operational views a prior art connector;

FIGs. 8A-8C are similar operational views of the connector of FIG. 1;

FIG. 9A and 9B are backplane hole and signal trace patterns for single ended and differential embodiments of the invention, respectively; and

FIG. 10 is a view of an alternative embodiment of the invention.

FIG. 11A is a an alternative embodiment for the plate 128 in FIG. 1;

FIG. 11B is a cross sectional view taken through the line B-B of FIG. 11A;

FIG. 12 is an isometric view of a connector according to the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

FIG. 1 shows an exploded view of backplane assembly 100. Backplane 110 has pin header 114 attached to it. Daughter card 112 has daughter card connector 116 attached to it. Daughter card connector 116 can be mated to pin header 114 to form a connector. Backplane assembly likely has many other pin headers attached to it so that multiple daughter cards can be connected to it. Additionally, multiple pin headers might be aligned end to end so that multiple pin headers are used to connect to one daughter card. However, for clarity, only a portion of backplane assembly and a single daughter card 112 are shown.

Pin header 114 is formed from shroud 120. Shroud 120 is preferably injection molded from a plastic, polyester or other suitable insulative material. Shroud 120 serves as the base for pin header 114.

The floor (not numbered) of shroud 120 contains columns of holes 126. Pins 122 are inserted into holes 126 with their tails 124 extending through the lower surface of shroud 120. Tails 124 are pressed into signal holes 136. Holes 136 are plated through-holes in backplane 110 and serve to electrically connect pins 122 to traces (not shown) on backplane 110. For clarity of illustration, only a single pin 122 is shown. However, pin header 114 contains many parallel columns of pins. In a preferred embodiment, there are eight rows of pins in each column.

The spacing between each column of pins is not critical. However, it is one object of the invention to allow the pins to be placed close together so that a high density connector can be formed. By way of example, the pins within each column can be spaced apart by 2.25 mm and the columns of pins can be spaced apart by 2mm. Pins 122 could be stamped from 0.4 mm thick copper alloy.

Shroud 120 contains a groove 132 formed in its floor that runs parallel to the column of holes 126. Shroud 120 also has grooves 134 formed in its sidewalls. Shield plate 128 fits into grooves 132 and 134. Tails 130 protrude through holes (not visible) in the bottom of groove 132. Tails 130 engage ground holes 138 in backplane 110. Ground holes 138 are plated through-holes that connect to ground traces on backplane 110.

In the illustrated embodiment, plate 128 has seven tails 130. Each tail 130 falls between two adjacent pins 122. It would be desirable for shield 128 to have a tail 130 as close as possible to each pin 122. However, centering the tails 130 between adjacent signal pins 122 allows the spacing between shield 128 and a column of signal pins 122 to be reduced.

Shield plate 128 has several torsional beams contacts 142 formed therein. Each contact 142 is formed by stamping arms 144 and 146 in plate 128. Arms 144 and 146 are then bent out of the plane plate 128. Arms 144 and 146 are long enough that they will flex when pressed back into the plane of plate 128. Arms 144 and 148 are sufficiently resilient to provide a spring force when pressed back into the plane of plate 128. The spring force generated by arms 144 and 146 creates a point of contact between each arm 144 or 146 and plate 150. The generated spring force must be sufficient to ensure this contact even after the daughter card connector 116 has been repeatedly mated and unmated from pin header 114.

During manufacture, arms 144 and 146 are coined. Coining reduces the thickness of the material and increases the compliancy of the beams without weakening of plate 128.

For enhanced electrical performance, it is desirable that arms 144 and 146 be as short and straight as possible. Therefore, they are made only as long as needed to provide the required spring force. In

addition, for electrical performance, it is desirable that there be one arm 144 or 146 as close as possible to each signal pin 122. Ideally, there would be one arm 144 and 146 for each signal pin 122. For the illustrated embodiment with eight signal pins 122 per column, there would ideally be eight arms 144 or 146, making a total of four balanced torsional beam contacts 142. However, only three balanced torsional beam contacts 142 are shown. This configuration represents a compromise between the required spring force and desired electrical properties.

Grooves 140 on shroud 120 are for aligning daughter card connector 116 with pin header 114. Tabs 152 fit into grooves 140 for alignment and to prevent side to side motion of daughter card connector 116 relative to pin header 114.

Daughter card connector 116 is made of wafers 154. Only one wafer 154 is shown for clarity, but daughter card connector 116 has, in a preferred embodiment, several wafers stacked side to side. Each wafer 154 contains one column of receptacles 158. Each receptacle 158 engages one pin 122 when the pin header 114 and daughter card connector 116 are mated. Thus, daughter card connector 116 is made from as many wafers as there are columns of pins in pin header 114.

Wafers 154 are supported in stiffener 156. Stiffener 156 is preferably stamped and formed from a metal strip. It is stamped with features to hold wafer 154 in a required position without rotation and therefore preferably includes three attachment points. Stiffener 156 has slot 160A formed along its front edge. Tab 160B fits into slot 160A. Stiffener 156 also includes holes 162A and 164A. Hubs 162B and 164B fit into holes 162A and 164A. The hubs 162B and 164B are sized to provide an interference fit in holes 162A and 164A.

FIG. 1 shows only a few of the slots 160A and holes 162A and 164A for clarity. The pattern of slots

and holes is repeated along the length of stiffener 156 at each point where a wafer 156 is to be attached.

In the illustrated embodiment, wafer 154 is made in two pieces, shield piece 166 and signal piece 168. Shield piece 166 is formed by insert molding housing 170 around the front portion of shield 150. Signal piece 168 is made by insert molding housing 172 around contacts 410A...410H (FIG. 4).

Signal piece 168 and shield piece 166 have features which hold the two pieces together. Signal piece 168 has hubs 512 (FIG. 5) formed on one surface. The hubs align with and are inserted into clips 174 cut into shield 150. Clips 174 engage hubs 512 and hold plate 150 firmly against signal piece 168.

Housing 170 has cavities 176 formed in it. Each cavity 176 is shaped to receive one of the receptacles 158. Each cavity 176 has platform 178 at its bottom. Platform 178 has a hole 180 formed through it. Hole 180 receives a pin 122 when daughter card connector 116 mates with pin header 114. Thus, pins 122 mate with receptacles 158, providing a signal path through the connector.

Receptacles 158 are formed with two legs 182. Legs 182 fit on opposite sides of platform 178 when receptacles 158 are inserted into cavities 176. Receptacles 158 are formed such that the spacing between legs 182 is smaller than the width of platform 178. To insert receptacles 158 into cavity 176, it is therefore necessary to use a tool to spread legs 182.

The receptacles form what is known as a preloaded contact. Preloaded contacts have traditionally been formed by pressing the receptacle against a pyramid shaped platform. The apex of the platform spreads the legs as the receptacle is pushed down on it. Such a contact has a lower insertion force and is less likely to stub on the pin when the two connectors are mated. The

receptacles of the invention provide the same advantages, but are achieved by inserting the receptacles from the side rather than by pressing them against a pyramid.

Housing 172 has grooves 184 formed in it. As described above, hubs 512 (FIG. 5) project through plate 150. When two wafers are stacked side by side, hubs 512 from one wafer 154 will project into grooves 184 of an adjacent wafer. Hubs 512 and grooves 184 help hold adjacent wafers together and prevent rotation of one wafer with respect to the next. These features, in conjunction with stiffener 156 obviate the need for a separate box or housing to hold the wafers, thereby simplifying the connector.

Housings 170 and 172 are shown with numerous holes (not numbered) in them. These holes are not critical to the invention. They are "pinch holes" used to hold plates 150 or receptacle contacts 410 during injection molding. It is desirable to hold these pieces during injection molding to maintain uniform spacing between the plates and receptacle contacts in the finished product.

FIG. 2 shows in greater detail the blank used to make plate 150. In a preferred embodiment, plates 150 are stamped from a roll of metal. The plates are retained on carrier strip 210 for ease of handling. After plate 150 is injection molded into a shield piece 166, the carrier strip can be cut off.

Plates 150 include holes 212. Holes 212 are filled with plastic from housing 170, thereby locking plate 150 in housing 170.

Plates 150 also include slots 214. Slots 214 are positioned to fall between receptacles 158. Slots 214 serve to control the capacitance of plate 150, which can overall raise or lower the impedance of the connector. They also channel current flow in the plate near receptacles 158, which are the signal paths. Higher

return current flow near the signal paths reduces cross talk.

Slot 216 is similar to the slots 214, but is larger to allow a finger 316 (FIG. 3) to pass through plate 150 when plate 150 is molded into a housing 170. Finger 316 is a small finger of insulating material that could aid in holding a plate 128 against plate 150. Finger 316 is optional and could be omitted. Note in FIG. 1 that the central two cavities 176 have their intermediate wall partially removed. Finger 316 from an adjacent wafer 154 (not shown) would fit into this space to complete the wall between the two central cavities. Finger 316 would extend beyond housing 170 and would fit into a slot 184B of an adjacent wafer (not shown).

Slot 218 allows tail region 222 to be bent out of the plane of plate 150, if desired. FIG. 9A shows traces 910 and 912 on a printed circuit board routed between holes used to mount a connector according to the invention. FIG. 9A shows portions of a column of signal holes 186 and portions of a column of ground contacts 188. When the connector is used to carry single ended signals, it is desirable that the traces 910 and 912 be separated by ground to the greatest extent possible. Thus, it is desirable that the ground holes 188 be centered between the column of signal holes 186 so that the signal traces 910 and 912 can be routed between the signal holes 186 and ground holes 188. On the other hand, FIG. 9B shows the preferred routing for differential pair signals. For differential pair signals, it is desirable that the traces be routed as close together as possible. To allow the traces 914 and 916 to be close together, the ground holes 188 are not centered between columns of signal holes 186. Rather, they are offset to be as close to one row of signal contacts 186. That placement allows both signal traces 914 and 916 to be routed between the ground holes 188 and

a column of signal holes 186. In the single ended configuration, tail region 222 is bent out of the plane of plate 150. For the differential configuration, it is not bent.

It should also be noted that plate 128 (FIG. 1) can be similarly bent in its tail region, if desired. In the preferred embodiment, though, plate 128 is not bent for single ended signals and is bent for differential signals.

Tabs 220 are bent out of the plane of plate 150 prior to injection molding of the housing 170. Tabs 220 will wind up between holes 180 (FIG. 1). Tabs 220 aid in assuring that plate 150 adheres to housing 170. They also reinforce housing 170 across its face, i.e. that surface facing pin header 114.

FIG. 3 shows shield 150 after it has been insert molded into housing 170 to form ground portion 166. FIG. 3 shows that housing 170 includes pyramid shaped projections 310 on the face of shield piece 166. Matching recesses (not shown) are included in the floor of pin header 114. Projections 310 and the matching recesses serve to prevent the spring force of torsional beam contacts 142 from spreading adjacent wafers 154 when daughter card connector 116 is inserted into pin header 114.

FIG. 4 shows receptacle contact blank 400. Receptacle contact blank is preferably stamped from a sheet of metal. Numerous such blanks are stamped in a roll. In the preferred embodiment, there are eight receptacle contacts 410A...410H. The receptacle contacts 410 are held together on carrier strips 412, 414, 416, 418 and 422. These carrier strips are severed to separate contacts 410A....410H after housing 172 has been molded around the contacts. The carrier strips can be retained during much of the manufacturing operation for easy handling of receptacle portions 168.

Each of the receptacle contacts 410A...410H includes two legs 182. The legs 182 are folded and bent to form the receptacle 158.

Each receptacle contact 410A...410H also includes a transmission region 424 and a tail region 426. FIG. 4 shows that the transmission regions 424 are equally spaced. This arrangement is preferred for single ended signals as it results in maximum spacing between the contacts.

FIG. 4 shows that the tail regions are suitable for being press fit into plated through-holes. Other types of tail regions might be used. For example, solder tails might be used instead.

FIG. 5 shows receptacle contact blank 400 after housing 172 has been molded around it.

FIG. 6 shows a receptacle contact blank 600 suitable for use in an alternative embodiment of the invention. Receptacle contacts 610A...610H are grouped in pairs: (610A and 610B), (610C and 610D), (610E and 610F) and (610G and 610H). Transmission regions 624 of each pair are as close together as possible while maintaining differential impedance. This increases the spacing between adjacent pairs. This configuration improves the signal integrity for differential signals.

The tail region 626 and the receptacles of receptacle contact blank 400 and 600 are identical. These are the only portions of receptacle contacts 410 and 610 extending from housing 172. Thus, externally, signal portion 168 is the same for either single ended or differential signals. This allows single ended and differential signal wafers to be mixed in a single daughter card connector.

FIG. 7A illustrates a prior art connector as an aid in explaining the improved performance of the invention. FIG. 7A shows a shield plate 710 with a cantilevered beam 712 formed in it. The cantilevered beam 712 engages a

blade 714 from the pin header. The point of contact is labeled X. Blade 714 is connected to a backplane (not shown) at point 722.

Signals are transmitted through signal pins 716 and 718 running adjacent to the shield plate. Plate 710 and blade 714 act as the signal return. The signal path 720 through these elements is shown as a loop. It should be noted that signal path 720 cuts through pin 718. As is well known, a signal traveling in a loop passing through a conductor will inductively couple to the conductor. Thus, the arrangement of FIG. 7A will have relatively high coupling or cross talk from pin 716 to 718.

FIG. 7B shows a side view of the arrangement of FIG. 7A. As the cantilevered beam 712 is above the blade 714 its distance from pin 716 is d_1. In contrast, blade 714 has a spacing of d_2, which is larger. In the transmission of high frequency signals, the distance between the signal path and the ground dictates the impedance of the signal path. Changes in distance mean changes in impedance. Changes in impedance cause signal reflections, which is undesirable.

FIG. 7C shows the same arrangement upon mating. The blade 714 must slide under cantilevered beam 712. If not inserted correctly, blade 714 can but up against the end of cantilevered beam 712. This phenomenon is called "stubbing." It is highly undesirable in a connector because it can break the connector.

In contrast, FIG. 8 shows in a schematic sense the components of a connector manufactured according to the invention. Shield plates 128 and 150 overlap. Contact is made at the point marked X on torsional beam 146. Signal path 820 is shown to pass through a signal pin 122, return through plate 150 to point of contact X, pass through arm 146, through plate 128 and through tail 130. Signal path 820 is then completed through the backplane (not shown in FIG. 8). Significantly, signal path 820

does not cut through any adjacent signal pin 122. In this way, cross talk is significantly reduced over the prior art.

FIG. 8B illustrates schematically plates 128 and 150 prior to mating of daughter card connector 116 to pin header 114. In the perspective of FIG. 8B, arm 146 is shown bent out of the plane of plate 128. As plates 150 and 128 slide along one another during mating, arm 146 is pressed back into the plane of plate 128.

FIG. 8C show plates 128 and 150 in the mated configuration. Dimple 810 pressed into arm 146 is shown touching plate 150. The torsional spring force generated by pressing arm 146 back into the plane of plate 128 ensures a good electrical contact. It should be noted that the spacing between the plates 128 or 150 and an adjacent signal contact do not have as large a discontinuity as shown in FIG. 7B. This improvement should improve the electrical performance of the connector.

It should also be noted that in moving from the configuration of FIG. 8B to FIG. 8C, there is not an abrupt surface that could lead to stubbing. Thus, with torsional contacts, the mechanical robustness of the connector should be improved in comparison to the prior art.

FIG. 10 shows an alternative embodiment of a wafer 154 (FIG. 1). In the embodiment of FIG. 10, a shield blank on carrier strip 1010 is encapsulated in an insulative housing 1070 through injection molding. Shield tails 1030 are shown extending from housing 1070. Housing 1070 includes cavities 1016, 1017, 1018 and 1019. The shield blank is cut and bent to make contacts 1020 within cavities 1016, 1017, 1018 and 1019.

Cavities 1016, 1017, 1018 and 1019 have holes 1022 formed in their floors. Pins from the pin header are inserted through the holes during mating and engage,

through the springiness of the pin as well as of contacts 1020 ensure electrical connection to the shield.

In the embodiment of FIG. 10, the signal contacts are stamped separately. The transmission line section of the contacts are laid into cavities 1026. The receptacle portions of the signal contacts are inserted into cavities 1024.

A wafer as in FIG. 10 illustrates that any number of signal contacts might be used per column. In FIG. 10, four signal contacts per column are shown. That figure also illustrates that pins might be used in place of a plate 128. However, there might be differences in electrical performance. A plate could be used in conjunction with the configuration of FIG. 10. In that case, instead of a series of separate holes 1022 in cavities 1016, 1017, 1018 and 1019, a slot would be cut through the cavities.

FIG. 11A shows an alternative embodiment for contacts 142 on plate 128. Plate 1128 includes a series of torsional contacts 142. Each contact is made by stamping an arm 1146 from plate 1128. Here the arms have a generally serpentine shape. As described above, it is desirable for the arms 146 to be long enough to provide good flexibility. However, it is also desirable for the current to flow through the contacts 1142 in an area that is as narrow as possible in a direction perpendicular to the flow of current through signal pins 122. To achieve both of these goals, arms 1146 are stamped in a serpentine shape.

FIG. 11B shows plate 1128 in cross section through the line indicated as B-B in FIG. 1A. As shown, arms 1146 are bent out of the plane of plate 1128. During mating of the connector half, they are pressed back into the plane of plate 1128, thereby generating a torsional force.

FIG. 12 shows an additional view of connector 100. FIG. 12 shows face 1210 of daughter card connector 116. The lower surface of pin header 114 is also visible. In this view, it can be seen that the press fit tails 124 of plate 128 have an orientation that is at right angles to the orientation of press fit tails 130 of signal pins 122.

EXAMPLE

A connector made according to the invention was made and tested. The test was made with the single ended configuration and measurements were made on one signal line with the ten closest lines driven. For signal rise times of 500ps, the backward crosstalk was 4.9%. The forward cross talk was 3.2%. The reflection was too small to measure. The connector provided a real signal density of 101 per linear inch.

Having described one embodiment, numerous alternative embodiments or variations might be made. For example, the size of the connector could be increased or decreased from what is shown. Also, it is possible that materials other than those expressly mentioned could be used to construct the connector.

Various changes might be made to the specific structures. For example. clips 174 are shown generally to be radially symmetrical. It might improve the effectiveness of the shield plate 150 if clips 174 were elongated with a major axis running parallel with the signal contacts in signal pieces 168 and a perpendicular minor axis which is as short as possible.

Also, manufacturing techniques might be varied. For example, it is described that daughter card connector 116 is formed by organizing a plurality of wafers onto a stiffener. It might be possible that an equivalent structure might be formed by inserting a plurality of shield pieces and signal receptacles into a molded housing.

Therefore, the invention should be limited only by the spirit and scope of the appended claims.

What is claimed is

1. An electrical connector comprising:
   a) a pin header comprising:
      i) an insulative base;
      ii) a plurality of columns of pins attached to the insulative based, each column having a plurality of pins;
      iii) a first plurality of plates attached to the insulative base, each plate disposed between an adjacent column of pins and each plate having formed therein a plurality of torsional contacts;
   b) a daughter card connector comprising:
      i) an insulative base shaped to mate with the insulative base of the pin header;
      ii) a plurality of columns of receptacles, each column having a plurality of receptacles disposed to engage one of the plurality of pins;
      iii) a second plurality of plates, each plate disposed between an adjacent column of receptacles and being disposed to engage the plurality of torsional contacts on one of the plurality of plates in the pin header.

2. The electrical connector of claim 1 wherein
   a) each of the plurality of columns of pins includes a first number of pins; and
   b) each of the first plurality of plates in the pin header has a second number of contact tails extending therefrom, said second number being equal to or greater than the first number minus one.

3. The electrical connector of claim 1 wherein each of the torsional contacts comprises at least one arm stamped from one of the first plurality of plates, the arm being connected to the plate at two points and bent out of the plane of the plate.

4. The electrical connector of claim 1 wherein each of the torsional contacts comprises an arm stamped out of one of the first plurality of plates, the arm having a thickness less than the thickness of the plate.

5. The electrical connector of claim 1 wherein adjacent receptacles within the same column are spaced apart by an amount less than or equal to 2 mm and adjacent columns of receptacles are spaced apart by an amount less than or equal to 2.25 mm.

6. The electrical connector of claim 1 wherein each of the torsional contacts contains an arm and the arm has a serpentine shape.

7. The electrical connector of claim 1 wherein the daughter card connector comprises a plurality of modules, the connector additionally comprising a metal stiffener to which each of the plurality of modules is attached.

8. An electrical connector incorporated into a back plane assembly with a backplane and at least one daughter card, the electrical connector comprising:
a) a first connector piece having:
i) a plurality of pin shaped signal contacts, each signal contact having a tail portion attached to the backplane, the pin shaped

signal contacts being disposed in a plurality of parallel columns;

ii) a first plurality of shield plates, each shield plate being disposed between adjacent columns of signal contacts and each having a plurality of tail portions extending therefrom and attached to the backplane, each tail portion of each shield plate being disposed between tails portions of adjacent signal contacts within the same column of signal contacts, wherein, for each shield plate, there is one tail portion between each pair of adjacent signal contacts in an adjacent column of signal contacts;

b) a second connector piece having:

i) a plurality of receptacle signal contacts, the plurality of receptacle signal contacts being disposed in a plurality of parallel columns with each receptacle disposed to engage a pin shaped signal contact;

ii) a second plurality of shield plates, each shield plate being disposed between adjacent columns of receptacle signal contacts, wherein each of the second plurality of shield plates mechanically engages one of the first plurality of shield plates with contact arms attached to one of the first or second plurality of shield plates at two points.

9. The electrical connector of claim 8 wherein each column of signal contacts has at least six signal contacts.

10. The electrical connector of claim 8 additionally comprising a means for providing a return current path for any given pin shaped signal contact does not cross any other pin shaped signal contact, wherein said means includes the first plurality of shield plates and the second plurality of shield plates.

11. The electrical connector of claim 8 wherein the tail portions of the signal contacts and the tail portions of the plates are press fit tails and he tail portions of the signal contacts are at right angles to the tail portions of the plates.

12. The electrical connector of claim 8 wherein a portion of the first plurality of plates has a slot cut therein and the plate has a bend along a line perpendicular to the slot, with the portion of the plate on one side of the bend forming a tail region and the portion of the plate on the other side of the bend forming a shield region, with the tail region and the shield region being parallel and the tail portions being connected to the tail region of the plate.

13. The electrical connector of claim 8 wherein the tail portions of the first plurality of plates are grounded in the backplane.

14. An electrical connector of the type having two inermateable pieces, each piece having a plurality of signal contacts disposed in columns to define a field of signal contacts, the connector additionally comprising a plurality of means, disposed between adjacent columns of signal contacts, for providing a return current path for each of the signal contacts

within a column of signal contacts, the return current paths being within the field of signal contacts, wherein each means for providing a return current path comprises a pair of parallel plates electrically engaging one another at a plurality of points, the plates having a plurality of contact tails extending therefrom, said contact tails being disposed intermediate adjacent signal contacts.

15. The connector of claim 14 wherein the number of contact tails on each of the plates is greater than or equal to the number of signal contacts in each column minus one.

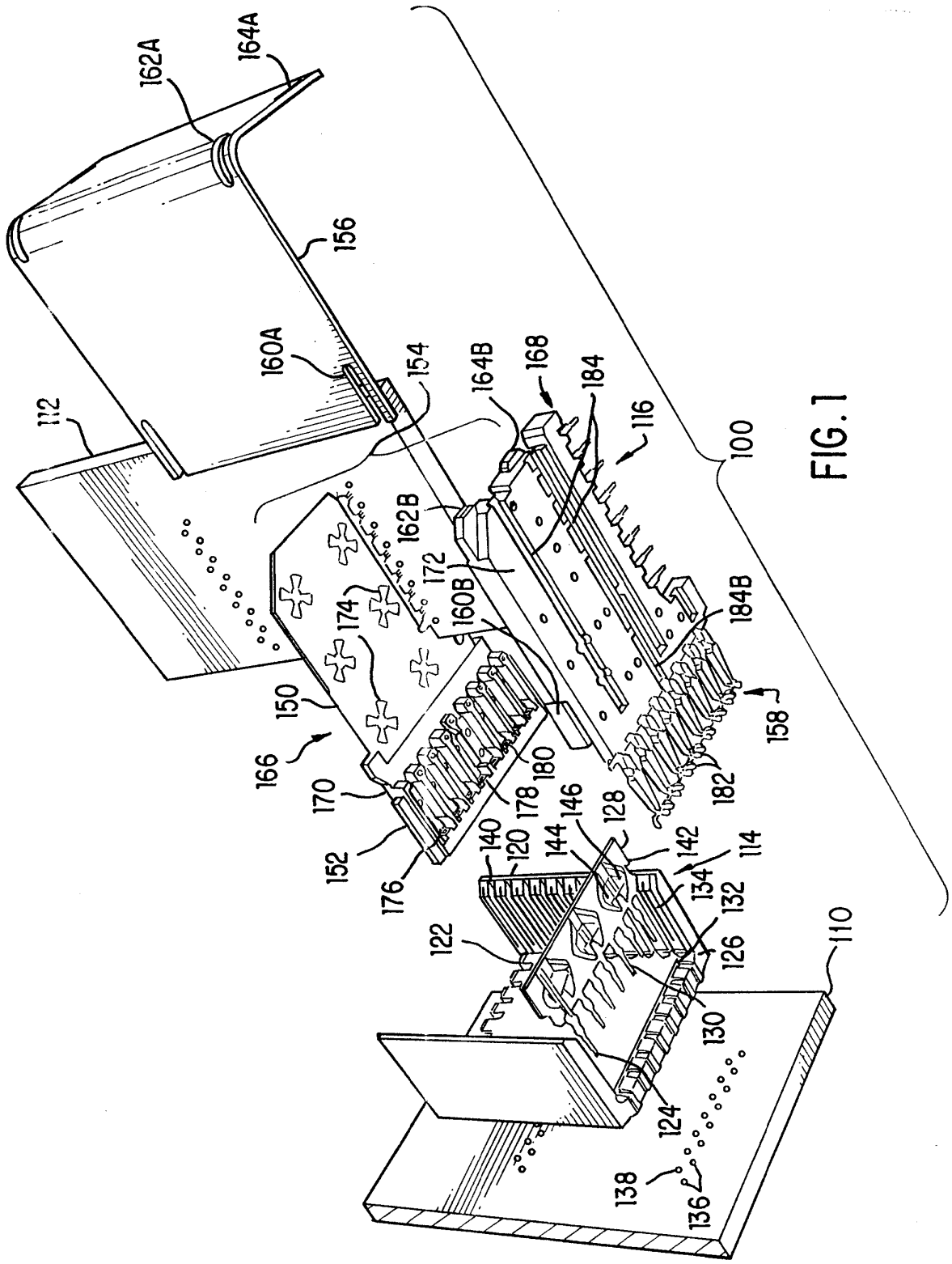
16. The connector of claim 15 wherein one of the plates in each pair of parallel plates has stamped therein a plurality of arms having at least two ends and being attached to the plate at the two ends.

17. The connector of claim 16 wherein each of the arms is coined to have a thickness than the thickness of the plate.

18. The connector of claim 17 wherein each of the arms has a serpentine shape.

19. The connector of claim 14 wherein the signal contacts are spaced to provide a real signal density of at least 100 per linear inch and a backward cross talk below 5% at 500 psec rise time.

20. The connector of claim 19 wherein the number of signal contacts in each column is eight.


162A
164A
156
160A
154
164B
168
184
116
112
100
162B
172
160B
184B
174
150
158
166
180
170
178
146
128
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142
114
152
176
134
132
122
126
110
130
124
138
136

FIG. 1

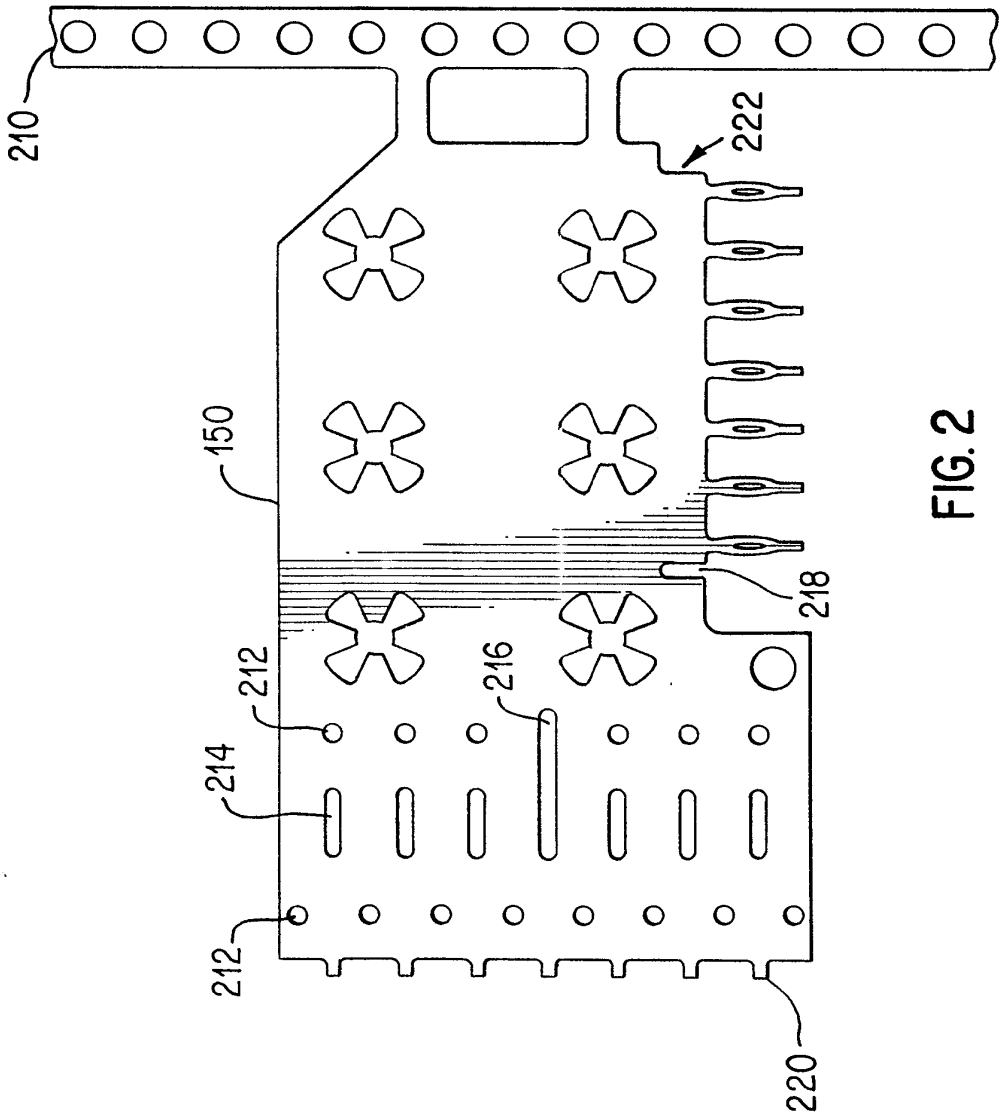

FIG. 2

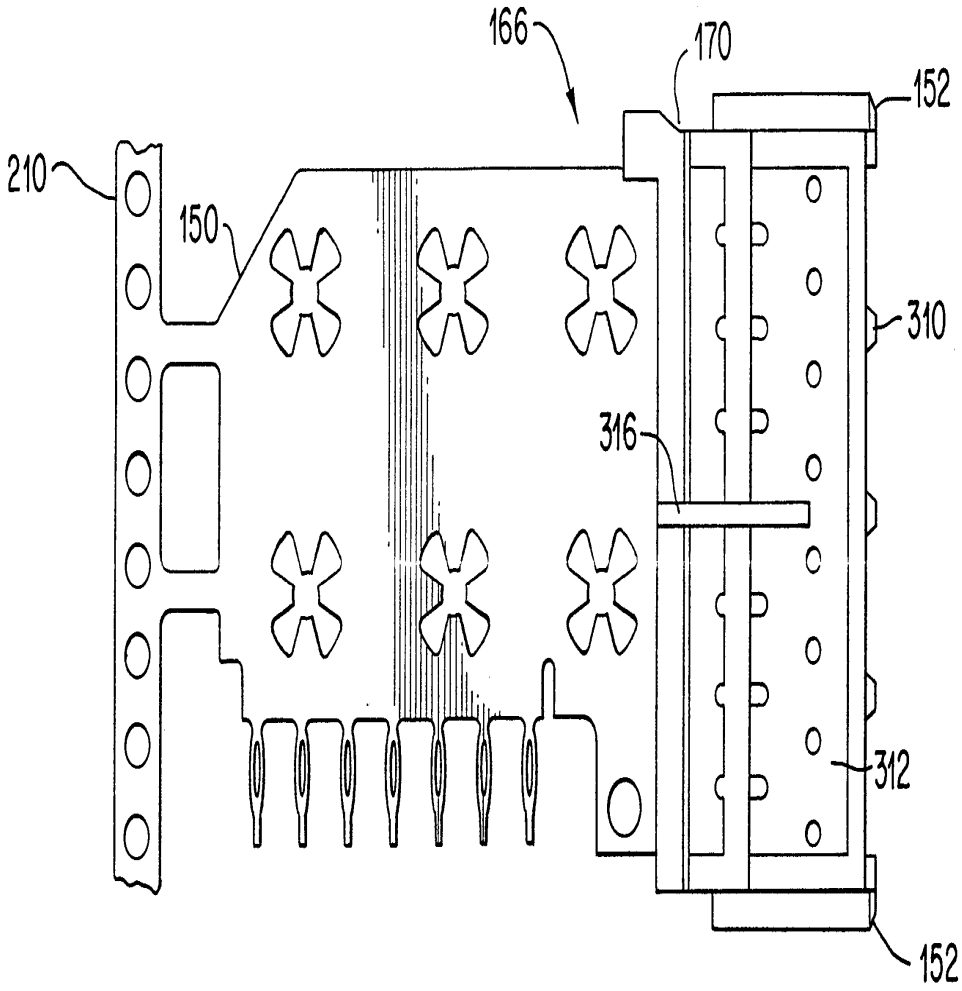

FIG. 3

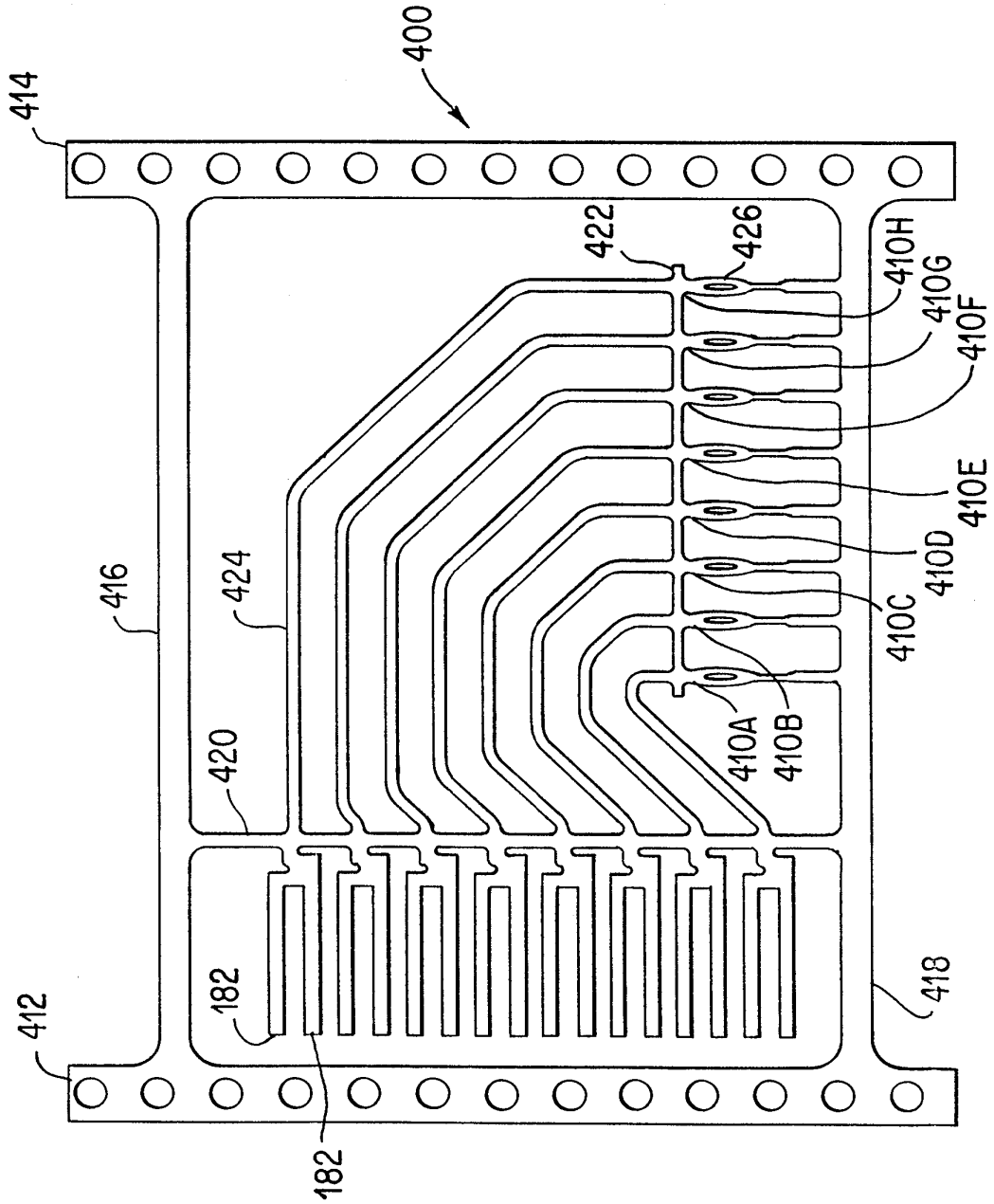
400
414
422
426
410H
410G
410F
410E
410D
410C
410A
410B
416
424
420
182
412
418
182

FIG.4

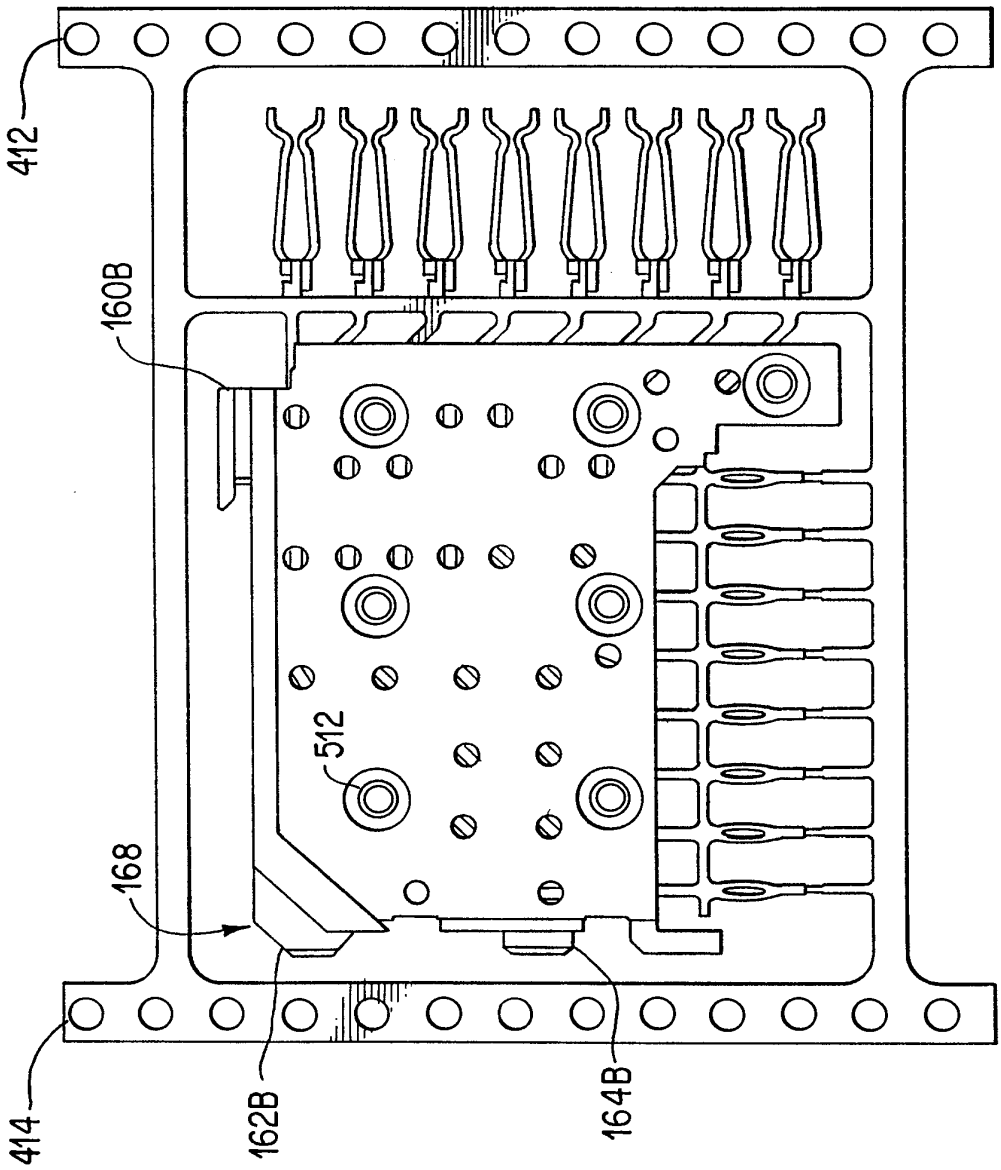

FIG.5

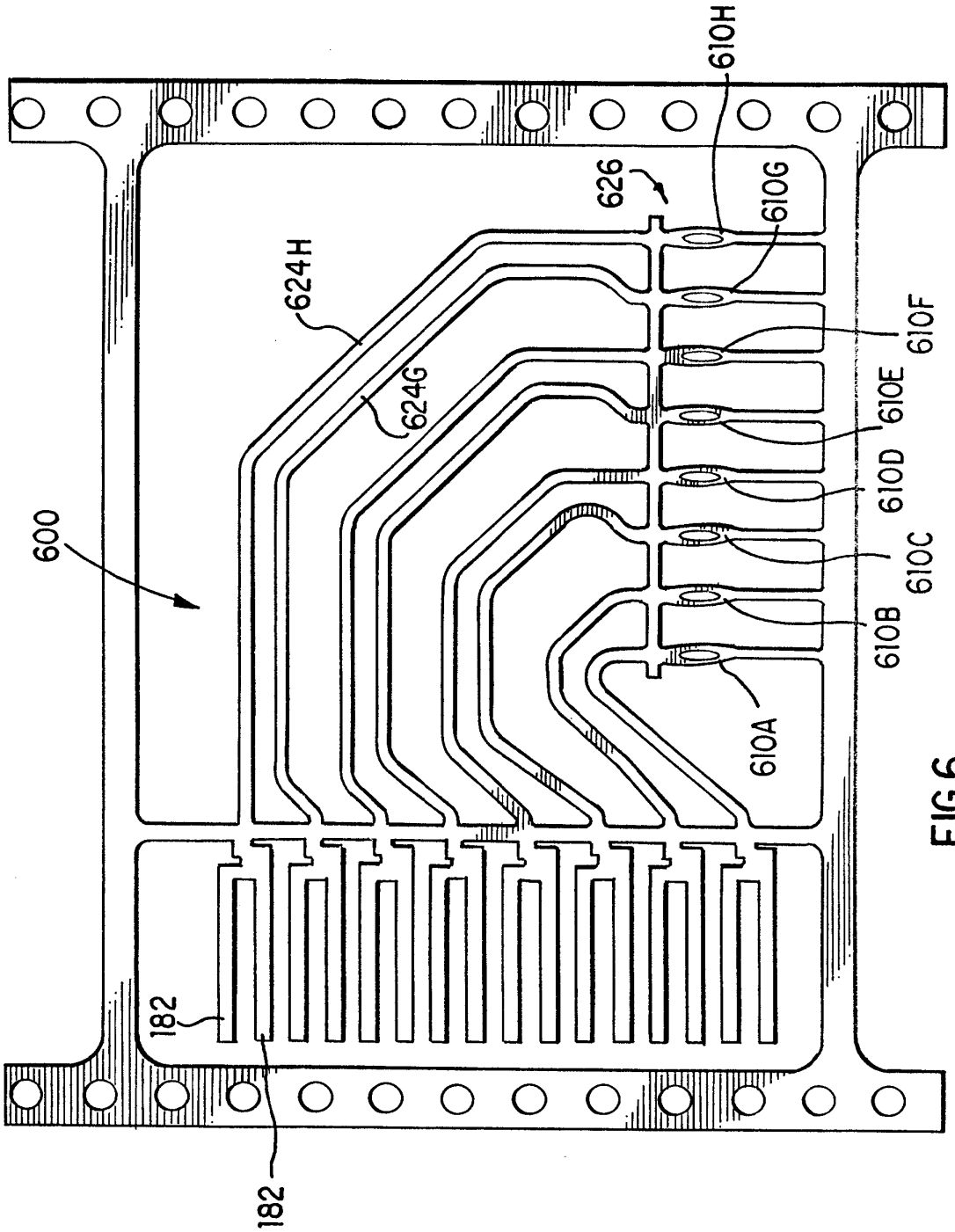
610H
626
610G
624H
610F
624G
610E
610D
600
610C
610B
610A
182
182

FIG.6

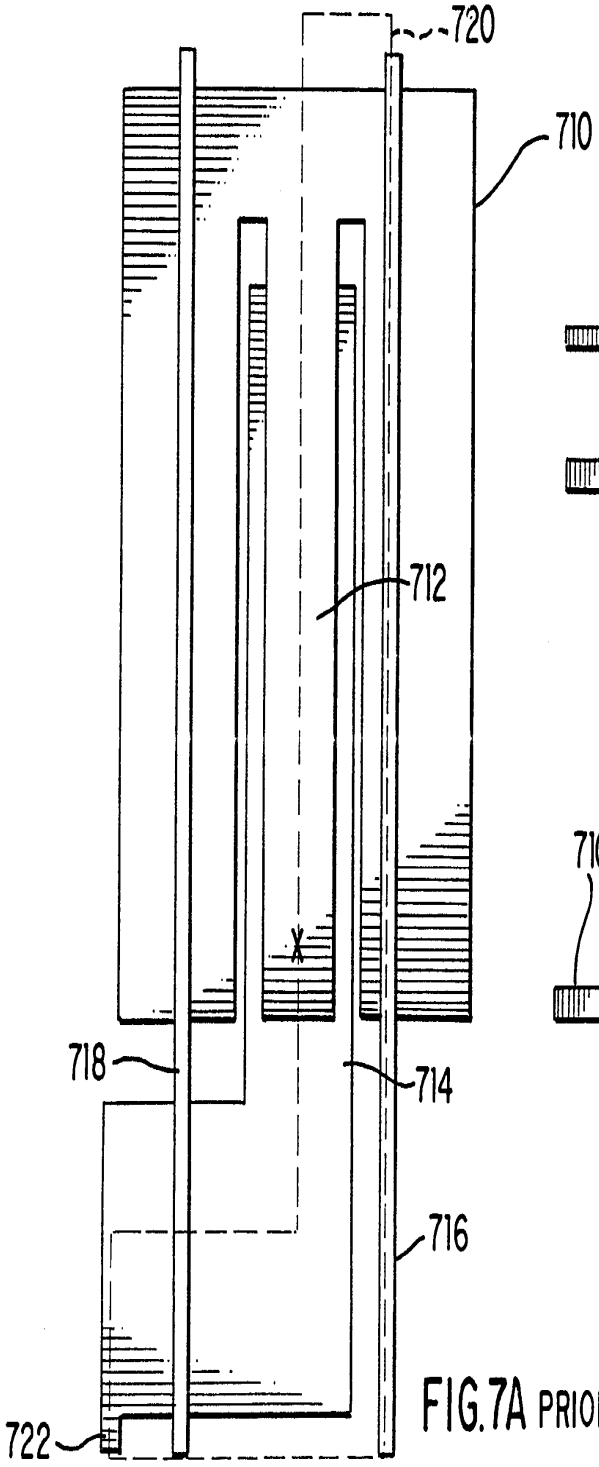

FIG.7A PRIOR ART

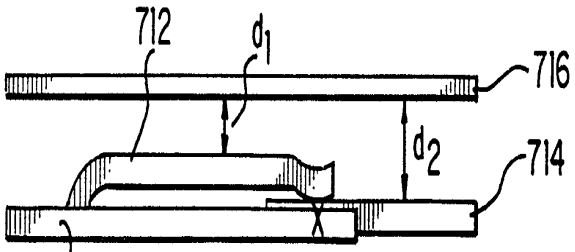

FIG.7B PRIOR ART

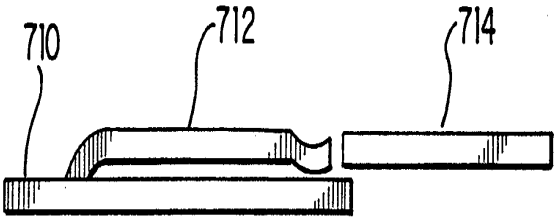

FIG.7C PRIOR ART

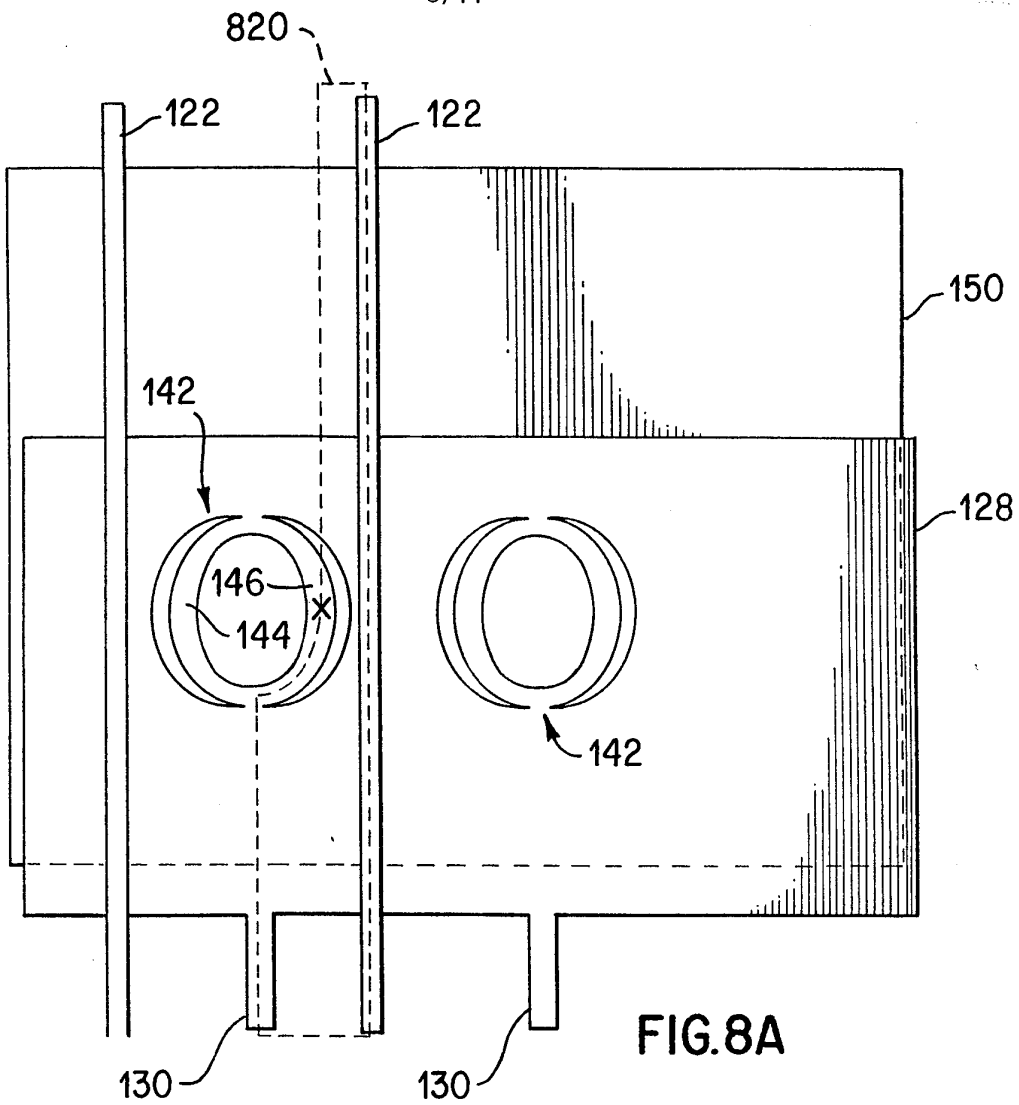

FIG.8A

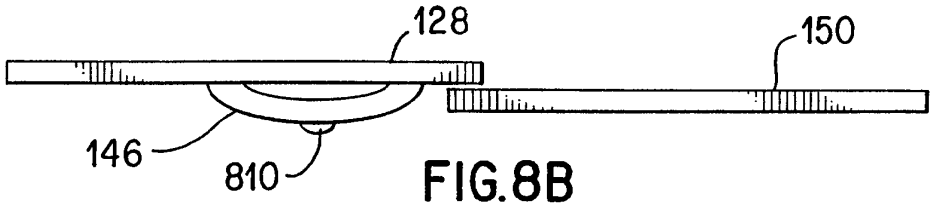

FIG.8B

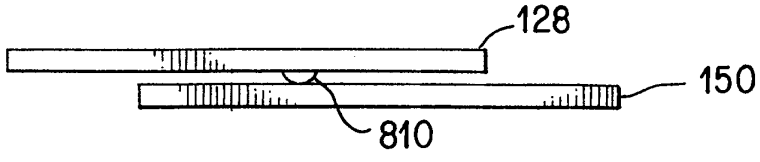

FIG.8C

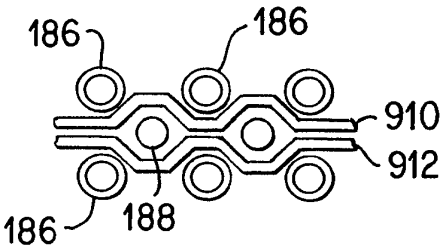

FIG. 9A

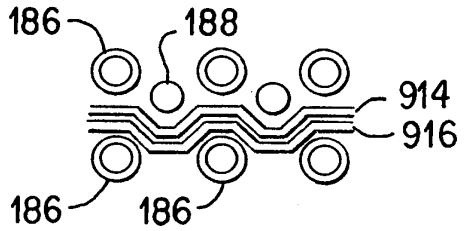

FIG. 9B

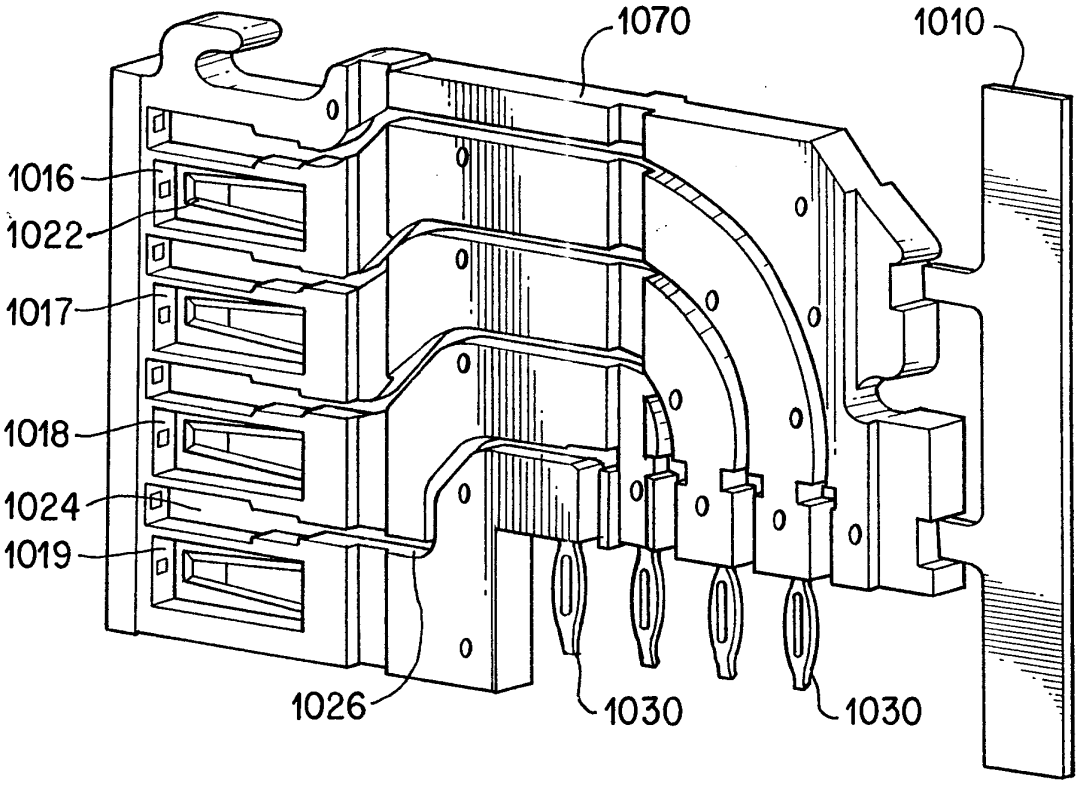

FIG. 10

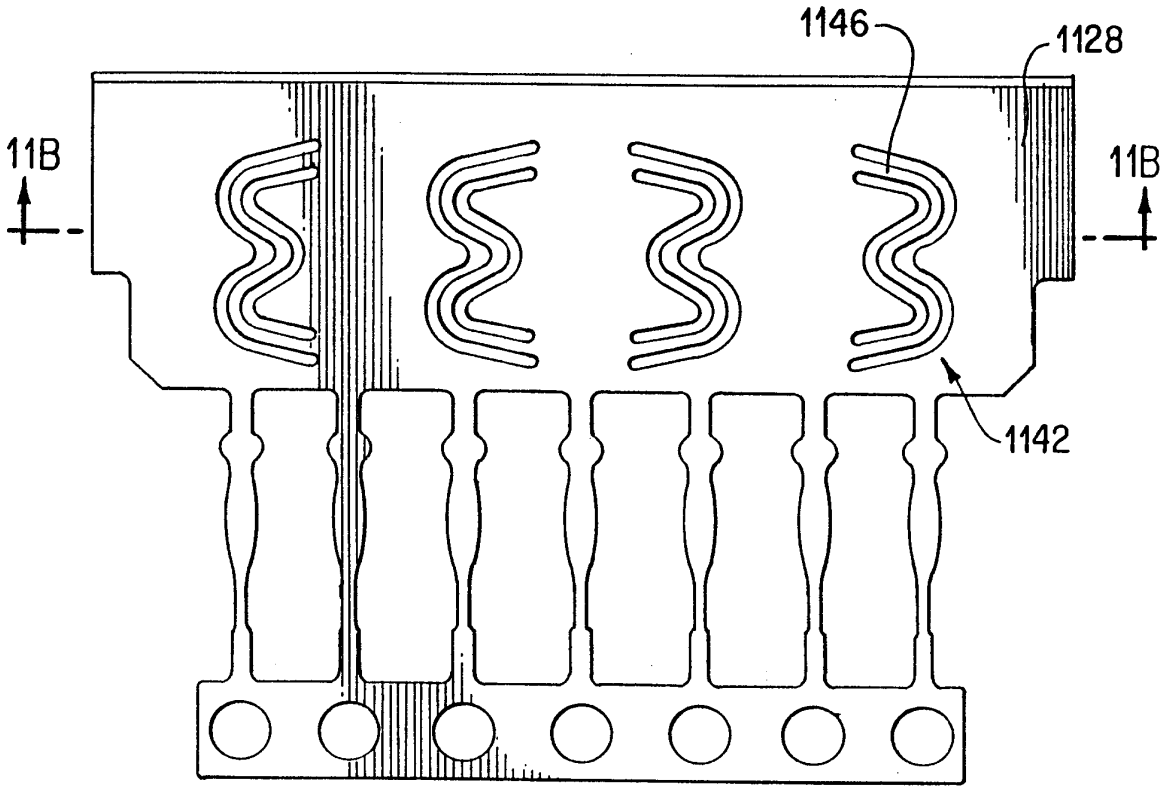

FIG.11A

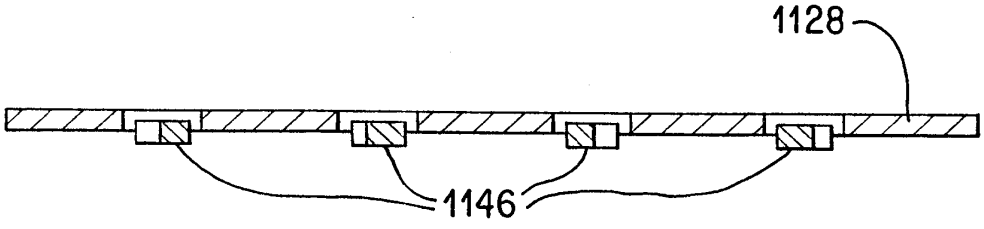

FIG.11B

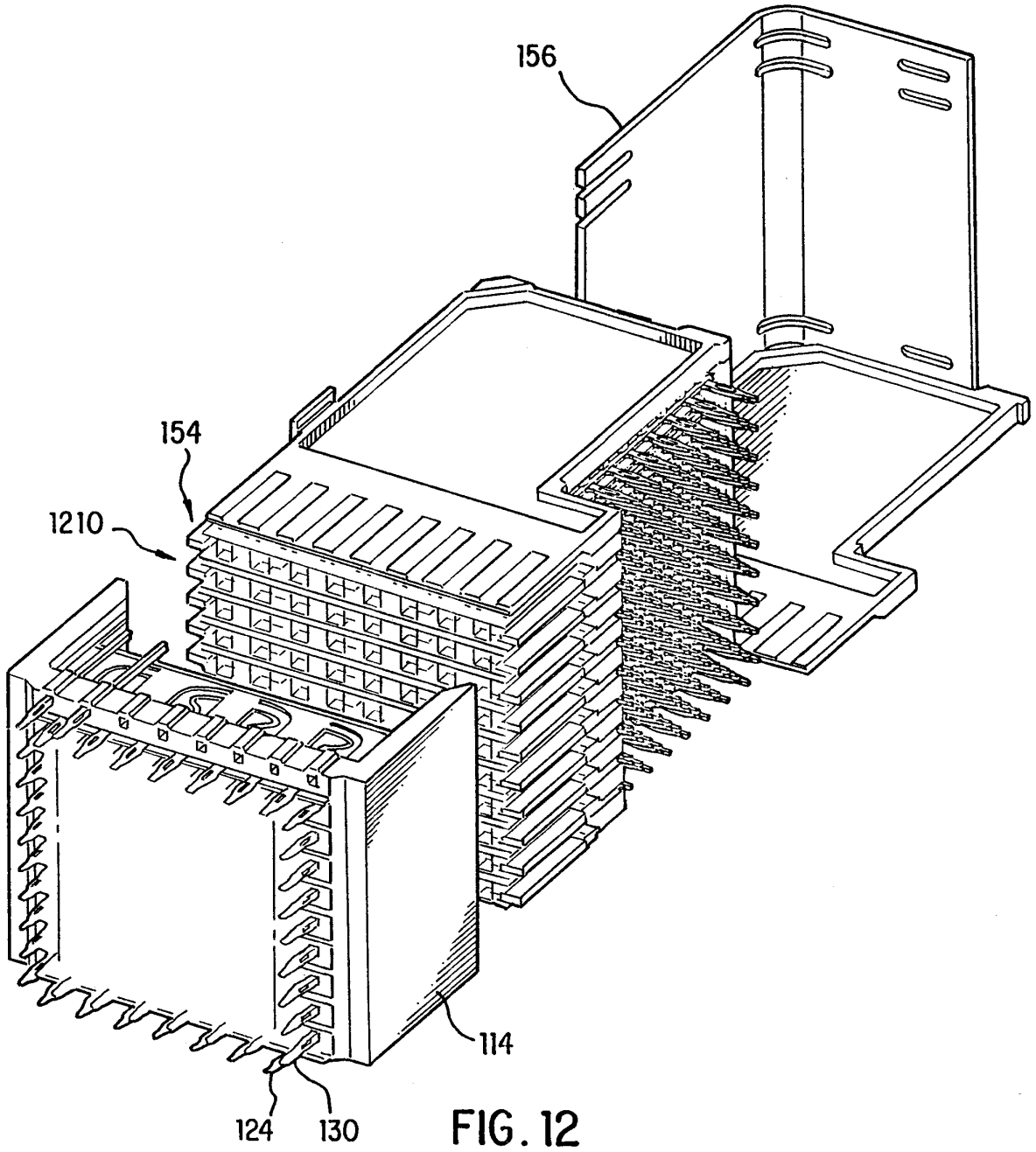

FIG. 12

INTERNATIONAL SEARCH REPORT

Int. ational Application No
PCT/US 98/01168

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01R23/68

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01R

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0 492 944 A (AMP INC) 1 July 1992 see column 3, line 28 - column 6, line 12 see column 7, line 13 - line 48 see figures 1-15	1,3,6, 8-14,16
A	DE 195 46 932 C (INOVAN STROEBE) 30 January 1997 see column 4, line 22 - column 5, line 19 see figures 1,2	1,3,6,8, 16-18
P,A	US 5 645 436 A (SHIMIZU MANABU ET AL) 8 July 1997 see column 5, line 54 - column 6, line 57 see column 8, line 34 - column 9, line 20 see figure 9	1,8,9,14

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

1

Date of the actual completion of the international search	Date of mailing of the international search report
31 March 1998	22. 04. 98

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Stirn, J-P

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

In..ational Application No
PCT/US 98/01168

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0492944 A	01-07-92	US 5046960 A	10-09-91
		DE 69117703 D	11-04-96
		DE 69117703 T	19-09-96
		JP 4294076 A	19-10-92
		KR 9704221 B	26-03-97
DE 19546932 C	30-01-97	NONE	
US 5645436 A	08-07-97	JP 6243936 A	02-09-94

Form PCT/ISA/210 (patent family annex) (July 1992)

Electronic Patent Application Fee Transmittal

Application Number:	15065683
Filing Date:	09-Mar-2016
Title of Invention:	HIGH PERFORMANCE CABLE CONNECTOR
First Named Inventor/Applicant Name:	Donald W. Milbrand
Filer:	Edmund J. Walsh/Patricia McDonald
Attorney Docket Number:	A0863.70051US04

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension - 1 month with $0 paid	1251	1	200	200
Miscellaneous:				
RCE- 2ND AND SUBSEQUENT REQUEST	1820	1	1900	1900
		Total in USD ($)		**2100**

Electronic Acknowledgement Receipt

EFS ID:	35635945
Application Number:	15065683
International Application Number:	
Confirmation Number:	5112
Title of Invention:	HIGH PERFORMANCE CABLE CONNECTOR
First Named Inventor/Applicant Name:	Donald W. Milbrand
Customer Number:	23628
Filer:	Edmund J. Walsh/Patricia McDonald
Filer Authorized By:	Edmund J. Walsh
Attorney Docket Number:	A0863.70051US04
Receipt Date:	04-APR-2019
Filing Date:	09-MAR-2016
Time Stamp:	22:08:53
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$2100
RAM confirmation Number	040519INTEFSW22094000
Deposit Account	232825
Authorized User	Patricia McDonald
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.17 (Patent application and reexamination processing fees)	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Continued Examination (RCE)	A086370051US04-RCE-EJW.pdf	28086 74190df766870c737f628561314a2b92c7dc9385	no	1
Warnings:					
This is not a USPTO supplied RCE SB30 form.					
Information:					
2	Extension of Time	A086370051US04-EXT-EJW.pdf	24444 67f8cb752691ec52fd71c56a74f1b70d448cf87e	no	1
Warnings:					
Information:					
3	Fee Worksheet (SB06)	A086370051US04-FEE-EJW.pdf	32811 2f4aaa8d98bb0ee135bc7ffe70f371ba11cb19a4	no	1
Warnings:					
Information:					
4		A086370051US04-AMN-EJW.pdf	156837 11bb8fe40c88b008ad84901bb6fe96df1dc0333c	yes	24

Multipart Description/PDF files in .zip description

Document Description	Start	End
Amendment Submitted/Entered with Filing of CPA/RCE	1	1
Claims	2	11
Applicant Arguments/Remarks Made in an Amendment	12	24

Warnings:

Information:

5		A086370051US04-IDS-EJW.pdf	60589 670e85a36c3a683d8e674d30949bf3e2e1fefeba	yes	6
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Transmittal Letter		1	4	
	Information Disclosure Statement (IDS) Form (SB08)		5	6	
Warnings:					
Information:					
6	Foreign Reference	CN1179448C_w_Eng_MT.pdf	785796 b5ea04a85c620c39ce7aac6d3cdcbe9bab9faf91	no	45
Warnings:					
Information:					
7	Foreign Reference	CN1799290_w_Eng_MT.pdf	2950217 b8321ea48d14f8bbe8353d051a18593999901828	no	91
Warnings:					
Information:					
8	Foreign Reference	CN101120490B_w_Eng_MT.pdf	922332 96a6c448ed2419ea5168d00c9979537113bddbbe	no	53
Warnings:					
Information:					
9	Foreign Reference	CN101176389_w_Eng_MT.pdf	729851 80c5c6265a2587274c36330fde867303c8a65674	no	44
Warnings:					
Information:					
10	Foreign Reference	CN101600293A_w_Eng_MT.pdf	556190 a96a4c6ce44776f56e69bb6754419e77c92fa4d7	no	19
Warnings:					
Information:					

11	Foreign Reference	CN101600293B_w_Eng_MT.pdf	1132022 7b89c86d75d8572b03d30c1c98b254ec9d2c118a	no	19
Warnings:					
Information:					
12	Foreign Reference	CN201846527U_w_Eng_MT.pdf	662607 b5784bf3570f54bbf73f645089e52eea59db13b0	no	35
Warnings:					
Information:					
13	Foreign Reference	DE60216728T2_w_Eng_Abs_Only.pdf	812896 7fb441f91f6e9f28fe1a37920d806631903dd73b	no	23
Warnings:					
Information:					
14	Foreign Reference	EP1018784.pdf	800006 a05ac35f9d15699504632ce0d379af15b235efe0	no	17
Warnings:					
Information:					
15	Foreign Reference	JP2001510627A_w_Eng_Abs_Only.pdf	1277103 94a7b183b33976d70b3a5367fed69ca1ca04db50	no	44
Warnings:					
Information:					
16	Foreign Reference	MX9907324A_w_Eng_Abstract_Only.pdf	1811029 a5d4ddcd8057c581a7c83c5df578eb8cec5f6c3b	no	51
Warnings:					
Information:					
17	Foreign Reference	WO9835409A1.pdf	1463994 b03213c96a413d3c6a3fb6f708f9d7ccdf6ad568	no	39
Warnings:					
Information:					

18	Fee Worksheet (SB06)	fee-info.pdf	32794 2e733b91e8866096dcb6dddb7b60128c57fdc595	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	14239604	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 15/065,683	Filing Date 03/09/2016	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $80 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $420 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	04/04/2019	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 32	Minus	** 29	= 3		x $100 =	300
	Independent (37 CFR 1.16(h))	* 4	Minus	*** 4	= 0		x $460 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	300

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/ROLITA M WIMBUSH/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

Document code: WFEE

United States Patent and Trademark Office
Sales Receipt for Accounting Date: 04/10/2019

RWIMBUSH SALE #00000001 Mailroom Dt: 04/04/2019 232825 15065683
01 FC : 1202 300.00 DA

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

23628 7590 06/05/2019

WOLF GREENFIELD & SACKS, P.C.
600 ATLANTIC AVENUE
BOSTON, MA 02210-2206

EXAMINER
FIGUEROA, FELIX O

ART UNIT	PAPER NUMBER
2833	

DATE MAILED: 06/05/2019

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/065,683	03/09/2016	Donald W. Milbrand JR.	A0863.70051US04	5112

TITLE OF INVENTION: HIGH PERFORMANCE CABLE CONNECTOR

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0.00	$0.00	$1000	09/05/2019

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

23628 7590 06/05/2019
WOLF GREENFIELD & SACKS, P.C.
600 ATLANTIC AVENUE
BOSTON, MA 02210-2206

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/065,683	03/09/2016	Donald W. Milbrand JR.	A0863.70051US04	5112

TITLE OF INVENTION: HIGH PERFORMANCE CABLE CONNECTOR

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0.00	$0.00	$1000	09/05/2019

EXAMINER	ART UNIT	CLASS-SUBCLASS
FIGUEROA, FELIX O	2833	439-676000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1_____
2_____
3_____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑Issue Fee ❑Publication Fee (if required) ❑Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/065,683	03/09/2016	Donald W. Milbrand JR.	A0863.70051US04	5112

23628 7590 06/05/2019

WOLF GREENFIELD & SACKS, P.C.
600 ATLANTIC AVENUE
BOSTON, MA 02210-2206

EXAMINER	
FIGUEROA, FELIX O	

ART UNIT	PAPER NUMBER
2833	

DATE MAILED: 06/05/2019

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 15/065,683	Applicant(s) Milbrand et al.	
	Examiner FELIX O FIGUEROA	Art Unit 2833	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to the amendment and remarks filed 4/4/2019.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 1-8 and 10-33 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information , please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file areply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☑ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/FELIX O FIGUEROA/
Primary Examiner, Art Unit 2833

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/065,683	Milbrand et al.
	Examiner	Art Unit
	FELIX O FIGUEROA	2833

CPC - Searched*		
Symbol	**Date**	**Examiner**
H01R13/65807*, H01R13/6587*, H01R13/6586, H01R13/6585*, H01R13/658, H01R13/646, H01R13/6471	5/30/2017	FF
Updated search	12/27/2017	FF
Updated search	05/24/2019	FF

CPC Combination Sets - Searched*		
Symbol	**Date**	**Examiner**

US Classification - Searched*			
Class	**Subclass**	**Date**	**Examiner**
439	607.02, 607.03, 607.05, 607.06, 607.08, 607.1	5/30/2017	FF

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	**Date**	**Examiner**
EAST search including US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO ; DERWENT; IBM_TDB		FF
Inventor name search	5/30/2017	FF

Interference Search			
US Class/CPC Symbol	**US Subclass/CPC Group**	**Date**	**Examiner**
	See EAST history print out	05/24/2019	FF

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/065,683	Milbrand et al.
	Examiner	**Art Unit**
	FELIX O FIGUEROA	2833

CPC							
Symbol						**Type**	**Version**
H01R	/	13	/	26		F	2013-01-01
H01R	/	12	/	75		I	2013-01-01
H01R	/	13	/	6587		I	2013-01-01
H01R	/	13	/	6585		I	2013-01-01

CPC Combination Sets								
Symbol						**Type**	**Set**	**Ranking**	**Version**
	/		/						

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	32	
/FELIX O FIGUEROA/ Primary Examiner, Art Unit 2833	24 May 2019	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	6

U.S. Patent and Trademark Office — Part of Paper No.: 20190524

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/065,683	Milbrand et al.
	Examiner	**Art Unit**
	FELIX O FIGUEROA	2833

INTERNATIONAL CLASSIFICATION				
CLAIMED				
H01R	/	13	/	658

NON-CLAIMED				
	/		/	

US ORIGINAL CLASSIFICATION	
CLASS	**SUBCLASS**

CROSS REFERENCES(S)						
CLASS	**SUBCLASS (ONE SUBCLASS PER BLOCK)**					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	32	
/FELIX O FIGUEROA/ Primary Examiner, Art Unit 2833	24 May 2019	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	6

U.S. Patent and Trademark Office — Part of Paper No.: 20190524

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/065,683	Milbrand et al.
	Examiner	**Art Unit**
	FELIX O FIGUEROA	2833

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	5	10	19	19	29	28								
11	2	6	11	20	20	30	29								
12	3	7	12	21	21	31	30								
13	4	8	13	22	22	25	31								
14	5	9	14	10	23	26	32								
2	6	15	15	24	24	27	33								
3	7	16	16	32	25										
4	8	17	17	23	26										
	9	18	18	28	27										

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	32	
/FELIX O FIGUEROA/ Primary Examiner, Art Unit 2833	24 May 2019	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	6

U.S. Patent and Trademark Office — Part of Paper No.: 20190524

FORM PTO-1449/A and B (modified PTO/SB/08)				APPLICATION NO.: 15/065,683	ATTY. DOCKET NO.: A0863.70051US04
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				FILING DATE: March 9, 2016	CONFIRMATION NO.: 5112
				FIRST NAMED INVENTOR: Donald W. Milbrand, Jr.	
Sheet	1	of	1	GROUP ART UNIT: 2833	EXAMINER: F. O. Figueroa

U.S. PATENT DOCUMENTS

Examiner's Initials #	Cite No.	U.S. Patent Document Number	Kind Code	Name of Patentee or Applicant of Cited Document	Date of Publication or Issue of Cited Document MM-DD-YYYY
		5,166,527	A	Solymar	11-24-1992
		7,806,729	B2	Nguyen et al.	10-05-2010
		10,122,129	B2	Milbrand, Jr. et al.	11-06-2018

FOREIGN PATENT DOCUMENTS

Examiner's Initials #	Cite No.	Foreign Patent Document Office/ Country	Number	Kind Code	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Translation (Y/N)
		WO	2010/030622	A1	Molex Inc.	03-18-2010	

OTHER ART -- NON PATENT LITERATURE DOCUMENTS

Examiner's Initials #	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	Translation (Y/N)

[NOTE – No copies of U.S. patents, published U.S. patent applications, or pending, unpublished patent applications stored in the USPTO's Image File Wrapper (IFW) system, are included. See 37 CFR § 1.98 and 1287OG163. Copies of all other patent(s), publication(s), unpublished, pending U.S. patent applications, or other information listed are provided as required by 37 CFR § 1.98 unless 1) such copies were provided in an IDS in an earlier application that complies with 37 CFR § 1.98, and 2) the earlier application is relied upon for an earlier filing date under 35 U.S.C. § 120.]

EXAMINER:	DATE CONSIDERED:
/FELIX O FIGUEROA/	05/24/2019

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

6723165.1

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /F.O.F/

FORM PTO-1449/A and B (modified PTO/SB/08)	APPLICATION NO.: 15/065,683	ATTY. DOCKET NO.: A0863.70051US04
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	FILING DATE: March 9, 2016	CONFIRMATION NO.: 5112
	FIRST NAMED INVENTOR: Donald W. Milbrand, Jr.	
Sheet 1 of 2	GROUP ART UNIT: 2833	EXAMINER: F. O. Figueroa

U.S. PATENT DOCUMENTS

Examiner's Initials #	Cite No.	U.S. Patent Document Number	Kind Code	Name of Patentee or Applicant of Cited Document	Date of Publication or Issue of Cited Document MM-DD-YYYY
		5,176,538	A	Hansell III et al.	01-05-1993
		5,334,050	A	Andrews	08-02-1994
		6,409,543	B1	Astbury, Jr. et al.	06-25-2002
		10,243,304		Kirk et al.	03-26-2019
		2004-0005815	A1	Mizumura et al.	01-08-2004
		2005-0233610	A1	Tutt et al.	10-20-2005
		2006-0255876	A1	Kushta et al.	11-16-2006
		2009-0305533	A1	Feldman et al.	12-10-2009
		2018-0062323	A1	Kirk et al.	03-01-2018
		2018-0145438	A1	Cohen	05-24-2018
		2018-0219331	A1	Cartier et al.	08-02-2018

FOREIGN PATENT DOCUMENTS

Examiner's Initials #	Cite No.	Foreign Patent Document Office/ Country	Number	Kind Code	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Translation (Y/N)
		CN	1179448	C	Whitaker Corp	12-08-2004	Y
		CN	1799290	A	Nippon Electric Co	07-05-2006	Y
		CN	101120490	B	Amphenol Corp	11-17-2010	Y
		CN	101176389	A	Teradyne Inc	05-07-2008	Y
		CN	101600293	A	Hongfujin Prec Ind Shenzhen	12-09-2009	Y
		CN	101600293	B	Hongfujin Prec Ind Shenzhen	05-16-2012	Y
		CN	201846527	U	Molex Inc	05-25-2011	Y
		DE	60216728	T2	Amphenol Corp	11-08-2007	Y-abstract only; see also US6409543
		EP	1018784	A1	Fci S Hertogenbosch Bv	07-12-2000	
		JP	2001-510627	A		07-31-2001	Y-abstract only; see also WO9835409
		MX	9907324	A	Teradyne, Inc.	08-01-2000	Y-abstract only
		WO	98/35409	A1	Teradyne, Inc	08-13-1998	

EXAMINER:	DATE CONSIDERED:
/FELIX O FIGUEROA/	05/24/2019

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

7061174.1

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /F.O.F/

FORM PTO-1449/A and B (modified PTO/SB/08)				APPLICATION NO.: 15/065,683	ATTY. DOCKET NO.: A0863.70051US04
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				FILING DATE: March 9, 2016	CONFIRMATION NO.: 5112
				FIRST NAMED INVENTOR: Donald W. Milbrand, Jr.	
Sheet	2	of	2	GROUP ART UNIT: 2833	EXAMINER: F. O. Figueroa

OTHER ART -- NON PATENT LITERATURE DOCUMENTS

Examiner's Initials #	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	Translation (Y/N)

[NOTE – No copies of U.S. patents, published U.S. patent applications, or pending, unpublished patent applications stored in the USPTO's Image File Wrapper (IFW) system, are included. See 37 CFR § 1.98 and 1287OG163. Copies of all other patent(s), publication(s), unpublished, pending U.S. patent applications, or other information listed are provided as required by 37 CFR § 1.98 unless 1) such copies were provided in an IDS in an earlier application that complies with 37 CFR § 1.98, and 2) the earlier application is relied upon for an earlier filing date under 35 U.S.C. § 120.]

EXAMINER:	DATE CONSIDERED:

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

7061174.1

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /F.O.F/

EAST Search History

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S42	7	(receptacle and printed and circuit and board and housing and lead and conductive and parallel and perpendicular).clm.	US-PGPUB; USPAT	OR	ON	2019/05/24 11:23
S43	117	(receptacle and parallel and perpendicular and signal and ground).clm.	US-PGPUB; USPAT	OR	ON	2019/05/24 11:36

5/ 24/ 2019 1:40:03 PM
C:\ Users\ ffigueroa\ Documents\ EAST\ Workspaces\ 15065683.wsp

Doc Code: TRAN.LET
Document Description: Transmittal Letter

USED IN LIEU OF PTO/SB/21 (07-09)

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission	

Application Number	15/065,683-Conf. #5112
Filing Date	March 9, 2016
First Named Inventor	Donald W. Milbrand, Jr.
Art Unit	2833
Examiner Name	F. O. Figueroa
Attorney Docket Number	A0863.70051US04

ENCLOSURES (*Check all that apply*)

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment/Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Reply to Missing Parts/ Incomplete Application
  - ☐ Reply to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
- ☐ Request for Refund
- ☐ CD, Number of CD(s) _____
  - ☐ Landscape Table on CD
- ☐ After Allowance Communication to TC
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☐ Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- ☐ Proprietary Information
- ☐ Status Letter
- ☒ Other Enclosure(s) (please Identify below):

  Issue Fee Transmittal (Form PTOL-85B)

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	WOLF, GREENFIELD & SACKS, P.C.		
Signature	/Edmund J. Walsh/		
Printed name	Edmund J. Walsh		
Date	June 5, 2019	Reg. No.	32,950

Certificate of Electronic Filing under 37 C.F.R. § 1.8

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being transmitted via the Office's electronic filing system in accordance with 37 C.F.R. § 1.6(a)(4).

Dated: June 5, 2019 Electronic Signature for: /Trish McDonald/

7280283.1

PART B–FEE(S) TRANSMITTAL

Complete and send this form, together with the applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

By fax, send to: (571) 273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

WOLF, GREENFIELD & SACKS, P.C.
600 Atlantic Avenue
Boston, Massachusetts 02210-2206

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of ~~Mailing or~~ Transmission

I hereby certify that this Fee(s) Transmittal is being ~~deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being~~ transmitted to the USPTO via EFS-Web ~~or by facsimile to (571) 273-2885,~~ on the date below.

Trish McDonald	(Typed or printed name)
/Trish McDonald/	(Signature)
VIA EFS-Web June 5, 2019	(Date)

APPLICATION NO	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO	CONFIRMATION NO
15/065,683	03/09/2016	Donald W. Milbrand, Jr.	A0863.70051US04	5112

TITLE OF INVENTION: HIGH PERFORMANCE CABLE CONNECTOR

APPLN: TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1,000.00			$1,000.00	09/05/2019

EXAMINER	ART UNIT	CLASS-SUBCLASS
F. O. Figueroa	2833	

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363)

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1. Wolf, Greenfield & Sacks, P.C.
2.
3.

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Amphenol Corporation

(B) RESIDENCE: (CITY and STATE or COUNTRY): Wallingford, Connecticut

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. Fees Submitted: ☒ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies _____

4b. Method of Payment (*Please first reapply any previously paid fee shown above*):

☒ Electronic Payment via EFS-Web ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☒ The Director is hereby authorized to charge ~~the required fee(s),~~ any deficiency, or credit any overpayment to Deposit Account No. 23/2825

5. Change of Entity Status (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29. NOTE: Absent a valid Certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

☐ Applicant asserting small entity status. See 37 CFR 1.27. NOTE: If the application was previously under micro entity status, checking this box will be taken as a notification of loss of entitlement to micro entity status.

☐ Applicant changing to regular undiscounted fee status. NOTE: Checking this box will be taken as a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Edmund J. Walsh/ Date June 5, 2019

Typed or printed name Edmund J. Walsh Registration No. 32,950

7280284.1

Electronic Patent Application Fee Transmittal

Application Number:	15065683
Filing Date:	09-Mar-2016
Title of Invention:	HIGH PERFORMANCE CABLE CONNECTOR
First Named Inventor/Applicant Name:	Donald W. Milbrand
Filer:	Edmund J. Walsh/Patricia McDonald
Attorney Docket Number:	A0863.70051US04

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	1000	1000

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**1000**

Electronic Acknowledgement Receipt	
EFS ID:	36216445
Application Number:	15065683
International Application Number:	
Confirmation Number:	5112
Title of Invention:	HIGH PERFORMANCE CABLE CONNECTOR
First Named Inventor/Applicant Name:	Donald W. Milbrand
Customer Number:	23628
Filer:	Edmund J. Walsh/Patricia McDonald
Filer Authorized By:	Edmund J. Walsh
Attorney Docket Number:	A0863.70051US04
Receipt Date:	05-JUN-2019
Filing Date:	09-MAR-2016
Time Stamp:	19:26:30
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$1000
RAM confirmation Number	060619INTEFSW19265700
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	A086370051US04-TRN-EJW.pdf	25998 1610338d8418eff3cf6c0b2664970c0df682db9f	no	1
Warnings:					
Information:					
2	Issue Fee Payment (PTO-85B)	A086370051US04-ISSFEE-EJW.pdf	39887 2bb82b81cb3b001a27045355d513b79a84f457e1	no	1
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	30642 ce493ac42151efab010b0961ccac1f9707c5688a	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	96527		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/065,683	03/09/2016	Donald W. Milbrand JR.	A0863.70051US04	5112

23628 7590 07/02/2019

WOLF GREENFIELD & SACKS, P.C.
600 ATLANTIC AVENUE
BOSTON, MA 02210-2206

EXAMINER
FIGUEROA, FELIX O

ART UNIT	PAPER NUMBER
2833	

NOTIFICATION DATE	DELIVERY MODE
07/02/2019	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

Patents_eOfficeAction@WolfGreenfield.com
WGS_eOfficeAction@WolfGreenfield.com

UNITED STATES DEPARTMENT OF COMMERCE
U.S. Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450

APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR/ PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.
15/065,683	03/09/2016	Milbrand et al.	A0863.70051US04

WOLF GREENFIELD & SACKS, P.C.
600 ATLANTIC AVENUE
BOSTON, MA 02210-2206

EXAMINER	
FELIX O FIGUEROA	
ART UNIT	PAPER
2833	20190617

DATE MAILED: _____

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner for Patents

The IDSs of 3/20/16, 11/6/17, 4/5/18, and 4/4/19 have been considered.

/FELIX O FIGUEROA/
Primary Examiner, Art Unit 2833

PTO-90C (Rev.04-03)

DOCKET NO.: A0863.70051US04

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor:	Donald W. Milbrand, Jr.
Application No.:	15/065,683
Confirmation No.:	5112
Filed:	March 9, 2016
For:	HIGH PERFORMANCE CABLE CONNECTOR
Examiner:	F. O. Figueroa
Art Unit:	2833

Certificate of Electronic Filing under 37 CFR §1.8
I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being transmitted via the Office's electronic filing system in accordance with 37 CFR § 1.6(a)(4).

Dated: April 5, 2018 Electronic Signature for : /Eileen M. MacKenzie/

MAIL STOP RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

STATEMENT FILED PURSUANT TO THE DUTY OF DISCLOSURE UNDER 37 C.F.R. §§ 1.56, 1.97 AND 1.98

Sir:

Pursuant to the duty of disclosure under 37 C.F.R. §§ 1.56, 1.97 and 1.98, the undersigned requests consideration of this Information Disclosure Statement.

PART I: Compliance with 37 C.F.R. § 1.97

This Information Disclosure Statement has been filed before the mailing of a first Office Action after the filing of a Request for Continued Examination under 37 C.F.R. § 1.114.

No fee or certification is required.

PART II: Information Cited

The undersigned hereby makes of record in the above-identified application the information listed on the attached form PTO-1449 (modified PTO/SB/08). The order of presentation of the references should not be construed as an indication of the importance of the references.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /F.O.F/

The undersigned hereby makes the following additional information of record in the above-identified application.

The undersigned would like to bring to the Examiner's attention the following co-pending applications that may contain subject matter related to this application:

Serial No.	Filing Date	Inventor(s)	Docket No.
*15/823,494	11-27-2017	Cohen	A0863.70063US03
*15/713,887	09-25-2017	Cartier et al.	A0863.70078US04

*A copy of this reference is not provided as the Office has waived the requirement under 37 C.F.R. § 1.98(a)(2)(iii) for submitting a copy of a cited U.S. patent application if it is scanned to the Image File Wrapper system and is available on Private PAIR .

The above-identified co-pending applications may include subject matter that is technically-related to subject matter of the present application and may contain claims that recite elements similar to those recited in claims of the present application. In handling prosecution of the above-identified applications, the Examiners for these other applications presumably will search for relevant prior art and, in some circumstances, may take positions about the prior art and/or the interpretation of the claims that may be material to the examination of the present application.

Accordingly, the Examiner in the present application is requested to review the file histories of the above-identified co-pending applications to see whether there is any information that the Examiner believes may be relevant to the prosecution of the present application. It is assumed that the Examiner has access to the file histories of the above-identified applications. However, if the Examiner would like copies of any or all of the information included in the file histories of the above-identified applications, the Examiner is asked to contact the undersigned representative.

The undersigned would like to bring to the Examiner's attention the enclosed search report or other communication from a corresponding or related International or Foreign National Application:

Serial No.	Date of Mailing	Type(s) of Communication	Docket No.
PCT/US2017/0478905	**12-04-2017**	**International Search Report and Written Opinion**	**A0863.70102WO00**

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /F.O.F/

PART III: Remarks

Documents cited anywhere in the Information Disclosure Statement are enclosed unless otherwise indicated. It is respectfully requested that:

1. The Examiner consider completely the cited information, along with any other information, in reaching a determination concerning the patentability of the present claims;

2. The enclosed form PTO-1449 (modified PTO/SB/08) be signed by the Examiner to evidence that the cited information has been fully considered by the United States Patent and Trademark Office during the examination of this application;

3. The citations for the information be printed on any patent which issues from this application.

By submitting this Information Disclosure Statement, the undersigned makes no representation that a search has been performed, of the extent of any search performed, or that more relevant information does not exist.

By submitting this Information Disclosure Statement, the undersigned makes no representation that the information cited in the Statement is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b).

By submitting this Information Disclosure Statement, the undersigned makes no representation that the information cited in the Statement is, or is considered to be, in fact, prior art as defined by 35 U.S.C. § 102.

Notwithstanding any statements by the undersigned, the Examiner is urged to form his or her own conclusion regarding the relevance of the cited information.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /F.O.F/

An early and favorable action is hereby requested.

The Director is hereby authorized to charge any deficiency or credit any overpayment in the fees occasioned by the filing of this Information Disclosure Statement to our Deposit Account No. 23/2825 under Docket No. A0863.70051US04 from which the undersigned is authorized to draw.

Respectfully submitted,

By: /Marcus E. Browne/
Marcus E. Browne, Reg. No. 71,897
Wolf, Greenfield & Sacks, P.C.
600 Atlantic Avenue
Boston, Massachusetts 02210-2206
Telephone: (617) 646-8000

Docket No.: A0863.70051US04
Date: April 5, 2018

/FELIX O FIGUEROA/ 06/17/2019

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /F.O.F/

DOCKET NO.: A0863.70051US04

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor:	Donald W. Milbrand, Jr.
Application No.:	15/065,683
Confirmation No.:	5112
Filed:	March 9, 2016
For:	HIGH PERFORMANCE CABLE CONNECTOR
Examiner:	F. O. Figueroa
Art Unit:	2833

Certificate of Electronic Filing under 37 C.F.R. § 1.8
I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being transmitted via the Office's electronic filing system in accordance with 37 C.F.R. § 1.6(a)(4).

Dated: April 4, 2019 Electronic Signature for: /Trish McDonald/

MAIL STOP RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

STATEMENT FILED PURSUANT TO THE DUTY OF DISCLOSURE UNDER 37 C.F.R. §§ 1.56, 1.97 AND 1.98

Sir:

Pursuant to the duty of disclosure under 37 C.F.R. §§ 1.56, 1.97 and 1.98, the undersigned requests consideration of this Information Disclosure Statement.

PART I: Compliance with 37 C.F.R. § 1.97

This Information Disclosure Statement has been filed before the mailing of a first Office Action after the filing of a Request for Continued Examination under 37 C.F.R. § 1.114.

No fee or certification is required.

PART II: Information Cited

The undersigned hereby makes of record in the above-identified application the information listed on the attached form PTO-1449 (modified PTO/SB/08). The order of presentation of the references should not be construed as an indication of the importance of the references.

7061175.1

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /F.O.F/

The undersigned hereby makes the following additional information of record in the above-identified application.

The undersigned would like to bring to the Examiner's attention the following co-pending applications that may contain subject matter related to this application:

Serial No.	Filing Date	Inventor(s)	Docket No.
*15/683,199	08-22-2017	Kirk et al.	A0863.70102US01
*15/742,244	01-05-2018	Sasame et al.	A1156.70241US00

*A copy of this reference is not provided as the Office has waived the requirement under 37 C.F.R. § 1.98(a)(2)(iii) for submitting a copy of a cited U.S. patent application if it is scanned to the Image File Wrapper system and is available on Private PAIR .

The above-identified co-pending applications may include subject matter that is technically-related to subject matter of the present application and may contain claims that recite elements similar to those recited in claims of the present application. In handling prosecution of the above-identified applications, the Examiners for these other applications presumably will search for relevant prior art and, in some circumstances, may take positions about the prior art and/or the interpretation of the claims that may be material to the examination of the present application.

Accordingly, the Examiner in the present application is requested to review the file histories of the above-identified co-pending applications to see whether there is any information that the Examiner believes may be relevant to the prosecution of the present application. It is assumed that the Examiner has access to the file histories of the above-identified applications. However, if the Examiner would like copies of any or all of the information included in the file histories of the above-identified applications, the Examiner is asked to contact the undersigned representative.

PART III: Remarks

Documents cited anywhere in the Information Disclosure Statement are enclosed unless otherwise indicated. It is respectfully requested that:

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /F.O.F/

1. The Examiner consider completely the cited information, along with any other information, in reaching a determination concerning the patentability of the present claims;

2. The enclosed form PTO-1449 (modified PTO/SB/08) be signed by the Examiner to evidence that the cited information has been fully considered by the United States Patent and Trademark Office during the examination of this application;

3. The citations for the information be printed on any patent which issues from this application.

By submitting this Information Disclosure Statement, the undersigned makes no representation that a search has been performed, of the extent of any search performed, or that more relevant information does not exist.

By submitting this Information Disclosure Statement, the undersigned makes no representation that the information cited in the Statement is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b).

By submitting this Information Disclosure Statement, the undersigned makes no representation that the information cited in the Statement is, or is considered to be, in fact, prior art as defined by 35 U.S.C. § 102.

Notwithstanding any statements by the undersigned, the Examiner is urged to form his or her own conclusion regarding the relevance of the cited information.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /F.O.F/

An early and favorable action is hereby requested.

The Director is hereby authorized to charge any deficiency or credit any overpayment in the fees occasioned by the filing of this Information Disclosure Statement to our Deposit Account No. 23/2825 under Docket No. A0863.70051US04 from which the undersigned is authorized to draw.

Respectfully submitted,

By: /Edmund J. Walsh/
Edmund J. Walsh, Reg. No. 32,950
Wolf, Greenfield & Sacks, P.C.
600 Atlantic Avenue
Boston, Massachusetts 02210-2206
Telephone: (617) 646-8000

Docket No.: A0863.70051US04
Date: April 4, 2019

/FELIX O FIGUEROA/ 06/27/2019

7061175.1

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /F.O.F/

FORM PTO-1449/A and B (modified PTO/SB/08)	APPLICATION NO.: 15/065,683	ATTY. DOCKET NO.: A0863.70051US04
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	FILING DATE: March 9, 2016	CONFIRMATION NO.: 5112
	FIRST NAMED INVENTOR: Donald W. Milbrand, Jr.	
Sheet 1 of 2	GROUP ART UNIT: 2833	EXAMINER: F. O. Figueroa

U.S. PATENT DOCUMENTS

Examiner's Initials #	Cite No.	U.S. Patent Document Number	Kind Code	Name of Patentee or Applicant of Cited Document	Date of Publication or Issue of Cited Document MM-DD-YYYY
		5,176,538	A	Hansell III et al.	01-05-1993
		5,334,050	A	Andrews	08-02-1994
		6,409,543	B1	Astbury, Jr. et al.	06-25-2002
		10,243,304		Kirk et al.	03-26-2019
		2004-0005815	A1	Mizumura et al.	01-08-2004
		2005-0233610	A1	Tutt et al.	10-20-2005
		2006-0255876	A1	Kushta et al.	11-16-2006
		2009-0305533	A1	Feldman et al.	12-10-2009
		2018-0062323	A1	Kirk et al.	03-01-2018
		2018-0145438	A1	Cohen	05-24-2018
		2018-0219331	A1	Cartier et al.	08-02-2018

FOREIGN PATENT DOCUMENTS

Examiner's Initials #	Cite No.	Foreign Patent Document Office/ Country	Number	Kind Code	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Translation (Y/N)
		CN	1179448	C	Whitaker Corp	12-08-2004	Y
		CN	1799290	A	Nippon Electric Co	07-05-2006	Y
		CN	101120490	B	Amphenol Corp	11-17-2010	Y
		CN	101176389	A	Teradyne Inc	05-07-2008	Y
		CN	101600293	A	Hongfujin Prec Ind Shenzhen	12-09-2009	Y
		CN	101600293	B	Hongfujin Prec Ind Shenzhen	05-16-2012	Y
		CN	201846527	U	Molex Inc	05-25-2011	Y
		DE	60216728	T2	Amphenol Corp	11-08-2007	Y-abstract only; see also US6409543
		EP	1018784	A1	Fci S Hertogenbosch Bv	07-12-2000	
		JP	2001-510627	A		07-31-2001	Y-abstract only; see also WO9835409
		MX	9907324	A	Teradyne, Inc.	08-01-2000	Y-abstract only
		WO	98/35409	A1	Teradyne, Inc	08-13-1998	

EXAMINER:	DATE CONSIDERED:
/FELIX O FIGUEROA/	05/24/2019

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

7061174.1

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /F.O.F/

FORM PTO-1449/A and B (modified PTO/SB/08)				APPLICATION NO.: 15/065,683	ATTY. DOCKET NO.: A0863.70051US04
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				FILING DATE: March 9, 2016	CONFIRMATION NO.: 5112
				FIRST NAMED INVENTOR: Donald W. Milbrand, Jr.	
Sheet	2	of	2	GROUP ART UNIT: 2833	EXAMINER: F. O. Figueroa

OTHER ART -- NON PATENT LITERATURE DOCUMENTS

Examiner's Initials #	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	Translation (Y/N)

[NOTE – No copies of U.S. patents, published U.S. patent applications, or pending, unpublished patent applications stored in the USPTO's Image File Wrapper (IFW) system, are included. See 37 CFR § 1.98 and 1287OG163. Copies of all other patent(s), publication(s), unpublished, pending U.S. patent applications, or other information listed are provided as required by 37 CFR § 1.98 unless 1) such copies were provided in an IDS in an earlier application that complies with 37 CFR § 1.98, and 2) the earlier application is relied upon for an earlier filing date under 35 U.S.C. § 120.]

EXAMINER:	DATE CONSIDERED:
/FELIX O FIGUEROA/	06/17/2019

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

7061174.1

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /F.O.F/

DOCKET NO.: A0863.70051US04

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor:	Donald W. Milbrand
Application No.:	15/065,683
Confirmation No.:	5112
Filed:	March 09, 2016
For:	HIGH PERFORMANCE CABLE CONNECTOR
Examiner:	Felix O. Figueroa
Art Unit:	2833

CERTIFICATE OF ELECTRONIC FILING UNDER 37 C.F.R. § 1.8

The undersigned hereby certifies that this paper, along with any paper referred to as being attached or enclosed, is being transmitted via the Office electronic filing system in accordance with § 1.6(a)(4), on the 6th day of November, 2017.

Electronic Signature: /Trish McDonald/

MAIL STOP AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

STATEMENT FILED PURSUANT TO THE DUTY OF DISCLOSURE UNDER 37 C.F.R. §§ 1.56, 1.97 AND 1.98

Sir:

Pursuant to the duty of disclosure under 37 C.F.R. §§ 1.56, 1.97 and 1.98, the undersigned requests consideration of this Information Disclosure Statement.

PART I: Compliance with 37 C.F.R. § 1.97

This Information Disclosure Statement has been filed more than three months after the filing date of this application and after the mailing date of a first Office Action, but before the mailing date of any of a Final Action under 37 C.F.R. § 1.113, a Notice of Allowance under 37 C.F.R. § 1.311, or an action that otherwise closes prosecution in this application.

Please charge our Credit Card in the amount of $180.00 covering the fee set forth in 37 C.F.R. § 1.17(p).

5750185.1 ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /F.O.F/

PART II: Information Cited

The undersigned hereby makes of record in the above-identified application the information listed on the attached form PTO-1449 (modified PTO/SB/08). The order of presentation of the references should not be construed as an indication of the importance of the references.

The undersigned hereby makes the following additional information of record in the above-identified application.

The undersigned would like to bring to the Examiner's attention the following applications that may contain subject matter related to this application:

Serial No.	Filing Date	Inventor(s)	Docket No.
*15/645,931	07-10-2017	Atkinson et al.	A0863.70041US05

*A copy of this reference is not provided as the Office has waived the requirement under 37 C.F.R. § 1.98(a)(2)(iii) for submitting a copy of a cited U.S. patent application if it is scanned to the Image File Wrapper system and is available on Private PAIR.

The above-identified application may include subject matter that is technically-related to subject matter of the present application and may contain claims that recite elements similar to those recited in claims of the present application. In handling prosecution of the above-identified application, the Examiner for this other application presumably will search for relevant prior art and, in some circumstances, may take positions about the prior art and/or the interpretation of the claims that may be material to the examination of the present application.

Accordingly, the Examiner in the present application is requested to review the file history of the above-identified co-pending application to see whether there is any information that the Examiner believes may be relevant to the prosecution of the present application. It is assumed that the Examiner has access to the file history of the above-identified application. However, if the Examiner would like copies of any or all of the information included in the file history of the above-identified application, the Examiner is asked to contact the undersigned representative.

5750185.1 ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /F.O.F/

PART III: Remarks

Documents cited anywhere in the Information Disclosure Statement are enclosed unless otherwise indicated. It is respectfully requested that:

1. The Examiner consider completely the cited information, along with any other information, in reaching a determination concerning the patentability of the present claims;

2. The enclosed form PTO-1449 (modified PTO/SB/08) be signed by the Examiner to evidence that the cited information has been fully considered by the United States Patent and Trademark Office during the examination of this application;

3. The citations for the information be printed on any patent which issues from this application.

By submitting this Information Disclosure Statement, the undersigned makes no representation that a search has been performed, of the extent of any search performed, or that more relevant information does not exist.

By submitting this Information Disclosure Statement, the undersigned makes no representation that the information cited in the Statement is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b).

By submitting this Information Disclosure Statement, the undersigned makes no representation that the information cited in the Statement is, or is considered to be, in fact, prior art as defined by 35 U.S.C. § 102.

Notwithstanding any statements by the undersigned, the Examiner is urged to form his or her own conclusion regarding the relevance of the cited information.

5750185.1 ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /F.O.F/

An early and favorable action is hereby requested.

The Director is hereby authorized to charge any deficiency or credit any overpayment in the fees occasioned by the filing of this Information Disclosure Statement to our Deposit Account No. 23/2825 under Docket No. A0863.70051US04 from which the undersigned is authorized to draw.

Respectfully submitted,

By: /Marcus E. Browne/
Marcus E. Browne, Reg. No. 71,897
Wolf, Greenfield & Sacks, P.C.
600 Atlantic Avenue
Boston, Massachusetts 02210-2206
Telephone: (617) 646-8000

Docket No.: A0863.70051US04
Date: November 6, 2017
xNDDx

/FELIX O FIGUEROA/ 06/17/2019

5750185.1 ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /F.O.F/

DOCKET NO.: A0863.70051US04

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor:	Donald W. Milbrand, Jr.
Application No.:	15/065,683
Confirmation No.:	5112
Filed:	March 9, 2016
For:	HIGH PERFORMANCE CABLE CONNECTOR
Examiner:	Not Yet Assigned
Art Unit:	2833

CERTIFICATE OF ELECTRONIC FILING UNDER 37 C.F.R. § 1.8

The undersigned hereby certifies that this paper, along with any paper referred to as being attached or enclosed, is being transmitted via the Office electronic filing system in accordance with § 1.6(a)(4), on the 20th day of March, 2016.

/Yehoshua E. Zehavi/
Yehoshua E. Zehavi

MAIL STOP AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

STATEMENT FILED PURSUANT TO THE DUTY OF DISCLOSURE UNDER 37 C.F.R. §§ 1.56, 1.97 AND 1.98

Sir:

Pursuant to the duty of disclosure under 37 C.F.R. §§ 1.56, 1.97 and 1.98, the undersigned requests consideration of this Information Disclosure Statement.

PART I: Compliance with 37 C.F.R. § 1.97

This Information Disclosure Statement has been filed within three months of the filing date of a national application other than a continued prosecution application under 37 C.F.R. § 1.53(d).

No fee or certification is required.

PART II: Information Cited

The undersigned hereby makes of record in the above-identified application the information listed on the attached form PTO-1449 (modified PTO/SB/08). The order of

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /F.O.F/

presentation of the references should not be construed as an indication of the importance of the references.

The undersigned hereby makes the following additional information of record in the above-identified application.

The undersigned would like to bring to the Examiner's attention the following co-pending applications that may contain subject matter related to this application:

Serial No.	Filing Date	Inventor(s)	Docket No.
*13/752,534	January 29, 2013	Gailus et al.	N/A
*13/775,808	February 25, 2013	Khilchenko et al.	N/A
*14/948,171	November 20, 2015	Atkinson et al.	A0863.70041US04
*13/683,295	November 21, 2012	Milbrand, Jr. et al.	A0863.70051US02
*13/973,921	August 22, 2013	Cohen	A0863.70063US01
*13/930,447	June 28, 2013	Cartier, Jr. et al.	A0863.70065US02
*14/640,114	March 6, 2015	Paniagua	A0863.70066US02
*14/209,240	March 13, 2014	Cartier, Jr. et al.	A0863.70068US01
*14/209,079	March 13, 2014	Cartier, Jr. et al.	A0863.70069US01
*14/603,300	January 22, 2015	Cartier, Jr. et al.	A0863.70078US01
*14/603,294	January 22, 2015	Cartier, Jr. et al.	A0863.70078US02

*A copy of this reference is not provided as the Office has waived the requirement under 37 C.F.R. § 1.98(a)(2)(iii) for submitting a copy of a cited U.S. patent application if it is scanned to the Image File Wrapper system and is available on Private PAIR.

The undersigned would like to bring to the Examiner's attention the enclosed search report or other communication from a corresponding or related International or Foreign National Application:

Serial No.	Date of Mailing	Type(s) of Communication	Docket No.
***EP 11166820.8**	**January 24, 2012**	**Extended European Search Report**	**N/A**

4657264.1

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /F.O.F/

***PCT/US2005/034605**	**January 26, 2006**	**International Search Report and Written Opinion**	**N/A**
***PCT/US2006/025562**	**October 31, 2007**	**International Search Report with Written Opinion**	**N/A**
***PCT/US2010/056482**	**March 14, 2011**	**International Search Report and Written Opinion**	**A0863.70049WO00**
***PCT/US2010/056482**	**May 24, 2012**	**International Preliminary Report on Patentability**	**A0863.70049WO00**
***PCT/US2011/026139**	**November 22, 2011**	**International Search Report and Written Opinion**	**A0863.70055WO00**
***PCT/US2011/026139**	**September 7, 2012**	**International Preliminary Report on Patentability**	**A0863.70055WO00**
***PCT/US2011/034747**	**July 28, 2011**	**International Search Report and Written Opinion**	**N/A**
***PCT/US2012/023689**	**September 12, 2012**	**International Search Report and Written Opinion**	**A0863.70061WO00**
***PCT/US2012/023689**	**August 15, 2013**	**International Preliminary Report on Patentability**	**A0863.70061WO00**
***PCT/US2012/060610**	**March 29, 2013**	**International Search Report and Written Opinion**	**A0863.70066WO00**
PCT/US2015/012463	**May 13, 2015**	**International Search Report and Written Opinion**	**A0863.70078WO00**

*a copy of this reference is not provided as it was previously cited by or submitted to the office in a prior application, Serial No. 13/683,295, filed November 21, 2012, and relied upon for an earlier filing date under 35 U.S.C. 120 (continuation, continuation-in-part, and divisional applications).

PART III: Remarks

Documents cited anywhere in the Information Disclosure Statement are enclosed unless otherwise indicated. It is respectfully requested that:

1. The Examiner consider completely the cited information, along with any other information, in reaching a determination concerning the patentability of the present claims;

2. The enclosed form PTO-1449 (modified PTO/SB/08) be signed by the Examiner to evidence that the cited information has been fully considered by the United States Patent and Trademark Office during the examination of this application;

3. The citations for the information be printed on any patent which issues from this application.

By submitting this Information Disclosure Statement, the undersigned makes no representation that a search has been performed, of the extent of any search performed, or that more relevant information does not exist.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /F.O.F/

By submitting this Information Disclosure Statement, the undersigned makes no representation that the information cited in the Statement is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b).

By submitting this Information Disclosure Statement, the undersigned makes no representation that the information cited in the Statement is, or is considered to be, in fact, prior art as defined by 35 U.S.C. § 102.

Notwithstanding any statements by the undersigned, the Examiner is urged to form his or her own conclusion regarding the relevance of the cited information.

An early and favorable action is hereby requested.

The Director is hereby authorized to charge any deficiency or credit any overpayment in the fees occasioned by the filing of this Information Disclosure Statement to our Deposit Account No. 23/2825 under Docket No. A0863.70051US04 from which the undersigned is authorized to draw.

Respectfully submitted,

By: /Edmund J. Walsh/
Edmund J. Walsh, Reg. No. 32,950
Wolf, Greenfield & Sacks, P.C.
600 Atlantic Avenue
Boston, Massachusetts 02210-2206
Telephone: (617) 646-8000

Docket No.: A0863.70051US04
Date: March 20, 2016
xNDDx

/FELIX O FIGUEROA/

06/17/2019

4657264.1

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /F.O.F/

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/065,683	08/13/2019	10381767	A0863.70051US04	5112

23628 7590 07/24/2019

WOLF GREENFIELD & SACKS, P.C.
600 ATLANTIC AVENUE
BOSTON, MA 02210-2206

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Donald W. Milbrand JR., Bristol, NH;
Amphenol Corporation, Wallingford Center, CT;
Prescott B. Atkinson, Nottingham, NH;
Brian Kirk, Amherst, NH;

PTO/AIA/80 (07-12)
Approved for use through 11/30/2014. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(c).

I hereby appoint:

[X] Practitioners associated with the Customer Number: 27557

OR

[ ] Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

as attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned **only** to the undersigned according to the USPTO assignment records or assignment documents attached to this form in accordance with 37 CFR 3.73(c).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(c) to:

[X] The address associated with Customer Number: 27557

OR

[ ] Firm or Individual Name			
Address			
City		State	Zip
Country			
Telephone		Email	

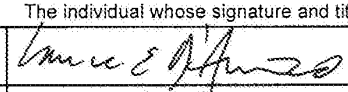
Assignee Name and Address:

Amphenol Corporation
358 Hall Avenue
Wallingford, Connecticut 06492

A copy of this form, together with a statement under 37 CFR 3.73(c) (Form PTO/SB/96 or equivalent) is required to be filed in each application in which this form is used. The statement under 37 CFR 3.73(c) may be completed by one of the practitioners appointed in this form, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature		Date	November 22, 2016
Name	Lance D'Amico, Esq.		
Title	Vice President, Secretary and General Counsel, Amphenol Corporation		

124315.00100/104040417v.1

Electronic Acknowledgement Receipt

EFS ID:	37694923
Application Number:	15065683
International Application Number:	
Confirmation Number:	5112
Title of Invention:	HIGH PERFORMANCE CABLE CONNECTOR
First Named Inventor/Applicant Name:	Donald W. Milbrand
Customer Number:	23628
Filer:	Peter S. Weissman/Keyla Clements
Filer Authorized By:	Peter S. Weissman
Attorney Docket Number:	A0863.70051US04
Receipt Date:	08-NOV-2019
Filing Date:	09-MAR-2016
Time Stamp:	10:54:54
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		12431501013StatementandPOA.pdf	2365529 8ffea40e7e7efc54c3cd0d57d86ad32d6c4a0b94	yes	3

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Assignee showing of ownership per 37 CFR 3.73	1	2
	Power of Attorney	3	3
Warnings:			
Information:			
	Total Files Size (in bytes):	2365529	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/AIA/96 (08-12)
Approved for use through 01/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: Amphenol Corporation

Application No./Patent No.: 10,381,767 Filed/Issue Date: August 13, 2019

Titled: HIGH PERFORMANCE CABLE CONNECTOR

Amphenol Corporation (Name of Assignee) , a Corporation (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. [X] The assignee of the entire right, title, and interest.

2. [ ] An assignee of less than the entire right, title, and interest (check applicable box):

   [ ] The extent (by percentage) of its ownership interest is _____ %). Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

   [ ] There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. [ ] The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. [ ] The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

A. [X] An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 049378 , Frame 0982 , or for which a copy thereof is attached.

B. [ ] A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: _____ To: _____
   The document was recorded in the United States Patent and Trademark Office at
   Reel _____ , Frame _____ , or for which a copy thereof is attached.

2. From: _____ To: _____
   The document was recorded in the United States Patent and Trademark Office at
   Reel _____ , Frame _____ , or for which a copy thereof is attached.

124315.01013/122177436v.1

PTO/AIA/96 (08-12)
Approved for use through 01/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____
The document was recorded in the United States Patent and Trademark Office at
Reel _____ , Frame _____ , or for which a copy thereof is attached.

4. From: _____ To: _____
The document was recorded in the United States Patent and Trademark Office at
Reel _____ , Frame _____ , or for which a copy thereof is attached.

5. From: _____ To: _____
The document was recorded in the United States Patent and Trademark Office at
Reel _____ , Frame _____ , or for which a copy thereof is attached.

6. From: _____ To: _____
The document was recorded in the United States Patent and Trademark Office at
Reel _____ , Frame _____ , or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☒ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Peter S. Weissman/	November 8, 2019
Signature	Date
Peter S. Weissman – Registration No. 40,220	Attorney for Assignee
Printed or Typed Name	Title or Registration Number

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/065,683	03/09/2016	Donald W. Milbrand JR.	A0863.70051US04

CONFIRMATION NO. 5112

23628
WOLF GREENFIELD & SACKS, P.C.
600 ATLANTIC AVENUE
BOSTON, MA 02210-2206

POWER OF ATTORNEY NOTICE

OC000000112564083

Date Mailed: 11/13/2019

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 11/08/2019.

- The Power of Attorney to you in this application has been revoked by the applicant. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/rmohamed/

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/065,683	03/09/2016	Donald W. Milbrand JR.	A0863.70051US04

CONFIRMATION NO. 5112

27557
BLANK ROME LLP
1825 Eye Street NW
WASHINGTON, DC 20006-5403
UNITED STATES OF AMERICA

POA ACCEPTANCE LETTER

OC000000112564137

Date Mailed: 11/13/2019

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 11/08/2019.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/rmohamed/

FEE TRANSMITTAL

Complete if known	
Application Number	Patent #: 10,381,767
Filing Date	Issued: August 13, 2019
First Named Inventor	Donald W. Milbrand, Jr.
Examiner Name	F. O. Figueroa
Art Unit	2833
Practitioner Docket No.	A0863.70051US04

☐ Applicant asserts small entity status. See 37 CFR 1.27.

☐ Applicant certifies micro entity status. See 37 CFR 1.29. Form PTO/SB/15A or B or equivalent must either be enclosed or have been submitted previously.

TOTAL AMOUNT OF PAYMENT ($)2,100.00

METHOD OF PAYMENT (check all that apply)

☐ Check ☒ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☒ Deposit Account Deposit Account Number: 23/2825 Deposit Account Name: Wolf, Greenfield & Sacks, P.C.

For the above-identified deposit account, the Director is hereby authorized to (check all that apply):

☐ Charge fee(s) indicated below

☐ Charge fee(s) indicated below, **except for the filing fee**

☒ Charge any additional fee(s) or underpayment of fee(s) under 37 CFR 1.16 and 1.17, **except for any excess claims fees or multiple dependent claim fee**

☐ Charge any additional fee(s) or underpayment of fee(s) under 37 CFR 1.16 and 1.17

☒ Credit any overpayment of fee(s)

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES (U = undiscounted fee; S = small entity fee; M = micro entity fee)

	FILING FEES			SEARCH FEES			EXAMINATION FEES			
Application Type	**U ($)**	**S ($)**	**M ($)**	**U ($)**	**S ($)**	**M ($)**	**U ($)**	**S ($)**	**M ($)**	**Fees Paid ($)**
Utility	320	160*	80	700	350	175	800	400	200	
Design	220	110	55	160	80	40	640	320	160	
Plant	220	110	55	440	220	110	660	330	165	
Reissue	320	160	80	700	350	175	2,320	1,160	580	
Provisional	300	150	75	0	0	0	0	0	0	

* The $160 small entity status filing fee for a utility application is further reduced to $80 for a small entity status applicant who files the application via EFS-Web.

2. EXCESS CLAIM FEES

Fee Description	**Undiscounted Fee ($)**	**Small Entity Fee ($)**	**Micro Entity Fee ($)**
Each claim over 20 (including Reissues)	100	50	25
Each independent claim over 3 (including Reissues)	480	240	120
Multiple dependent claims	860	430	215

Total Claims		**Extra Claims**		**Fee ($)**		**Fee Paid ($)**	**Multiple Dependent Claims**	
29	- or HP =		x		=		**Fee ($)**	**Fee Paid ($)**

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims		**Extra Claims**		**Fee ($)**		**Fee Paid ($)**
	- or HP =		x		=	

HP = highest number of independent claims paid for, if greater than 3.

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $420 ($210 for small entity) ($105 for micro entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets		**Extra Sheets**		**Number of each additional 50 or fraction thereof**		**Fee ($)**		**Fee Paid ($)**
	- 100 =		/50 =		(round **up** to a whole number) x		=	

4. OTHER FEE(S)

	Fees Paid ($)
Non-English specification, $130 fee (no small or micro entity discount)	
Non-electronic filing fee under 37 CFR 1.16(t) for a utility application, $400 fee ($200 small or micro entity)	
Other (e.g., late filing surcharge): 1453 Petition for revival of an abandoned application ...	2,100.00

SUBMITTED BY

Signature	/Edmund J. Walsh/	Registration No. (Attorney/Agent)	32,950	Telephone	617.646.8000
Name (Print/Type)	Edmund J. Walsh			Date	October 19, 2020

Certificate of Electronic Filing under 37 C.F.R. § 1.8

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being transmitted via the Office's electronic filing system in accordance with 37 C.F.R. § 1.6(a)(4).

Dated: October 19, 2020 Electronic Signature for Jenica L. Roberts: /Jenica L. Roberts/

8621920.1

Electronic Patent Application Fee Transmittal

Application Number:	15065683
Filing Date:	09-Mar-2016
Title of Invention:	HIGH PERFORMANCE CABLE CONNECTOR
First Named Inventor/Applicant Name:	Donald W. Milbrand
Filer:	Edmund J. Walsh/Jenica Roberts
Attorney Docket Number:	A0863.70051US04

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
PET. REVIVE ABANDON APP, DELAY PYMT-RESP	1453	1	2100	2100
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**2100**

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

Decision Date : October 19, 2020

In re Application of :
Donald Milbrand

DECISION ON PETITION

Application No: 15065683

Filed: 09-Mar-2016

Attorney Docket No: A0863.70051US04

This is an electronic decision on the petition, filed October 19, 2020 , which is being treated as a petition under 37 CFR 1.137(a) to revive the instant nonprovisional application for failure to timely notify the U.S. Patent and Trademark Office (USPTO) of the filing of an application in a foreign country, or under a multinational treaty that requires publication of applications eighteen months after filing. See 37 CFR 1.137(f).

The petition is **GRANTED.**

Petitioner states that the present nonprovisional application is the subject of a foreign or international application filed on 11-02-2016
However, the USPTO was unintentionally not notified of this filing within 45 days subsequent to the filing of the subject application in a foreign country.

In view of the above, this application became abandoned pursuant to 35 U.S.C. § 122(b)(2)(B)(iii) and 37 CFR 1.213(c) for failure to timely notify the Office of the filing of an application in a foreign country, or under a multilateral international agreement that requires publication of applications 18 months after filing.

A petition under 37 CFR 1.137(f) must be accompanied by:
(1) the reply which is met by the notification of such filing in a foreign country or under a multinational treaty;
(2) the petition fee as set forth in 37 CFR 1.17(m); and
(3) a statement that the entire delay in filing the required notice of a foreign or international filing from the due date for the required notice until the filing of a grantable petition under 37 CFR 1.137(a) was unintentional.

The instant petition has been found to be in compliance with 37 CFR 1.137(a) Accordingly, the failure to timely notify the USPTO of a foreign or international filing within 45 days after the date of filing of such foreign or international application as provided by 35 U.S.C. § 122(b)(2)(B)(iii) and 37 CFR 1.213(c) is accepted as having been unintentionally delayed.

The previous Request and Certification under 35 U.S.C. § 122(b)(2)(B)(i) has been rescinded. A Notice Regarding Rescission of Nonpublication Request which sets forth the projected publication date will be viewable in Private PAIR within one (1) business day.

It is not apparent whether the person signing the statement of unintentional delay was in a position to have firsthand or direct knowledge of the facts and circumstances of the delay at issue. Nevertheless, such statement is being treated as having been made as the result of a reaso nable inquiry into the facts and circumstances of such delay. See 37 CFR 10.18(b) and Changes to Patent Practice and Procedure; Final Rule Notice, 62 Fed. Reg. 53131, 53178 (October 10, 1997), 1203 Off. Gaz. Pat. Office 63, 103 (October 21, 1997). In the event that such an inquiry has not been made, petitioner must make such an inquiry. If such inquiry results in the discovery that it is not correct that the entire delay in filing the required reply from the due date for the reply until the filing of a grantable petition pursuant to 37 CFR 1.137(a) was unintentional, petitioner must notify the Office.

This application file is being directed to the Office of Data Management.

Telephone inquiries concerning this decision should be directed to the Patent Electronic Business Center (EBC) at 866-217-9197.

Office of Petitions

Electronic Acknowledgement Receipt	
EFS ID:	40876476
Application Number:	15065683
International Application Number:	
Confirmation Number:	5112
Title of Invention:	HIGH PERFORMANCE CABLE CONNECTOR
First Named Inventor/Applicant Name:	Donald W. Milbrand
Customer Number:	27557
Filer:	Edmund J. Walsh/Jenica Roberts
Filer Authorized By:	Edmund J. Walsh
Attorney Docket Number:	A0863.70051US04
Receipt Date:	19-OCT-2020
Filing Date:	09-MAR-2016
Time Stamp:	12:17:39
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
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Payment was successfully received in RAM	$2100
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Petition automatically granted by EFS	petition-request.pdf	32626 a61b76c6bac2d12b5482b22af09b0bf645649025	no	2
Warnings:					
Information:					
2	Rescind Nonpublication Request for Pre Grant Pub	A086370051US04-RCNPUB-EJW.pdf	40249 40c60c3a0fa4bfda003920f9634f5c2eaa721c84	no	2
Warnings:					
Information:					
3	Fee Worksheet (SB06)	A086370051US04-FEE-EJW.pdf	32690 dd108a8c5fc40059a4d8770595b18f4026320866	no	1
Warnings:					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	30811 89d32ad49f990423e374cb9351c9139b06d6fd7c	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	136376		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc Code: PET.AUTO Document Description: Petition automatically granted by EFS-Web	PTO/SB/64a U.S. Patent and Trademark Office Department of Commerce

Electronic Petition Request	**PETITION FOR REVIVAL OF AN APPLICATION FOR PATENT ABANDONED FOR FAILURE TO NOTIFY THE OFFICE OF A FOREIGN OR INTERNATIONAL FILING UNDER 37 CFR 1.137(f)**
Application Number	15065683
Filing Date	09-Mar-2016
First Named Inventor	Donald Milbrand
Art Unit	2833
Examiner Name	FELIX FIGUEROA
Attorney Docket Number	A0863.70051US04
Title	HIGH PERFORMANCE CABLE CONNECTOR

The above-identified application became abandoned pursuant to 35 U.S.C. 122(b)(2)(B)(iii) for failure to timely notify the Office of the filing of an application in a foreign country or under a multinational treaty that requires publication of applications eighteen months after filing. The date of abandonment is the day after the expiration date of the forty-five (45) day period set in 35 U.S.C. 122(b)(2)(B)(iii).

PURSUANT TO 37 CFR 1.137(f), APPLICANT HEREBY PETITIONS FOR REVIVAL OF THIS APPLICATION UNDER 37 CFR 1.137(a).

A grantable petition requires the following items:
(1) Petition fee;
(2) Reply;
(3) Statement that the entire delay was unintentional.

Petition Fee

- ○ Small Entity
- ○ Micro Entity
- ◉ Regular Undiscounted

Notice of Foreign or International Filing (35 U.S.C. 122(b)(2)(B)(iii) and 37 CFR 1.213(c))

☒ Subsequent to the filing of the above-identified application, an application was filed in another country, or under a multinational international treaty (e.g., filed under the Patent Cooperation Treaty), that requries publication of applications eighteen months after the filing. The filing date of the subsequently filed foreign or international application is 11-02-2016

☒ The non-publication request has been filed on 09-Mar-2016

☒ STATEMENT: The entire delay in filing the required notice of a foreign or international filing from the due date for the required notice until the filing of a grantable petition under 37 CFR 1.137(a) was unintentional.

THIS PORTION MUST BE COMPLETED BY THE SIGNATORY OR SIGNATORIES

I certify, in accordance with 37 CFR 1.4(d)(4) that I am:

- ○ An attorney or agent registered to practice before the Patent and Trademark Office who has been given power of attorney in this application.
- ◉ An attorney or agent registered to practice before the Patent and Trademark Office, acting in a representative capacity.
- ○ A sole inventor
- ○ A joint inventor; I certify that I am authorized to sign this submission on behalf of all of the inventors as evidenced by the power of attorney in the application
- ○ A joint inventor; all of whom are signing this e-petition.

Signature	/Edmund J Walsh/
Name	Edmund J Walsh
Registration Number	32950

PTO/SB/36 (07-09)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U. S. DEPARTMENT OF COMMERCE

RESCISSION OF PREVIOUS NONPUBLICATION REQUEST
(35 U.S.C. 122(b)(2)(B)(ii))
AND, IF APPLICABLE,
NOTICE OF FOREIGN FILING
(35 U.S.C. 122(b)(2)(B)(iii))

Send completed form to:
Mail Stop PG Pub
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
FAX: (571) 273-8300

Application Number	15/065,683-Conf. #5112
Filing Date	March 9, 2016
First Named Inventor	Donald W. Milbrand, Jr.
Title	HIGH PERFORMANCE CABLE CONNECTOR
Atty Docket Number	A0863.70051US04
Art Unit	2833
Examiner	F. O. Figueroa

A request that the above-identified application not be published under 35 U.S.C. 122(b) (nonpublication request) was included with the above-identified application on filing pursuant to 35 U.S.C. 122(b)(2)(B)(i).
I hereby **rescind** the previous nonpublication request.

If a notice of foreign or international filing is or will be required by 35 U.S.C. 122(b)(2)(B)(iii) and 37 CFR 1.213(c), I hereby provide such notice. This notice is being provided no later than forty-five (**45**) days after the date of such foreign or international filing.

*If a notice of subsequent foreign or international filing required by 35 U.S.C. 122(b)(2)(B)(iii) and 37 CFR 1.213(c) was not filed within forty-five (**45**) days after the date of filing of the foreign or international application, the application is ABANDONED, and a petition to revive under 37 CFR 1.137(b) is required. See 37 CFR 1.137(f).*

/Edmund J. Walsh/
Signature

October 19, 2020
Date

Edmund J. Walsh
Typed or printed name

32,950
Registration Number, if applicable

617.646.8000
Telephone Number

This request must be signed in compliance with 37 CFR 1.33(b).

If information or assistance is needed in completing this form, please contact the Pre-Grant Publication Division at (703)605-4283 or by e-mail at PGPub@USPTO.gov.

~~CERTIFICATE OF MAILING OR TRANSMISSION~~

~~I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop PG Pub, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, or facsimile transmitted to the U.S. Patent and Trdemark Office on the date shown below.~~

~~Signature~~

~~Name (Print/Type)~~	~~Date~~	

8622043.1

PTO/SB/92 (07-16)
Approved for use through 11/30/2020. OMB 0561-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Certificate of Mailing or Transmission under 37 CFR 1.8

I hereby certify that this correspondence is being:

1. ☐ Deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to:
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   Commissioner for Patents
   P.O. Box 1450
   Alexandria, VA 22313-1450

   on _____ .
   Date

2. ☐ Facsimile transmitted to the United States Patent and Trademark Office, or

   OR

3. ☒ EFS-Web transmitted to the USPTO.

/Jenica L. Roberts/	October 19, 2020
Signature	Date
Jenica L. Roberts	617.646.8553
Typed or printed name	Telephone number

Note: Each paper must have its own certificate of mailing or transmission, or this certificate must identify each submitted paper:

Rescission of Previous Nonpublication Request (1 page)

8622043.1

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/065,683	03/09/2016	Donald W. Milbrand JR.	A0863.70051US04

CONFIRMATION NO. 5112

27557
BLANK ROME LLP
1825 Eye Street NW
WASHINGTON, DC 20006-5403

NONPUBLICATION RESCISSION LETTER

OC000000120744671

Date Mailed: 10/20/2020

Communication Regarding Rescission Of Nonpublication Request and/or Notice of Foreign Filing

Applicant's rescission of the previously-filed nonpublication request and/or notice of foreign filing is acknowledged. The paper has been reflected in the Patent and Trademark Office's (USPTO's) computer records so that the earliest possible projected publication date can be assigned.

The projected publication date is 01/28/2021.

If applicant rescinded the nonpublication request before or on the date of "foreign filing,"[1] then no notice of foreign filing is required.

If applicant foreign filed the application after filing the above application and before filing the rescission, and the rescission did not also include a notice of foreign filing, then a notice of foreign filing (not merely a rescission) is required to be filed within 45 days of the date of foreign filing. See 35 U.S.C. § 122(b)(2)(B)(iii), and Clarification of the United States Patent and Trademark Office's Interpretation of the Provisions of 35 U.S.C. § 122(b)(2)(B)(ii)-(iv), 1272 Off. Gaz. Pat. Office 22 (July 1, 2003).

If a notice of foreign filing is required and is not filed within 45 days of the date of foreign filing, then the application becomes abandoned pursuant to 35 U.S.C. § 122(b)(2)(B)(iii). In this situation, applicant should either file a petition to revive or notify the Office that the application is abandoned. See 37 CFR 1.137(f). Any such petition to revive will be forwarded to the Office of Petitions for a decision. Note that the filing of the petition will not operate to stay any period of reply that may be running against the application.

Questions regarding petitions to revive should be directed to the Office of Petitions at (571) 272-3282.

[1] Note, for purpose of this notice, that "foreign filing" means "filing an application directed to the same invention in another country, or under a multilateral international agreement, that requires publication of applications 18 months after filing".

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/eefswuser/