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Polysilicon integrated microsystems: technologies and applications

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Abstract

Co-fabrication of polysilicon microstructures with CMOS electronics enables monolithic inertial sensors to be fabricated. Correlations are well established between the deposition, doping, and annealing conditions of LPCVD polysilicon and its mechanical properties, such as residual strain, strain gradient, and Young's modulus. Surface passivations for alleviating stiction have been demonstrated recently that greatly reduce the tendency for polysilicon microstructures to adhere to adjacent surfaces when dried after release by wet etching and rinsing, or when brought into contact due to mechanical shock during use. Sigma–delta control strategies are attractive for linearizing closed-loop sensors and are well suited to implementation in CMOS. Basic design principles for sense elements and electromechanical actuation in a single structural layer of polysilicon have emerged rapidly in the past several years. Monolithic polysilicon integrated sensors for the *X*, *Y*, and *Z* components of linear acceleration, angular rate, and angular acceleration have been demonstrated using the BiMEMS process of Analog Devices, Inc. Mechanical suspensions, electrostatic actuators and capacitive pickoffs, and interface- and control-circuit building blocks are all portable to alternative integrated technologies that share the basic characteristic of thin, laminar suspended microstructures.

Keywords: Integrated microsystems; Polysilicon

1. Introduction

By selectively etching sacrificial layers from a multilayer sandwich of patterned thin films, micromechanical structures can be fabricated using integrated-circuit (IC) equipment and processes. This surface-micromachining process was first used to make air bridges for low-capacitance interconnections in high-frequency ICs. Micromechanical beams were co-fabricated with simple MOSFETs in the resonant-gate transistor in the mid-1960s [1]. In the early 1980s, surface micromachining was applied to make polysilicon microstructures, using an SiO_2 sacrificial layer [2,3]. Due primarily to the difficulty of off-chip detection of the motional current from a vibrating microbridge, a simple process to integrate NMOS electronics with polysilicon microstructures was demonstrated in 1984 [4]. Polysilicon micromechanics was increasingly recognized as a promising technology through the 1980s. A major contributing factor to the growth of polysilicon micromachining was the mature infrastructure for depositing, patterning, and etching thin films that had been established by the IC industry. Polysilicon integrated microsystems are now being successfully commercialized, starting with a 50*g* accelerometer for air-bag deployment introduced in 1993 [5].

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This paper begins by reviewing polysilicon micromachining technology and the approaches to co-fabrication of polysilicon microstructures with CMOS. The control of the mechanical properties of polysilicon has been studied extensively and is relatively well understood. Although the initial commercial integrated technology, Analog Devices' BiMEMS process [5], interleaves micromachining and electronics processing steps, progress has been made recently in modularizing the fabrication sequence. In the second part of the paper, several integrated sensors are described that have recently been demonstrated in BiMEMS, including linear accelerometers, angular accelerometers, vibratory rate gyroscopes, and resonant accelerometers. These initial results establish the feasibility of monolithic multi-sensing ICs that will have many applications in, for example, vehicle control and head-mounted display systems. Furthermore, the microelectromechanical building blocks for the sense elements, such as suspensions and position-sensing capacitors, together with the interface and control circuits, can be captured in CAD models and reused in new designs, in the same way as is done in integrated circuits. At present, there is much room for improving the sophistication and ease of use of CAD for integrated microsystems

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2. Polysilicon micromachining technology

The fabrication sequence of a polysilicon lateral resonator [6,7] is useful to outline the basic process. After describing the basic process modules, we shall summarize recent research in mechanical property control and in the elimination of stiction during the final drying step.

Fig. 1 shows cross sections through the process sequence, starting with the formation of a substrate ground plane using an n^+ diffusion in Fig. 1(a). The wafer is passivated with a layer of 1500 Å thick LPCVD nitride deposited on top of a layer of 0.5 μm thick thermal SiO_2. Contact windows to the substrate ground plane are then opened. Deposition, definition, and patterning of an in situ phosphorus-doped polysilicon interconnection layer follows in Fig. 1(b). This layer serves as a second electrode plane and as the interconnection to the n^+ diffusion and the microstructure.

A 2 μm thick LPCVD sacrificial phosphosilicate glass (PSG) layer is deposited and patterned in two separate masking steps. The first is a timed etch to create dimples, as shown in Fig. 1(c). The second masking step etches through the PSG layer in windows to become the anchors of the polysilicon structure, as shown in Fig. 1(d). The 2 μm thick polysilicon structural layer is then deposited by LPCVD (undoped) at 610 °C in Fig. 1(e). The structural layer is doped by depositing another layer of 0.3 μm thick PSG (Fig. 1(f)) and then annealing at 1050 °C in N_2 for one hour. This step dopes the polysilicon symmetrically by diffusion from the top and the bottom layers of PSG, in order to achieve a uniform grain texture and avoid gradients in the residual stress. The top PSG layer is then stripped and the structural polysilicon is patterned by reactive-ion etching to yield the cross section in Fig. 1(g). Finally, the wafer is immersed in 10:1 diluted HF to etch the sacrificial PSG layer. The wafer is rinsed extensively in deionized water to form a native oxide passivation on the polysilicon. A brief H_2O_2 dip is sufficient to form the hydrophilic native oxide layer. After drying under an IR lamp, the final cross section is as shown in Fig. 1(h).

2.1. Polysilicon mechanical properties

Polysilicon as a mechanical material has been the subject of extensive study since the 1980s [3,8]. Residual stress and its gradient through the thickness of the film are critical con-

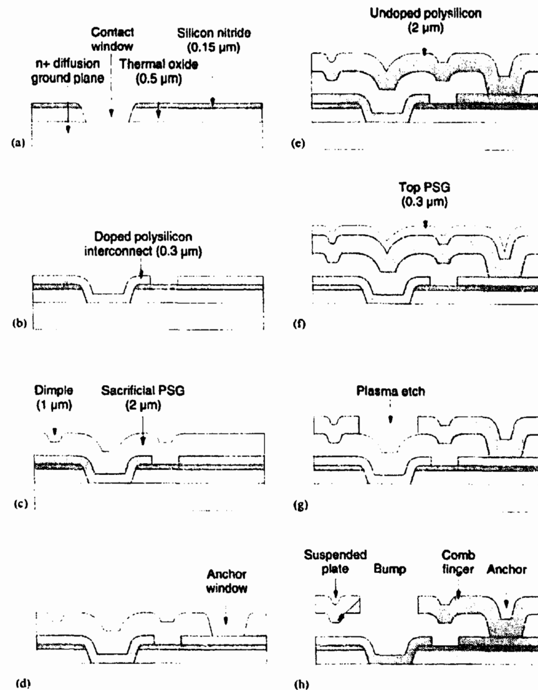

Fig. 1. Polysilicon surface-micromachining process sequence [7] (courtesy of Dr W.C. Tang, Jet Propulsion Laboratory, Pasadena, CA, USA).

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straints on microstructure design. If the average stress is compressive, then microbridges will buckle if longer than a critical length. Stress gradients generate an internal bending moment that causes cantilever beams to warp out-of-plane upon release. The Young's modulus and yield stress vary somewhat with processing, but the range of variation is small, compared with the residual stress.

The basic correlations between residual stress and stress gradient and the texture of undoped and phosphorus-doped polysilicon are now reasonably well understood [9]. From these fundamental studies, several types of polysilicon have been developed. The fine-grained, undoped polysilicon developed at the University of Wisconsin is deposited in a microcrystalline state at 575 °C. A low-temperature anneal results in little grain growth, but the residual strain becomes tensile and is stable for further annealing cycles. Conducting regions are formed by ion implantation into this semi-insulating fine-grained polysilicon [10]. At Berkeley, the focus has been on in situ phosphorus-doped polysilicon with rapid thermal stress annealing, in order to reduce the impact on pre-processed CMOS [11]. By reducing the phosphine flow and using a deposition temperature of 585–590 °C, a higher deposition rate is achieved without much increase in the sheet resistance. Low sheet resistance and uniform doping through the polysilicon are desirable to minimize depletion effects on the linearities of sense and force-feedback capacitors [12]. By using rapid thermal annealing at 950 °C for 7 min, a tensile residual stress of less than 25 MPa with negligible stress gradient through the film thickness can be achieved [11].

The typical widths and thicknesses of LPCVD polysilicon microstructures are both in the range of 1–2 μm. Due to variations in the deposition, lithography, and etching processes, the run-to-run variations in the width and thickness are on the order of 10%, which results in substantial variations in the spring rates, masses, and the resulting resonance frequencies [13], even if the stress and other properties such as Young's modulus were perfectly controlled. In order to achieve a precise resonance frequency, electrical or mechanical post-fabrication trimming is necessary.

It is worth emphasizing that polysilicon is a low-loss, extremely stable mechanical material. Quality factors of 50 000–100 000 are typical of polysilicon microresonators [7,14]. Electrostatically driven polysilicon resonant structures encapsulated in thin-film vacuum chambers have a short-term stability of better than 0.02 Hz, for a resonance frequency of 625 kHz [14]. Operation for over three years with less than 0.4 ppm long-term frequency variation demonstrates conclusively the suitability of polysilicon for precision sensing applications [15].

2.2. Microstructure release and surface passivation

The final step in surface micromachining involves wet etching of the sacrificial oxide in hydrofluoric acid. The basic understanding of this process has improved considerably and models have been developed to predict etching times [16]. Release and drying of the microstructure is a critical step in the process, which may result in stiction of the structure to the substrate after rinsing and drying. Several approaches to stiction-free drying have been demonstrated, including freeze-drying [17], supercritical CO_2 drying [18], and the addition of polymer spacers to allow the final release to be done in an oxygen plasma [19].

Stiction due to contact with adjacent surfaces after release remains a fundamental reliability question for surface-micromachined structures. In order to minimize the work of adhesion, it is desirable to form a hydrophobic surface on the polysilicon. Hydrogen-terminated silicon is extremely hydrophobic [20], as are self-assembled monolayers (SAMs) [21]. Recent results with SAM coatings have demonstrated that 2.15 μm thick polysilicon cantilevers, which are spaced 2 μm from the substrate and up to 1 mm in length, can be released with high yield when the wafer is pulled directly from the final water rinse, as shown in the scanning electron micrograph (SEM) in Fig. 2. When cantilevers are electrostatically deflected into contact with an underlying polysilicon electrode at the same potential, SAM-coated beams are found to have a 50% sticking probability at a length of 950 μm, in comparison with 110 μm for hydrophilic polysilicon. When these results are translated into works of adhesion, the SAM coatings have a work of adhesion of 3 $\mu J\ m^{-2}$ in comparison with 20 $mJ\ m^{-2}$ for polysilicon passivated with a hydrophilic native oxide [21].

The design of the 'back-end' sequence of microstructure release, anti-stiction coating process, drying, dicing and assembly, and, finally, hermetic packaging is highly constrained. For example, an oxygen plasma release [19] will remove organic coatings such as SAM films, with the implication that they must be deposited after microstructure release. Anti-stiction coatings or processes must be able to survive the thermal cycle required by the hermetic packaging process. SAM coatings are stable to at least 400 °C in a

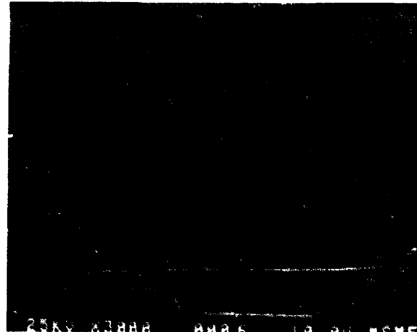

Fig. 2. Tips of SAM-coated polysilicon cantilevers (2.15 μm thick, offset 2.0 μm above the substrate; longest is 1000 μm long) that have been dried by pulling the wafer directly from the water rinse. Note the near-zero gradient in the residual stress for this in situ phosphorus-doped polysilicon film [21].

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nitrogen ambient, but only to around 150 °C in air [21]. Thin-film microshell packaging processes are attractive for simplifying the back-end [10,22]; however, the high deposition temperatures of LPCVD films eliminate most options for reducing the work of adhesion of the encapsulated microstructures. Recently, a process has been developed for wafer-to-wafer transfer of molded-polysilicon caps for vacuum packaging. Hermetic sealing is achieved using a Au–Si eutectic bond at a temperature of 370 °C, which is compatible with SAM coatings [23].

3. Polysilicon integrated microsystems technology

Technologies to co-fabricate polysilicon surface microstructures and CMOS electronics are necessarily complex. In addition to the deposition and patterning steps required by the micromechanical and electronic processes, there are steps inserted to protect one region from damage during processing of the other. As well as considering the thermal cycles and materials compatibility, the typical overall step height of a polysilicon process is 4–5 μm for a single structural layer and 6–7 μm for a double-structural-polysilicon process [24].

An interleaving of microstructure and electronics steps is perhaps the most straightforward approach [4,5]. Most micromachining steps are executed after the completion of the CMOS structures, but prior to metallization with aluminum. The BiMEMS process by Analog Devices integrates both bipolar and MOS transistors along with a single-structural-layer polysilicon microstructure process [5]. An SEM of a BiMEMS accelerometer, the ADXL-05 low-*g* device, is shown in Fig. 3 [25].

In order to avoid threshold voltage shifts, the polysilicon microstructure anneal must be limited to under about 950 °C. The in situ phosphorus-doped polysilicon process discussed earlier [11] is compatible with this temperature ceiling. The contact and metallization steps require modifications due to the rather severe topography created by the thin-film stacks of PSG and structural polysilicon. Photoresist is used to protect the circuit area during the hydrofluoric acid etching of the sacrificial PSG layer [4].

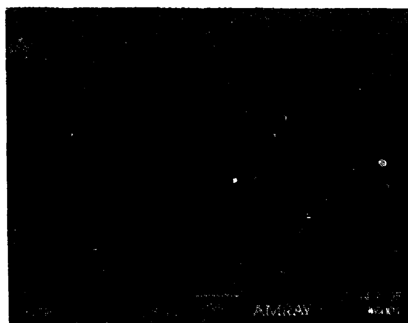

Fig. 3. SEM of the Analog Devices ADXL-05 accelerometer [27]. The structural polysilicon layer is 2 μm thick and suspended 1.6 μm over the substrate. (Courtesy of Dr K.H.-L. Chau, Analog Devices, Inc., Wilmington, MA, USA).

There are several benefits if a modular fabrication process can be designed, in which the micromachining and electronic steps are separated. The MICS process, developed at UC Berkeley in the early 1990s, fabricates a modified p-well CMOS prior to polysilicon micromachining [24,26]. In order to raise the temperature ceiling of the CMOS, tungsten is used instead of aluminum for the metallization. $TiSi_2$/TiN diffusion barriers prevent WSi_2 formation during the subsequent Si_3N_4 deposition at 830 °C and rapid thermal stress-annealing step at 950 °C. Although MICS was used to demonstrate several integrated microsystems, subsequent research at Sandia National Laboratories showed that it is not sufficiently robust for manufacturing [27]. High and variable contact resistance to the p^+ diffusions after the polysilicon microstructure thermal cycles, as well as delamination of tungsten metal lines, remain problems.

Recent work at Sandia National Laboratories has established that a micromechanics-first integrated technology is feasible [28]. The key innovation is to bury the polysilicon microstructures in a well etched into the substrate, after which an overfilled oxide deposition is chemical–mechanical polished (CMP) to planarize the wafer. The schematic cross section of the single-structural-layer process is shown in Fig. 4. Studs of mechanical polysilicon are used to interconnect the CMOS aluminum metallization with the first polysilicon layer in the well (MM Poly 0 in Fig. 4). In this process, the mechanical polysilicon can be annealed at high temperature in order to stabilize its properties against the thermal cycles of the CMOS fabrication steps.

Advanced CMOS processes (e.g., with multiple levels of metallization) can be used without changing the micromechanical process flow. Alternatively, a deeper well would make feasible multiple structural polysilicon layers. If deep reactive ion etching (RIE) patterns are refilled with sacrificial and structural layers, then three-dimensional structures can also be integrated. Using this approach, a 30 μm high molded polysilicon proof mass was embedded in the wafer, prior to conventional surface micromachining [29]. Modularity is therefore very attractive, since it enables separate development paths for the CMOS and polysilicon MEMS, which will be necessary for high-performance integrated microsystems.

Finally, a different approach to polysilicon integrated microsystems is the epi-poly technology [30]. The mechanical material is polysilicon formed in an epitaxial silicon reactor over a patterned layer of SiO_2. Since the deposition temperature is high, the epi-poly film deposits rapidly to a thickness of 10 μm. The CMOS electronics are fabricated in the silicon epitaxial layer surrounding the island of epi-poly. This process has the advantage of providing thick structures with narrow gaps. Since it provides a single structural layer with high-aspect-ratio features, it can be classified with the

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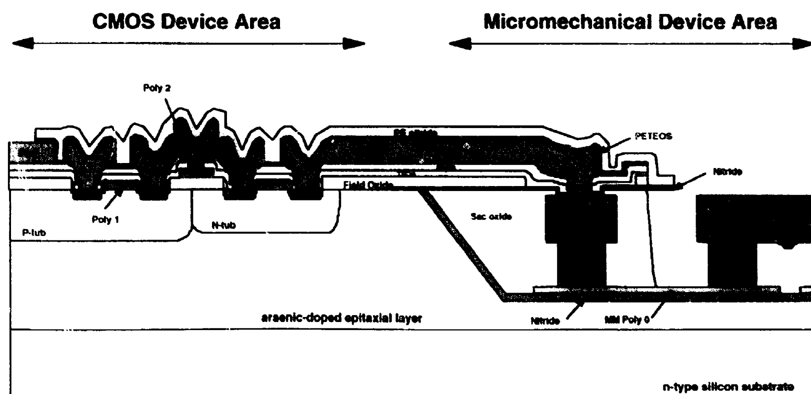

Fig. 4 Cross-sectional schematic of the embedded MEMS integrated technology [28] (courtesy of Dr J.H. Smith, Sandia National Laboratories, Albuquerque, NM, USA).

deep-RIE single-crystal silicon integrated processes to be discussed later.

4. Polysilicon integrated inertial sensors

In a merged surface-micromachined polysilicon microstructure + CMOS process, a variety of MEMS building blocks are available from which to design closed-loop inertial sensors. Interdigitated comb structures are useful for lateral and vertical electrostatic actuation, as well as for position and velocity sensing. The sense capacitances are typically on the order of 100 fF, which requires that great care be taken in designing the front-end amplifier.

Fig. 5 is a die photograph of the second BiMEMS multi-project run, which was completed in June 1995. In this Section, we describe a variety of inertial sensors designed in the Analog Devices BiMEMS technology by our group at Berkeley.

4.1. Linear accelerometers

The initial application of the MICS and BiMEMS technologies was to linear accelerometers [26,31]. With only a single structural layer, it is challenging to design a closed-loop accelerometer that is sensitive to the Z-axis component of acceleration, which is defined to be perpendicular to the surface of the substrate. The interdigitated comb is employed to provide a d.c. levitation force, which is balanced by the downward force supplied by a parallel-plate capacitor formed by the suspended proof mass and an underlying electrode. This sensor architecture was demonstrated in MICS [26] and fully implemented in BiMEMS [32].

The asymmetrical nature of the Z-axis accelerometer makes it essential to use a digital-feedback scheme, since matched differential capacitors are not required in order to linearize the quadratic electrostatic feedback force. Using a sigma–delta controller, a one-bit decision is made every clock cycle on the proof-mass position; the output signal is a serial bit stream at the clock frequency [33]. A simple level-shift circuit translates the bit stream into electrostatic force pulses that balance the suspended proof mass against deflections caused by input accelerations. As the clock frequency is increased, various artifacts of the quantization process are reduced. Digital signal processing is necessary to decimate the oversampled output signal and recover a digital representation of the input acceleration signal.

Lateral components of acceleration, which are in the plane of the substrate, can be detected using a suspended structure incorporating differential interdigitated sense and feedback combs such as the ADXL-05 shown in Fig. 3. The electrostatic force can be linearized using analog techniques in this case, since the differential capacitor is well matched. However, the sigma–delta feedback loop is still attractive, since it does not require precision analog signal processing and is suitable for implementation in digital CMOS. In addition, the sampled nature of the position measurement makes it amenable to canceling drift in the electronic circuit by subtracting the initial offset and errors due to charge injection.

Fig. 6 is a die photograph of a fully differential lateral accelerometer using sigma–delta control of the proof-mass position [34,35]. The capacitive sensing on this accelerometer is done by applying a pulse waveform to the sense element and detecting the charge imbalance in a common-centroid layout of differential capacitors, which is opposite to the method used in the ADXL-50 [31] and ADXL-05 [25]. As a result, the sense amplifier is fully differential, which helps to eliminate offsets.

For a sampling frequency of 500 kHz and a resonance frequency of 8 kHz, the sensor achieves a noise floor of 500

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