

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,

Petitioner,

v.

VERVAIN, LLC,

Patent Owner.

Case No.: IPR2021-01550

U.S. Patent No. 10,950,300

Original Issue Date: March 16, 2021

Title: LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM

**PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 10,950,300
PURSUANT TO 35 U.S.C. §§ 311-319 and 37 C.F.R. § 42**

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1.	Claim 1	32
a.	[1.PRE] “A system for storing data comprising:”	32
b.	[1.A.1] “memory space containing volatile memory space and nonvolatile memory space;”	33
c.	[1.A.2] “wherein the nonvolatile memory space includes both multilevel cell (MLC) memory space and single level cell (SLC) memory space;”	37
d.	[1.B] “at least one controller to operate memory elements and associated memory space;”.....	38
e.	[1.C] “at least one MLC nonvolatile memory element that can be mapped into the MLC memory space;”	40
f.	[1.D] “at least one SLC nonvolatile memory element that can be mapped into the SLC memory space;”	41

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g. [1.E] “at least one random access volatile memory;” 42

h. [1.F] “an FTL flash translation layer, wherein the at least one controller, or FTL, or a combination of both maintain an address table in one or more of the memory elements and random access volatile memory” 42

i. [1.G.1] “the controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory for storage of data therein” 46

j. [1.G.2] “the controller, in at least a Write access operation to the MLC nonvolatile memory element, operable to store data in the MLC nonvolatile memory element and retain such stored data in the random access volatile memory;” 47

k. [1.H] “the controller performing a data integrity test on stored data in the MLC nonvolatile memory element after at least a Write access operation performed thereon by comparing the stored data to the retained data in the random access volatile memory;” 48

l. [1.I] “wherein the address table maps logical and physical addresses adaptable to the system, wherein the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories; and” 50

m. [1.J] “wherein a failure of the data integrity test performed by the controller results in a remapping of the address space to a different physical range of addresses and transfer of data corresponding to the stored data to those remapped physical addresses from those determined to have failed the data integrity test to achieve enhanced endurance.” 52

2.	Claim 2: “The system of claim 1, wherein the FTL flash translation layer is a software module, or a firmware module containing software updates.”	54
3.	Claim 3: “The system of claim 1, wherein at least one of the random access volatile memory or the MLC and SLC nonvolatile memory elements are embedded in the at least one controller.”	54
4.	Claim 4: “The system of claim 1, wherein the MLC and SLC nonvolatile memory elements comprise flash memory.”	55
5.	Claim 5: “The system of claim 1, wherein the random access volatile memory is dynamic random access memory.”	55
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7.	Claim 7: “The system of claim 1, wherein the controller, upon detection of a failure of the data integrity test, remaps the data to the SLC nonvolatile memory element.”	57
8.	Claim 8: “The system of claim 7, wherein the SLC memory element has a higher endurance than the MLC memory element.”	57
9.	Claim 9: “The system of claim 1, wherein the MLC is a multilevel cell, wherein the multilevel cell stores at least 2 bits per cell.”	58
10.	Claim 11: “The system of claim 1 wherein the MLC allows a single cell to store multiple bits.”	58
11.	Claim 12:	58
	a. [12.PRE] “A system for storing data comprising:”	58
	b. [12.A] “memory space containing volatile memory space and nonvolatile memory space, wherein the nonvolatile memory space includes both multilevel cell (MLC) space and single level cell (SLC) space;”	59

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