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**Friedman et al.**

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(54) **WRITE-MANY MEMORY DEVICE AND METHOD FOR LIMITING A NUMBER OF WRITES TO THE WRITE-MANY MEMORY DEVICE**

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(73) Assignee: **Matrix Semiconductor, Inc.**, Santa Clara, CA (US)

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(\* ) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 342 days.

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*Primary Examiner*—Kevin L. Ellis

(22) Filed: **Oct. 5, 2001**

(74) *Attorney, Agent, or Firm*—Brinks Hofer Gilson & Lione

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(57) **ABSTRACT**

(51) **Int. Cl.**  
**G06F 12/14** (2006.01)

The preferred embodiments described herein provide a write-many memory device and method for limiting a number of writes to the write-many memory device. In one preferred embodiment, a write-many memory device is provided comprising a plurality of blocks of memory, each block being limited to N number of writes. Data can be stored in a block of memory only if there has been fewer than N number of writes to the block. In another preferred embodiment, a write-many memory device is provided comprising a plurality of blocks of memory, wherein each block comprises a first sideband field storing data indicating whether the block is free and a second sideband field storing data indicating how many times the block has been written into. The first and second sideband fields are used in a method for limiting a number of writes to the write-many memory device. Other preferred embodiments are provided, and each of the preferred embodiments can be used alone or in combination with one another.

(52) **U.S. Cl.** ..... **711/103**  
(58) **Field of Classification Search** ..... **711/103,**  
**711/154, 163**

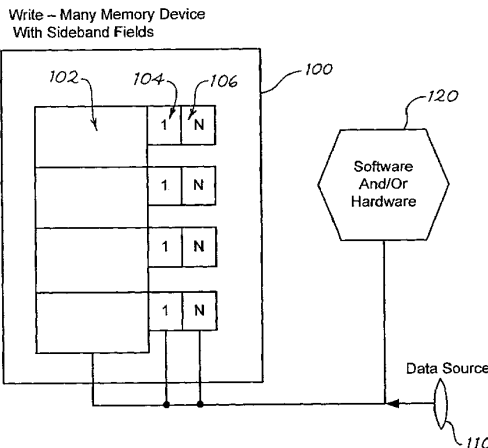
See application file for complete search history.

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**45 Claims, 3 Drawing Sheets**



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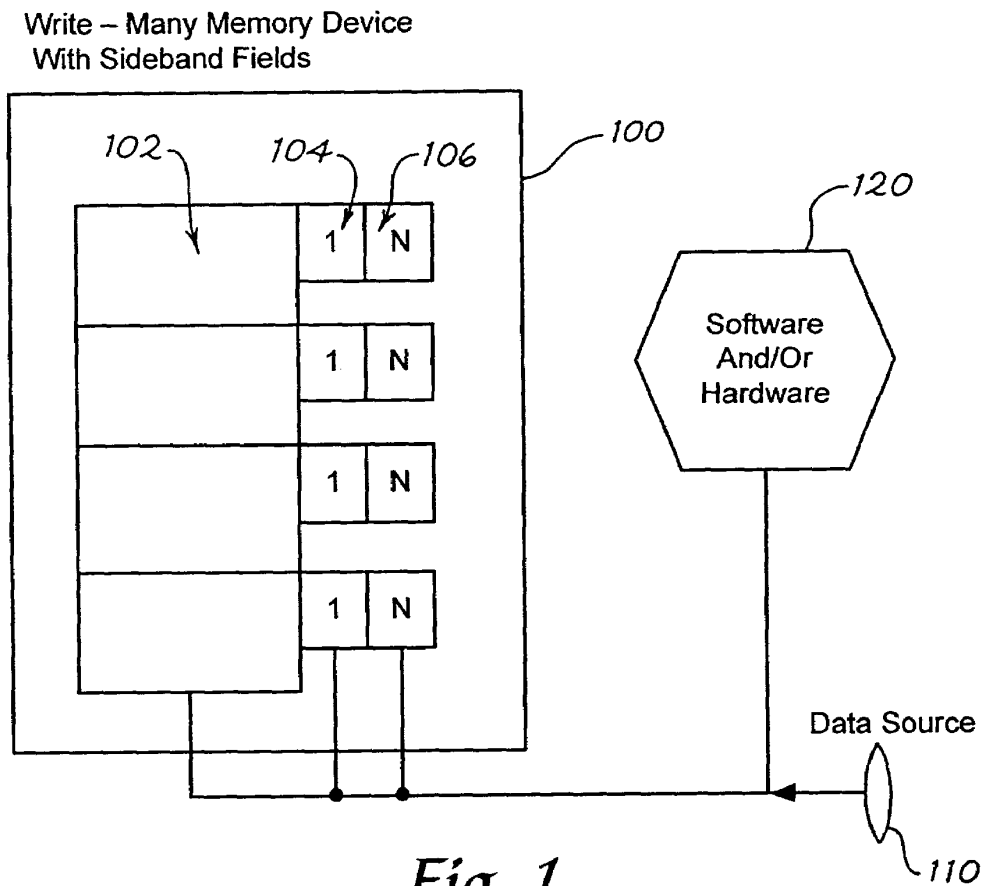


Fig. 1

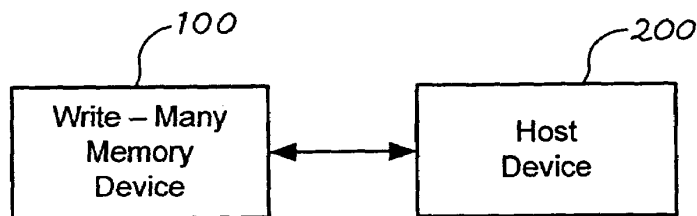


Fig. 2

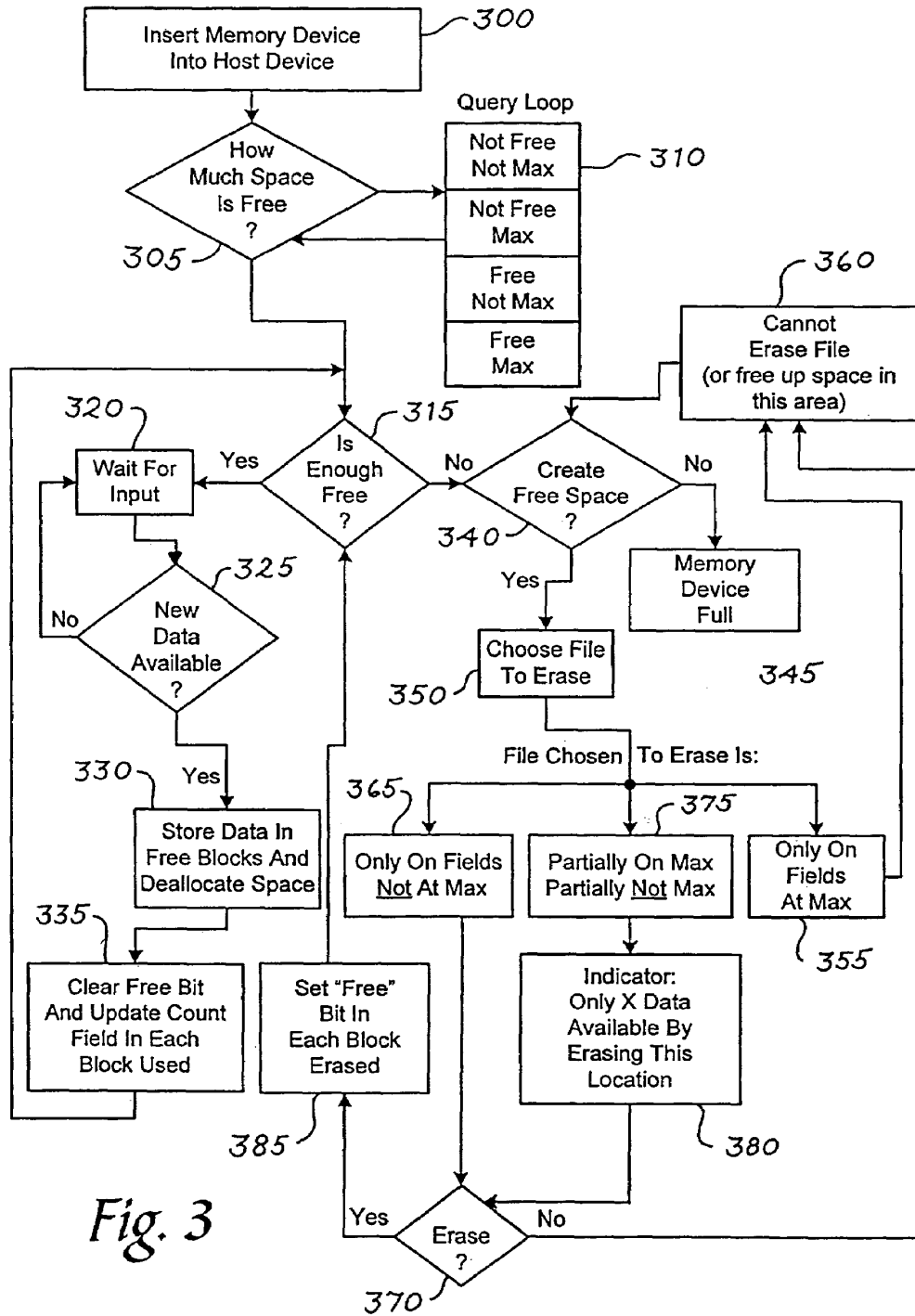


Fig. 3

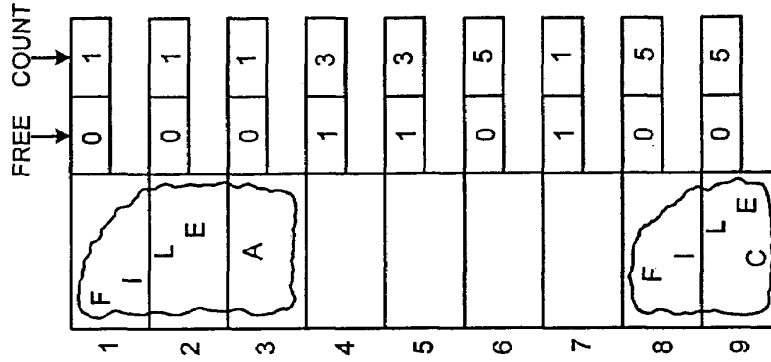


Fig. 4A

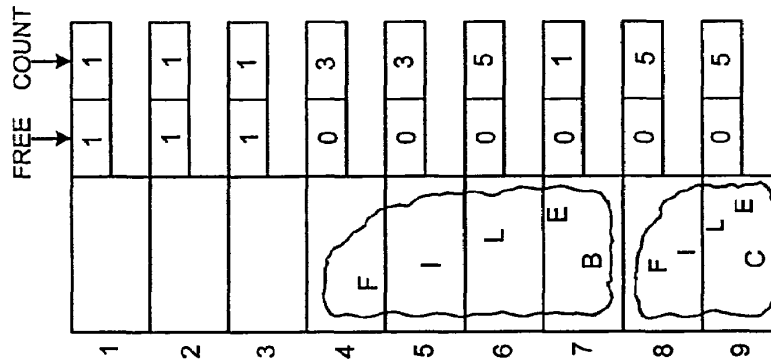


Fig. 4B

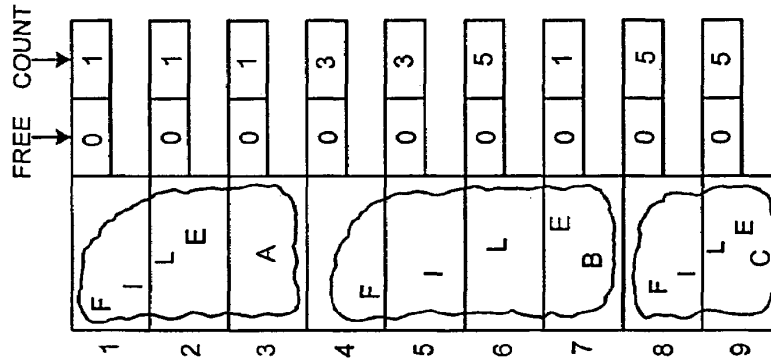


Fig. 4C

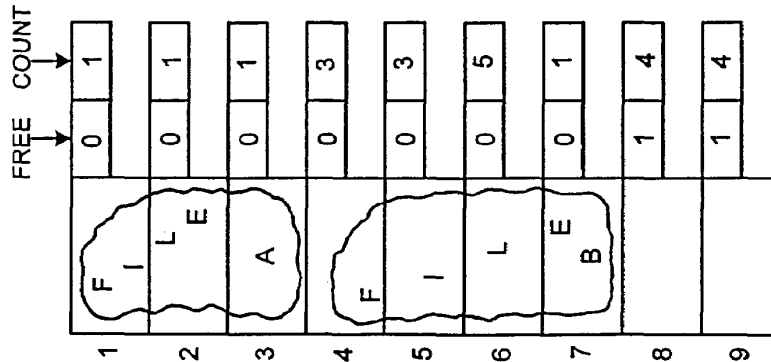


Fig. 4D

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