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Kirschner et al.

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(45) **Date of Patent: *Aug. 30, 2011**

(54) **SYSTEMS AND METHODS FOR EFFICIENT UNCORRECTABLE ERROR DETECTION IN FLASH MEMORY**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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Related U.S. Application Data

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(51) **Int. Cl.**
G11C 29/00 (2006.01)

(52) **U.S. Cl.** **714/763**

(58) **Field of Classification Search** 714/763
See application file for complete search history.

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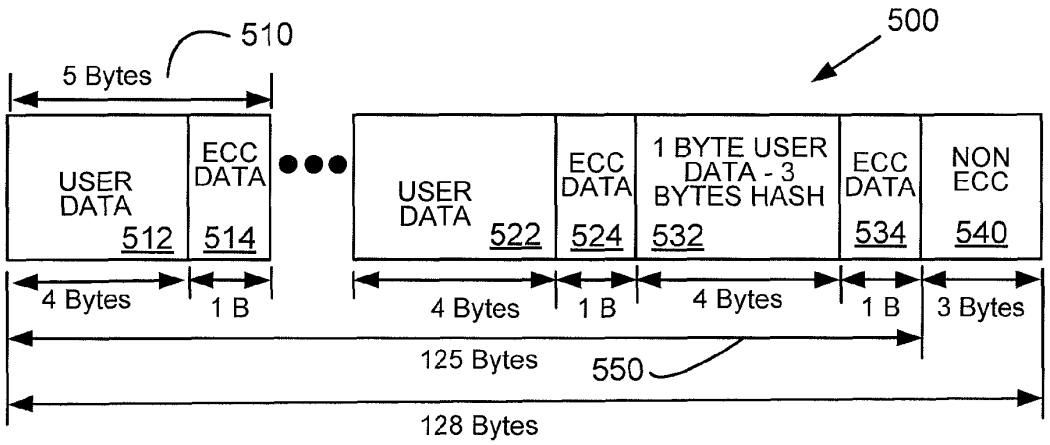
(57) **ABSTRACT**

A system and method for efficient uncorrectable error detection in flash memory is described. A microcontroller including a non-volatile flash memory utilizes an Error Correction Code (ECC) having a certain error detection and correction bit strength. The user data is first processed by a hash function and hash data is stored with the user data. Then, the user data and hash data are processed by the ECC system. In detection, the hash ensures that a relatively low bit-strength ECC system did not incorrectly manipulate the user data. Such a hash integrity check provides an efficient, robust detection of incorrectly corrected user data resulting from errors beyond the correction but strength of the ECC system utilized.

20 Claims, 4 Drawing Sheets



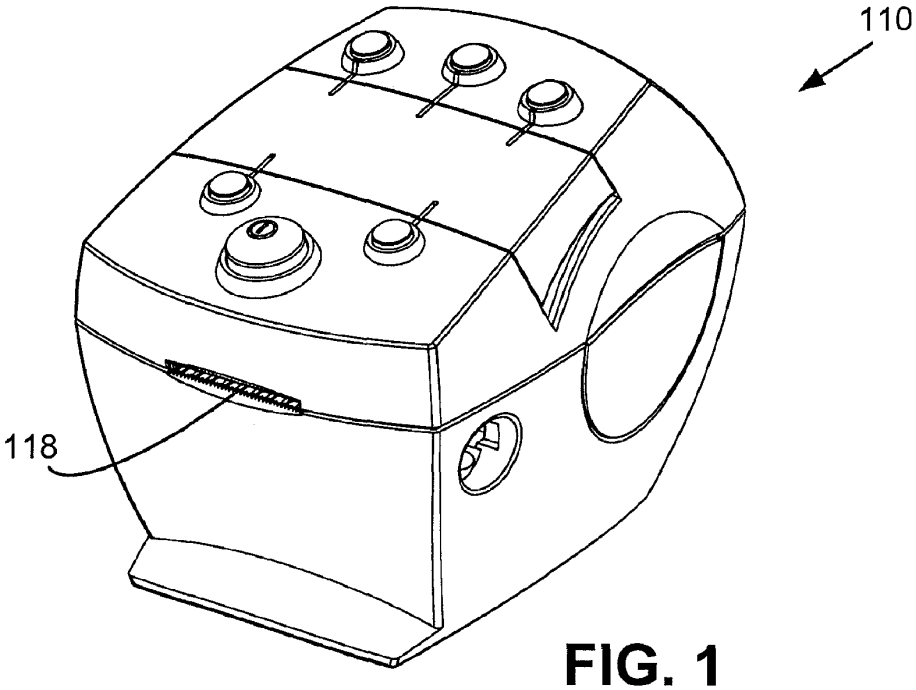


FIG. 1

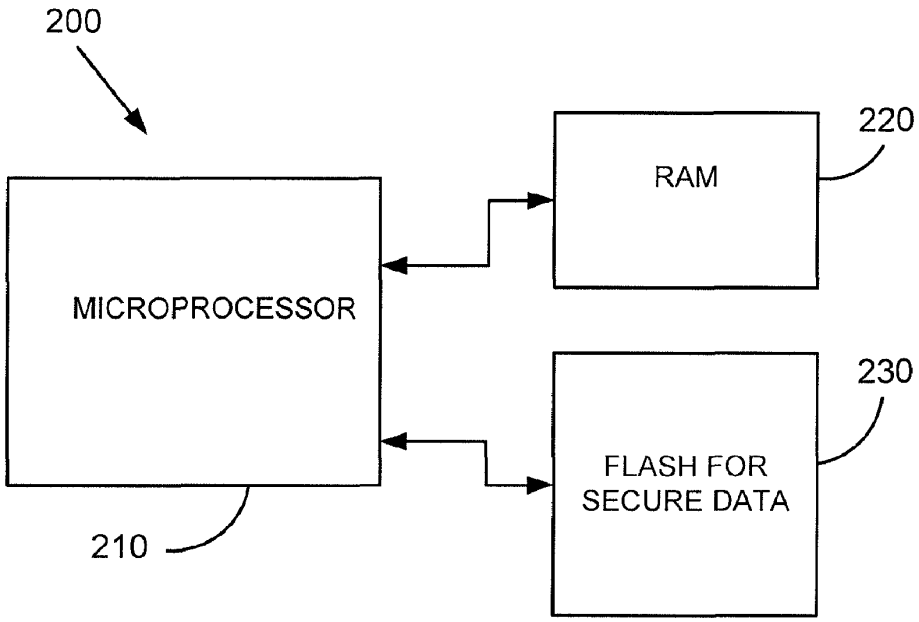


FIG. 2

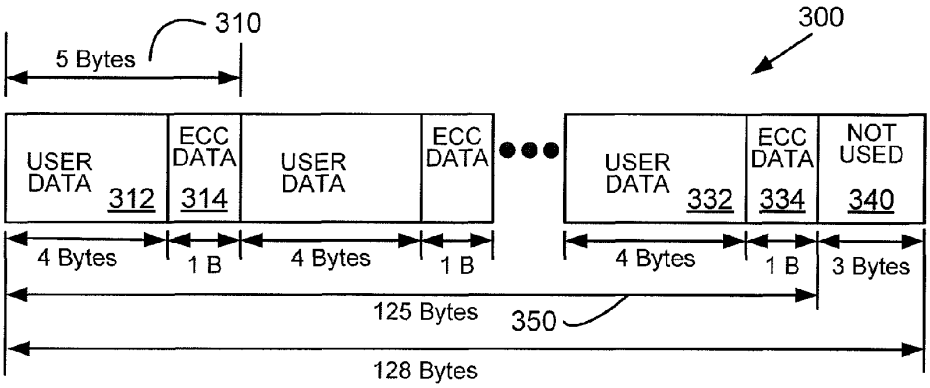


FIG. 3

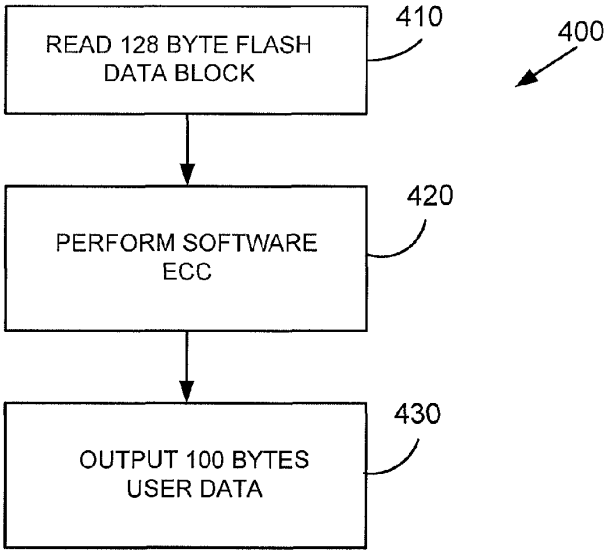


FIG. 4

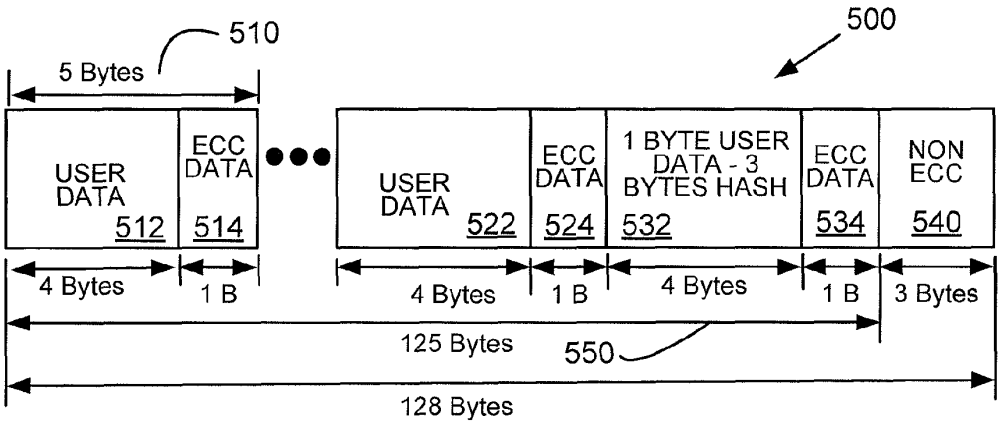


FIG. 5

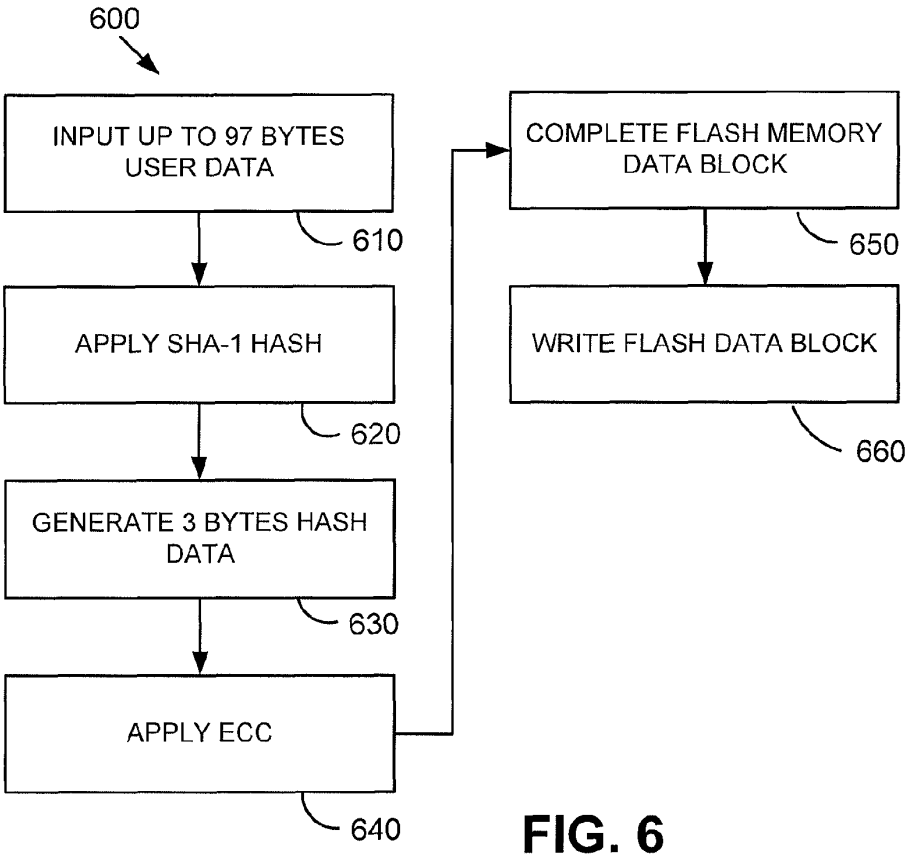


FIG. 6

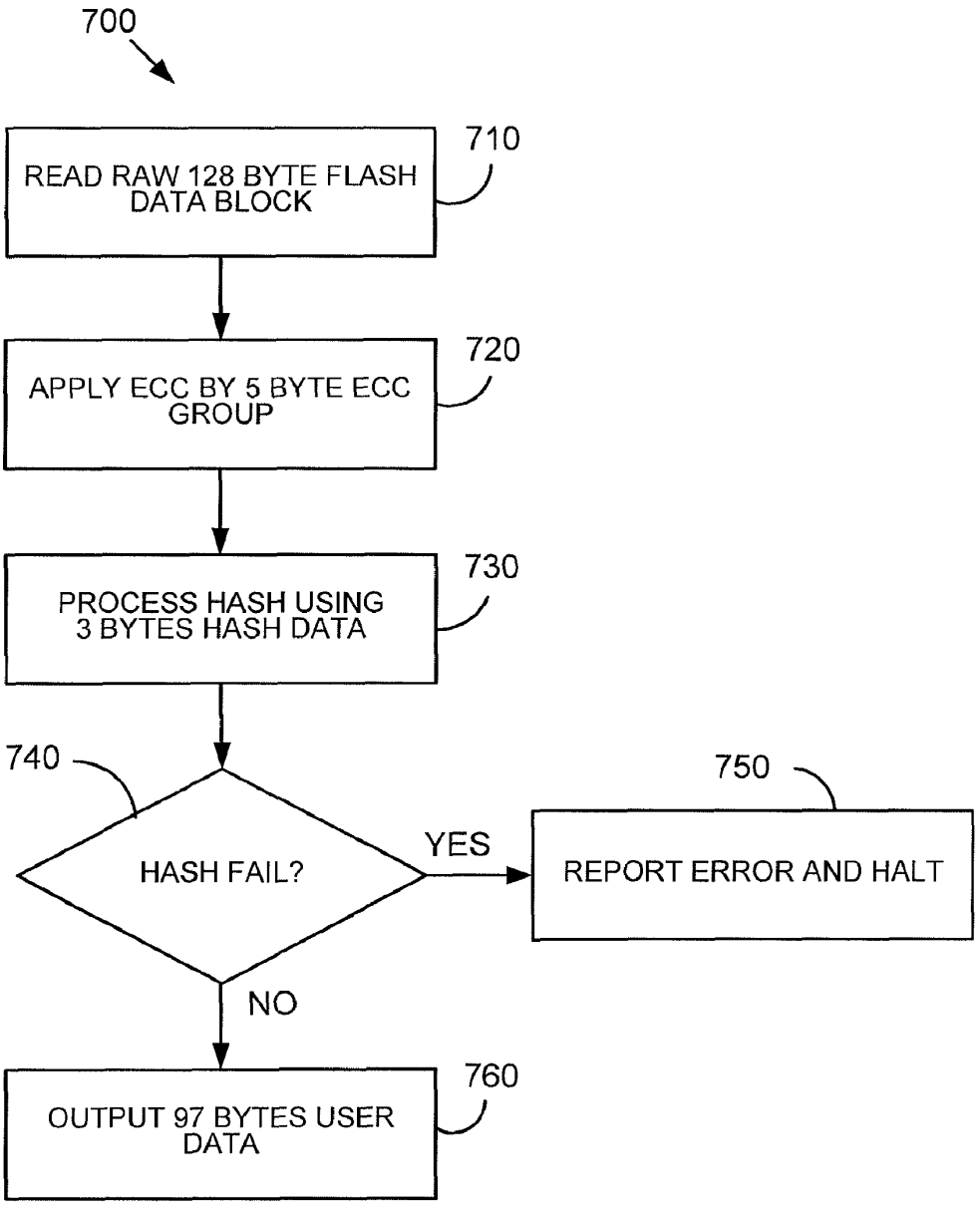


FIG. 7

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