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United States Patent [19]

Sartore et al.

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[54] **ENHANCED DRAM WITH SINGLE ROW SRAM CACHE FOR ALL DEVICE READ OPERATIONS**

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[73] Assignee: **Ramtron International Corporation**, Colorado Springs, Colo.

[*] Notice: The term of this patent shall not extend beyond the expiration date of Pat. No. 5,699,317.

[21] Appl. No.: **460,665**

[22] Filed: **Jun. 2, 1995**

Related U.S. Application Data

[63] Continuation of Ser. No. 319,289, Oct. 6, 1994, which is a continuation-in-part of Ser. No. 824,211, Jan. 22, 1992, abandoned.

[51] **Int. Cl.**[6] **G06F 12/00**

[52] **U.S. Cl.** **395/445**; 365/189.04; 365/189.05

[58] **Field of Search** 395/445, 433; 365/189.02, 189.03, 189.04, 189.05, 230.08, 230.06, 230.02, 49

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[57] **ABSTRACT**

An enhanced DRAM contains embedded row registers in the form of latches. The row registers are adjacent to the DRAM array, and when the DRAM comprises a group of subarrays, the row registers are located between DRAM subarrays. When used as on-chip cache, these registers hold frequently accessed data. This data corresponds to data stored in the DRAM at a particular address. When an address is supplied to the DRAM, it is compared to the address of the data stored in the cache. If the addresses are the same, then the cache data is read at SRAM speeds. The DRAM is decoupled from this read. The DRAM also remains idle during this cache read unless the system opts to precharge or refresh the DRAM. Refresh or precharge occur concurrently with the cache read. If the addresses are not the same, then the DRAM is accessed and the embedded register is reloaded with the data at that new DRAM address. Asynchronous operation of the DRAM is achieved by decoupling the row registers from the DRAM array, thus allowing the DRAM cells to be precharged or refreshed during a read of the row register. Additionally, the row registers/memory cache is sized to contain a row of data of the DRAM array. Furthermore, a single column decoder addresses corresponding locations in both the memory cache and the DRAM array. And finally, all reads are only from the memory cache.

36 Claims, 5 Drawing Sheets

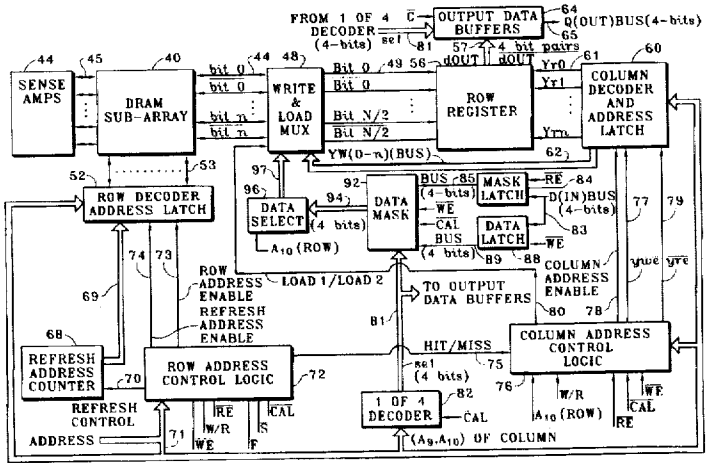

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FIG. 1
PRIOR ART

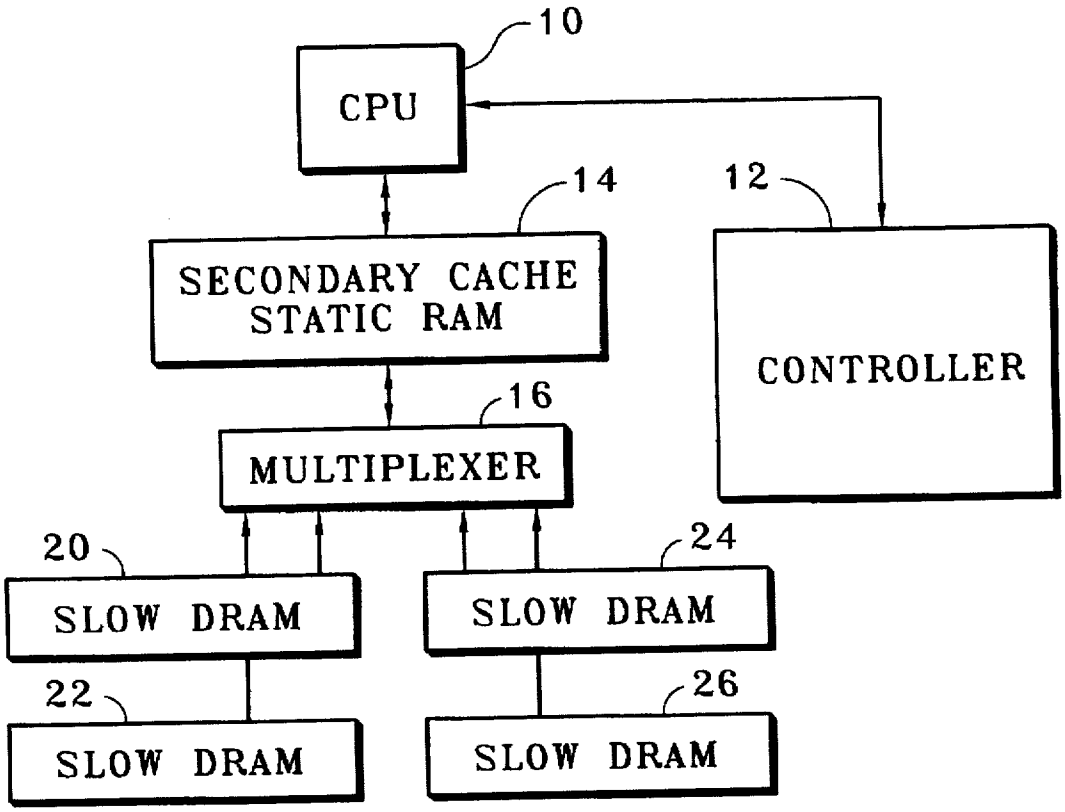
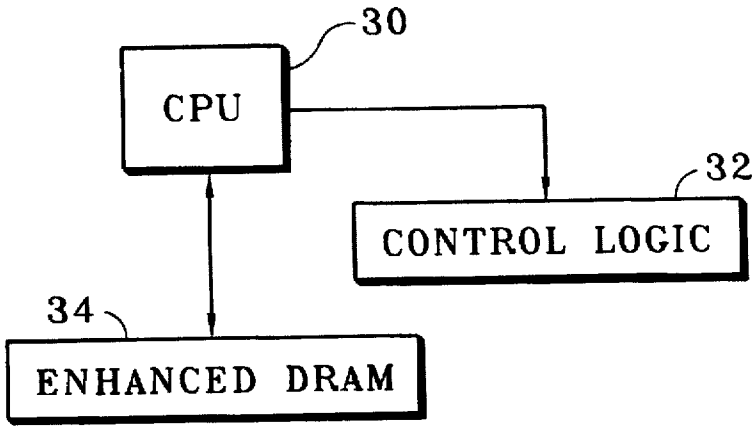
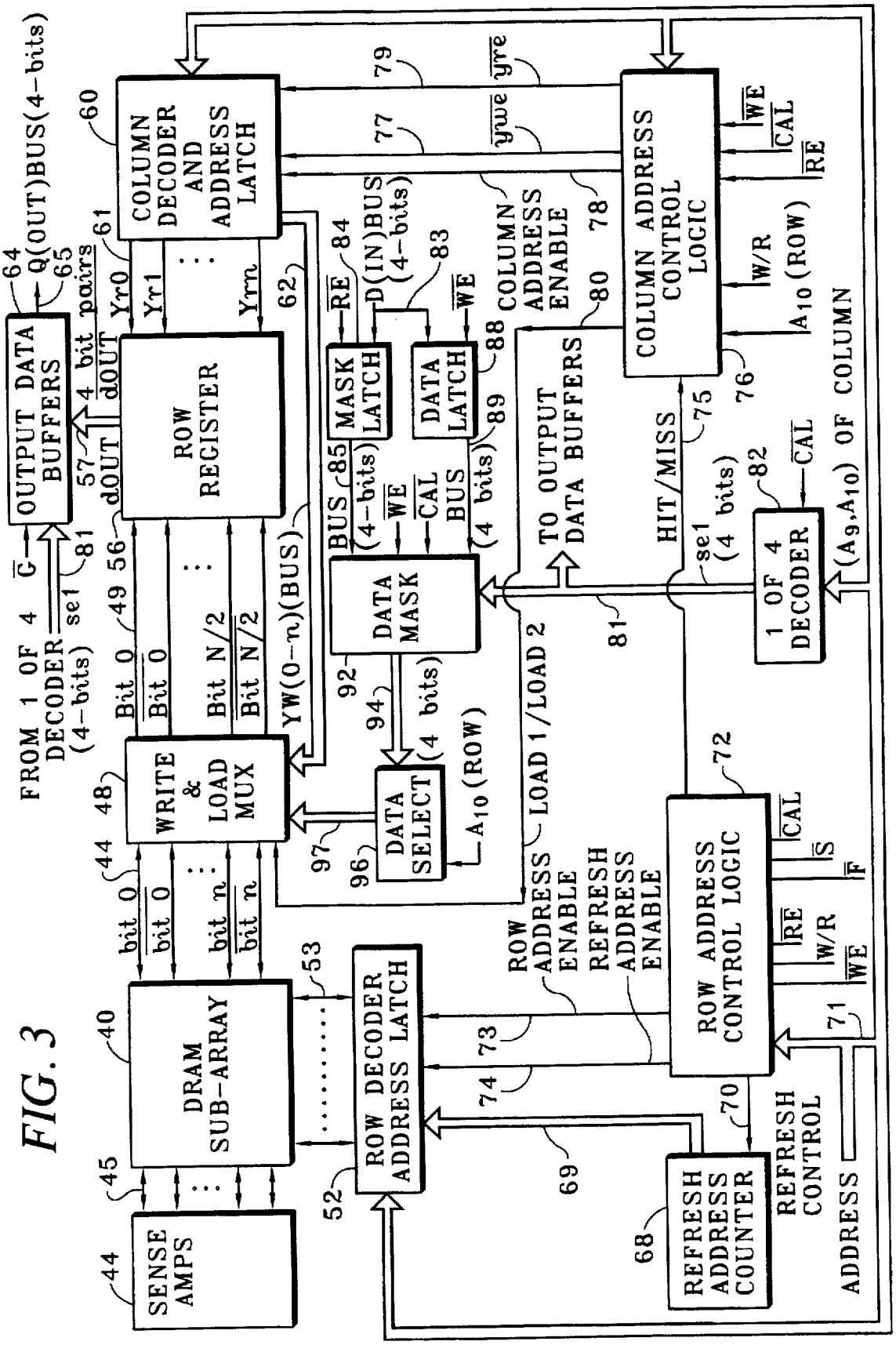


FIG. 2





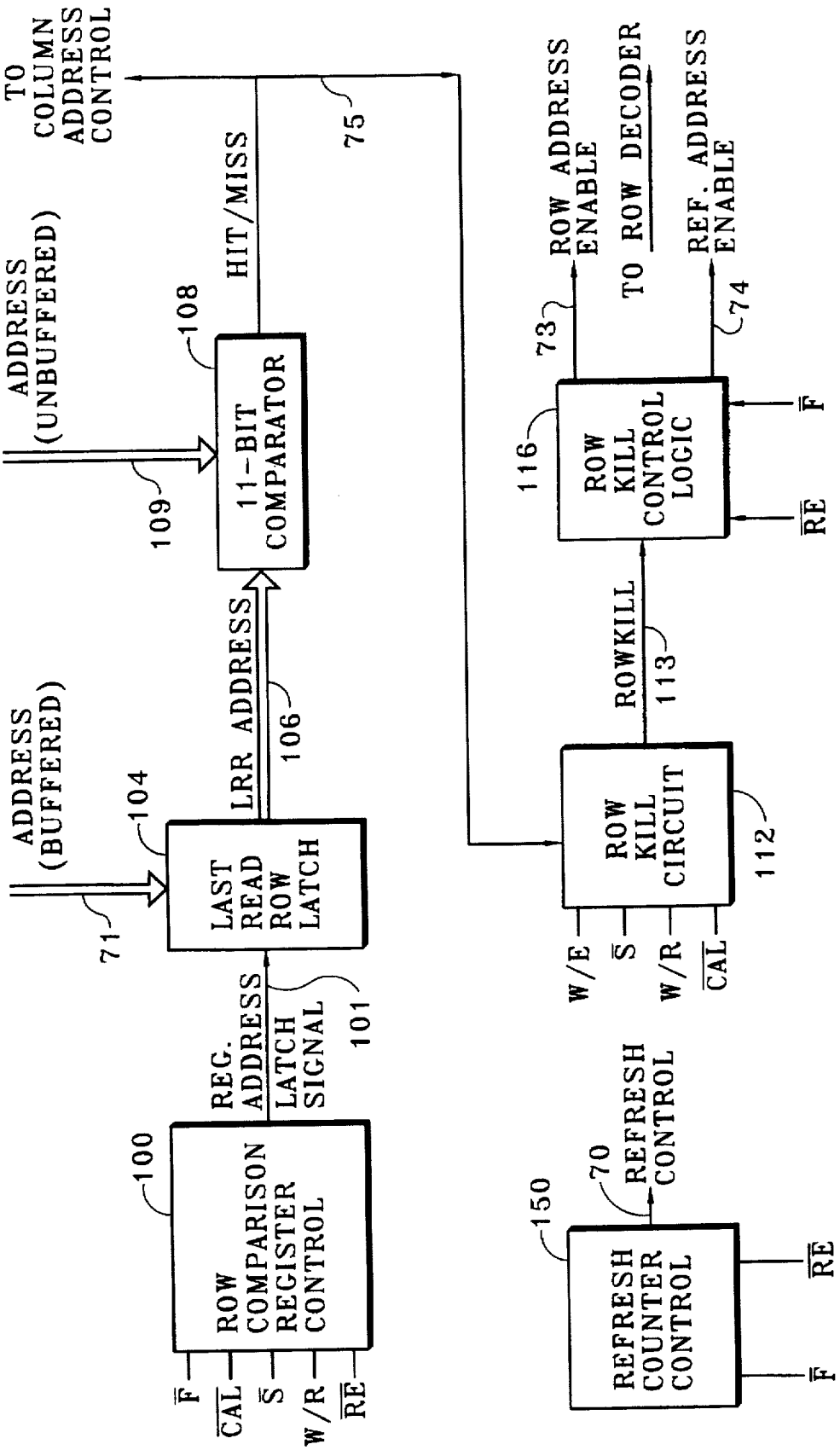


FIG. 4

ROW ADDRESS CONTROL LOGIC

DOCKET ALARM

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