

**UNITED STATES PATENT AND TRADEMARK OFFICE**

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**BEFORE THE PATENT TRIAL AND APPEAL BOARD**

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MICRON TECHNOLOGY, INC.,  
Petitioner,

v.

VERVAIN, LLC,  
Patent Owner.

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IPR2021-01550  
U.S. Patent No. 10,950,300

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**DECLARATION OF SUNIL P. KHATRI  
IN SUPPORT OF PATENT OWNER'S RESPONSE**

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Declaration of Sunil P. Khatri, Ph. D.  
IPR2021-01550  
U.S. Patent No. 10,950,300

## **DECLARATION OF SUNIL P. KHATRI, PH. D**

I, Sunil P. Khatri, do hereby declare as follows:

### **I. INTRODUCTION**

1. I have been retained on behalf of Vervain, LLC (“Vervain”), and its counsel, McKool Smith, P.C., as an expert in this proceeding. I am personally knowledgeable about the matters stated herein and am competent to make this declaration.

2. I understand that Vervain will submit this Declaration in connection with the Patent Owner’s Response in IPR2021-01550, which I have been informed is an *inter partes* review (IPR) proceeding challenging the patentability of certain claims of U.S. Patent No. 10,950,300 (“the ’300 patent” or “the challenged patent”).

3. I receive compensation at an hourly rate of \$700 per hour for my time working on this matter, plus expenses. I have no financial interest in Vervain or in the patents involved in this litigation, and my compensation is not dependent on the outcome of this litigation. The conclusions I present are due to my own judgment.

### **II. BACKGROUND AND QUALIFICATIONS**

4. I have over thirty-five years of experience with electronics, electrical engineering, and computer engineering. A copy of my latest curriculum vitae (CV), which I understand was submitted previously as part of my prior declaration in this

Declaration of Sunil P. Khatri, Ph. D.

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proceeding (Exhibit 2001, Appendix A), provides further details regarding my background and qualifications. During my career, I have acquired extensive knowledge and experience with VLSI circuits, computer architecture, testing, computer-aided design (CAD) algorithms and algorithm acceleration, logic synthesis, semiconductor memory, redundancy, synchronous and asynchronous circuits, and related software and hardware topics. Most relevant to the challenged patents, my technical expertise includes extensive work with semiconductor memory devices such as DRAM, SRAM and flash. My work with semiconductor memory devices has included work on 3D integration and novel ring-based memory architectures, power and speed tradeoffs using selective body bias, architectures and circuit approaches for processing-in-memory, radiation hardening analysis for memories, the use of flash transistors for designing logic circuits (such as ternary Content-addressable Memories (CAMs), Field Programmable Gate Arrays (FPGAs), convolutional neural networks (CNNs) for machine learning (ML), low drop-out (LDO) voltage regulators, digital to analog converters (DACs), and traditional binary-valued as well as ternary-valued general-purpose digital logic), and clocking and source-synchronous design. I recently was awarded a research grant by the Air Force Research Laboratory (AFRL) in Rome, NY, to conduct research in secure digital circuits using flash-based digital design approaches.

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