EXHIBIT D-18
INVALIDITY CLAIM CHART FOR THE '300 PATENT
BASED ON U.S. PATENT APPLICATION PUB. NO. 2008/0140918 ("Sutardja")

U.S. Patent Application Publication No. US 2008/0140918 ("Sutardja") was filed on December 7, 2007 and published on June 12, 2008. Sutardja is prior art to the '300 patent under at least 35 U.S.C. §§ 102(a), (b), (e) (pre-AIA). The asserted claims of the '300 patent are anticipated by Sutardja expressly and/or inherently or rendered obvious, either alone or in combination with other references, as set forth in the cover pleading for Micron's Initial Invalidity Contentions and as further explained in the chart below.

This chart is based on Defendants' present understanding of Plaintiff's apparent positions as to the scope of the asserted claims. By including prior art that invalidates the claims of the patent based on Plaintiff's claim construction and infringement positions, Defendants are neither adopting nor acceding in any manner to Plaintiff's claim construction and infringement positions. Furthermore, nothing stated herein shall be treated as an admission or suggestion that Defendants agree with Plaintiff regarding either the scope of any of the asserted claims or the claim constructions Plaintiff advances in its infringement allegations or anywhere else. Nor shall anything in this chart be treated as an admission that any of Defendants' accused technology meets any limitations of the claims.

U.S. Pat. No. 10,950,300	
Claim 1	**Disclosure in Sutardja**
[1.Pre] A system for storing data comprising:	To the extent the preamble is limiting, Sutardja discloses and/or renders obvious a system for storing data. *See, e.g.,* • FIGs. 1-3 • [0012] • [0108]
[1.A.1] memory space containing volatile memory space and nonvolatile memory space	Sutardja discloses and/or renders obvious memory space containing volatile memory space and nonvolatile memory space. *See, e.g.,* • FIG. 1 • [0009] • [0108]

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	• [0172] (may include RAM and/or nonvolatile memory) • [0178] • [0181] • [0007] • [0048] • [0114] • [0142]
[1.A.2] wherein the nonvolatile memory space includes both multilevel cell (MLC) memory space and single level cell (SLC) memory space	Sutardja discloses and/or renders obvious wherein the nonvolatile memory space includes both multilevel cell (MLC) memory space and single level cell (SLC) memory space. *See, e.g.,* • [0108]
[1.B] at least one controller to operate memory elements and associated memory space	Sutardja discloses and/or renders obvious at least one controller to operate memory elements and associated memory space. *See, e.g.,* • FIGs. 1-7 • [0105]-[0107] • [0118] • [0129]-[1030]
[1.C] at least one MLC nonvolatile memory element that can be mapped into the MLC memory space	Sutardja discloses and/or renders obvious at least one MLC nonvolatile memory element that can be mapped into the MLC memory space. *See, e.g.,*

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U.S. Pat. No. 10,950,300	
	[0148] [0149] [0108] [0105]
[1.D] at least one SLC nonvolatile memory element that can be mapped into the SLC memory space	Sutardja discloses and/or renders obvious at least one SLC nonvolatile memory element that can be mapped into the SLC memory space. *See, e.g.,* [0148] [0149] [0108] [0105]
[1.E] at least one random access volatile memory	Sutardja discloses and/or renders obvious at least one random access volatile memory. *See, e.g.,* [0172] [0175] [0178] [0184] [0172] (may include RAM and/or nonvolatile memory) [0178] [0181] [0007] [0048] [0114] [0142]

U.S. Pat. No. 10,950,300	
[1.F] an FTL flash translation layer, wherein the at least one controller, or FTL, or a combination of both maintain an address table in one or more of the memory elements and random access volatile memory	Sutardja discloses and/or renders obvious an FTL flash translation layer, wherein the at least one controller, or FTL, or a combination of both maintain an address table in one or more of the memory elements and random access volatile memory. *See, e.g.,* • [0042] • [0105] • [0118] • [0149] • [0150] • FIG. 7C • [0011]-[0012] (controller performs logical to physical mapping) • [0047] • [0107]
[1.G.i] the controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory for storage of data therein	Sutardja discloses and/or renders obvious the controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory for storage of data therein. *See, e.g.,* • [0042] • [0105]-[0108] • [0118] • [0129]-[0130] • [0149] • [0150] • FIG. 7C

U.S. Pat. No. 10,950,300	
[1.G.ii] the controller, in at least a Write access operation to the MLC nonvolatile memory element, operable to store data in the MLC nonvolatile memory element and retain such stored data in the random access volatile memory	Sutardja discloses and/or renders obvious the controller, in at least a Write access operation to the MLC nonvolatile memory element, operable to store data in the MLC nonvolatile memory element and retain such stored data in the random access volatile memory. *See, e.g.,* • [0048] • [0074] (caching data) • [0142]
[1.H] the controller performing a data integrity test on stored data in the MLC nonvolatile memory element after at least a Write access operation performed thereon by comparing the stored data to the retained data in the random access volatile memory	Sutardja discloses and/or renders obvious the controller performing a data integrity test on stored data in the MLC nonvolatile memory element after at least a Write access operation performed thereon by comparing the stored data to the retained data in the random access volatile memory. *See, e.g.,* • [0134]-[0138] (degradation module)
[1.I] wherein the address table maps logical and physical addresses adaptable to the system, wherein the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories; and	Sutardja discloses and/or renders obvious wherein the address table maps logical and physical addresses adaptable to the system, wherein the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories. *See, e.g.,* • [0139] • [0011] (mapping based on wear levels) • [0102]

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