EXHIBIT D-3
INVALIDITY CLAIM CHART FOR THE '300 PATENT
BASED ON U.S. PATENT APPLICATION PUB. NO. 2011/009460 ("Dusija")

U.S. Patent Application Publication No. 2011/0099460 ("Dusija") was filed on December 18, 2009 and published on April 28, 2011. Dusija is prior art to the '300 patent under at least 35 U.S.C. §§ 102(a), (e) (pre-AIA). The asserted claims of the '300 patent are anticipated by Dusija expressly and/or inherently or rendered obvious, either alone or in combination with other references, as set forth in the cover pleading for Micron's Initial Invalidity Contentions and as further explained in the chart below.

This chart is based on Defendants' present understanding of Plaintiff's apparent positions as to the scope of the asserted claims. By including prior art that invalidates the claims of the patent based on Plaintiff's claim construction and infringement positions, Defendants are neither adopting nor acceding in any manner to Plaintiff's claim construction and infringement positions. Furthermore, nothing stated herein shall be treated as an admission or suggestion that Defendants agree with Plaintiff regarding either the scope of any of the asserted claims or the claim constructions Plaintiff advances in its infringement allegations or anywhere else. Nor shall anything in this chart be treated as an admission that any of Defendants' accused technology meets any limitations of the claims.

U.S. Pat. No. 10,950,300	
Claim 1	**Disclosure in Dusija**
[1.Pre] A system for storing data comprising:	To the extent the preamble is limiting, Dusija discloses and/or renders obvious a system for storing data. *See, e.g.*, • [0059] • FIG. 1
[1.A.1] memory space containing volatile memory space and nonvolatile memory space	Dusija discloses and/or renders obvious memory space containing volatile memory space and nonvolatile memory space. *See, e.g.*, • FIG. 1 • [0059] • [0068] • [0111]–[0117]

U.S. Pat. No. 10,950,300	
	• [0062] • [0020]-[0023] (cache) *See also* Claim limitation [1.A.2] and accompanying citations.
[1.A.2] wherein the nonvolatile memory space includes both multilevel cell (MLC) memory space and single level cell (SLC) memory space	Dusija discloses and/or renders obvious wherein the nonvolatile memory space includes both multilevel cell (MLC) memory space and single level cell (SLC) memory space. *See, e.g.*, • FIG. 14B • [0109]
[1.B] at least one controller to operate memory elements and associated memory space	Dusija discloses and/or renders obvious at least one controller to operate memory elements and associated memory space. *See, e.g.*, • FIG. 1 • [0060] • [0062] • [0117] *See also* Claim limitations [1.A.1-2] and accompanying citations.
[1.C] at least one MLC nonvolatile memory element that can be mapped into the MLC memory space	Dusija discloses and/or renders obvious at least one MLC nonvolatile memory element that can be mapped into the MLC memory space. *See, e.g.*,

U.S. Pat. No. 10,950,300	
	• [0059] • [0060] • [0117] • [0120] • FIG. 14B *See also* Claim limitation [1.A.2] and accompanying citations.
[1.D] at least one SLC nonvolatile memory element that can be mapped into the SLC memory space	Dusija discloses and/or renders obvious at least one SLC nonvolatile memory element that can be mapped into the SLC memory space. *See, e.g.*, • [0117] • [0129] • [0059] • [0109] • [0120] *See also* Claim limitations [1.A.2, 1.C] and accompanying citations.
[1.E] at least one random access volatile memory	Dusija discloses and/or renders obvious at least one random access volatile memory. *See, e.g.*, • FIG. 1 • [0059] • [0068] • [0111]–[0117] • [0062]

U.S. Pat. No. 10,950,300	
	• [0020]-[0023] (cache) *See also* Claim limitation [1.A.1] and accompanying citations.
[1.F] an FTL flash translation layer, wherein the at least one controller, or FTL, or a combination of both maintain an address table in one or more of the memory elements and random access volatile memory	Dusija discloses and/or renders obvious an FTL flash translation layer, wherein the at least one controller, or FTL, or a combination of both maintain an address table in one or more of the memory elements and random access volatile memory. *See, e.g.*, • [0017] • [0059] • [0060] • [0117] *See also* Claim limitation [1.A.1] and accompanying citations.
[1.G.i] the controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory for storage of data therein	Dusija discloses and/or renders obvious the controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory for storage of data therein. *See, e.g.*, • FIG. 1 • [0059] • [0060] • [0117] *See also* Claim limitation [1.A.1] and accompanying citations.
[1.G.ii] the controller, in at	Dusija discloses and/or renders obvious the controller, in at least a Write access operation to the MLC

U.S. Pat. No. 10,950,300	
least a Write access operation to the MLC nonvolatile memory element, operable to store data in the MLC nonvolatile memory element and retain such stored data in the random access volatile memory	nonvolatile memory element, operable to store data in the MLC nonvolatile memory element and retain such stored data in the random access volatile memory. *See, e.g.*, • [0060] • [0111]-[0116] • [0119]-[0124] *See also* Claim limitation [1.A.1] and accompanying citations.
[1.H] the controller performing a data integrity test on stored data in the MLC nonvolatile memory element after at least a Write access operation performed thereon by comparing the stored data to the retained data in the random access volatile memory	Dusija discloses and/or renders obvious the controller performing a data integrity test on stored data in the MLC nonvolatile memory element after at least a Write access operation performed thereon by comparing the stored data to the retained data in the random access volatile memory. *See, e.g.*, • FIG. 1 • [0062] • [0111]-[0116] • [0119]-[0124] • [0203] *See also* Claim limitation [1.G.2] and accompanying citations.
[1.I] wherein the address table maps logical and physical addresses adaptable to the system, wherein the mapping is performed as necessitated	Dusija discloses and/or renders obvious wherein the address table maps logical and physical addresses adaptable to the system, wherein the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories.

DOCKET ALARM

Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

Real-Time Litigation Alerts

Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

Advanced Docket Research

With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

Analytics At Your Fingertips

Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

LAW FIRMS
Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

FINANCIAL INSTITUTIONS
Litigation and bankruptcy checks for companies and debtors.

E-DISCOVERY AND LEGAL VENDORS
Sync your system to PACER to automate legal marketing.