

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner

v.

VERVAIN, LLC,
Patent Owner

Case No.: IPR2021-01549
U.S. Patent No. 9,997,240
Original Issue Date: June 12, 2018

Title: LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM

DECLARATION OF DR. DAVID LIU

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3.	Claim 6.....	91
	a.	[6.PRE] “A system for storing data comprising:”91
	b.	[6.A] “at least one MLC non-volatile memory module comprising a plurality of individually erasable blocks;”91
	c.	[6.B] “at least one SLC non-volatile memory module comprising a plurality of individually erasable blocks”92
	d.	[6.C] “a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module”92
	e.	[6.D.i] “the controller maintaining an address map of at least one of the MLC and SLC non-volatile memory modules, the address map comprising a list of logical address ranges accessible by a computer system, [6.D.ii] the list of logical address ranges having a minimum quanta of addresses, [6.D.iii] wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non- volatile memory module or within the at least one MLC non-volatile memory module;”92

f. [6.E] “wherein the controller allocates those blocks that receive frequent writes into the SLC non-volatile memory module as hot blocks and those blocks that only receive infrequent writes into the MLC non-volatile memory module as cold blocks; and”93

g. [6.F] “wherein the controller is adapted to determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory module, fails a data integrity test, and in the event of such a failure, the controller remaps the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module;”94

h. [6.G.i] “wherein the controller is further adapted to maintain a count value of those blocks that are accessed most frequently, and [6.G.ii] and, on a periodic basis when the count value is a predetermined count value, transfer the contents of those counted blocks into the SLC non-volatile memory module, [6.G.iii] wherein the counted blocks transferred to after reaching the predetermined count value are determined in accordance with the next equivalent range of physical addresses determined by the controller.”94

4. Claim 7: “The system of claim 6, wherein the MLC and SLC each comprise flash memories.”.....96

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C. Ground 2: Dusija, Sutardja, And Chin In View Of The Knowledge Of A POSA Renders Obvious Claims 1-2 and 6-7 Of The 240 Patent.....99

- a. [1.G] “[1.G.i] maintain a count value of the blocks in the MLC non-volatile memory module determined to have received frequent writes and that are accessed most frequently [1.G.ii] on a periodic basis when the count value is a predetermined count value transfer the contents of the counted blocks in the MLC non-volatile memory module determined to have received frequent writes after reaching the predetermined count value to the SLC non-volatile memory module and [1.G.iii] which determined blocks in the SLC are determined in accordance with the next equivalent range of physical addresses determined by the controller.”100
- a. [6.G.i] “wherein the controller is further adapted to maintain a count value of those blocks that are accessed most frequently, and [6.G.ii] and, on a periodic basis when the count value is a predetermined count value, transfer the contents of those counted blocks into the SLC non-volatile memory module, [6.G.iii] wherein the counted blocks transferred to after reaching the predetermined count value are determined in accordance with the next equivalent range of physical addresses determined by the controller.”106

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