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Rao

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(54) **LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM**

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This patent is subject to a terminal disclaimer.

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G11C 16/04 (2006.01)
G11C 11/56 (2006.01)
(Continued)

(52) **U.S. Cl.**
CPC ***G11C 11/5635*** (2013.01); ***G06F 11/1068*** (2013.01); ***G06F 11/1072*** (2013.01);
(Continued)

(58) **Field of Classification Search**
CPC G11C 11/5621; G11C 2211/5641; G11C 2029/1806; G11C 29/50004; G11C 29/76;
(Continued)

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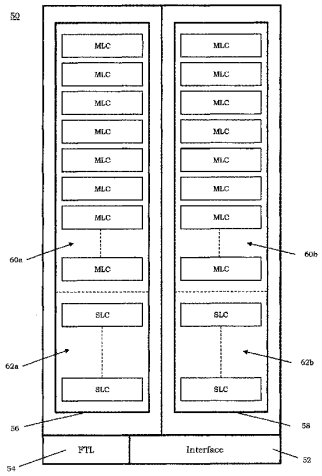
(57) **ABSTRACT**

A controller for managing at least one MLC non-volatile memory module and at least one SLC non-volatile memory module. The flash controller is adapted to determine if a range of addresses listed by an entry and mapped to said at least one MLC non-volatile memory module fails a data integrity test. In the event of such a failure, the controller remaps said entry to an equivalent range of addresses of said at least one SLC non-volatile memory module. The flash controller is further adapted to determine which of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently and allocating those blocks that receive frequent writes to the SLC non-volatile memory module and those blocks that receive infrequent writes to the MLC non-volatile memory module.

10 Claims, 5 Drawing Sheets



Related U.S. Application Data

division of application No. 13/455,267, filed on Apr. 25, 2012, now Pat. No. 8,891,298.

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G06F 11/10	(2006.01)
G11C 29/52	(2006.01)
G11C 29/00	(2006.01)
G11C 16/16	(2006.01)

(52) **U.S. Cl.**

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(58) **Field of Classification Search**

CPC . G11C 29/765; G06F 11/1068; G06F 11/1072

See application file for complete search history.

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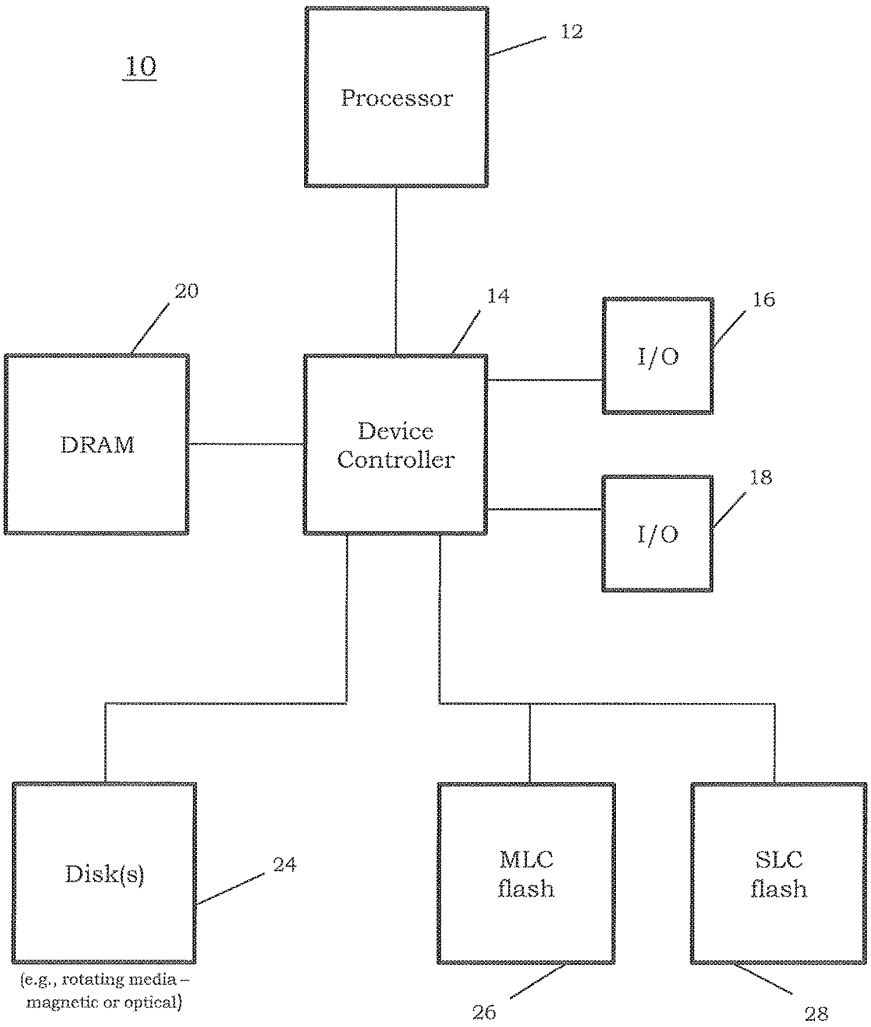

FIG. 1

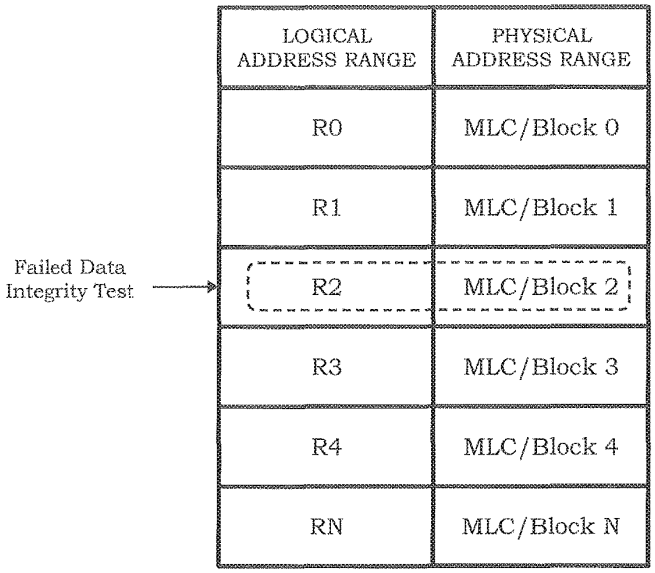

FIG. 2A

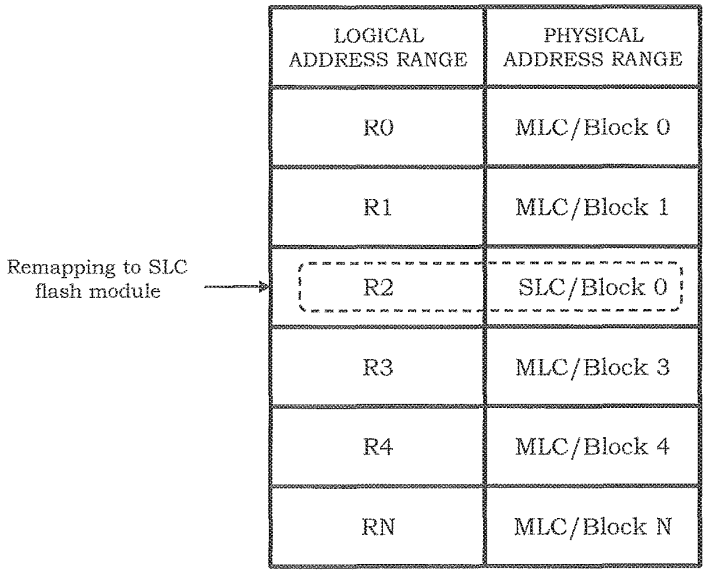

FIG. 2B

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