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(12) United States Patent

Rao

(54) LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM

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(57) **ABSTRACT**

A flash controller for managing at least one MLC non-volatile memory module and at least one SLC non-volatile memory module. The flash controller is adapted to determine if a range of addresses listed by an entry and mapped to said at least one MLC non-volatile memory module fails a data integrity test. In the event of such a failure, the controller remaps said entry to an equivalent range of addresses of said at least one SLC non-volatile memory module. The flash controller is further adapted to determine which of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently and allocating those blocks that receive frequent writes to the SLC non-volatile memory module and those blocks that receive infrequent writes to the MLC non-volatile memory module.

11 Claims, 5 Drawing Sheets



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<u>FIG. 1</u>

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	LOGICAL ADDRESS RANGE	PHYSICAL ADDRESS RANGE	
	RO	MLC/Block 0	
Failed Data Integrity Test	R1	MLC/Block 1	
	R2	MLC/Block 2	
	R3	MLC/Block 3	
	R4	MLC/Block 4	
	RN	MLC/Block N]

<u>FIG. 2a</u>





<u>FIG. 3a</u>

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