

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,

Petitioner,

v.

VERVAIN, LLC,

Patent Owner.

Case No.: IPR2021-01547

U.S. Patent No. 8,891,298

Original Issue Date: November 18, 2014

Title: LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM

**PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 8,891,298
PURSUANT TO 35 U.S.C. §§ 311-319 and 37 C.F.R. § 42**

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 b. [1.A] “at least one MLC non-volatile memory module
 comprising a plurality of individually erasable blocks;” 29

 c. [1.B] “at least one SLC non-volatile memory module
 comprising a plurality of individually erasable blocks; and” 31

 d. [1.C] “a controller coupled to the at least one MLC non-
 volatile memory module and the at least one SLC non-
 volatile memory module wherein the controller is adapted
 to:” 33

 e. [1.D] “maintain an address map of at least one of the MLC
 and SLC non-volatile memory modules, the address map
 comprising a list of logical address ranges accessible by a
 computer system, [1.D.ii.] the list of logical address ranges
 having a minimum quanta of addresses, [1.D.iii.] wherein
 each entry in the list of logical address ranges maps to a
 similar range of physical addresses within either the at least
 one SLC non-volatile memory module or within the at least
 one MLC non-volatile memory module;” 35

f.	[1.E] “[1.E.i] determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory module, fails a data integrity test, and, [1.E.ii] in the event of such a failure, the controller remaps the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module;”	38
g.	[1.F] “determine which of the blocks of the plurality of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently by maintaining a count of the number of times each one of the blocks is accessed; and”	42
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e.	[1.D] “maintain an address map of at least one of the MLC and SLC non-volatile memory modules, the address map comprising a list of logical address ranges accessible by a computer system, the list of logical address ranges having a minimum quanta of addresses, wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory module or within the at least one MLC non-volatile memory module;”	58
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