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## (12) United States Patent

## Weathers et al.

(54) APPARATUS AND METHOD FOR MULTI-MODE OPERATION OF A FLASH MEMORY DEVICE

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- (51) Int. Cl.

None

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#### (58) Field of Classification Search

See application file for complete search history.

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#### (57) ABSTRACT

Disclosed is an apparatus and method for operating a multilevel cell (MLC) flash memory circuit. Data is read from a memory block of a plurality of memory blocks in the MLC flash memory circuit, wherein each of the plurality of memory blocks can operate in one of at least three modes of operation comprising an MLC mode, a single-level cell (SLC) mode and a defective mode, and wherein the memory block is initially operating in the MLC mode. Error correction is performed on the read data to correct read errors in the read data. A determination is made if a number of bits corrected by the error correction exceeds a predetermined threshold value. If the number of bits corrected by the error correction exceeds the predetermined threshold value, the operating mode of the memory block is switched from the MLC mode to the SLC mode.

#### 20 Claims, 4 Drawing Sheets





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